Transistor electronic technologies

•Bipolar Junction Transistor

discrete or integrated circuit

discrete = individual component

•MOS (Metal-Oxide-Silicon) Field Effect Transistor

mainly used in integrated circuits

driven by digital applications but analogue

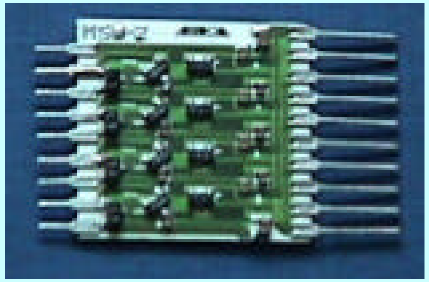
•Junction Field Effect Transistor

similar in many ways to MOS FET

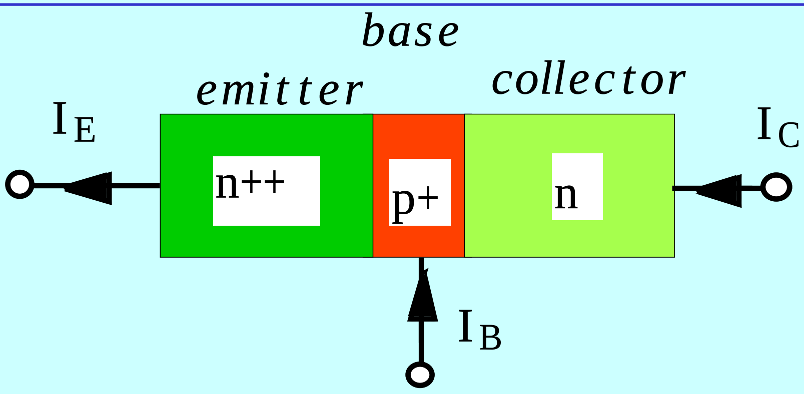
discrete, not easily implemented in ICs

•so - is this a course on circuits?

No but it is necessary to understand some basics to be able to deal with more complex elements, including some features of op-amps



Bipolar transistor



arrows show direction of current flow

- pnp or npn

  semiconductor, usually Si, but also Ge

  heavily doped emitter, lightly doped base

- Operation - npn

  base is biased more positive than emitter

  so a forward biased diode

  collector more positive than base = *reverse biased diode*

  majority carriers from emitter diffuse across base to collector

  small fraction combine with majority carriers in base

  current reaching collector is

$I_C = \alpha I_E$

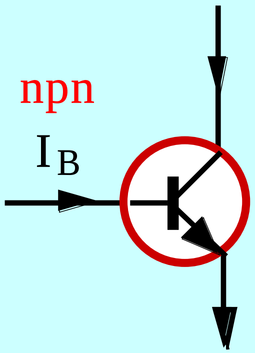
$I_B = (1-\alpha) I_E$

$I_C = \beta I_B \quad = [\alpha/(1-\alpha)] I_B$

$\beta = \alpha/(1-\alpha)$ = d.c current gain = h_{fe}

$I_E \approx I_C$

eg $\alpha = 0.99 \quad \beta = 99$



pnp transistor

- Works like npn transistor

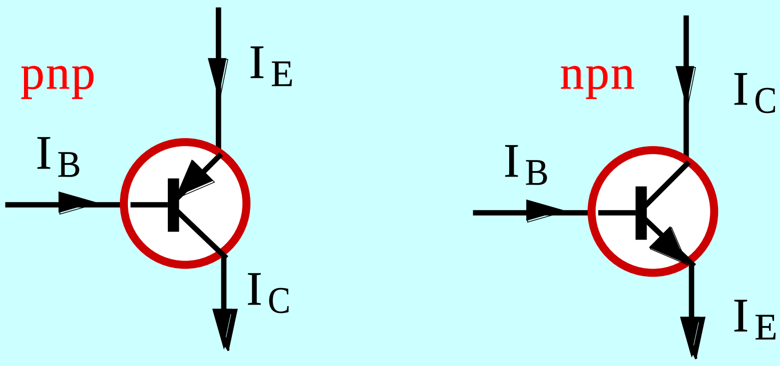
bias arrangements different

but

if emitter is positioned at top

easy to remember both pnp and npn

most positive



most negative

Slightly more precise picture

- to turn npn transistor on V_B-V_E = V_{BE} > 0.6-0.7V

  (invert for pnp)

- so we can use it as a switch by controlling V_{BE}

  $V_{BE} \approx 0$ $I_C = I_E = 0$

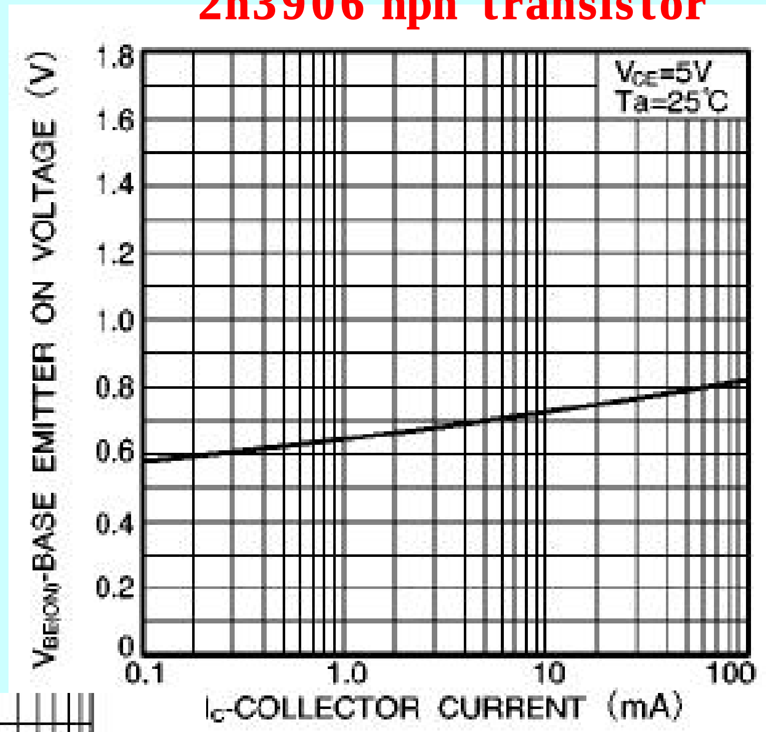
- however, if transistor is ON $V_{BE} \approx 0.7V$

  this is a consequence of the diode behaviour -

  discuss in a moment

- in contrast, β is not a reliable parameter for design

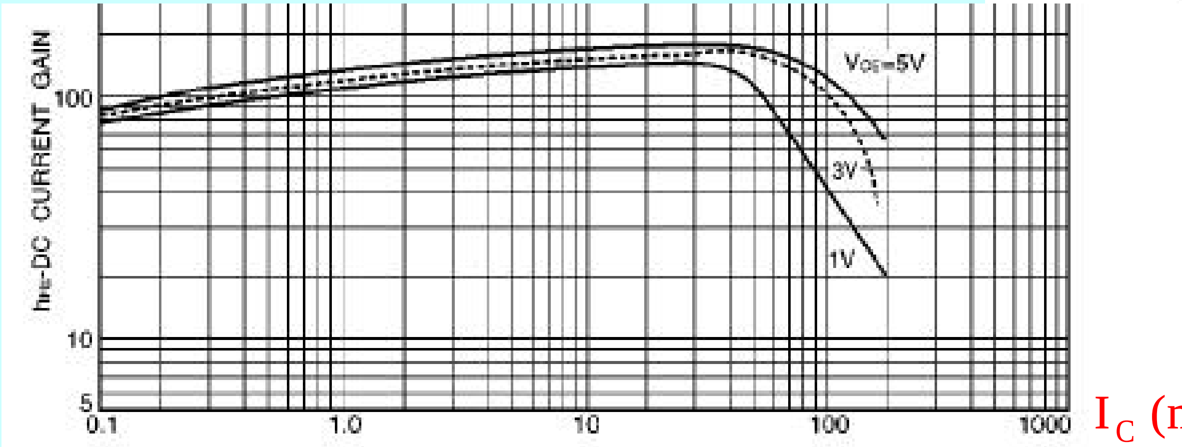
2n3906 npn transistor



NB log scale for I_C

β

NB both log scales



I_C (mA)

Ebers-Moll model

• Transistor can be modelled as two back-to-back diodes

I-V behaviour of diode $I \approx I_0[\exp(qV_{BE}/kT)-1)]$

• Base-emitter diode is forward biased

$I_E = I_{E0}.[\exp(qV_{BE}/kT)-1] \approx I_{E0}\exp(qV_{BE}/kT)$ ie $V_{BE} \approx (kT/q)\log_e I_E$

this explains why V_{BE} varies so little with I
also basis of band-gap T reference

• Base-collector diode is reverse biased

$I_{BC} = I_{CO}[\exp(qV_{BC}/kT)-1] \approx I_{C0}$ - which is small

so current arriving at collector is dominated by current from emitter, which has diffused across base

• How does current vary with small change in V_{BE}?

$dI_E/dV_{BE} = i_e/v_{be} = (q/kT)I_{E0}\exp(qV_{BE}/kT) = (q/kT)I_E$

$i_e r_e = v_{be}$ with $r_e = kT/qI = 25\Omega/I_E(mA)$

NB we don't usually need to distinguish between I_C and I_E - consider them equal

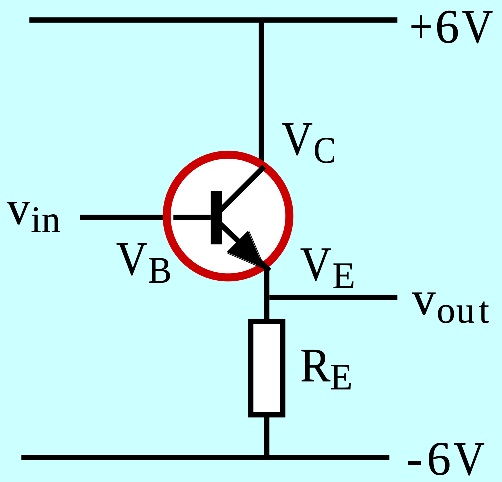
ie to ac current signals transistor looks like dynamic resistance

Emitter-follower

- DC conditions ±6V are example values, but results don't depend on them at all

    apply our rule that $V_{BE} \approx 0.7V$

    $I_E = [V_E - (-6V)]/R_E \approx (V_B + 5.3V)/R_E$



- Now ac behaviour

    $v_{in} = v_b = \Delta V_B = \Delta(V_E + 0.7V) = v_e = v_{out}$

    amplifier with gain = 1 - not very interesting!!??

- Input impedance

    $R_{in} = v_{in}/i_{in}$

    $i_{in} = i_b = i_c/\beta$

    $i_c = i_e = v_e/R_E$

    $R_{in} = \beta R_E$ high, eg $\beta \sim 100$, $R_E \sim 1k\Omega$

    (more careful treatment => $R_{in} = \beta(R_E + r_e)$)

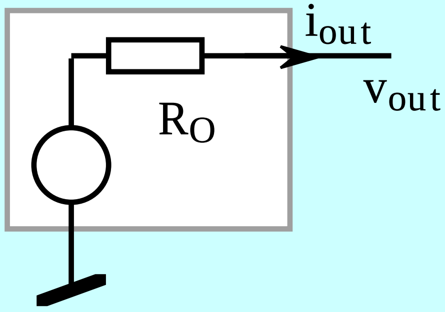
    this is promising for a voltage buffer - what is the output impedance?

Emitter-follower output impedance

- How to find it? Consider the black box...

  vary v_{out} and see what happens to i_{out}

  keep other conditions fixed



- Use Ebers-Moll result $V_{BE} = (kT/q)\log_e I_E$

  $dV_{BE}/dI_E = v_{be}/i_e = (kT/qI_E)$

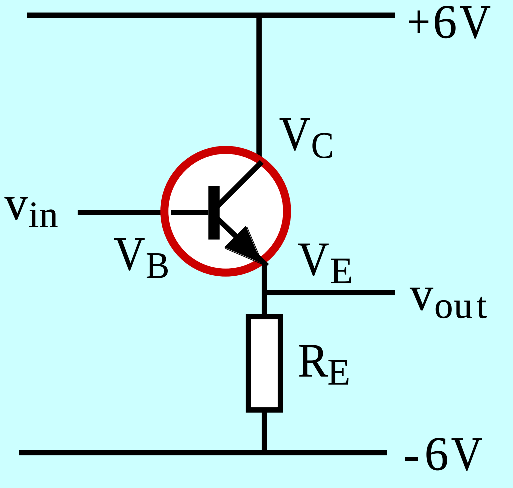
- If V_B is constant

  $v_{out} = v_e$

  $i_{out} = i_e$

  $Z_{out} = (kT/qI_E) = r_e = 25\Omega/I_E(mA)$

  small, as required for buffer



Short footnotes

- In analysing circuits for small signal (AC) behaviour

  all fixed DC levels are equivalent to ground

  ie ac current does not need to distinguish voltage at other end of path

- This is often useful in looking at circuits to tell if routes are in parallel

- Calculations

  keep simple

  try to make approximations - 1% answers are almost never required

  if so better tools exist

  eg parallel resistances

  transistor β - assume $\beta \approx 100$ - unless better value known or is critical

  $47\Omega \approx 51\Omega \approx 50\Omega$

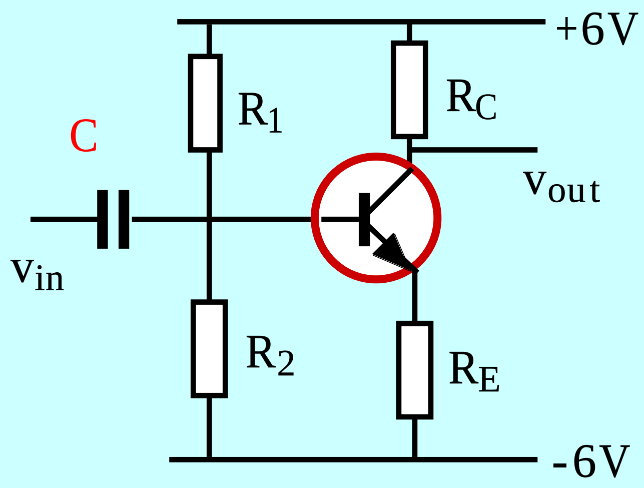
Common-emitter amplifier

- DC conditions ±6V are example values again

  $V_C = 6V - I_C R_C$

  $V_E = -6V + I_E R_E$

  Since $V_E = V_B - 0.7V$, I_E & I_C defined by bias network



- small signal, AC behaviour

  $v_e = v_b = v_{in} = i_e R_E$

  $v_{out} = -i_c R_C$

  so $v_{out}/v_{in} = -R_C/R_E$

  amplifier with gain

what's the purpose of C?

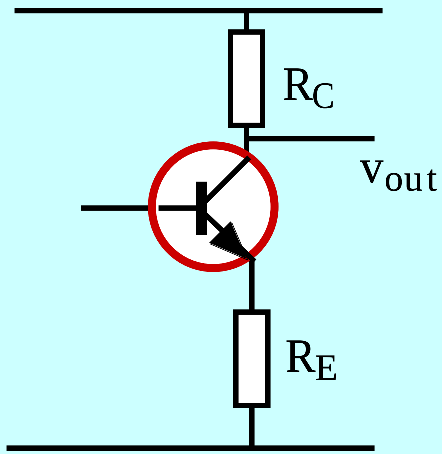
- Input impedance: signal sees bias network in parallel with transistor

  so $R_{in} = R_1 || R_2 || \beta(R_E + r_e)$ - typically a high value

Common-emitter output impedance

- Play same trick as emitter-follower

but this time, from output terminal, the two paths for i_{out} are



collector-base junction

reverse biased diode = high impedance

R_C

usually much lower than r_{cb}

no need to worry about any source impedance driving amplifier

so $Z_{out} \approx R_C$

usually relatively high

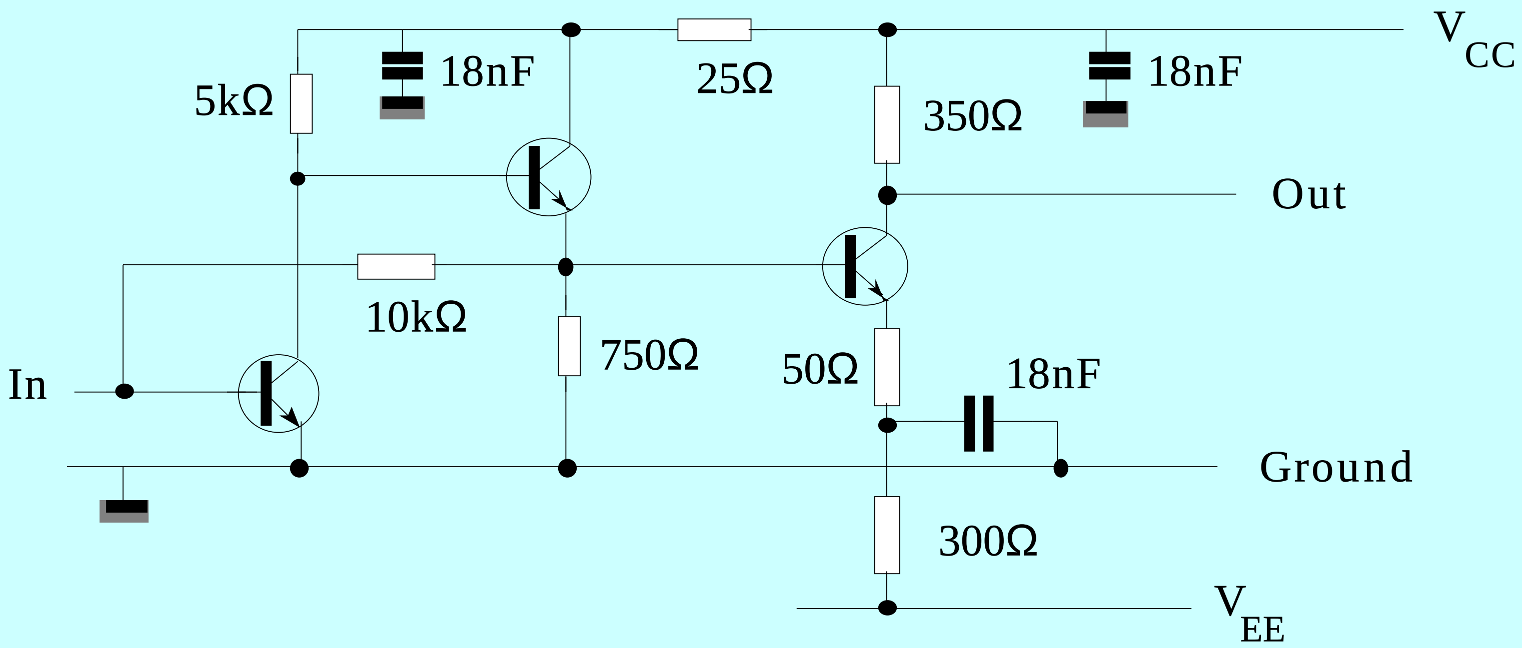
Reading circuits

- look for the building blocks

  usually blocks are "vertical columns"

- look for feedback paths

  horizontal paths,which are not DC bias, or output-input



Metal-Oxide-Silicon (MOS) devices

- Principle of MOS Field Effect Transistor transistor operation

  Metal (poly) gate on oxide between source and drain

  Source and drain implants of opposite type to substrate.

  Gate is biased to **invert** channel below oxide

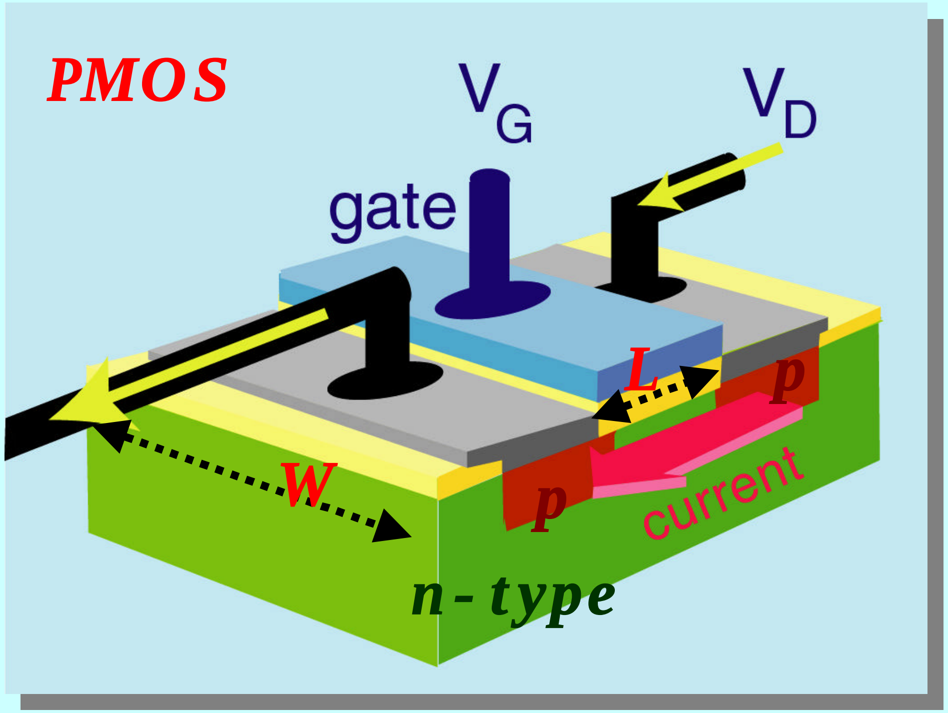
  apply voltage bias to gate, which...

  gives field across oxide

  modulates current in conducting channel

  transistor can be used as

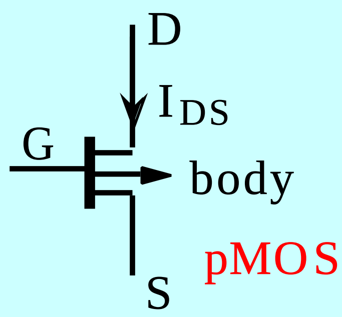
  switch (digital) or amplifier (analogue)

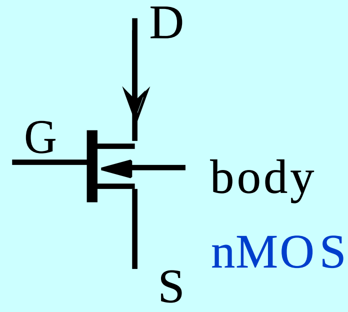


MOS Field Effect Transistor

•Operation - input signal is voltage on gate

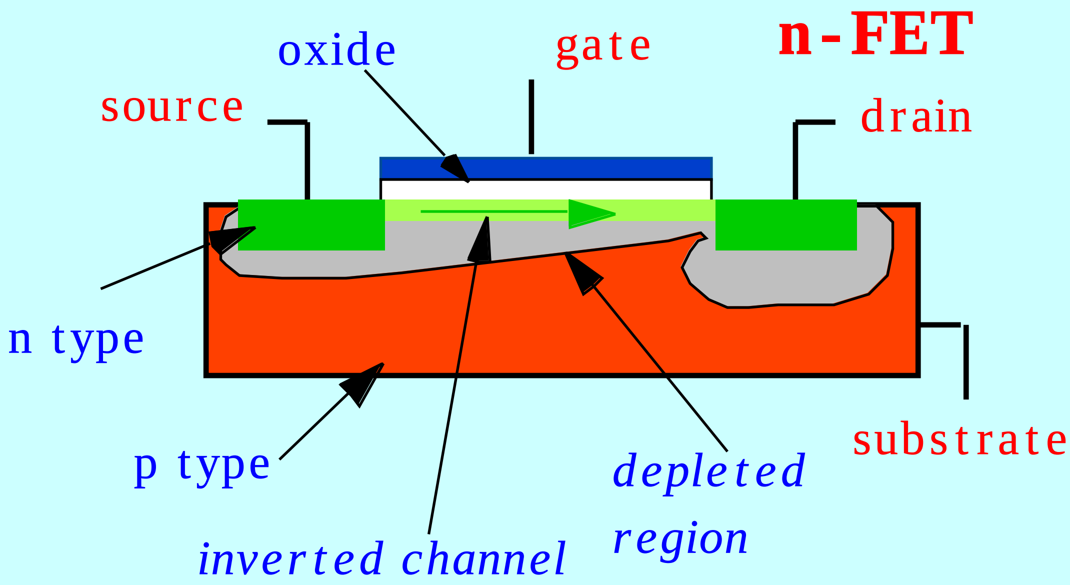
very high input impedance > $10^{12}\Omega$





•I-V behaviour nMOS

$V_G > V_T$ to switch on, vary V_{DS}



linear region

$I_{DS} \sim (V_G - V_T)V_{DS}$

saturation region

channel “pinch off” near drain

$I_{DS} \sim (V_G - V_T)^2$

$\partial I_{DS}/\partial V_{GS} = i_{ds}/v_{gs} = g_m = (2\mu C_{ox} I_{DS} W/L)^{1/2}$ transconductance

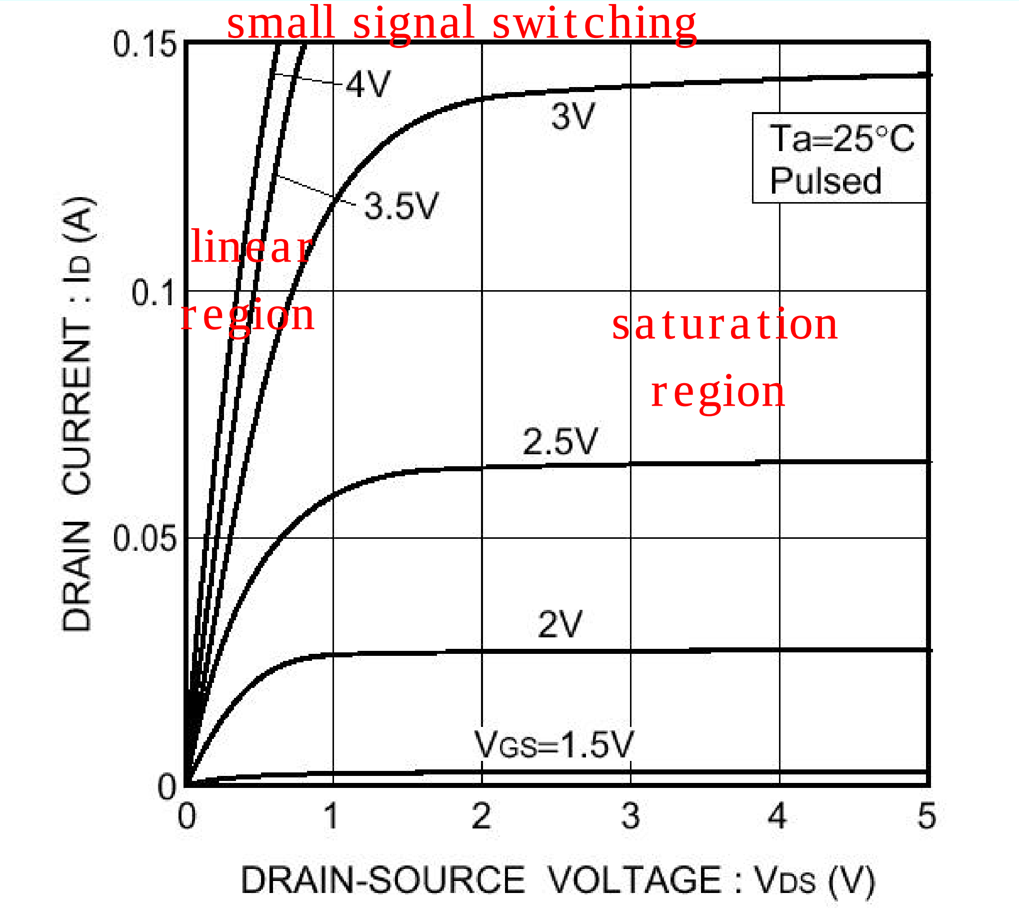
defined by geometry & current only - important for IC design

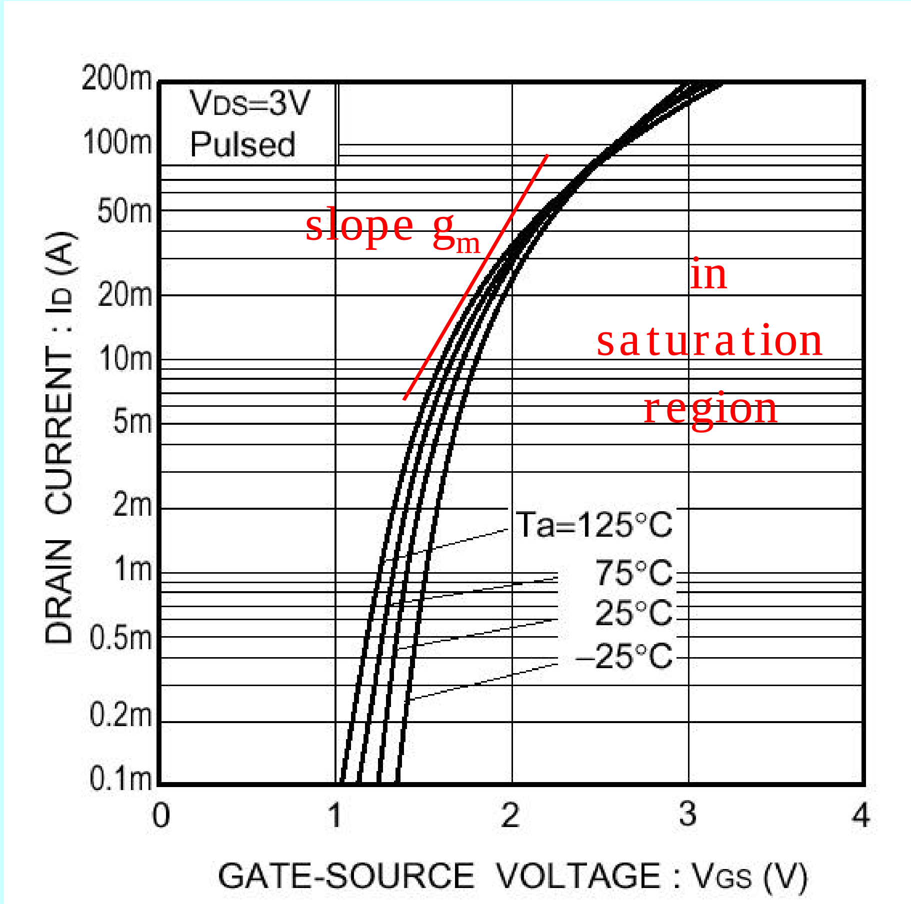
Designing with MOSFETs

• Mostly operate in saturation - choice of gate-source voltage determines current

but often bias with current source, so gate voltage "selected by" current

2SK3019





Simple MOSFET applications

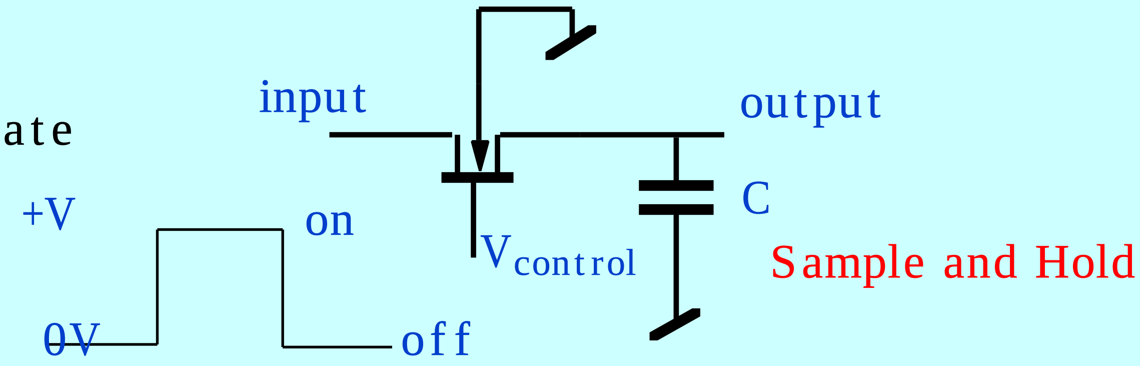
- Voltage controlled switch

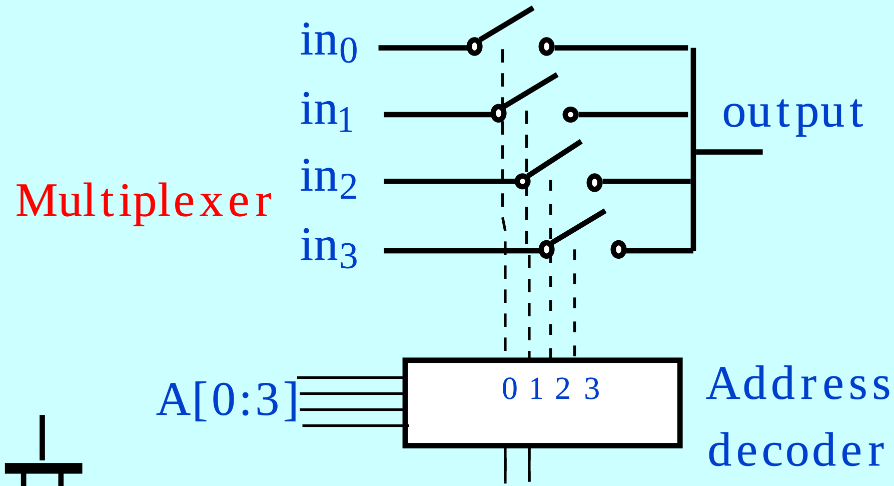
  very high resistance in OFF state

  R_{ON} ~ 5 - 100Ω

  fast response ~nsec

  bi-directional



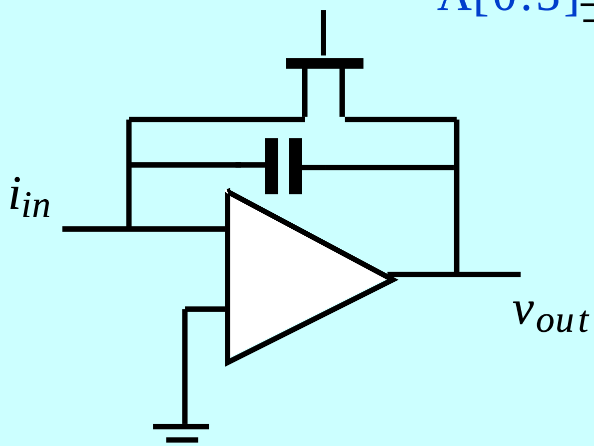


- Voltage controlled resistor

  operate in linear region

  $R_{DS} \sim 1/(V_G - V_T)$

  convenient for IC design



ElectroStatic Discharge

- MOS circuits are prone to damage from ESD

  gate oxides are thin layers - few nm in advanced technologies

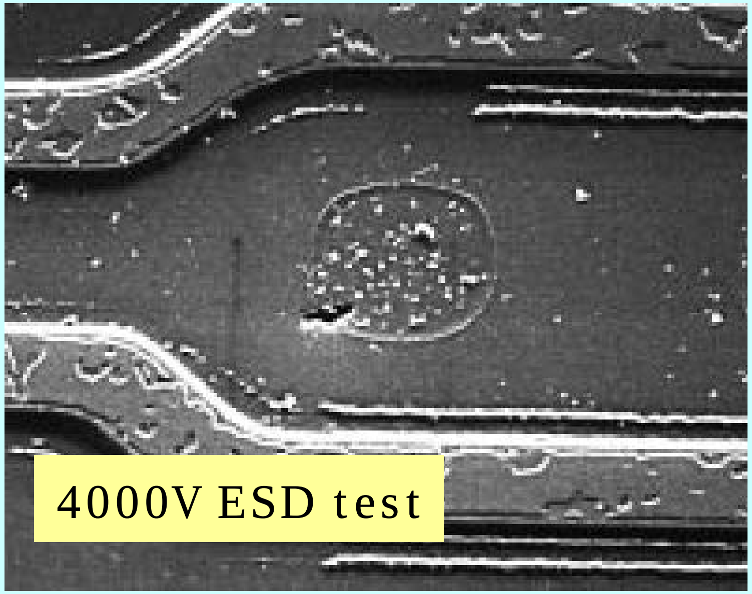
  oxide breakdown field < 1000MV/m = 1V/nm

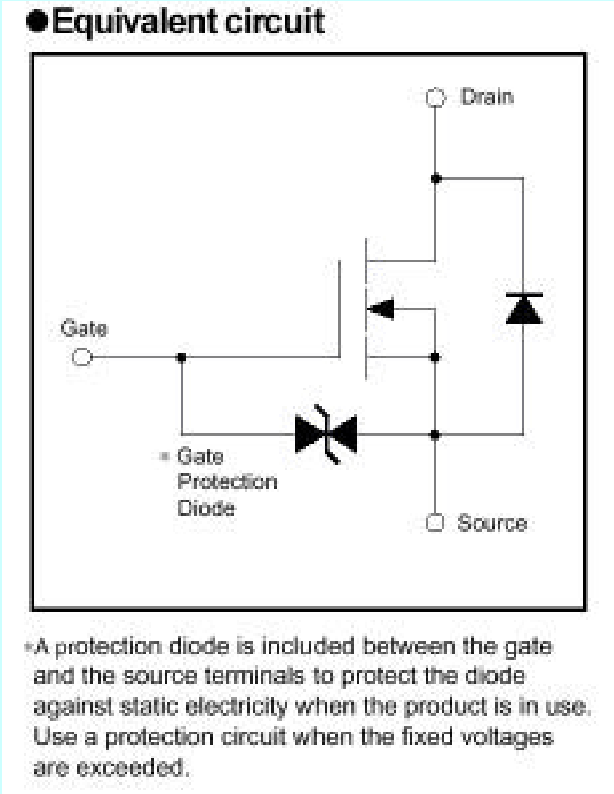
- Human body can easily charge to 30-40kV walking across carpet on a dry day

  precautions:

  circuits designed with protection diodes

  stand on conductive pad and earth body with wrist strap





CMOS = Complementary MOS

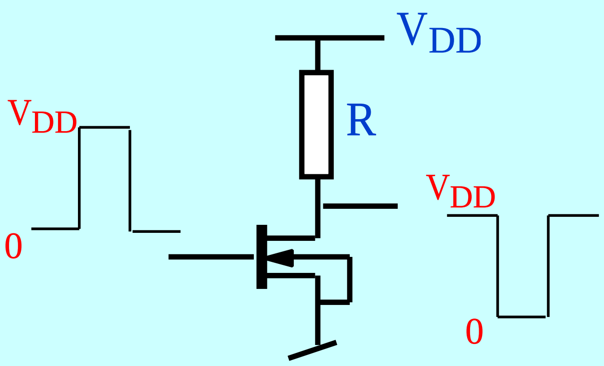
- Both pMOS and nMOS transistors on same wafer

  by putting p-type "wells" into n-type wafer (or vice-versa)

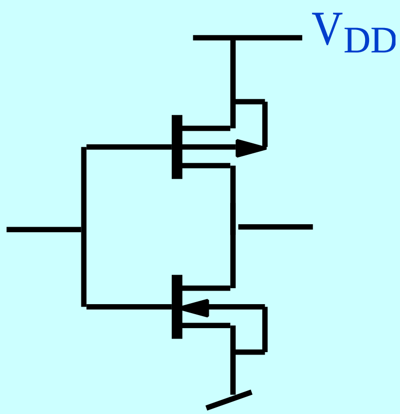
  build nMOS transistors in locally p-type region

- Why?

NMOS inverter



CMOS inverter



NMOS consumes power in low state

CMOS version consumes power only when switching

basis of almost all modern logic

In IC technologies, accurate resistors are harder to make than C and transistors

Junction FET

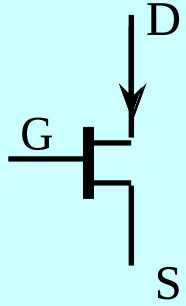
- Almost identical to MOSFET - difference is

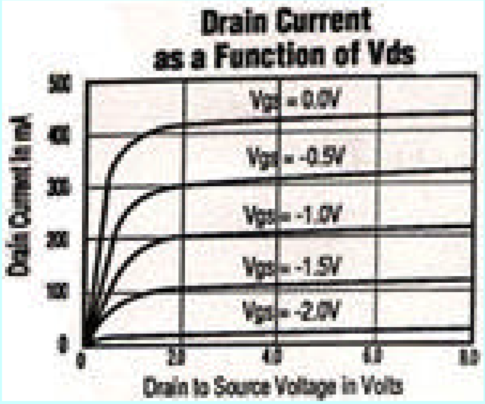
  Gate is implanted p-n junction

  voltage on gate depletes bulk silicon

  current conducting channel reduced or enlarged

  $\Delta V_{GS} \rightarrow \Delta I_{DS}$





- Characteristics - similar to MOSFET

  gate is reverse biased diode

  high input impedance ($\geq 10^9\ \Omega$)

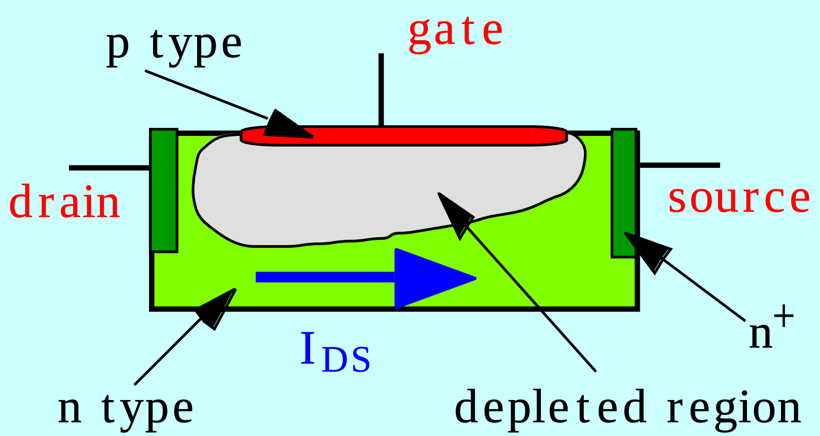
  small current from diode leakage

  usually operated in saturation

  channel 'pinched off' by depletion.

  "typical" values

  $g_m \sim 10\text{mA/V} = 1/100\Omega = 10\text{mS}$



FET circuits

- Building blocks resemble bipolar circuits
- Source follower (cf emitter follower)

$i_{ds} = g_m(v_g - v_s) = g_m(v_{in} - v_s)$

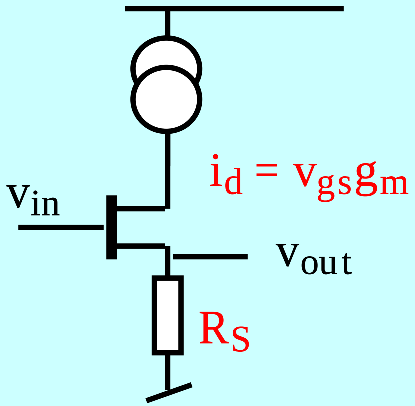
$v_{out} = v_s = i_{ds}R_S = g_m(v_{in} - v_s)\, R_S$

$v_{out}/v_{in} = g_mR_S/(1 + g_mR_S) \leq 1$

$R_{in} \sim 10^9 - 10^{12}\Omega$

$R_{out} = R_S||R_{DS} = R_S/(1 + g_mR_S)$

not low

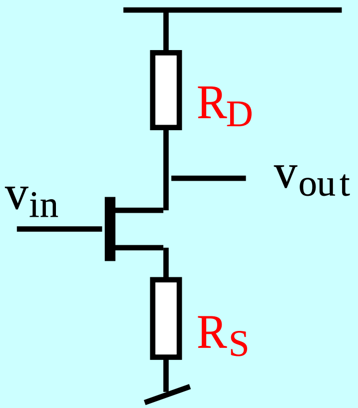


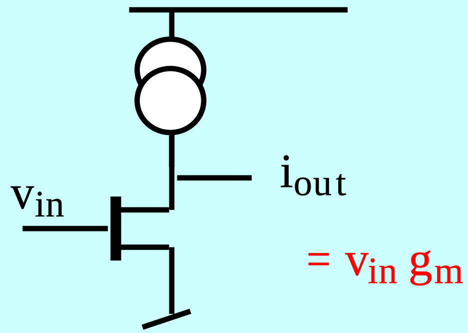
- Common Source amplifier -

$v_{out}/v_{in} = -g_mR_D\ /(1 + g_mR_S)$

R_{in} high

$R_{out} \approx R_D||R_{DS} = R_D/(1 + g_mR_D)$





but more common configuration uses current source with suitable load $i_{out} = g_mv_{in}$

FET limitations

- On Resistance

  although small, it contributes to RC time in fast switches

- Capacitance

  inevitable capacitances between nodes, important for high speed circuits

  $C_{gate} \sim C_{ox}WL$ for MOSFETs

- Relevance to op-amps

  FET amplifiers have much <u>higher input impedance</u>

  and draw much lower currents

- Cautions

- Latch-up

  under certain conditions, parasitic bipolar transistors formed

  MOS circuits can go into high current states - destructive

- ESD

  care needed in handling

  protection networks can degrade performance

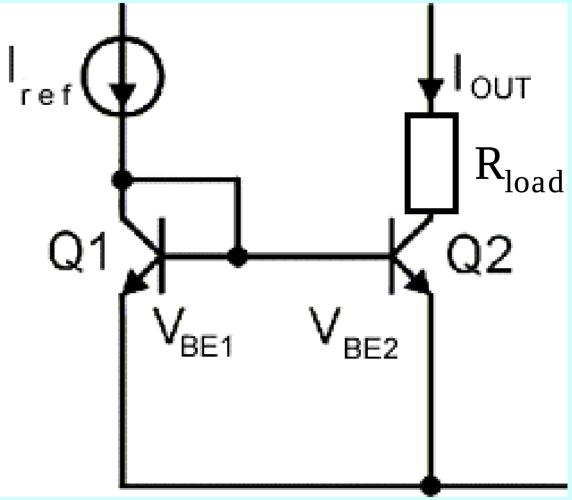
Another building block - the current mirror (if time)

- Q_1 & Q_2 are identical transistors

  $V_{BE1} = V_{BE2}$ and $V_{BE} \approx (kT/q)\log_e I_E$

  so $I_{out} = I_{ref}$

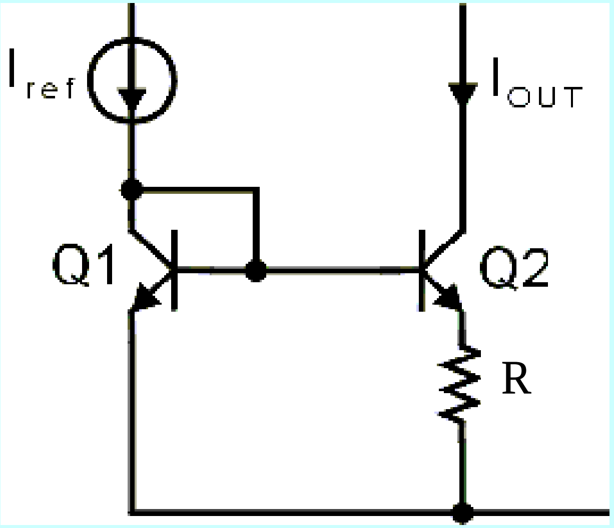
  widely used in ICs where closely matched transistors are easy to construct - useful to program currents



- add a resistor

  $I_{out} = (kT/qR)\log_e(I_{ref}/I_{out})$

  eg $R = 1k\Omega$, $I_{ref} = 1mA \Rightarrow I_{out} = 67\mu A$

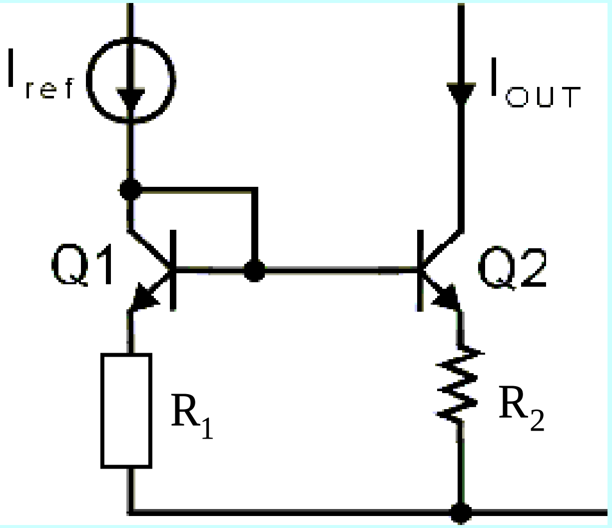


add another resistor

$V_{BE1} \approx V_{BE2}$

$I_1/I_2 = R_2/R_1$

also works for discrete circuits



Band-gap circuit

- To be more precise,

  V_{BE} ~ log(current density) so in non-matched transistors

  with same current, and ratio of emitter areas r

  $V_{BE1}-V_{BE2} = (kT/q)\ln(r)$

  easy to achieve in IC technology

- Principle of AD590 T sensor

  Proportional To Absolute Temperature (PTAT)

  $I_1 = I_2$

  $\Delta V_{BE} = (kT/q)\ln(r) = I_1 R$

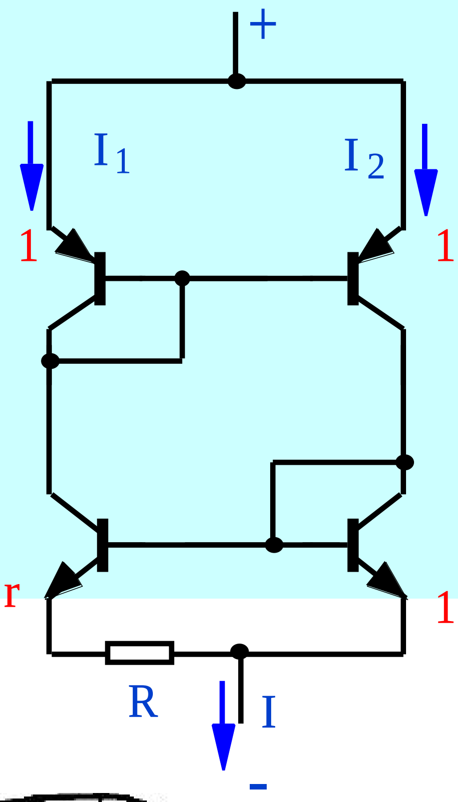
  $I = I_1 + I_2 = (2kT/qR)\ln(r)$

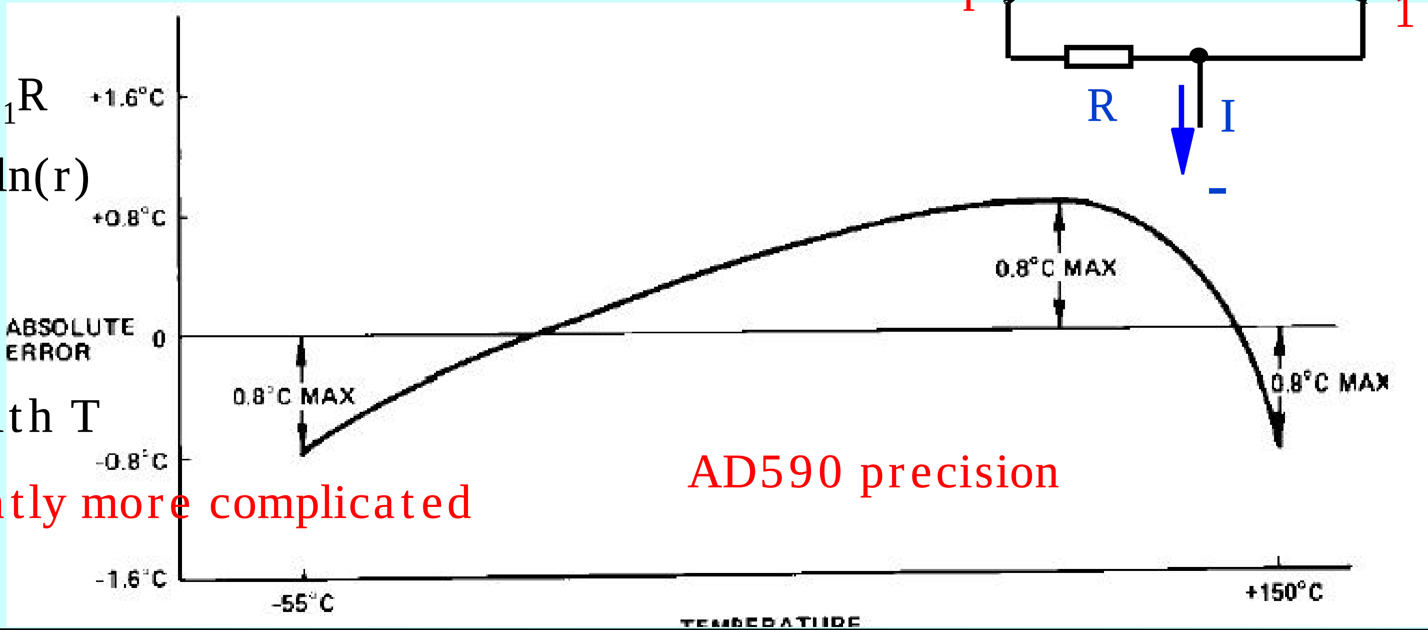
  $r = 8 \quad R \approx 1k\Omega$

  $I \approx 1\mu A/K$ @ 300K

  R should vary little with T

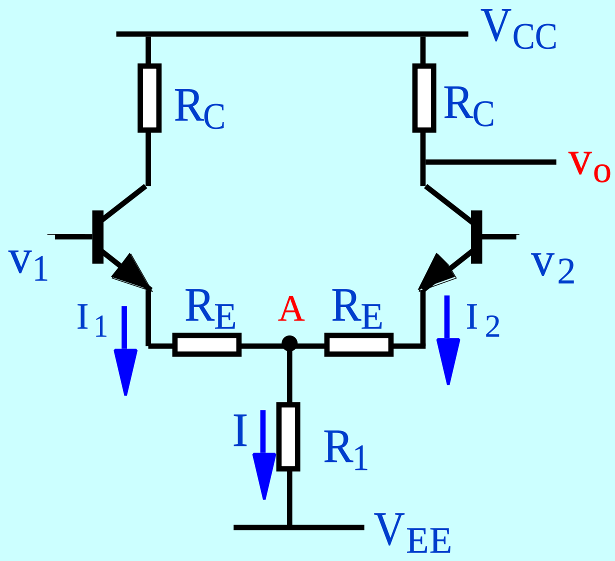
- actual AD590 only slightly more complicated





AD590 precision

Transistor differential amplifier (for the ambitious)



- DC R_1 is large, to act as current source

  $V_A = V_{EE} + IR_1$

  $V_{E1} = V_A + I_1R_E \quad V_{E2} = V_A + I_2R_E$ (ignoring r_e)

- AC

  $v_1 = v_A + i_1R_E = iR_1 + i_1R_E$

  $v_2 = v_A + i_1R_E = iR_1 + i_2R_E$

  $i = i_1 + i_2$

  $v_1 - v_2 = (i_1 - i_2)R_E$

  $v_0 = - i_2R_C$

- For differential inputs $v_1 = - v_2$ so $i = 0$

  $G_{diff} = v_0/(v_2 - v_1) = R_C/2R_E$

- Common mode $v_1 = v_2 = v_{cm}/2$

  $v_1 + v_2 = 2iR_1 + (i_1 + i_2)R_E = i(2R_1 + R_E)$

  $G_{cm} = v_0/v_{cm} = -R_C/(2R_1 + R_E)$

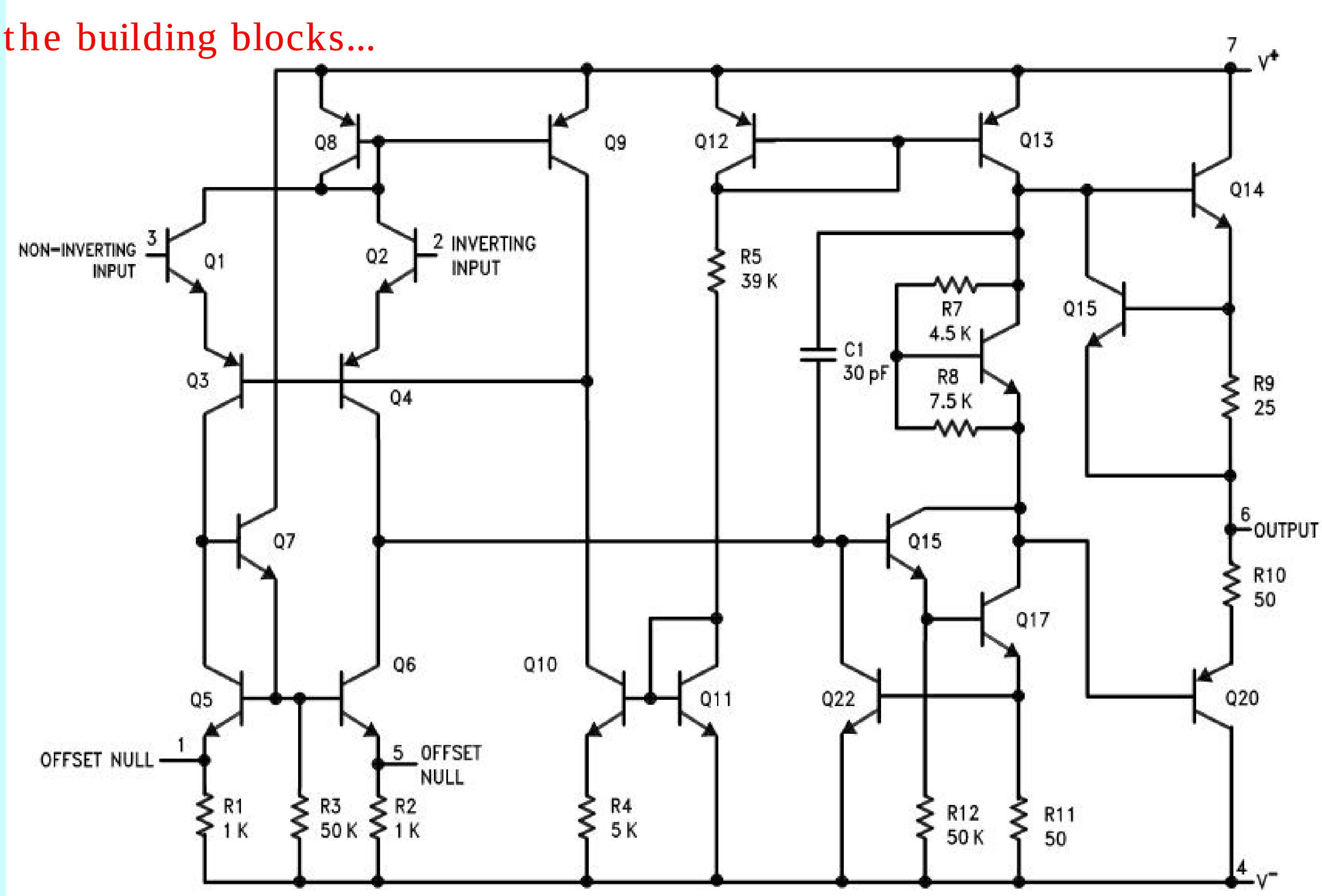
  CMRR $\approx 2R_1/R_E \quad R_1 >> R_E$

Variants

- R_C in Q1 loop omitted
- replace R by current source
- omit R_Es
- differential outputs

What's inside an op-amp...

- Look for the building blocks...



MOS IC amplifiers look similar but currents determined by transistor aspect ratios