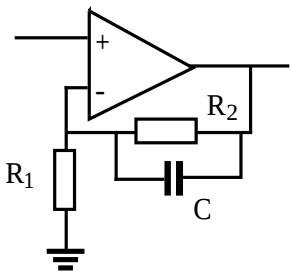
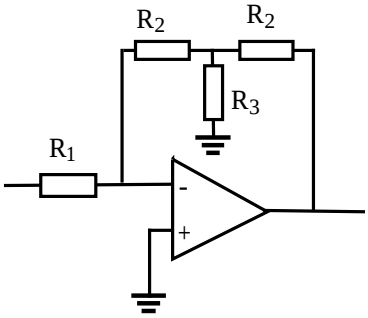
Instrumentation Problem Sheet 4 Amplifiers

(1) An amplifier has an open loop voltage gain of 140dB at f=0Hz and a single pole at f = 100Hz. What is the gain-bandwidth product (GBW)?

(2) The amplifier in the figure is designed with R_1 = 10kΩ, R_2 = 91kΩ. The open loop voltage gain is 100dB at f=0Hz and the amplifier has one pole at f = 100Hz and a second at 100kHz. What value of capacitor will ensure stability without affecting the gain too much at high frequencies where is it intended to operate?
(This problem is best solved starting with a graph.)

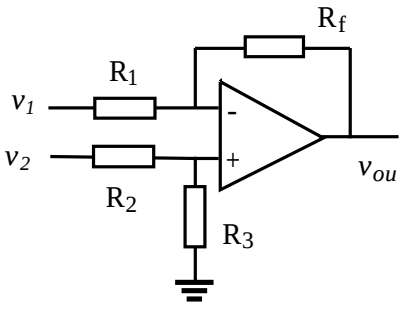


(3) Calculate the gain of the op-amp configuration shown in the figure.



(4) A general version of the differential amplifier is shown in the figure. Show the output voltage is

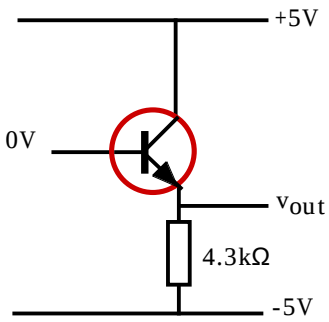
$v_{out} = v_2(R_3/R_1)[(R_1+R_f)/(R_2+R_3)] - v_1(R_f/R_1)$



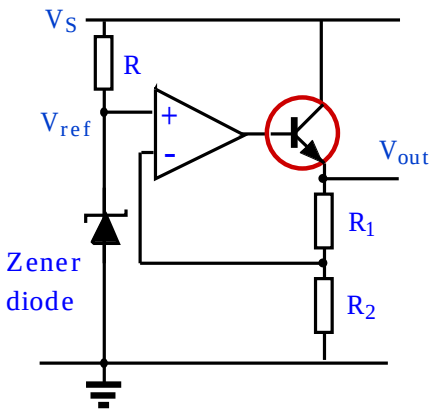
For a non-zero common mode signal v_{CM}, what is the resulting value of v_{out}? Show that this reduces to v_{out} = 0 for $R_1 = R_2$ and $R_f = R_3$
The amplifier is built with $R_1 = R_2$ and $R_f = R_3$. If the resistor values have a 5% tolerance, what is the accuracy in the required gain? (Assume an ideal op-amp)

(5) Show that at high frequencies a current sensitive amplifier with a single low frequency pole has an input impedance which is inductive, instead of purely resistive. Calculate the value of L for an amplifier with DC gain = 60dB, GBW = 10^7 Hz and R_f = 1MΩ. At what frequency would this become significant if the input load capacitance is 100pF?

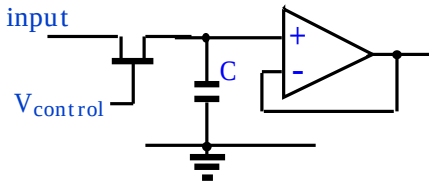
(6) What is the transistor current, the DC level at the output and the input impedance of the circuit of the circuit illustrated?



(7) The circuit shown produces a regulated voltage. The reference voltage V_{ref} is produced by a Zener diode, which has the property of a very steep I-V curve so that it has an almost constant voltage across it for a wide range of currents.
What is the output voltage V_{out}? What is the maximum V_{out} which can be produced?

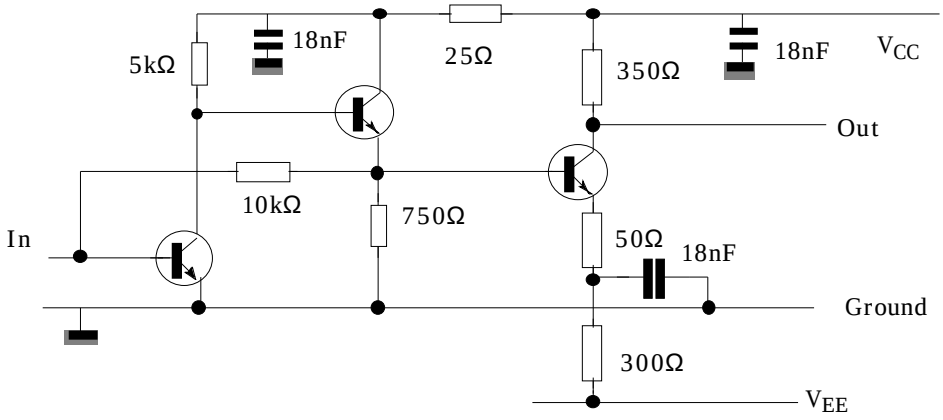


(8) The circuit shown is a sample and hold. A voltage $V_{control}$ is applied to the FET gate to turn it on and off. Initially the FET is off, and C = 0.1μF. When the FET is conducting it has a channel resistance R_{DS} = 5Ω. Sketch the output voltage if a voltage V(t) = At is applied at the input, and $V_{control}$ is switched so that FET conducts for 2μs, at t = 0, 100μs, 200μs, 300μs, ...



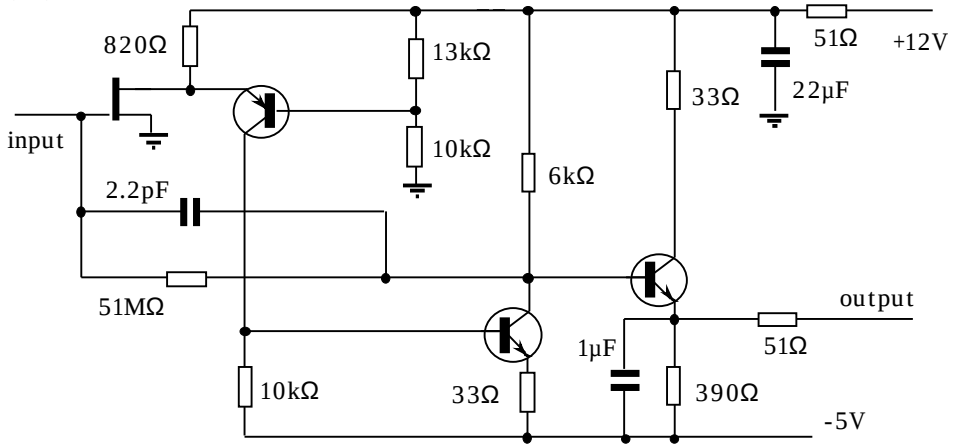
(9)

V_{CC} = 3.5V
V_{EE} = -1.5V.



The figure above shows the fast current pulse amplifier described in the lectures. Identify the feedback resistor, voltage gain stages and buffer stages. What is the input impedance? To calculate this you will need to work out the currents in each stage. Don't try to be more accurate than necessary. The output stage has some strange features. Can you suggest how it works and why it is designed this way?

(10)



The figure above shows a slightly simplified charge sensitive amplifier. The parts of the circuit omitted ensure that the DC level at the output is approximately 0V. What is the impulse response and its time constant? What is the output impedance? What current flows in the input transistor? What are the advantages of this amplifier compared to the one in the previous problem? Identify the buffers and gain stages. Try to work out the DC bias conditions and power consumption. What is the gain if the transconductance of the input transistor is 10mA/V or 10mS? (Siemens = A/V)

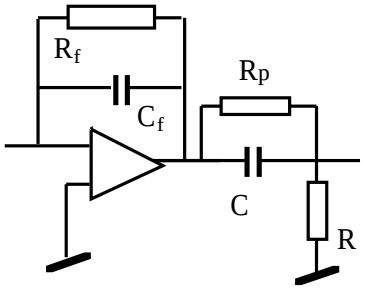
(11) Show that a charge integrator followed by a differentiation stage produces a unipolar impulse response, ie with no baseline crossing. Show that two stages of differentiation produce a pulse shape which has an undershoot below the baseline. For differentiator time constants τ_1 and τ_2, what is the relative magnitude of the undershoot? [Use transfer functions and work in frequency, then convert to time.]

(12) Show that the charge sensitive amplifier and high pass filter network in the figure has an output which is given by

$$v_0 = A(Q/C_f)\exp(-t/\tau)$$

where $\tau = R_pR_fC/(R_p+R_f)$

Find the condition on R_p which ensures this and the value of A.



(13) The charge sensitive amplifier of the previous problem is combined with further stage as shown in the figure to build an bandpass filter with two equal time constants. R_f = 10MΩ and C_f = 1pF. C= 220pF, R = 12kΩ, R_2 = 100kΩ and R_1 = 4.7kΩ. Suggest suitable values for R_p and C_2. A 47Ω resistor is placed in series with the output. Can you suggest a reason?