First ideas for readout/DAQ

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Contributions from all of UK: result of brainstorming meeting in Birmingham on 13 November

Several things we don't know...

- VFE chip shaping times, signal outputs, pin layout, etc?
- HCAL implications; common readout, fast control and timing, etc?
- Test beam time structure; rates, burst lengths, etc?

  Need feedback on these items today!

Assumed requirements

- Want to work as close to “LC-mode” as we can
  - Learn how to operate in semi-realistic conditions
- Want to study pedestals and noise as well as signals
  - Allow readout of data below threshold
- Want to filter (fit?) signal waveforms offline to extract best resolution
  - Need multiple samples over a single signal

Basis of conceptual design

TESLA burst timing; 1ms at 5 Hz.

- Run untriggered in ~1ms bursts, power down front-end electronics for rest of time
- Store all data at front-end during burst
- Read out all data, or data above threshold, before going live again for another 1ms burst

Basis of conceptual design 2

TESLA bunch spacing; ~300ns

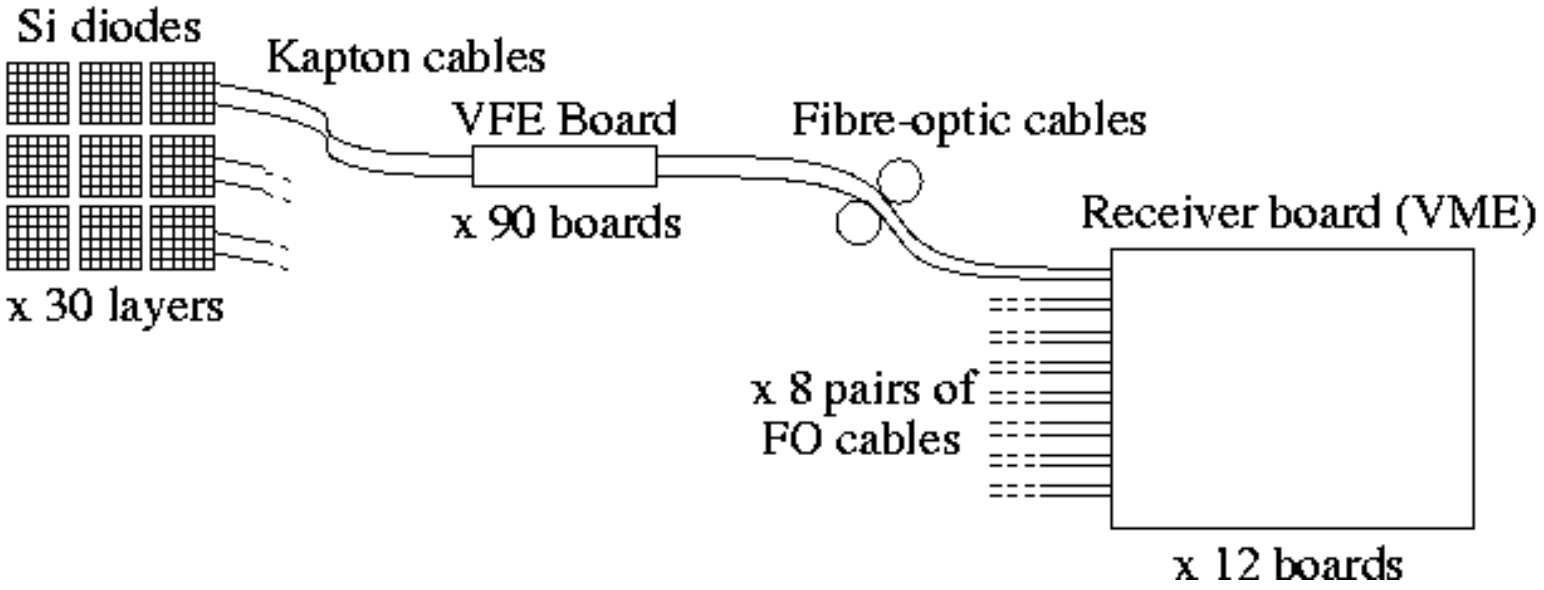
- VFE chip shaping times must be of same order to allow bunch separation. (Is this really needed?)
  - Assume ~20MHz ADC sampling rate gives adequate signal waveform shape
- Assume VFE chip will not do channel multiplexing, so need 1 ADC/channel
- Keep multiple samples for each channel, including tails below threshold

Basis of conceptual design 3

BUT we don't know beam structure, etc.

- Keep a flexible approach
  - Make as much as possible software configurable
- Allow the use of a trigger/veto if needed
  - Still do bursts but choose if to read out
  - Who will provide a trigger if needed?
- The following is a feasible system
  - Specific numbers are given but should be considered as examples, not hard choices

Overview of conceptual system

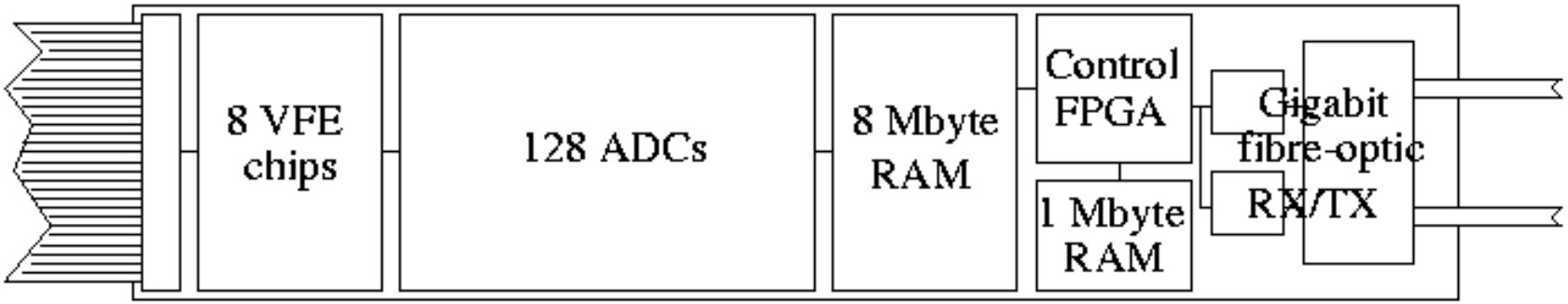


- 1 VFE board per 3 diode wafers = 90 total
- 1 receiver board per 8 VFE boards = 12 total

Overview of conceptual system 2

- All timing and control to very front-end board via fibre-optic cables
  - Gives clock (80 MHz) and simple control and configuration protocol on downlink
  - One downlink for multiple VFE boards?
  - Makes grounding and shielding of VFE boards easier
- Digitisation done on VFE board at 20 MHz
  - Digital data out of VFE board via uplink
  - Also allows hand-shaking for control protocol

VFE boards



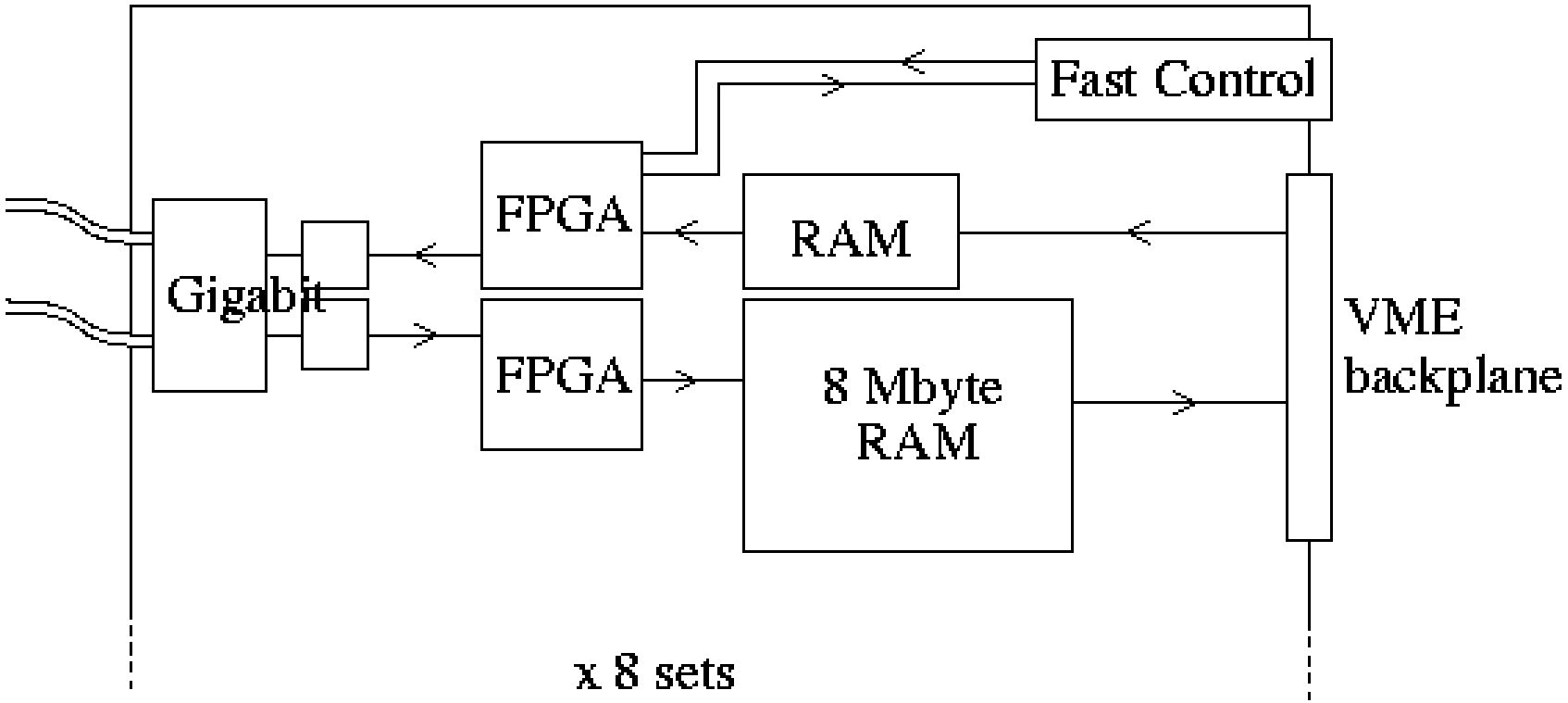
- 3 wafers = 3 x 6 x 6 = 108 diode channels
- Round up to 128 channels; allow for spares
  - 8 VFE chips (assuming 16 channels/VFE chip)
- Write directly to large memory during burst
- FPGA does pedestals and thresholds
  - Store in small memory until readout

VFE boards 2

- VFE chips on separate daughterboard
  - Decouples design details
  - Should kapton cables attach to this directly?
- VFE board mixed analog and digital
  - Could put on opposite sides of board if needed
- Physical mounting of 90 boards?
  - Need a custom built “crate”?

In final system, does the VFE board have to become a couple of ASICs?!?

Receiver boards



- Each receiver board handles 8 VFE boards
  - 1024 diode channels

Receiver boards 2

- Fast control distributes 80 MHz system clock throughout the system
  - Also commands to start and stop burst capture synchronously
- VME interface allows configuration data to be written to VFE boards
  - Thresholds, bad channel masks, etc.
- Large memory captures all data from uplink until VME read

Some numbers on data rates

- 8 or 10 bit ADC's and range bits; assume 2 bytes per sample per channel
- 256 bytes per 20MHz sample so for 1ms, this results in 5 Mbytes of raw data
- FO uplink sends 2 bytes at 80MHz; 32 times slower, i.e. 32 ms to send.
- VME speeds ~20 Mbytes/sec; full data gather of 450 Mbytes takes ~20 secs.
- Using thresholds, faster by x10, x100, x1000

Other questions

- A critical issue in final system is cross-talk and pick-up in 1.6m kapton cables
  - How will we test this in the beamtest?
  - Do we need to build a 1.6m-long set of wafers to test this? If so, we need to build some readout
- How does this all fit in with the HCAL plans?
  - How do we tie them together?
- Minor; what is the final data format needed?
  - ROOT? What format is simulation output in?

Cost guesstimate: VFE board

Components of the VFE board

- £2/ADC x 128 ADC's ~ £300
- £100 FPGA ~ £100
- £200 TX/RX FO set ~ £200
- £20/Mbytes x 9 Mbytes ~ £200
- £300 PCB ~ £300

Total for each VFE board ~ £1100

Cost guesstimate: receiver board

Components of the receiver board

- £100 FPGA x 8 FPGA's ~ £800
- £200 TX/RX FO set x 8 sets ~ £1600
- £20/Mbytes x 40 Mbytes ~ £800
- £2000 PCB ~ £2000

Total for each receiver board ~ £5200

Cost guesstimate: total

- 100 VFE boards ~ £110k
- 15 receiver boards ~ £80k
- Other infrastructure
  - VME crate ~ £10k
  - PC, disk and VME/PCI interface ~ £20k
  - Power supplies ~ £10k
- Total hardware cost ~ £230k
- Also need ~2 engineers for 1.5 years

The next steps

- Will go to UK funding body in March 2002
  - Maybe a preliminary report also needed in January; we need to make decisions soon
  - Not outrageous cost, but LHC budget overrun has made things complicated
- If approved, then much to do in 18 months
  - Very tight for full system from scratch in this time (includes two FPGA designs)
  - More credible if beamtest timing slips; we must be very honest about the realistic schedule