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# ECAL Readout Tests

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For the CALICE-UK electronics group

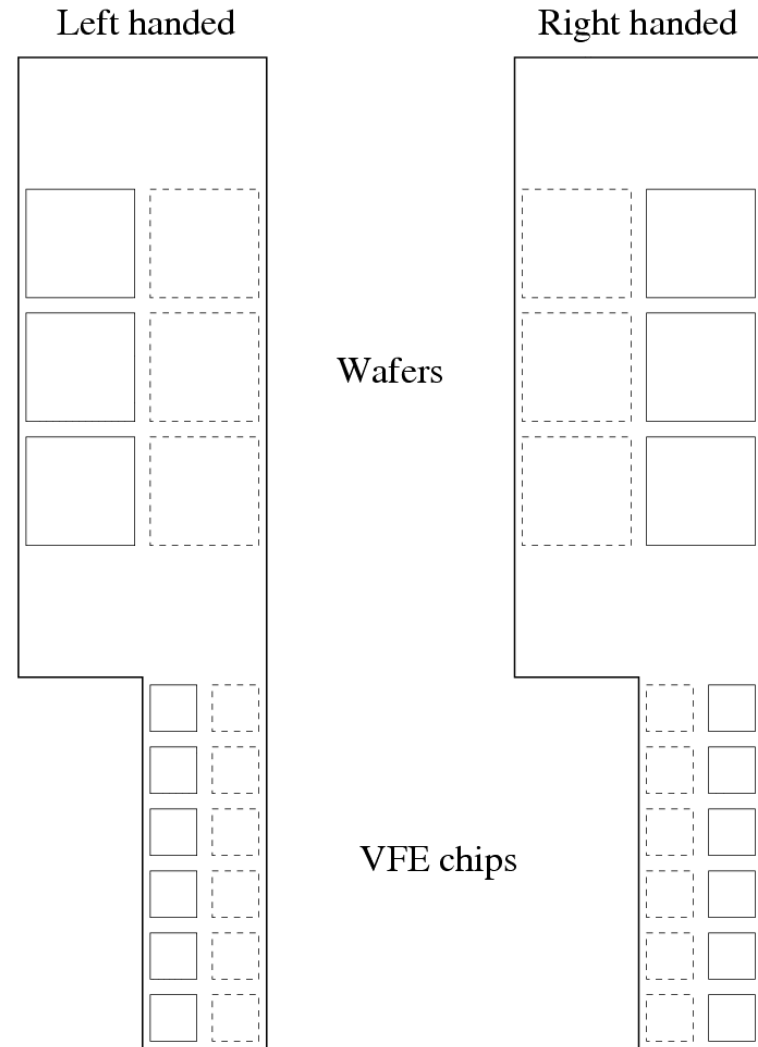
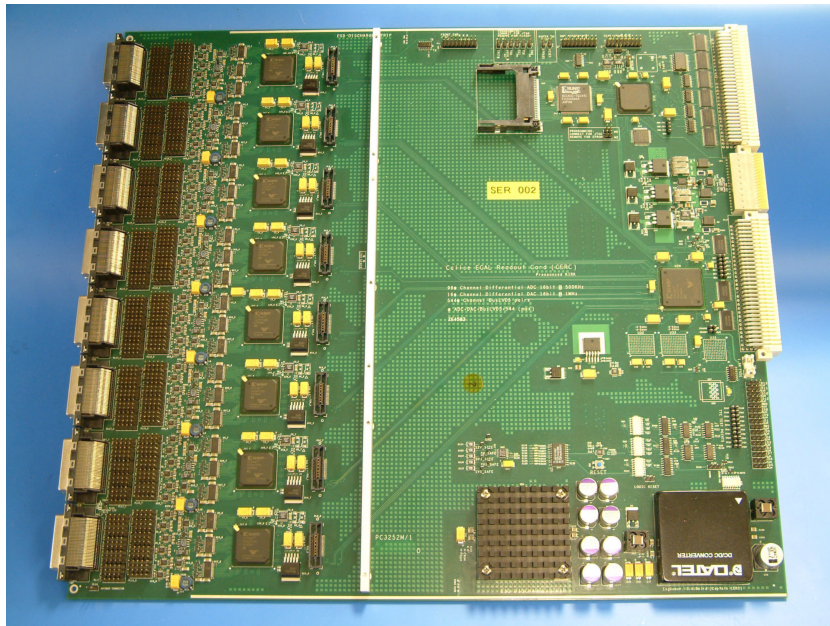
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A. Baird, D. Bowerman, P. Dauncey, C. Fry,  
R. Halsall, M. Postranecky, M. Warren, O. Zorba

Thanks to: J.C. Vanel, J. Fleury, C. de la Taille

# Available electronics

- Orsay **VFE PCB V2\_2** boards
  - Using VFE chip FLC\_PHY3
  - Preproduction version
  - Three boards available
    - One each full, left-handed, right-handed
- **CERC** UK readout board
  - Prototype version



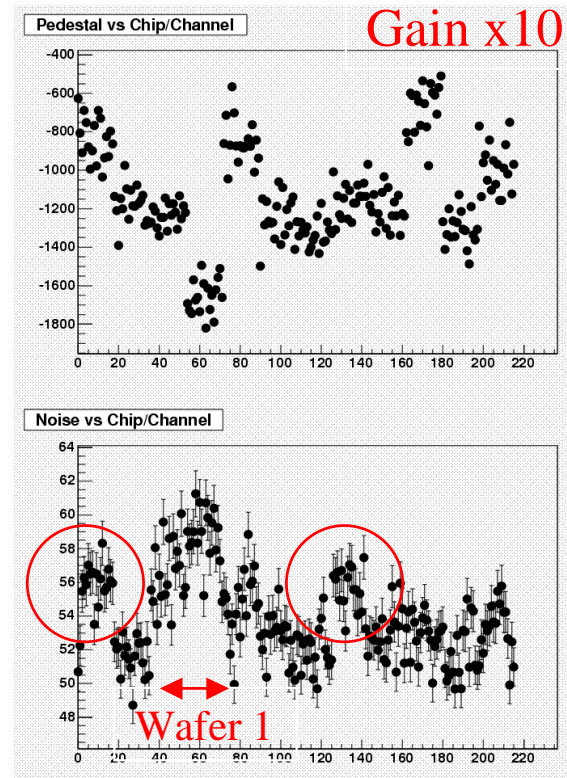
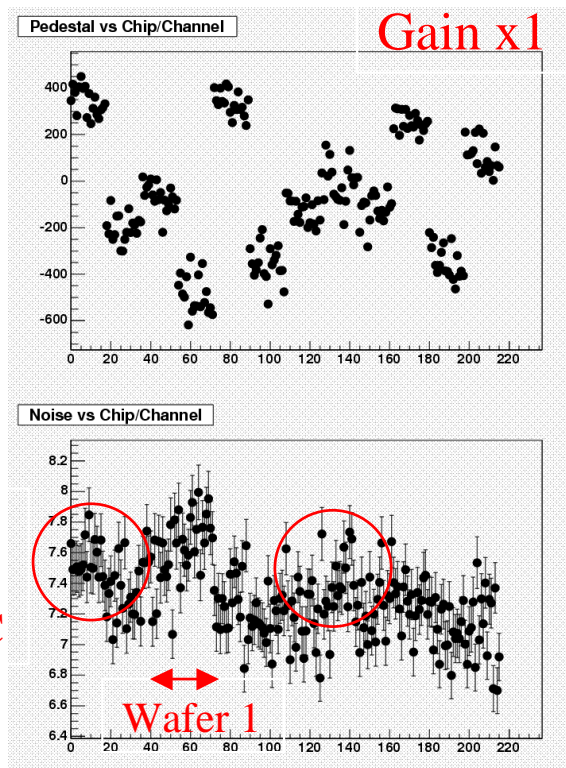
# Test motivation

- Tests which were done
  - Noise measurements
  - Calibration with DAC
  - Cosmics in LLR teststand
- To check
  - **Problems**: are there things which don't work?
  - **Uniformity**: do all channels look similar?
  - **Stability**: is the system stable with time?
  - **Dynamic range and signal/noise**: are they sufficient?
  - **Optimisation**: are there changes which will improve the system?
- Aim to verify VFE PCB V2\_2 and so release for production
- More details of test results available from

<http://www.hep.ph.imperial.ac.uk/calice/elecPrototypeTests/electronics.html>

# Noise tests

- Software selectable gain on VFE PCBs; **x1** or **x10**
- Full PCB has 6 wafers mounted; wafer 1 does not deplete



Known  
problem  
on CERC

Gain x1 noise= **7.2 ADC counts**, gain x10 noise= **52 ADC counts**

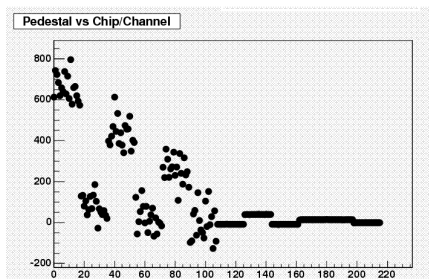
1 ADC count =  $78\mu\text{V}$ . No obvious dead channels

# Noise tests (cont)

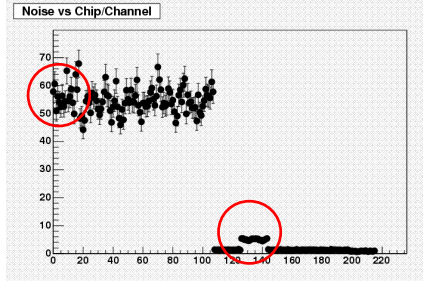
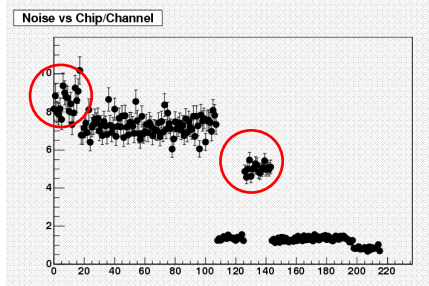
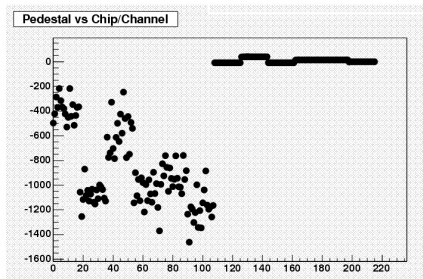
- Left-handed and right-handed had no wafers mounted

Left-handed

Gain x1

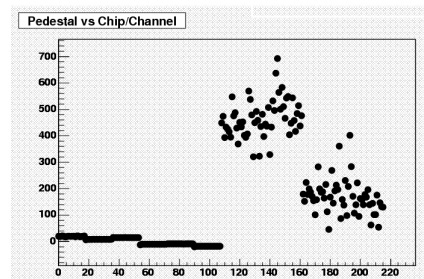


Gain x10

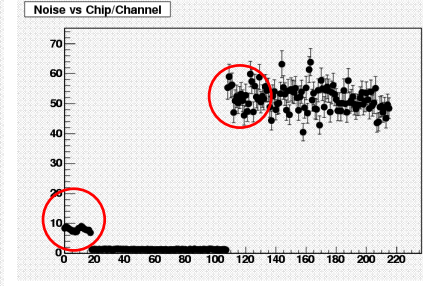
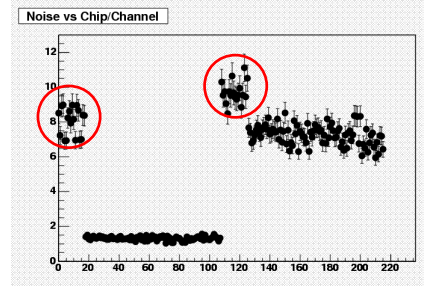
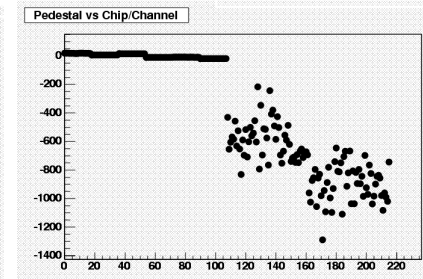


Right-handed

Gain x1



Gain x10



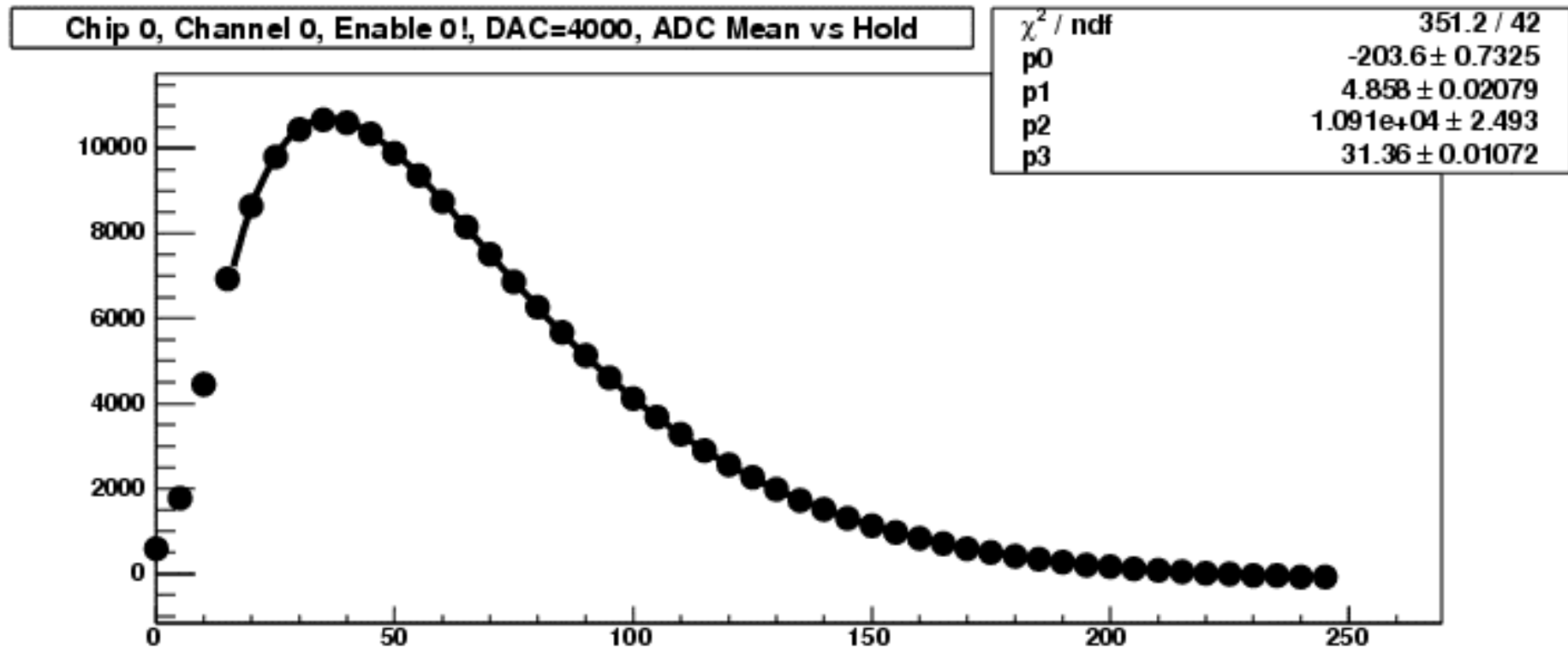
- Noise very **similar** to full PCB
  - Wafer leakage current and extra capacitance have only small effect

# Calibration with DAC

- Need to determine **timing**
  - Output signal is shaped by CR-RC circuit, shaping time  $\sim 200\text{ns}$
  - Adjust HOLD start time so that sample-and-hold captures peak
  - Can change HOLD time in software configuration; steps of  $6.25\text{ns}$
  - Scan HOLD time and fit for peak
- With HOLD timing set correctly, scan **DAC**
  - From zero to channel saturation
  - 16-bit DAC, 1 DAC count =  $20\ \mu\text{V}$
  - Determine mean and noise at each point
  - Fit for intercept and response
- Channels divided into **6 groups** for DAC
  - Calibration can be enabled independently for each group
  - Look at response of non-enabled channels
  - Measure **crosstalk**

# HOLD timing determination

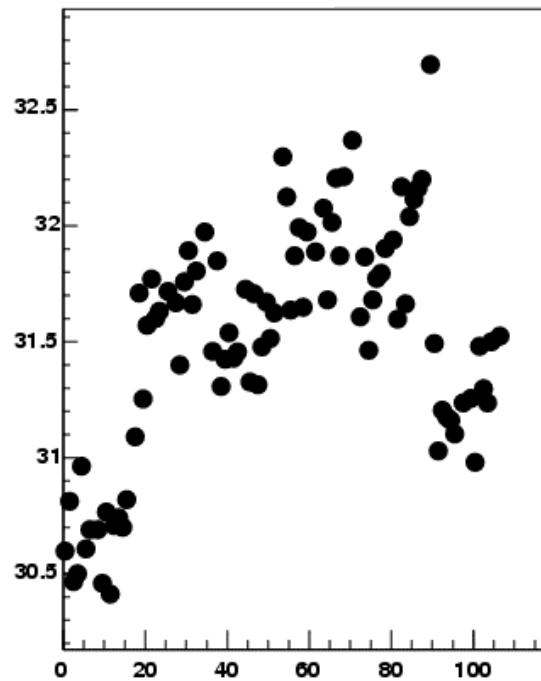
- Typical channel (first one on right-handed PCB), gain x1
- Fit CR-RC  $xe^{1-x}$  shape to response (averaged over 19 events)
- Shaping time = p3 = 31.36 units = 196 ns



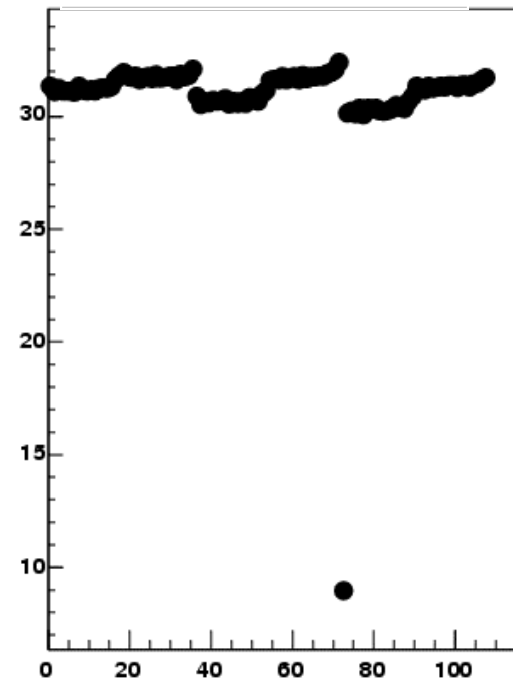
# HOLD timing determination (cont)

- Shaping times measured for left-handed and right-handed PCBs
  - Full PCB was not available for these tests (yet)

Left-handed



Right-handed

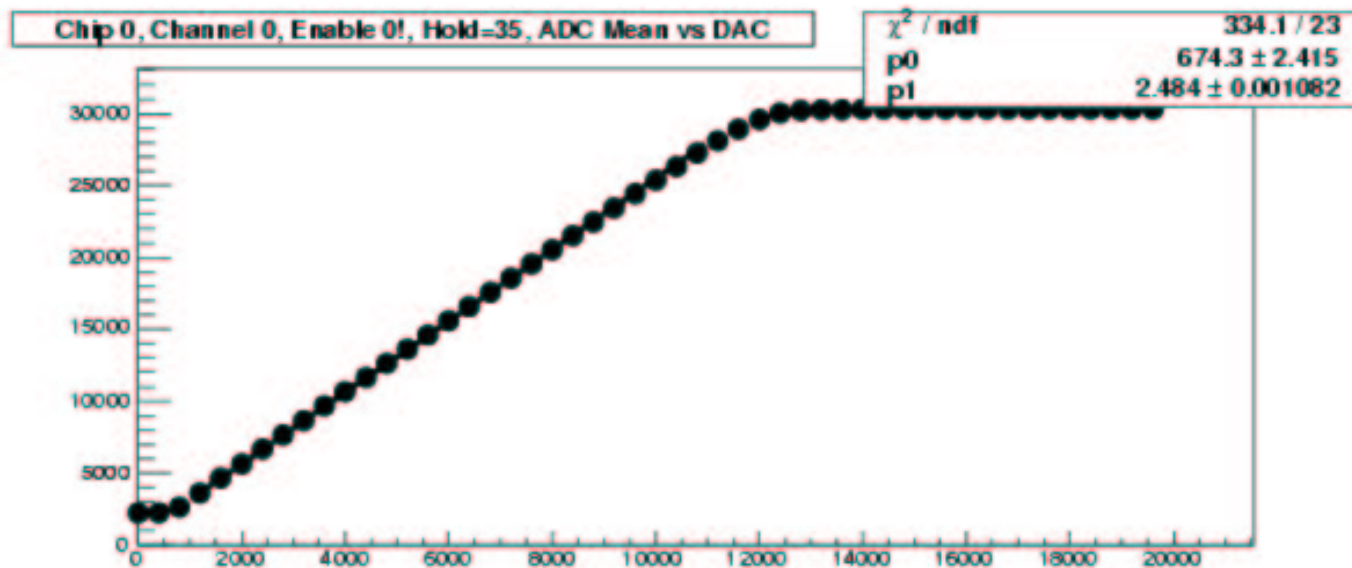


- Shaping times vary chip-to-chip; uniform to  $\pm 3\%$
- One **unresponsive channel** on right-handed PCB
  - Did not look odd in noise plot



# DAC scan

- Typical channel (same as for DAC scan), gain x1

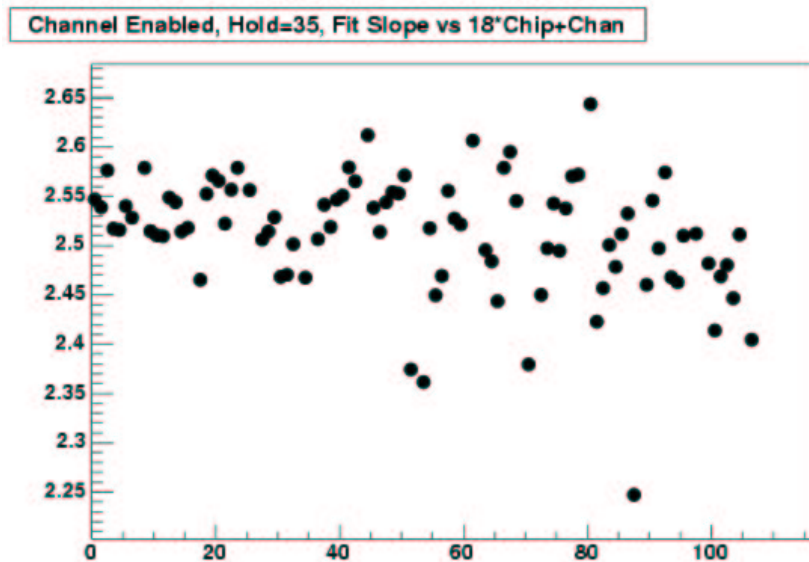


- Slope = **2.484 ADC counts/DAC count** = 9.57V/V
- **High end saturation** at ~ 12000 DAC counts ~244 mV
  - Does not make good use of full DAC range
  - 16-bits is 0-65535 counts = 0-1.33V; five times higher
- **Low end saturation** from CERC board; understood

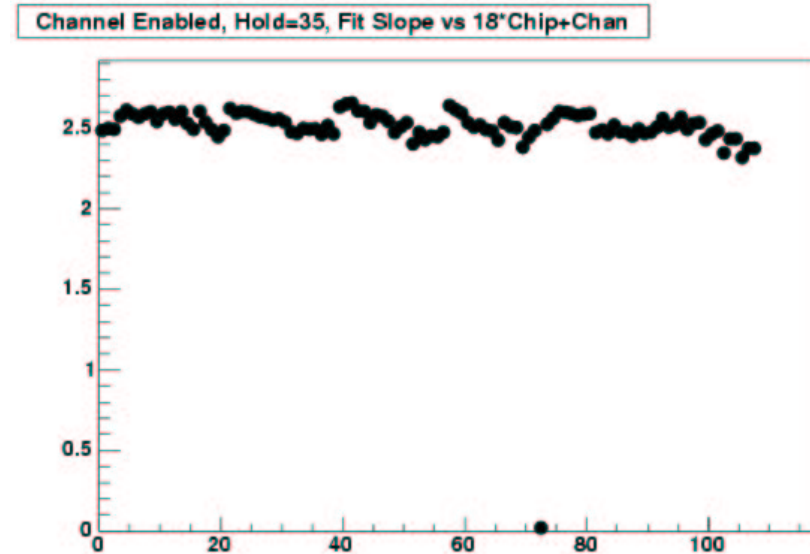
# DAC scan (cont)

- Results for left-handed and right-handed PCBs

Left-handed



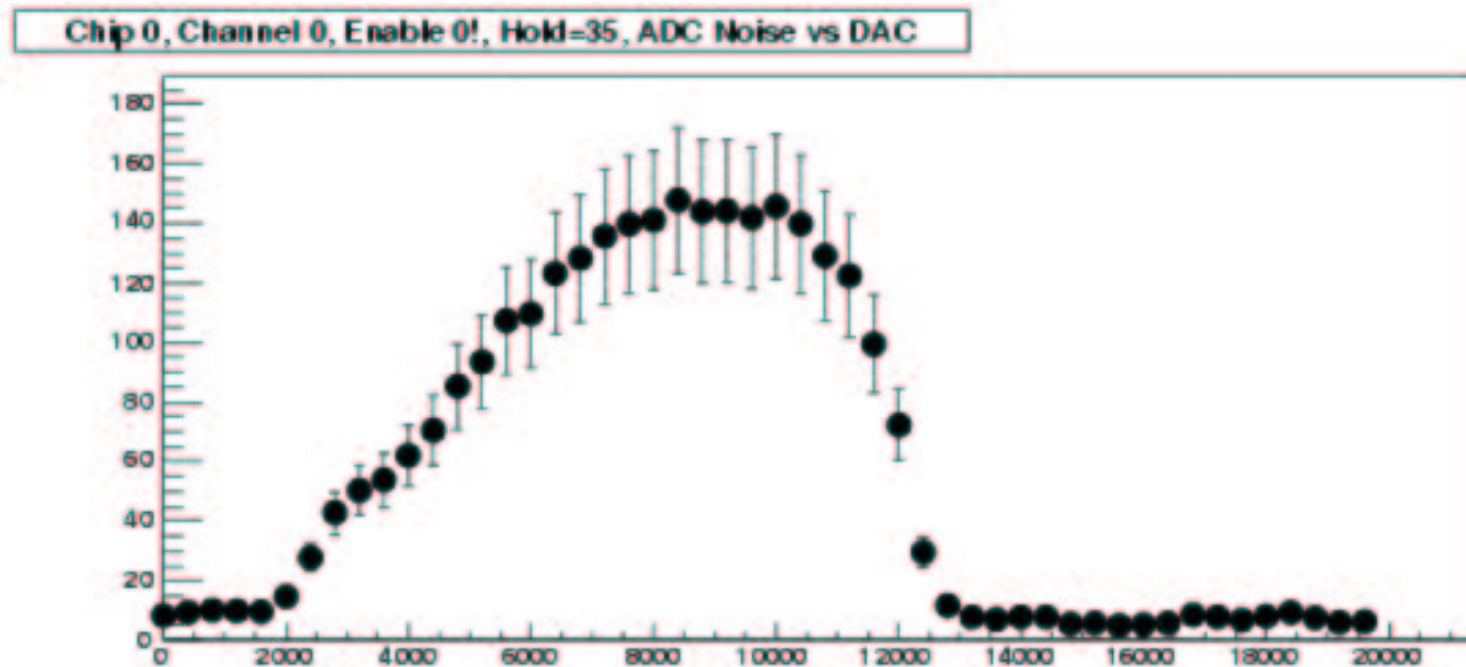
Right-handed



- Responses uniform to  $\pm 10\%$
- Same **unresponsive channel** on right-handed PCB shows up here

## DAC scan (cont)

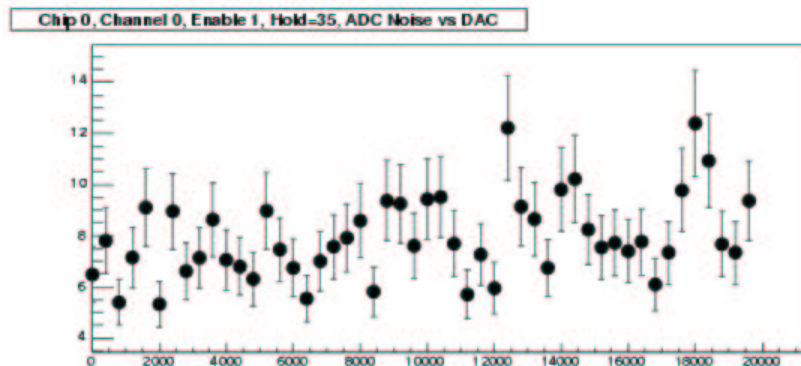
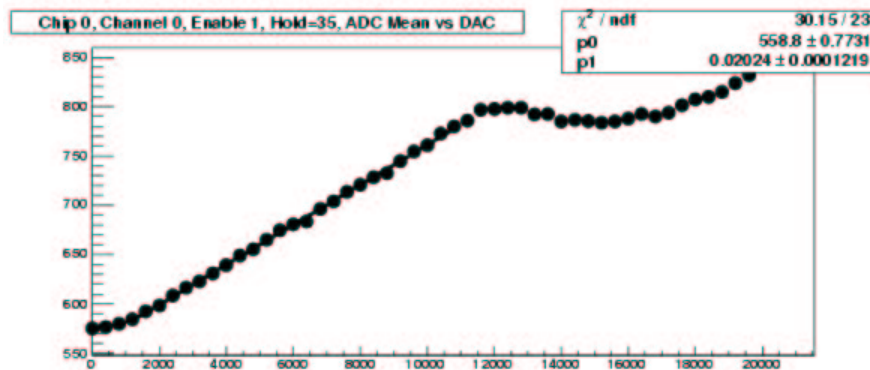
- Typical channel; noise vs DAC setting



- Extra noise  $\sim 0.025$  ADC counts/DAC count  $\sim 10\text{mV/V}$
- Equivalent to extra noise of **1% of signal size**
- Unknown if from calibration circuit or present in real signals
- Clips off at saturation; other noise does not (understood?)

# DAC crosstalk

- Typical non-enabled channel (same as before)

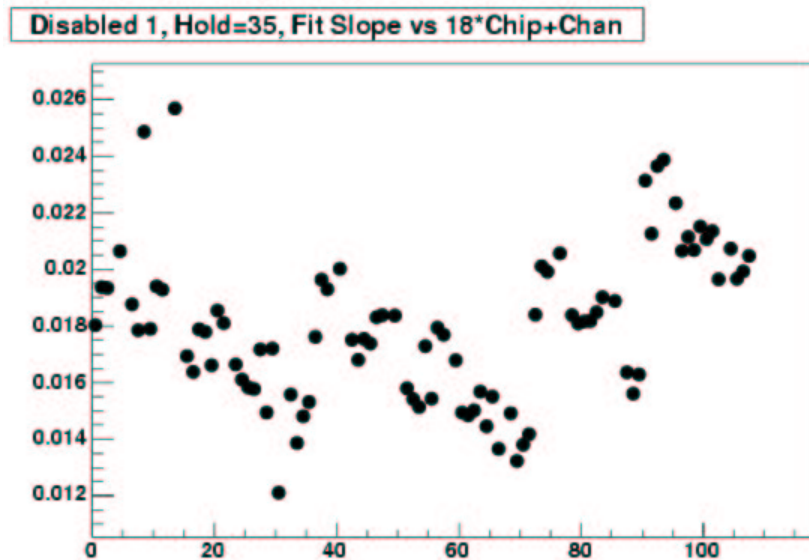


- Slope  $\sim 0.02 \sim 1\%$  of signal slope; **crosstalk is 1%** of signal
- Noise shows no significant increase
- Unresponsive channel looks like this; calibration not connected?

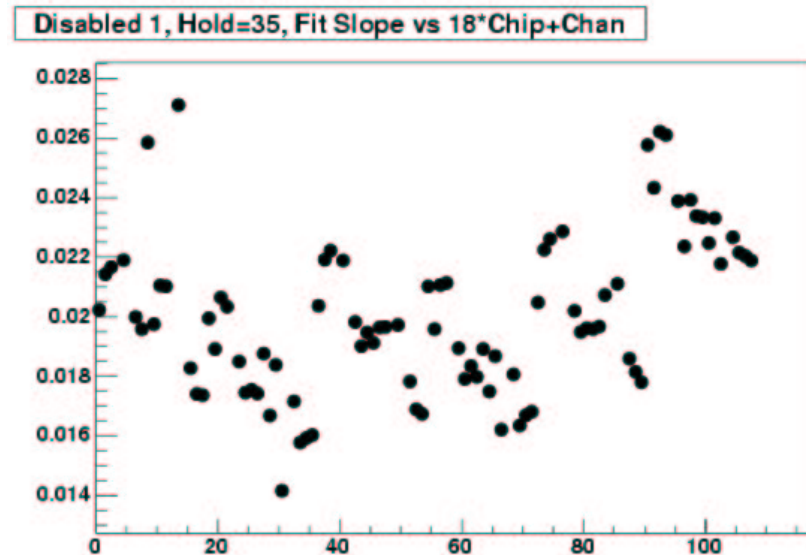
# DAC crosstalk (cont)

- Six different combinations of non-enabled channels
- Typical results for left-handed and right-handed PCBs

Left-handed



Right-handed



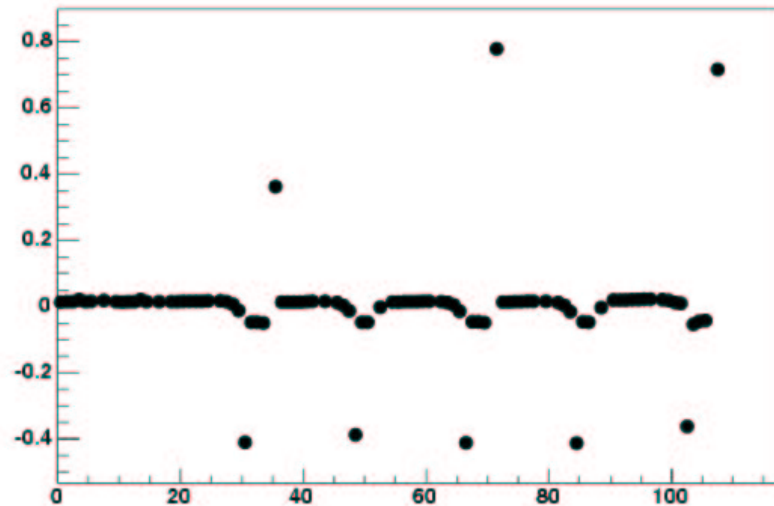
- Crosstalk uniform to  $\pm 25\%$  for most enables...

# DAC crosstalk (cont)

- ...but enables 2 and 5 show odd response

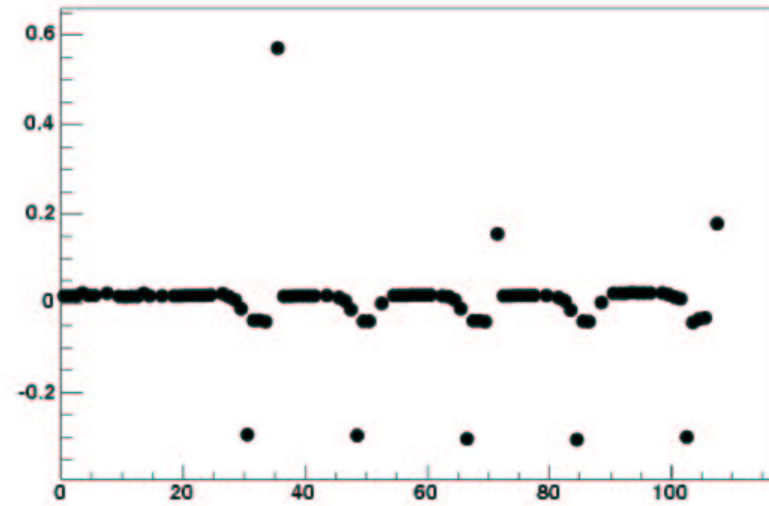
Left-handed

Disabled 2, Hold=35, Fit Slope vs 18\*Chip+Chan



Right-handed

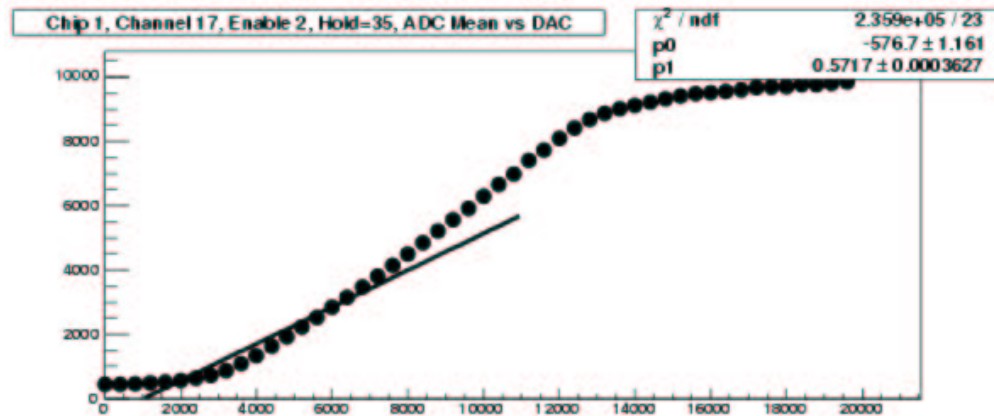
Disabled 2, Hold=35, Fit Slope vs 18\*Chip+Chan



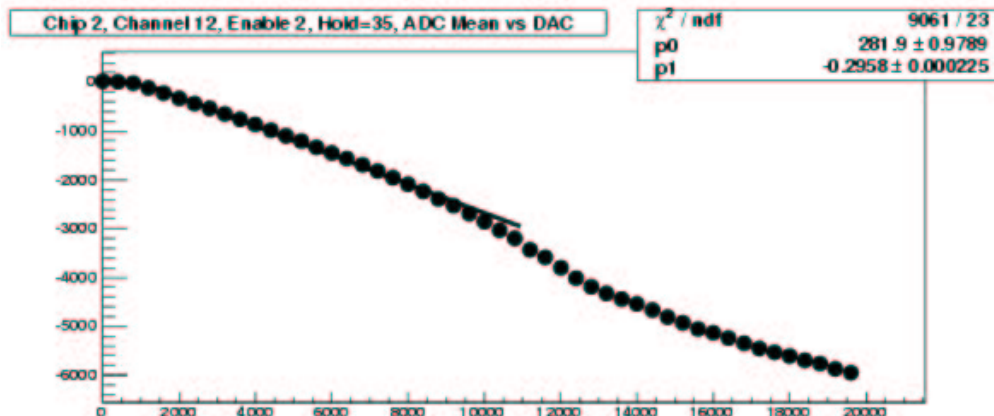
- Systematic on both PCBs
  - Highest are channel 17, lowest are channel 12
- Look at response in more detail

# DAC crosstalk (cont)

- Typical channels for the highest and lowest points



- Channel 17
- Slope  $\sim 1$  ADC counts/DAC count  $\sim$  40% crosstalk

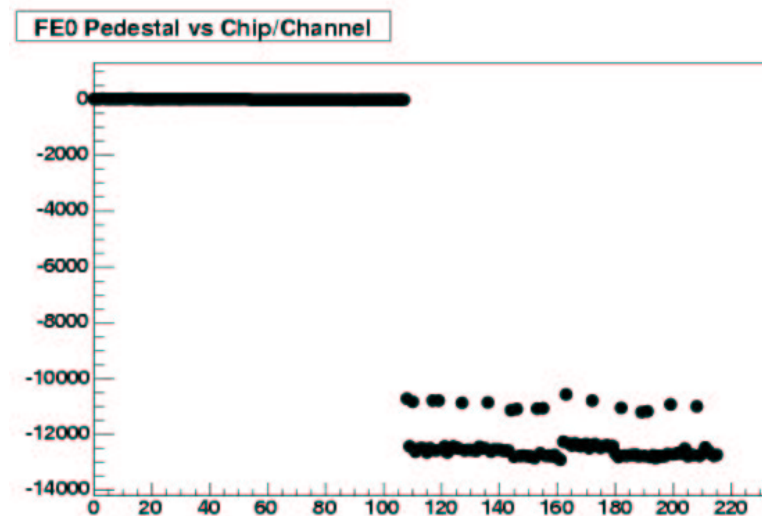


- Channel 12
- Slope  $\sim -0.3$  ADC counts/DAC count  $\sim$  -10% crosstalk

- Unknown if from calibration circuit or present in real signals

# ADC and DAC range optimisation

- Pedestals within **~1000 ADC counts of zero**; required for SSD
- 16-bit ADC range is  $-32768 - 32767$ ; only uses **upper 15 bits**
- One PCB resistor change (in parallel) can shift pedestal negative
- Quick check with  $4.7\text{k}\Omega$  resistor on left-handed PCB

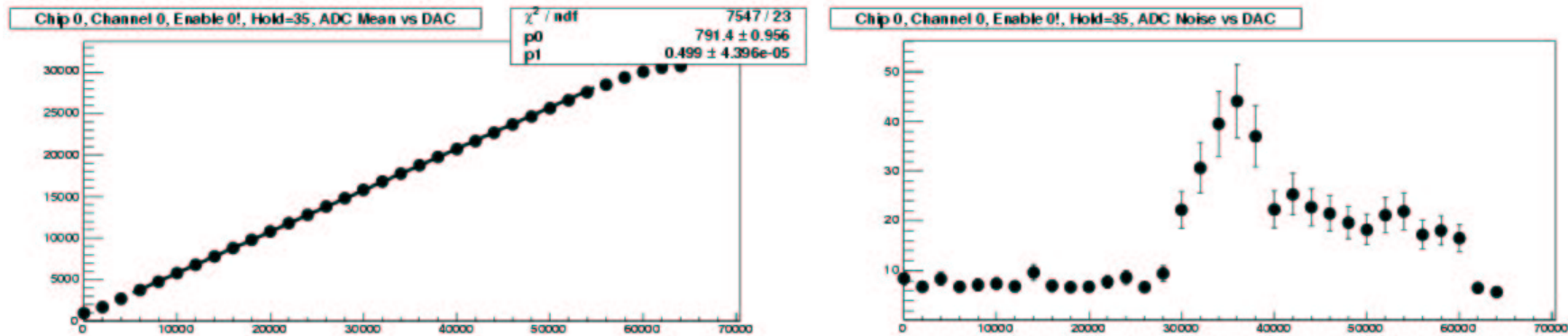


- Pedestal shifted to  $\sim -13000$ ; gain and noise unchanged
- Output range would be  $\sim -13000 - 18000$ ; better centred
  - Can then adjust gain of production CERCs to use most of 16 bit range



# ADC and DAC range optimisation (cont)

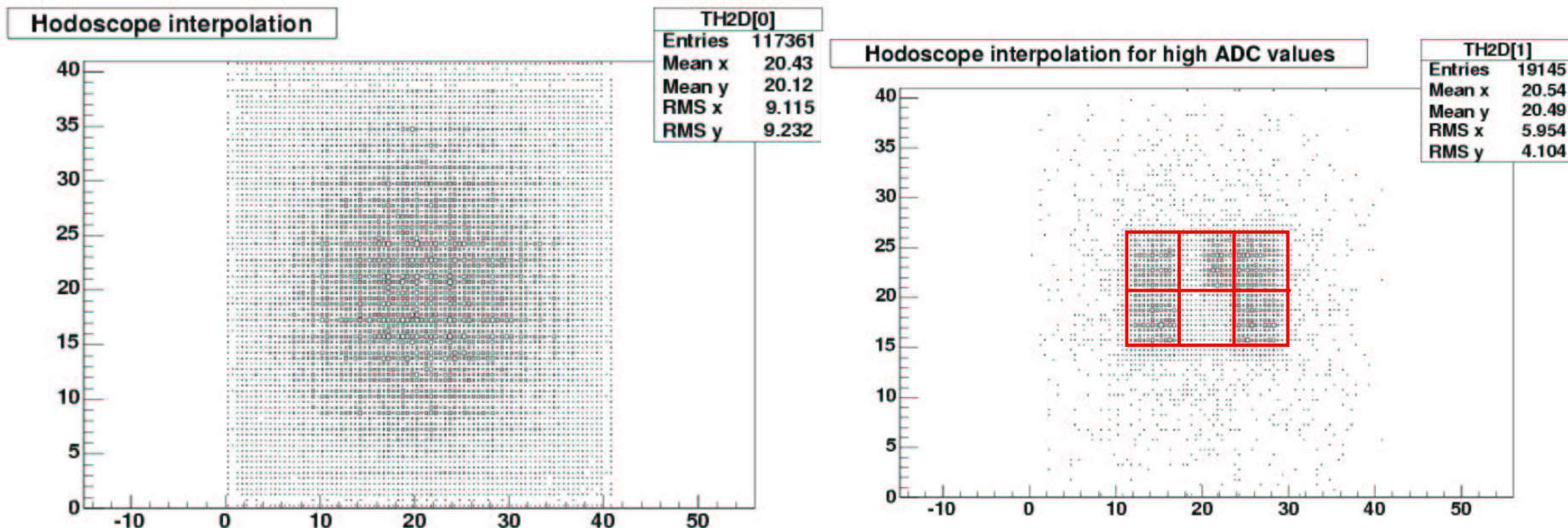
- DAC range underused by factor of  $\sim 5$ ; only uses **lower 14 bits**
- One PCB resistor change (in series) to rescale DAC gain
- Quick check with  $50\Omega$  resistor on left-handed PCB



- Slope = 0.499 ADC counts/DAC count = 1.92V/V
- High end saturation at  $\sim$  **60000 DAC counts**  $\sim$  1.2V
  - Much better match to DAC range
- Noise smaller even allowing for factor of five
  - Implies not DAC related, but due to PCB

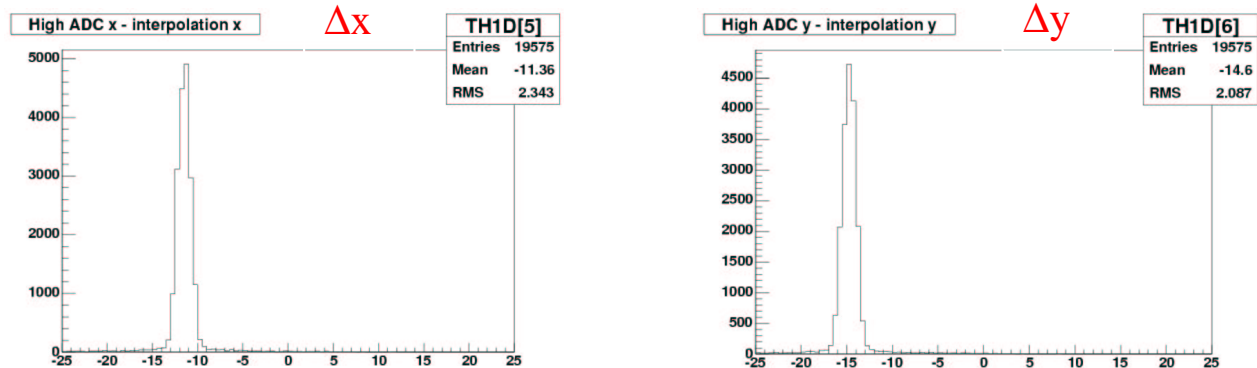
# Cosmics run

- Full PCB used in Ecole Polytechnique teststand, but...
  - Wafer 1 **not depleted**
  - Bad ADC on CERC for wafer 4; half the wafer has **very high noise**
- Ran over weekend 18-21 June
  - Total ~ 57 hours, 130083 events
  - Around 90% have unique track from scintillators
  - Interpolate into plane of PCB; check for ADC value  $> 40$  above pedestal

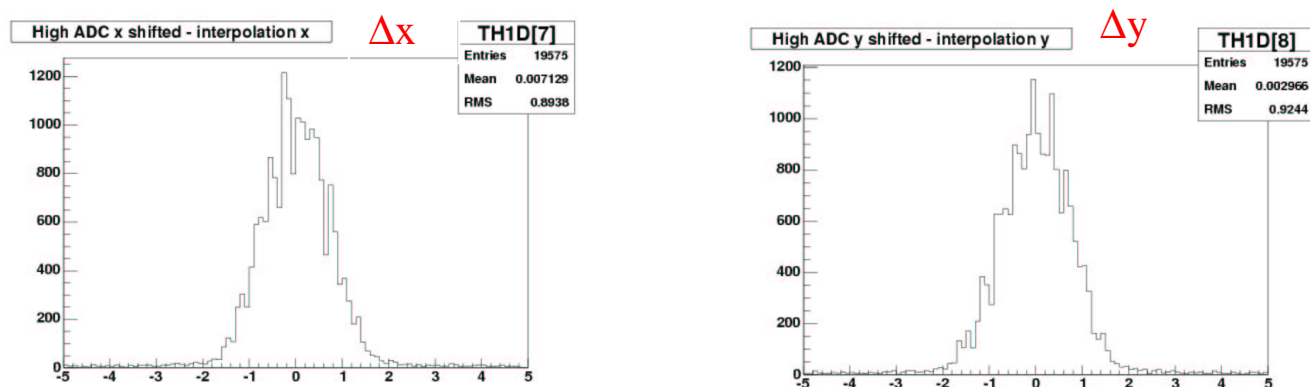


# Cosmics alignment

- Compare x and y **scintillator interpolation** with channel position



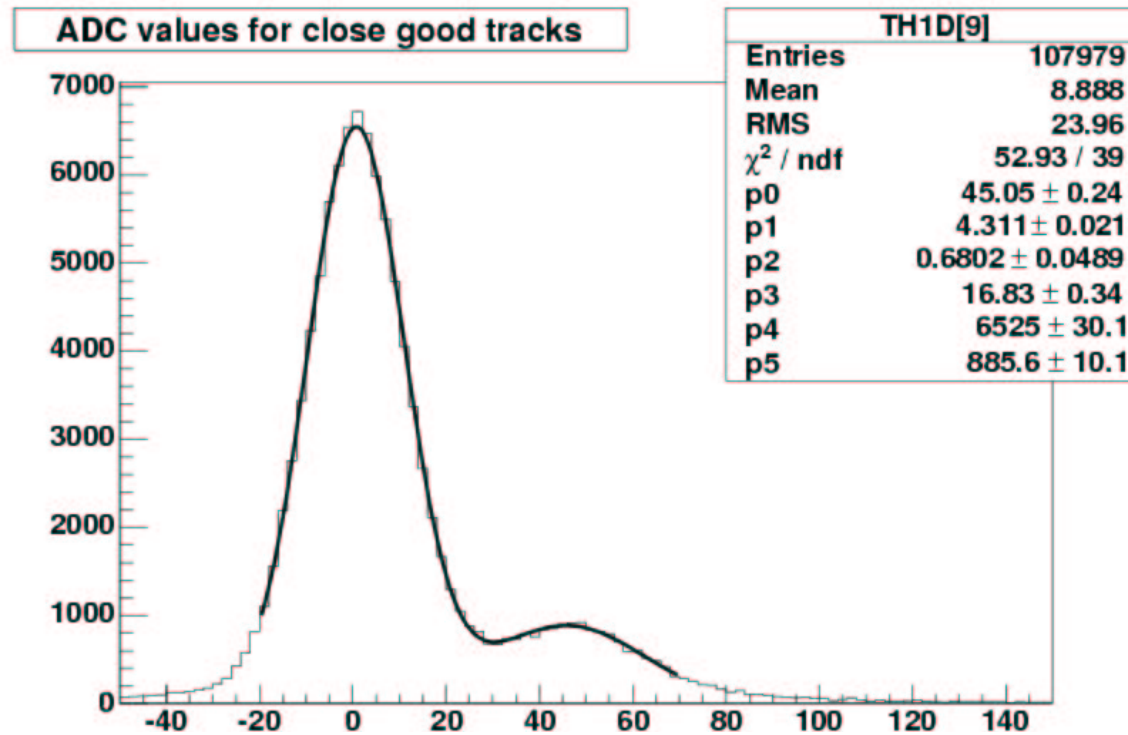
- Single peaks; proves no mis-wiring of channels or readout
- Hence, **align** coordinate systems to agree



- Width of  $\Delta x$  and  $\Delta y$  distributions  $\sim 0.9\text{cm}$

# Cosmic signal response

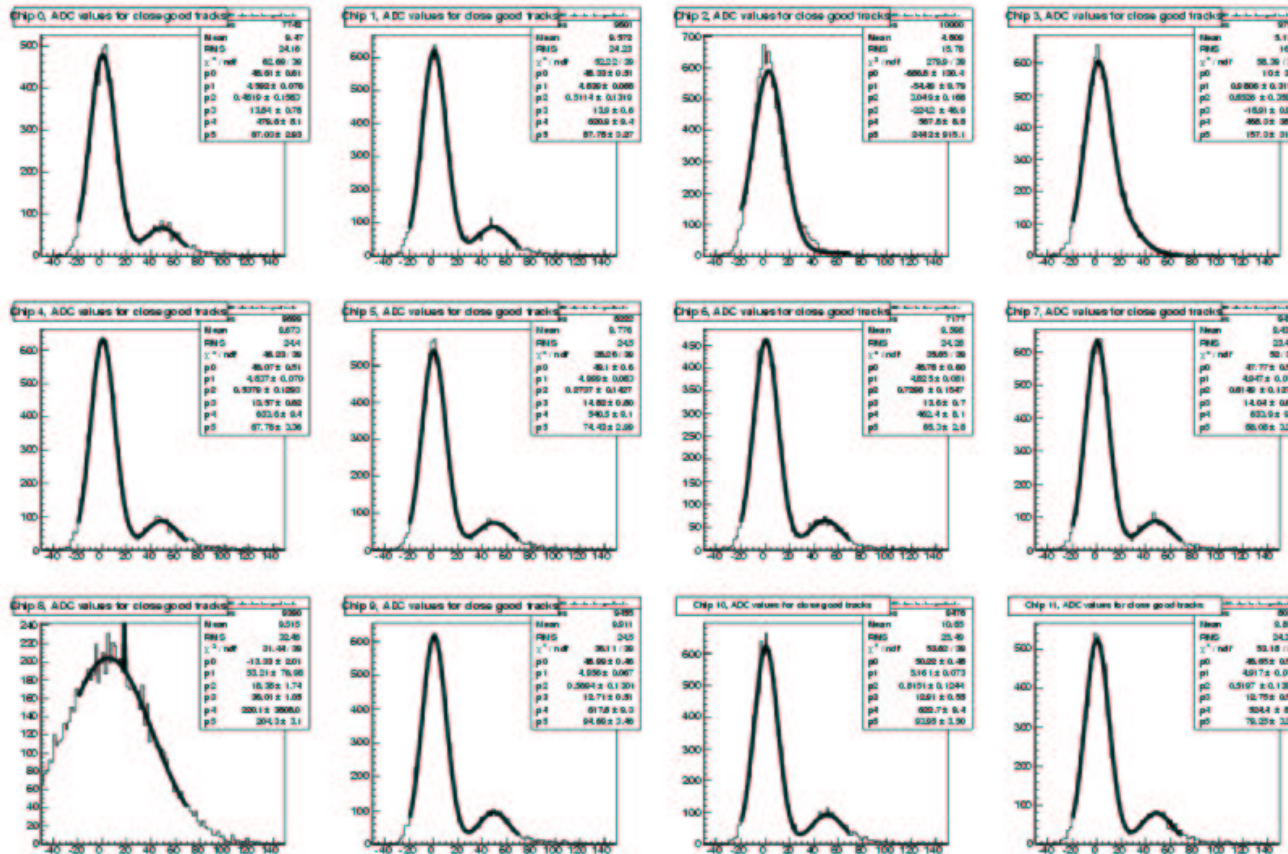
- Require interpolation within 0.9cm of pad centre
- All (good) channels **combined**



- Simple Gaussian fit gives signal peak at **45 ADC counts** = 3.5mV
- But **S/N = 4.3**, i.e. noise is 10.5 counts, not 7 counts

# Cosmic signal response (cont)

- Divide into separate chips
  - Wafer 1 is chips 2 and 3, bad ADC is chip 8



Chips 0-3

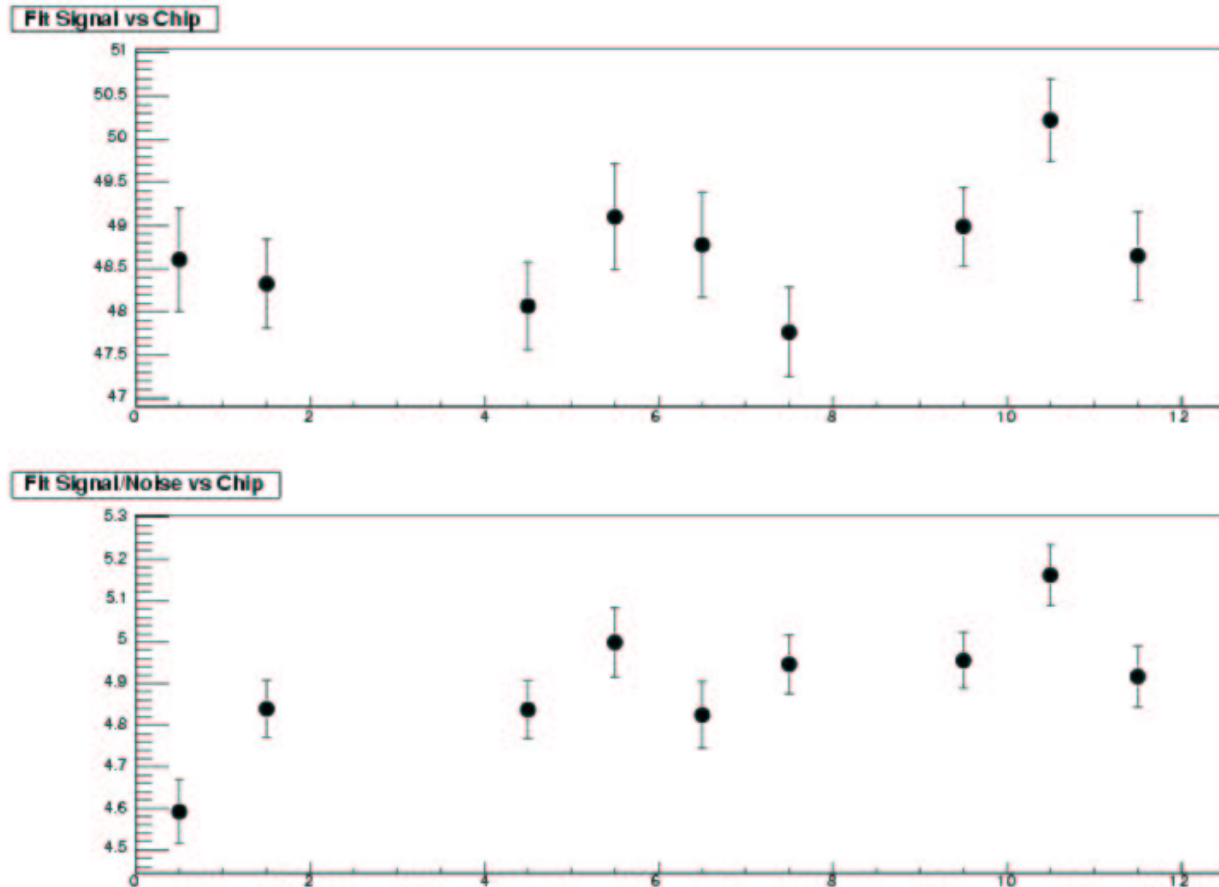
Chips 4-7

Chips 8-11

- Clear signal seen in all good chips

# Cosmic signal response (cont)

- Look at signal and S/N for good chips

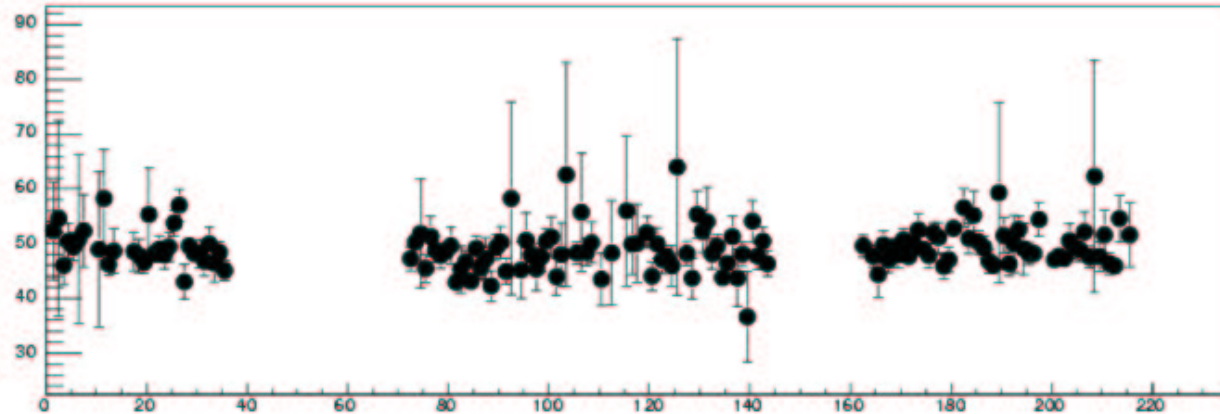


- Both uniform to  $\pm 3\%$
- Fit gives higher **signal**  $\sim 49$ , and hence **S/N**  $\sim 4.9$

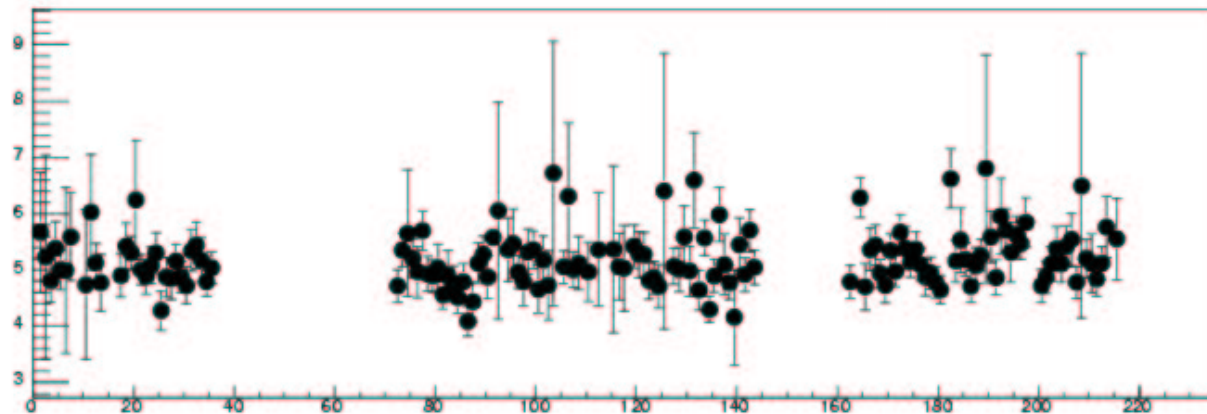
# Cosmic signal response (cont)

- Pushing the stats, look at signal and S/N for **good channels**

Fit Signal vs 18\*Chip+Chan



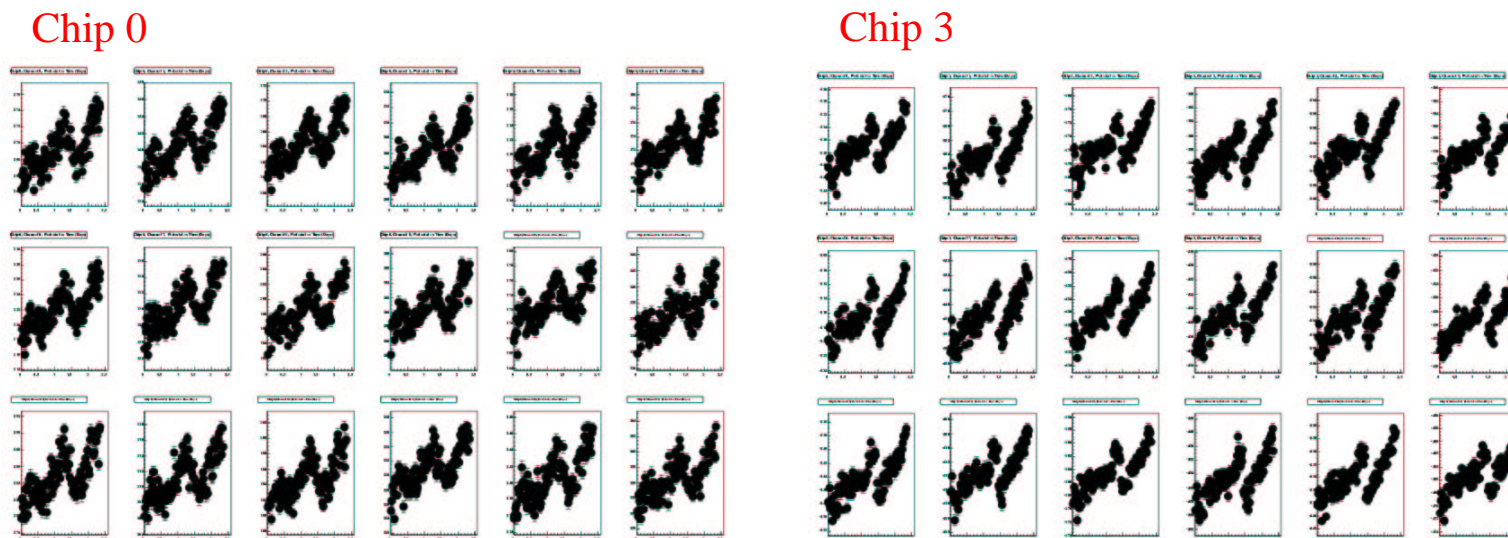
Fit Signal/Noise vs 18\*Chip+Chan



- No obvious bad channels...

# Stability over cosmic run

- Continuous data for 2.5 days; check pedestals vs time
- Drifts of up to 15 counts ( $2\sigma$ ) seen
- Same trend in all channels
  - Very similar within a chip, less so chip-to-chip



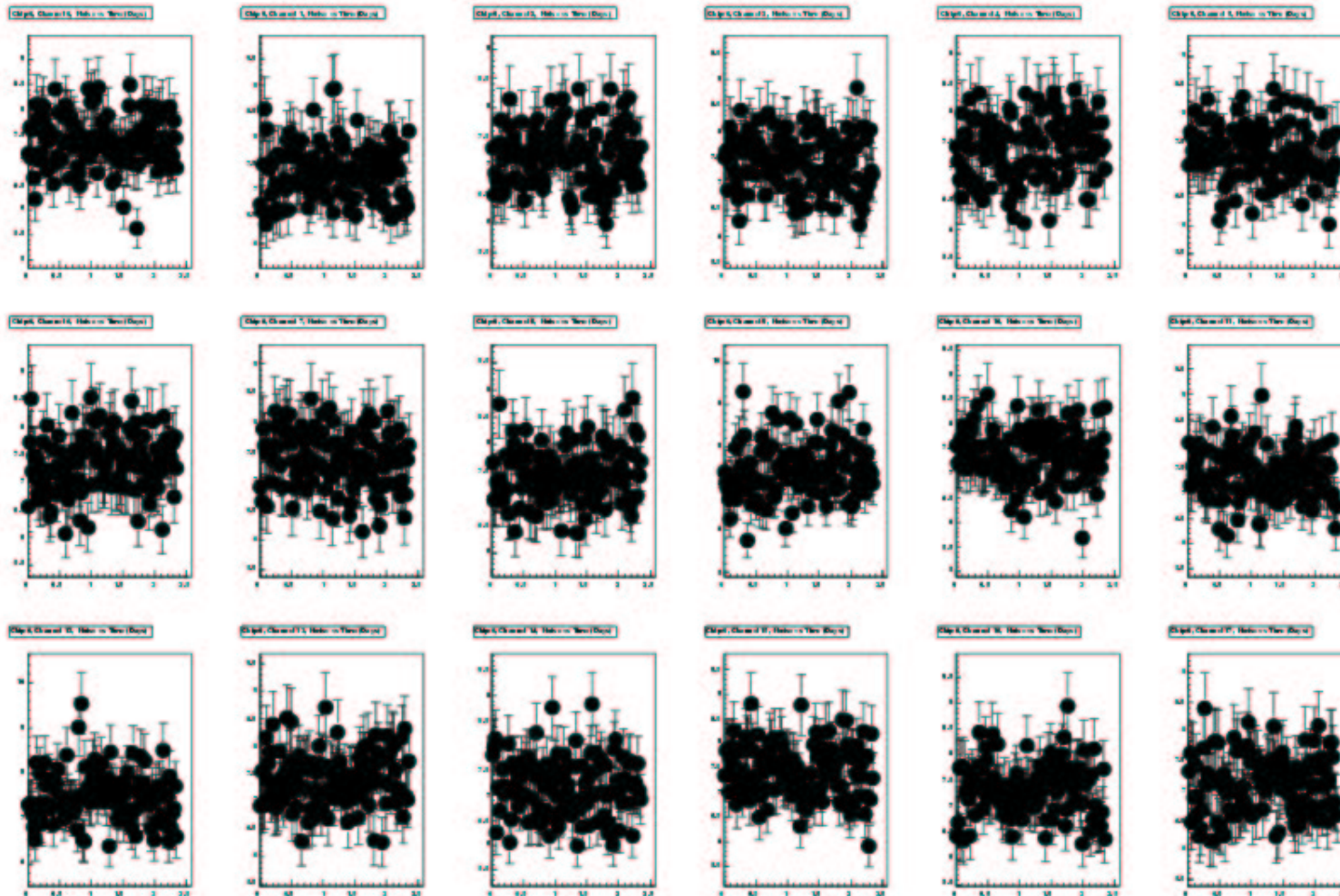
- **Temperature?** Not measured during run
- Need to monitor temperature in future to check this
  - Need temperature sensors **mounted on PCBs and/or wafers?**



# Stability over cosmic run (cont)

- Noise is much more stable; e.g.

Chip 0



# Conclusions

- Basic conclusion is that the system **works!**
  - We have all parts of the VFE PCB functioning
- Some **oddities** seen in calibration
  - Noise depends on DAC, some channels have high crosstalk
  - Must determine if due to calibration or if will occur in real data; how?
- Adjustment of the VFE PCB would **optimise** match to CERC
  - Working point for ADC and gain for DAC
- CERC has some **bugs**
  - Fixes are in hand and will be implemented for the production version
- **Signal** seen around 50 counts, **noise** around 7 counts
  - But realistic signal/noise in cosmics around 5
- Significant pedestal **drifts** observed
  - Will need frequent pedestal measurements during run; between spills?
  - Will need temperature monitoring?