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# Tech Board: DAQ/Online Status

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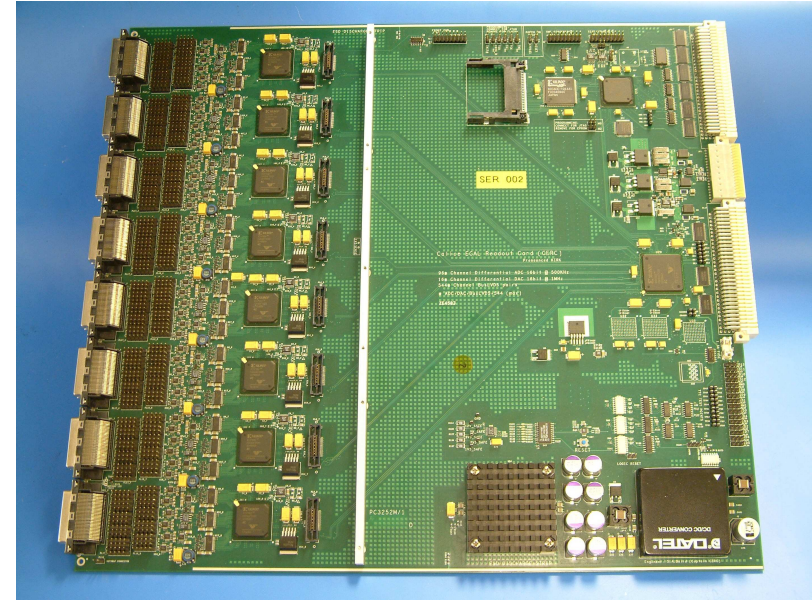
# Feb05 Technical Review outcome

- **Recommendations**

- Proceed with the hardware purchases as planned.
- Start on the firmware and software work immediately so as to optimize the chances of getting all changes completed by June.
- Test the new CRC boards to assess their performance as soon as possible.
- Perform tests with the multiple PCI card architecture to assess its performance; this will include AHCAL integration tests.
- Decide on how the slow controls and readout will be handled and implement at least the ECAL side of this before the June run.
- VME crates should be checked to see if they can work at low voltages. A solution needs to be found if they do not.

# CRC hardware status

- Need **13** CRCs total
  - ECAL requires **6** CRCs
  - AHCAL requires **5** CRCs
  - Trigger (probably) requires **1** CRC
  - Tail catcher requires **1** CRC
- Status
  - **9** exist (2 preproduction, 7 production) and are internally tested (~90%)
  - **7** are being manufactured via RAL, delivery in Nov (?)
  - Should have **13 plus 3 spares** by end of year
  - There are 2 prototype CRCs which could be used if really necessary
- Testing
  - Much better to test AHCAL CRCs in UK **before** shipping to DESY
  - Need test station (crate, VME-PCI, etc) in UK...
  - ...but also need to ship out existing system to DESY for ECAL cosmics
  - May be able to use (Atlas) system in UCL?



# DAQ hardware layout

- **DAQ CPU**

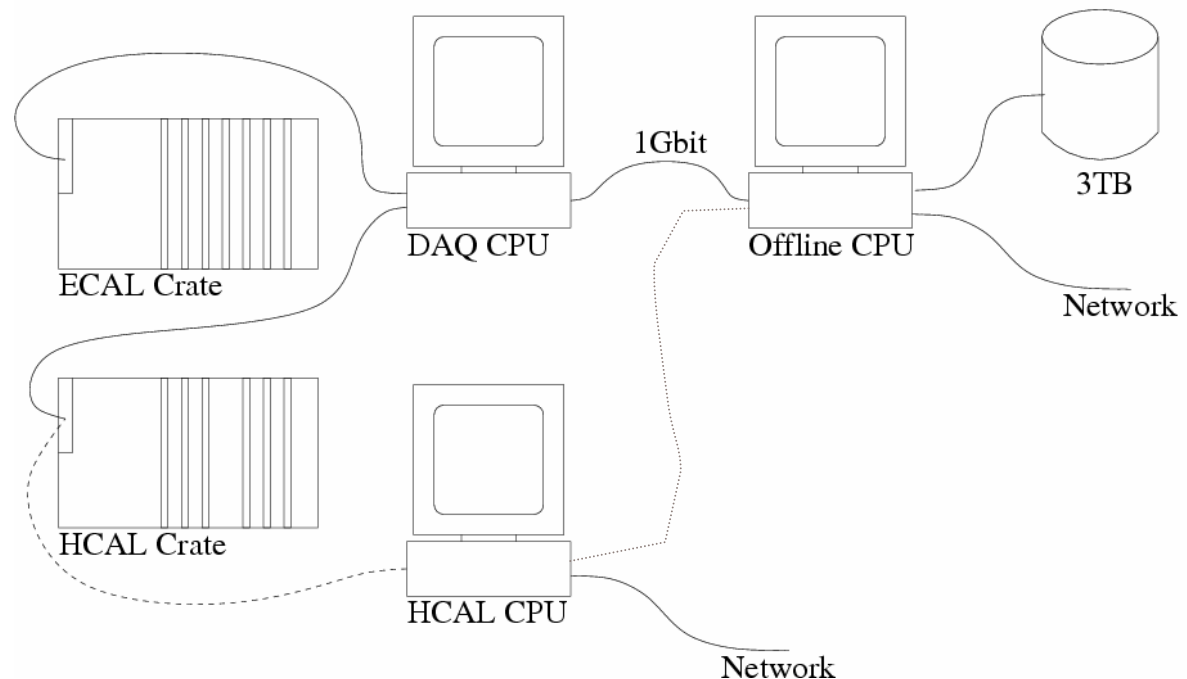
- Trigger/spill handling
- VME and slow access
- Data formatting
- Send data via dedicated link to offline CPU
- Redundant copy to local disk?

- **Offline CPU**

- Write to disk array
- Send to permanent storage
- Online monitoring
- Book-keeping

- **HCAL PC**

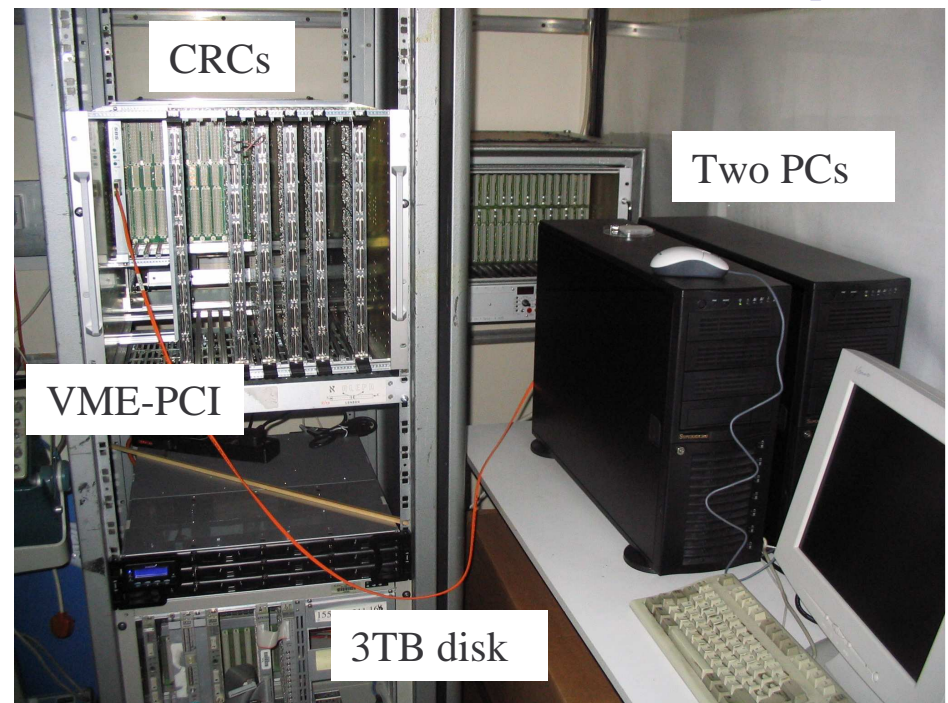
- Partitioning
- Alternative route to offline PC



# Status of non-CRC hardware

- Two 9U **VME crates** with custom backplanes needed
  - One for ECAL and trigger, one for AHCAL and tail catcher
  - Two crates exist at DESY but we have no spares (for parallel testing, etc)
  - Only one backplane exists, not thoroughly tested yet
- Three **VME-PCI bridges** needed
  - All purchased and tested
  - Plus fourth old-format PCI card
- 108 **mini-SCSI cables** needed (plus spares)
  - 60 ECAL, 40 AHCAL, 8(?) TC
  - Purchased 70 but not halogen free (so cannot be used at CERN)
  - Need to buy more
- **Three PCs** and disk
  - All purchased and tested

Test station  
at Imperial



# Firmware status

- **Three** different FPGA firmware designs needed
  - **VME**: can use CMS version directly; no work needed
  - **FE**: completely new, but effectively finished
  - **BE**: two parts to this
    - “Standard” BE: data handling on all CRCs
    - “Trigger” BE: specific for CRC being used for trigger control
- **Standard BE** firmware is critical path; not complete
  - Can only buffer up to 500 events, but need 2000
  - Can only buffer in 2MBytes of memory, but need 8MBytes
  - Without both of these, data rate will be reduced by **factor of four**
- **Trigger BE** firmware needs work also
  - Trigger data (including detection of multi-particle events) can only be read via slow serial path: limits rate to ~20Hz (c.f. 1kHz, not 100Hz)
  - Need to route trigger data into 8MByte memory so can read via fast Vlink
  - Fallback is not to read these data



# Slow controls/readout status

- Various slow controls and readout data are collected by DAQ
- **CRC** slow data
  - Temperatures: 22 different probes over surface of board
  - Power: 5 voltage level measurements of backplane inputs
  - Read out standardly during run: no work needed
- **ECAL** power and temperatures
  - Plan to read out via stand-alone PC (not yet existing)
  - Will need to interface to DAQ when it appears
- **ECAL** stage position
  - Stage controlled by stand-alone PC
  - Readout interface to DAQ tested and working
- **AHCAL** slow data and stage position
  - All centralised in stand-alone PC (running H1 slow control program)
  - Readout and control interface to DAQ tested; needs further work to be complete

# Crate power compatibility

- Crates need to work in **US and Europe**

- Not tested; never been shipped to the US

- UK crate is **CERN/LHC spec**

- User's manual at

- [http://ess.web.cern.ch/ESS/ePoolDoc/239\\_1261.pdf](http://ess.web.cern.ch/ESS/ePoolDoc/239_1261.pdf)

- states on page 2

- “The power supplies are equipped with a “World”- mains input, which works properly from 94VAC up to 264VAC and within a frequency range of 47 to 63Hz.”

- **AHCAL** crate should also be **OK** for the US

- Rated at 100-250V and 50-60Hz



# Work to be done

- Debug future versions of BE **firmware**, test new **CRCs**
  - Hope this can be finished by end of year
- Complete major **rewrite** of online software (and slow readout)
  - THE major task at present; target is again end of year
- Push **maximum trigger rate** during spill; currently **2kHz**
  - This satisfies basic requirement but would benefit from faster rate
- Push **maximum readout rate** during transfer; currently **50Hz**
  - Requirement is 100Hz; some tricks will be needed to achieve this
- Test **parallel access** for two PCI cards in one PC
  - PCI bus should not limit compared with two VME buses but need to check
- Test **socket access** for two PCI cards in two PCs
  - Each reads independently but need to merge records afterwards
- Integrate existing **beam line** equipment at CERN and FNAL
  - Big uncertainty at present