DAQ/Online: readiness for DESY and CERN beam tests

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Update of Orsay talk; concentrate on progress since then
CRC hardware production

- Need 13 CRCs total (8 for DESY)
  - ECAL requires 6 (4) CRCs
  - AHCAL requires 5 (2) CRCs
  - Trigger (possibly) requires 1 (1) CRC
  - Tail catcher requires 1 (1) CRC
- 18 exist: 2 prototype, 9 ECAL production, 7 AHCAL production
  - Prototypes SER001-2; less reliable and will only be used if necessary
  - ECAL production SER003-011, AHCAL production SER012-018
- AHCAL board production thicker than ECAL 😞
  - Change to lead-free PCB manufacturing
  - Luckily just fit into LHC-spec crate rails we will use
- Very difficult to make more CRCs
  - Almost all boards have needed some rework after delivery
  - Adam Baird (CRC designer) leaving RAL in July
  - Would need to train up someone to debug any new boards
CRC hardware status

- Not all CRCs have all channels working
  - Adam still working on several, but remaining errors are hard to fix
- Of production CRCs, 9/16 are (almost) fully working
  - SER005, SER006, SER009, SER011, SER013-017 (except one bad input)
- The rest have a variety of errors, no fixed pattern
  - SER003: FE0 dead, memory error in BE (fixable in f/w?)
  - SER004: Connector problems on 3 FEs, ground problems on 2 FEs
  - SER007: FE3 noisy
  - SER008: FE5 memory error (fixable in f/w?)
  - SER010: FE6 two dead ADCs (=36 channels)
  - SER012: FE4 dead, FE0 noisy
  - SER018: Have not even seen this one yet!
- With careful cabling, can make a complete system from the above
  - Of 16×8=128 FEs, we have 101 fully working now and need 45+40+1+4=90
Other hardware

• Second custom backplane installed at DESY beam area crate
  • Seems to work for slots tested; more thorough test needed
  • Includes connectors for crate-to-crate trigger cable
  • Must bring two crates together to test this

• Need to test two PCI cards in same PC
  • Also needs both crates in same place plus DAQ PC (currently at Imperial)

• Central DAQ nfs mount of 3TByte disk array now enabled
  • Other PCs connected to DAQ local network can see data directly
  • Allows monitoring/histogramming without using CPU of DAQ PC

• CERN beam line readout
  • Wire chambers (need a TDC) and Cherenkov detectors (need an ADC)
  • Hard to get detailed information; even number of channels is uncertain
  • CERN-recommended TDC only buffers 32 events before needing readout; this compares with our aim of ~1500 events per spill
DESY tracking

• Major issue of last run was flammable gas in drift chambers
  • Required 24 hour shift cover by two people, even when no beam
• We will try to use non-flammable gas
  • Minimal risk to (non-CALICE) chambers if using same gas types
  • Previously Ar:Ethane mixed 50:50; non-flammable needs 96:4
• Needs careful check of efficiency vs HV to be sure it is usable
  • Need dedicated runs in DESY beam for this
• This should be done soon so can plan shifts if unusable
  • Premixed gas ordered (thanks to DESY crew)
  • TDC reinstalled (except for trigger input) and working
  • Maybe try new gas within a week?
• Need volunteer to look at data to measure efficiency
  • Must give immediate feedback to prevent setting HV too high
  • Really needs to be at DESY or in very close contact
Firmware status

• Three different FPGA firmware designs needed
  • VME: can use CMS version directly; no work needed
  • FE: completely new, but effectively finished
  • BE: two parts to this
    • “Standard” BE: data handling on all CRCs
    • “Trigger” BE: specific for CRC being used for trigger control

• Standard BE firmware
  • Can only buffer up to 500 events, but need 2000
  • Can only buffer in 2MBytes of memory, but need 8MBytes
  • First version to fix this tested last week; some bugs found

• Trigger BE firmware
  • Trigger data (including detection of multi-particle events) can now be read via fast Vlink: allows ~100Hz readout including these data
  • Cannot also read ADCs in same CRC; this should be fixed
Main issue has been event readout synchronisation

- Real triggers can come at any time, i.e. any phase compared to the CRC 40MHz clock
- Cannot synchronise trigger to clock as would lose timing resolution; some signals (e.g. HOLD) timed from trigger leading edge
- Triggers close to clock edges caused different timing in different FEs
- FE-to-BE data transfer not synchronised so data buffering corrupted

Now use falling edge of trigger to synchronise FE-to-BE transfer

- This can be synchronised to clock without affecting HOLD
- Tests in beam area at DESY show zero event synchronisation errors in ~5M events; previous rate was around 10%

Do we need to fix up existing 2006 ECAL data offline?

- I.e. merge various parts of event during LCIO conversion
- Would we be better off retaking cosmics data when HOLD found?
Slow controls/readout status

• Various slow controls and readout data are collected by DAQ
  • This is the route to the LCCD database for long-term storage

• ECAL power and temperatures
  • Read out via stand-alone PC; will need to interface to DAQ
  • I had brief contact with LLR people since Orsay
  • Heard nothing since so progress unknown

• ECAL stage position
  • Stage controlled by stand-alone PC
  • Readout interface to DAQ tested and working
  • Passive read from DAQ only; we decided at Orsay we never want control

• AHCAL slow data and stage position (for CERN only)
  • All centralised in stand-alone PC (running H1 slow control program)
  • Readout and control interface to DAQ tested; stage position controllable
  • No other data sent yet; needs more work to be complete
ECAL “Read19” issue revisited

• Previously thought: read through multiplexer exactly 18 times
  • Output line left floating; drifts to position with high current
  • Contributes to rate dependent pedestal shift and hence extra noise
  • Decided at Orsay to run with 19 samples

• But Götz found the noise is worse with 19 reads!
  • See his talk for more details (I hope)

• We need to decide how to run
  • 18 or 19 samples for each event?
  • RESET before or after HOLD in timing sequence?

• We should decide this soon!

• Minor correction to Orsay talk
  • Reading 19 does not have to increase data volume
  • Can mask out last read from ADC so only 18 recorded to disk
Online software

• Biggest issue has been “Marius problem” (identifier, not causer!)
  • Only for first event in configuration (but not reliably repeatable)
• Symptom is VME bus error causing exception
  • Skips rest of read so ADC data structure is incomplete
  • Rest of event data interpreted as ADC data; complete garbage
  • Often causes offline crash as apparent number of ADC words is enormous
• Work around now installed; belt and braces
  • Catch exception immediately and retry read; never seems to fail again!
  • Also be more careful about integrity of data structure in case of errors
  • This should be stress tested as soon as possible!
• Fundamental cause not yet understood
  • Something during configuration causes bus error on first read of a valid VME location
  • Not consistent for all configurations nor for single reads vs block transfers
Remaining corruption issues

- Fixing major problems then reveals more minor ones
  - From $10^{-1}$ to $10^{-5}$ level
- Some events have no trigger!
  - Seems due to trigger occurring at same time as trigger BUSY reset
  - BUSY is never lowered, so next trigger does not happen
  - Whole event has no data and trigger counters do not increment
  - Rate proportional to pre-BUSY trigger rate; $\sim 2 \times 10^{-5}$ per kHz
  - No obvious solution; may have to live with this one
  - Completely random so event can be ignored with no bias
- VME driver cannot handle signals (Ctrl-C, etc) correctly
  - Signals used to start runs, end runs, end program, etc.
  - Sometimes get corrupted data if reading when signal arrives
  - Usually only last event of run
  - Possible to rewrite control to avoid use of signals; significant effort
Other software issues

- **Run size** an issue
  - In November Tech Board review, decided to allow large runs > 2GBytes
  - Roman now confirms file sizes limited to < 2GBytes by dCache
  - LCIO currently makes one output file per run; would be > 2GBytes
  - Chop runs into smaller chunks; e.g. into configuration periods? Some runs are only one configuration so no guarantee this helps
  - Need to decide on a solution soon; could be significant work

- **Run sequences** requested
  - Predefined lists of runs which can be executed sequentially
  - E.g. ECAL calibration combining HOLD scan and DAC scan
  - No intrinsic obstacle, but quite a lot of infrastructure; under development

- **Make accessor aware of new versions** of subrecord objects
  - Not critical but would be useful for easy backward compatibility
  - Probably easy to implement but significant effort to maintain
Summary

• Hardware is **usable** for DESY run
  • Remaining faults on CRCs getting hard to fix
  • Final DAQ system cannot be shipped to DESY until finished (Mar?)

• Firmware is **usable** for DESY run
  • Duplicated event readout should now be fixed
  • Starting to debug large buffering needed for CERN beam run

• Software is **usable** for DESY run
  • Need to check on corruption error and understand driver better
  • Several improvements in the pipeline; timescale uncertain
  • Do we need to limit run sizes again because of LCIO/dCache?

• Other items for DESY runs
  • Slow controls and readout **needs work**
  • Beam line equipment **needs work**