CALICE ECAL Readout Electronics: Project Specification

October 14, 2002

1 Introduction

The CALICE collaboration plans to test a prototype tungsten-silicon electromagnetic calorimeter (ECAL) with a beam in 2004. The prototype will have around 10000 channels and the UK hopes to provide the readout electronics and data acquisition for this experiment. There will also be a hadronic calorimeter (HCAL) prototype and, although the UK is not funding any electronics, it would be useful if the ECAL readout electronics could also be used for the HCAL. In this case, the non-UK groups involved would pay for the extra boards needed.

The prototype calorimeter will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers and the three silicon wafers in a row in each layer will be mounted on PCB's which route the diode signals to the very front end (VFE) chips which provide amplification and shaping. Each layer therefore consists of three such VFE-PCB's.

The system will be triggered using external logic based on fast scintillator detectors in the beam line. This trigger will be supplied to the readout electronics via lemo cables, presumably at NIM levels.

The diodes, VFE chips, VFE-PCB's and their power supplies, as well as the beam trigger and its logic, will be provide by non-UK groups, while the UK will need to provide all the readout electronics downstream and the data acquisition (DAQ) system to read it out. All signals from each VFE-PCB are assumed to be routed through a single connector. This will provide the well-defined interface between the two parts of the electronics. The UK will provide any cables needed from this connector.

2 Overview of proposed readout system

An overview of the proposed ECAL system is shown in Fig. 1. The system has the cables from the VFE-PCB's connecting directly to 6U VME boards, with all the necessary readout electronics on these boards. The system would run triggered and read out each event before allowing the next trigger to occur. This would be controlled by a single VME trigger handling board which distributes the trigger across the backplane. No data reduction is done in hardware, so all 9720 channels are read out for each trigger.

The basic unit of the readout is based on the 90 VFE-PCB's. These each hold 108 channels which are multiplexed onto 6 lines. It would be convenient to contain the whole system in a single standard VME crate of 21 slots. Assuming a PCI/VME interface card and a single width trigger card, this leaves 19 slots for the readout boards. The obvious division is then 15 readout boards, each handling the signals from 6 VFE-PCB's, equivalent to 2 of the 30 layers of the calorimeter.

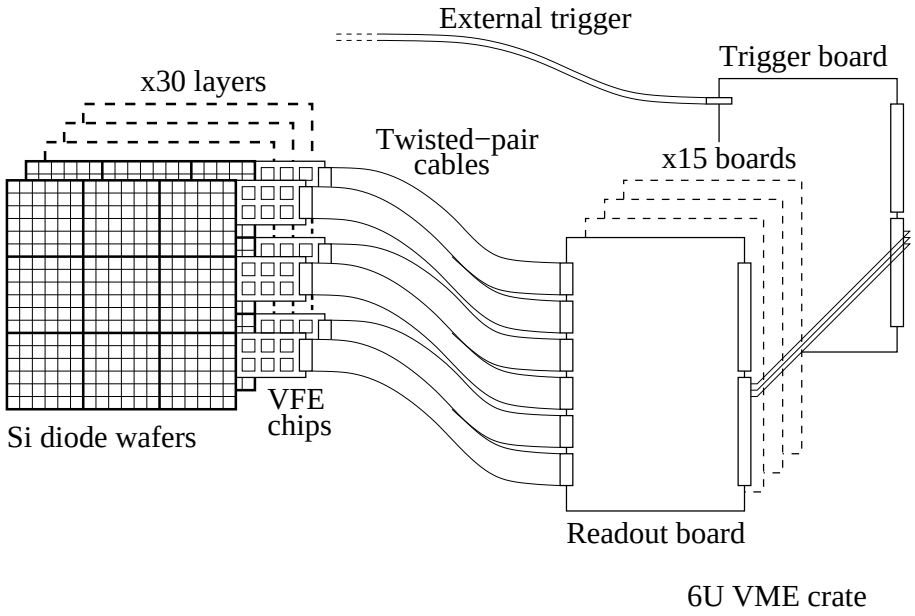

Figure 1: Overview of the proposed ECAL readout system.

Although the ECAL electronics will fit into a single VME crate, if the readout boards are also used for the HCAL, then more than one crate will be needed. Hence, the trigger board needs to be duplicated to drive a second crate.

A further board may be required for testing the readout boards during the prototype and production phases. This test board will send and receive the signals to and from a single readout board using the same cables as the VFE-PCBs.

3 Cost

We assume that we will build 2 prototypes of the readout boards and for production, we need 15 readout boards plus 5 spares. The trigger board will need at most 1 prototype board and, for production, 2 boards plus 1 spare. The test board will be produced during prototyping and no production of this is needed.

In addition to the purpose built boards, the system also needs commercially available infrastructure, namely, a PCI/VME interface card, a VME extender, a high-end PC, some disk storage and VME crates and power supplies.

All the following prices include VAT. A VME-PCI8026 PCI/VME interface card set, including a 2m cable, is quoted by National Instruments at £3889. A VXI-MXI-2 extender board, including cable, is quoted at the same location at £2755. Note, we may use an SBS VME-PCI fibre channel, Model 618, as this can have the PC outside the radiation area; the cost is assumed to be similar. A dual Pentium-IV, 2 GHz, 2 Gbytes memory PC, with screen and keyboard, is quoted by Compusys at £3680. For disk, a 1.4 Tbytes array spread over 12 IDE disks with RAID 5 redundancy and a SCSI interface, recently bought by the UCL group, was £8k. CERN-specification, Wes V429, 6U VME crates, including power supplies, are quoted at £4700.

Therefore, an estimated costing of the readout electronics is:

- Non-recurring design costs; for all electronics = £2k.
- Readout boards; £2700 per board × 22 boards = £59k.

- Trigger board; £1200 per board × 4 boards = £5k.
- Test board; £2900 per board = £3k.
- Cables (guesstimated); £30 per cable × 100 cables = £3k.
- PC and disk; £4k for the PC, £8k for 1.4 Tbytes of disk = £12k.
- VME interfaces; £4k for PCI-VME interface, £3k for VME extender = £7k.
- 6U VME crate and power supplies; £5k per crate × 2 crates = £10k.

All values given are in FY02/03 prices and include VAT, so the total cost of the equipment for the project is therefore FY02/03 £101k.

4 Schedule

Task	Date of completion
Readout electronics CDR	October 2002
Prototype readout board design completed	January 2003
Readout board PDR	February 2003
Prototype readout board layout and fabrication completed	March 2003
Test board design completed	April 2003
Prototype trigger board design completed	April 2003
Trigger board PDR	May 2003
Test board layout and fabrication completed	June 2003
Prototype trigger board layout and fabrication completed	June 2003
Prototype readout board and prototype VFE-PCB tests	July 2003
Prototype readout board testing completed	September 2003
Prototype trigger board testing completed	October 2003
Production readout board redesign completed	October 2003
Readout board FDR	November 2003
Production trigger board redesign completed	November 2003
Production readout board layout and fabrication completed	December 2003
Trigger board FDR	December 2003
Production trigger board layout and fabrication completed	January 2004
Production readout board testing completed	March 2004
Production trigger board testing completed	March 2004

Table 1: Schedule for the readout electronics.

Table 1 shows the schedule for the readout electronics. The system needs to be ready for a beam test in April 2004. It therefore needs to be completed by the end of March 2004. Fabrication, testing and data acquisition software development of the full system is likely to require around 6 months, which sets the end of the readout board prototype phase to be September 2003. Therefore, the time to January 2003 will be used to complete the specification and design of the readout boards. Full specification prototype fabrication of these will take place by March 2003 and prototype testing will take place over summer 2003.

Hence, prototype costs will be incurred in FY02/03, while production costs will be incurred in FY03/04. The prototype costs will be for some of the infrastructure (PC, the PCI-VME interface, one VME crate and a few cables), and two readout boards, giving a total of £20k in

FY02/03. The remaining infrastructure and board production costs, totalling FY02/03 £81k, will all be incurred in FY03/04.

5 Effort

The readout board is estimated to require around 18 months of engineering effort in total. We estimate that 6 months of engineering effort will be required for the design of the trigger board. Another 6 months is estimated for the incremental engineering to design the test board, given the readout board design. In addition, 1 month will be needed for layout and fabrication of each stage of each board; the prototype readout board, the production readout board, the prototype trigger board, the production trigger board and the test board, giving 5 months for these tasks. This is a total of 35 months.

There is a total of 18 months engineering effort available within the Universities over FY02/03 and FY03/04; 3 months from Manchester (Dave Mercer), 10 months from Imperial (Dave Price and Osman Zorba) and 5 months from UCL (Martin Postranecky and Matt Warren). Currently, Manchester are working on the readout board master FPGA, Imperial on the readout board slave FPGA and UCL on the trigger and test boards. Hence, 13 of the estimated 18 months for the readout board and 5 of the estimated 12 months for the test and trigger boards are covered at present. None of the expertise for layout or fabrication exists in the University groups.

Assuming the project is approved in December 2002, then effort from RAL ID would be required to complete the system. With effort starting in January 2003, then there is 3 months in FY02/03 and 12 months in FY03/04 available, i.e. 15 months in total. A single engineer to work on the board designs would need to contribute the missing 12 months of effort over this time, i.e. be working on the project at 0.8 FTE. Of this 1SY total, 0.2SY will be needed in FY02/03 and the remaining 0.8SY in FY03/04. It is clear that this engineer would need to cover all aspects of the project as all are short of effort at present and, depending on experience, the engineer might become project leader. Some rearrangement of tasks between groups might also be useful at this stage.

Additional technical effort of 5 months from the RAL drawing office for the layout and fabrication would also be needed. The readout prototype board will need 1 month of this is FY02/03, with the rest in FY03/04.

Test software for the boards will mainly be provided by the University groups.