CALICE ECAL Readout Electronics: VFE-PCB Interface Specification

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1 Introduction

The prototype calorimeter will consist of 30 layers of silicon diodes. Each layer comprises a 3×3 array of silicon diode wafers, each containing a 6×6 array of diodes. Each diode needs to be read out and so corresponds to a channel. Hence, each wafer contains 36 channels, each layer contains $36 \times 9 = 324$ channels and the whole prototype is $324 \times 30 = 9720$ channels.

Three wafers are mounted onto one very-front-end card (VFE-PCB). This contains six VFE FLC_PHY1 chips, each reading 18 channels. The channels are multiplexed onto a single output line per VFE chip. The VFE chip will also accept a calibration signal which is used to inject a pulse at the chip input. There are 90 VFE-PCB's in total.

The interface to the readout elecronics is the connector on the VFE-PCB which supplies the driving signals for the VFE-PCB and takes the output signals. The power for the VFE-PCB is supplied separately.

2 Signals

The readout electronics is assumed to have an independent ground from the VFE-PCB's. Hence, all signals on the PCB connector which provide the interface to the readout electronics are differential. Table 1 lists the signals to and from the VFE-PCB.

Signal	I/O	Type	Specification	Number	Pins	Notes
Sample-and-hold	In	Digital	LVDS	1	2	1
Shift register reset	In	Digital	LVDS	1	2	1
Shift register input	In	Digital	LVDS	1	2	1
Shift register multiplex clock	In	Digital	LVDS	1	2	1
Shift register output	Out	Digital	LVDS	2	4	1,2
Channel signal output	Out	Analogue	Differential $+2 \pm 1$V	6	12	3,4,5
Calibration timing strobe	In	Digital	LVDS	6	12	1,6
Calibration signal level	In	Analogue	Differential	1	2	7,8
Total				19	38	

Table 1: Signals to ("In") and from ("Out") the VFE-PCB.

Notes:

1. There is a problem with matching the "LVDS" signals above. Standard LVDS has a 1.2V quiescent level. However, the VFE-PCB will run from 0V to -5V, rather than $+5$V to

0V, so that this level will be -3.8V. If the grounds can be completely separated and the two systems floated, then the readout electronics could run standard LVDS. However, this could be difficult to achieve and this remains an outstanding issue to be resolved.

2. Each of the two shift register output signals are the AND of those from three of the VFE chips on the VFE-PCB.

3. The range of the channel signal output depends on the termination. The VFE-PCB has a 2 ± 2V differential driver output with 50Ω back termination. The above ± 1V range therefore assumes 50Ω termination within the readout electronics. However, as the cables will probably not be more than 2m, termination should not be critical and an open circuit in the readout electronics, giving a ± 2V swing, would be possible.

4. The six channel signal outputs each correspond to the output of one VFE ship.

5. The channel signal output must be digitised with a 10 bit signal range, but with 4 bits precision at the low end, rising to 10 bits precision at the high end. Hence, 14 bits dynamic range, 10 bits precision is needed.

6. The six calibration timing strobes select which group of channels to calibrate. The 18 channels per VFE chip are divided into six groups of three channels each. These can be calibrated in any combination.

7. The quiescent level and range of the differential calibration signal level has not yet been decided.

8. The calibration signal level dynamic range and precision must be at least at good as that for the channel signal output.

3 Timing

The time-dependent signals are shown in Fig. 1; the calibration signal level is constant during data capture and transfer.
Notes:

1. The calibration timing strobes are only present if calibrating. They must all have the same rising edge, if selected.

2. The timing between the start of the sequence (given by the rising edge of the trigger input) or, if calibrating, the rising edge of the calibration timing strobes, to the sample-and-hold must be accurately adjustable to ≤ 10ns.

3. The shift register input must overlap with the first shift register clock. It should go down before the first ADC channel is sampled.

4. The shift register clock speed must be ≤ 5MHz.

4 Connectors and cables

The physical thickness of the VFE-PCB and connector cannot exceed 4.5mm due to space contraints. The proposed connector is JST SHL 20-pin 1mm pitch, where two are required per VFE-PCB. The reference numbers are: contact SSHL-003T-PO.2, housing SHLP-20V-S-B, shrouded header SM20B-SHLS-TF. The detailed signal-to-pin ordering is not yet decided.

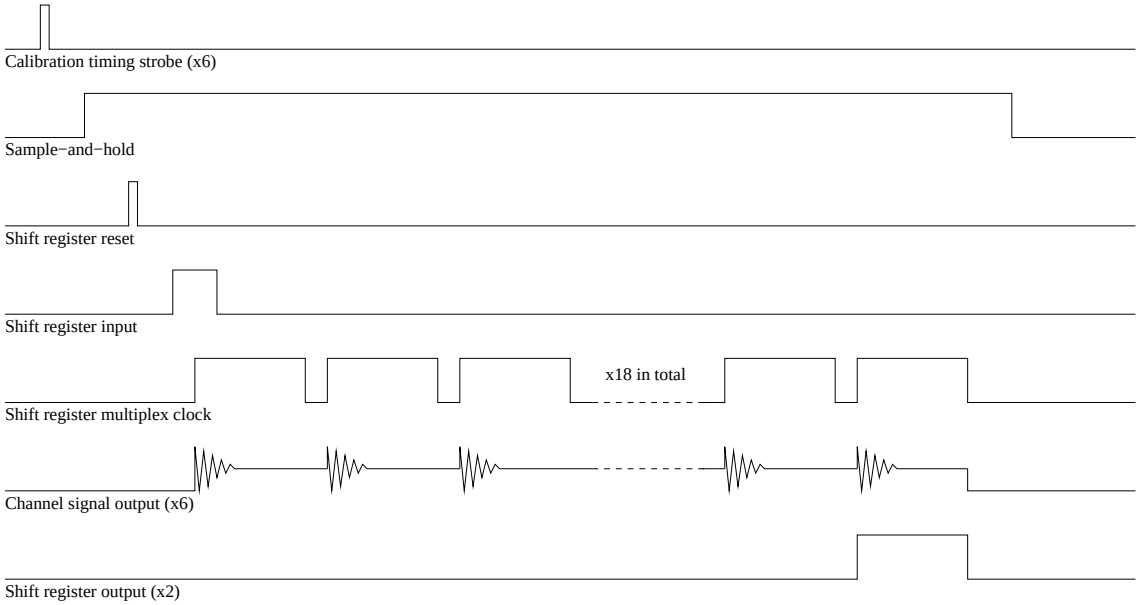

Figure 1: Time-dependent signals to and from the VFE-PCB.

These connectors have several potential drawbacks; they may require soldering of all 38 pins at both ends of the 90 cables, they require two connectors of 20 pins each per VFE-PCB and they do not allow two-deep mounting at the readout electronics end and so may not fit into the available space. The default would be to use the same connector set at the readout electronics end. However, given the above issues, it might be better to use a CERN-standard IDC 40-pin connector at the readout electronics end, which can be mounted two-deep.

The cable should be twisted pair and around 2m long. There are no radiation-hard requirements but the cable should meet CERN specifications for safety. No cable with 1mm pitch has yet been proposed.