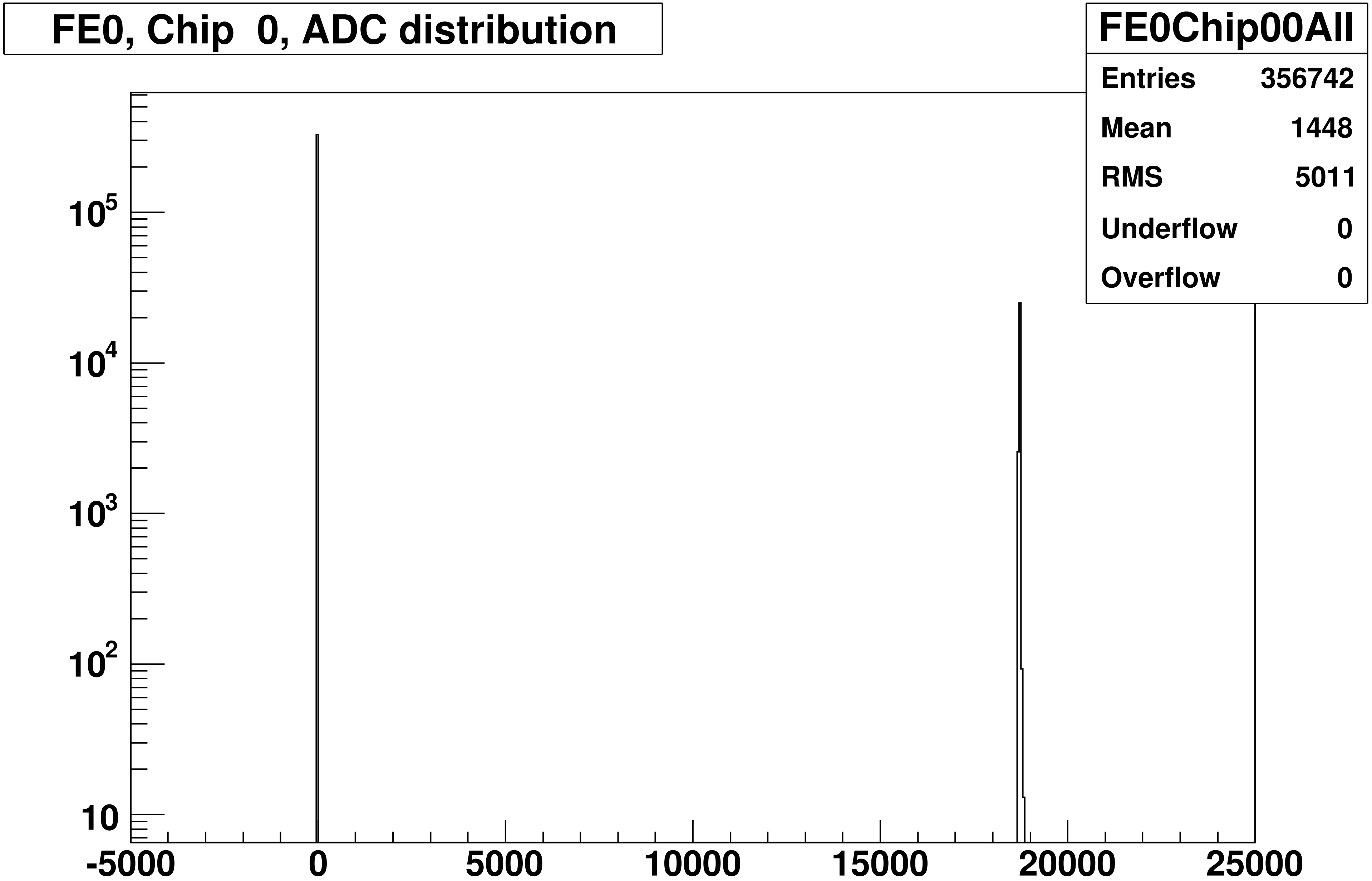

FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 356742
Mean 1448
RMS 5011
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
-5000
0
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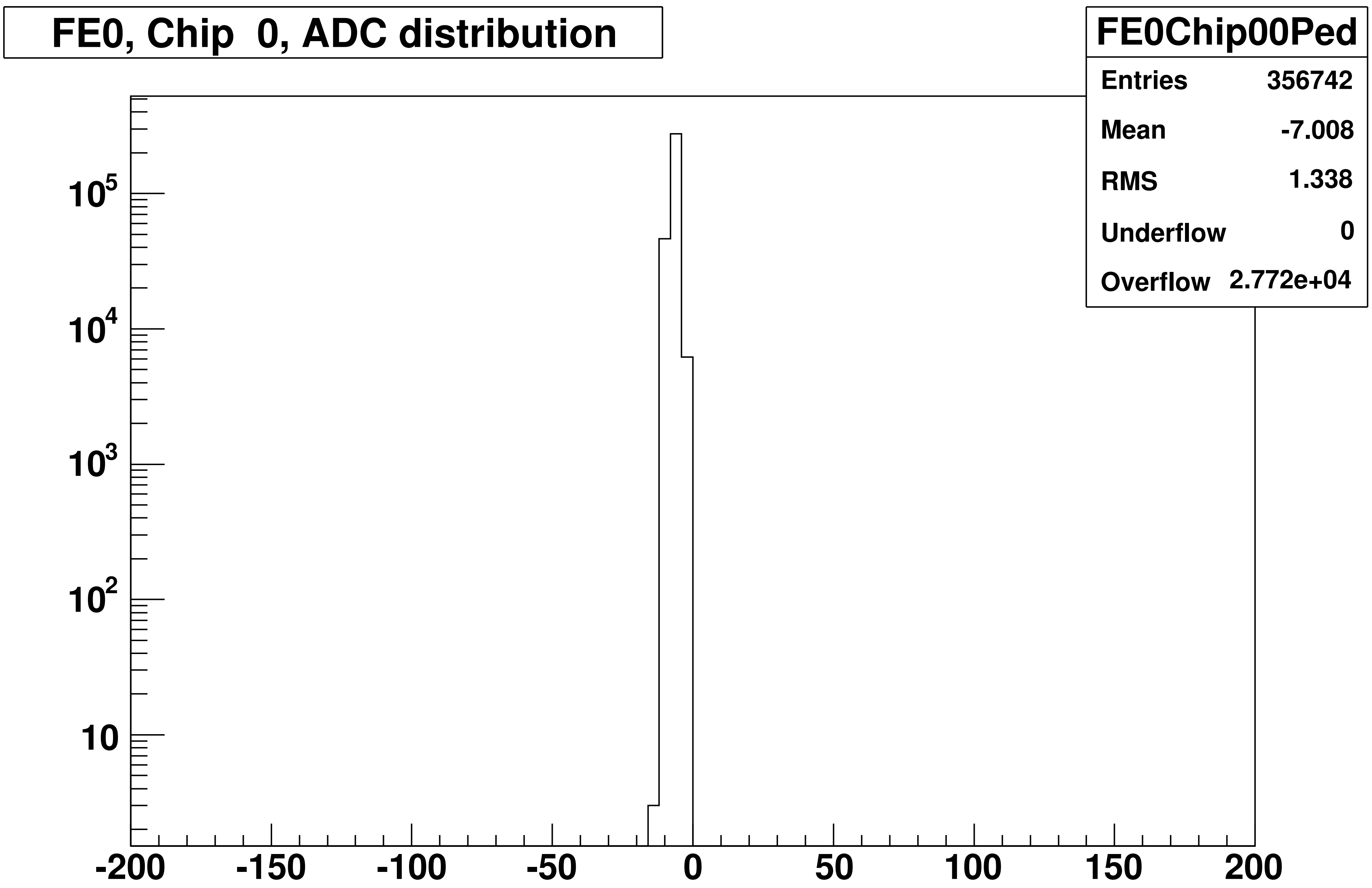
10000
15000
20000
25000



FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 356742
Mean -7.008
RMS 1.338
Underflow 0
Overflow 2.772e+04
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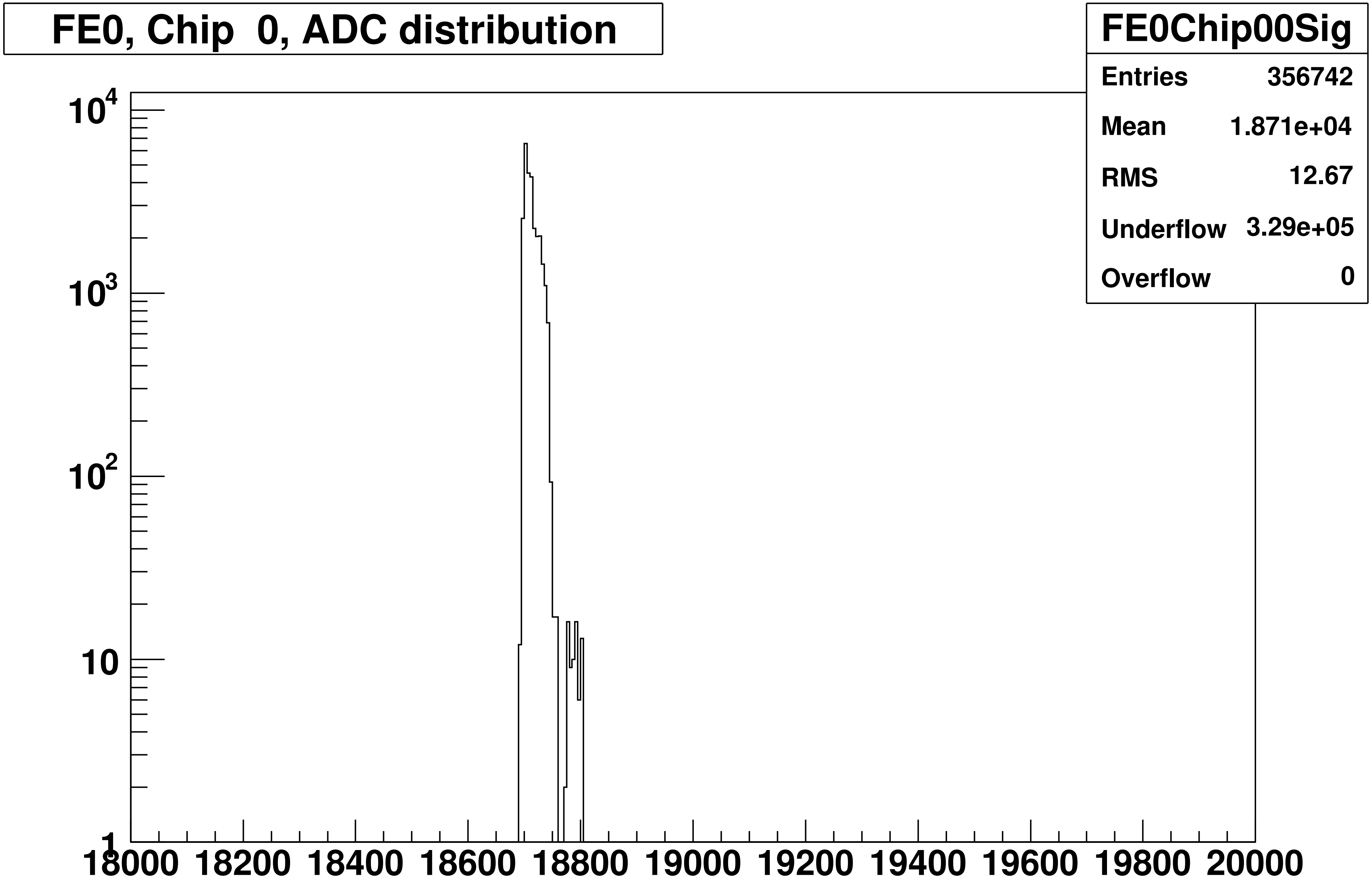
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 356742
Mean 1.871e+04
RMS 12.67
Underflow 3.29e+05
Overflow 0
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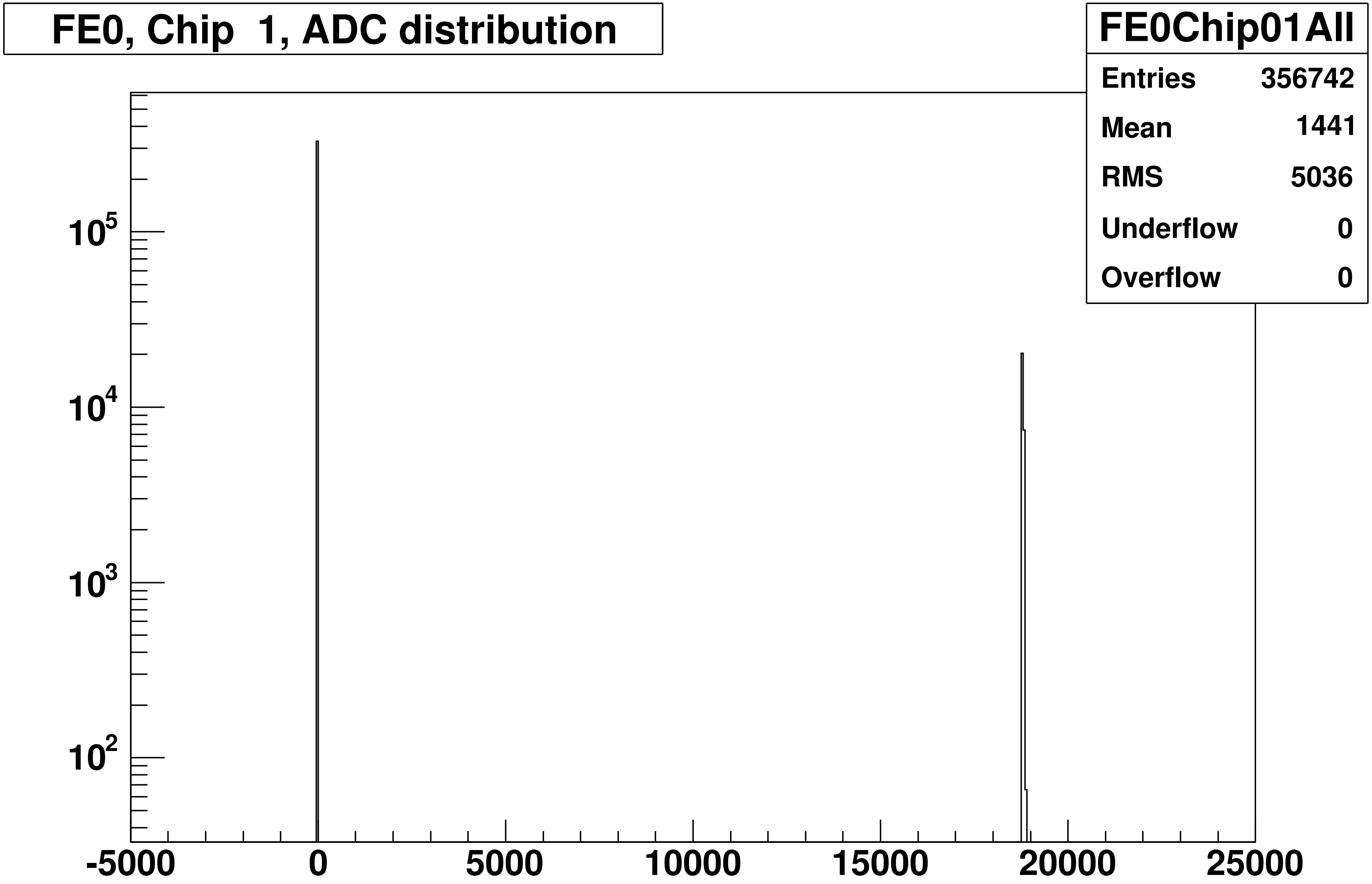
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 356742
Mean 1441
RMS 5036
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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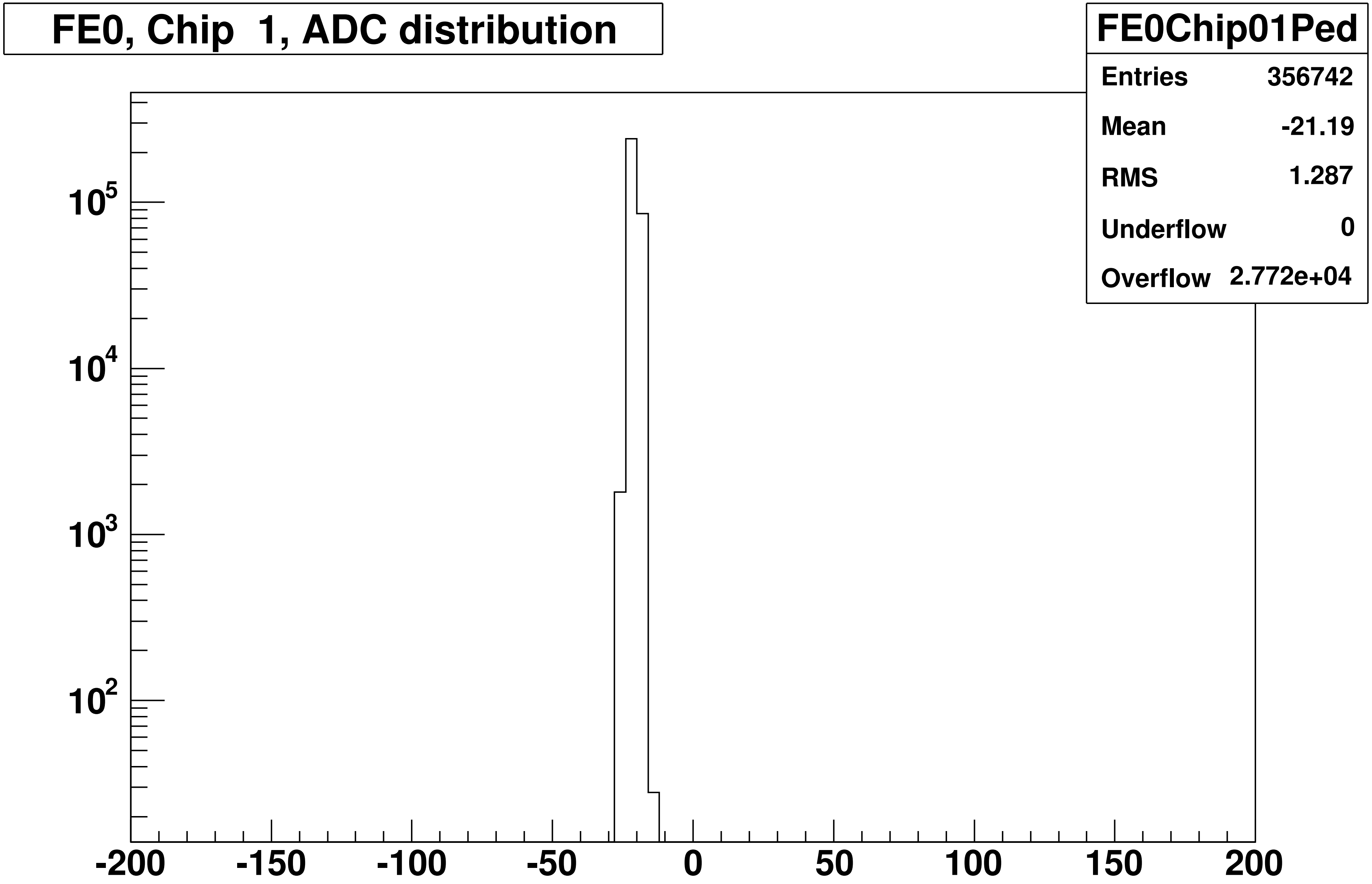
10000
15000
20000
25000


FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 356742
Mean -21.19
RMS 1.287
Underflow 0
Overflow 2.772e+04
10^5
10^4
10^3
10^2
-200
-150
-100
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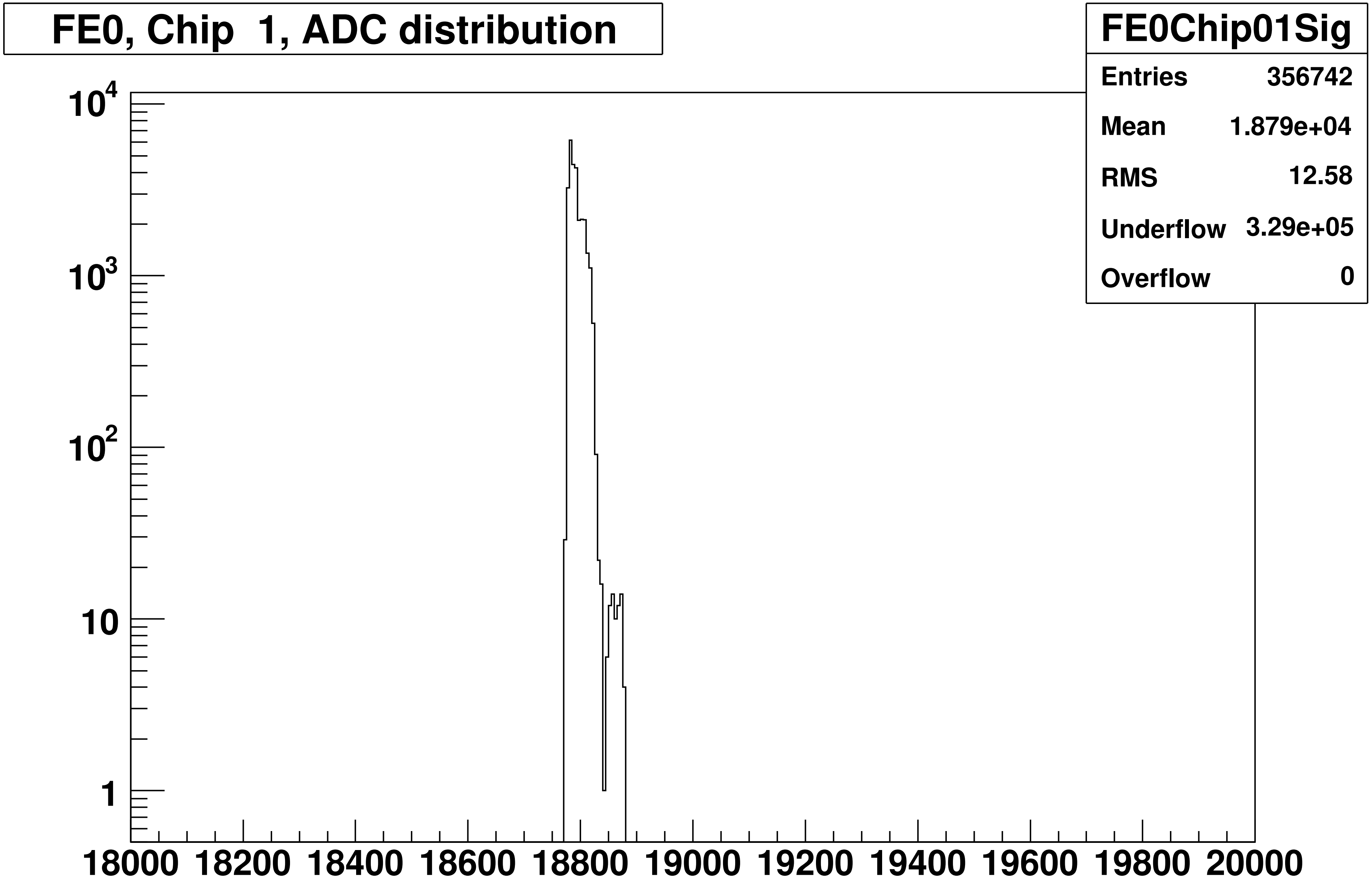
0
50
100
150
200


FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 356742
Mean 1.879e+04
RMS 12.58
Underflow 3.29e+05
Overflow 0
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10^3
10^2
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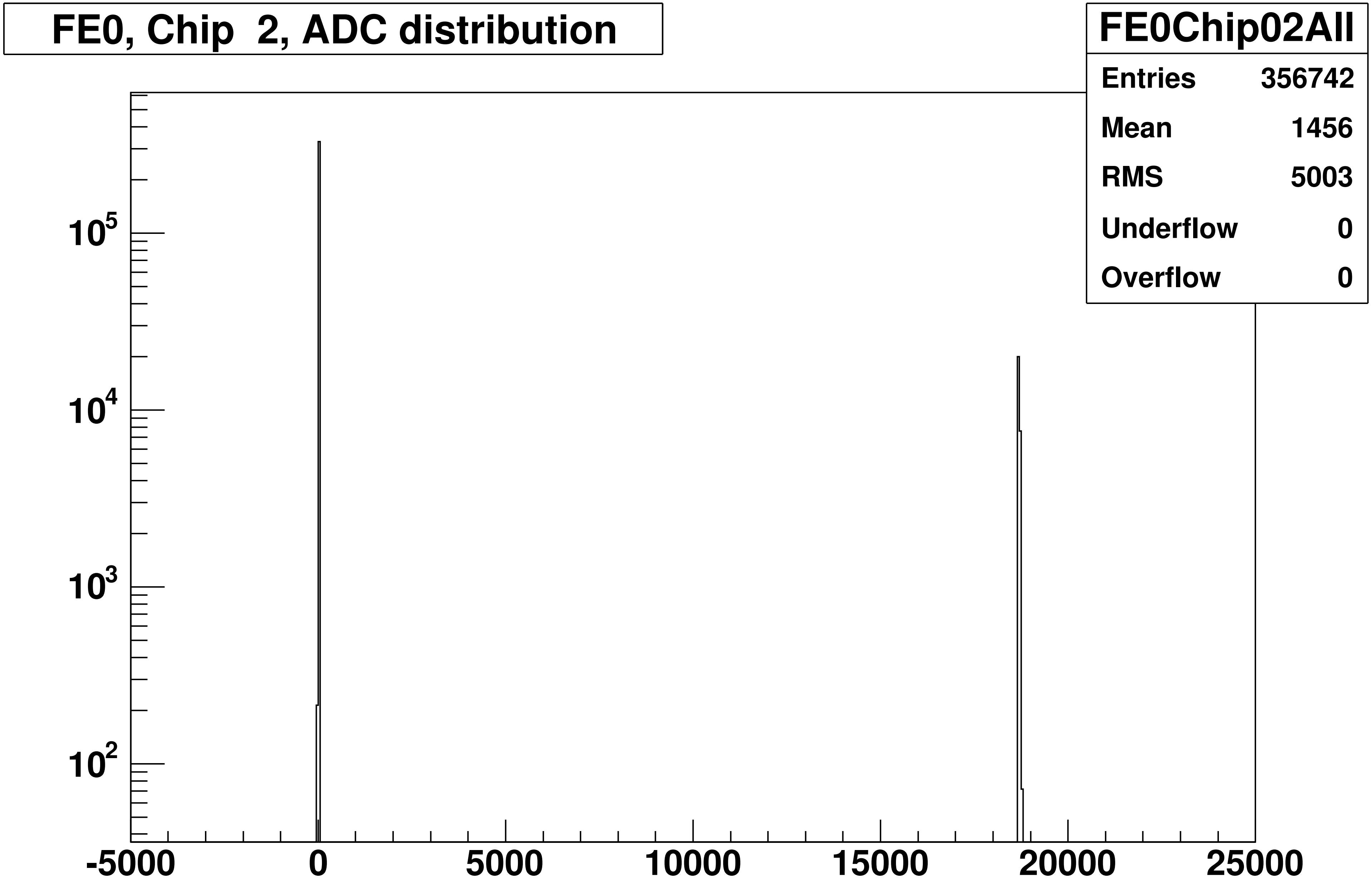
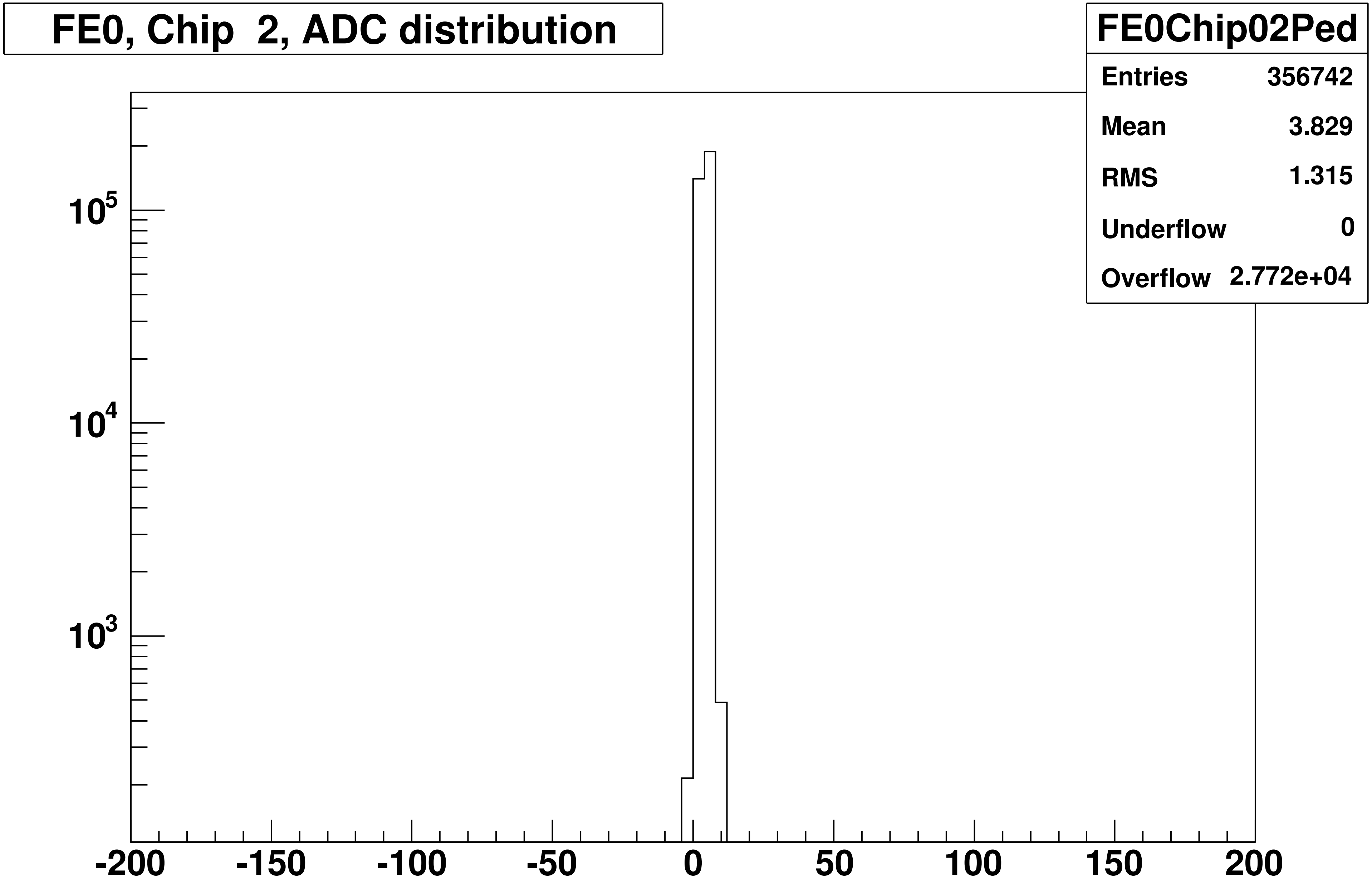
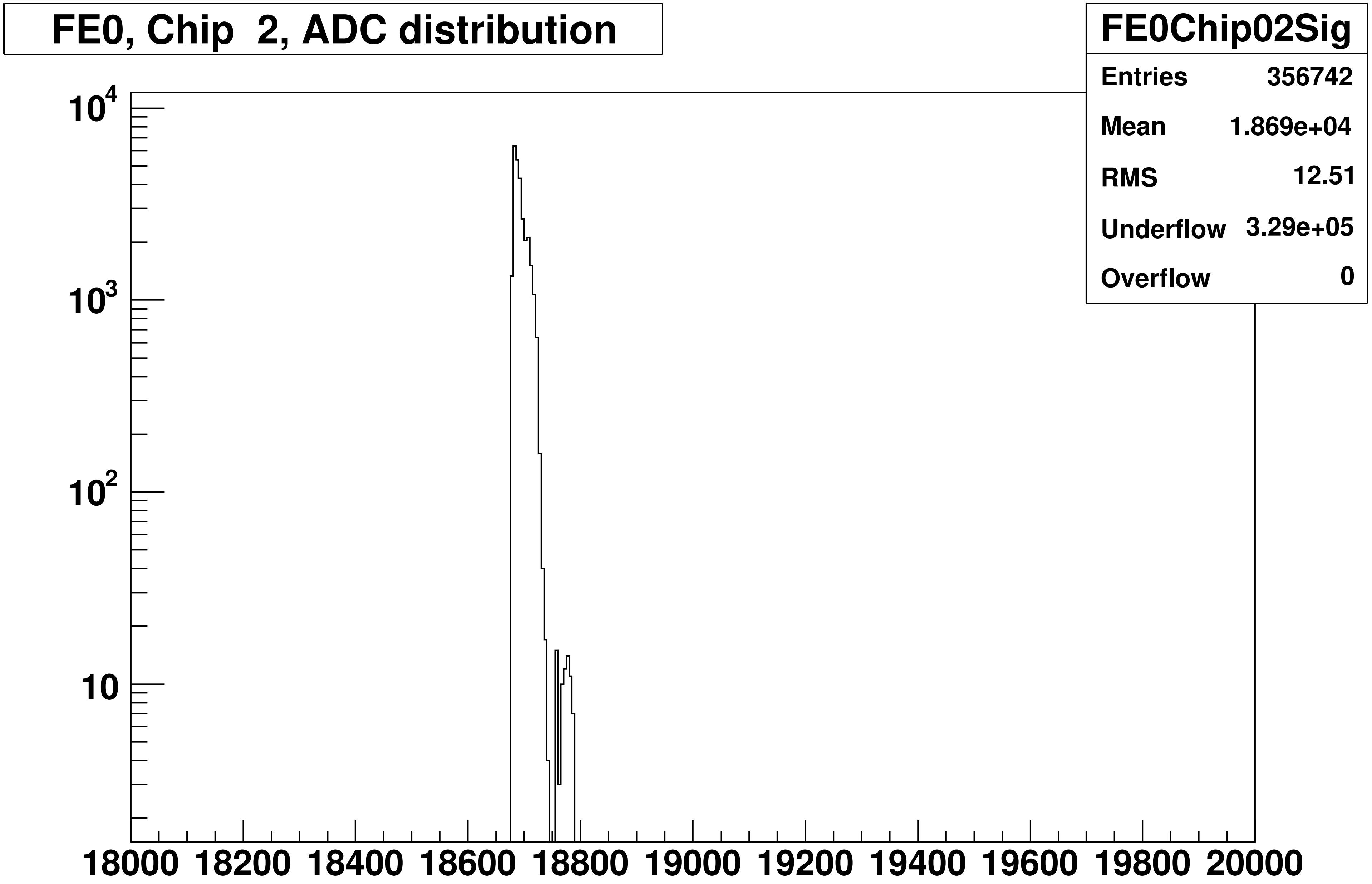
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 356742
Mean 1456
RMS 5003
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 356742
Mean 3.829
RMS 1.315
Underflow 0
Overflow 2.772e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 356742
Mean 1.869e+04
RMS 12.51
Underflow 3.29e+05
Overflow 0
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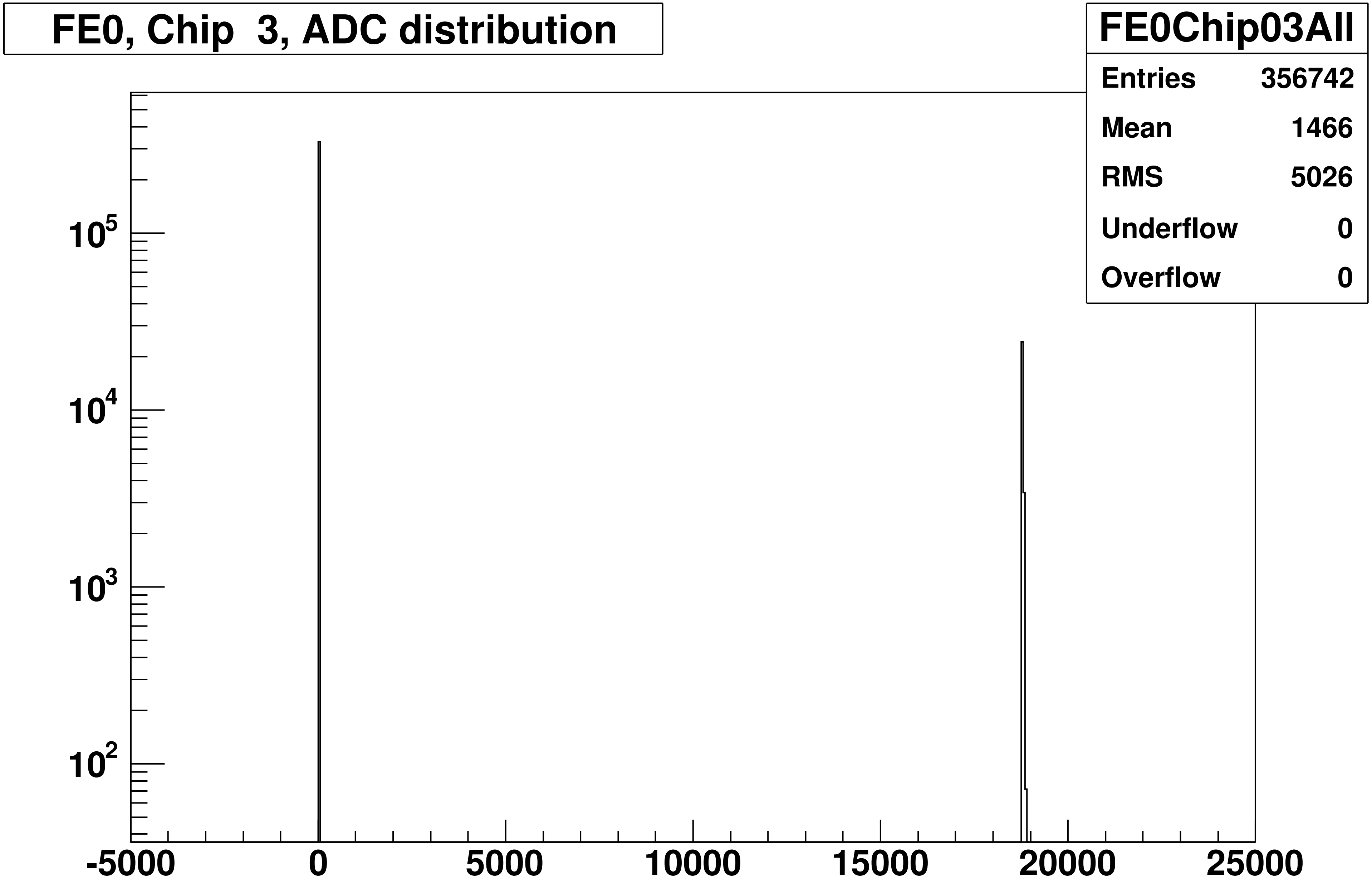
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 356742
Mean 1466
RMS 5026
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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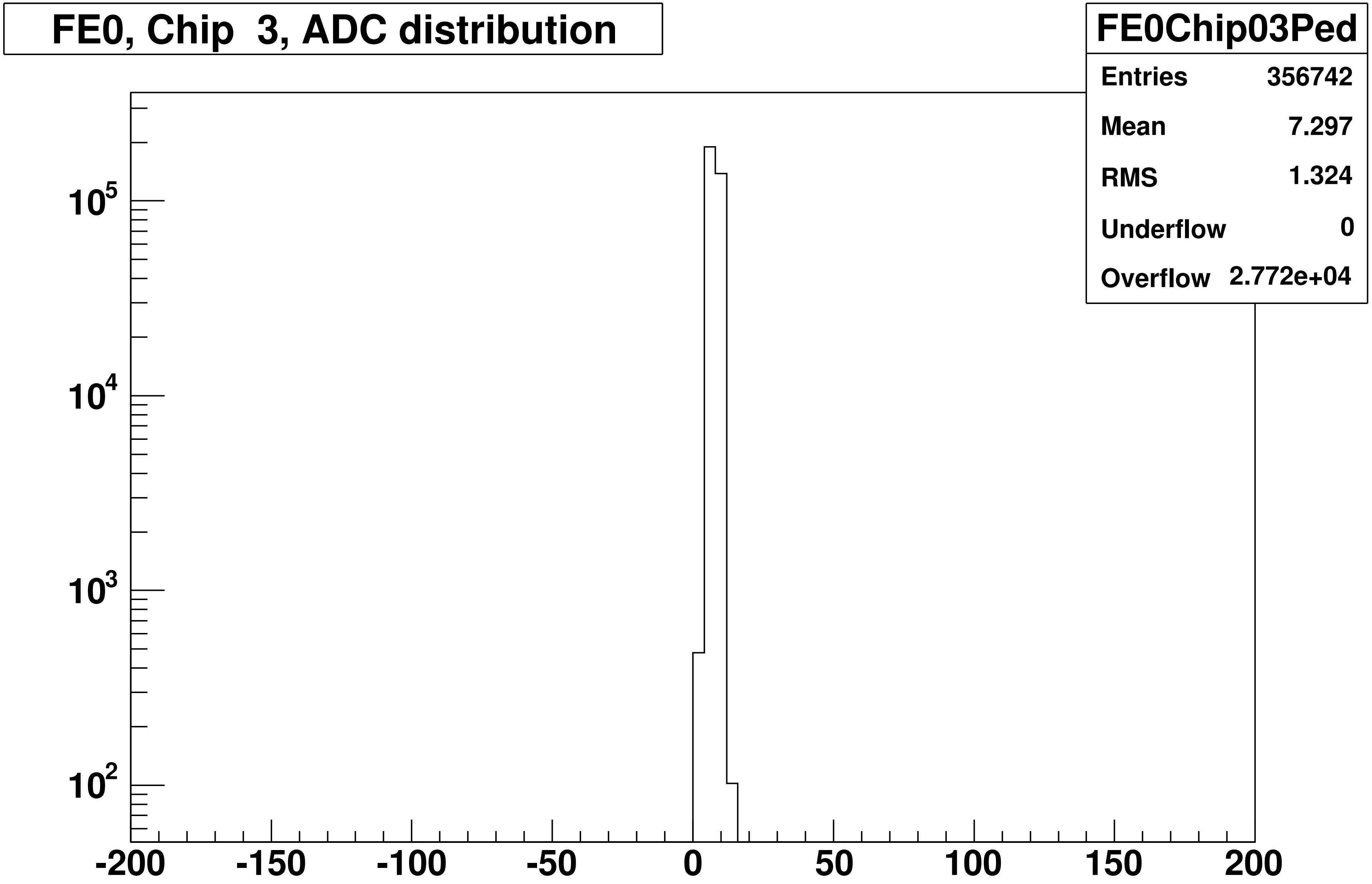
0
5000
10000
15000
20000
25000


FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 356742
Mean 7.297
RMS 1.324
Underflow 0
Overflow 2.772e+04
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10^4
10^3
10^2
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-100
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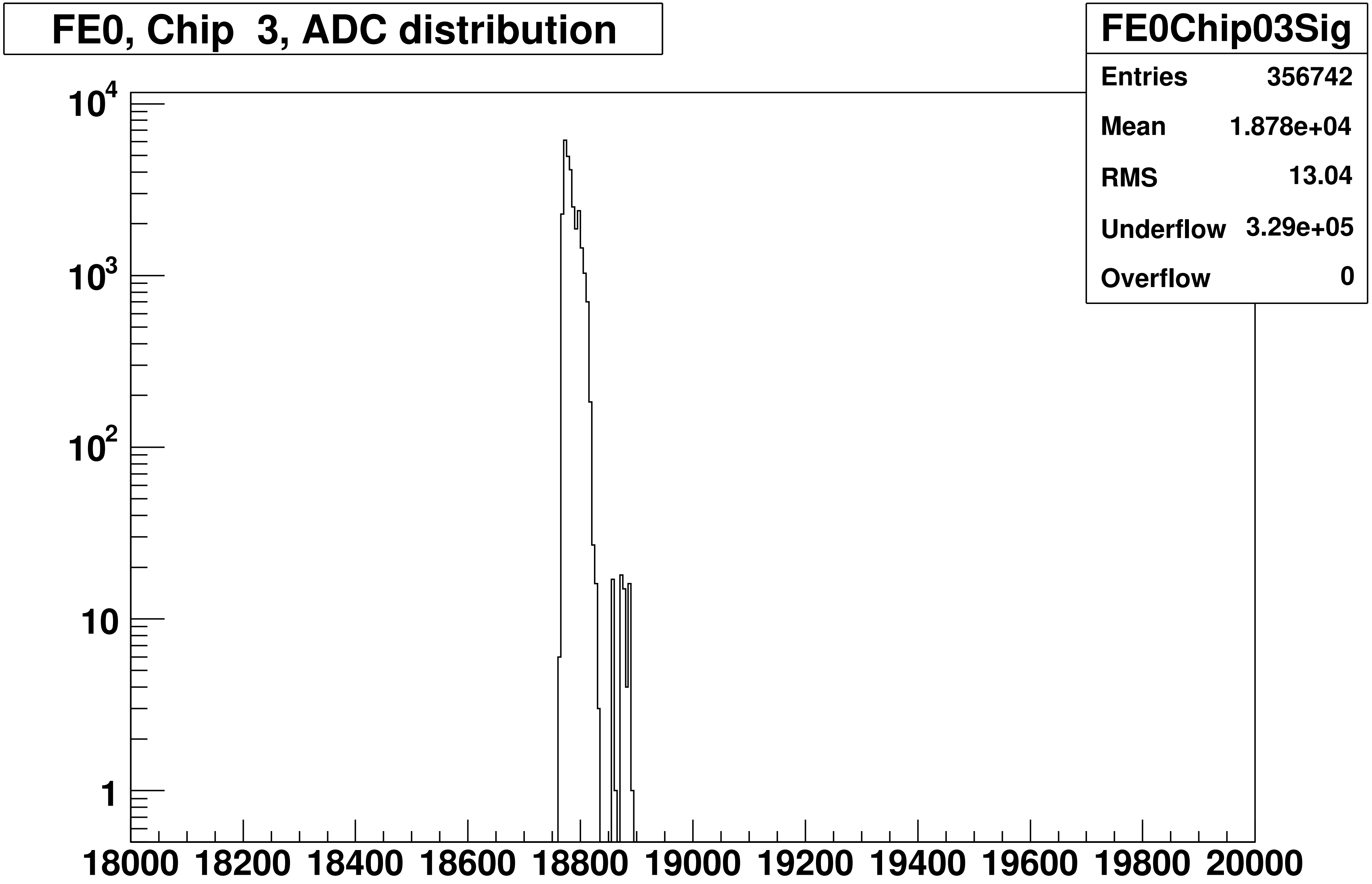
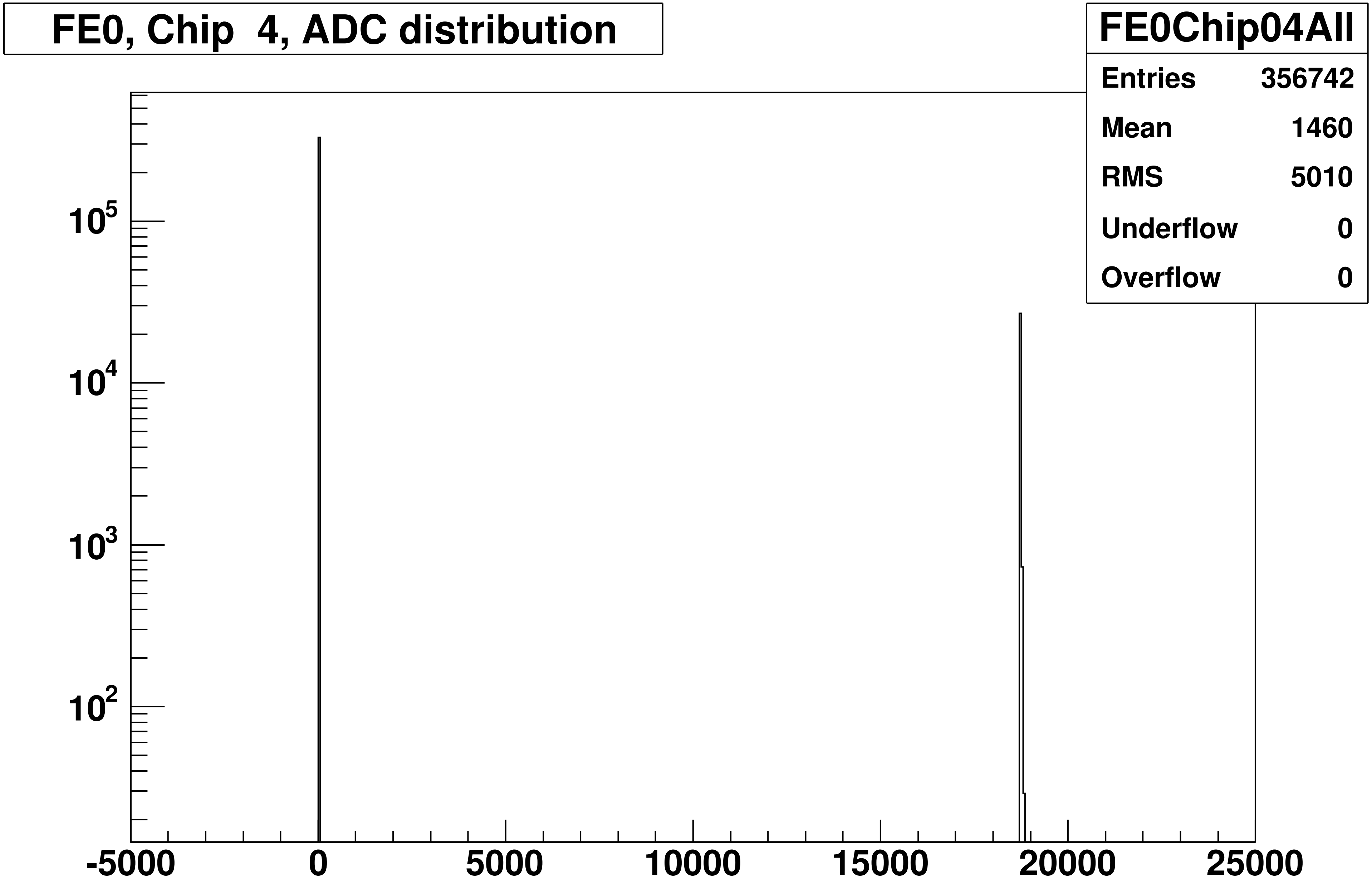
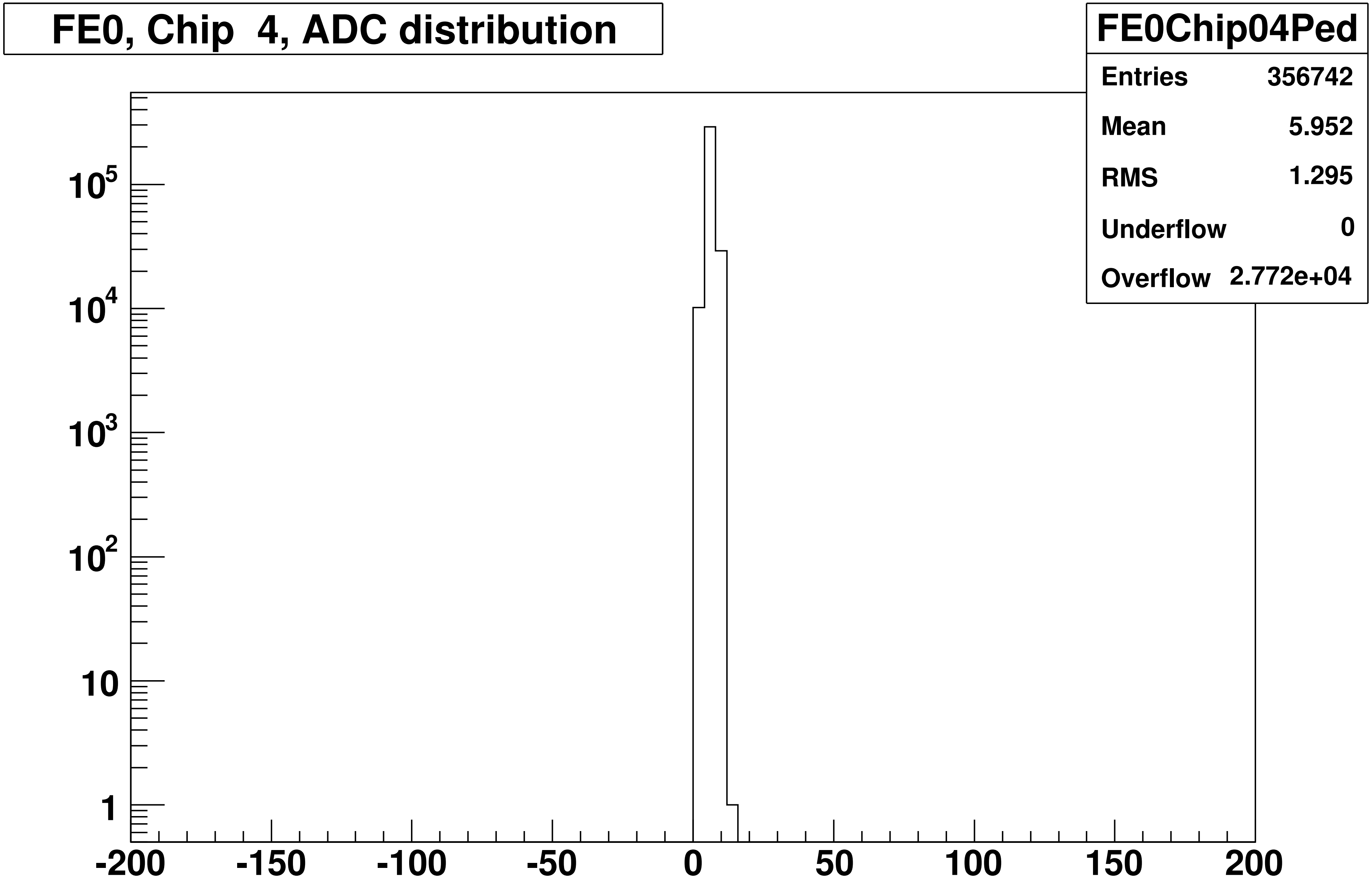
0
50
100
150
200



FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 356742
Mean 1.878e+04
RMS 13.04
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 356742
Mean 1460
RMS 5010
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 356742
Mean 5.952
RMS 1.295
Underflow 0
Overflow 2.772e+04
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10^4
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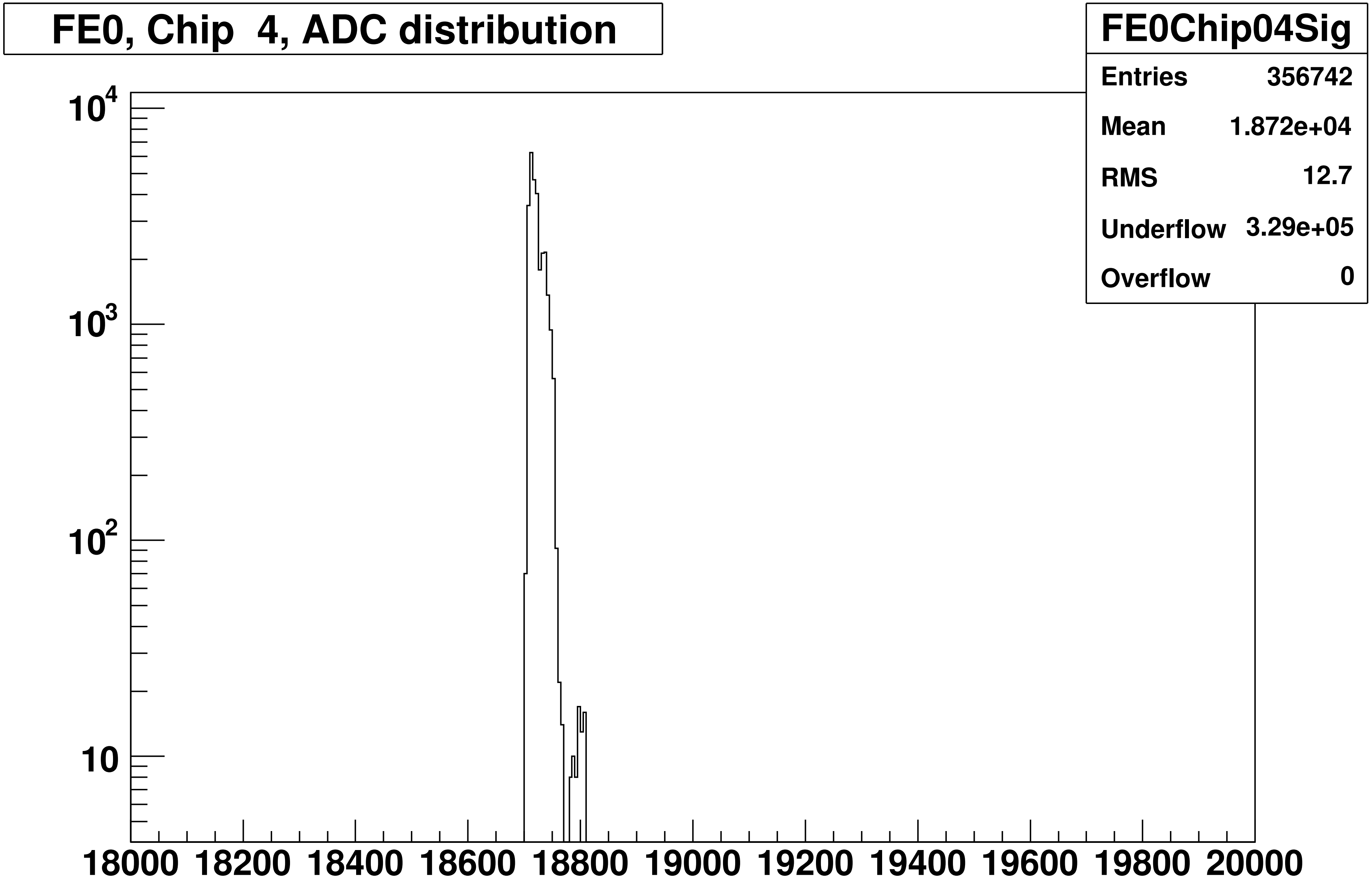
0
50
100
150
200


FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 356742
Mean 1.872e+04
RMS 12.7
Underflow 3.29e+05
Overflow 0
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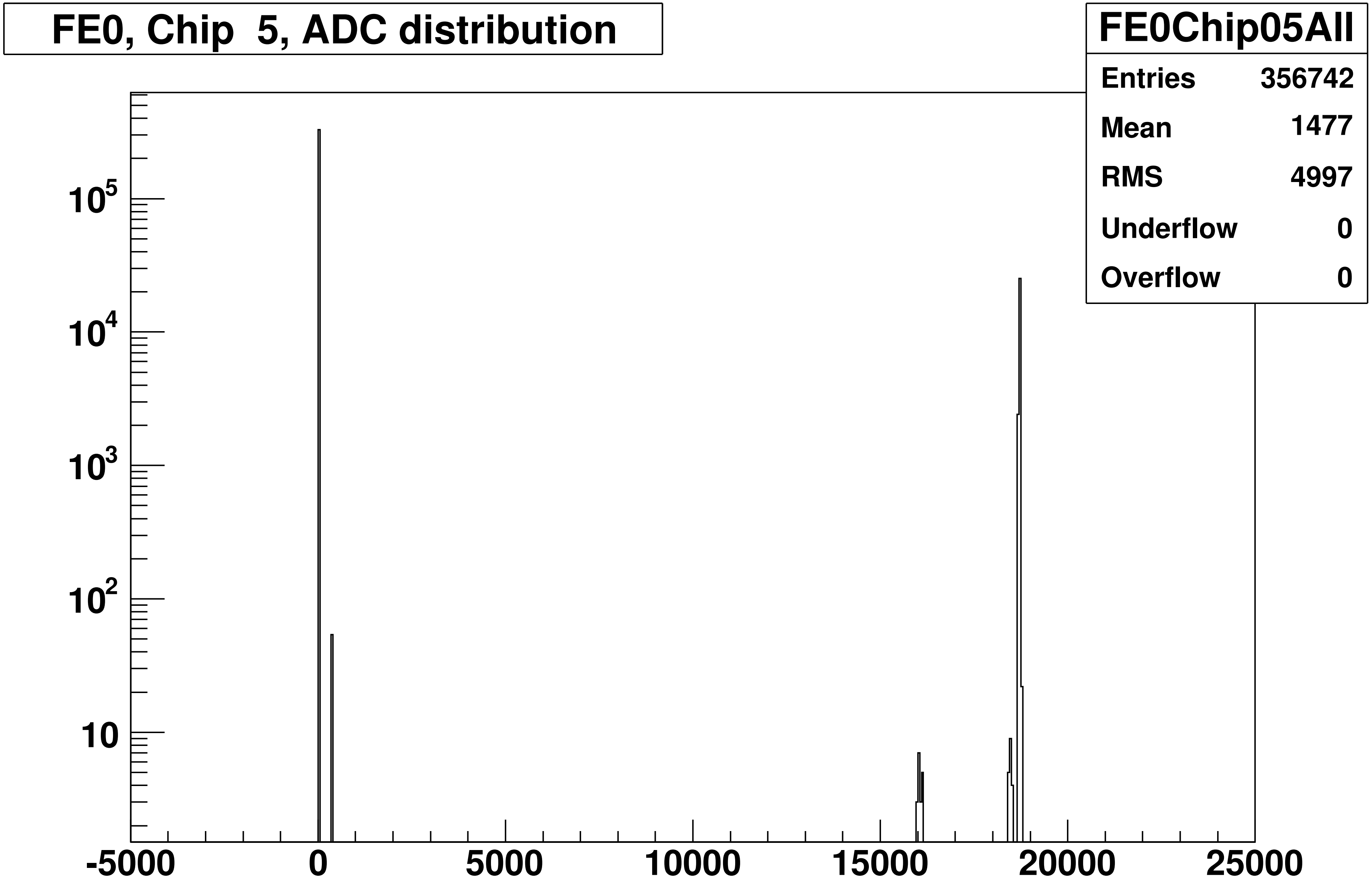
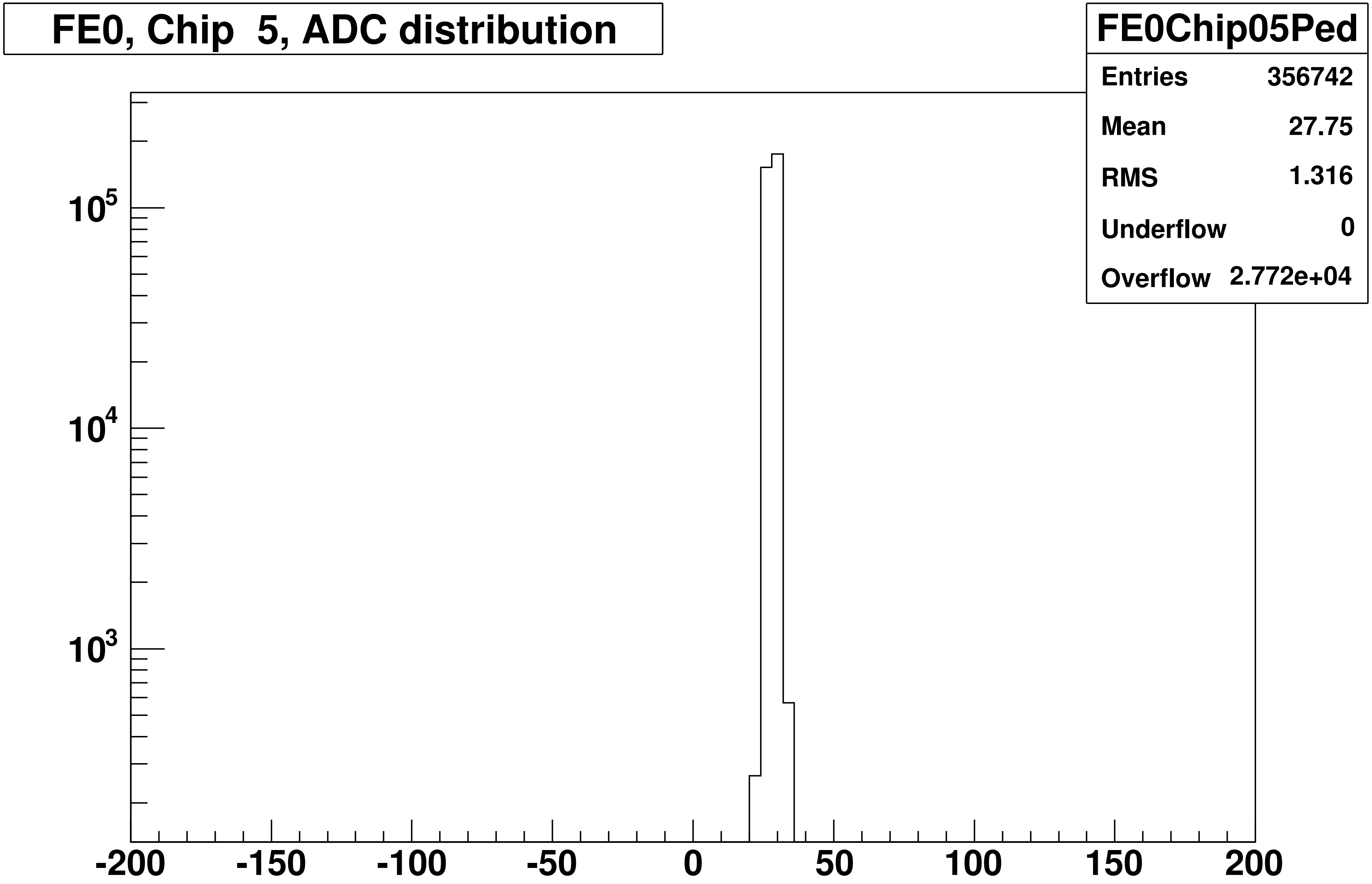
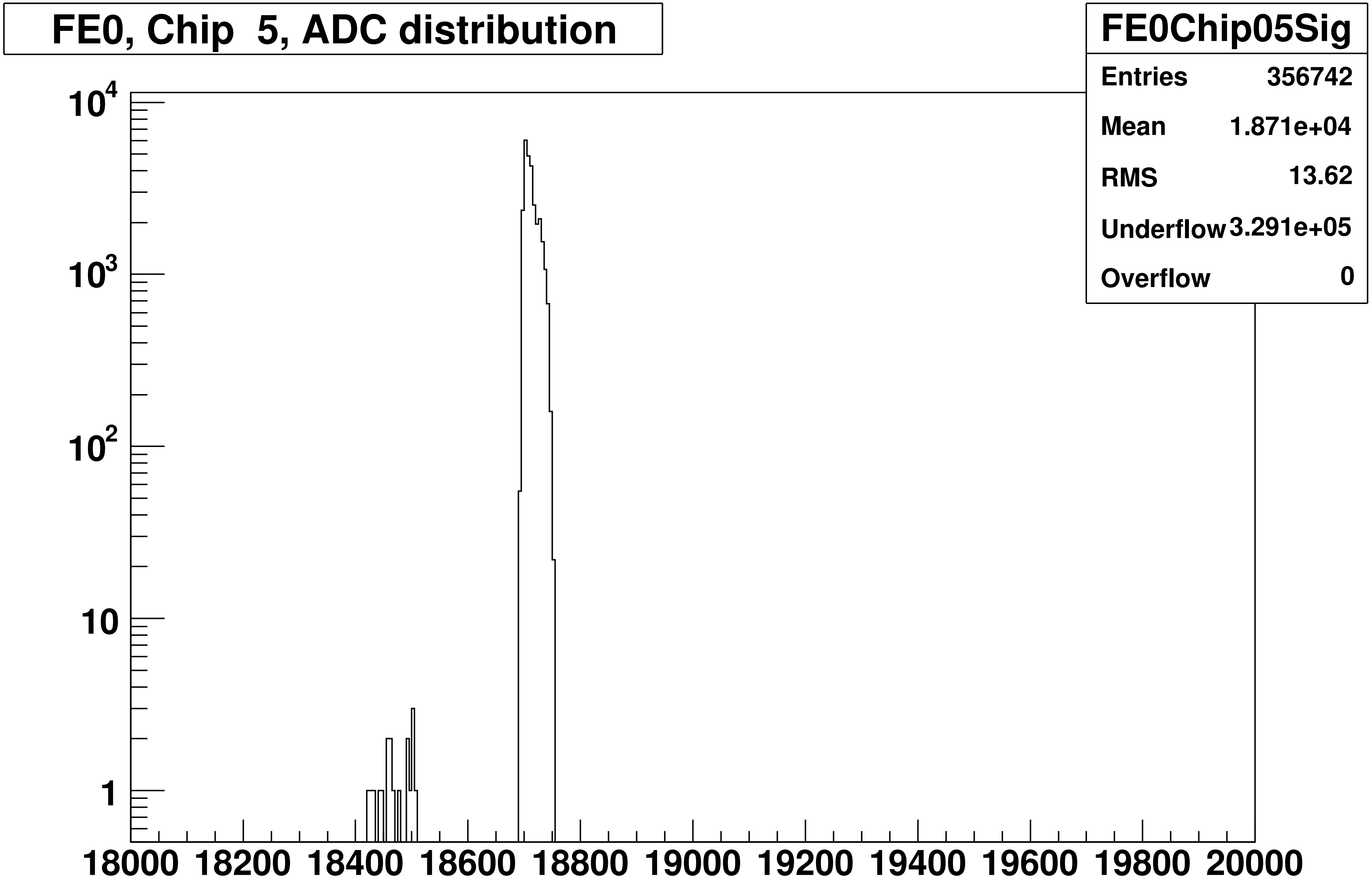
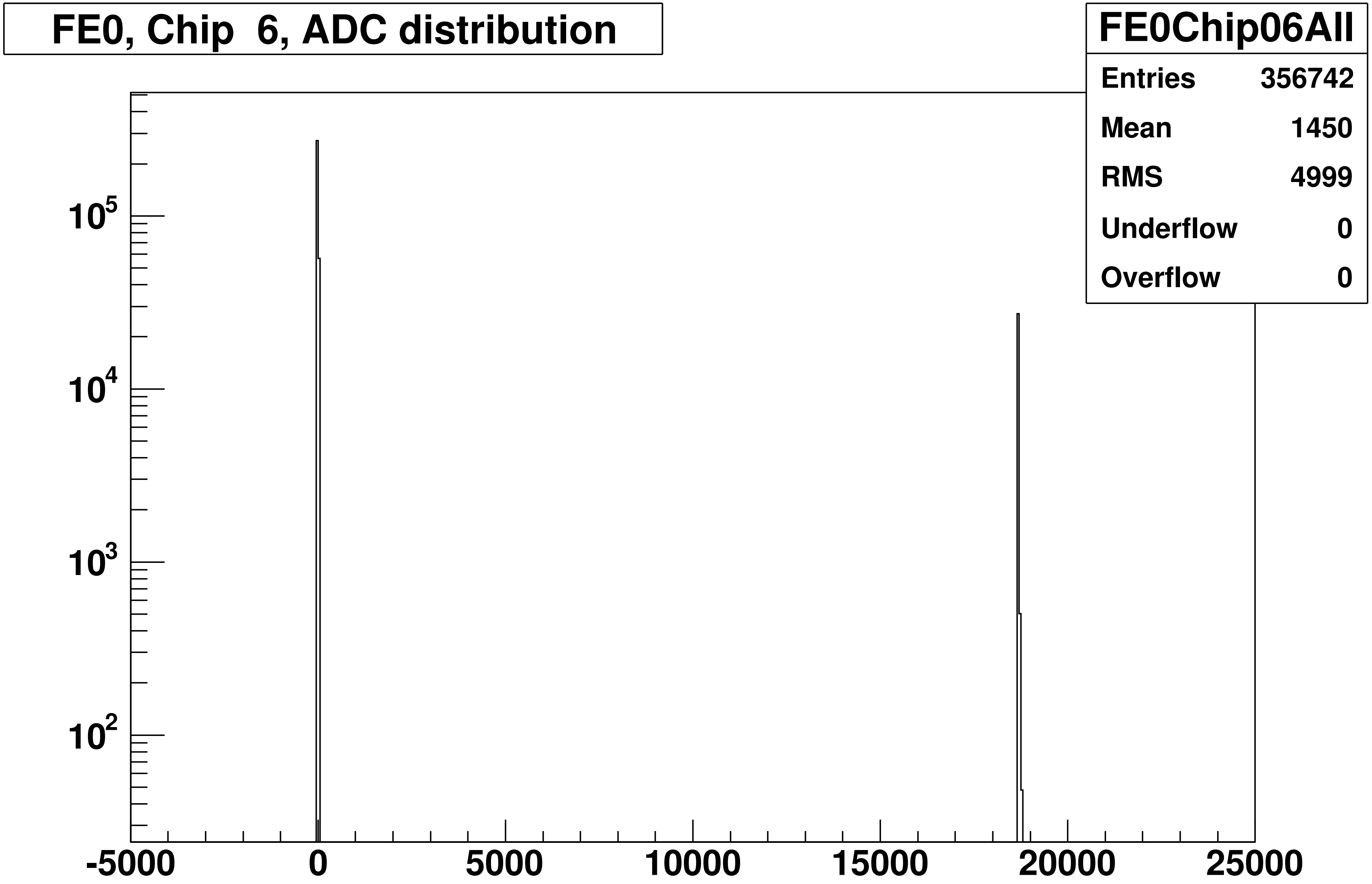
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

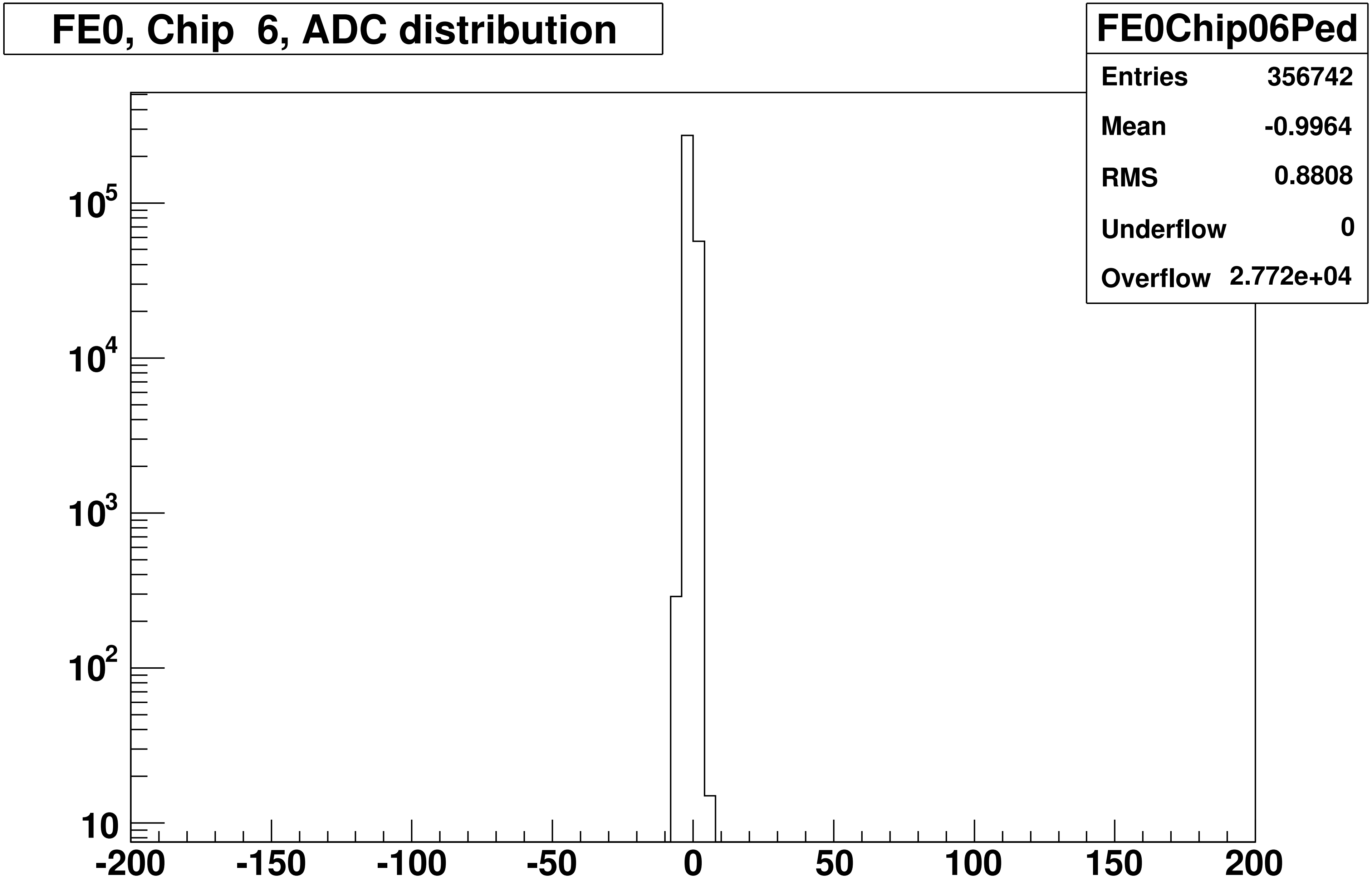

FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 356742
Mean 1477
RMS 4997
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 356742
Mean 27.75
RMS 1.316
Underflow 0
Overflow 2.772e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 356742
Mean 1.871e+04
RMS 13.62
Underflow 3.291e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 356742
Mean 1450
RMS 4999
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 356742
Mean -0.9964
RMS 0.8808
Underflow 0
Overflow 2.772e+04
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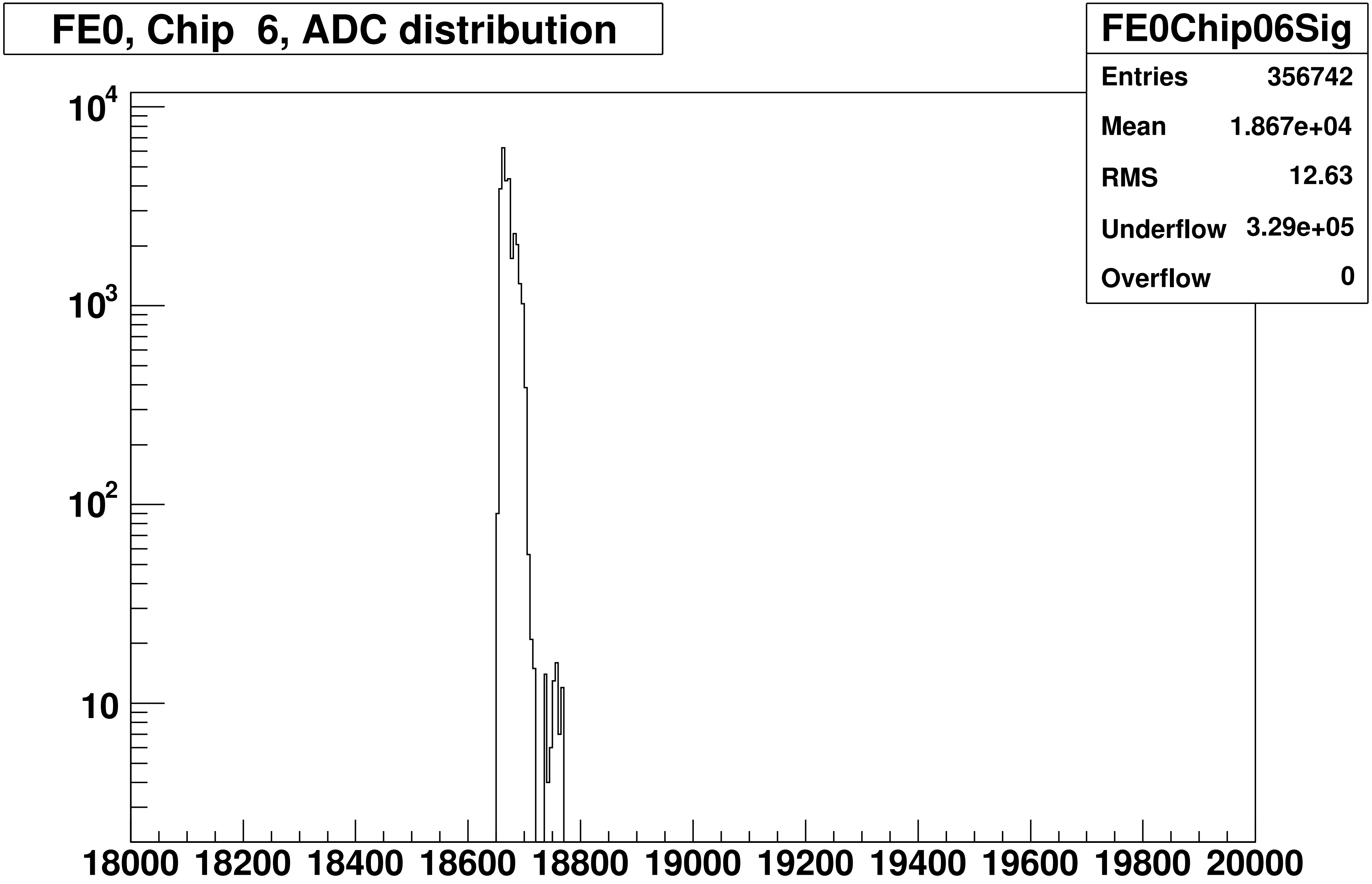
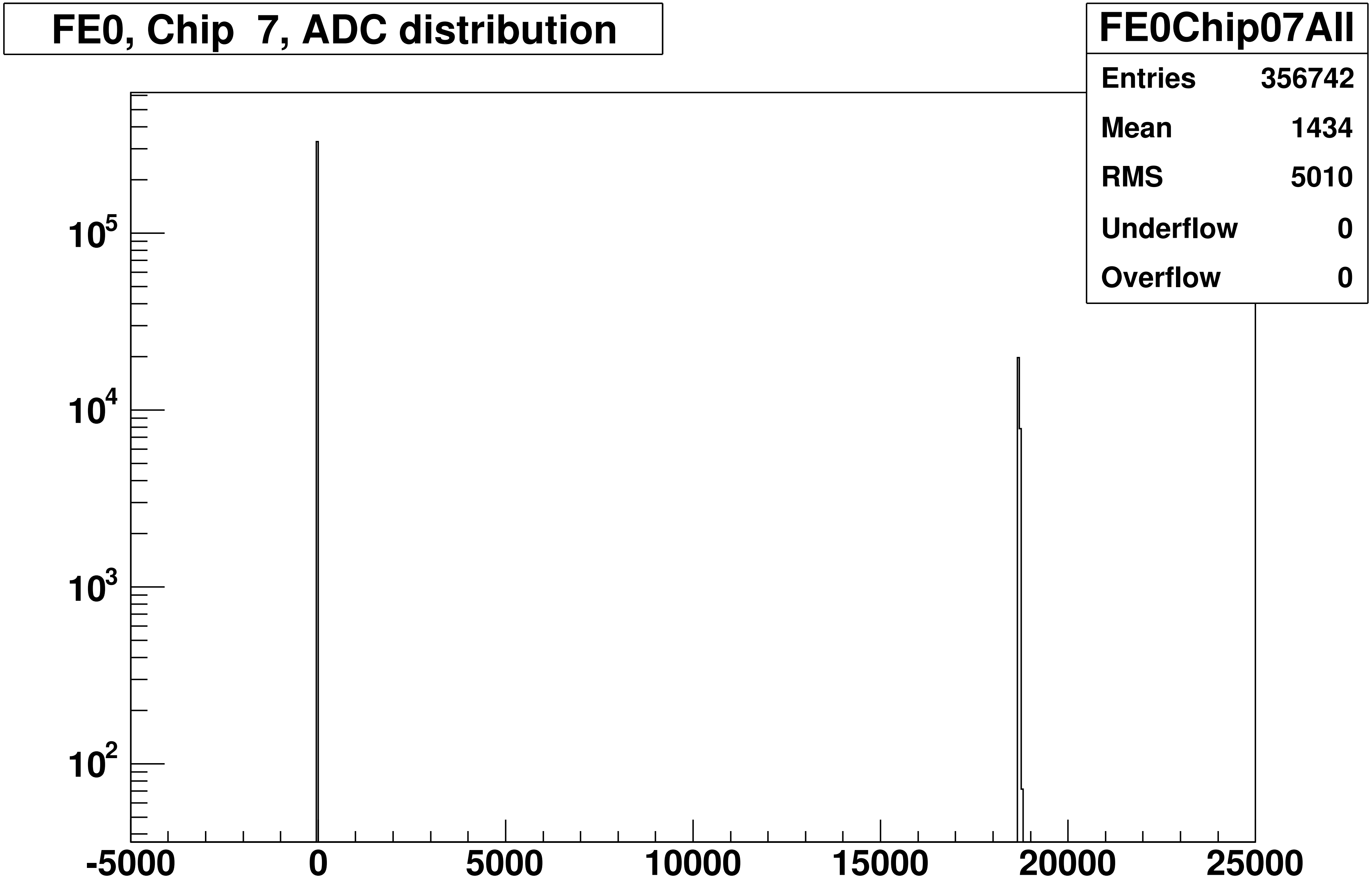
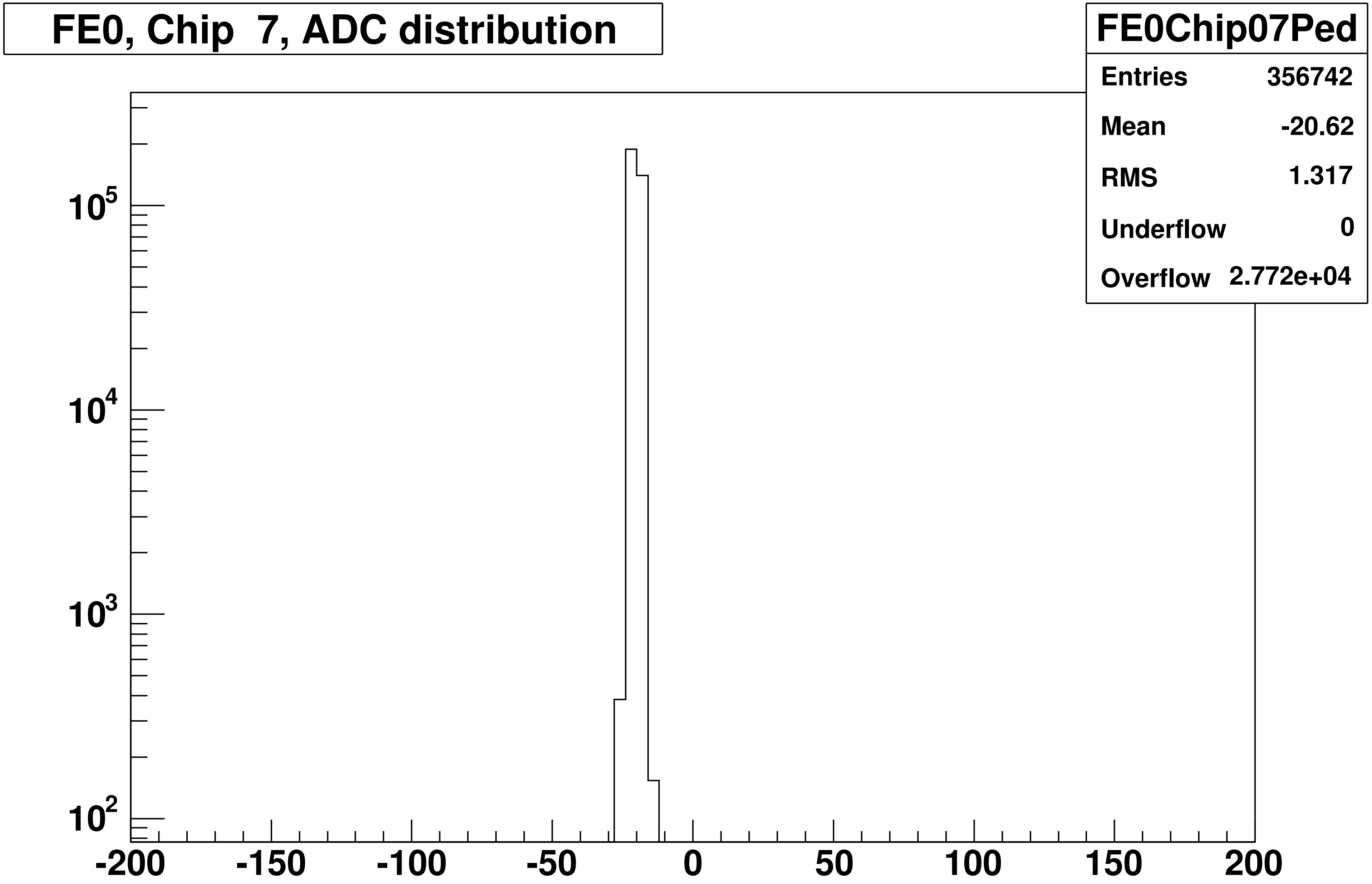
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 356742
Mean 1.867e+04
RMS 12.63
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 356742
Mean 1434
RMS 5010
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 356742
Mean -20.62
RMS 1.317
Underflow 0
Overflow 2.772e+04
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10^4
10^3
10^2
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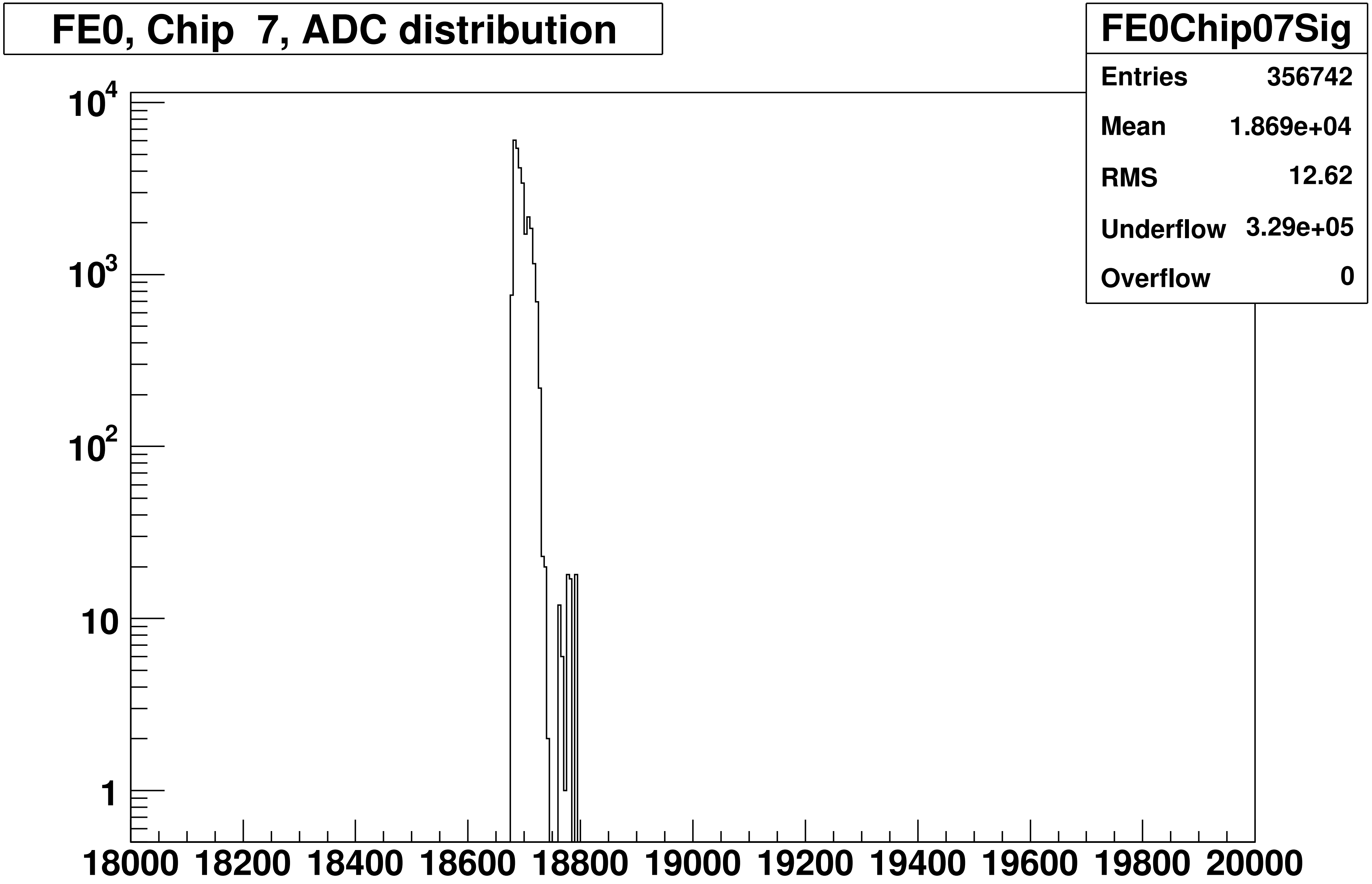
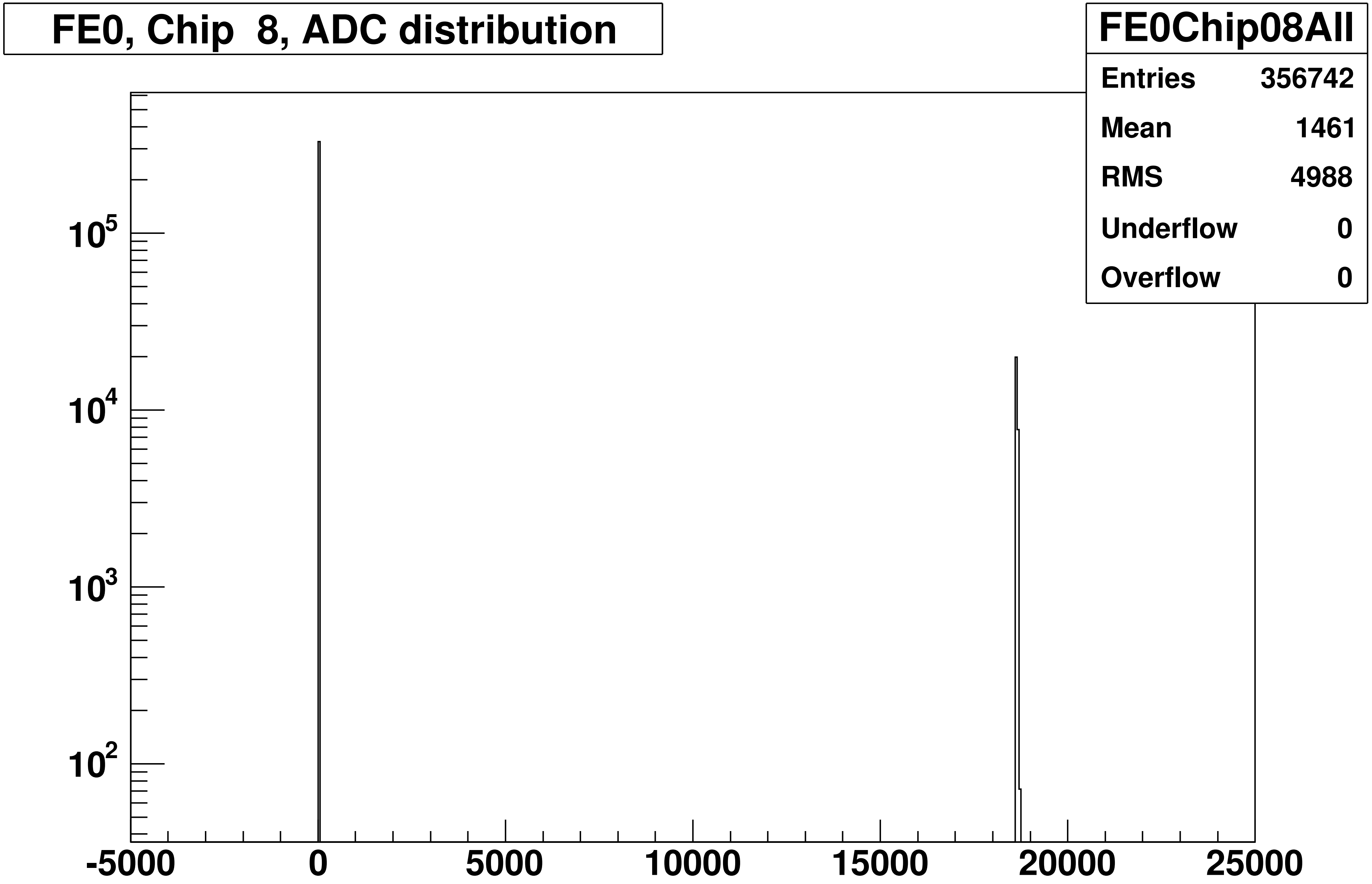
-150
-100
-50
0
50
100
150
200


FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 356742
Mean 1.869e+04
RMS 12.62
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 356742
Mean 1461
RMS 4988
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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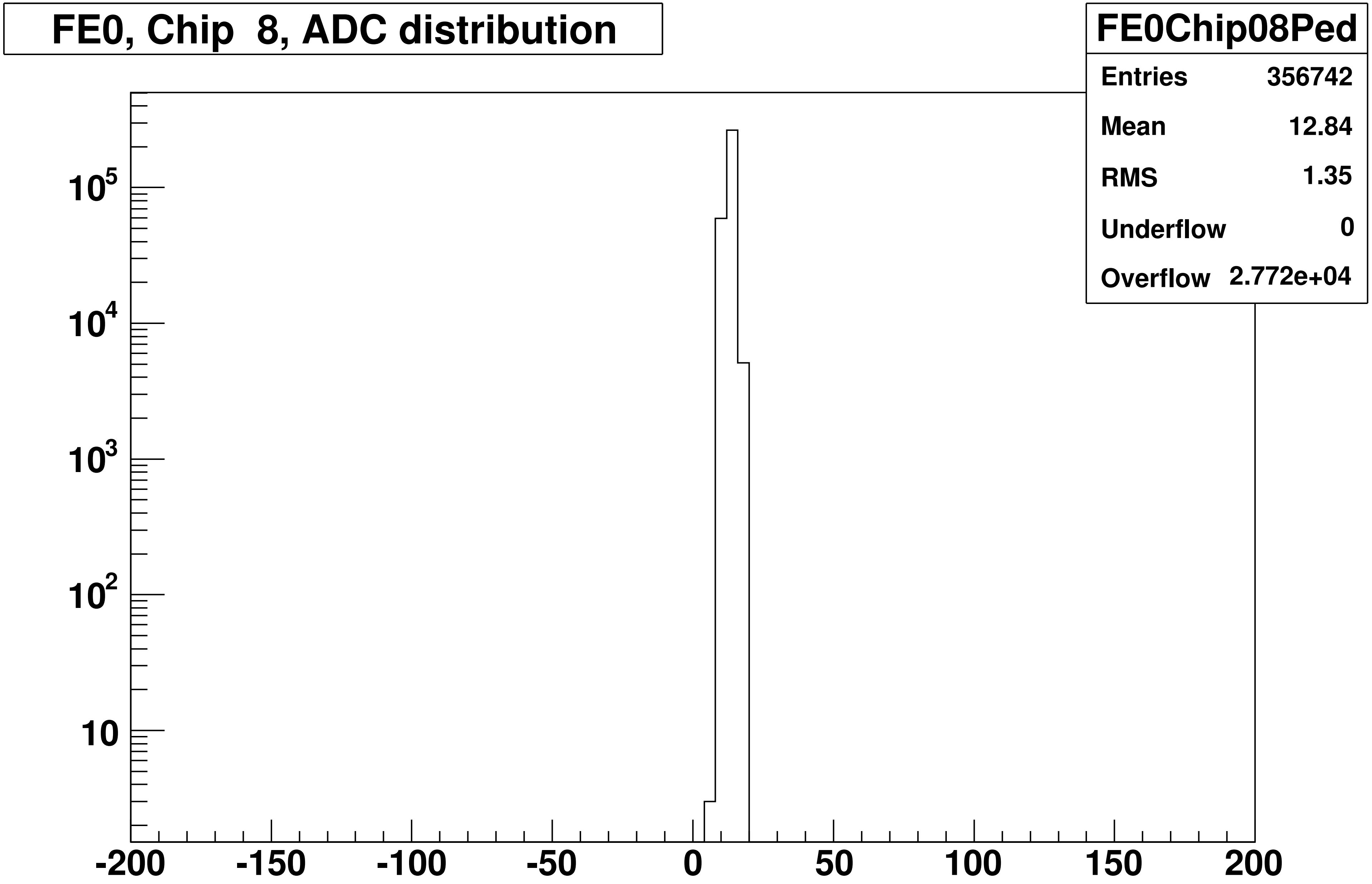
0
5000
10000
15000
20000
25000


FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 356742
Mean 12.84
RMS 1.35
Underflow 0
Overflow 2.772e+04
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10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
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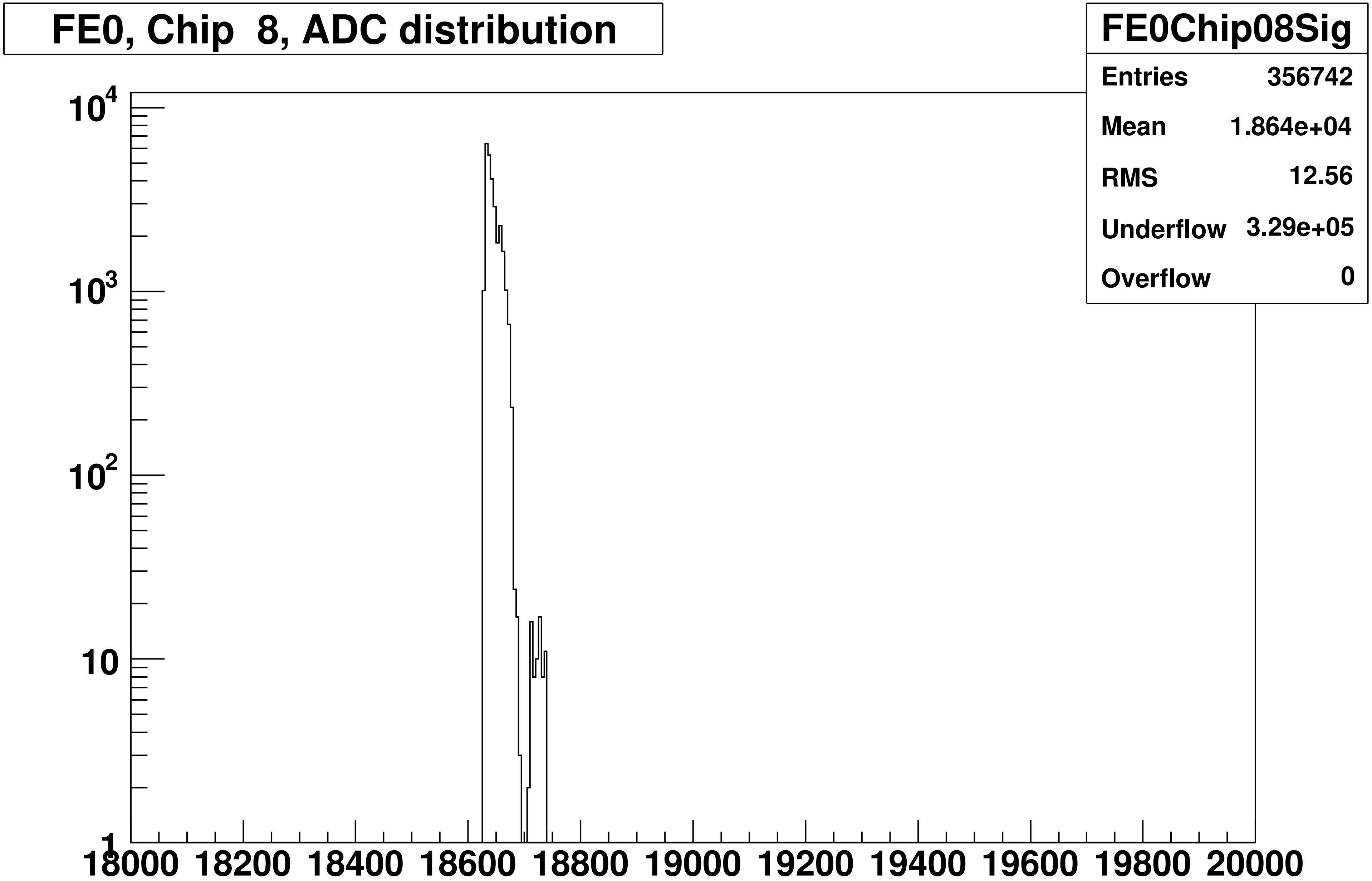
100
150
200



FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 356742
Mean 1.864e+04
RMS 12.56
Underflow 3.29e+05
Overflow 0
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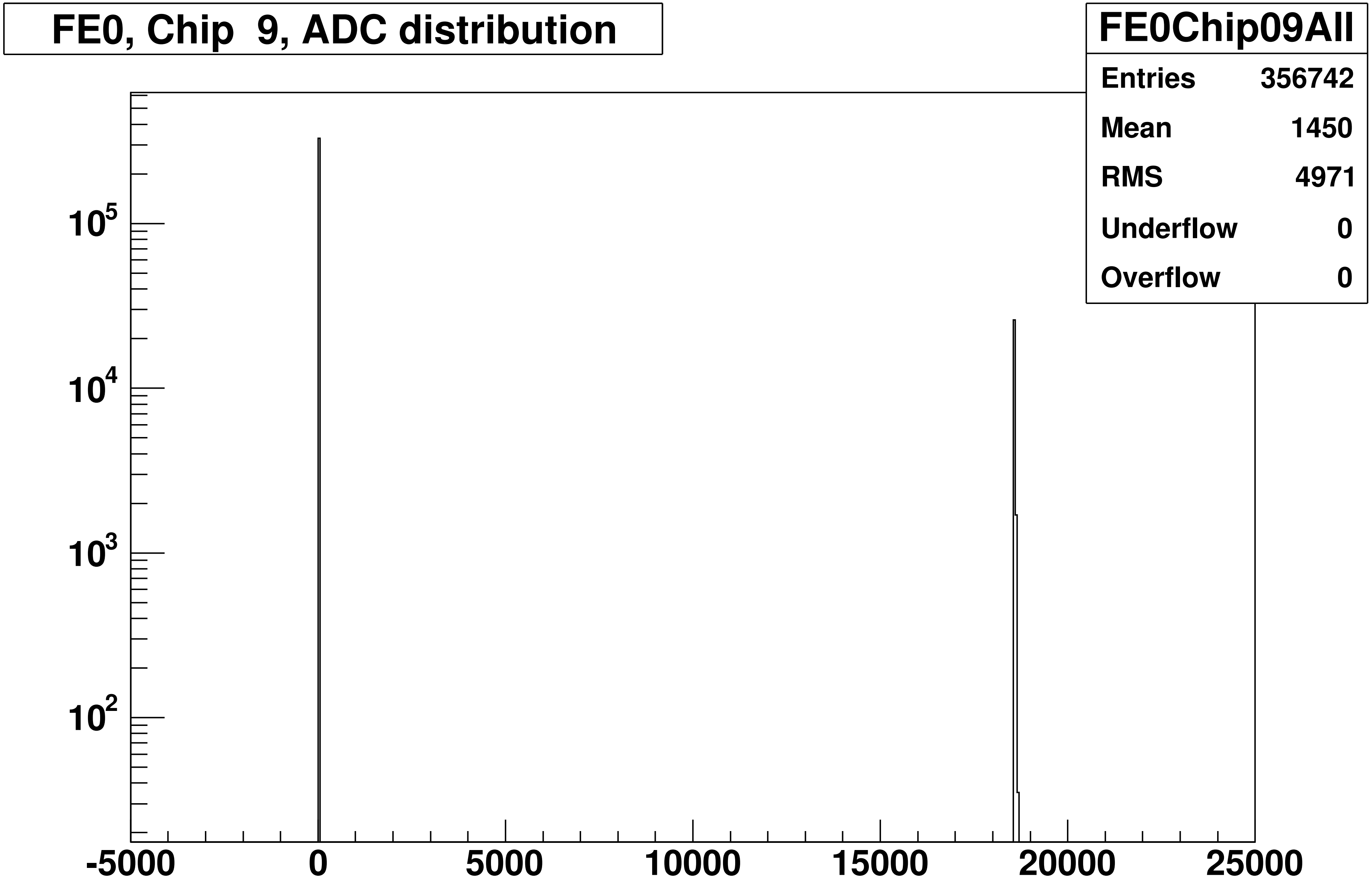
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 356742
Mean 1450
RMS 4971
Underflow 0
Overflow 0
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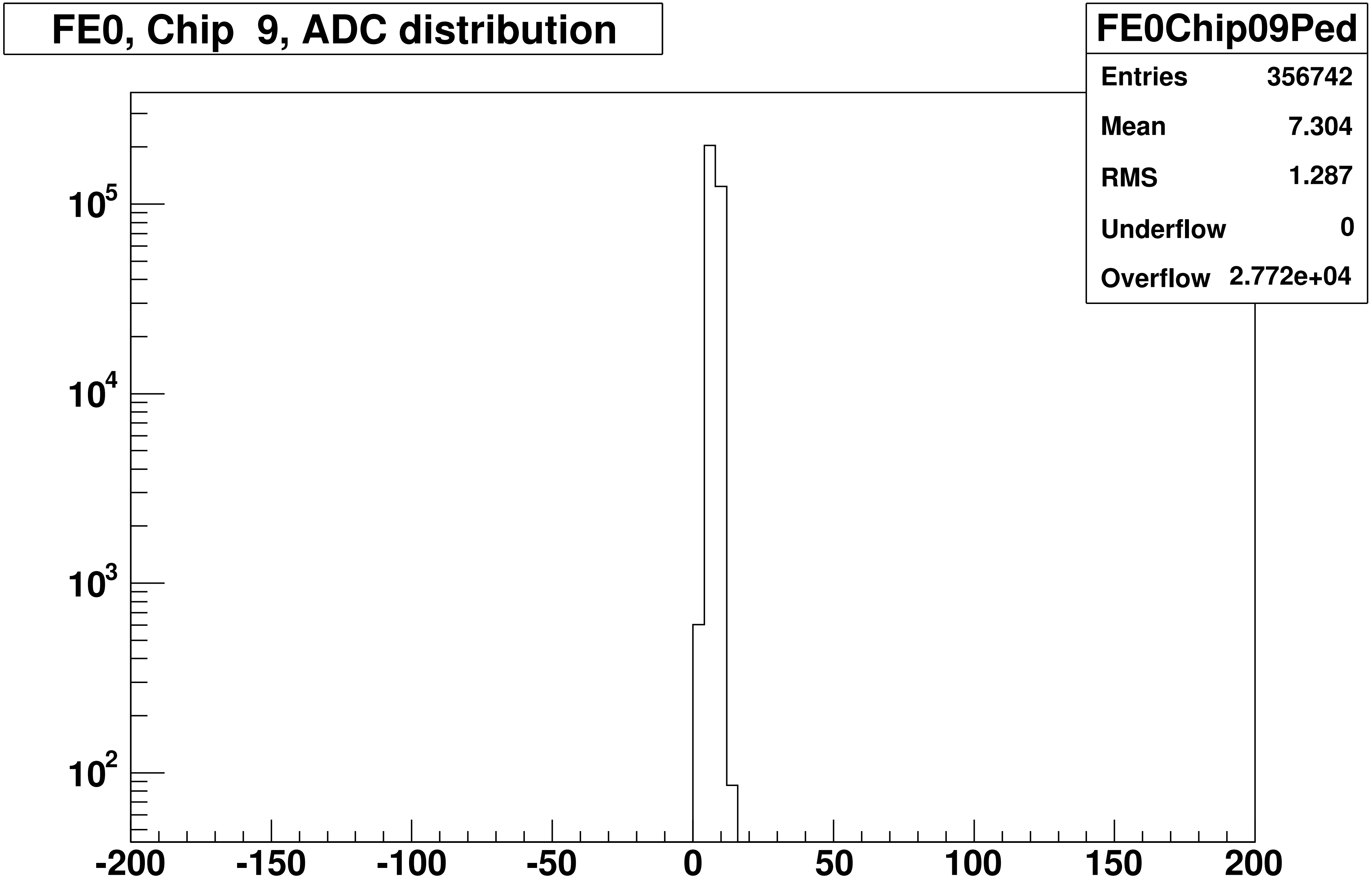
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 356742
Mean 7.304
RMS 1.287
Underflow 0
Overflow 2.772e+04
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10^4
10^3
10^2
-200
-150
-100
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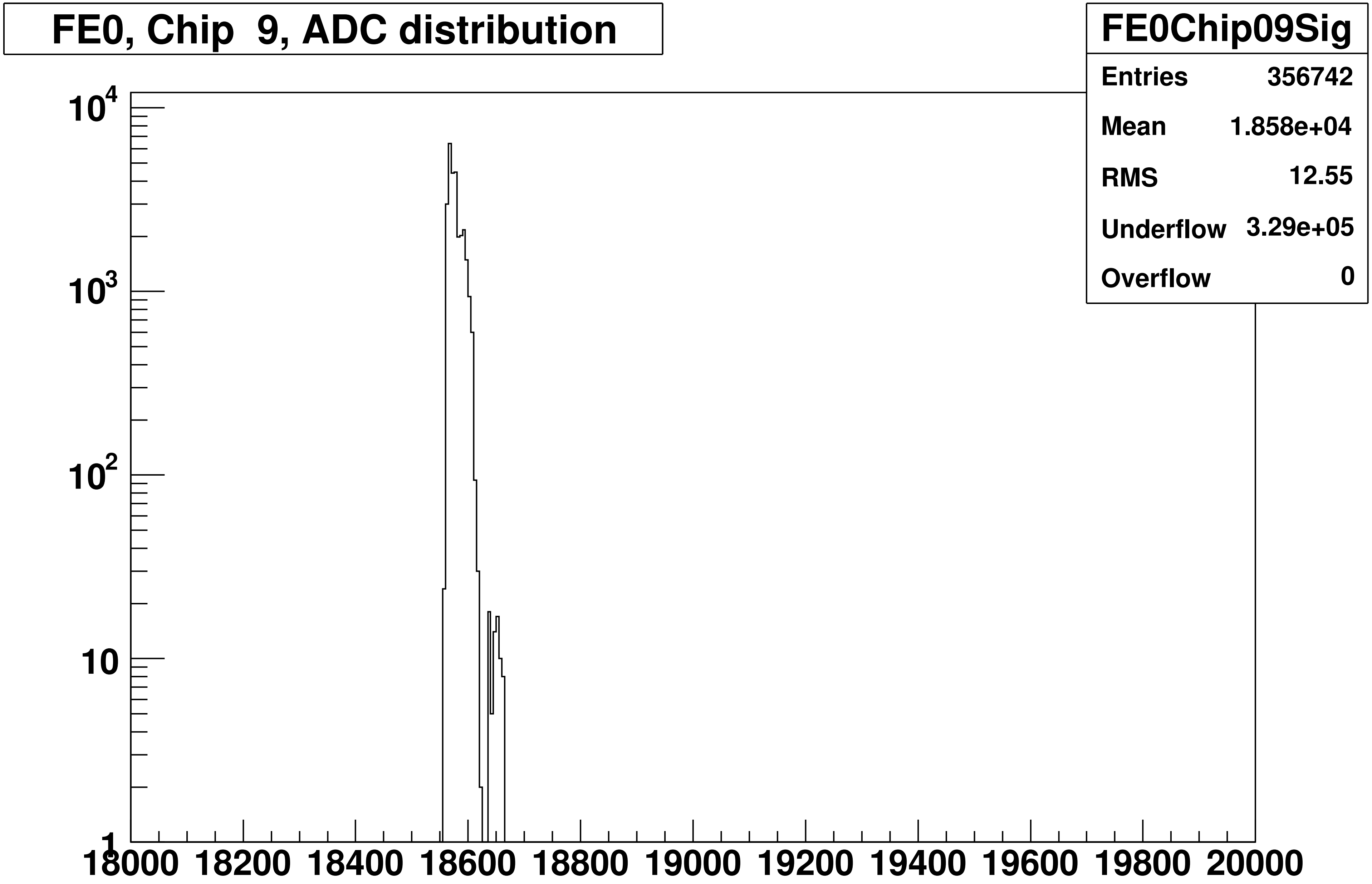
50
100
150
200



FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 356742
Mean 1.858e+04
RMS 12.55
Underflow 3.29e+05
Overflow 0
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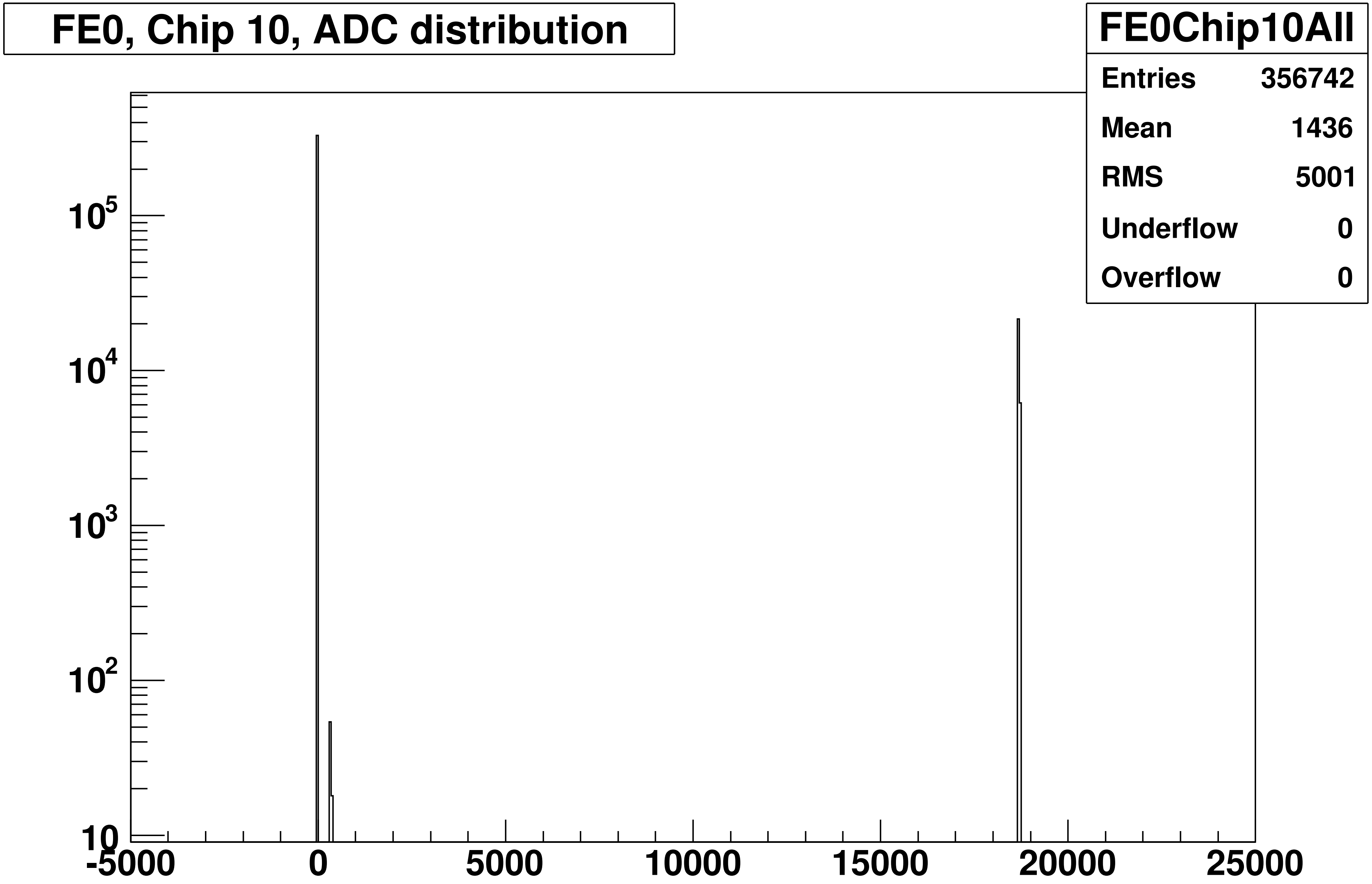
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 356742
Mean 1436
RMS 5001
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
-5000
0
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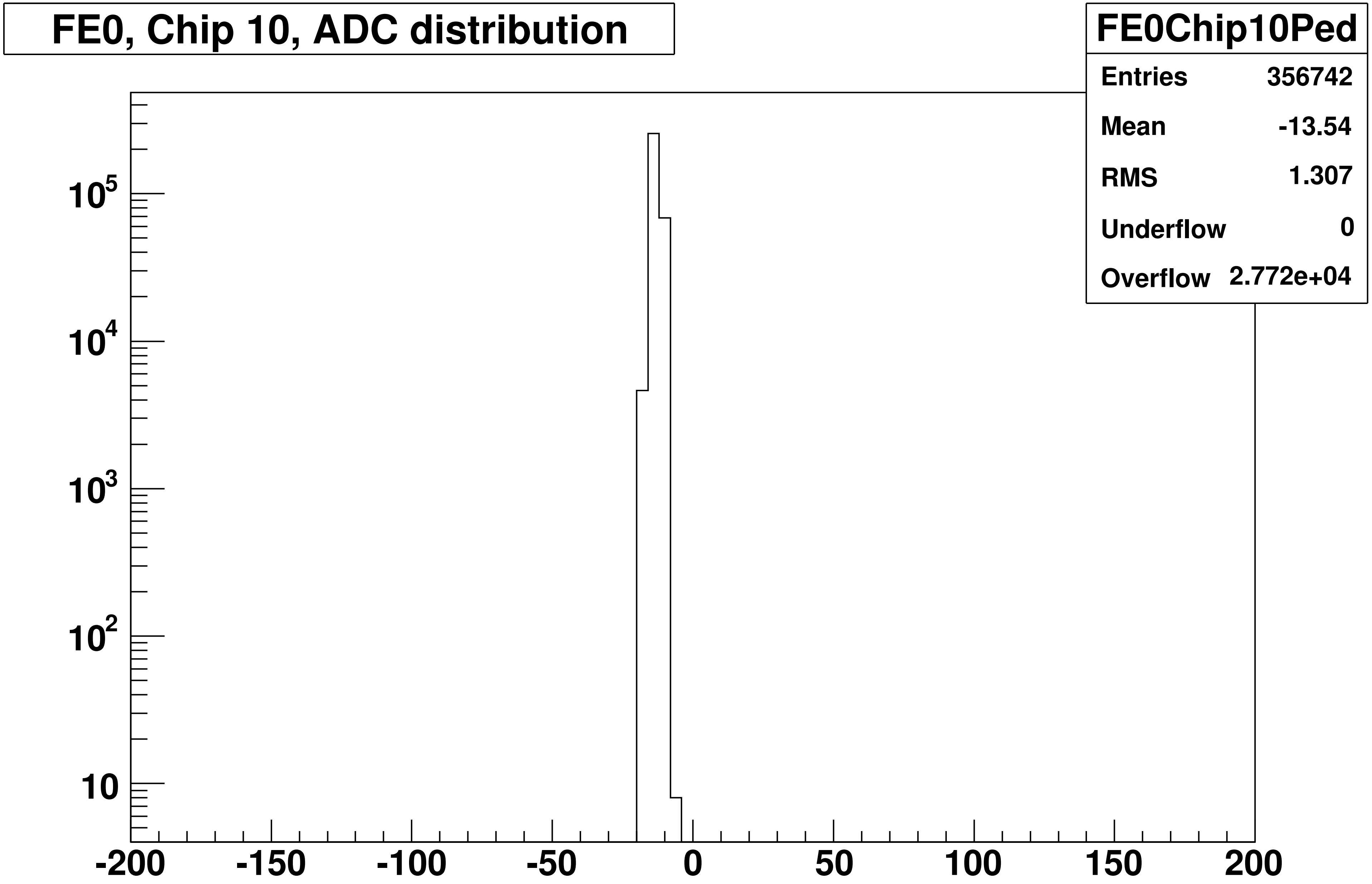
10000
15000
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 356742
Mean -13.54
RMS 1.307
Underflow 0
Overflow 2.772e+04
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10^2
10^3
10^4
10^5
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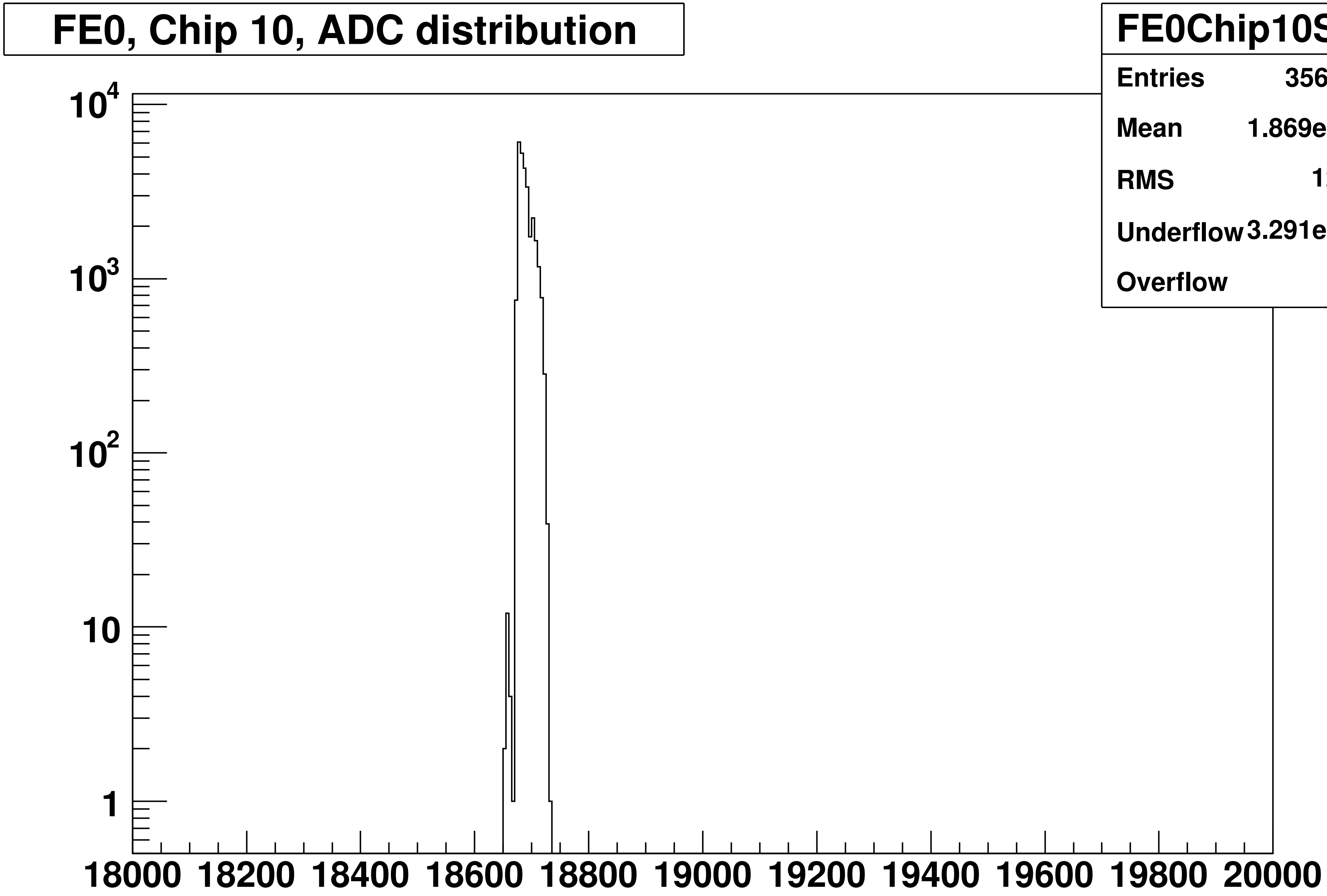
-100
-50
0
50
100
150
200


FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 356742
Mean 1.869e+04
RMS 12.01
Underflow 3.291e+05
Overflow 0
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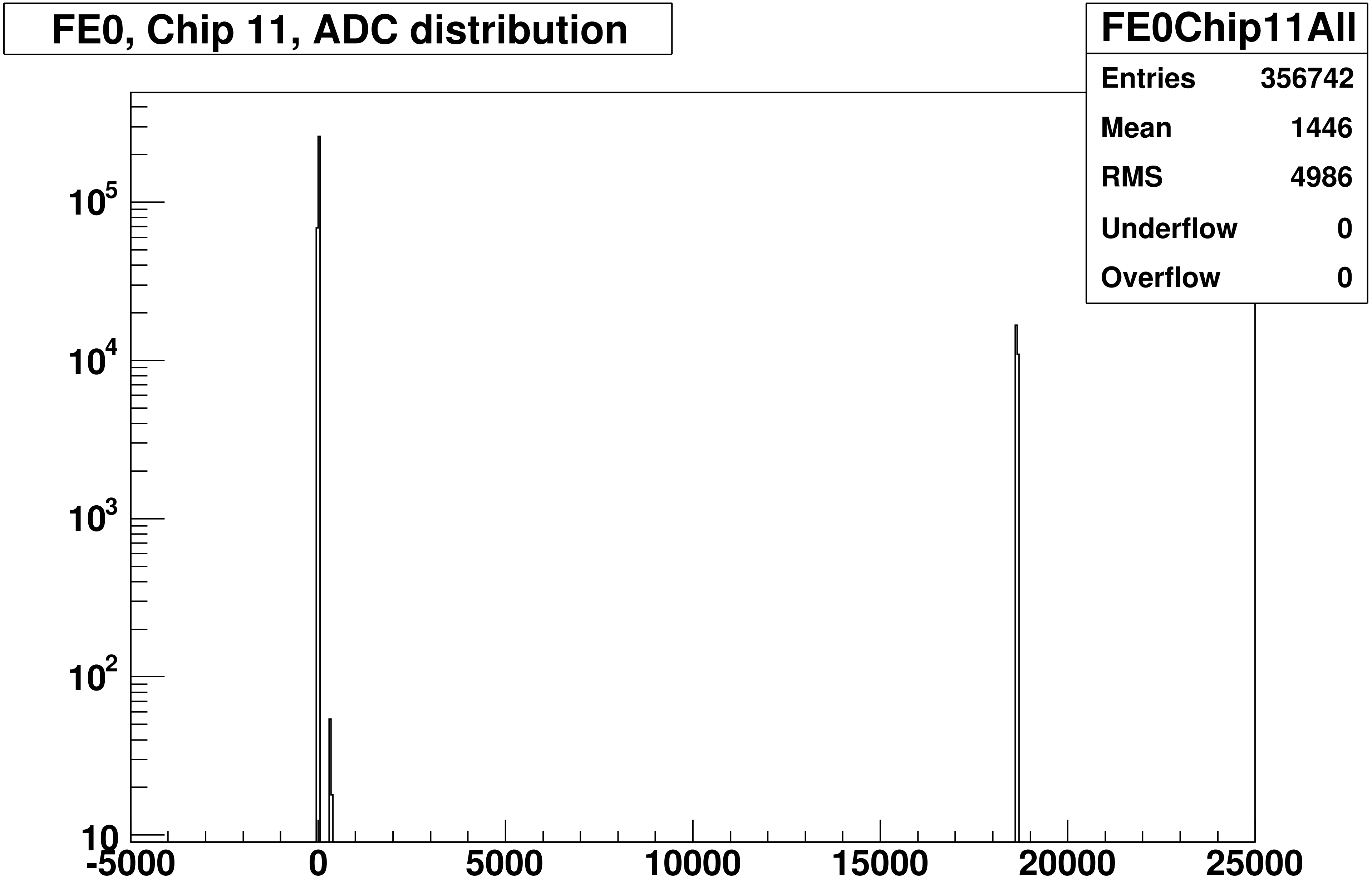
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 356742
Mean 1446
RMS 4986
Underflow 0
Overflow 0
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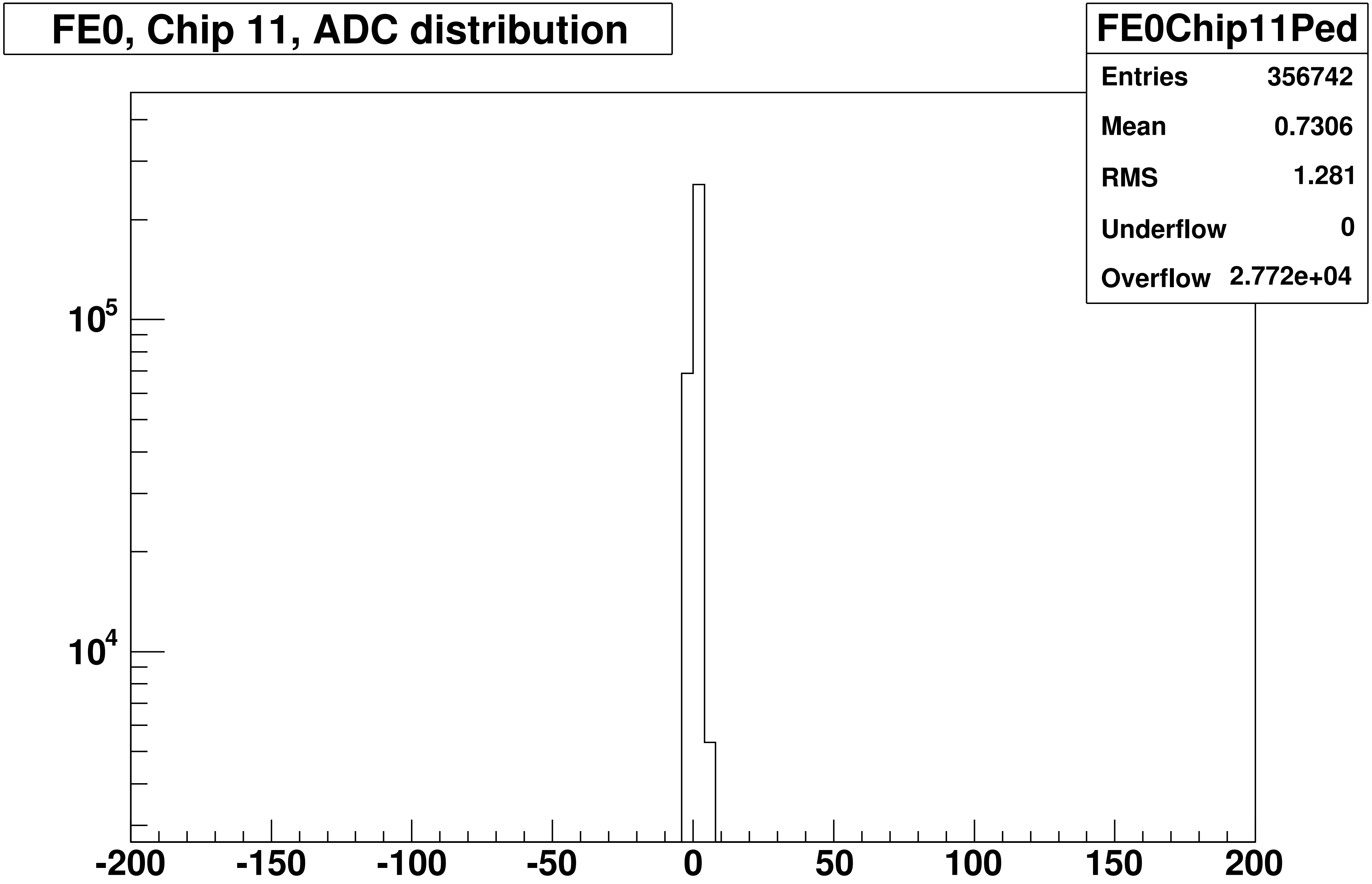
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 356742
Mean 0.7306
RMS 1.281
Underflow 0
Overflow 2.772e+04
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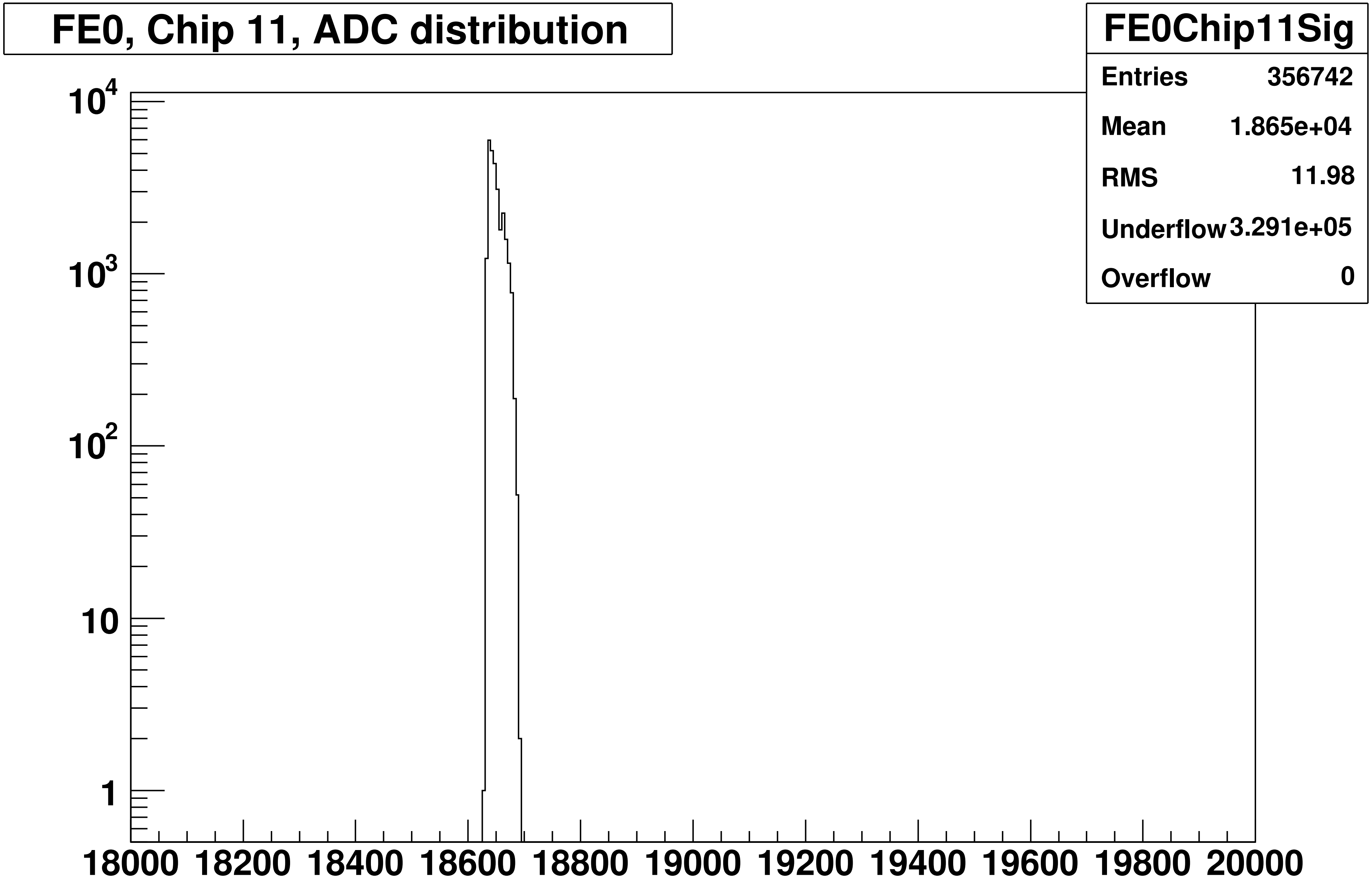
10^4
-200
-150
-100
-50
0
50
100
150
200



FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 356742
Mean 1.865e+04
RMS 11.98
Underflow 3.291e+05
Overflow 0
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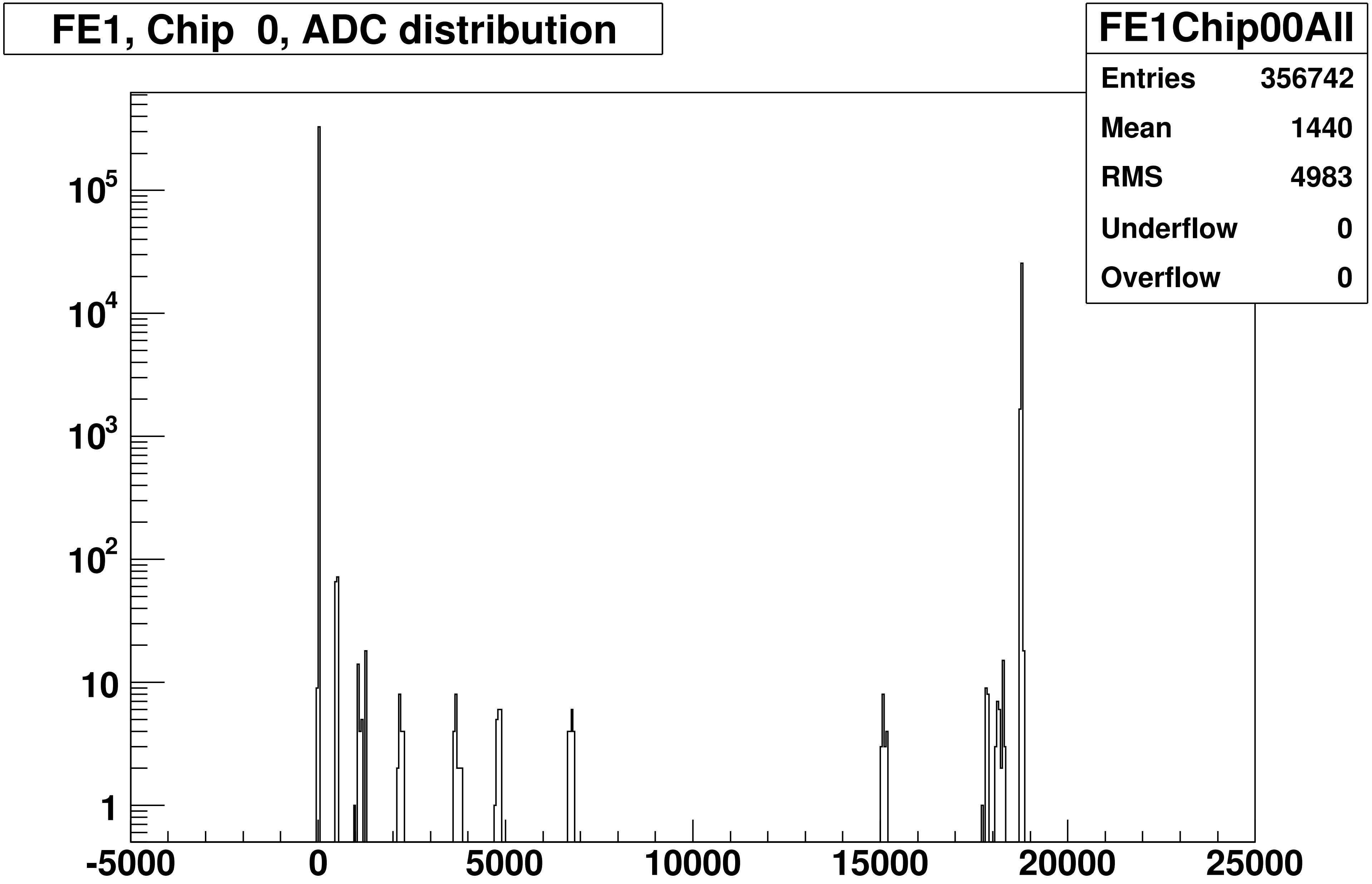
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 356742
Mean 1440
RMS 4983
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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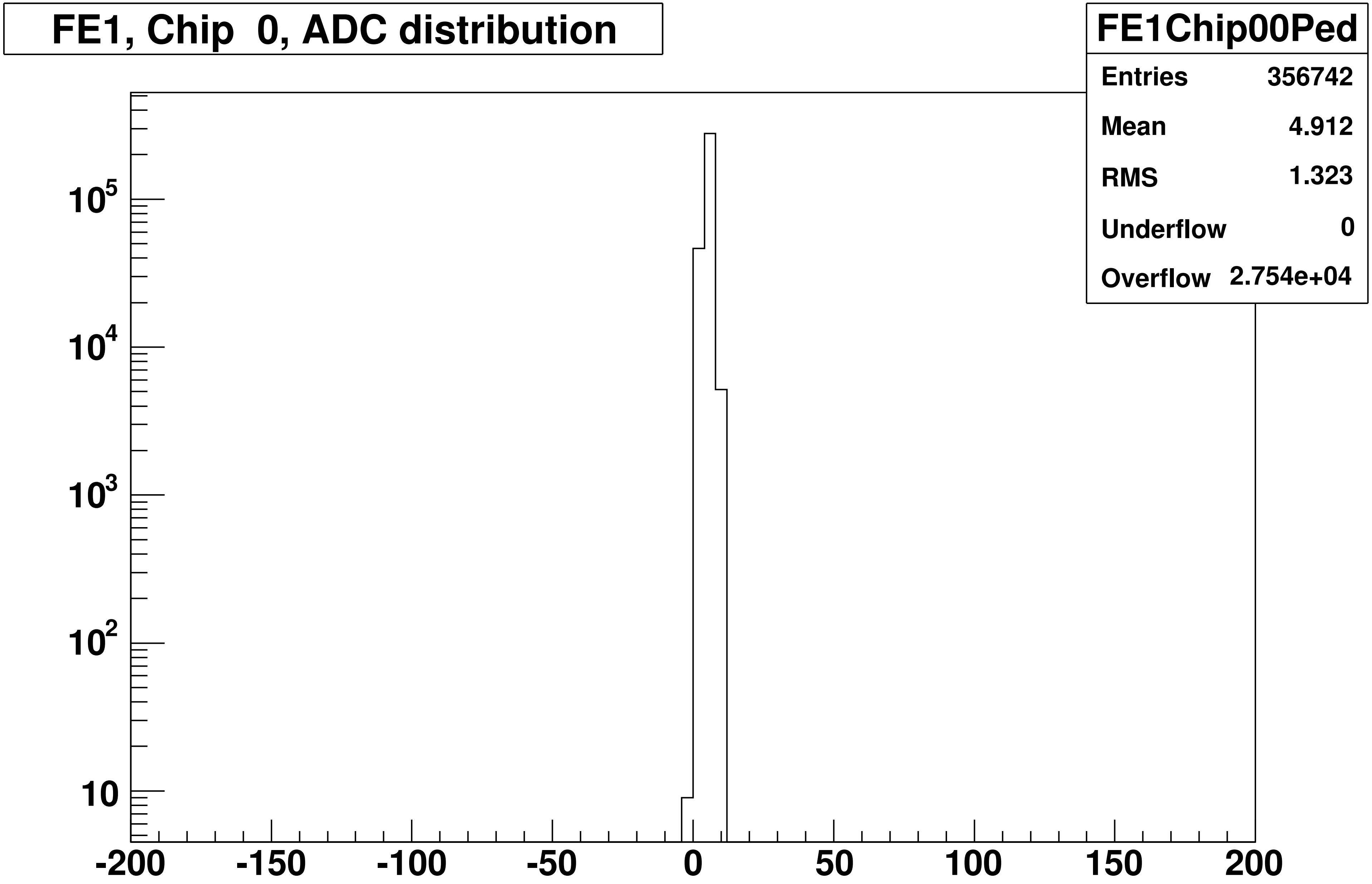
10000
15000
20000
25000


FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 356742
Mean 4.912
RMS 1.323
Underflow 0
Overflow 2.754e+04
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10^4
10^3
10^2
10
-200
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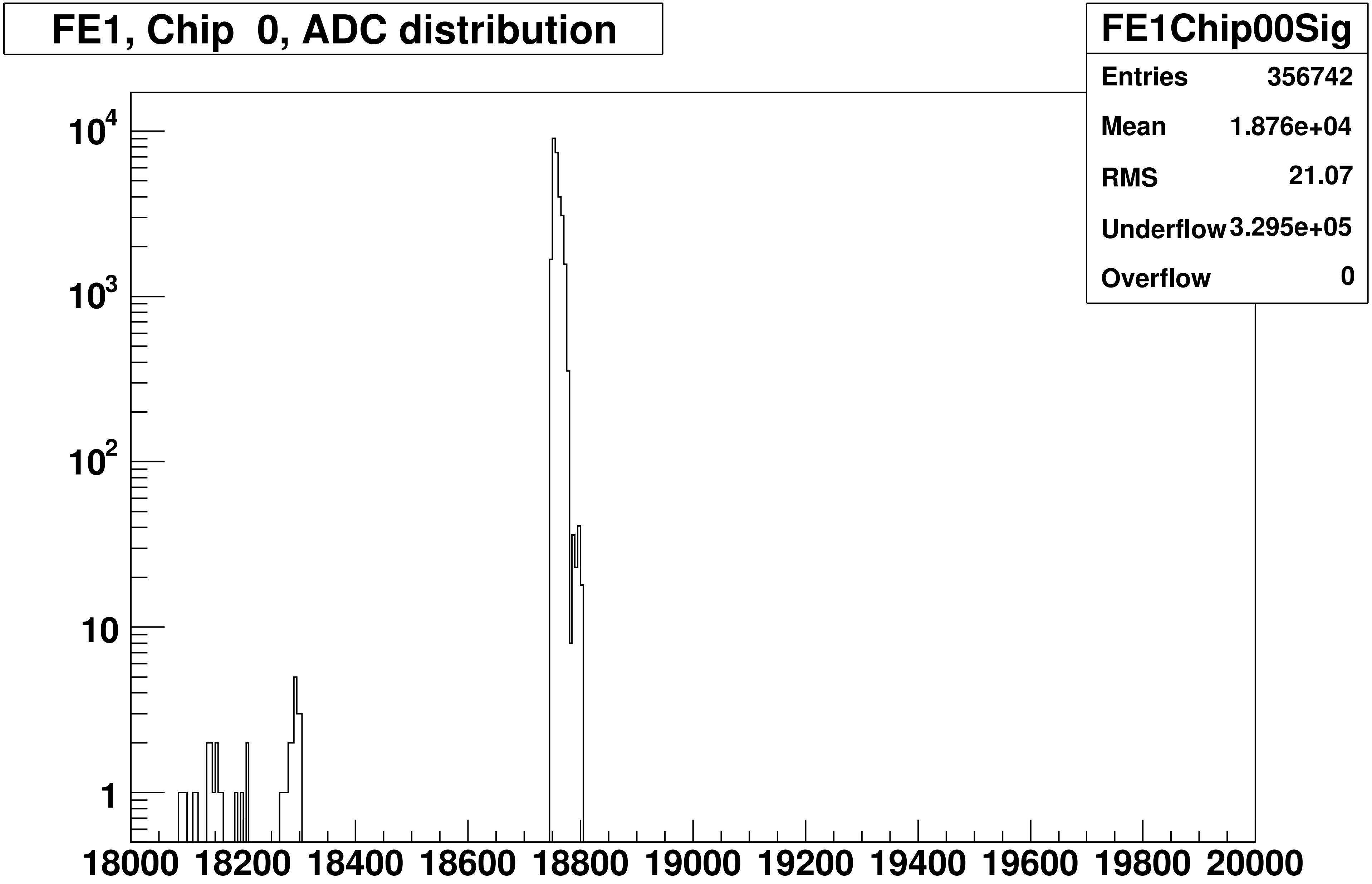
-100
-50
0
50
100
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 356742
Mean 1.876e+04
RMS 21.07
Underflow 3.295e+05
Overflow 0
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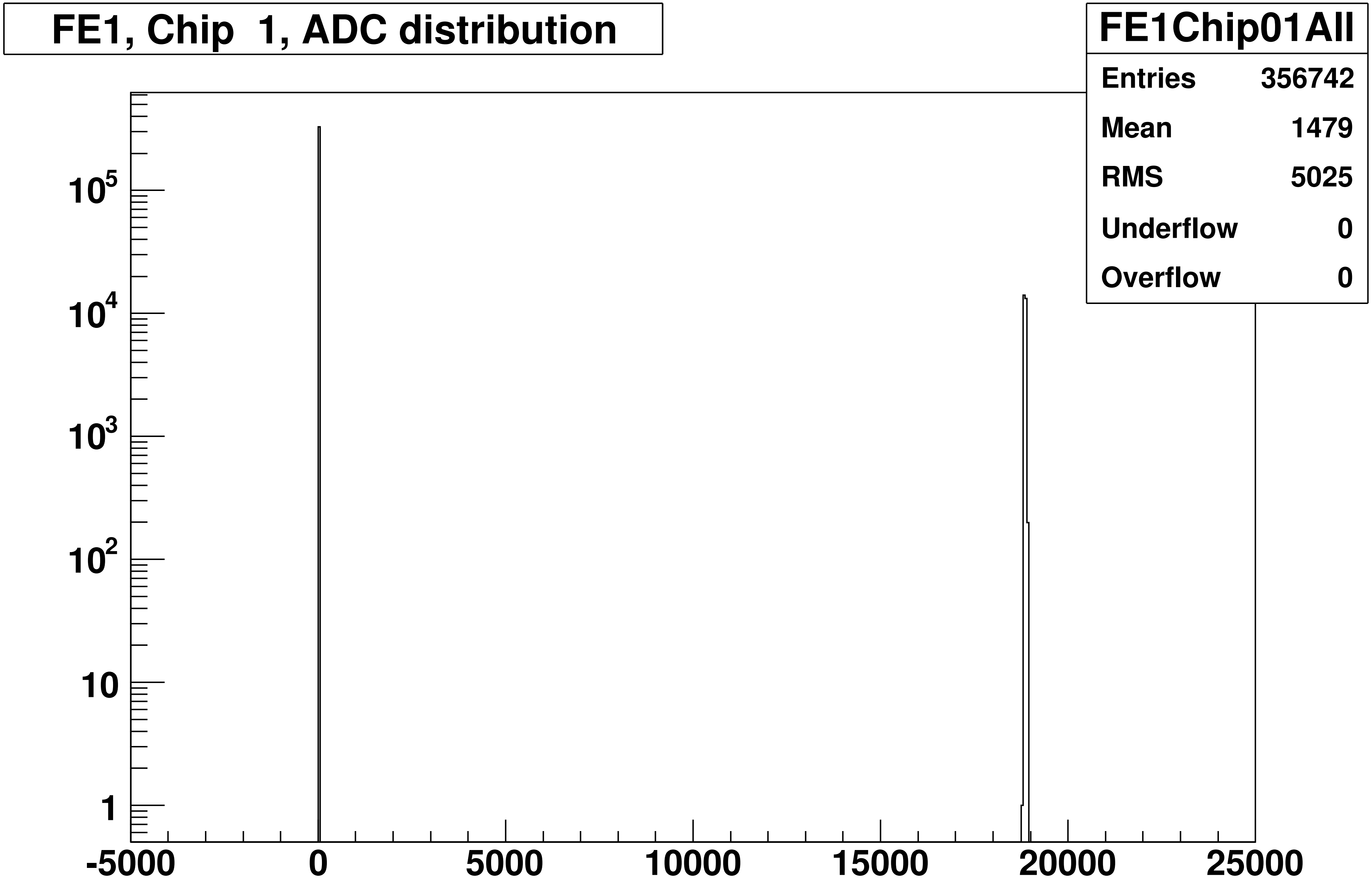
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 356742
Mean 1479
RMS 5025
Underflow 0
Overflow 0
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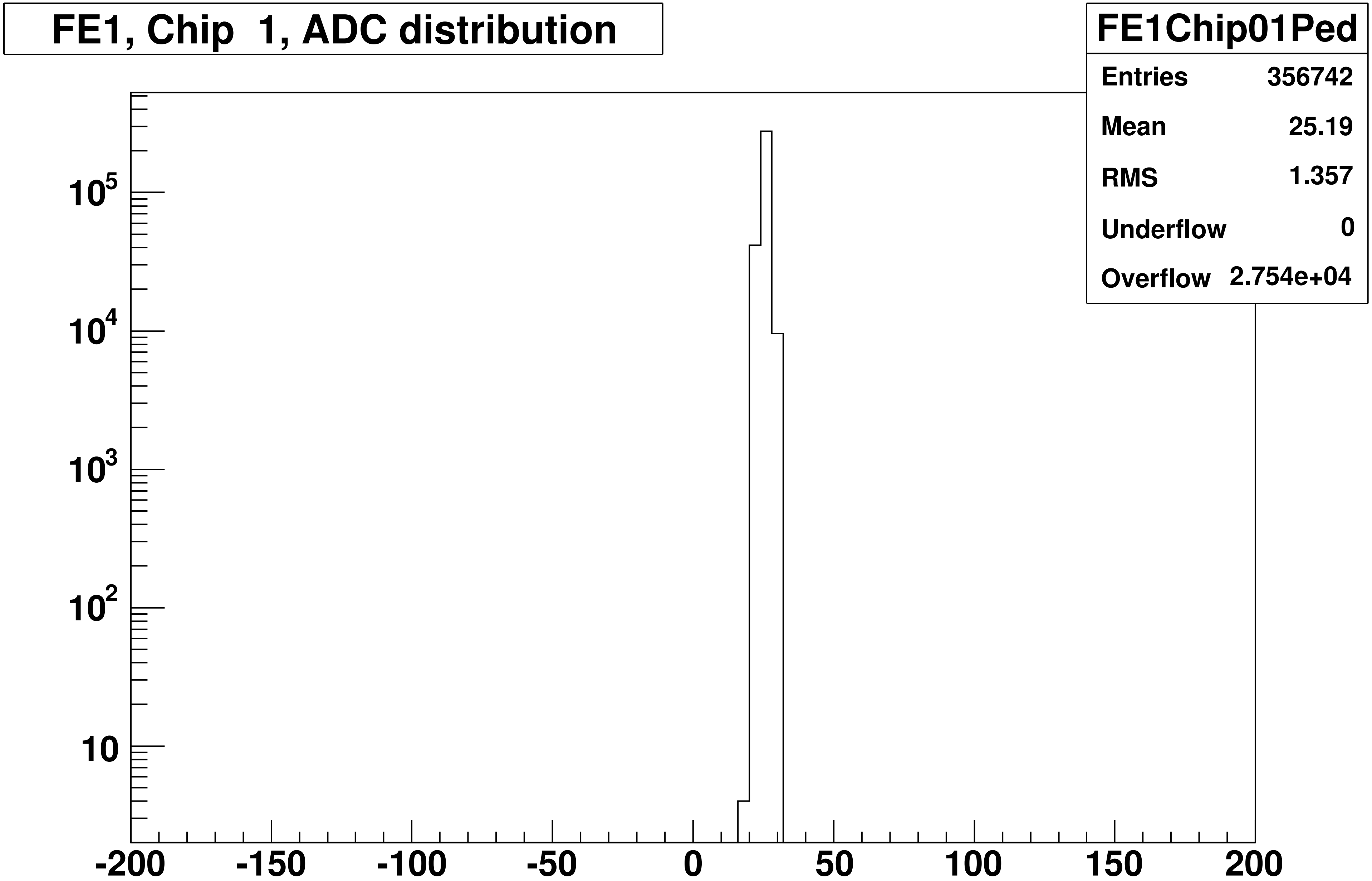
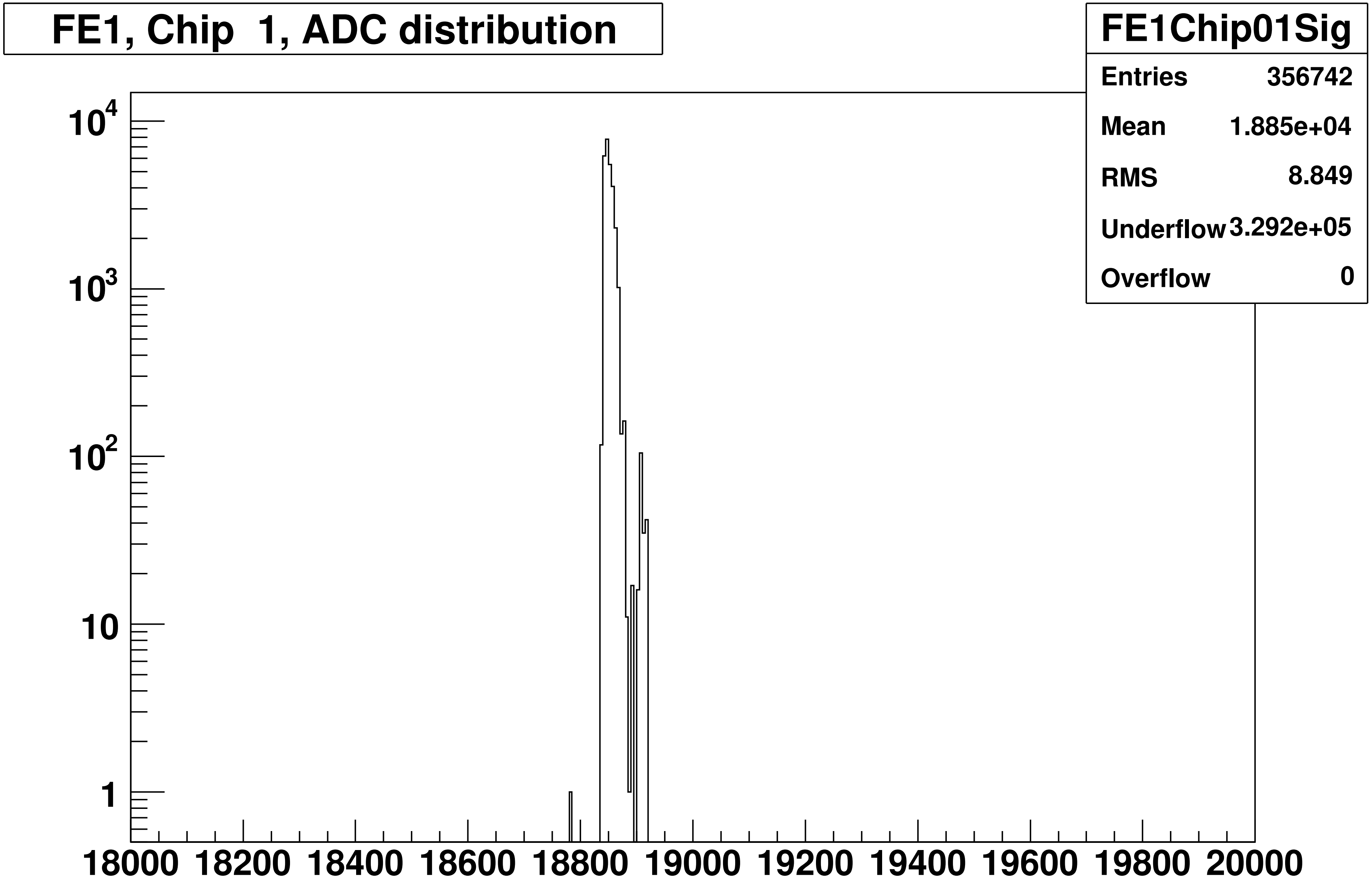
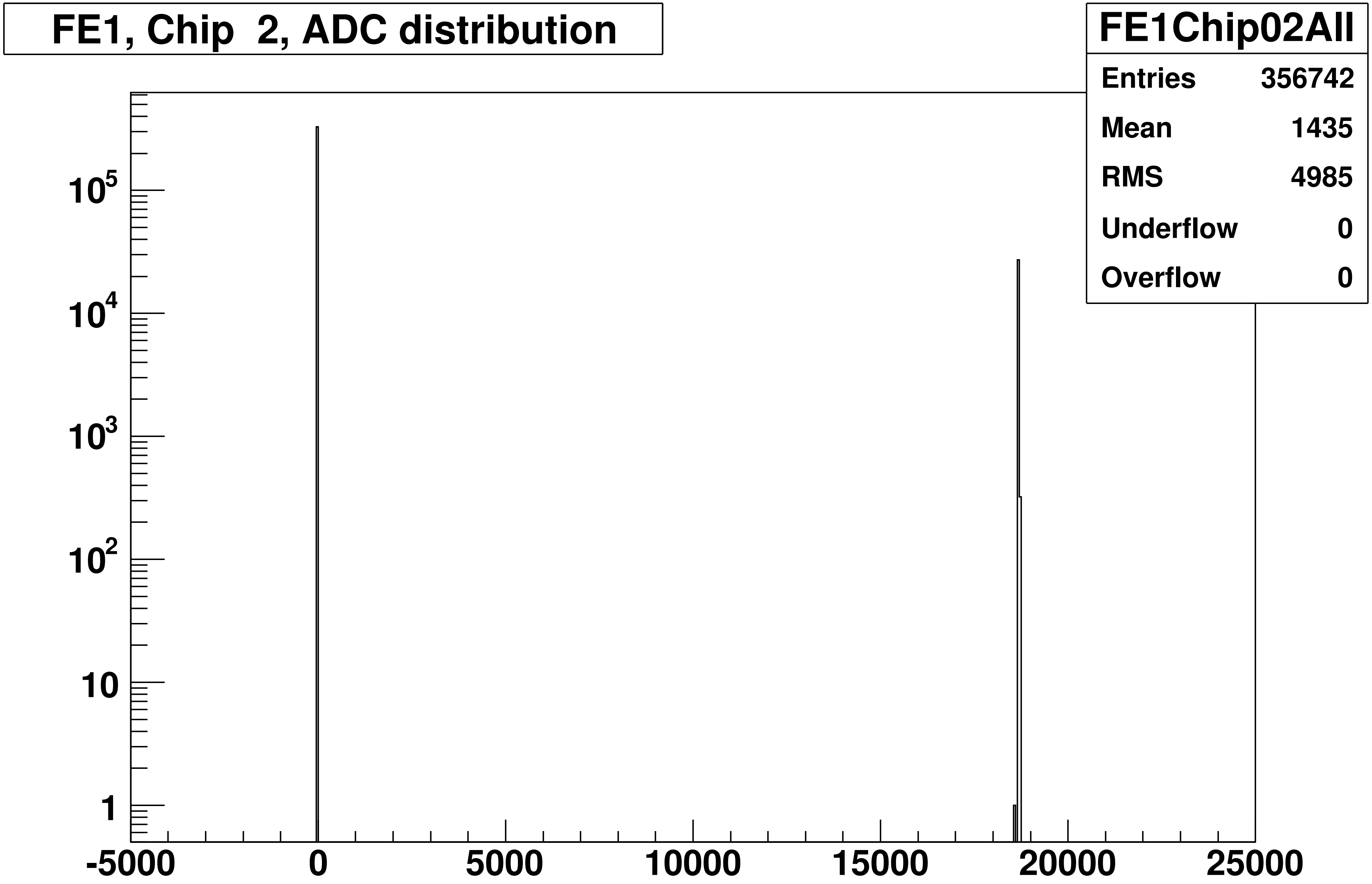
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 356742
Mean 25.19
RMS 1.357
Underflow 0
Overflow 2.754e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 356742
Mean 1.885e+04
RMS 8.849
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 356742
Mean 1435
RMS 4985
Underflow 0
Overflow 0
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10^4
10^3
10^2
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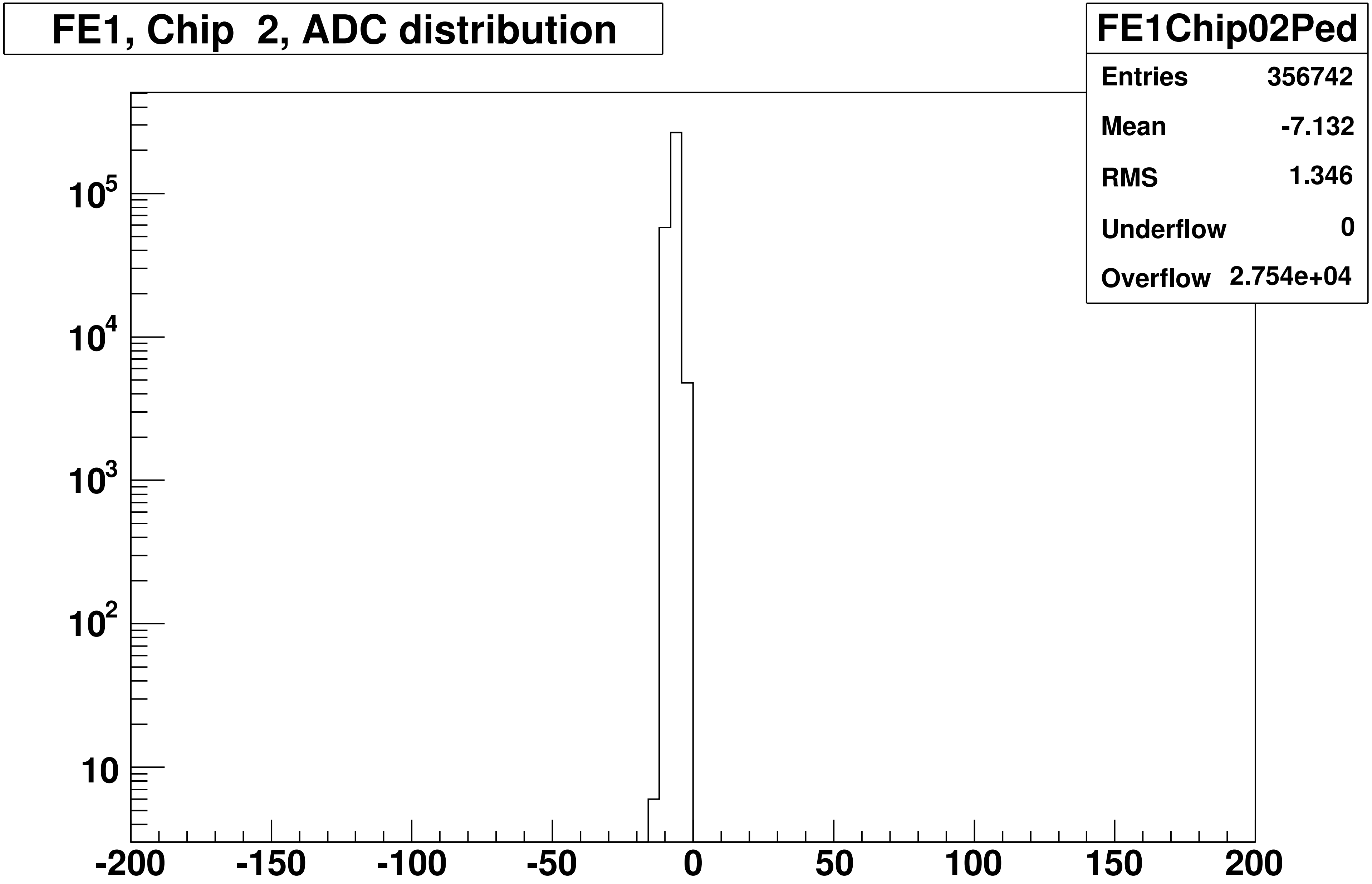

FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 356742
Mean -7.132
RMS 1.346
Underflow 0
Overflow 2.754e+04
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10^3
10^2
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150
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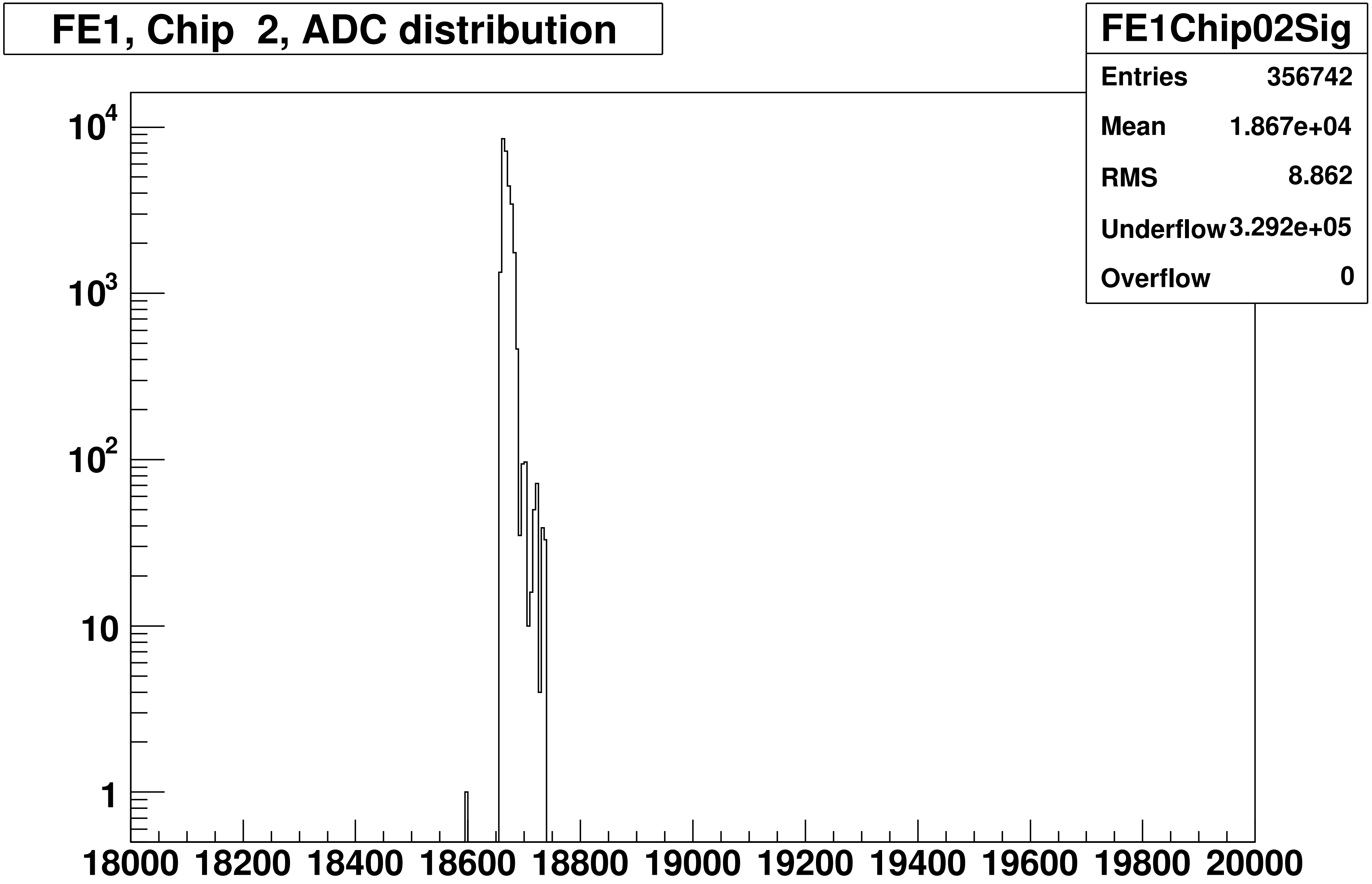

FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 356742
Mean 1.867e+04
RMS 8.862
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
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19600
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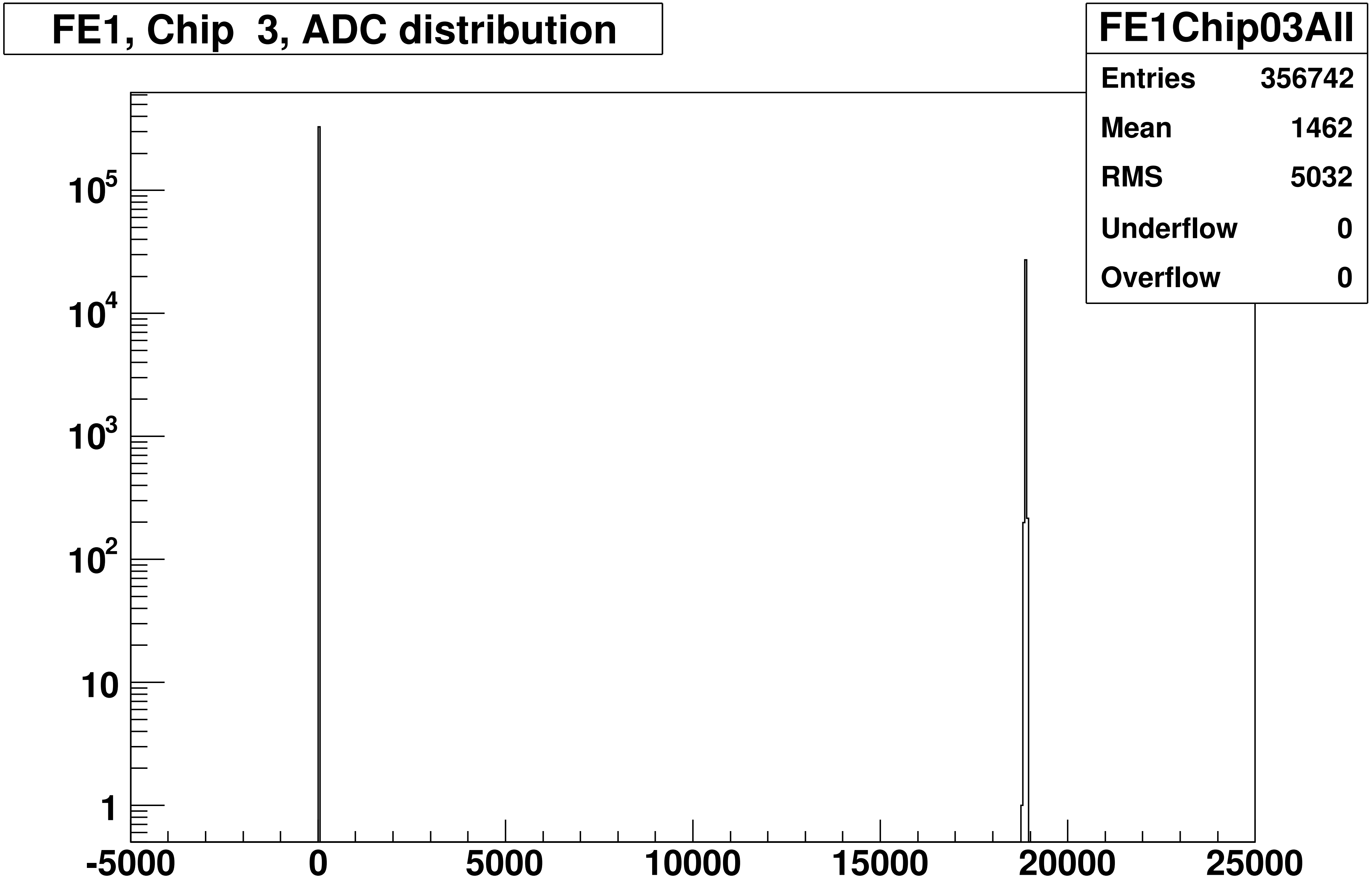
20000


FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 356742
Mean 1462
RMS 5032
Underflow 0
Overflow 0
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10^3
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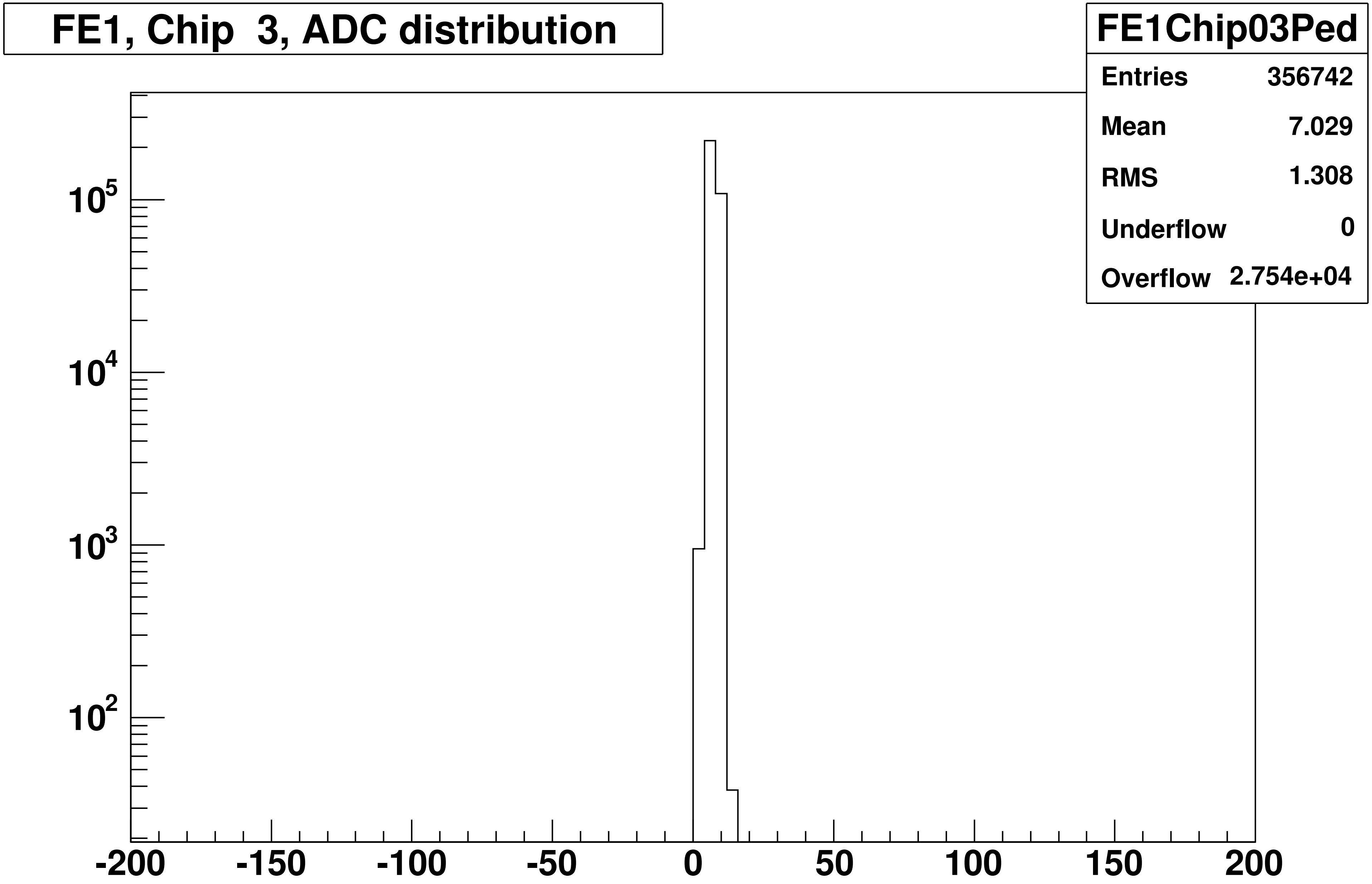

FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 356742
Mean 7.029
RMS 1.308
Underflow 0
Overflow 2.754e+04
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10^4
10^3
10^2
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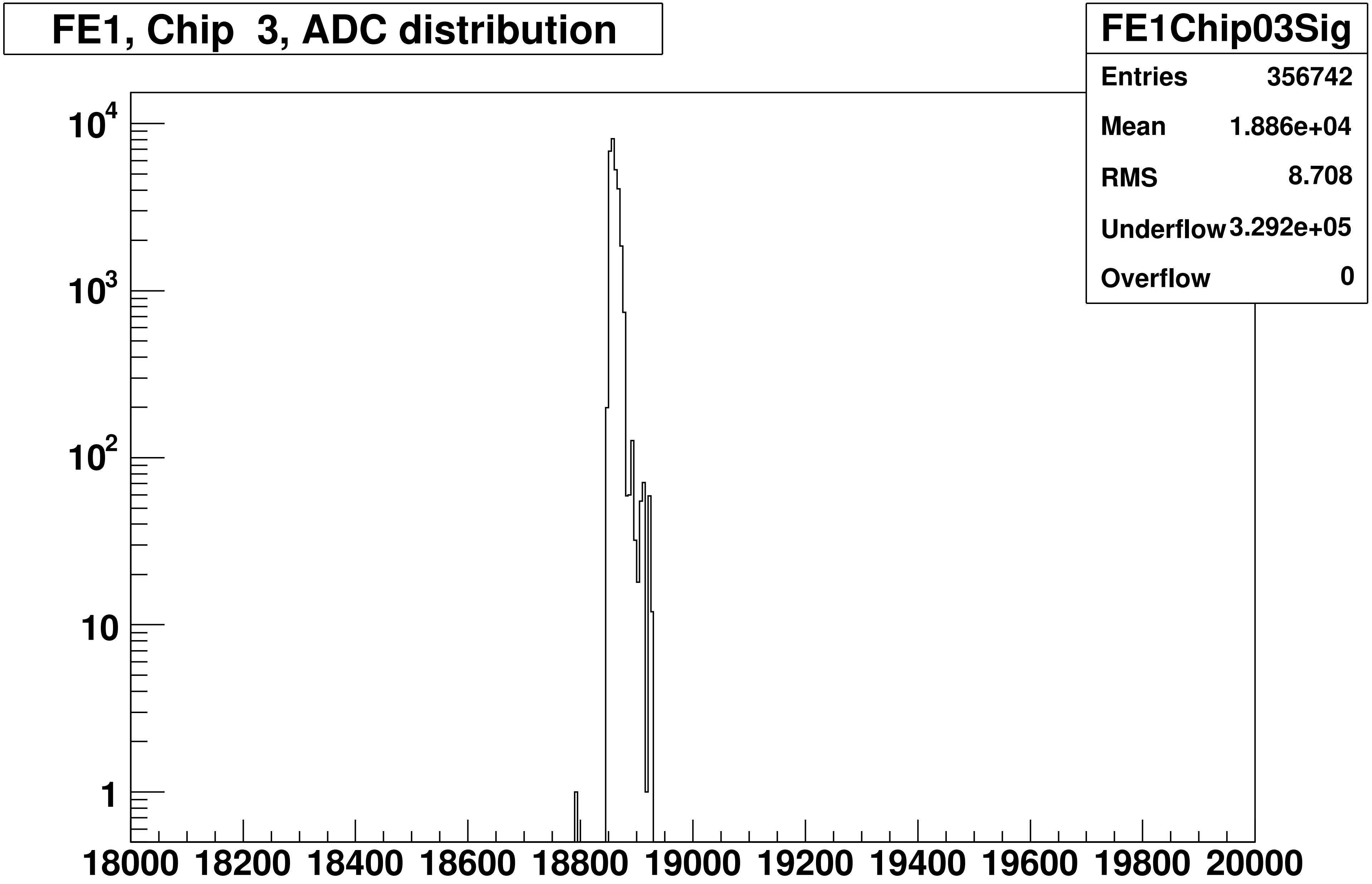
FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 356742
Mean 1.886e+04
RMS 8.708
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
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1
18000
18200
18400
18600
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19000
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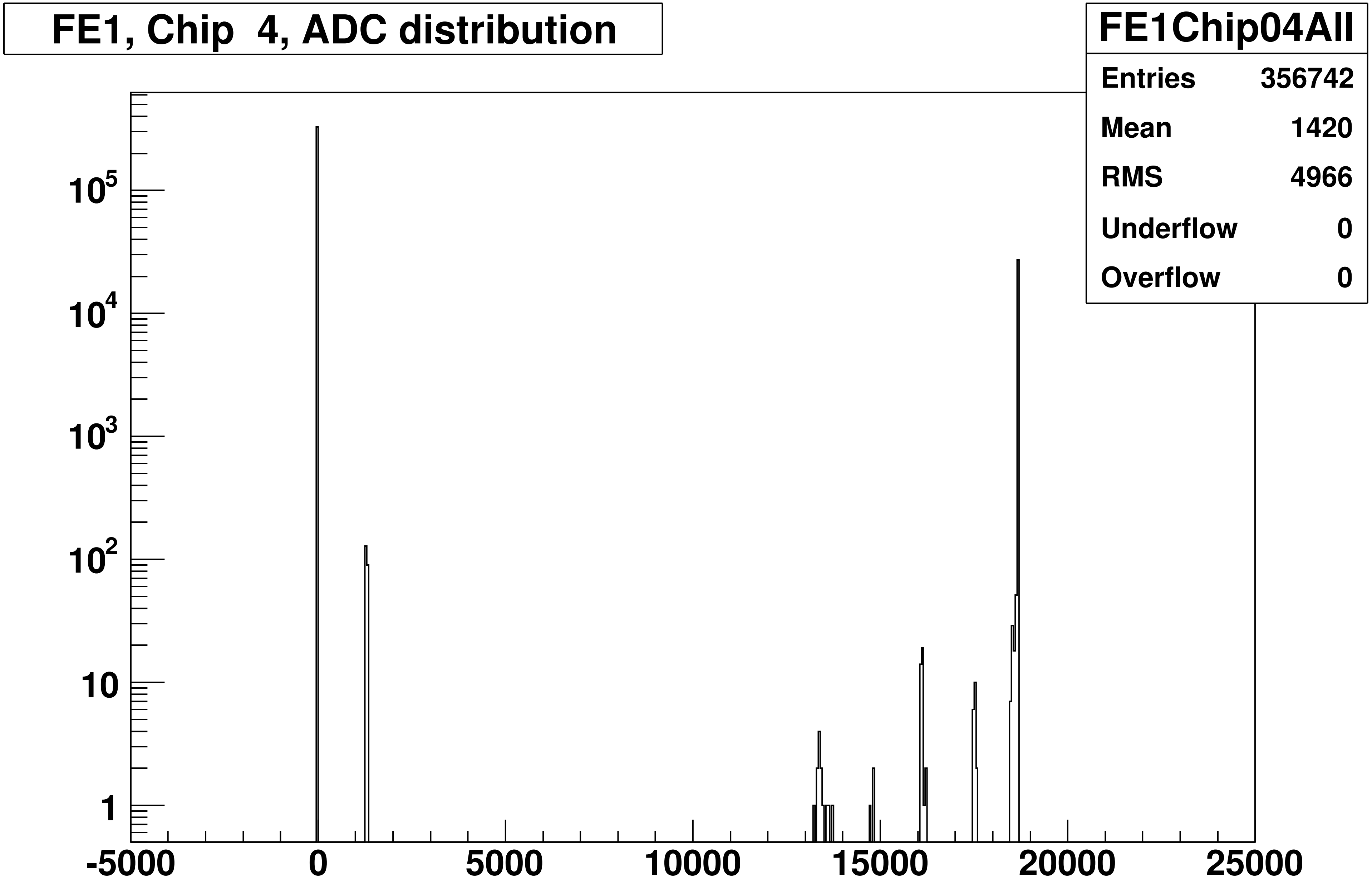
19400
19600
19800
20000


FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 356742
Mean 1420
RMS 4966
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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0
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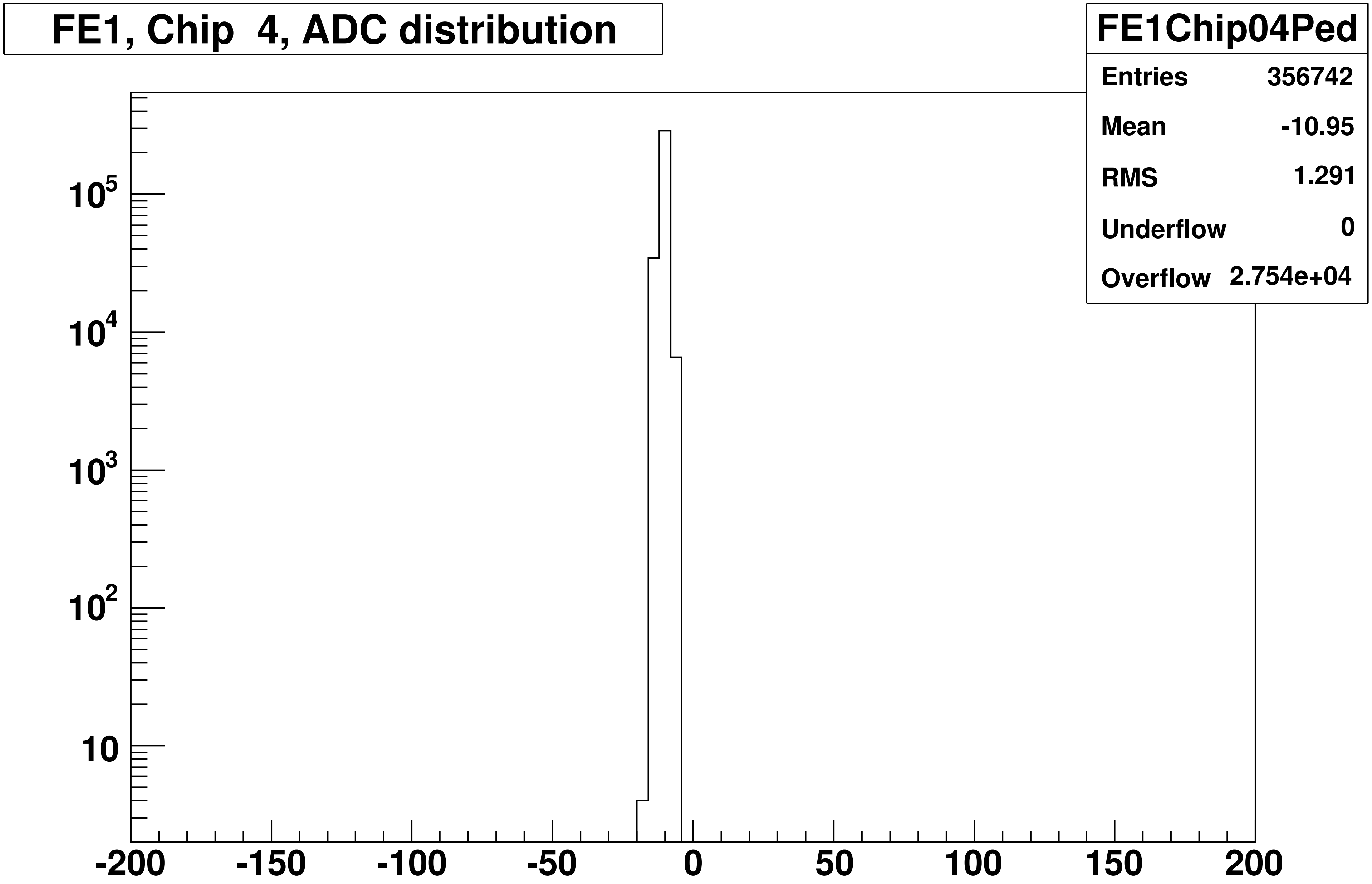
10000
15000
20000
25000



FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 356742
Mean -10.95
RMS 1.291
Underflow 0
Overflow 2.754e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
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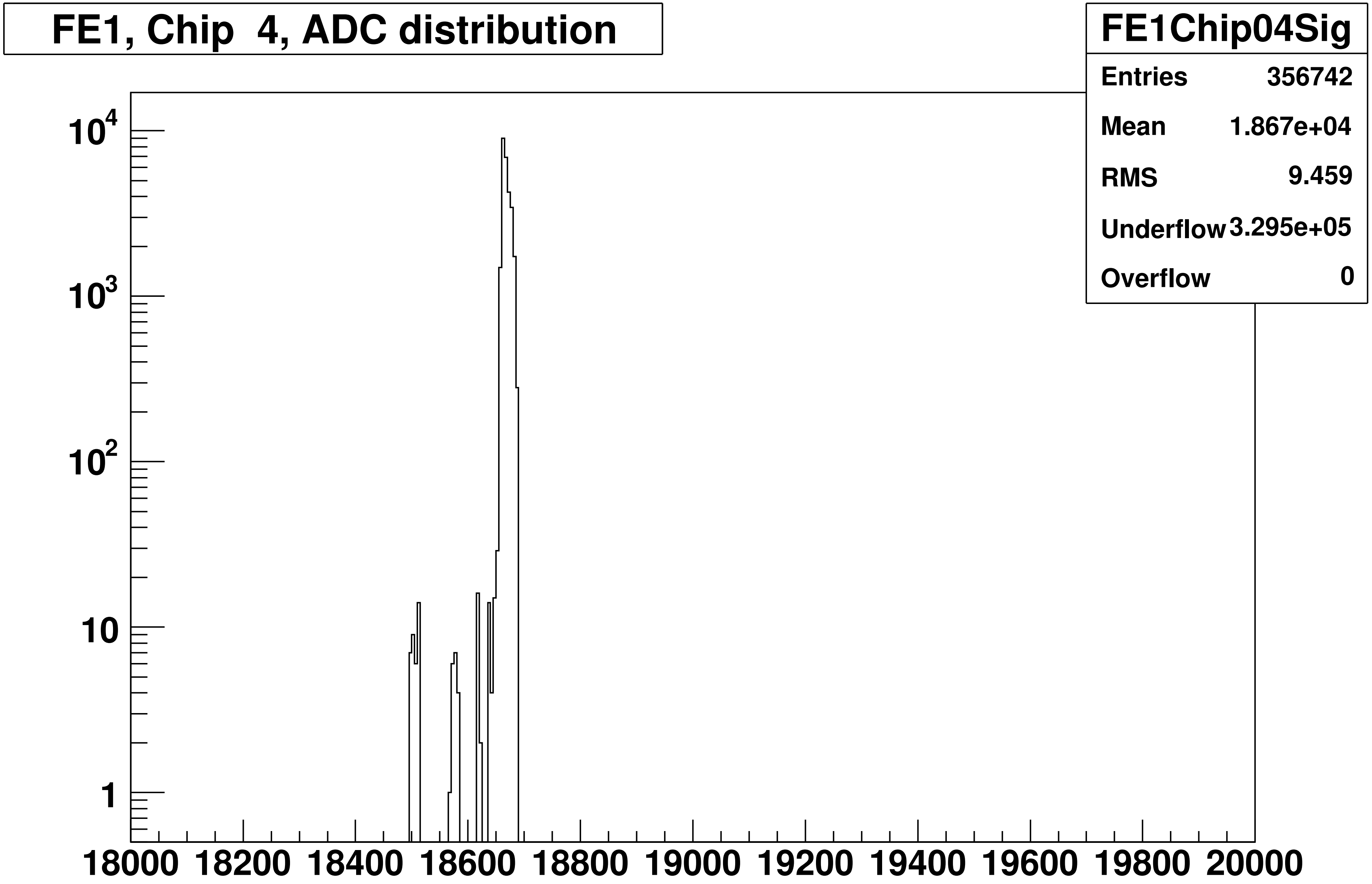
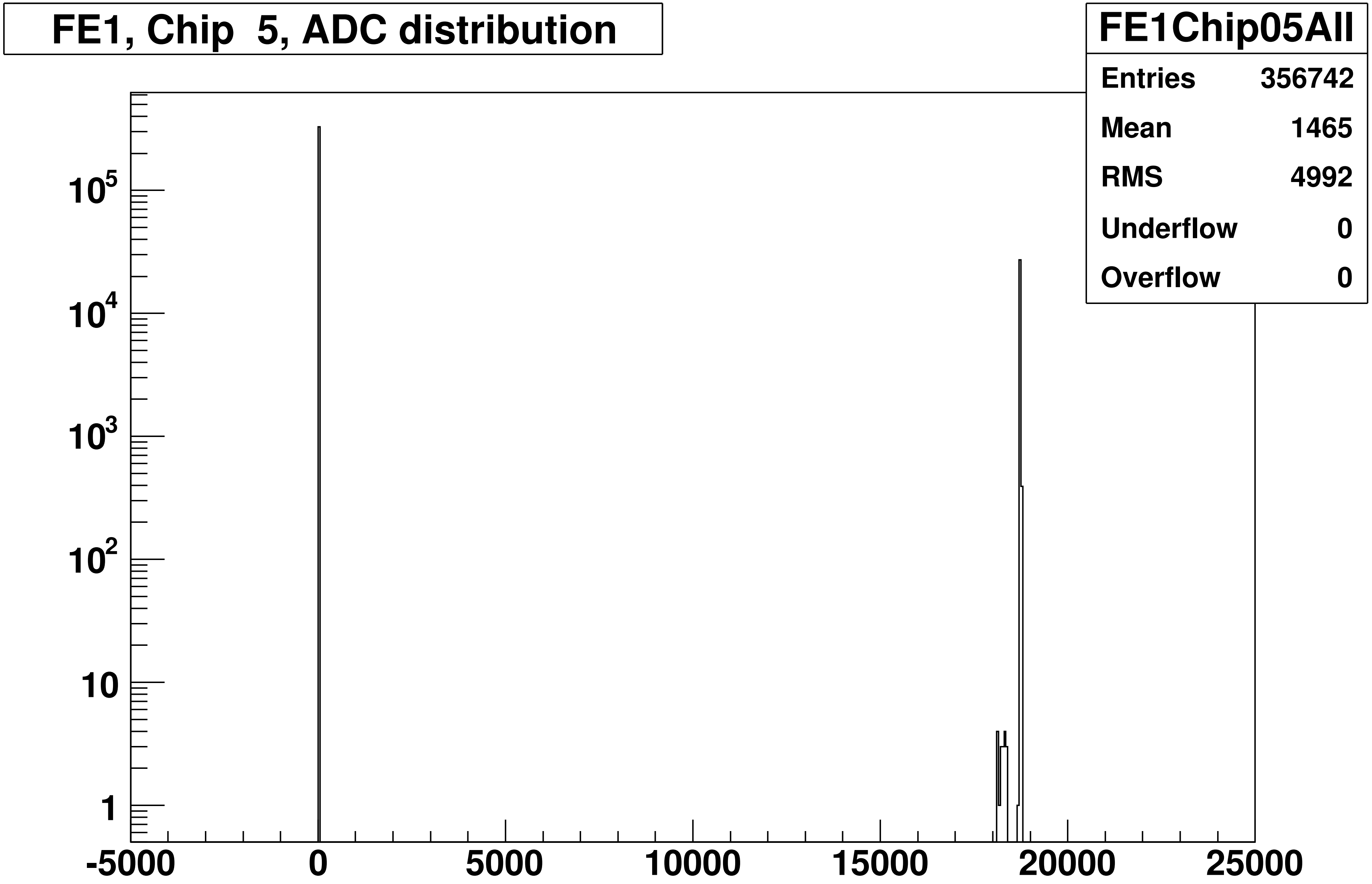
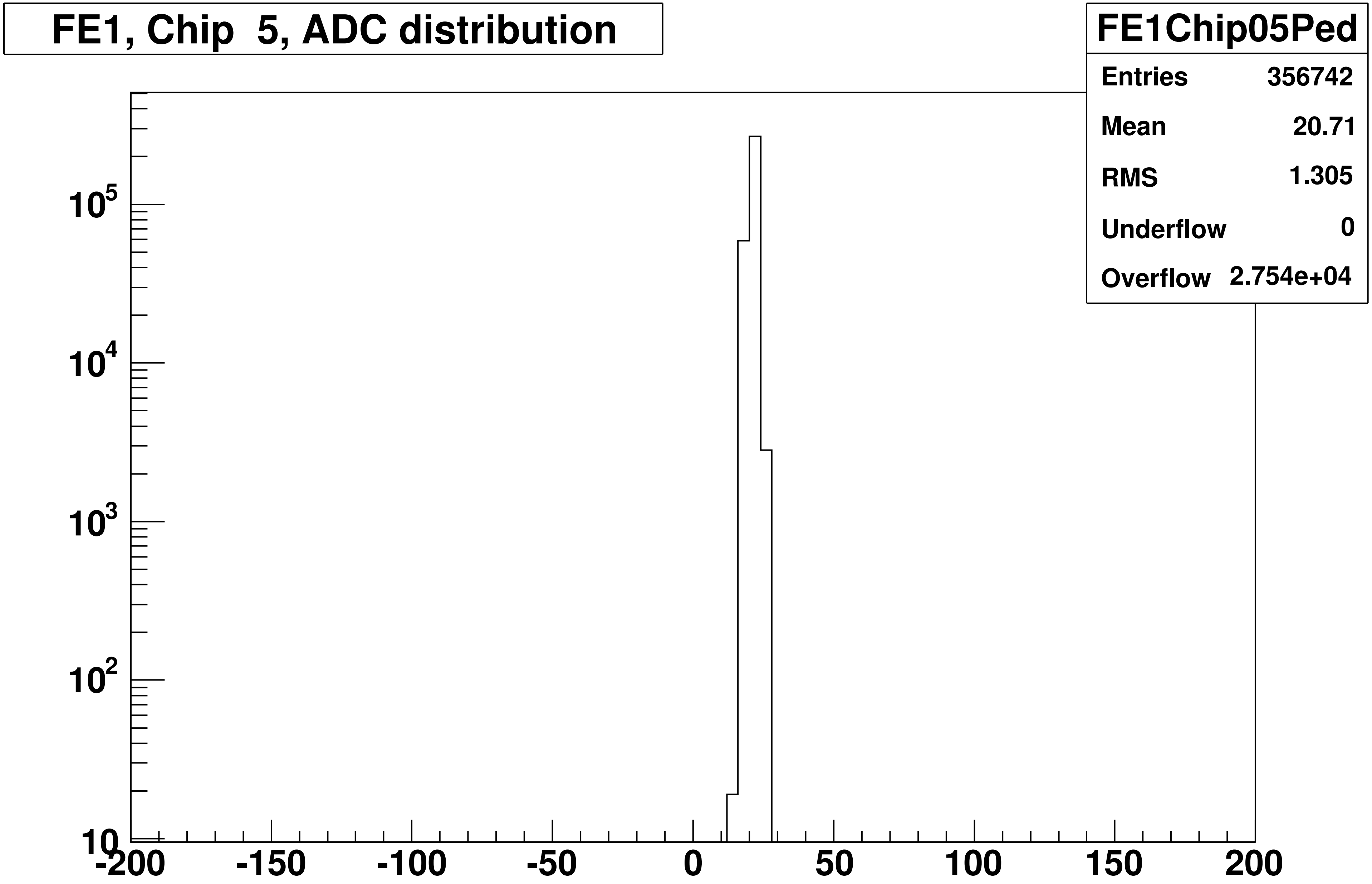
100
150
200


FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 356742
Mean 1.867e+04
RMS 9.459
Underflow 3.295e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 356742
Mean 1465
RMS 4992
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 356742
Mean 20.71
RMS 1.305
Underflow 0
Overflow 2.754e+04
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10^4
10^3
10^2
10
-200
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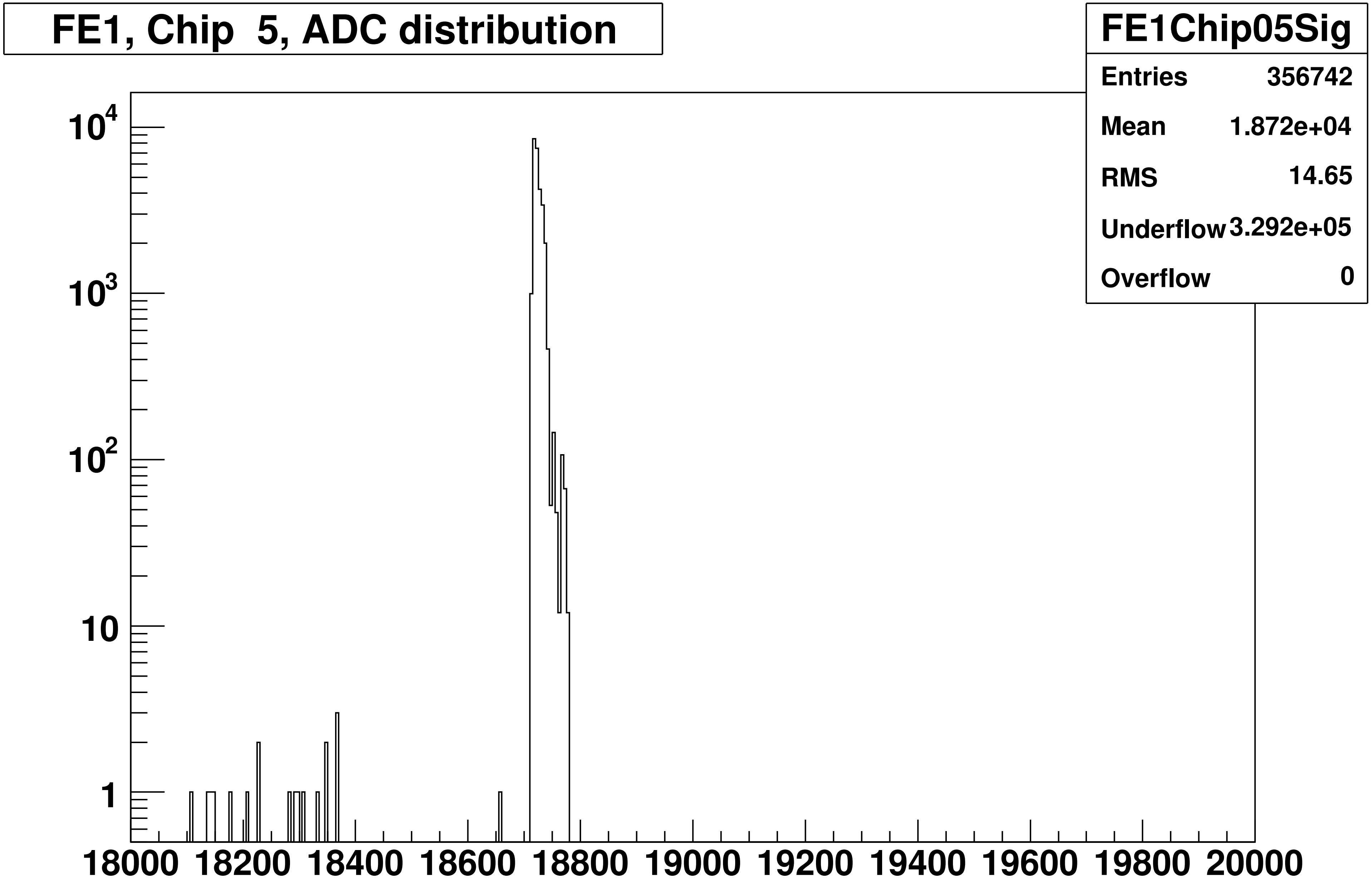
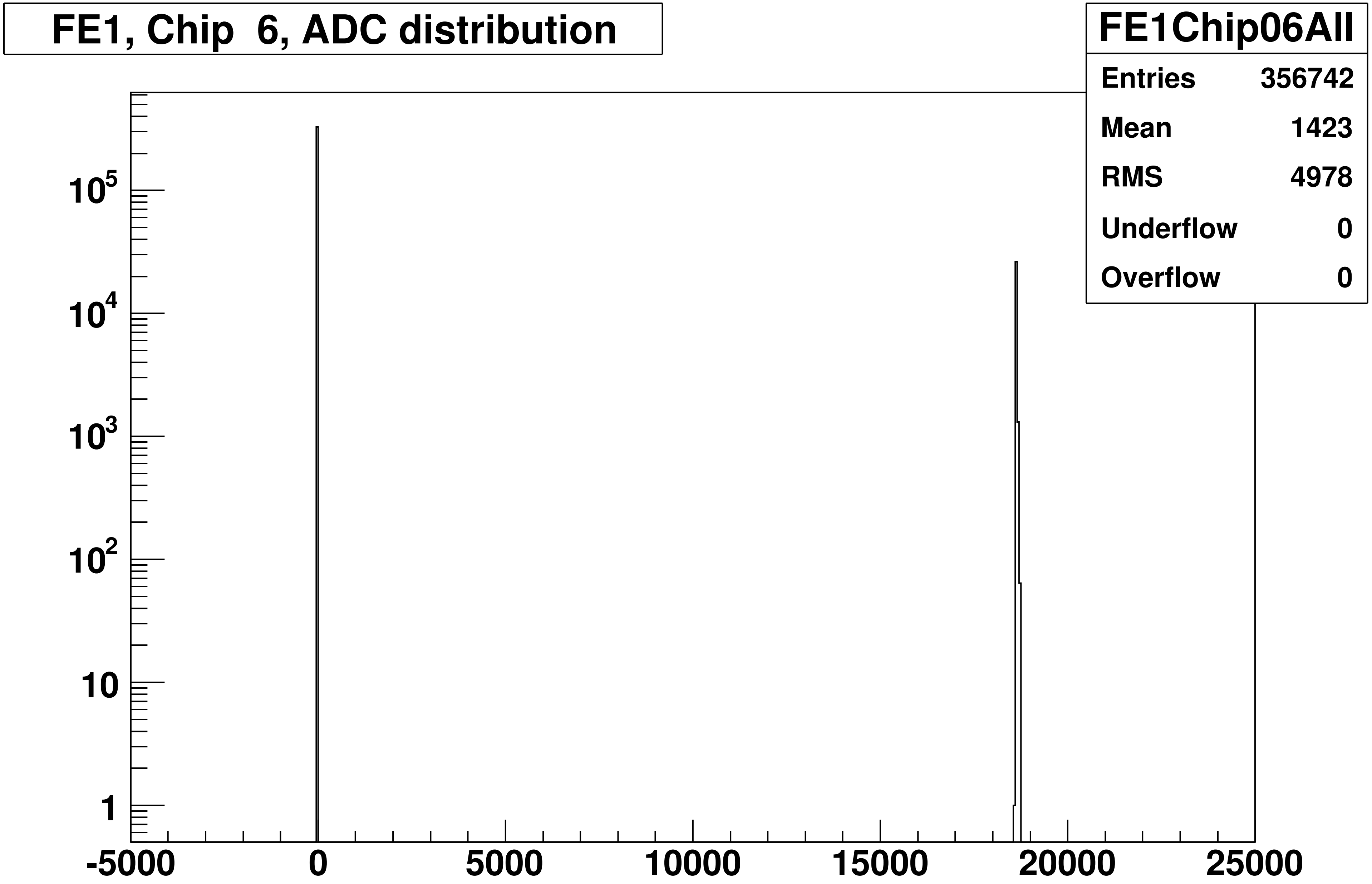

FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 356742
Mean 1.872e+04
RMS 14.65
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 356742
Mean 1423
RMS 4978
Underflow 0
Overflow 0
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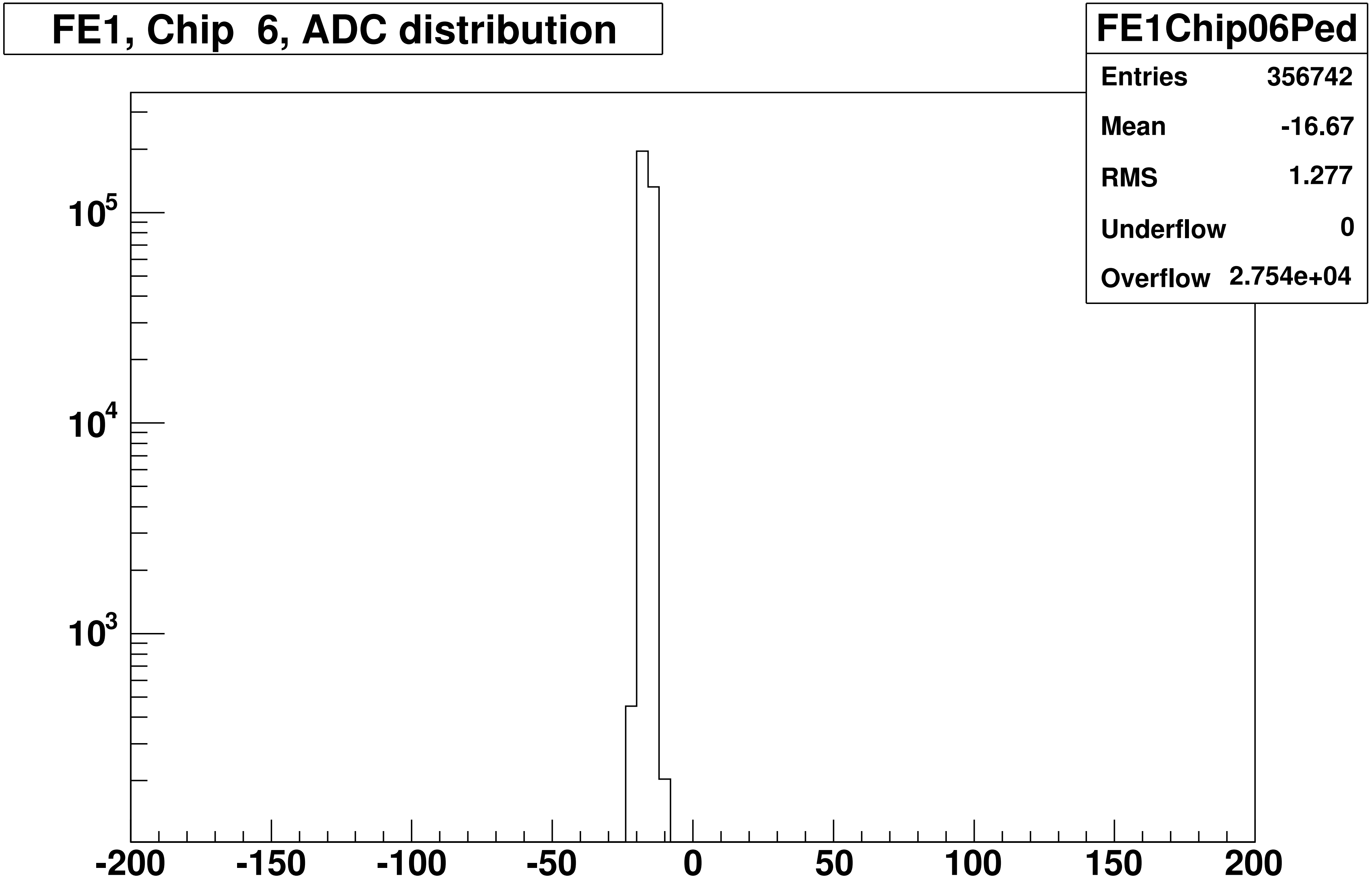
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 356742
Mean -16.67
RMS 1.277
Underflow 0
Overflow 2.754e+04
10^5
10^4
10^3
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-100
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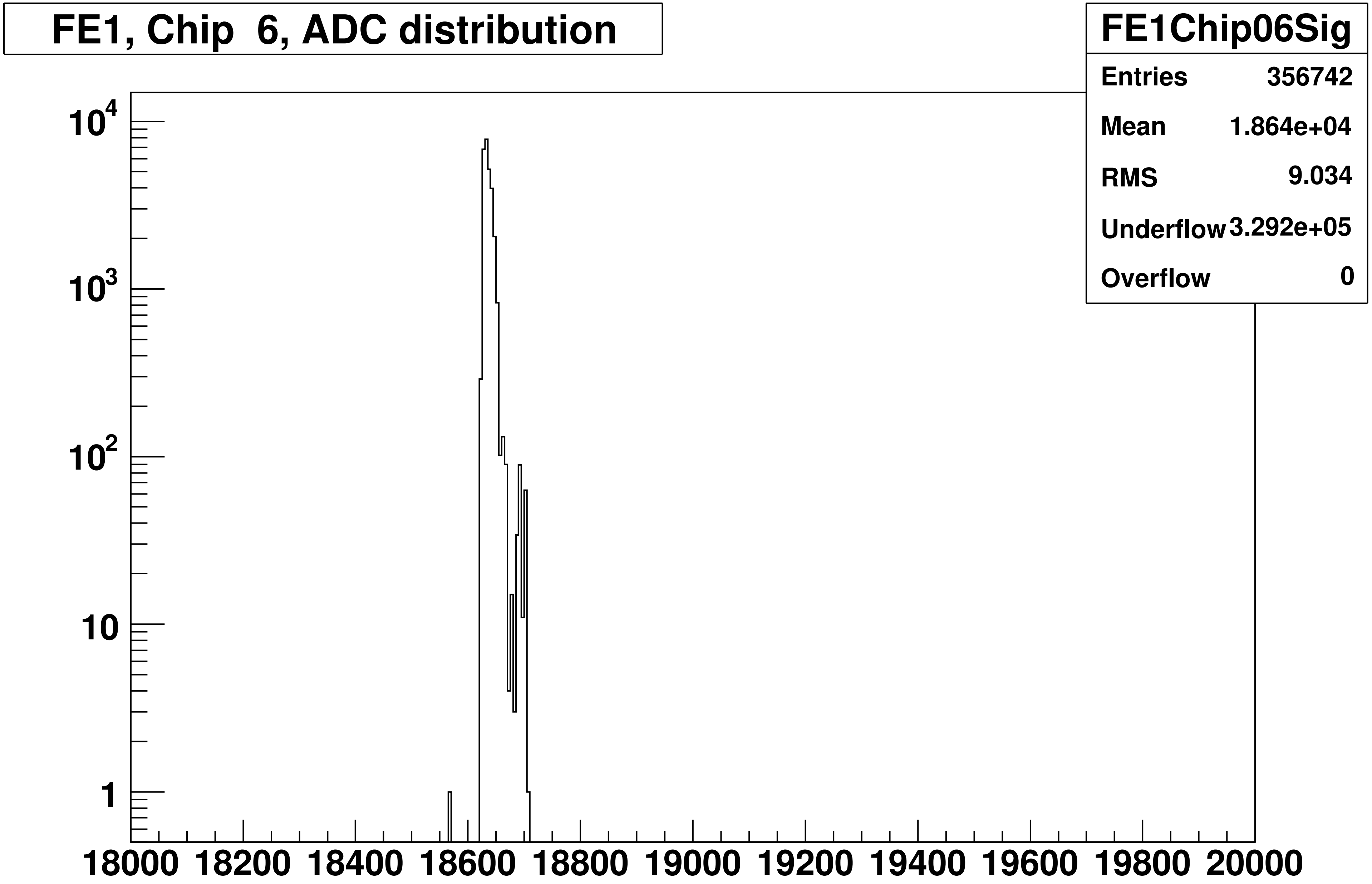
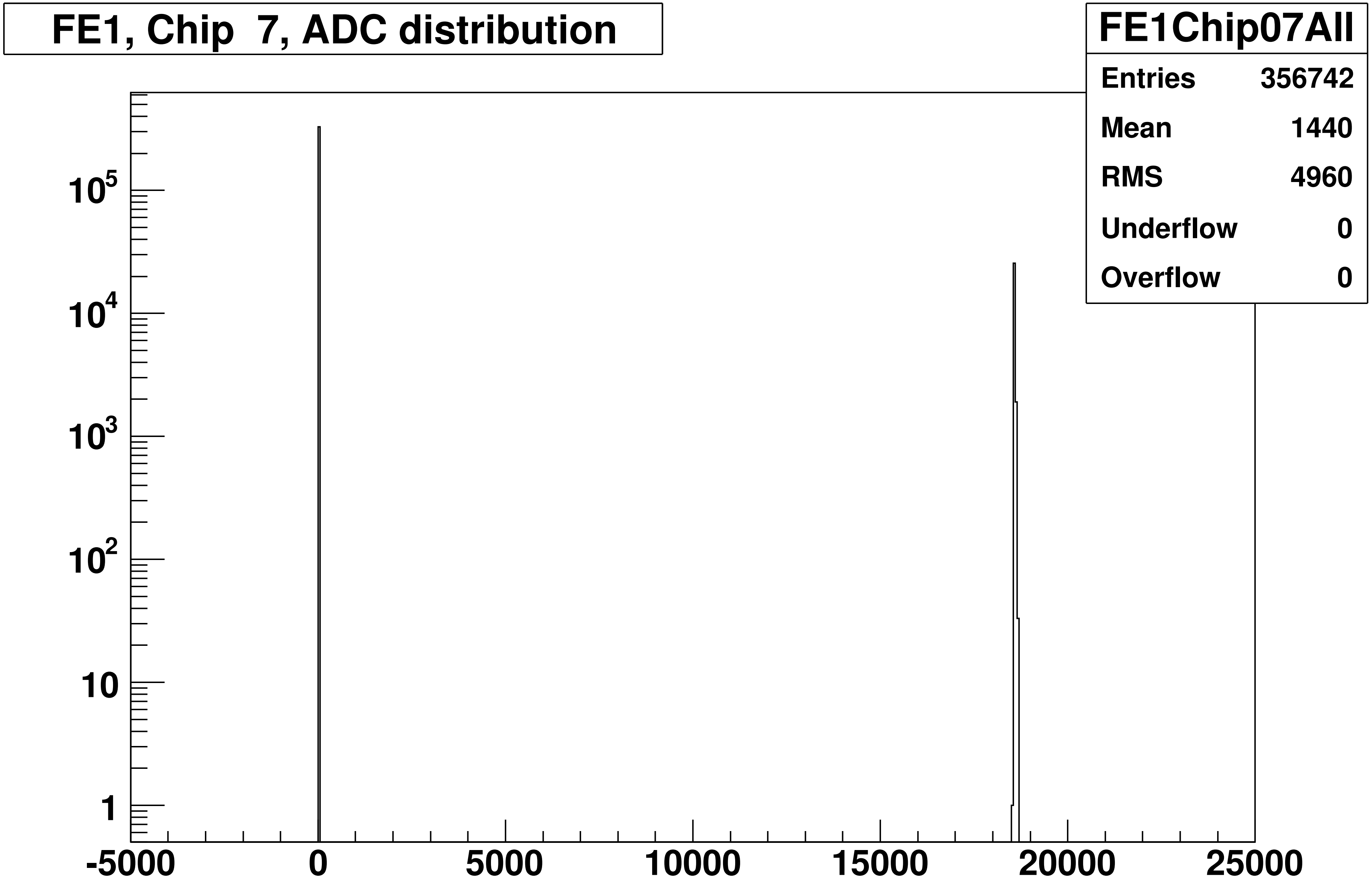
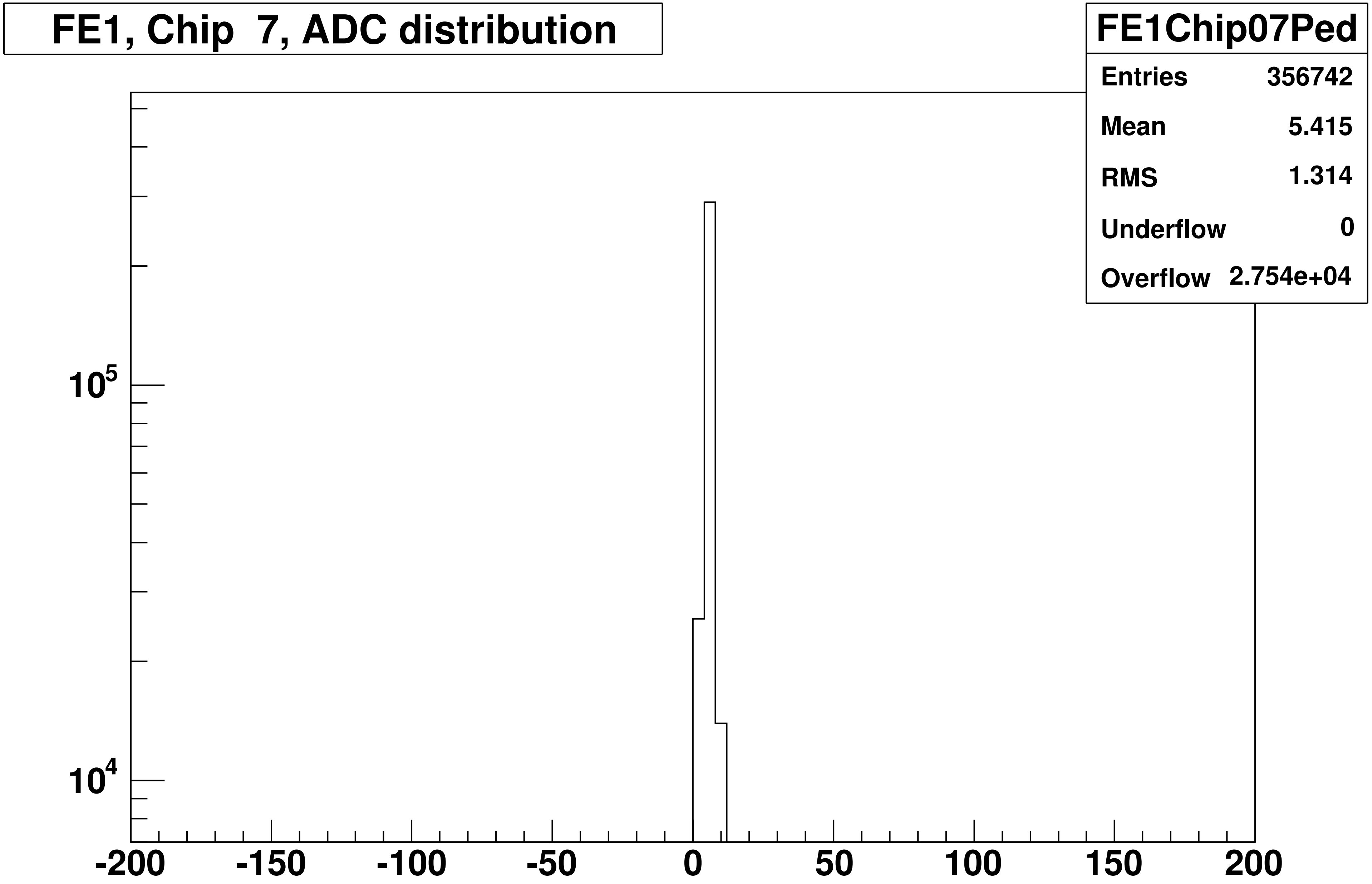
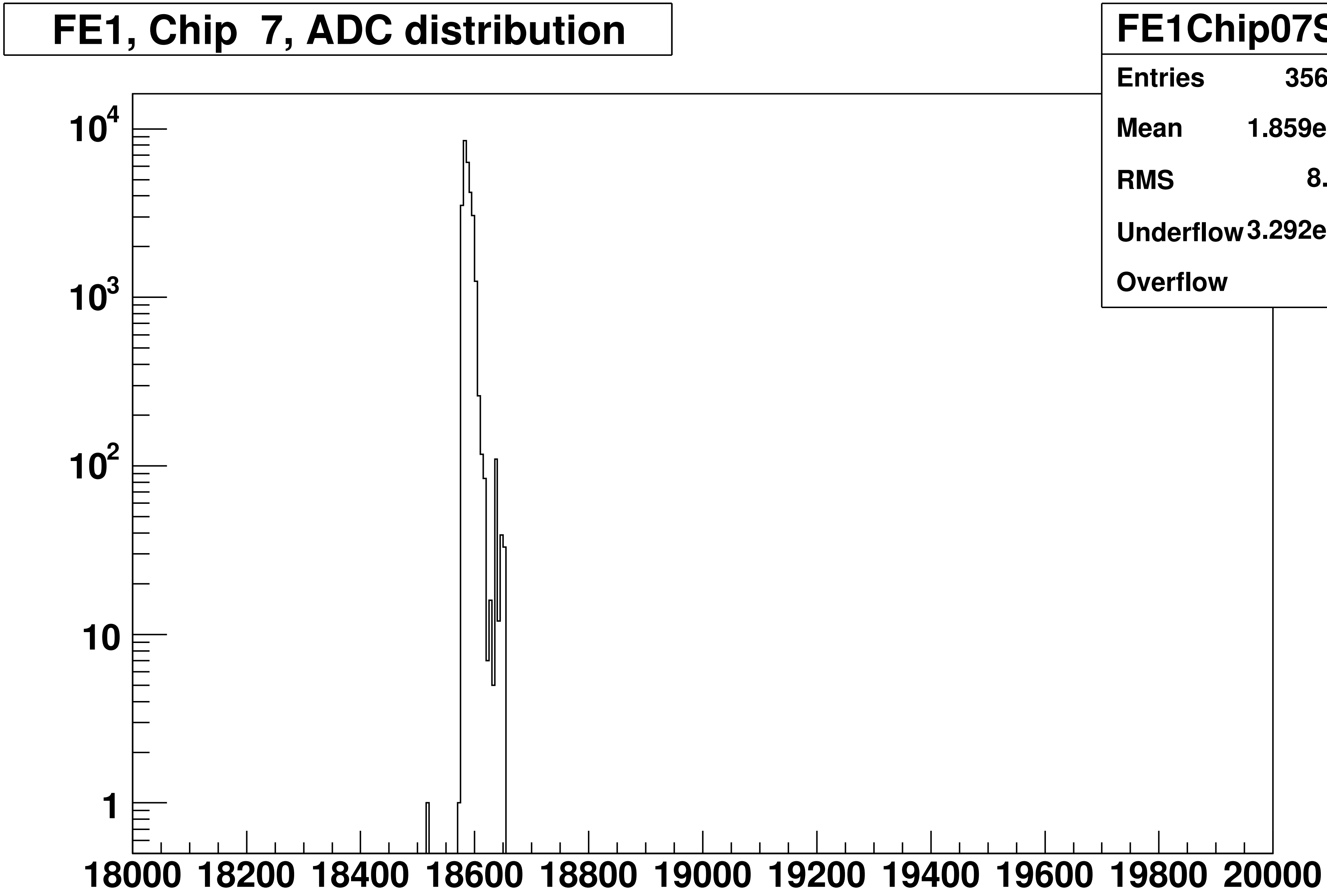
100
150
200

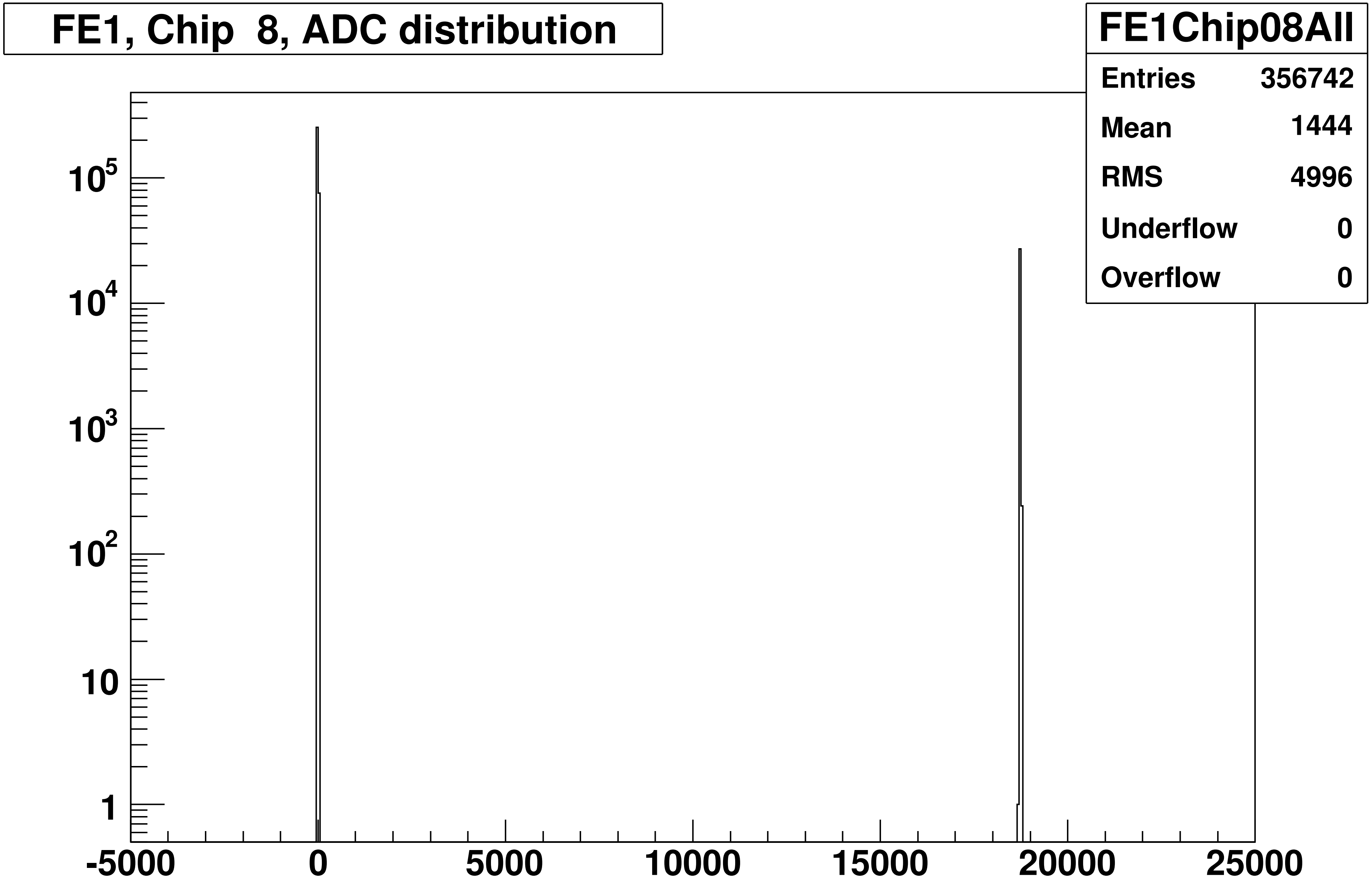

FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 356742
Mean 1.864e+04
RMS 9.034
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



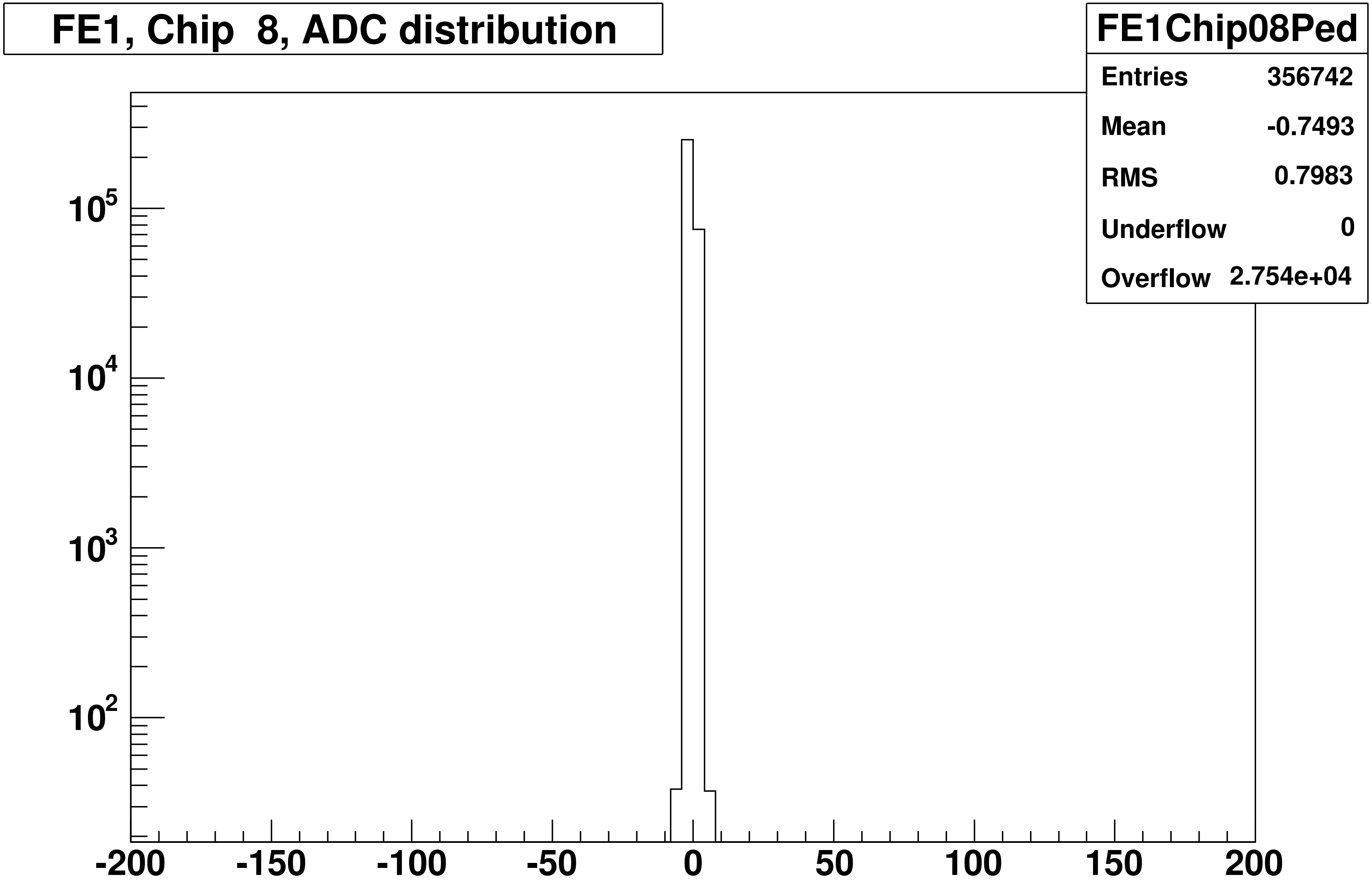
FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 356742
Mean 1440
RMS 4960
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 356742
Mean 5.415
RMS 1.314
Underflow 0
Overflow 2.754e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 356742
Mean 1.859e+04
RMS 8.659
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 356742
Mean 1444
RMS 4996
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 356742
Mean -0.7493
RMS 0.7983
Underflow 0
Overflow 2.754e+04
10^5
10^4
10^3
10^2
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-150
-100
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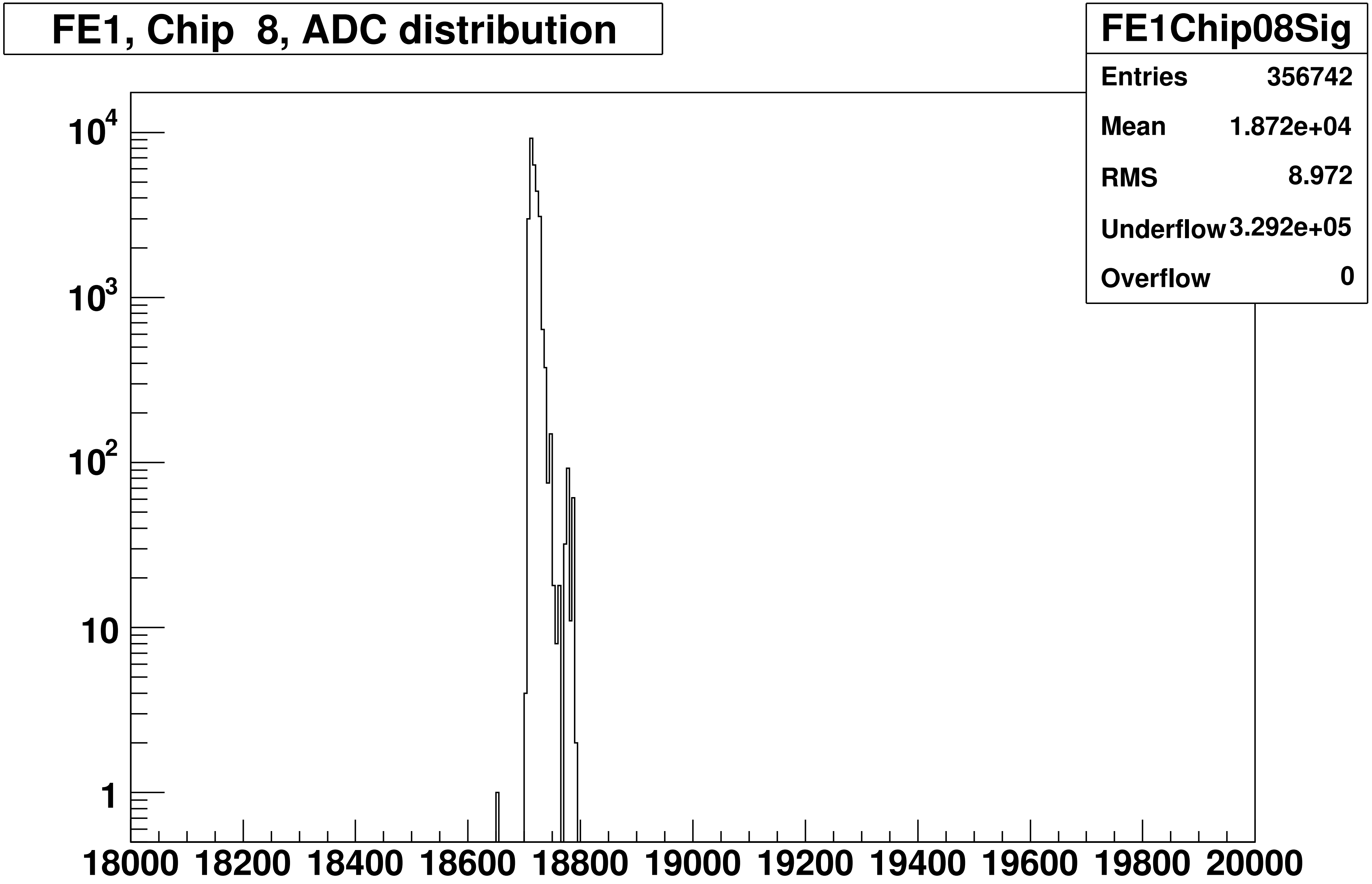
100
150
200


FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 356742
Mean 1.872e+04
RMS 8.972
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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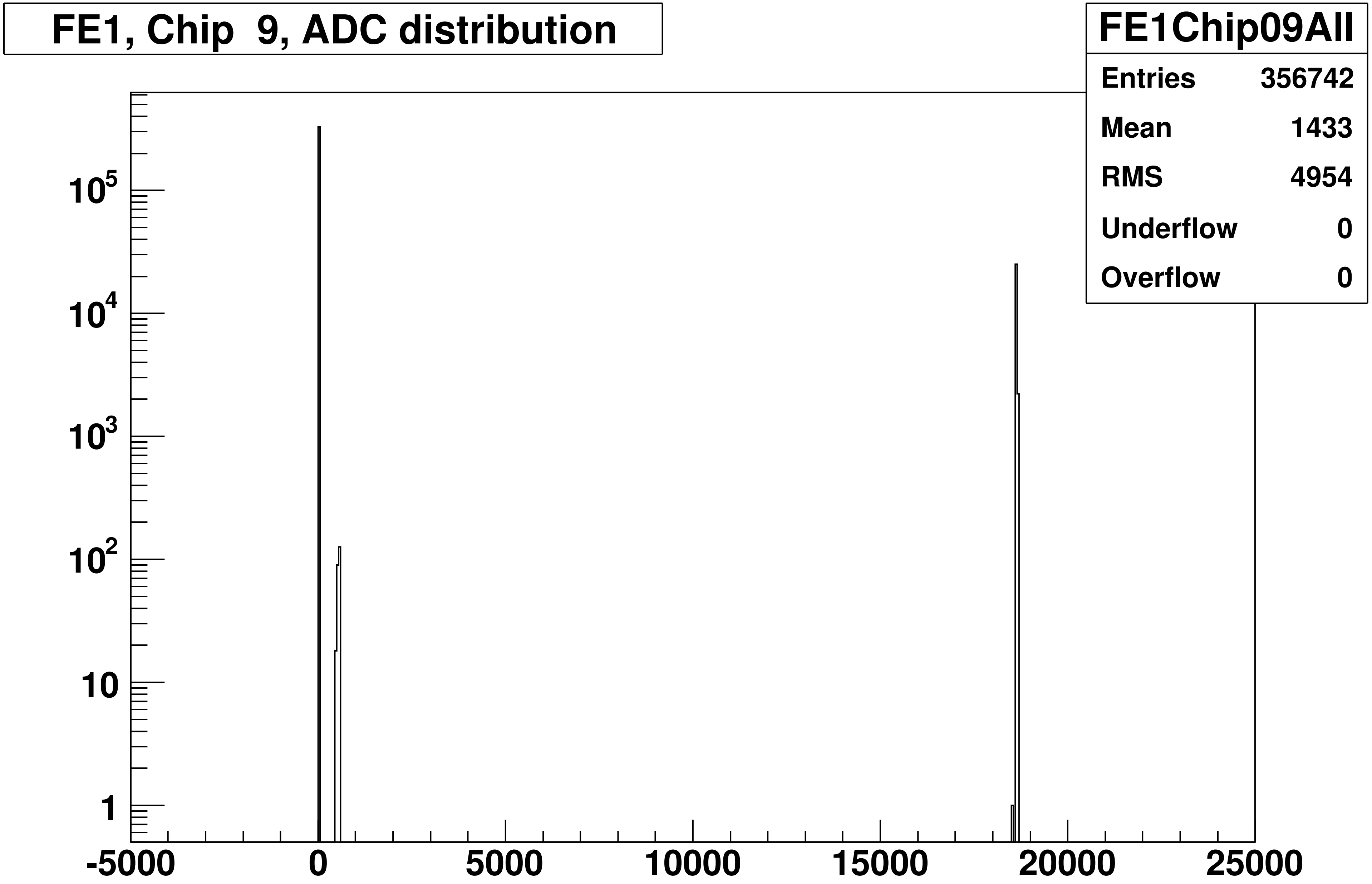
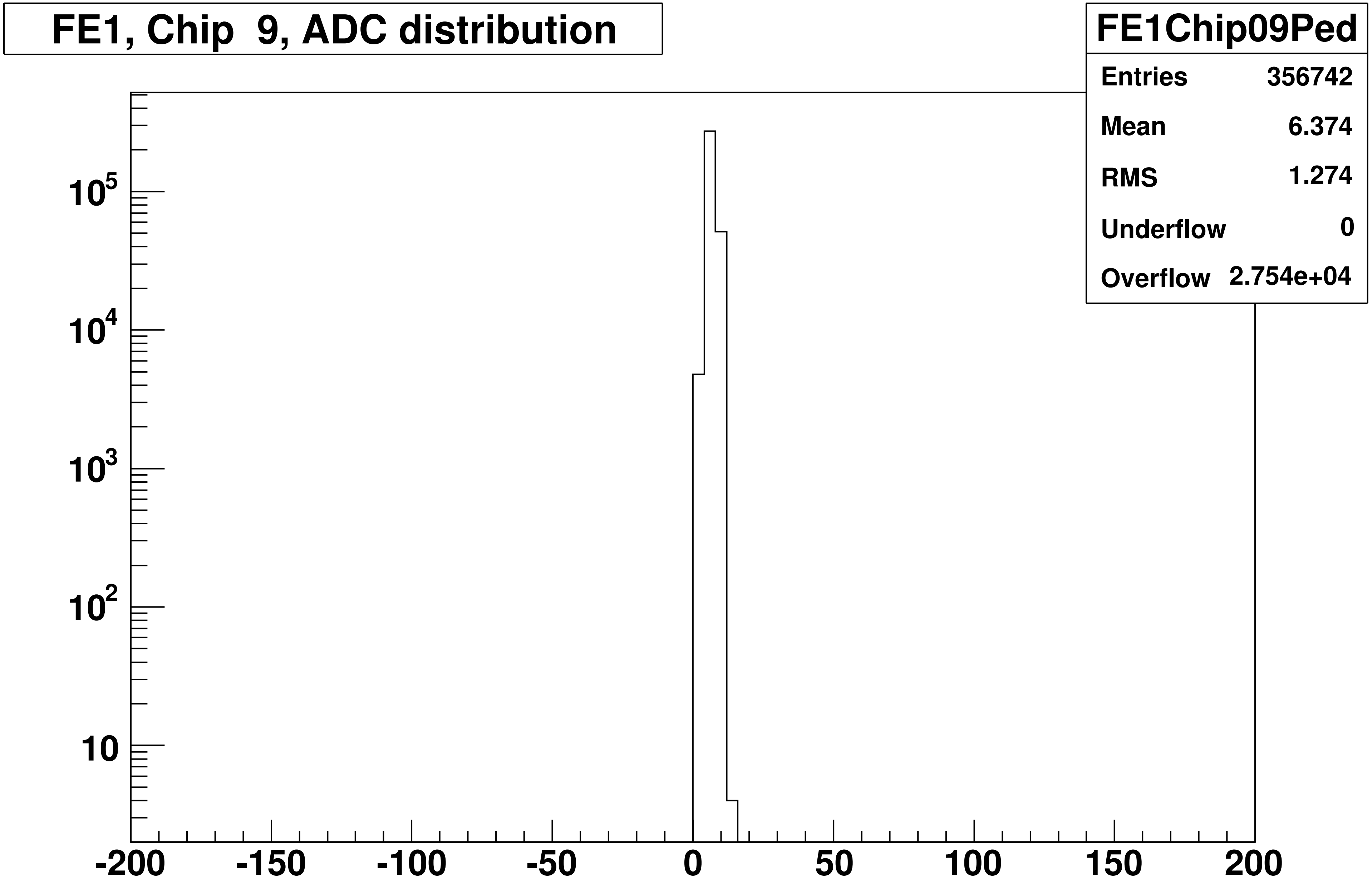
19400
19600
19800
20000



FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 356742
Mean 1433
RMS 4954
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 356742
Mean 6.374
RMS 1.274
Underflow 0
Overflow 2.754e+04
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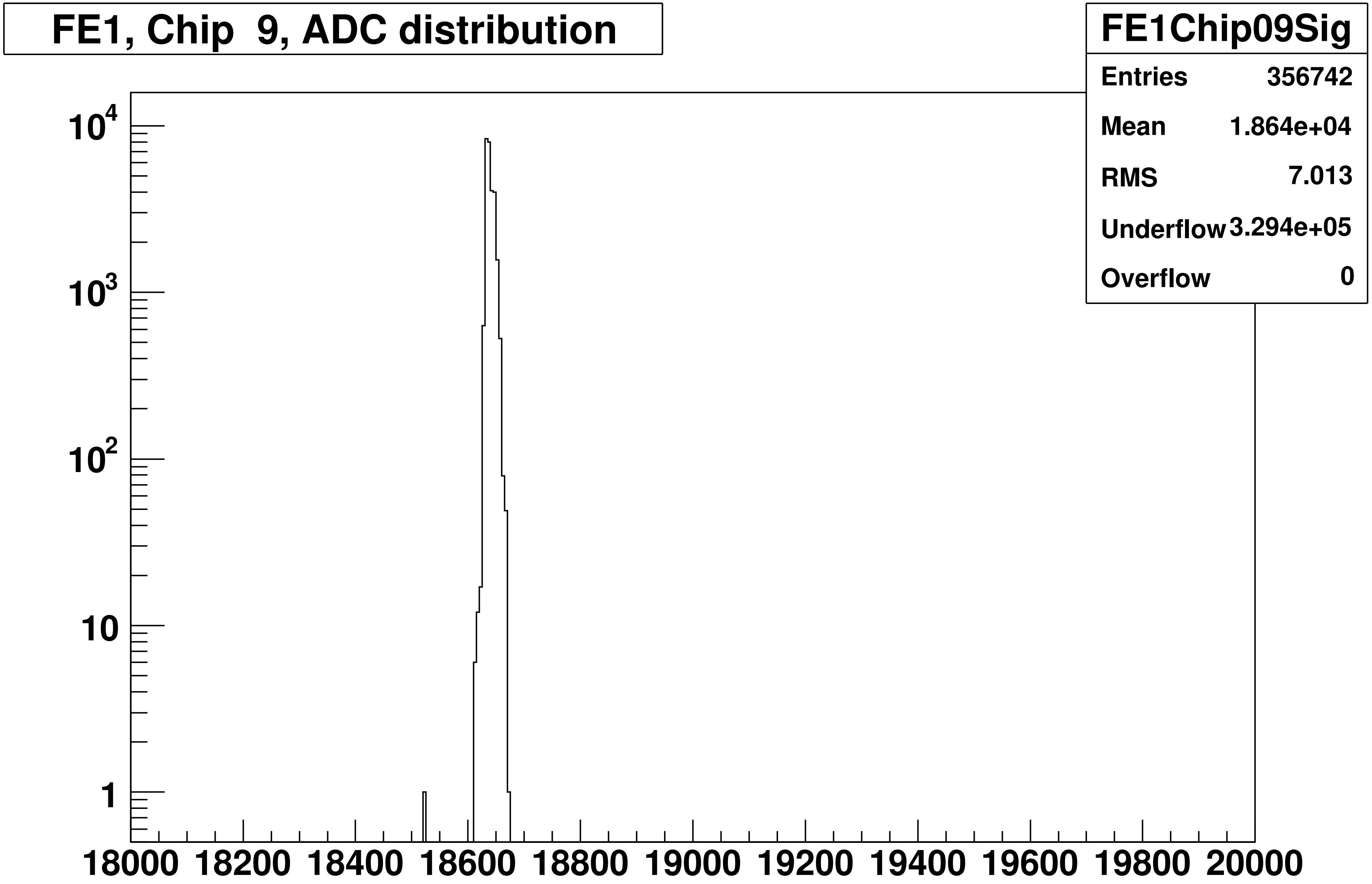
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200



FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 356742
Mean 1.864e+04
RMS 7.013
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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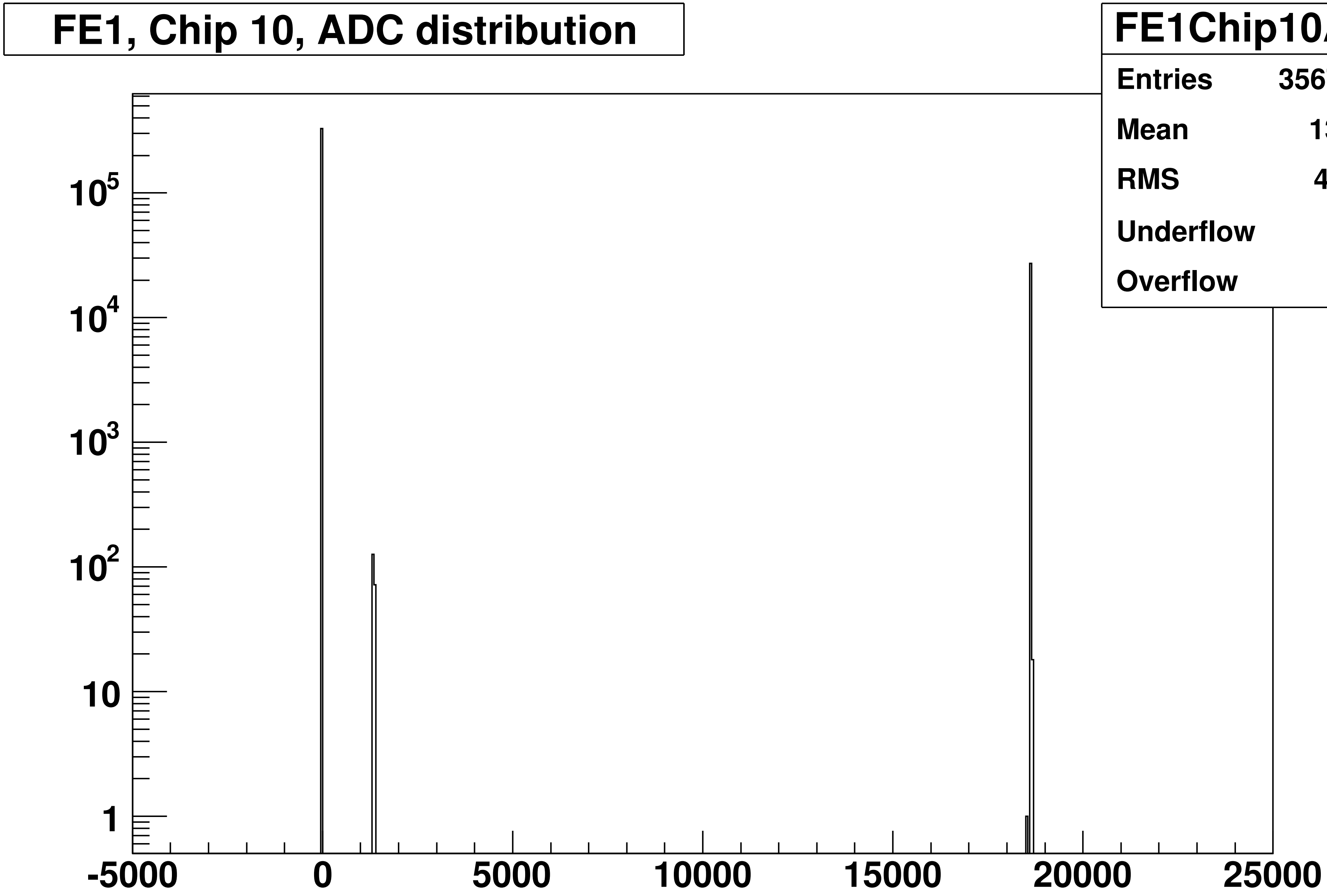
19600
19800
20000



FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 356742
Mean 1393
RMS 4961
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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0
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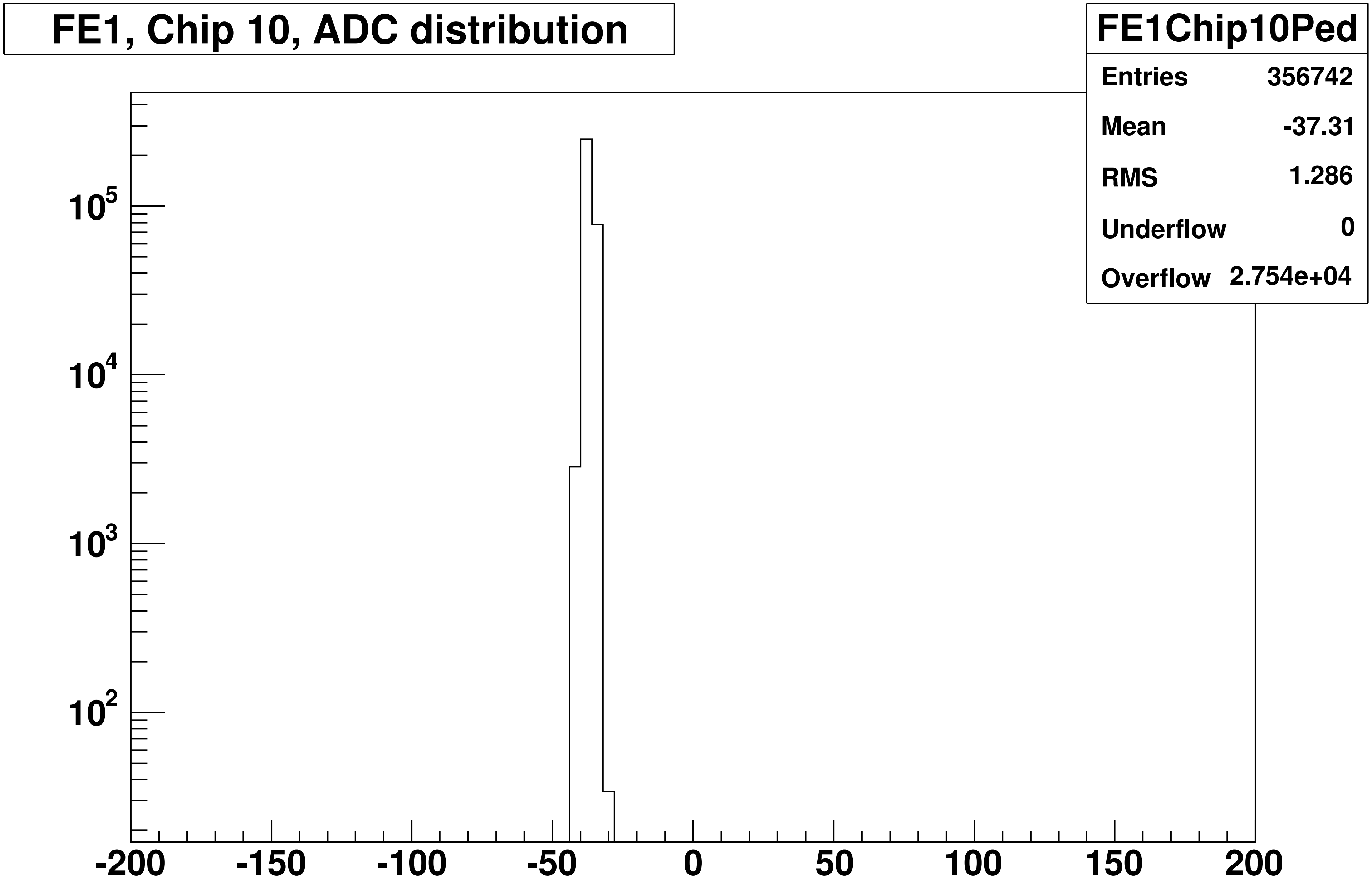
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 356742
Mean -37.31
RMS 1.286
Underflow 0
Overflow 2.754e+04
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10^4
10^3
10^2
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-100
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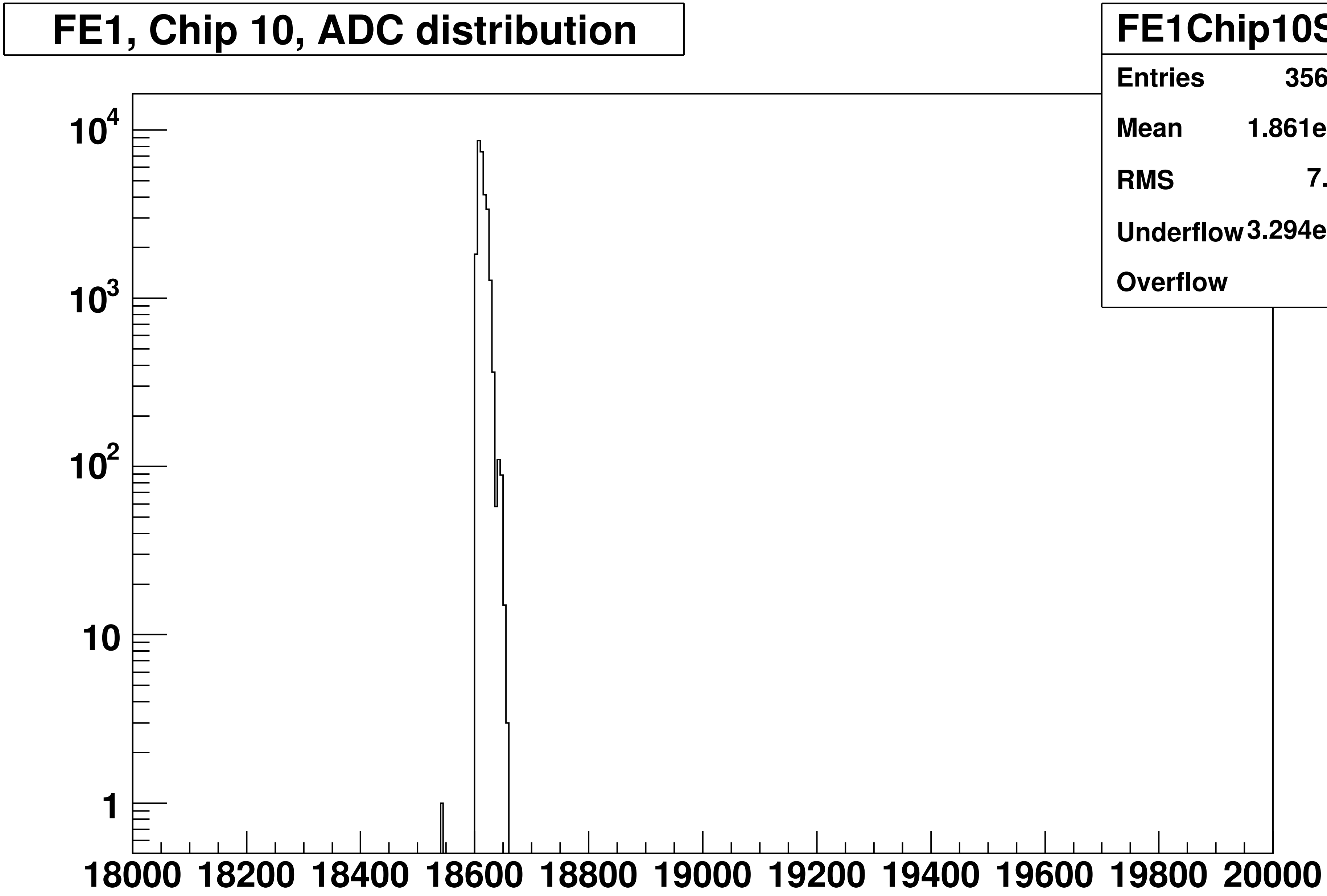
150
200


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 356742
Mean 1.861e+04
RMS 7.366
Underflow 3.294e+05
Overflow 0
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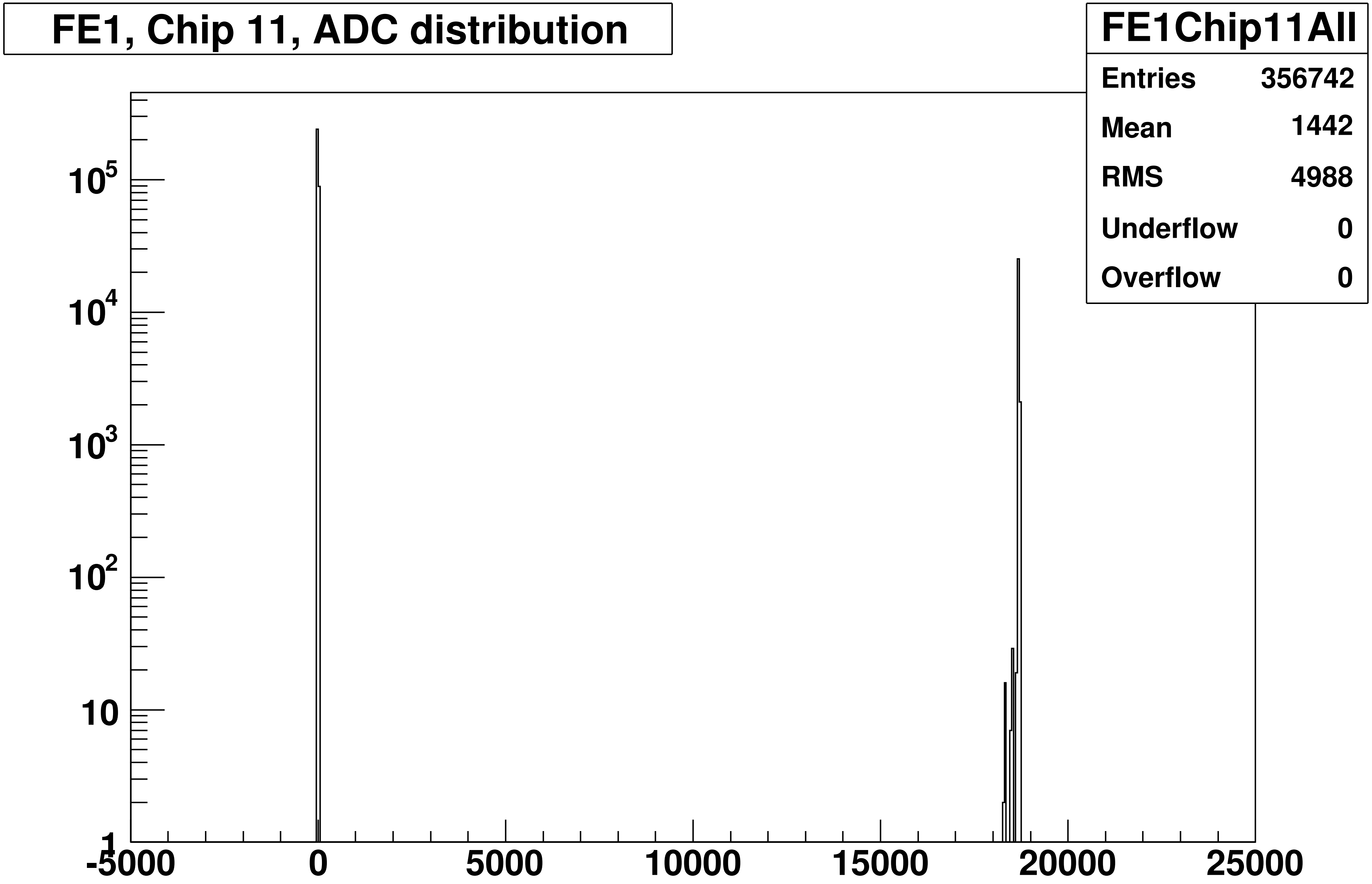
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 356742
Mean 1442
RMS 4988
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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0
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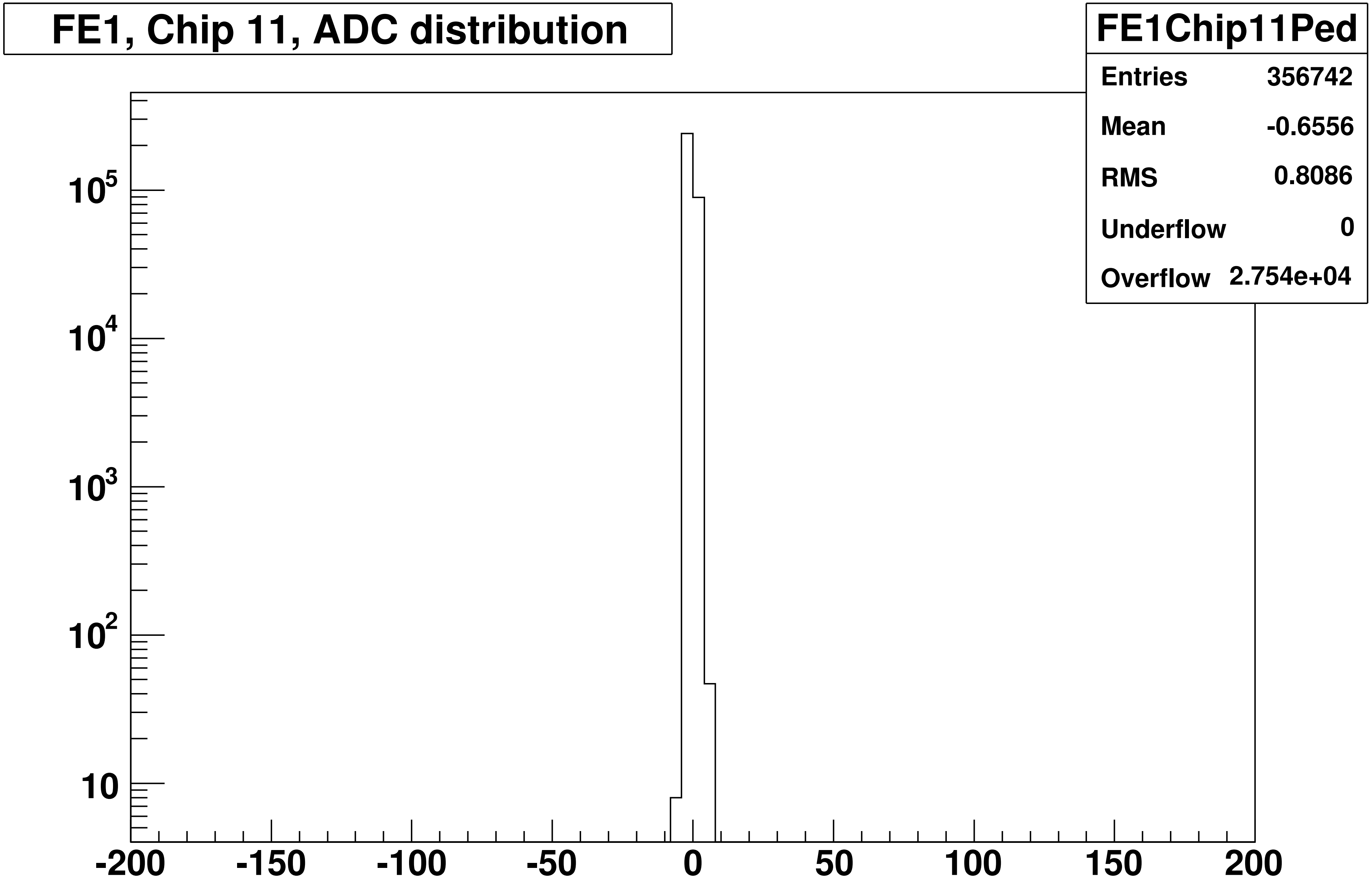
10000
15000
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 356742
Mean -0.6556
RMS 0.8086
Underflow 0
Overflow 2.754e+04
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10^2
10^3
10^4
10^5
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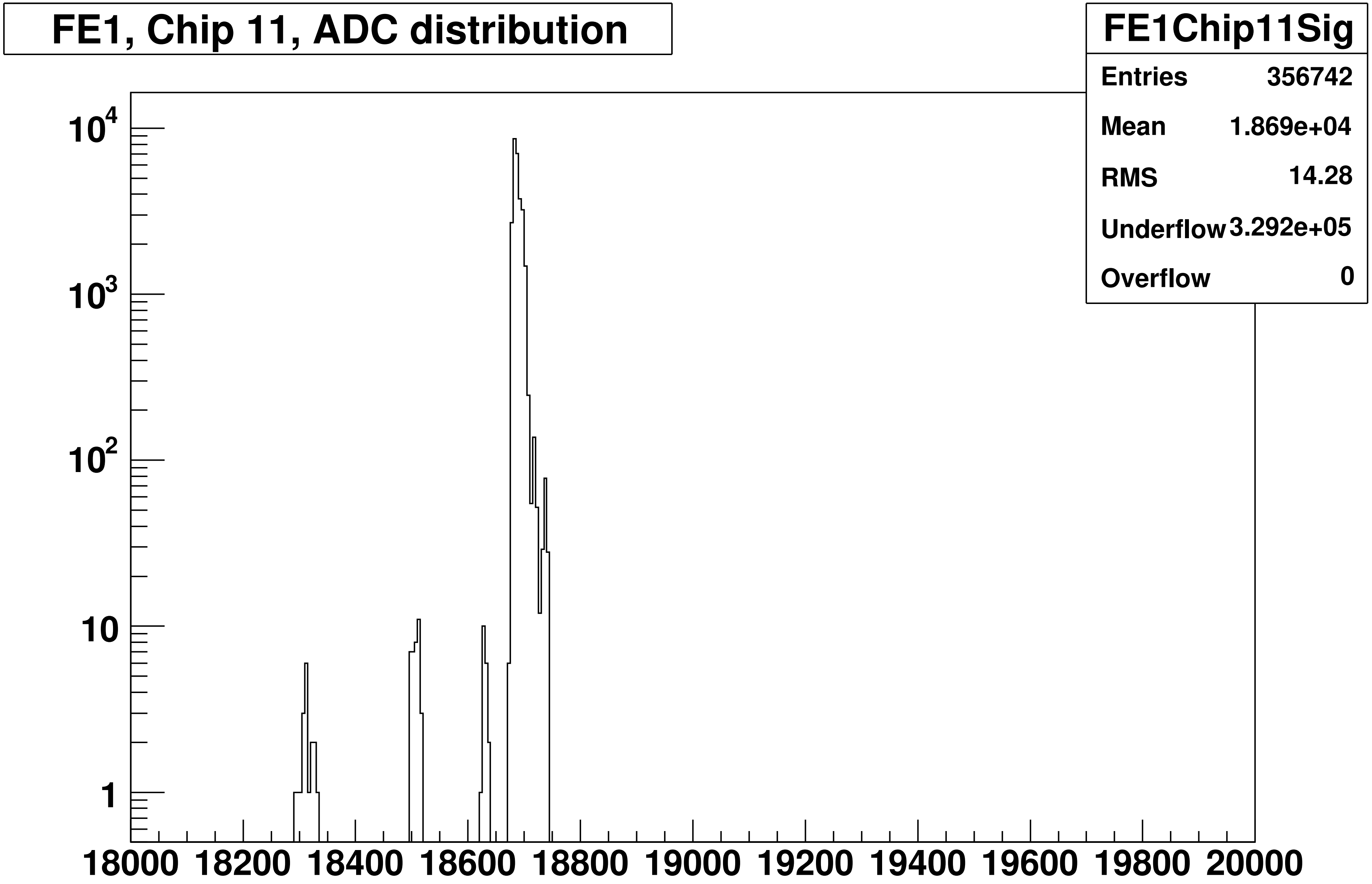
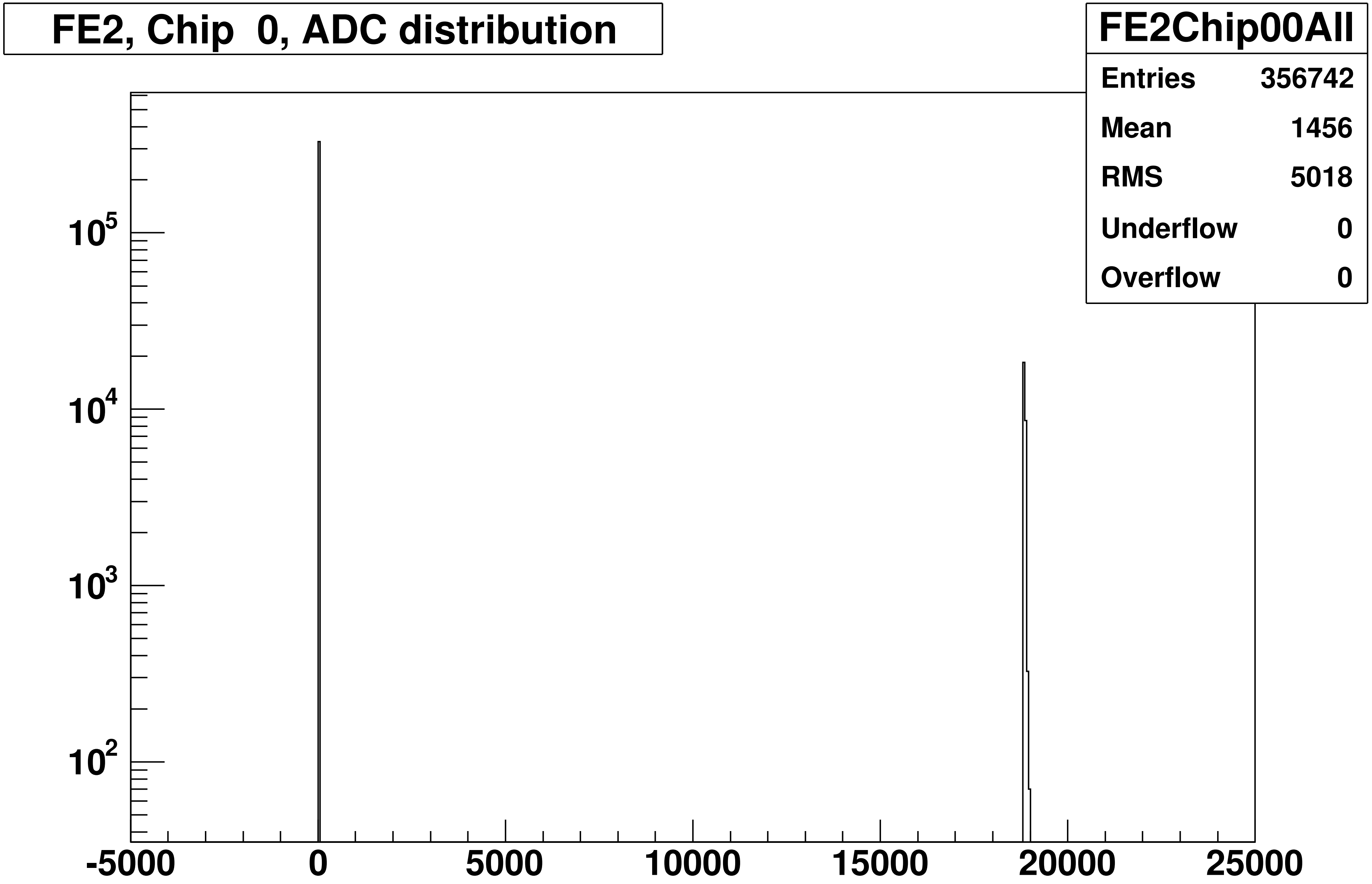
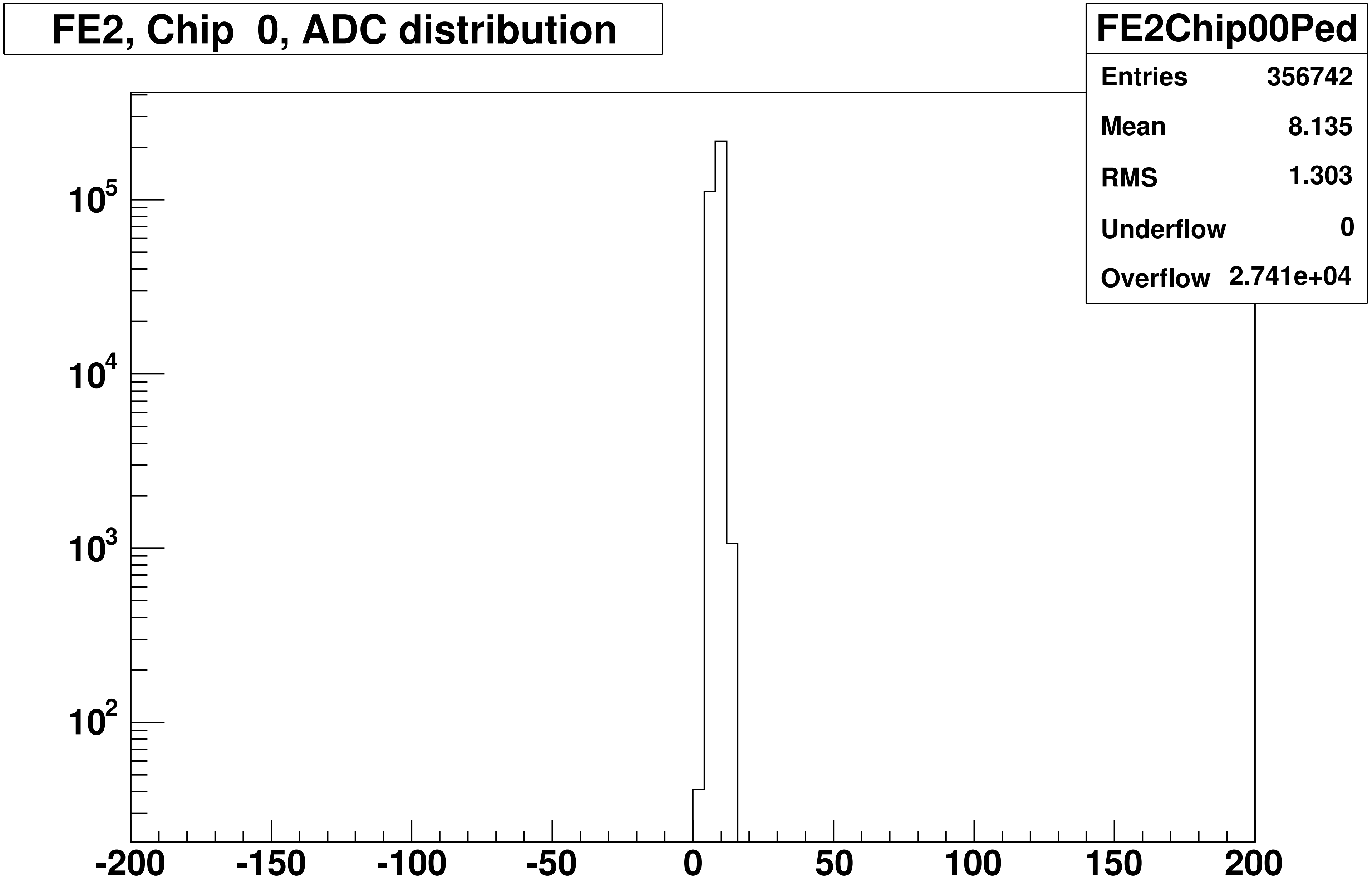
-150
-100
-50
0
50
100
150
200



FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 356742
Mean 1.869e+04
RMS 14.28
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 356742
Mean 1456
RMS 5018
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 356742
Mean 8.135
RMS 1.303
Underflow 0
Overflow 2.741e+04
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10^4
10^3
10^2
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-100
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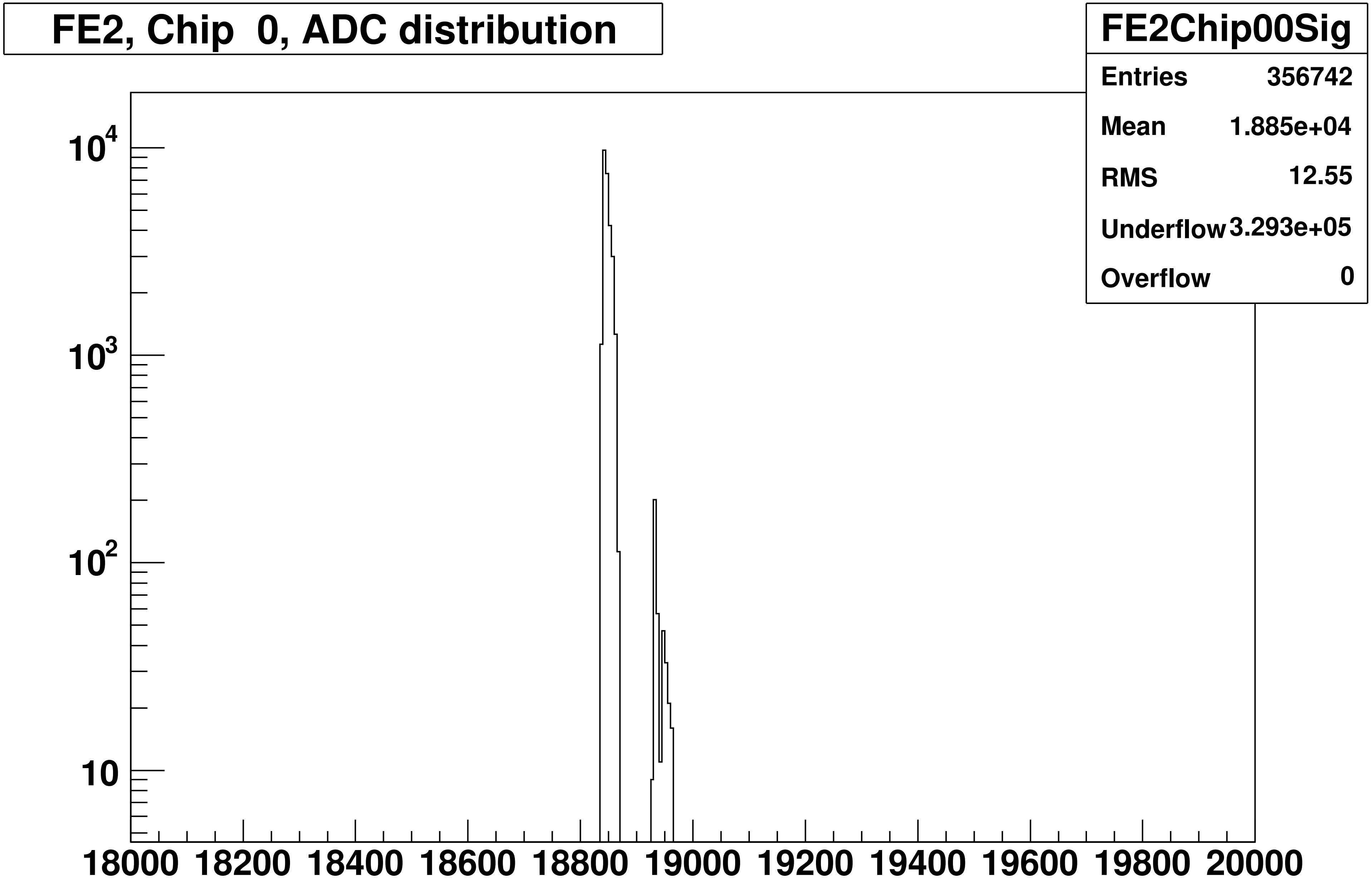
0
50
100
150
200


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 356742
Mean 1.885e+04
RMS 12.55
Underflow 3.293e+05
Overflow 0
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10^2
10^3
10^4
18000
18200
18400
18600
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19000
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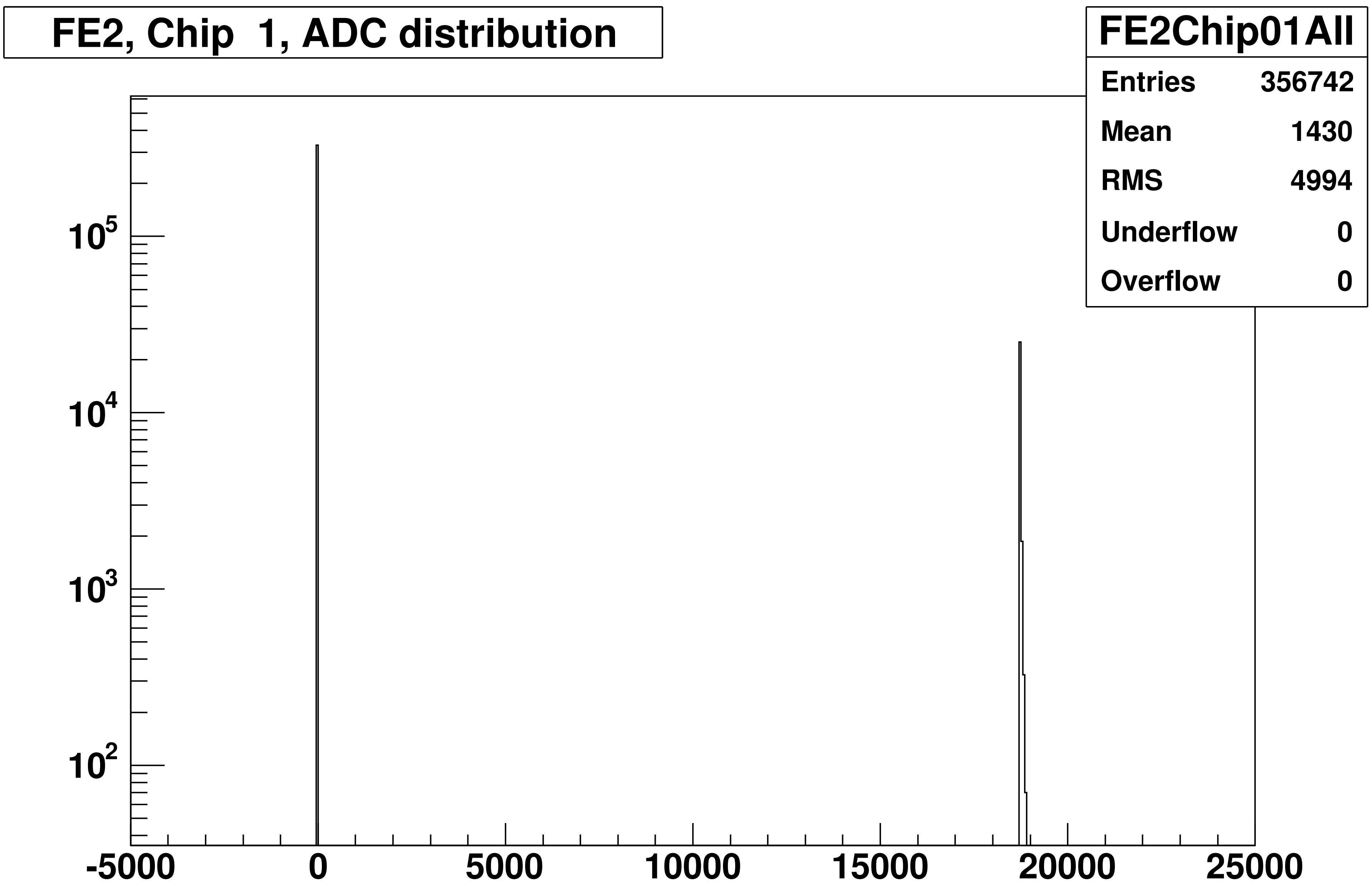
19600
19800
20000


FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 356742
Mean 1430
RMS 4994
Underflow 0
Overflow 0
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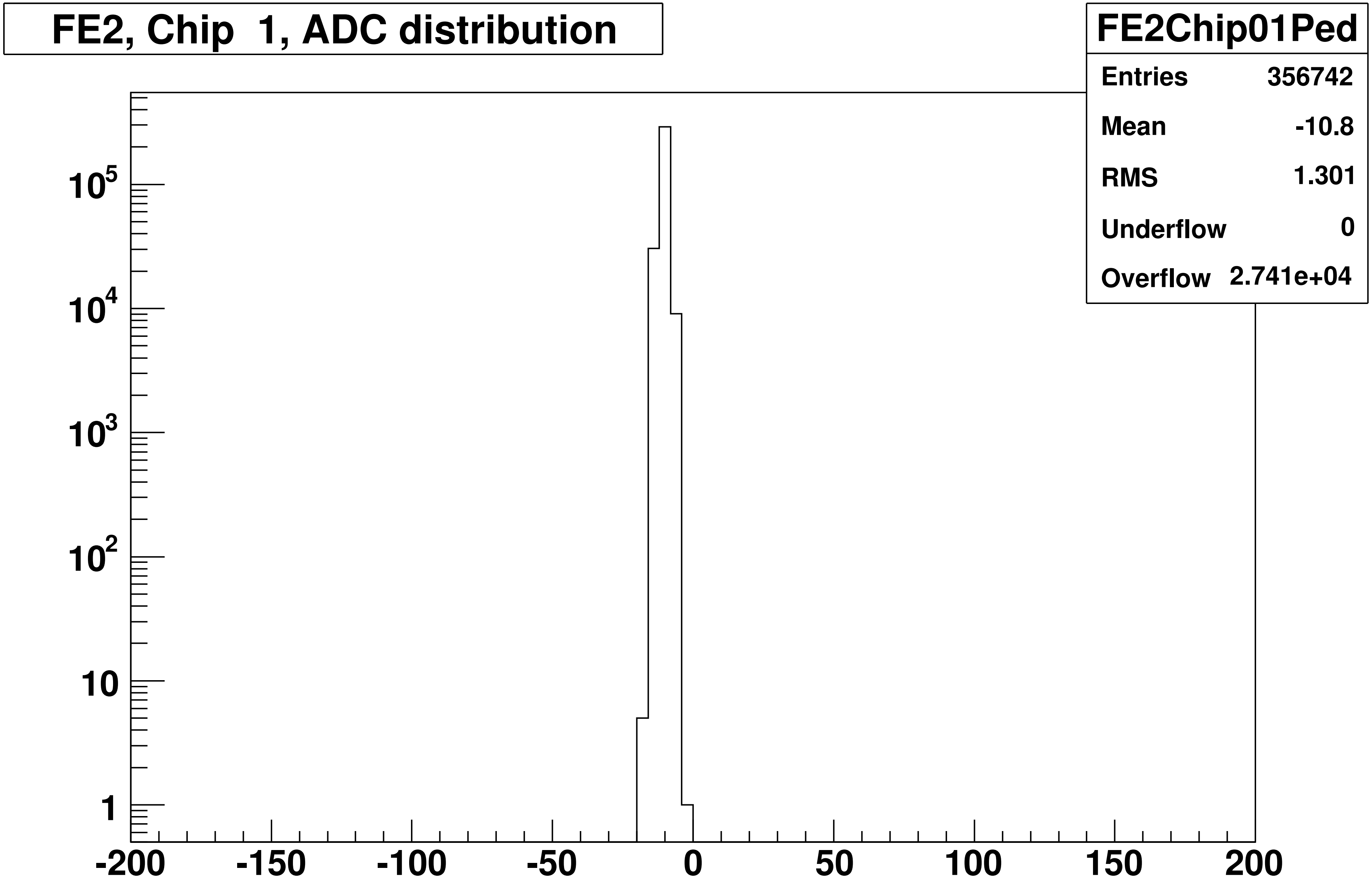
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 356742
Mean -10.8
RMS 1.301
Underflow 0
Overflow 2.741e+04
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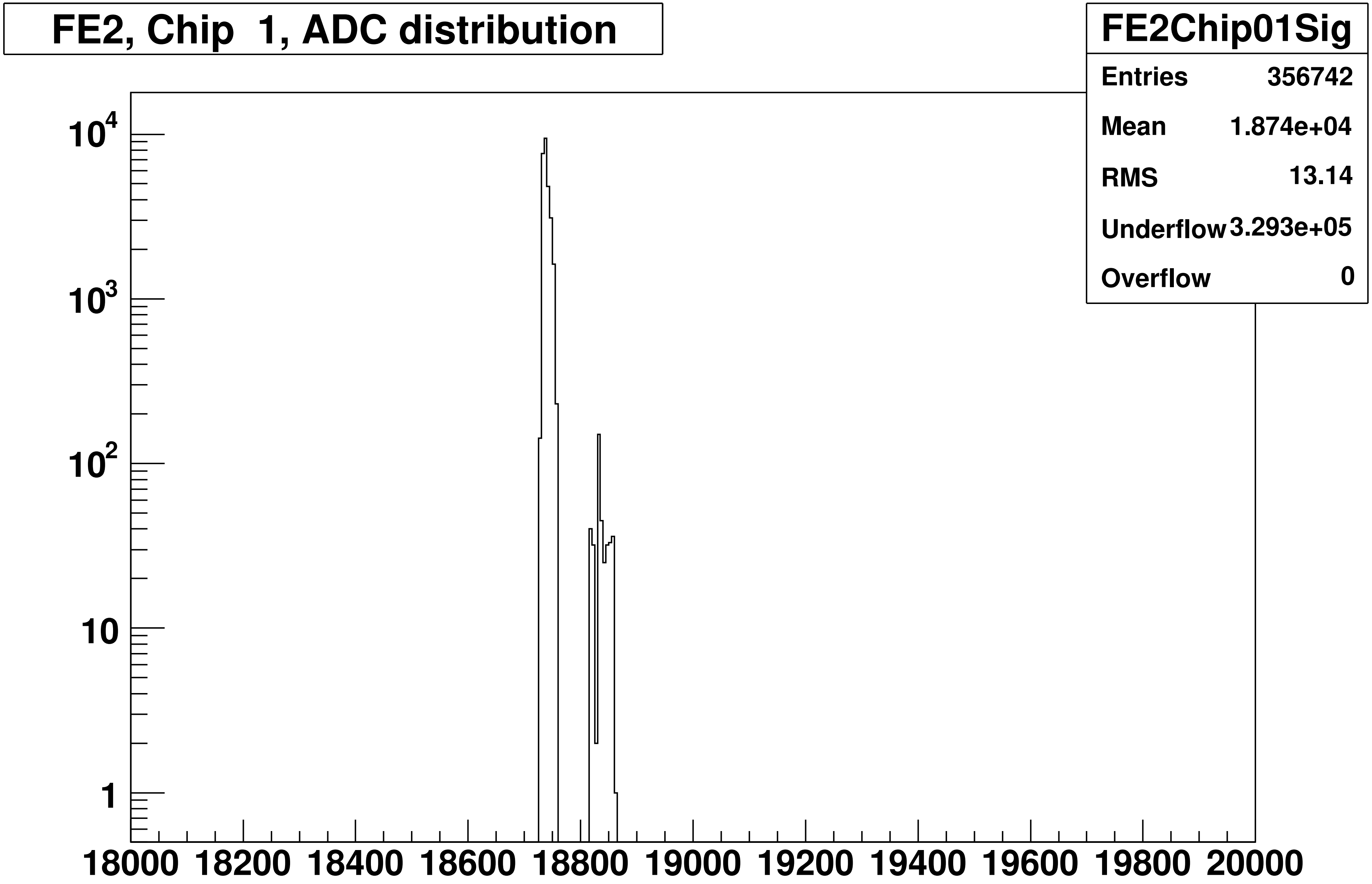
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 356742
Mean 1.874e+04
RMS 13.14
Underflow 3.293e+05
Overflow 0
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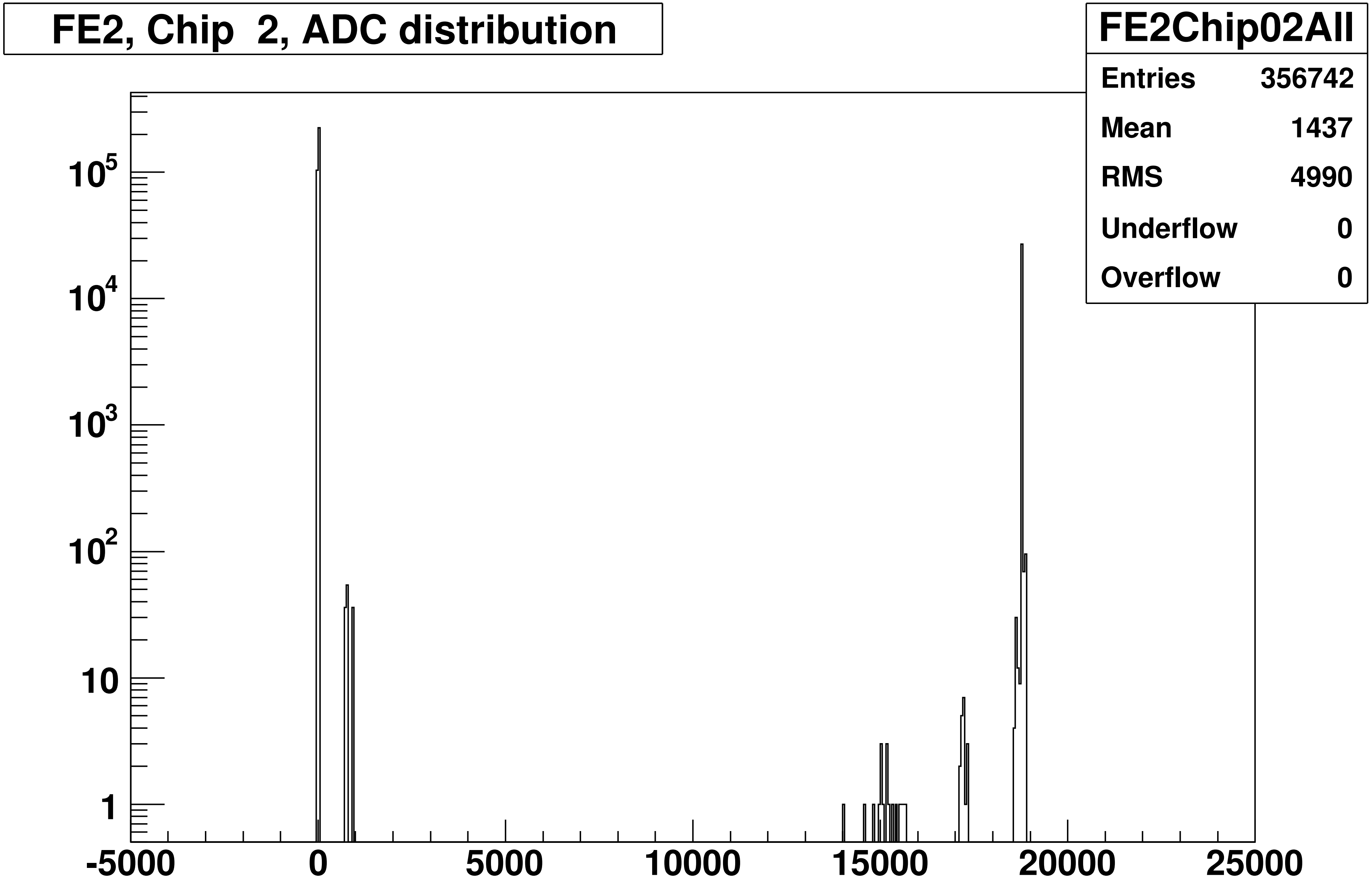
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 356742
Mean 1437
RMS 4990
Underflow 0
Overflow 0
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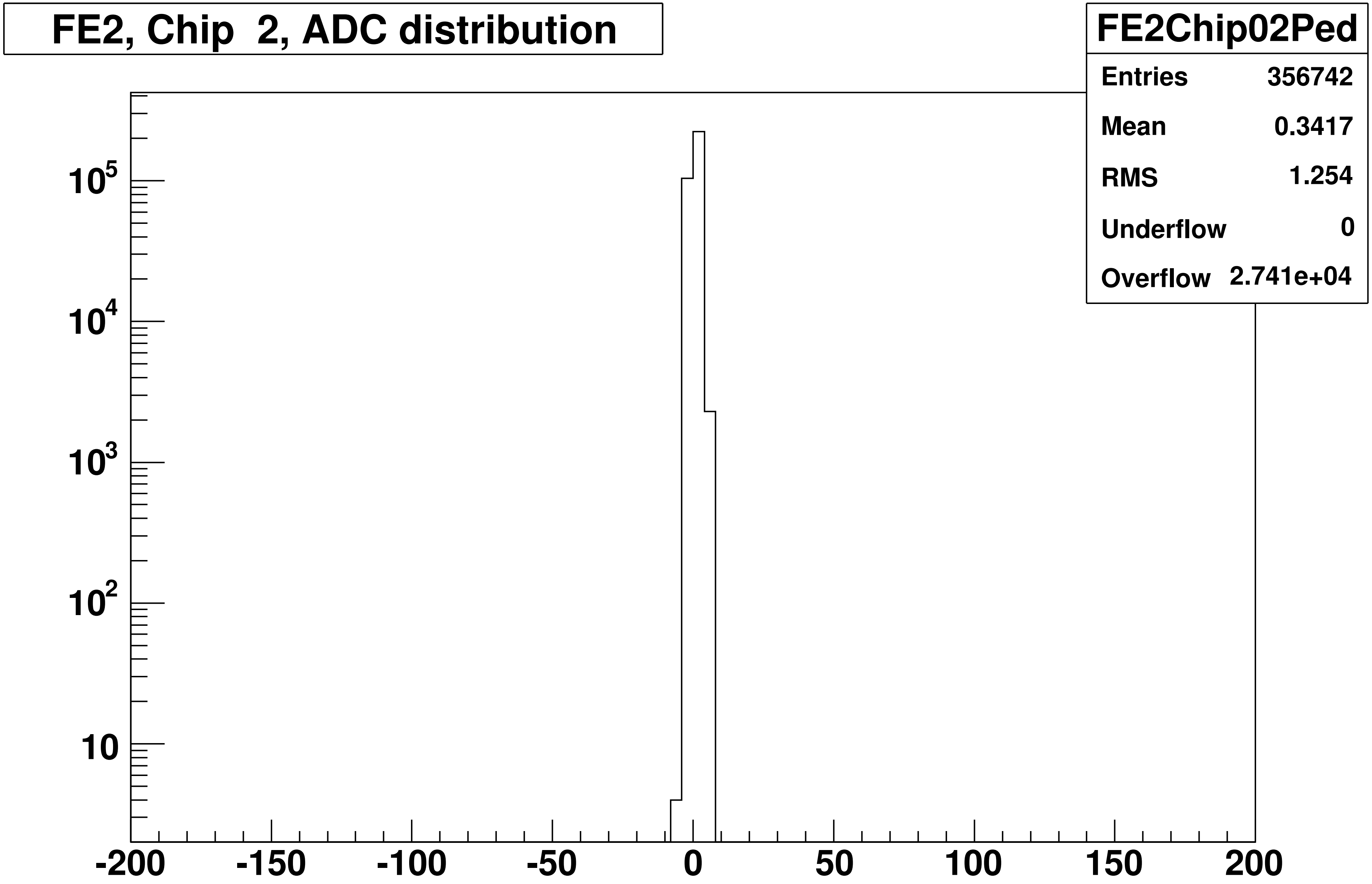
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 356742
Mean 0.3417
RMS 1.254
Underflow 0
Overflow 2.741e+04
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10^4
10^3
10^2
10
-200
-150
-100
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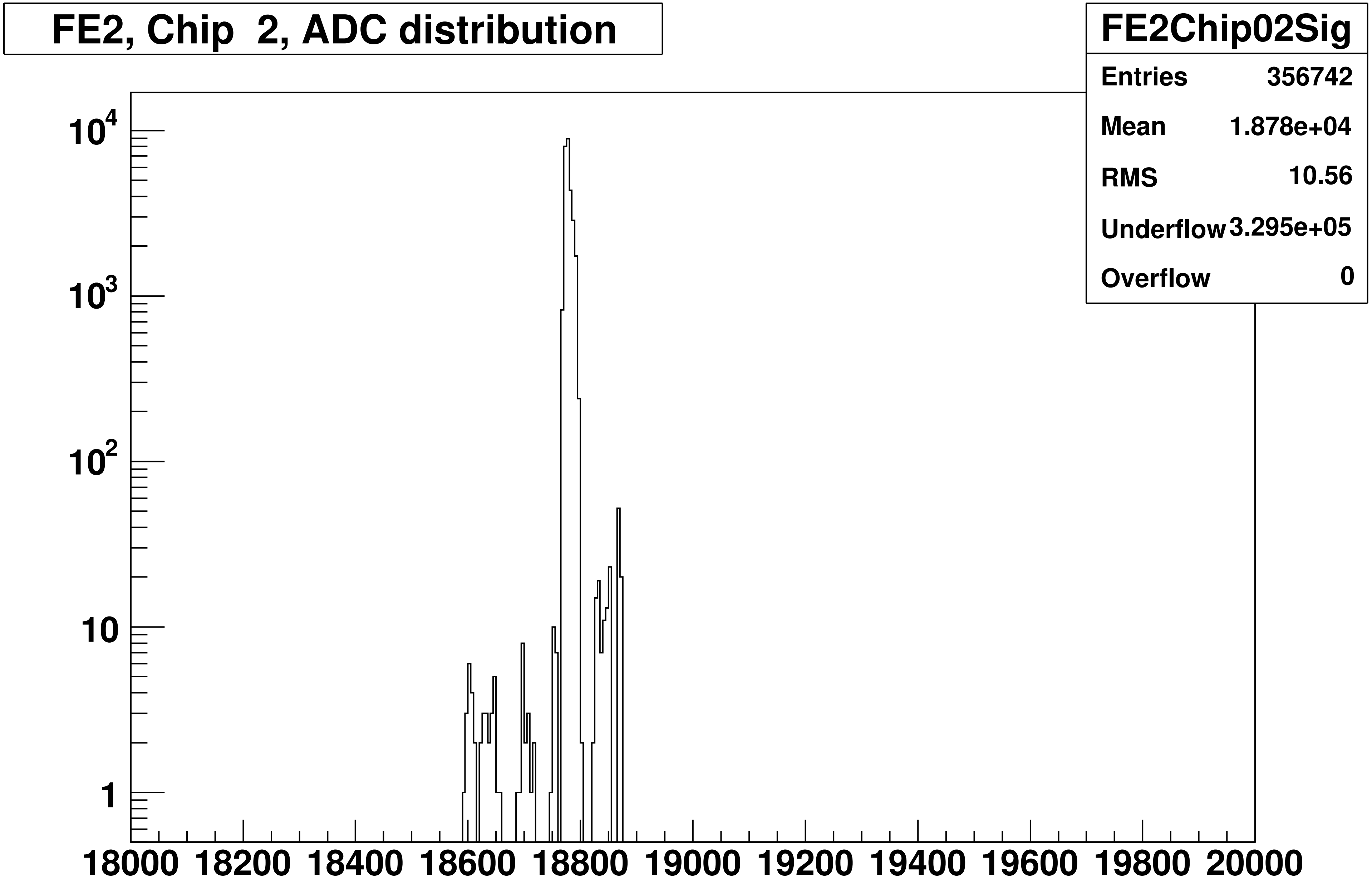
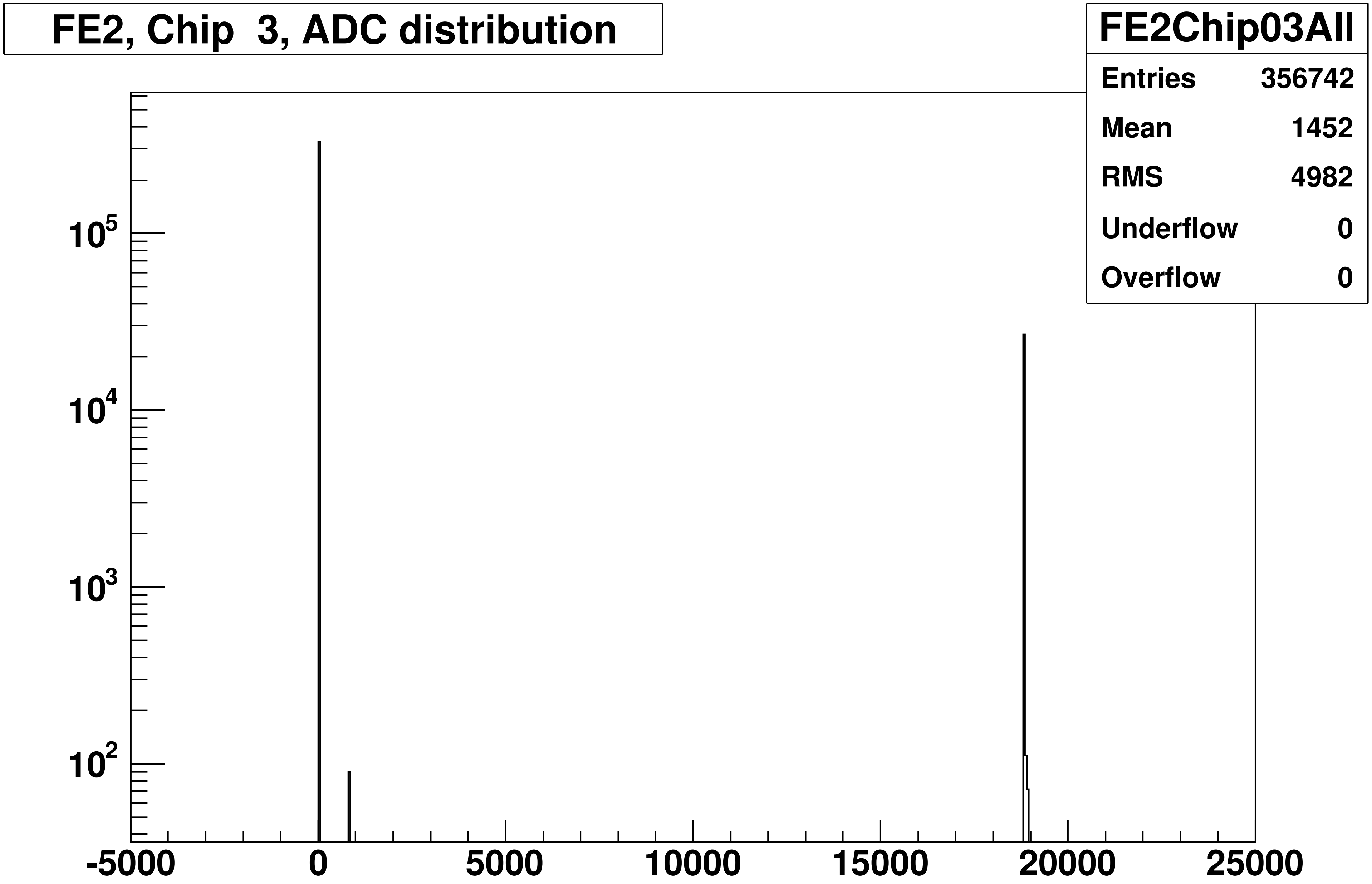
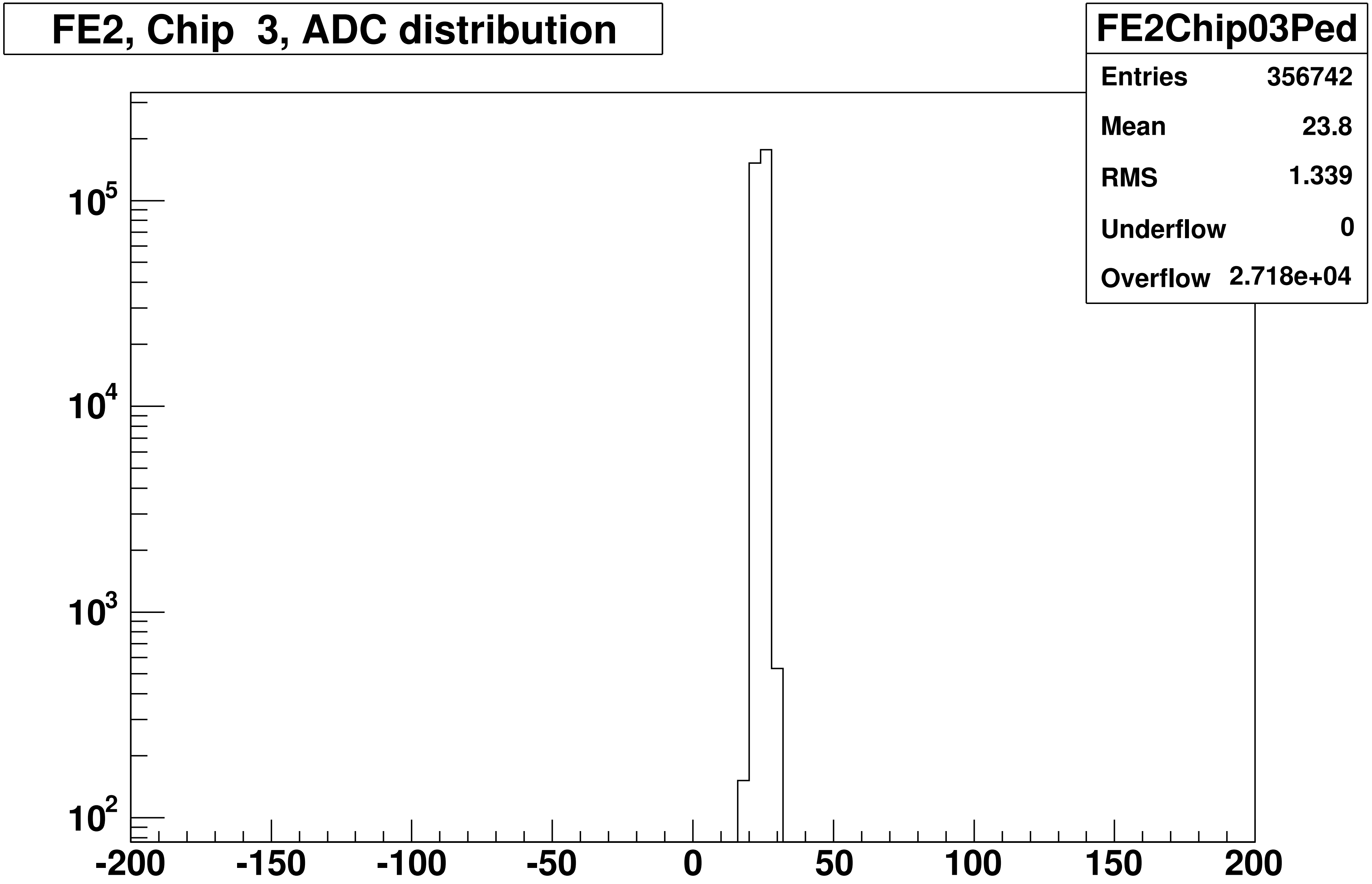
0
50
100
150
200


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 356742
Mean 1.878e+04
RMS 10.56
Underflow 3.295e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 356742
Mean 1452
RMS 4982
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 356742
Mean 23.8
RMS 1.339
Underflow 0
Overflow 2.718e+04
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10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
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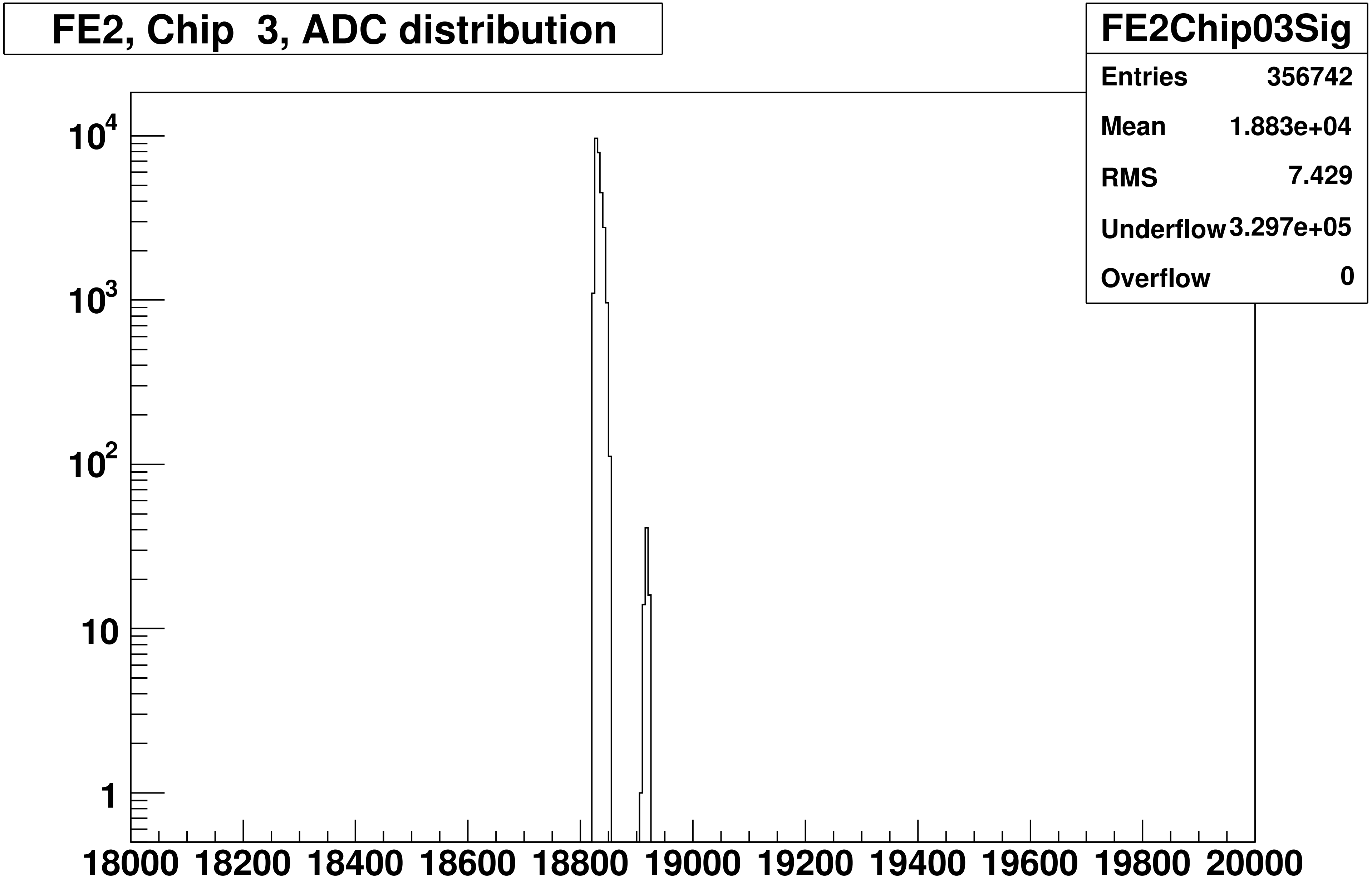
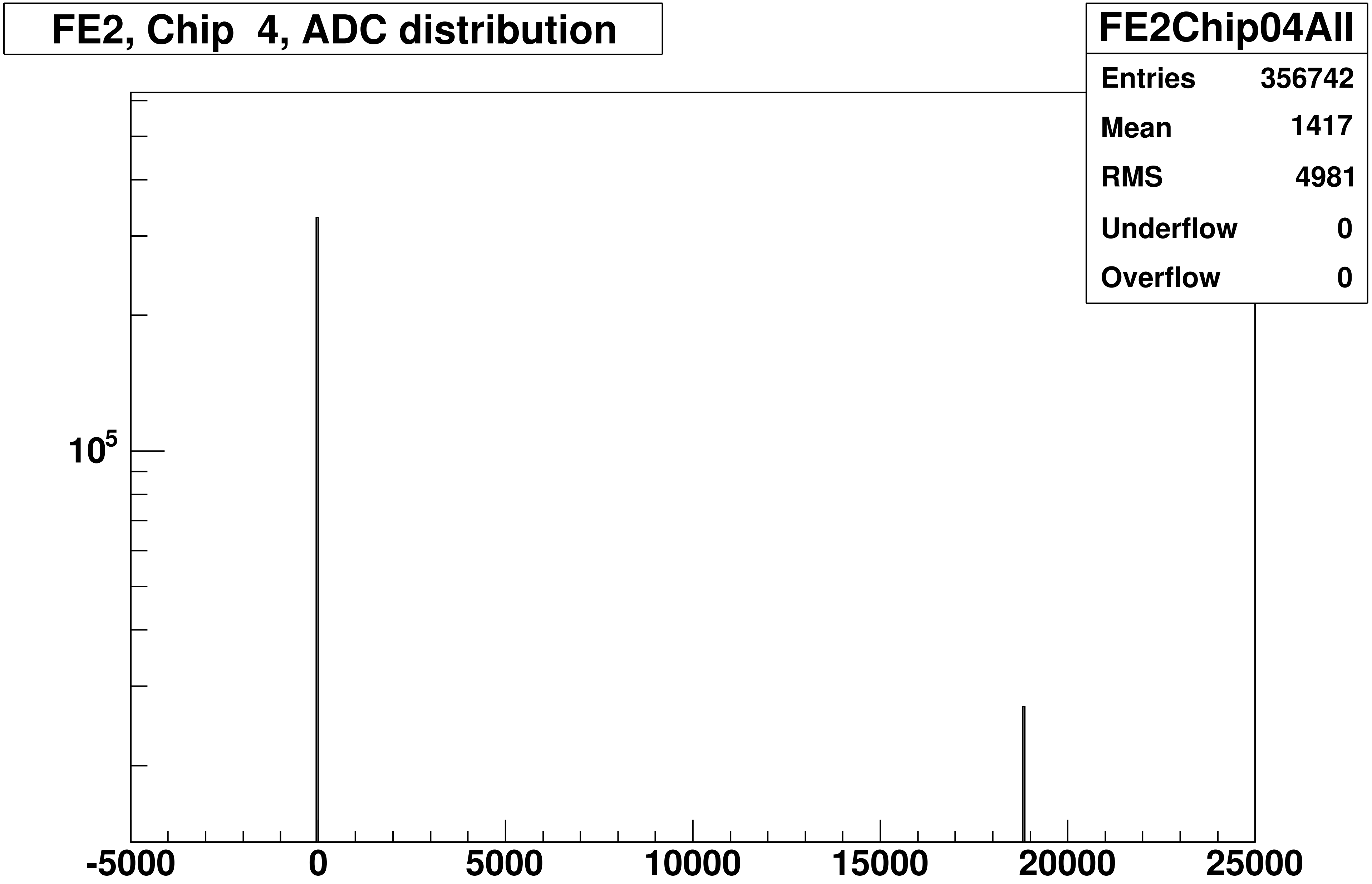
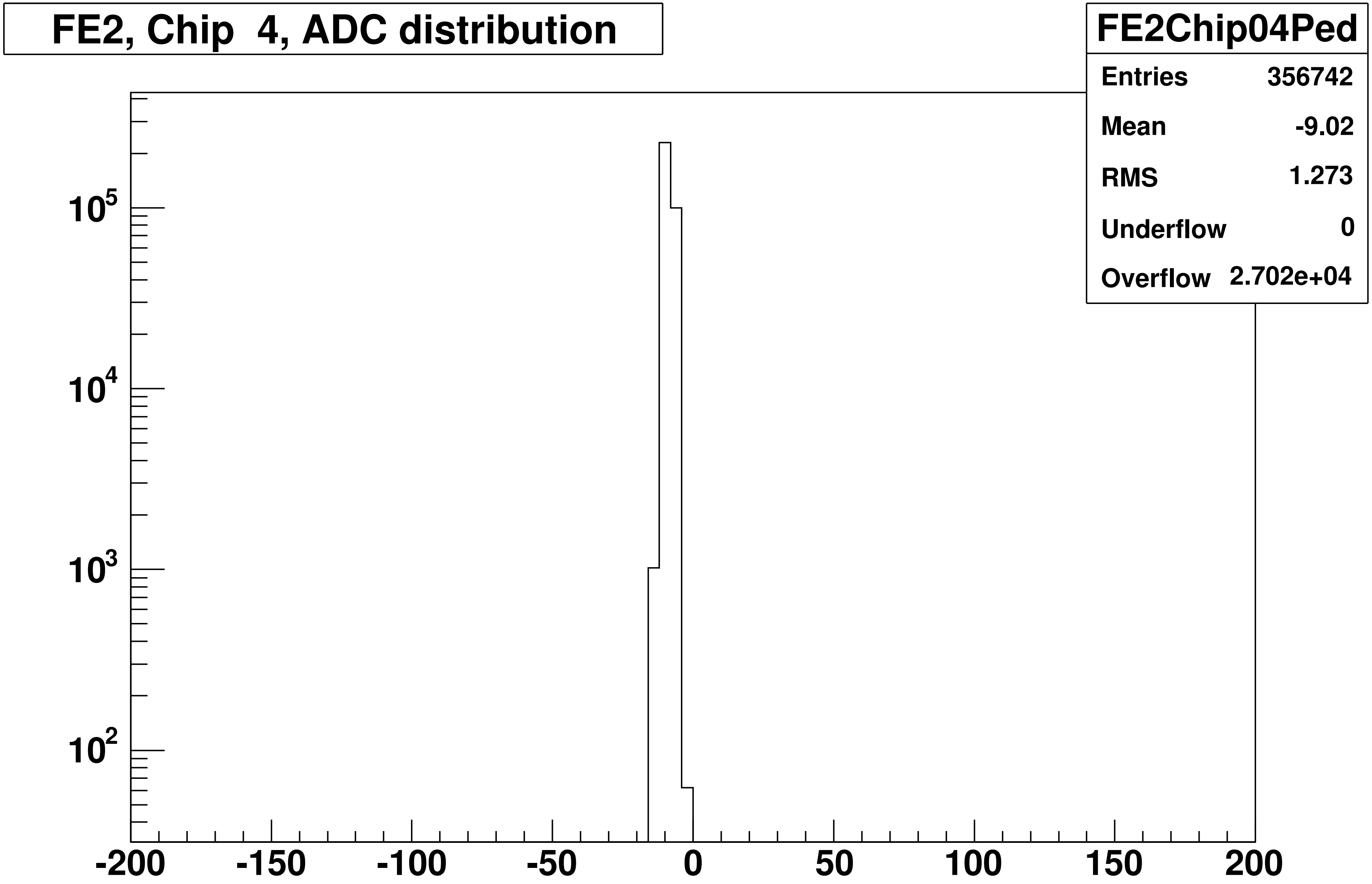
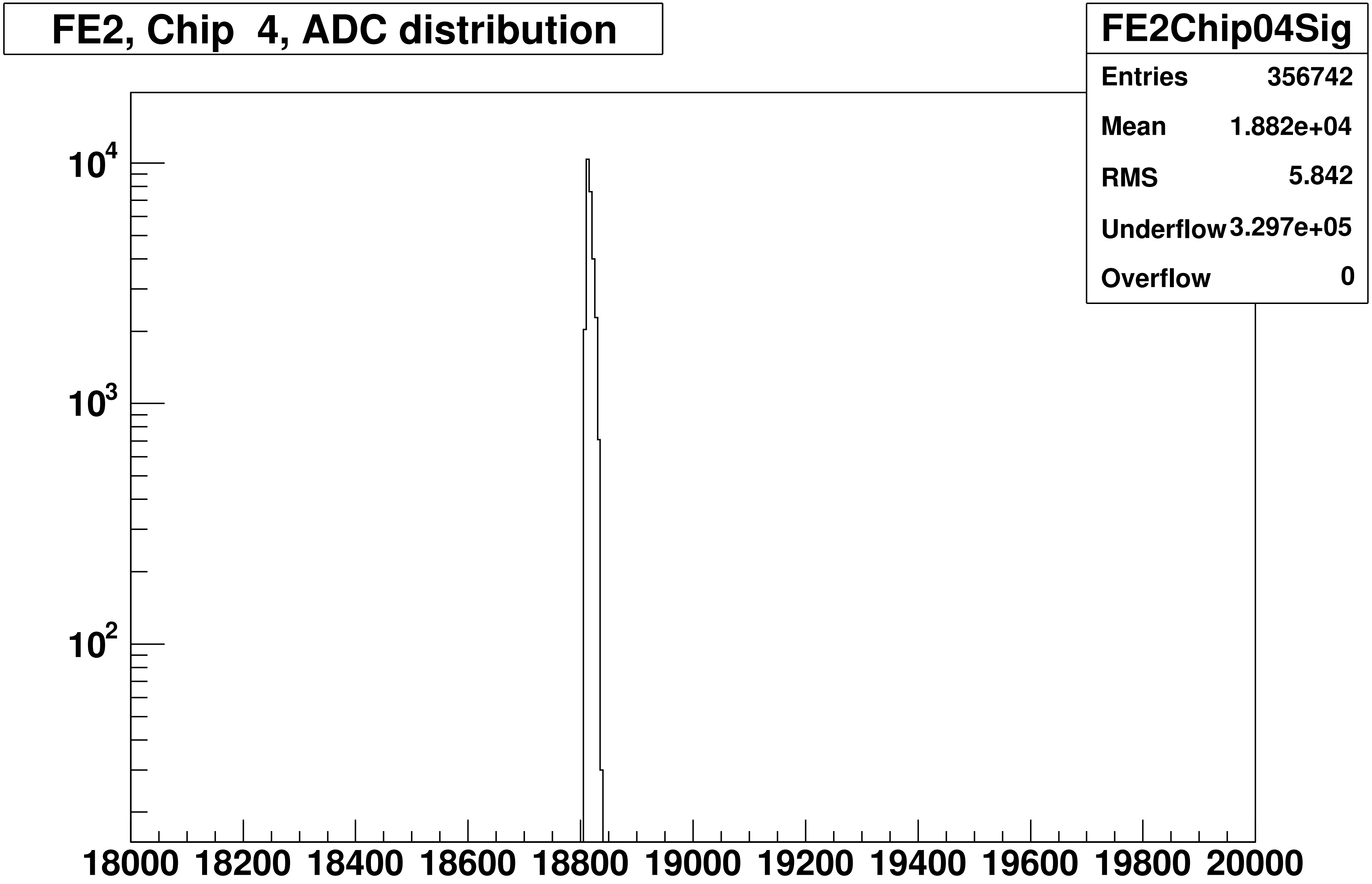


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 356742
Mean 1.883e+04
RMS 7.429
Underflow 3.297e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 356742
Mean 1417
RMS 4981
Underflow 0
Overflow 0
10^5
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 356742
Mean -9.02
RMS 1.273
Underflow 0
Overflow 2.702e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 356742
Mean 1.882e+04
RMS 5.842
Underflow 3.297e+05
Overflow 0
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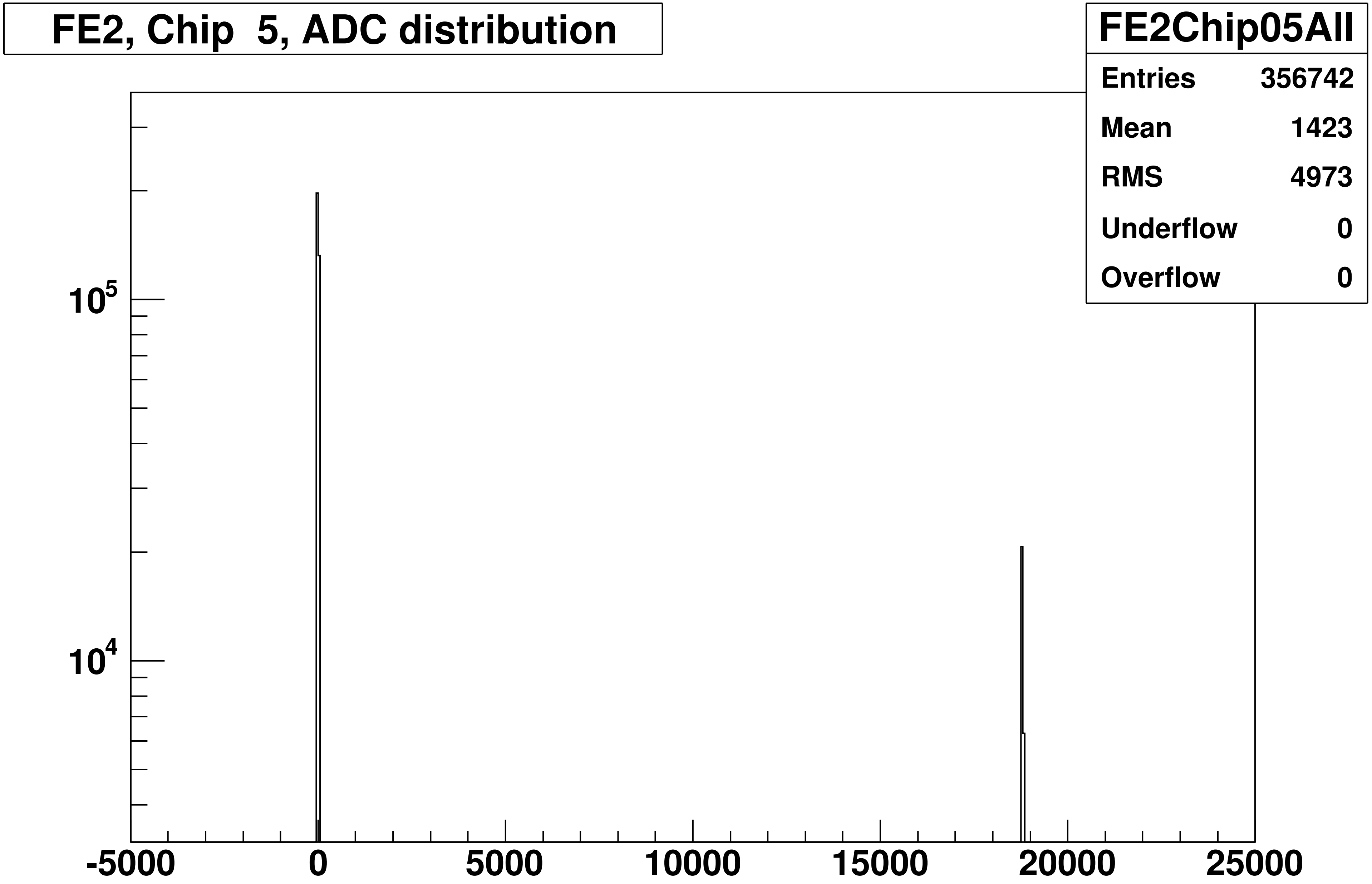
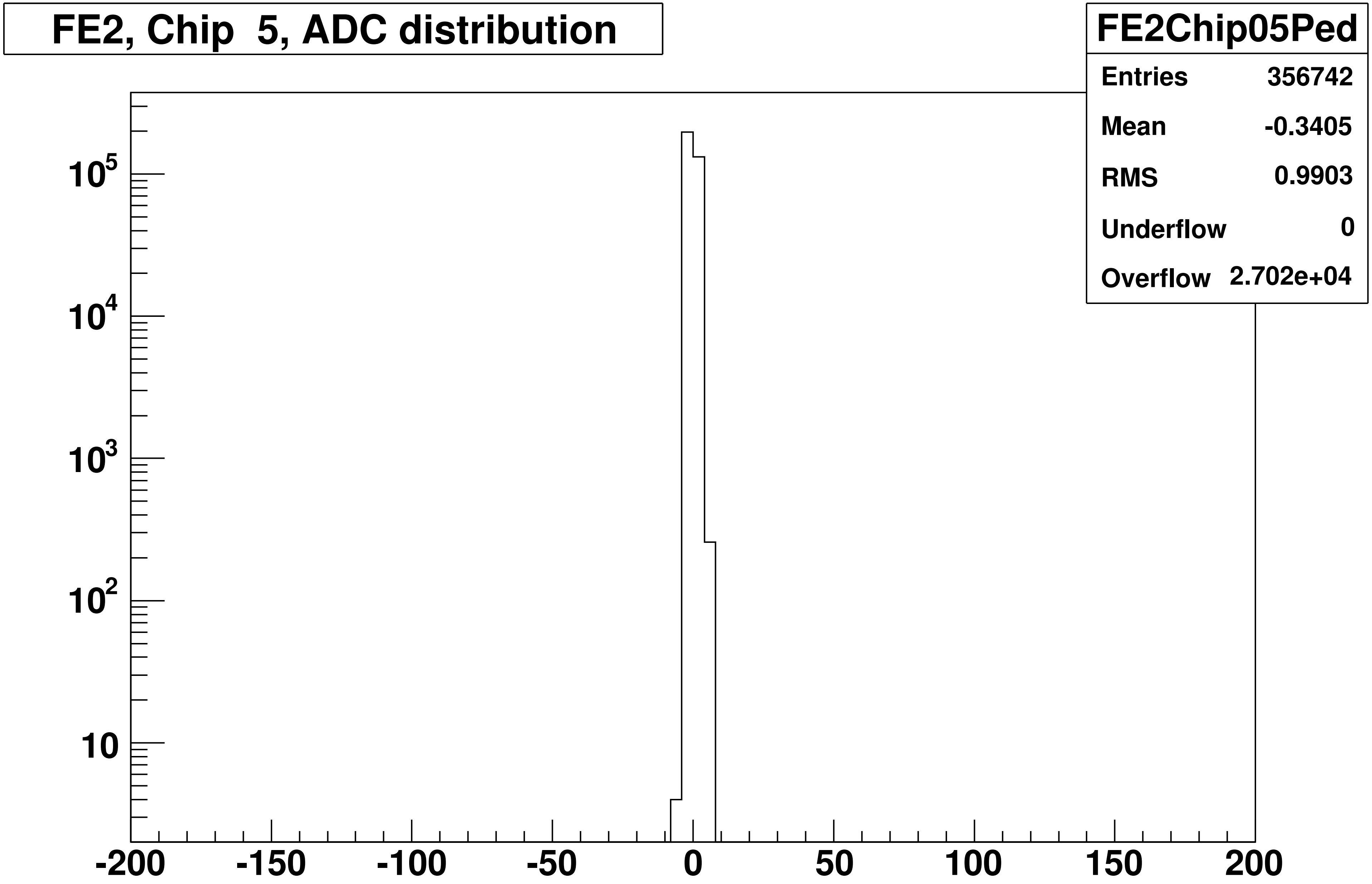
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 356742
Mean 1423
RMS 4973
Underflow 0
Overflow 0
10^5
10^4
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 356742
Mean -0.3405
RMS 0.9903
Underflow 0
Overflow 2.702e+04
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10^4
10^3
10^2
10
-200
-150
-100
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0
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100
150
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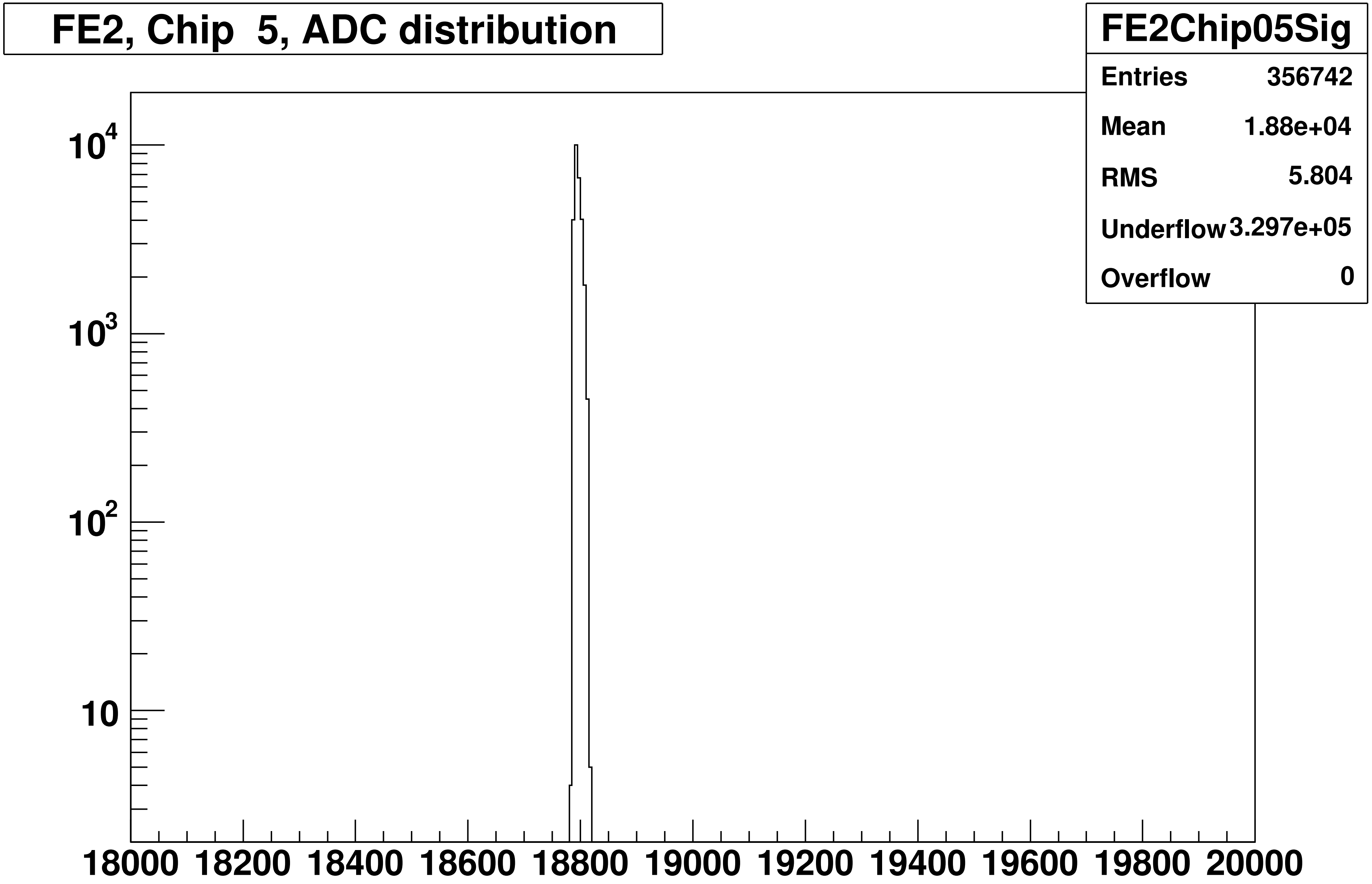
FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 356742
Mean 1.88e+04
RMS 5.804
Underflow 3.297e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
18600
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19000
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19600
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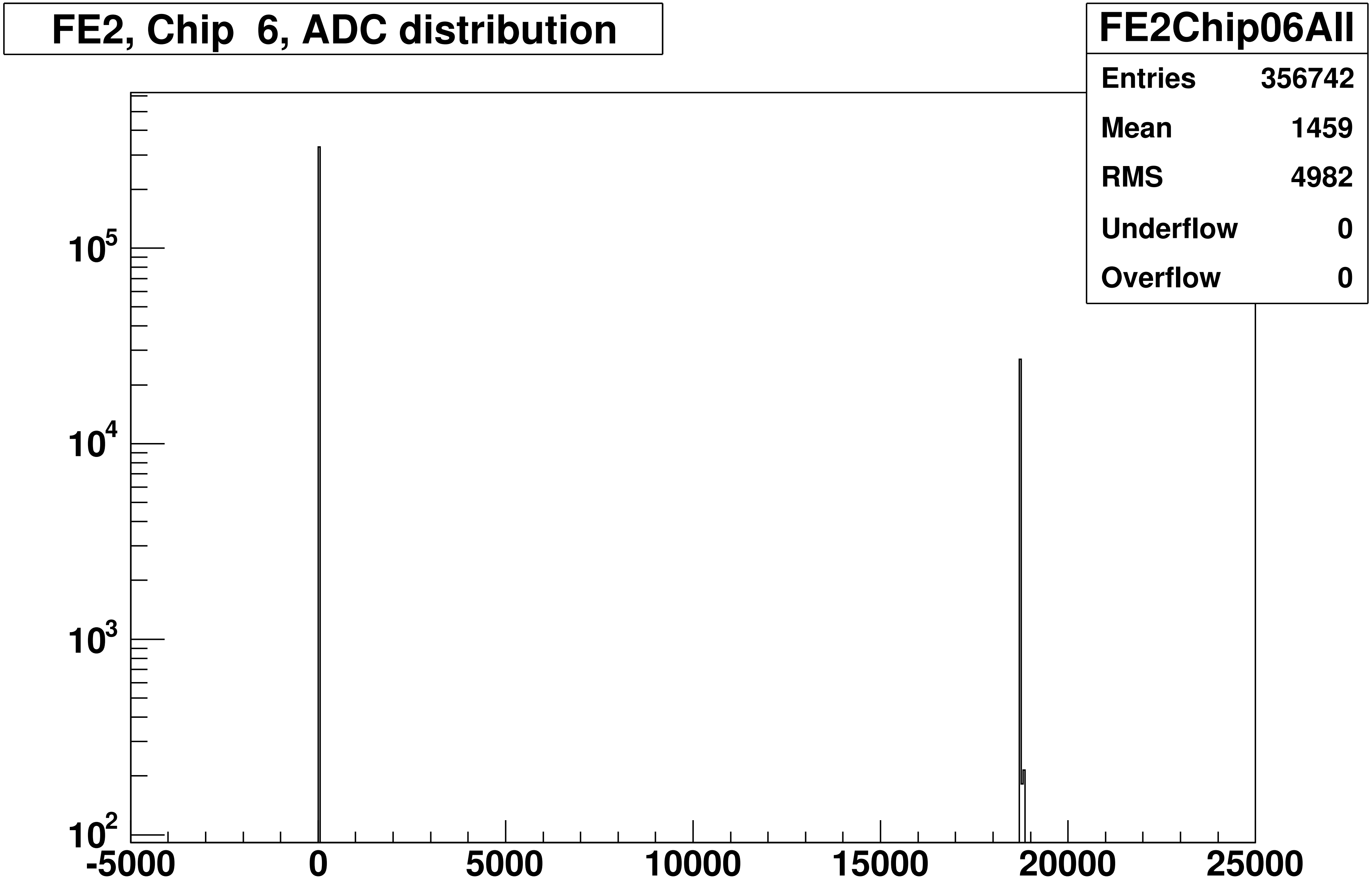
20000


FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 356742
Mean 1459
RMS 4982
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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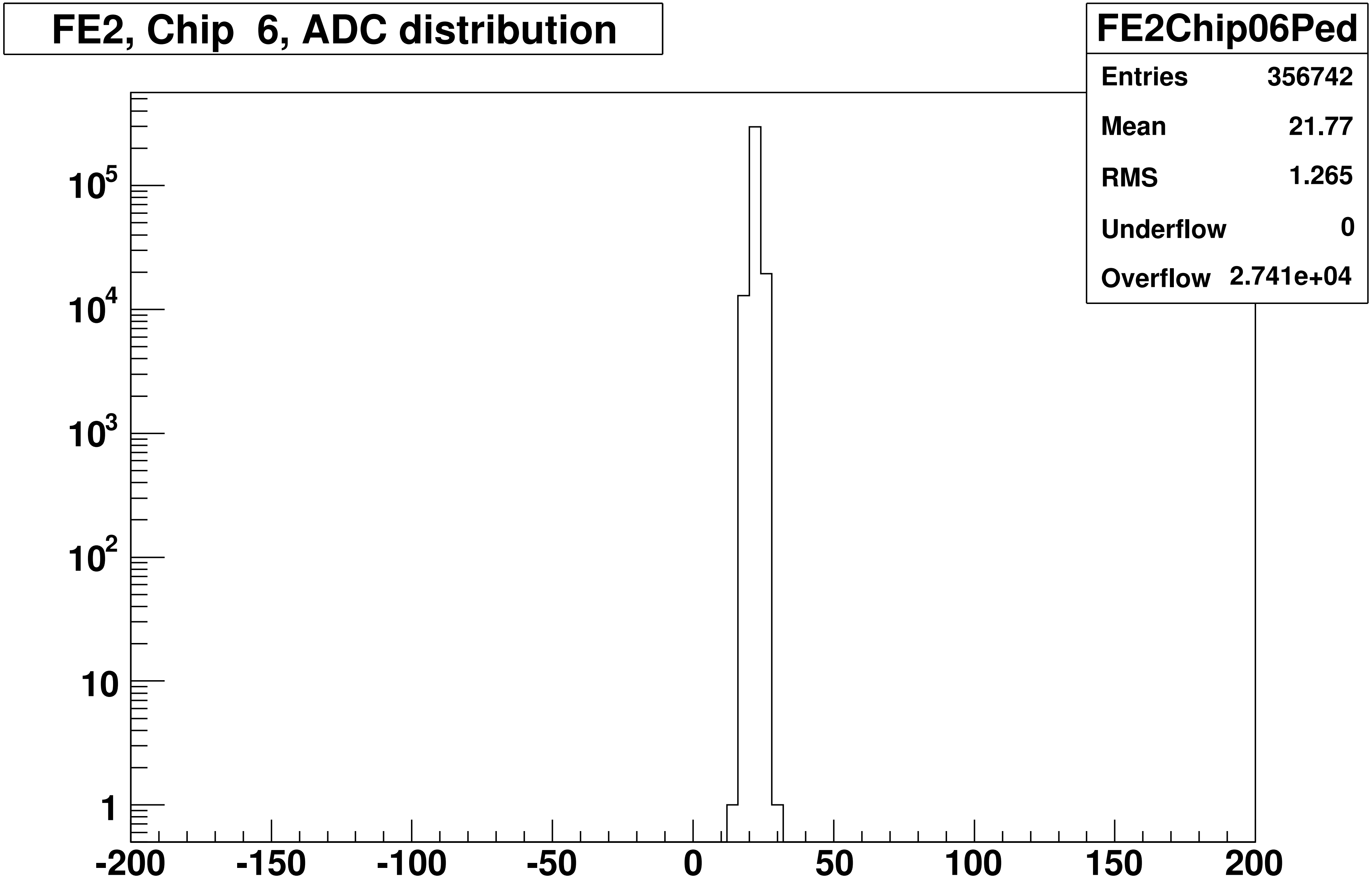
0
5000
10000
15000
20000
25000


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 356742
Mean 21.77
RMS 1.265
Underflow 0
Overflow 2.741e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
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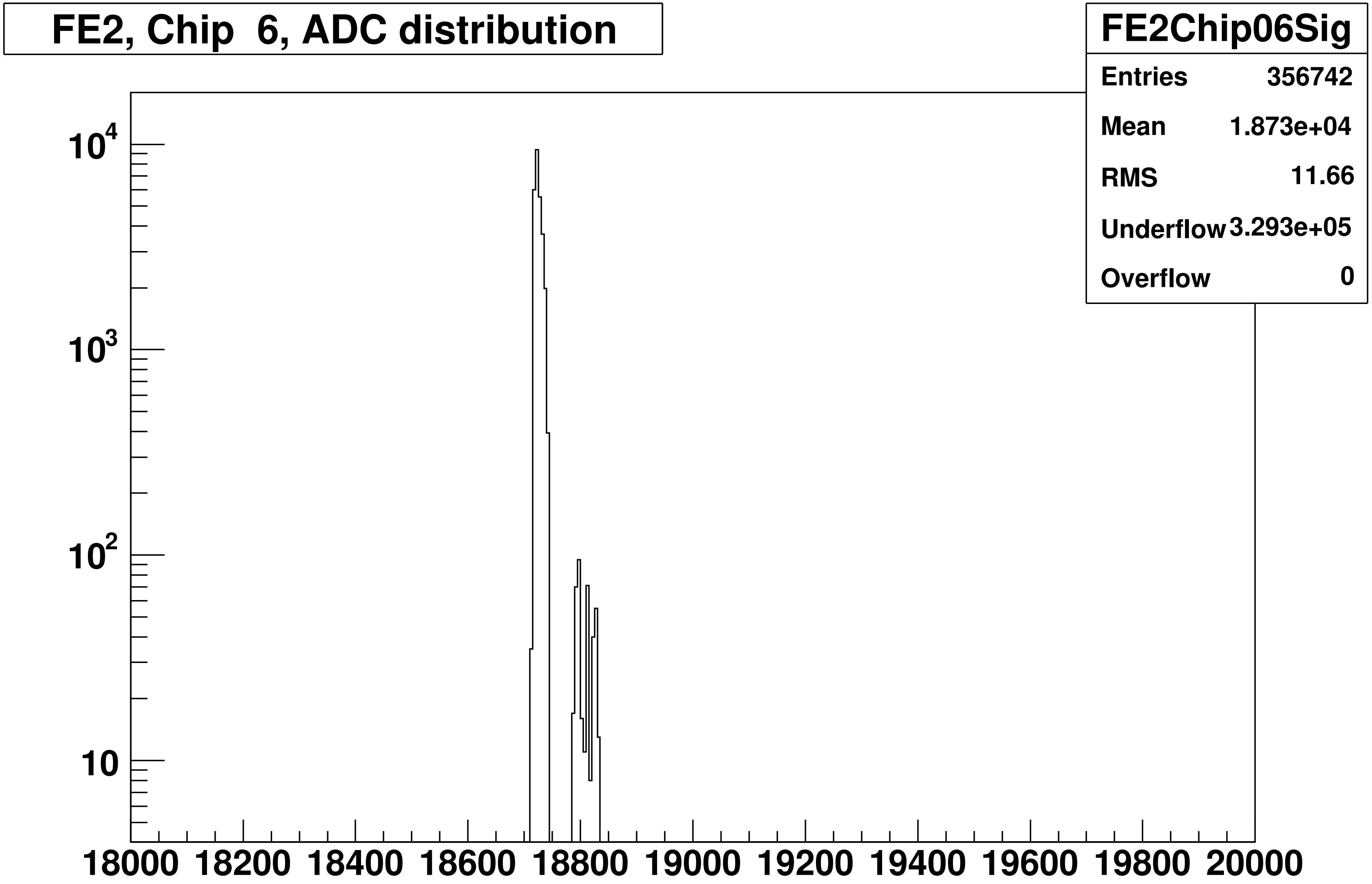
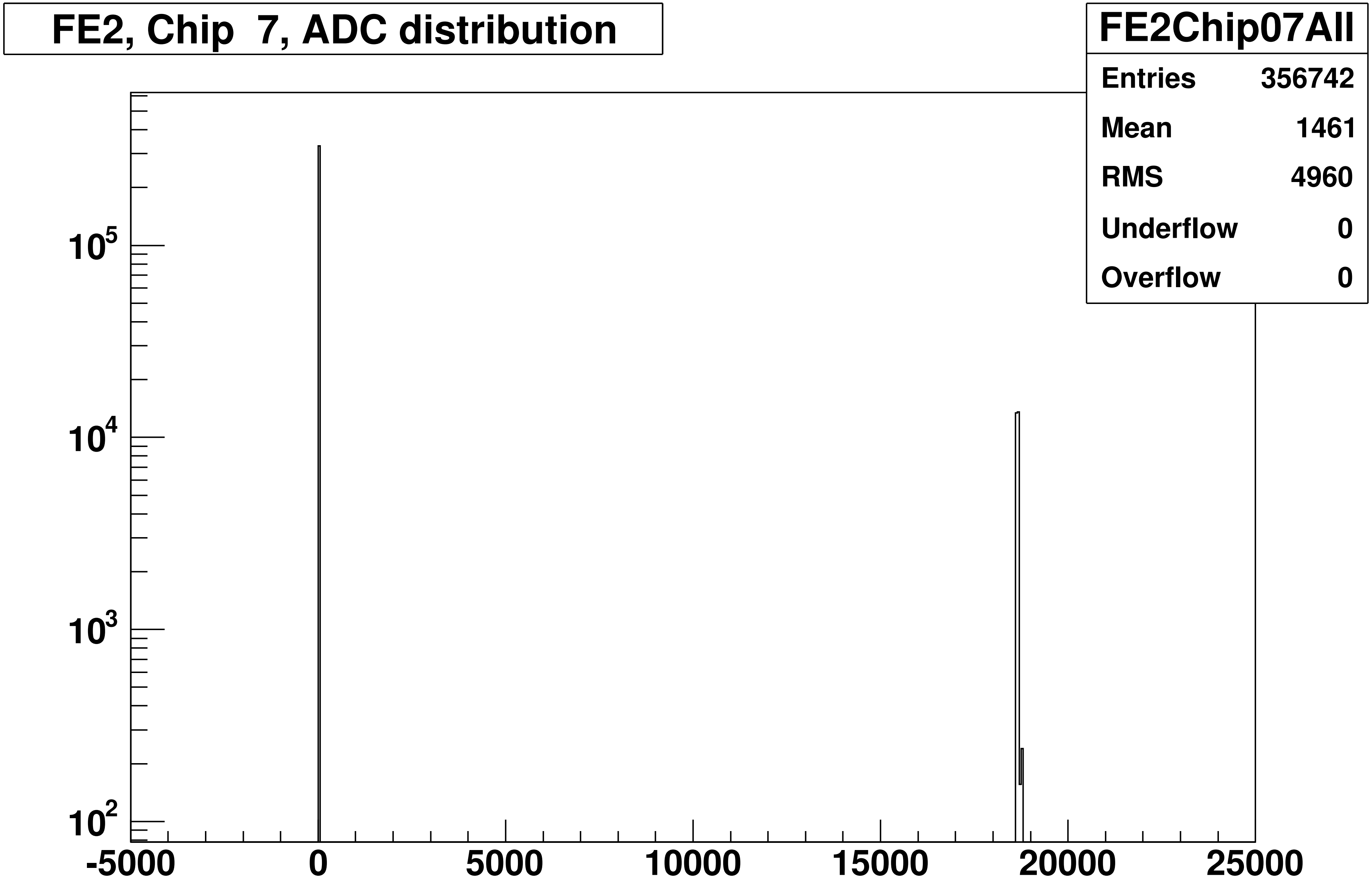
0
50
100
150
200


FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 356742
Mean 1.873e+04
RMS 11.66
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 356742
Mean 1461
RMS 4960
Underflow 0
Overflow 0
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10^4
10^3
10^2
-5000
0
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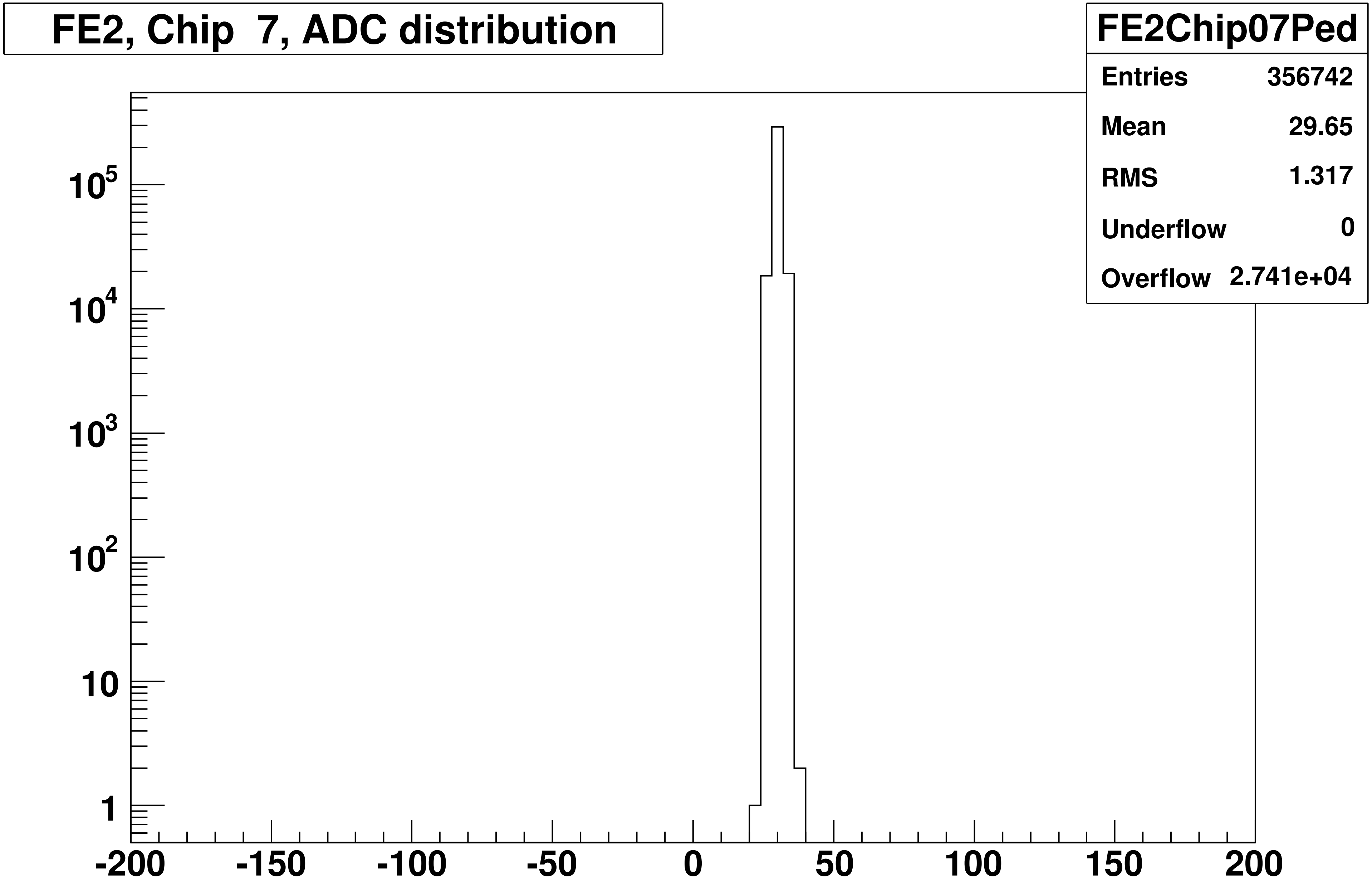
10000
15000
20000
25000



FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 356742
Mean 29.65
RMS 1.317
Underflow 0
Overflow 2.741e+04
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10^4
10^3
10^2
10
1
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-150
-100
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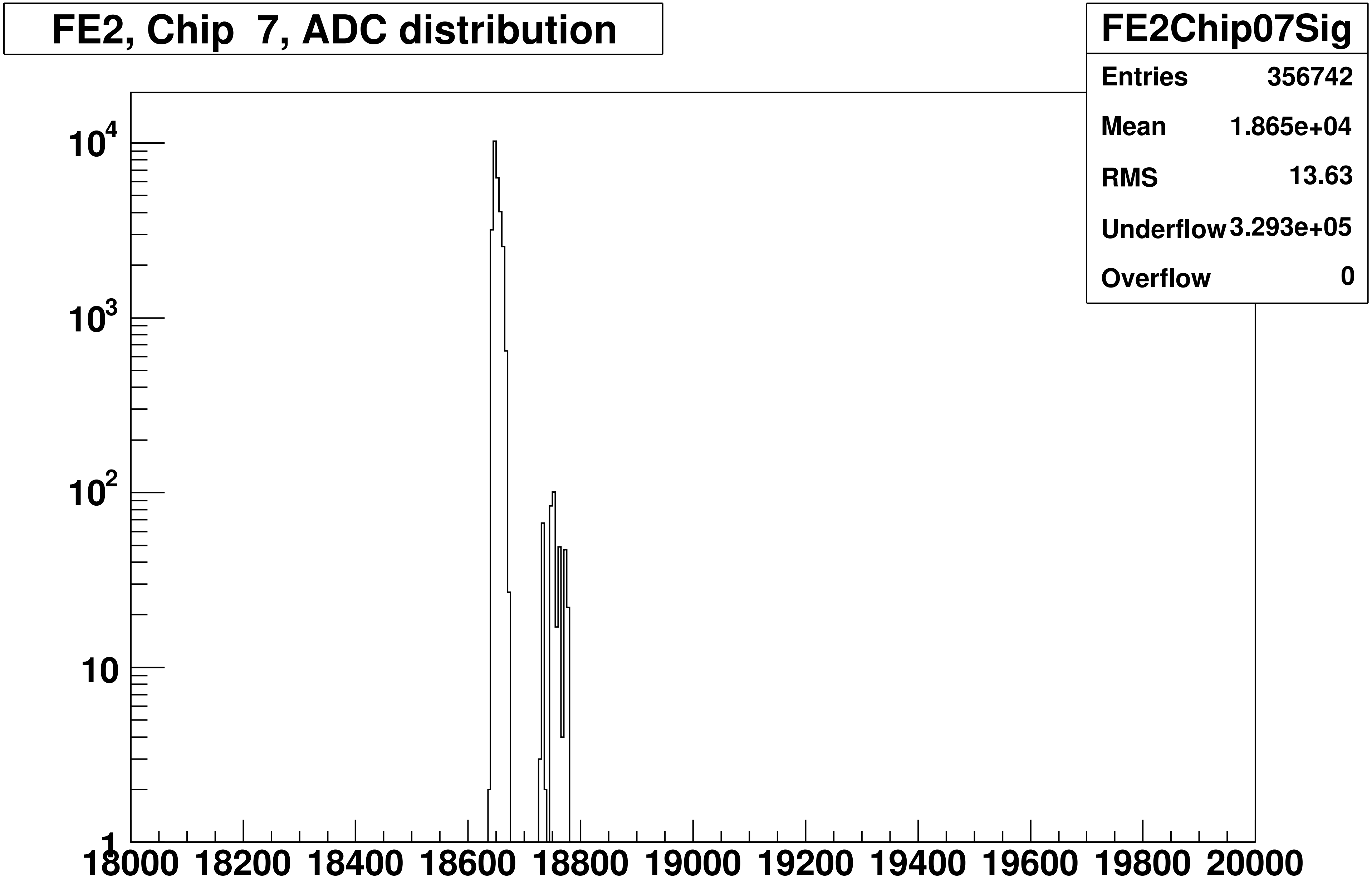
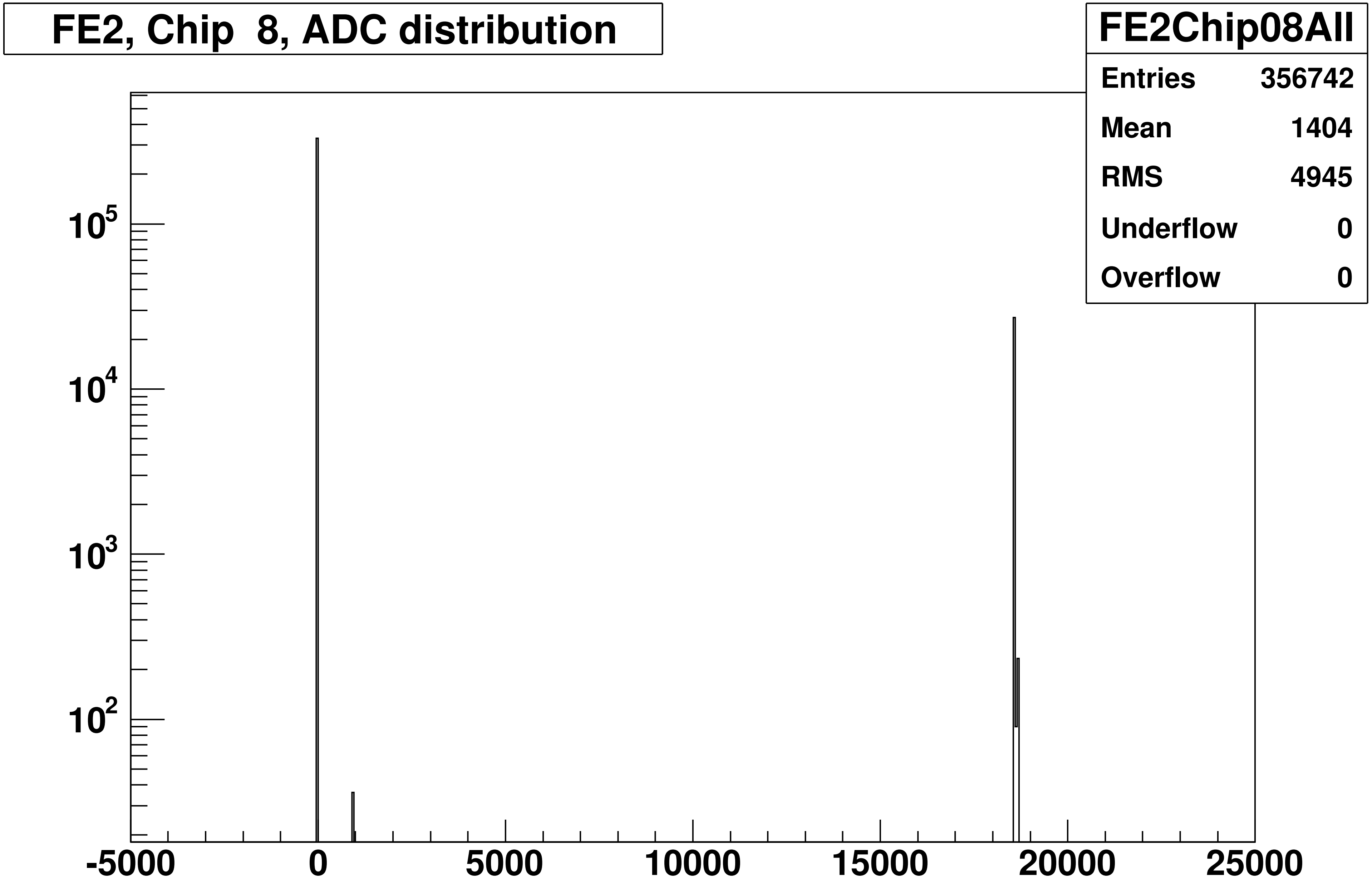
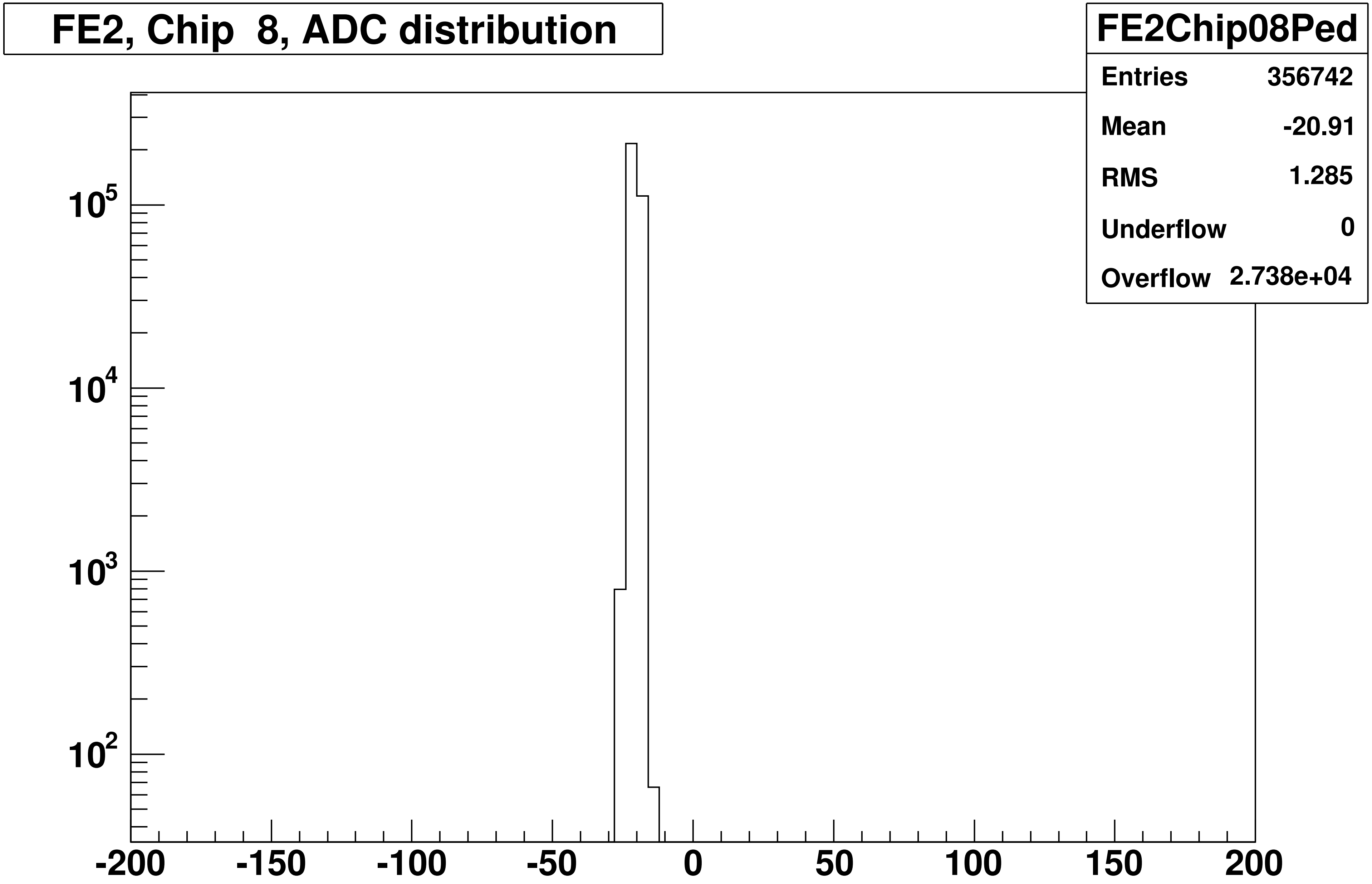
0
50
100
150
200


FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 356742
Mean 1.865e+04
RMS 13.63
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 356742
Mean 1404
RMS 4945
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 356742
Mean -20.91
RMS 1.285
Underflow 0
Overflow 2.738e+04
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10^4
10^3
10^2
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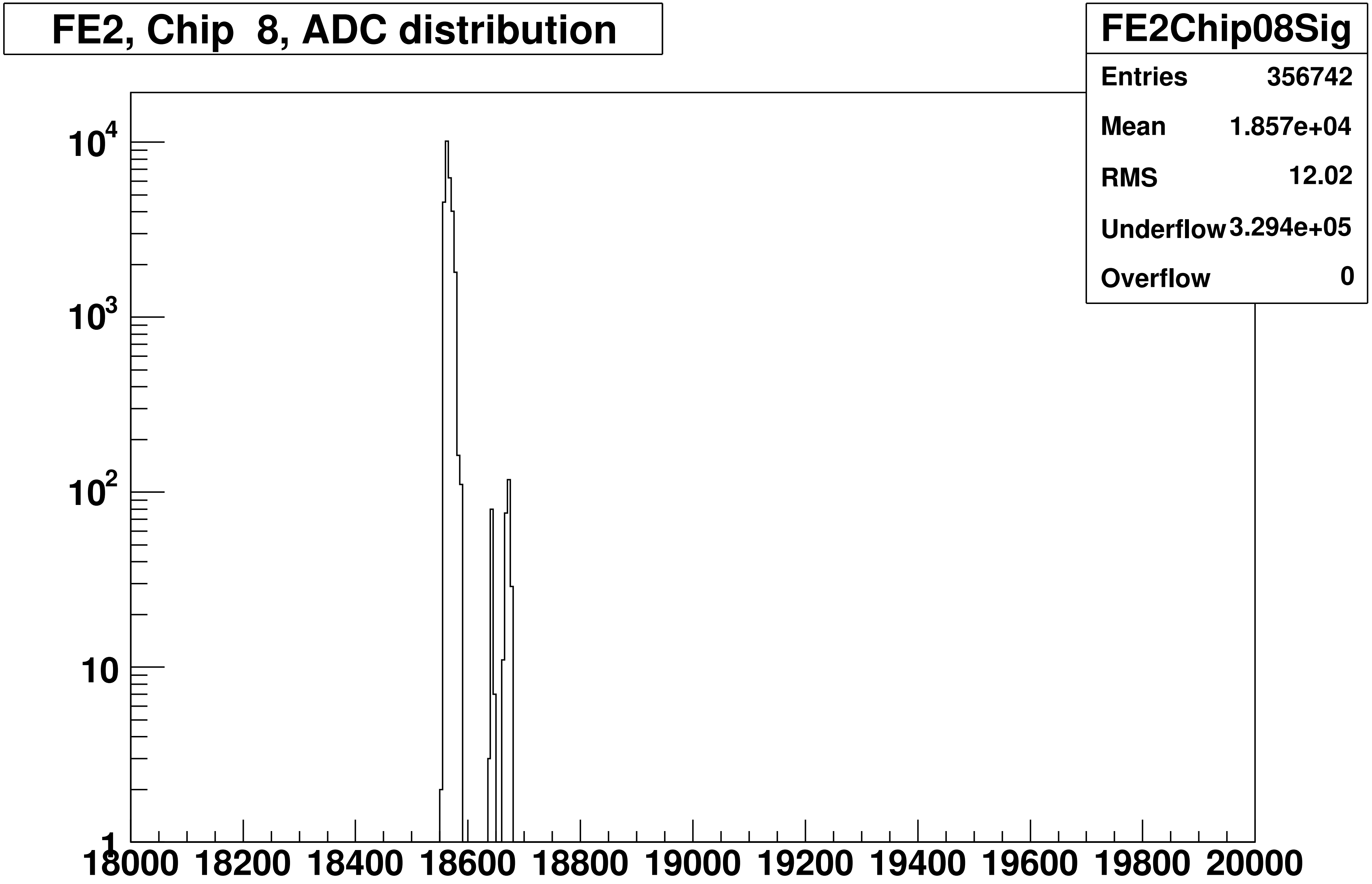
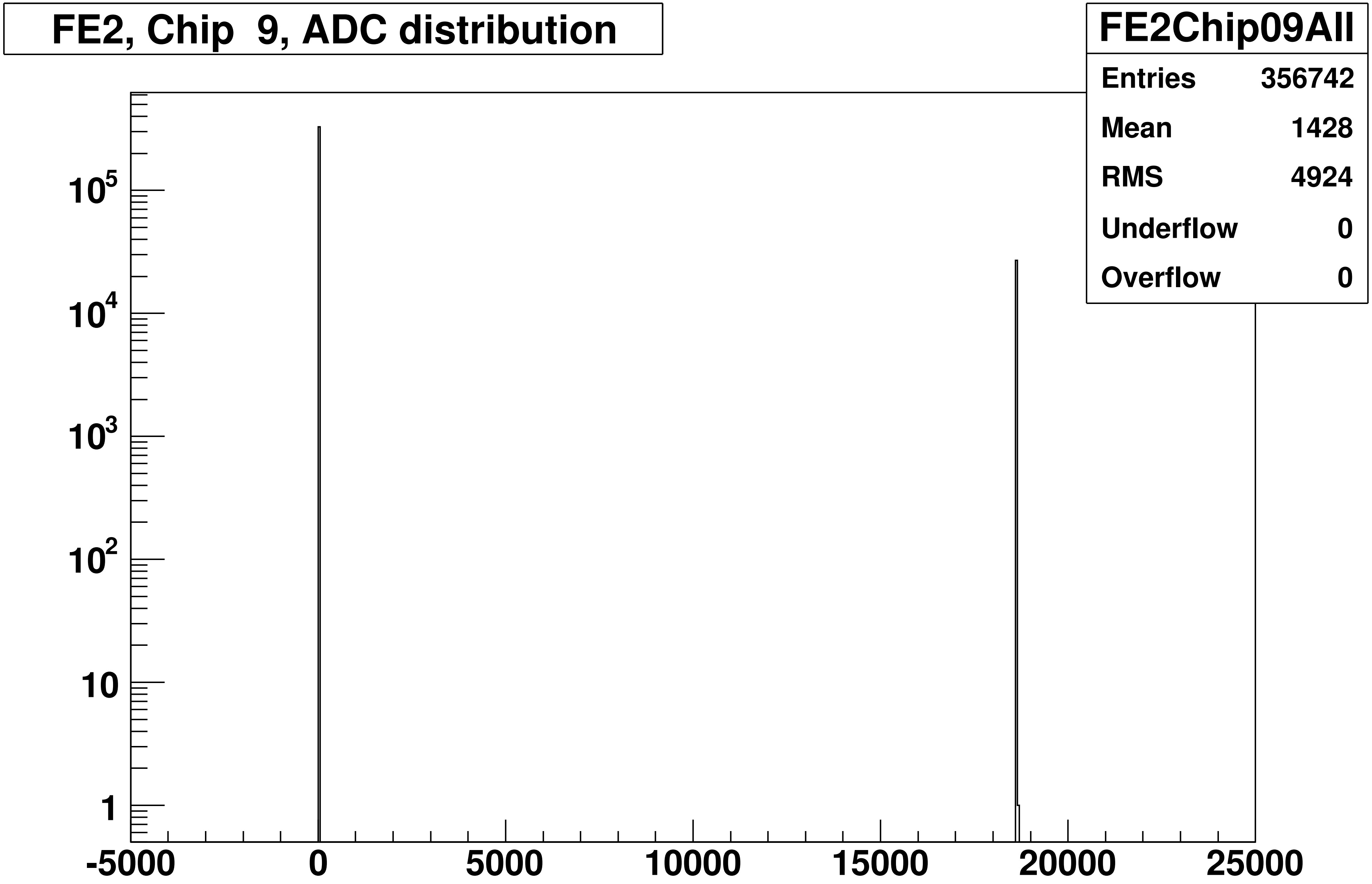
-150
-100
-50
0
50
100
150
200



FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 356742
Mean 1.857e+04
RMS 12.02
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 356742
Mean 1428
RMS 4924
Underflow 0
Overflow 0
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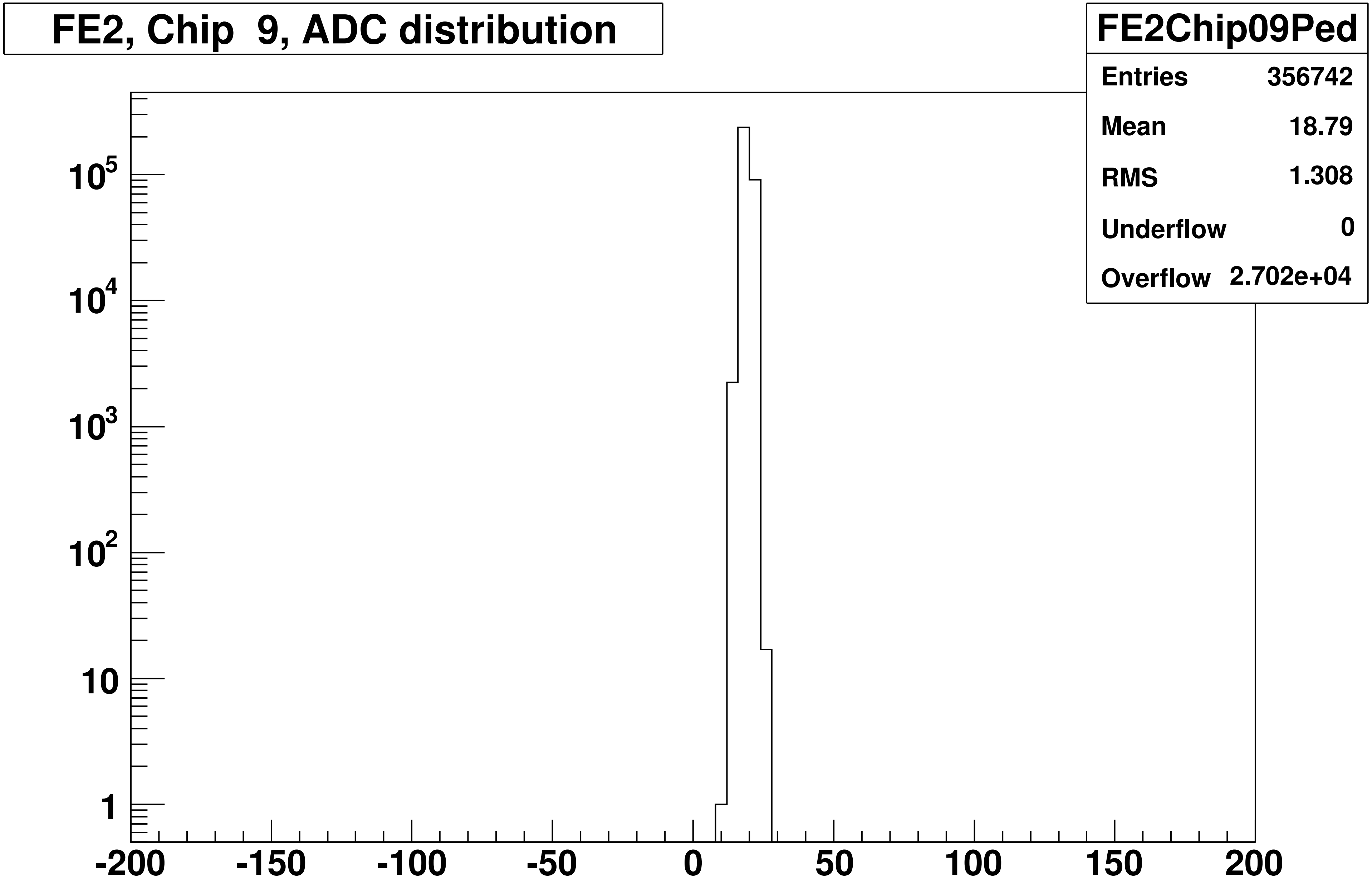
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 356742
Mean 18.79
RMS 1.308
Underflow 0
Overflow 2.702e+04
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10^4
10^3
10^2
10
1
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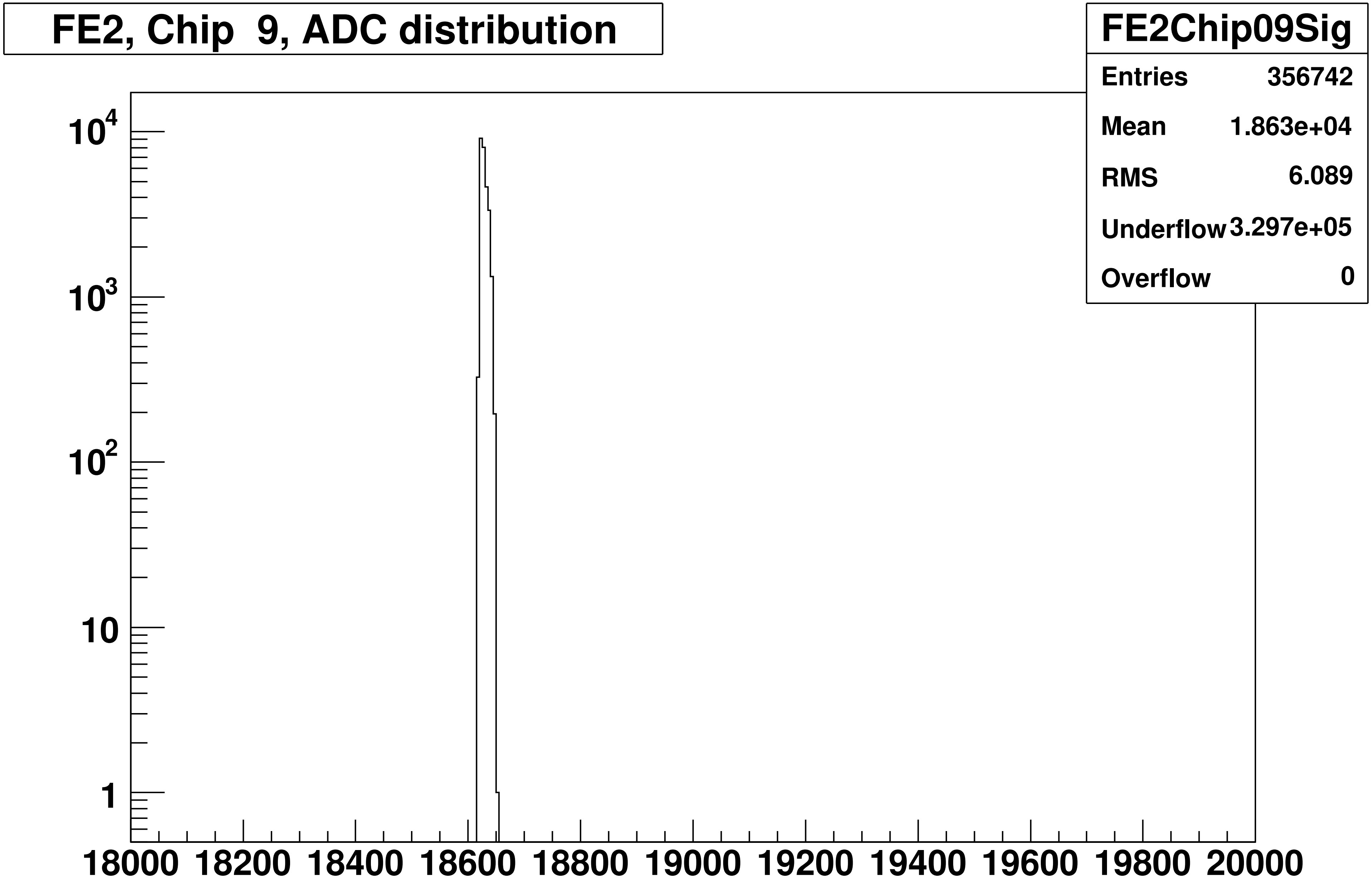
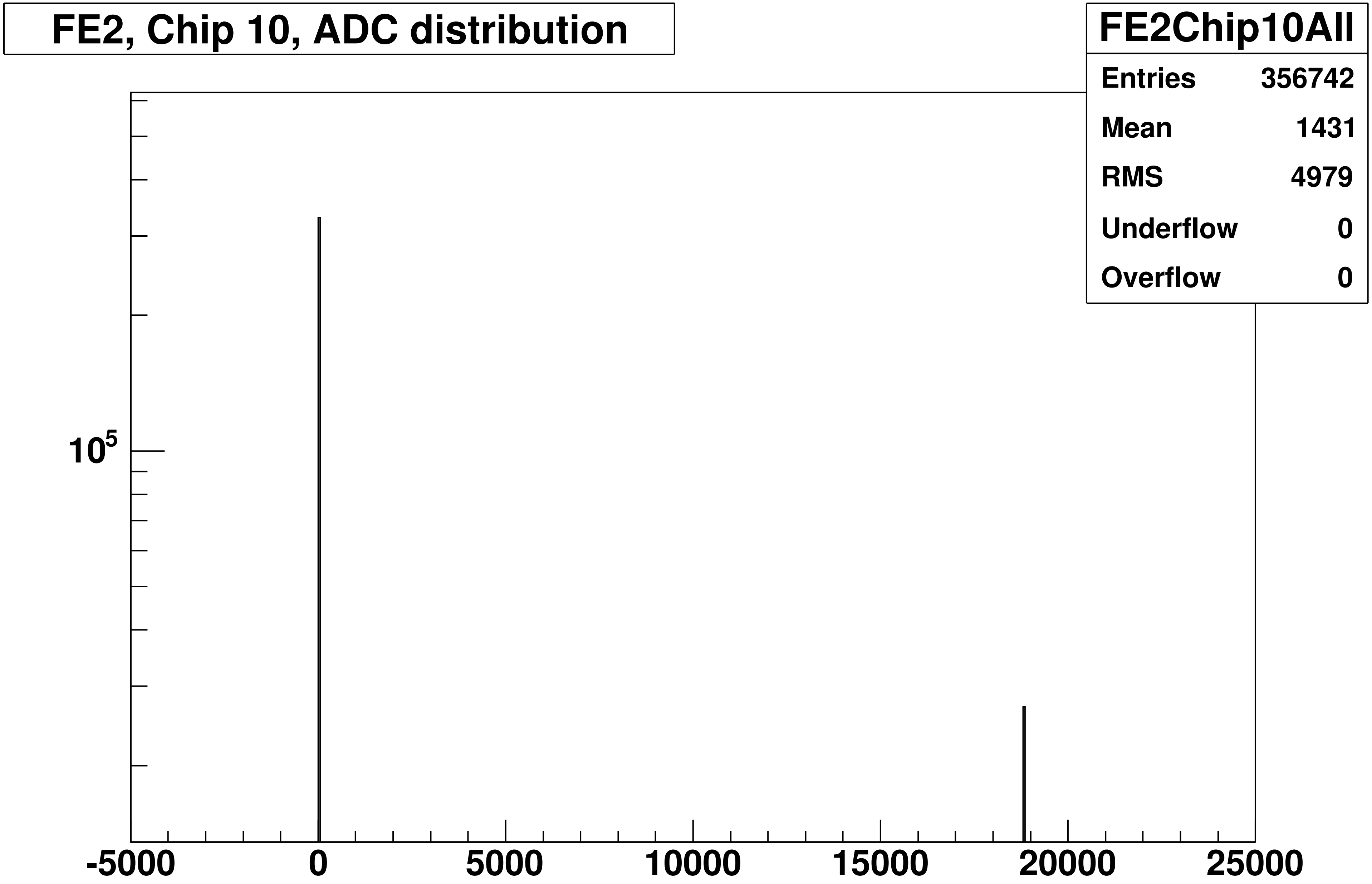
-150
-100
-50
0
50
100
150
200


FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 356742
Mean 1.863e+04
RMS 6.089
Underflow 3.297e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 356742
Mean 1431
RMS 4979
Underflow 0
Overflow 0
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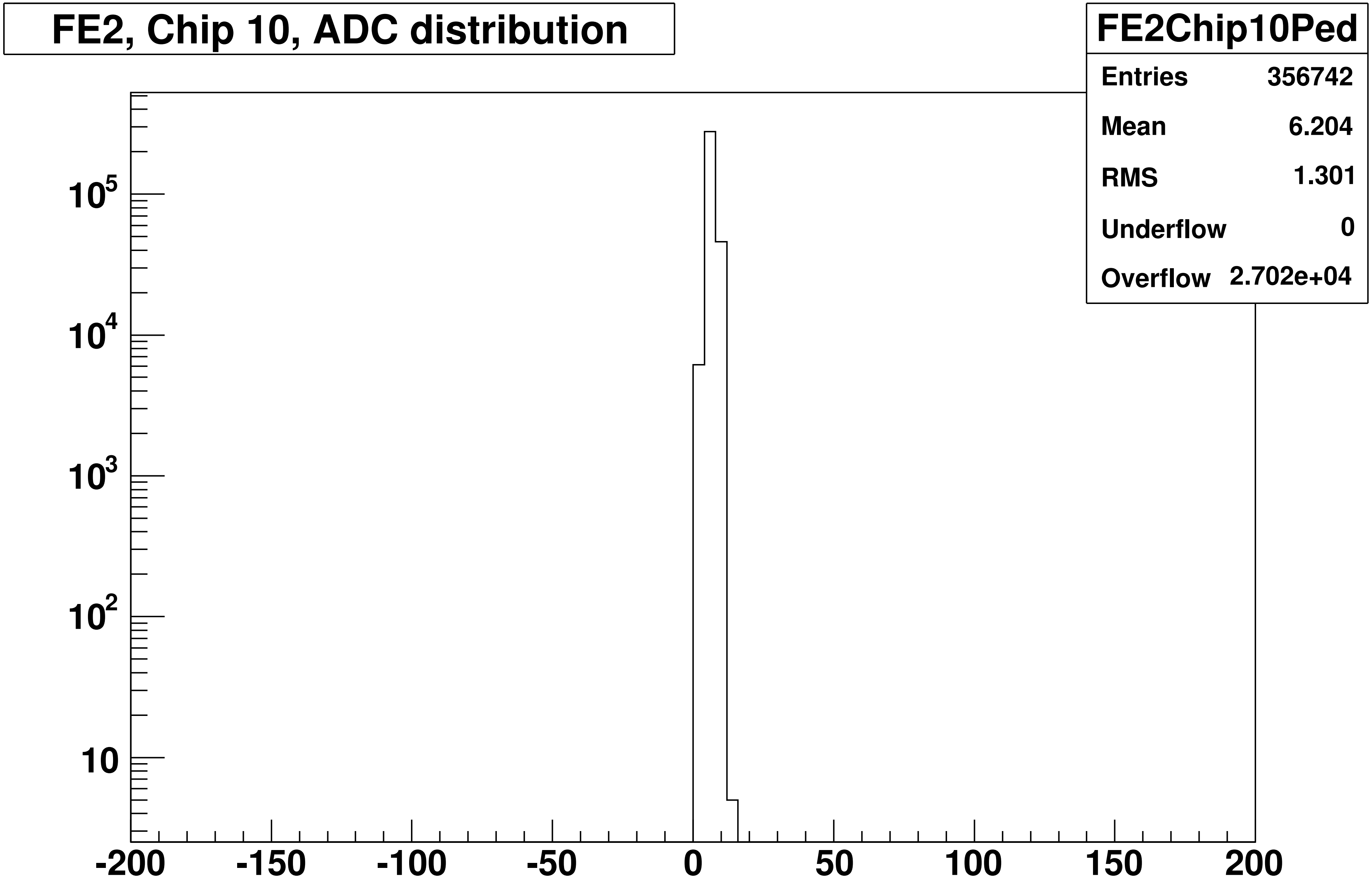
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 356742
Mean 6.204
RMS 1.301
Underflow 0
Overflow 2.702e+04
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10^4
10^3
10^2
10
-200
-150
-100
-50
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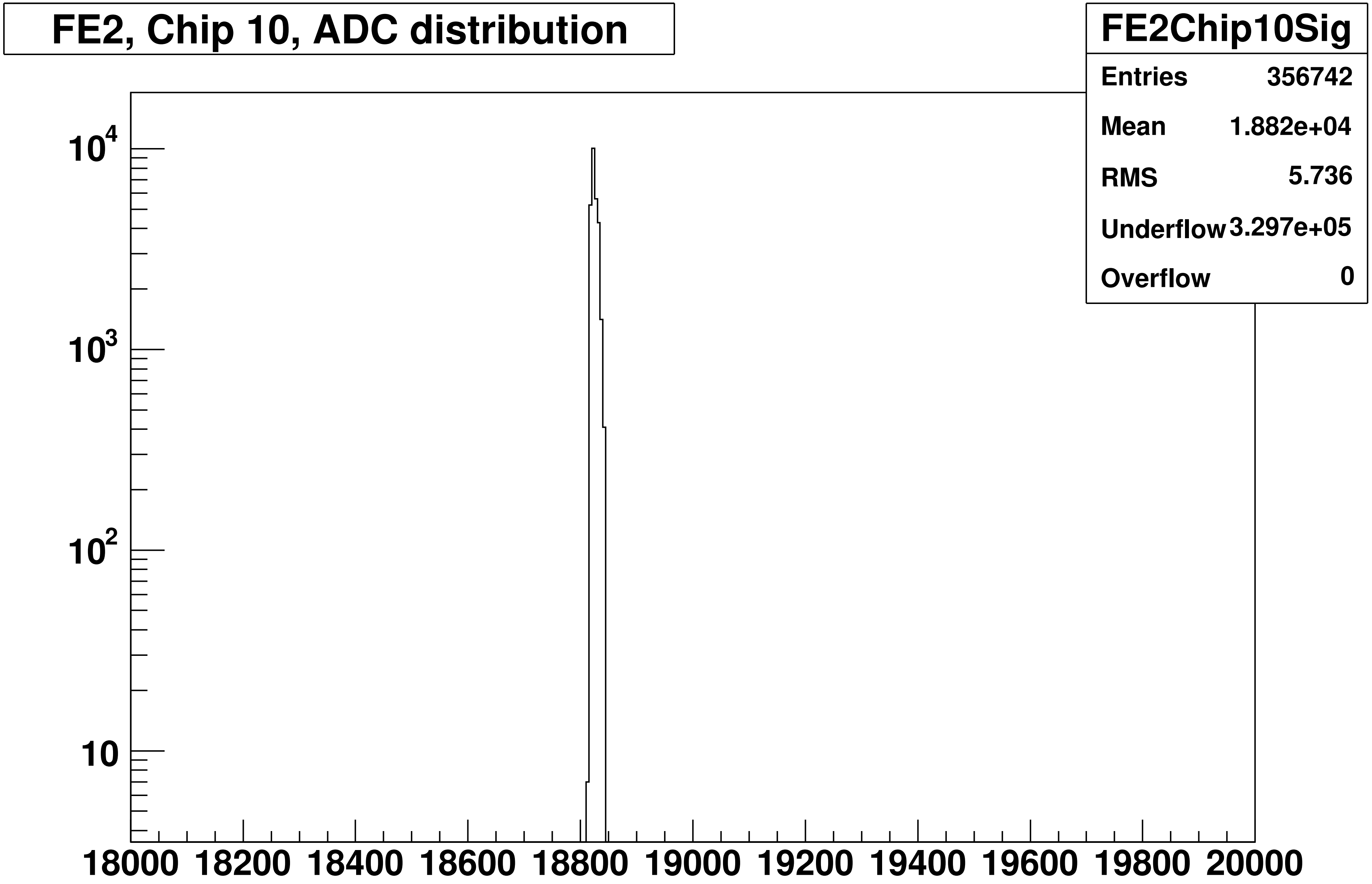
50
100
150
200


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 356742
Mean 1.882e+04
RMS 5.736
Underflow 3.297e+05
Overflow 0
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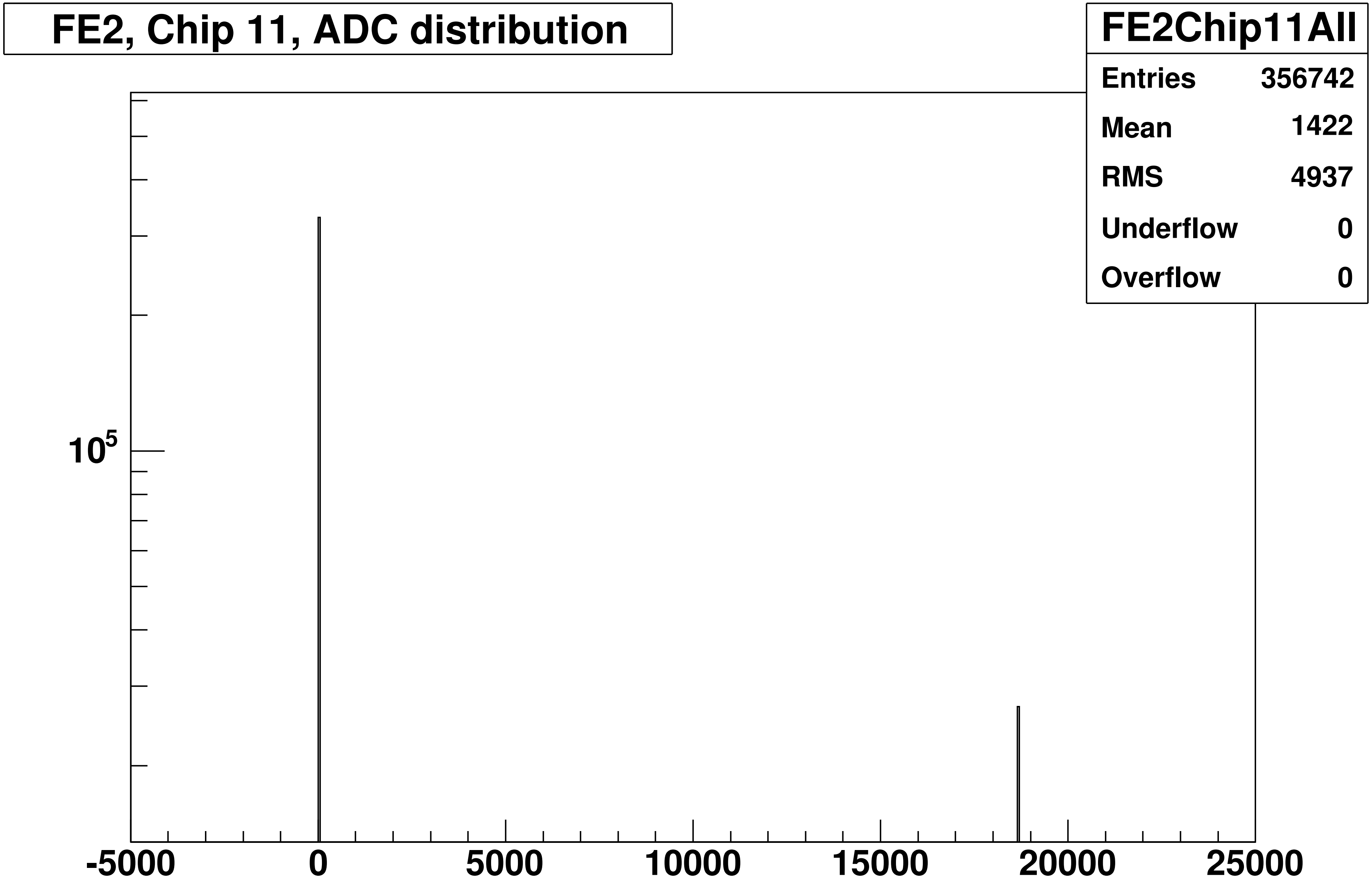
10^3
10^2
10
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 356742
Mean 1422
RMS 4937
Underflow 0
Overflow 0
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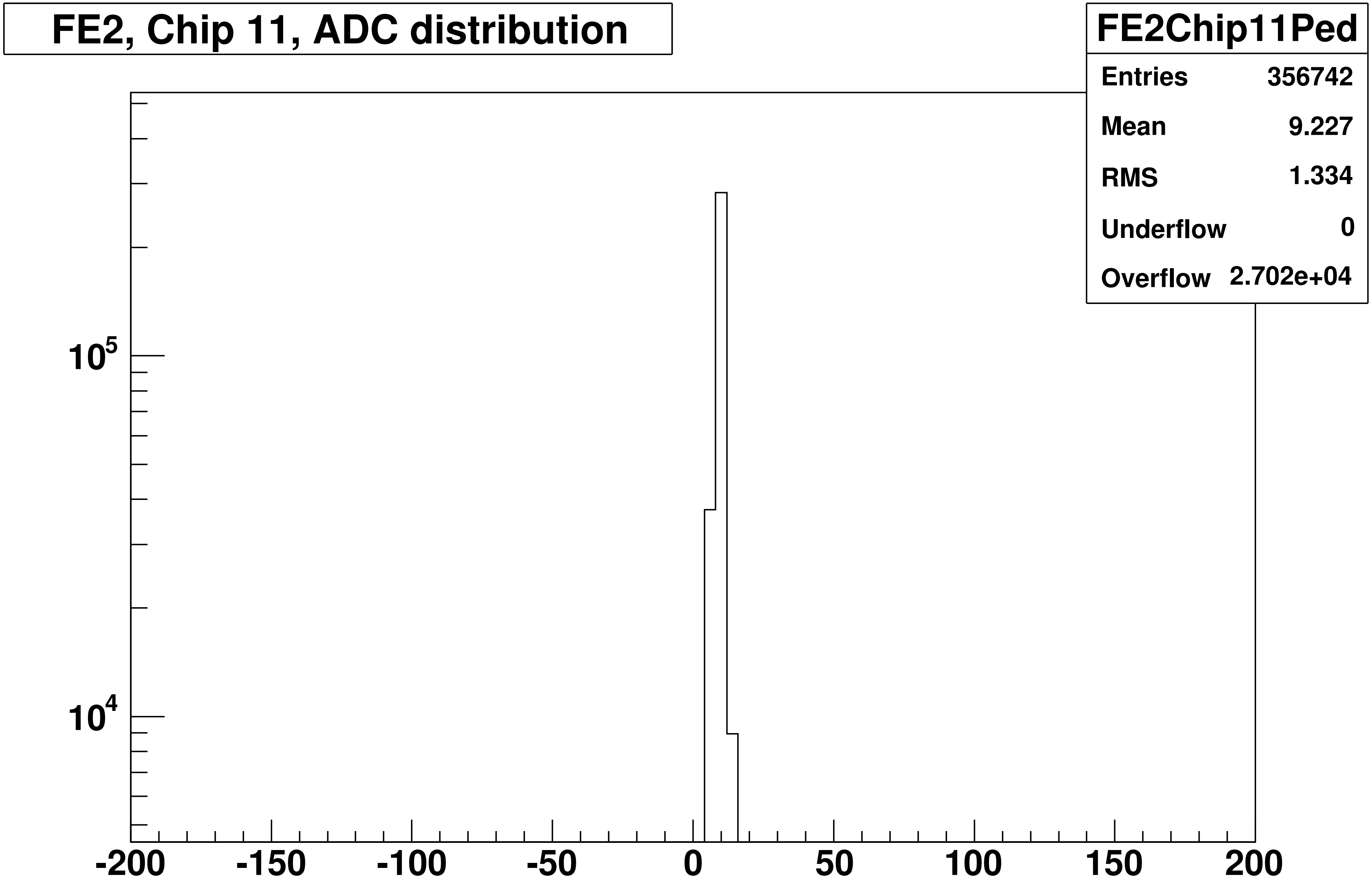
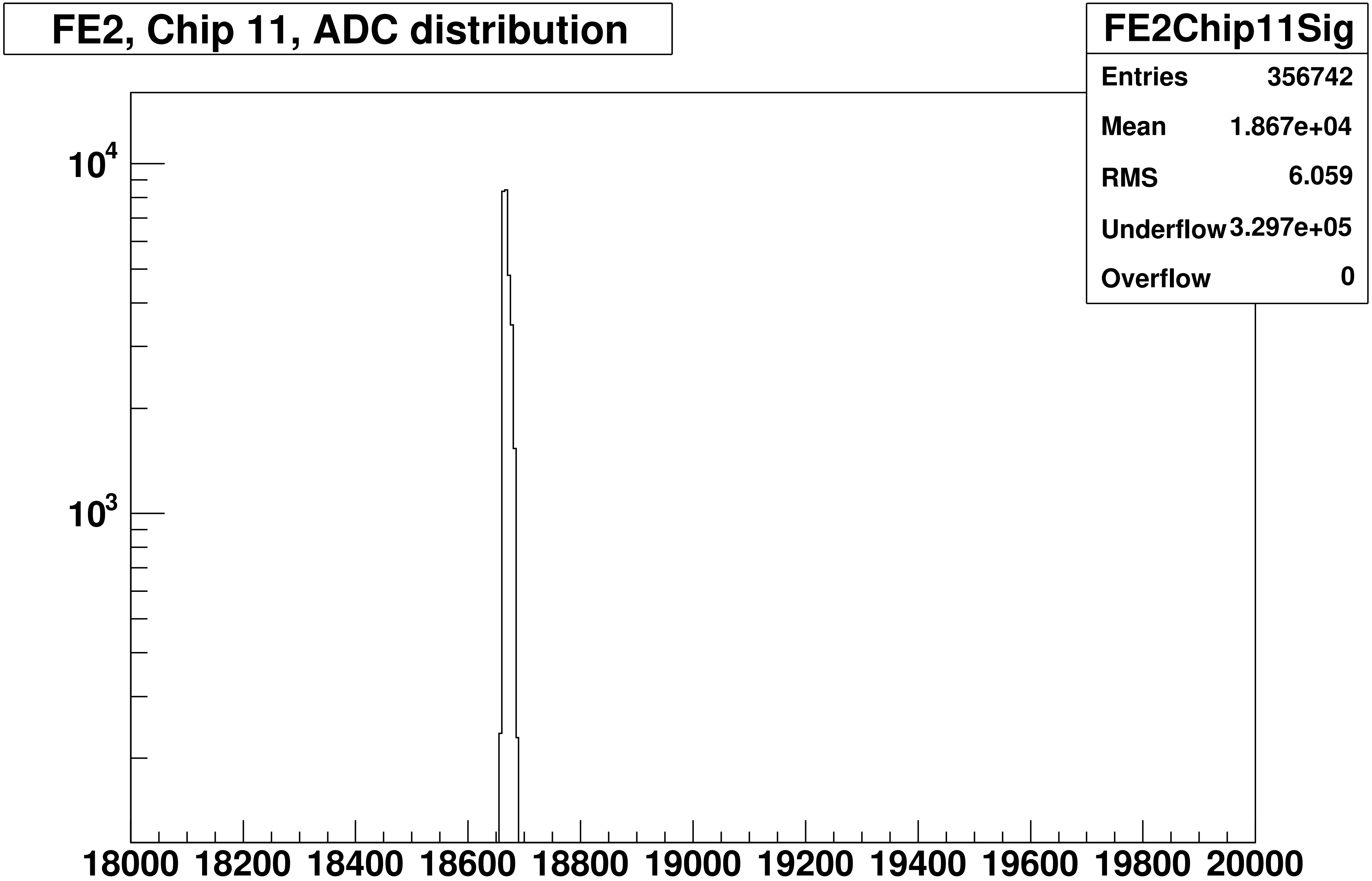
15000
20000
25000


FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 356742
Mean 9.227
RMS 1.334
Underflow 0
Overflow 2.702e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 356742
Mean 1.867e+04
RMS 6.059
Underflow 3.297e+05
Overflow 0
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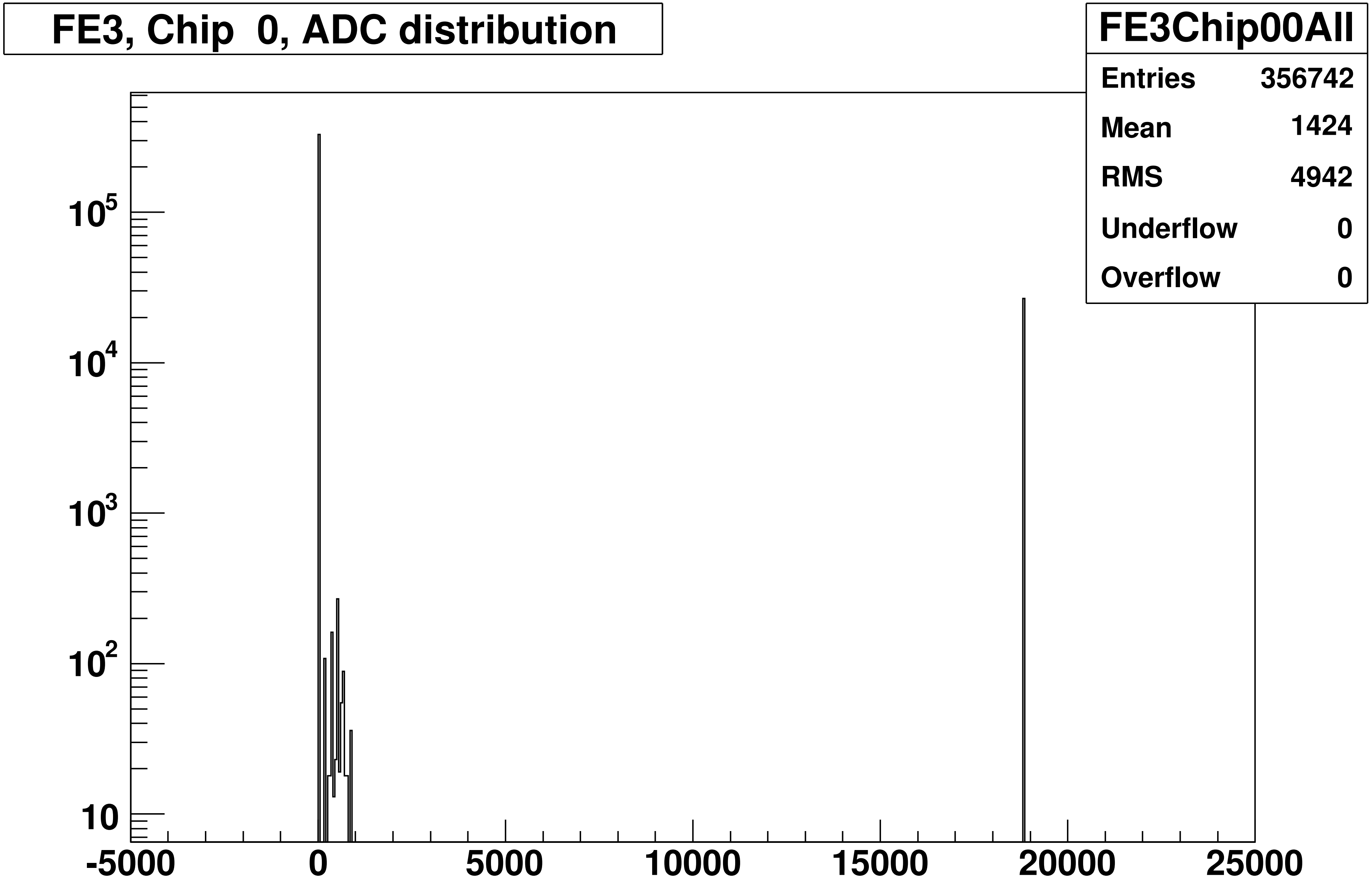
10^3
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 356742
Mean 1424
RMS 4942
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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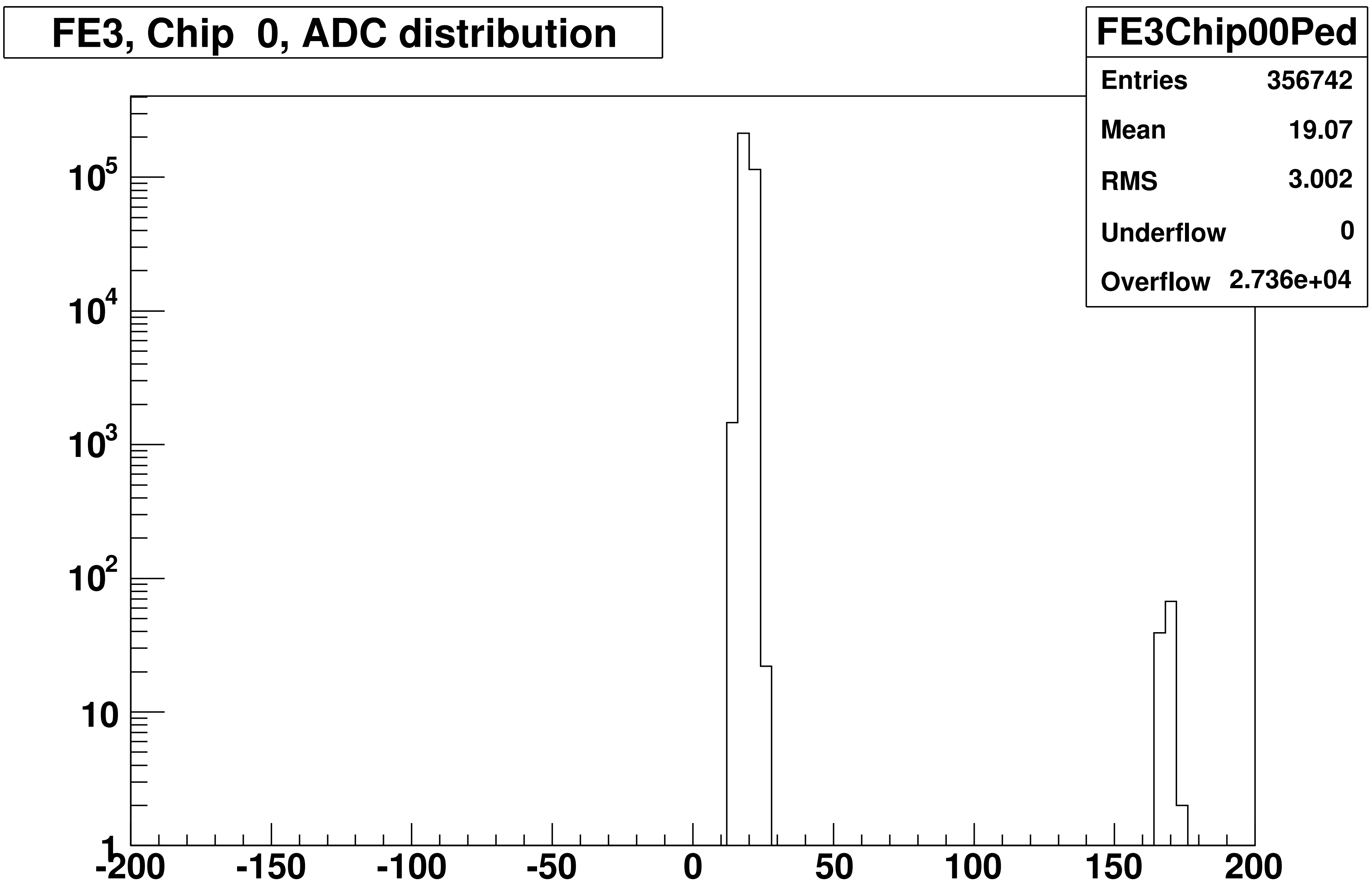
0
5000
10000
15000
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 356742
Mean 19.07
RMS 3.002
Underflow 0
Overflow 2.736e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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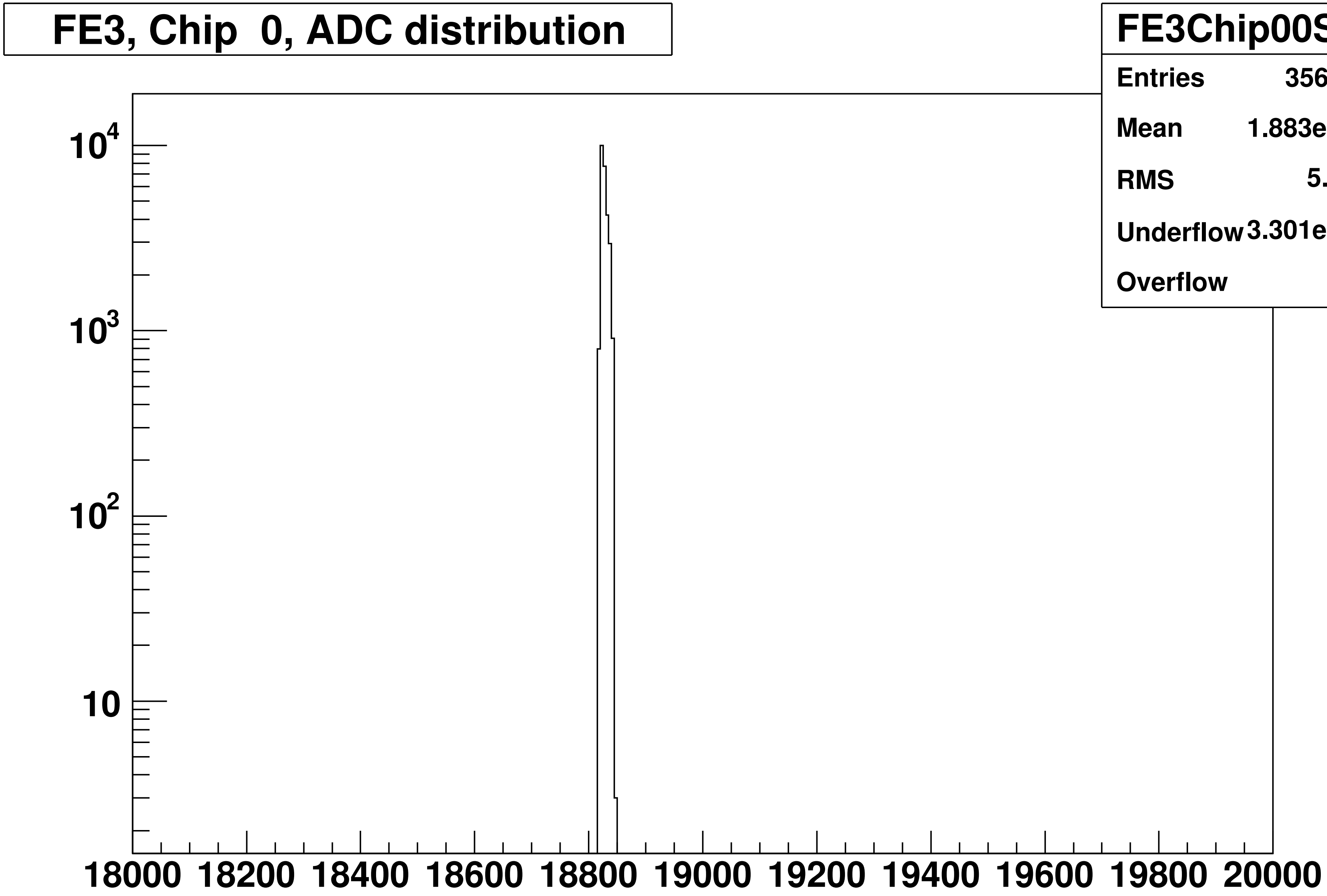
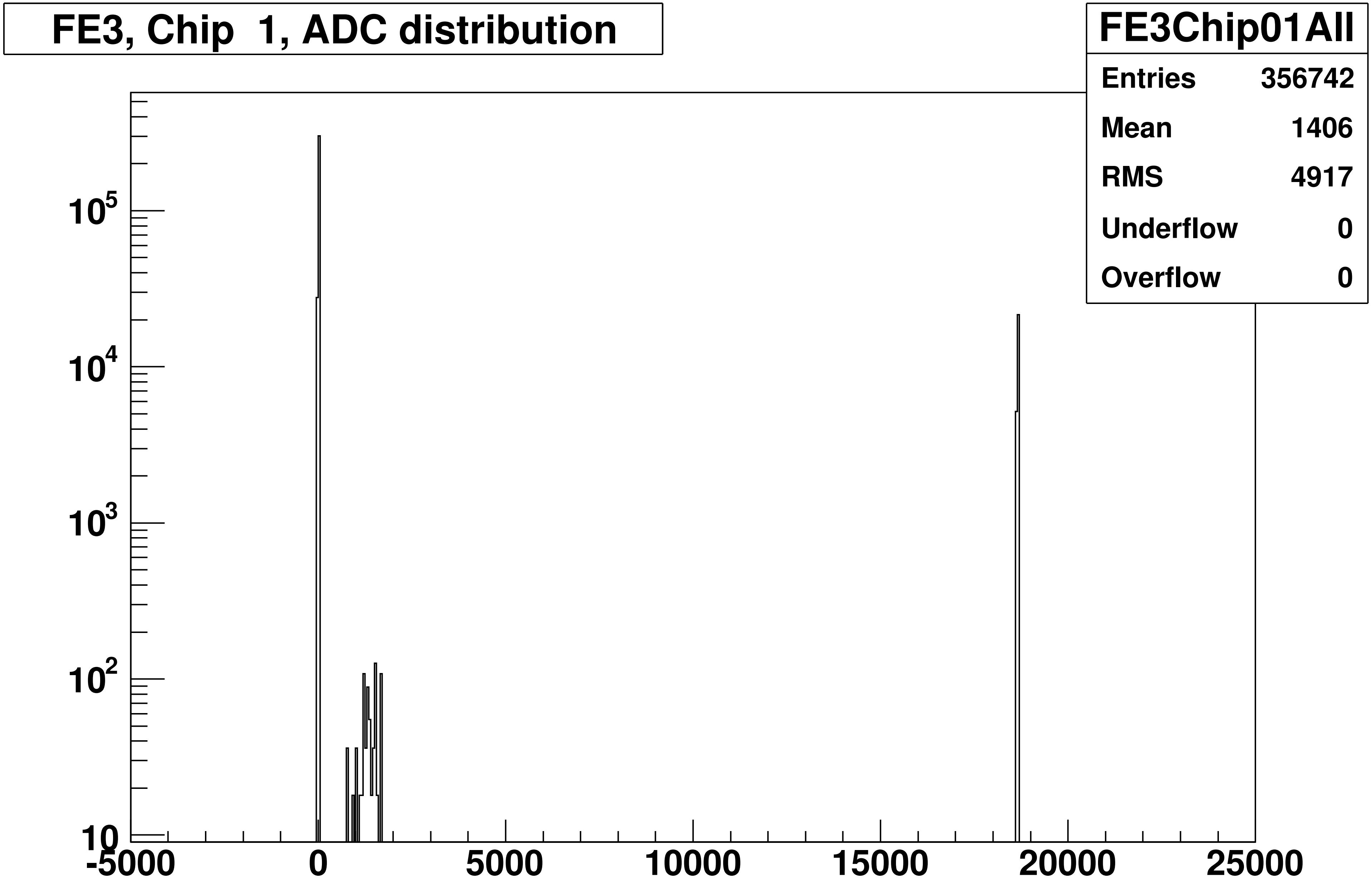
0
50
100
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 356742
Mean 1.883e+04
RMS 5.722
Underflow 3.301e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 356742
Mean 1406
RMS 4917
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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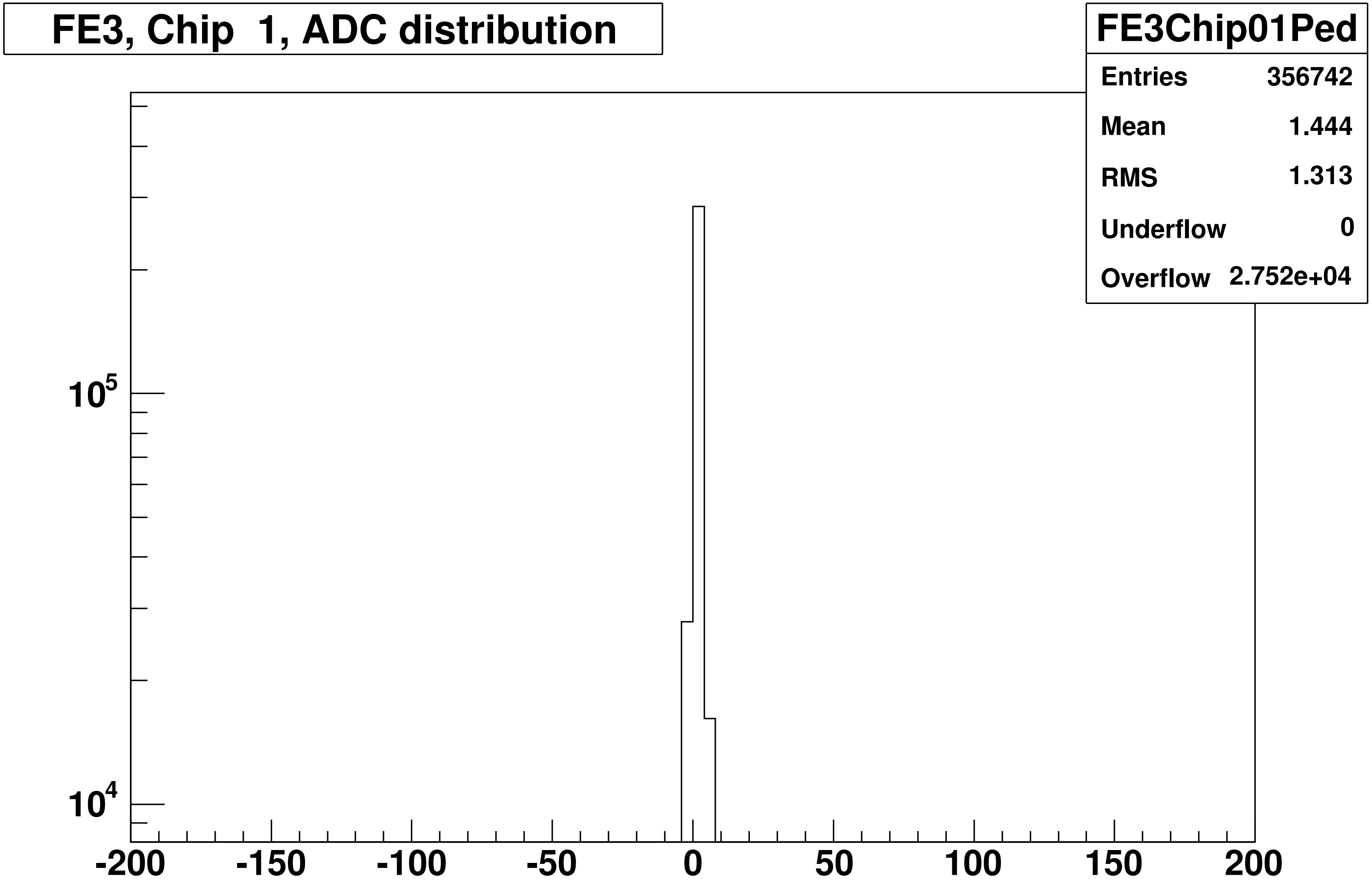
0
5000
10000
15000
20000
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 356742
Mean 1.444
RMS 1.313
Underflow 0
Overflow 2.752e+04
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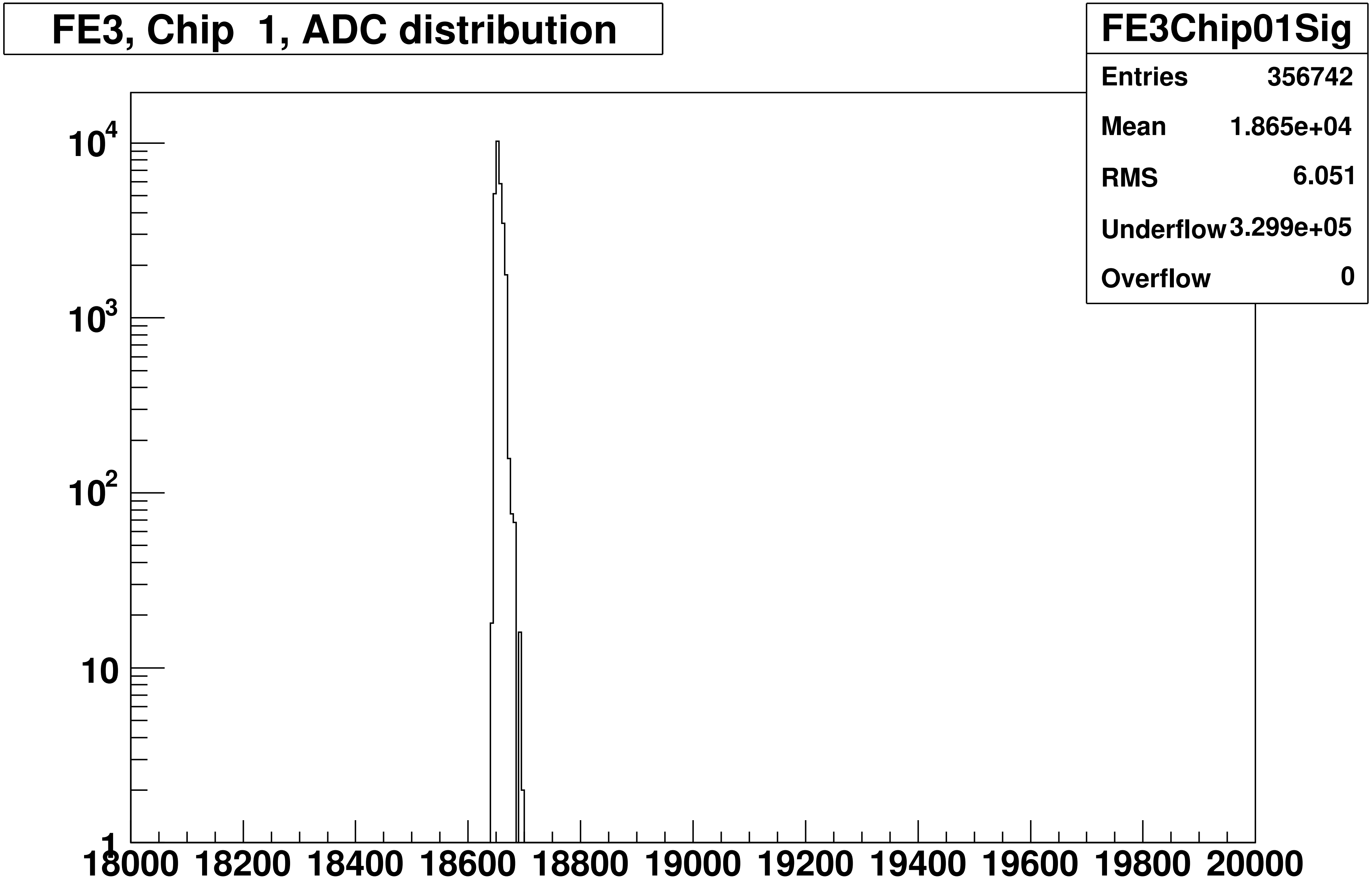
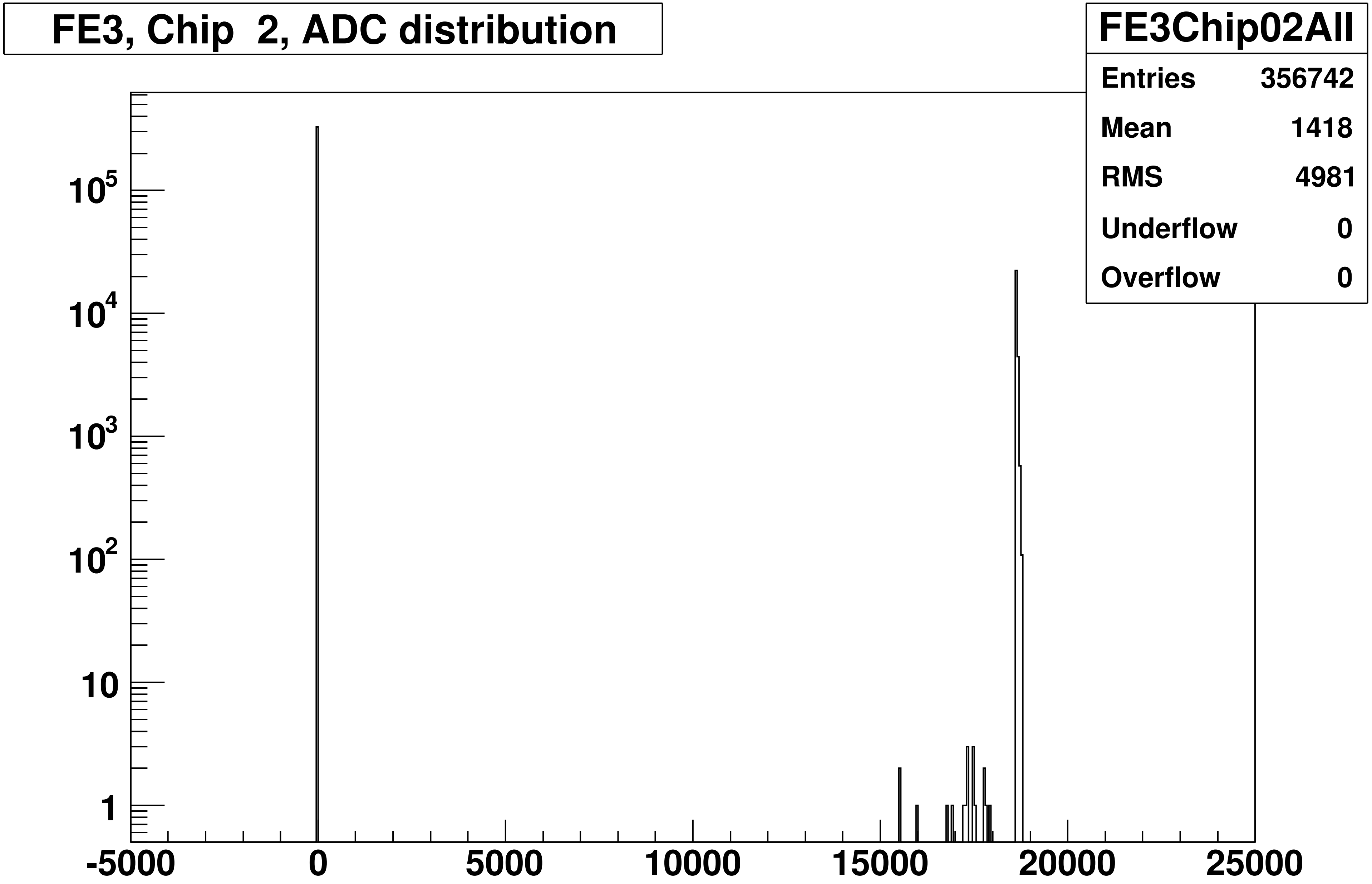
10^4
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 356742
Mean 1.865e+04
RMS 6.051
Underflow 3.299e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 356742
Mean 1418
RMS 4981
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
10000
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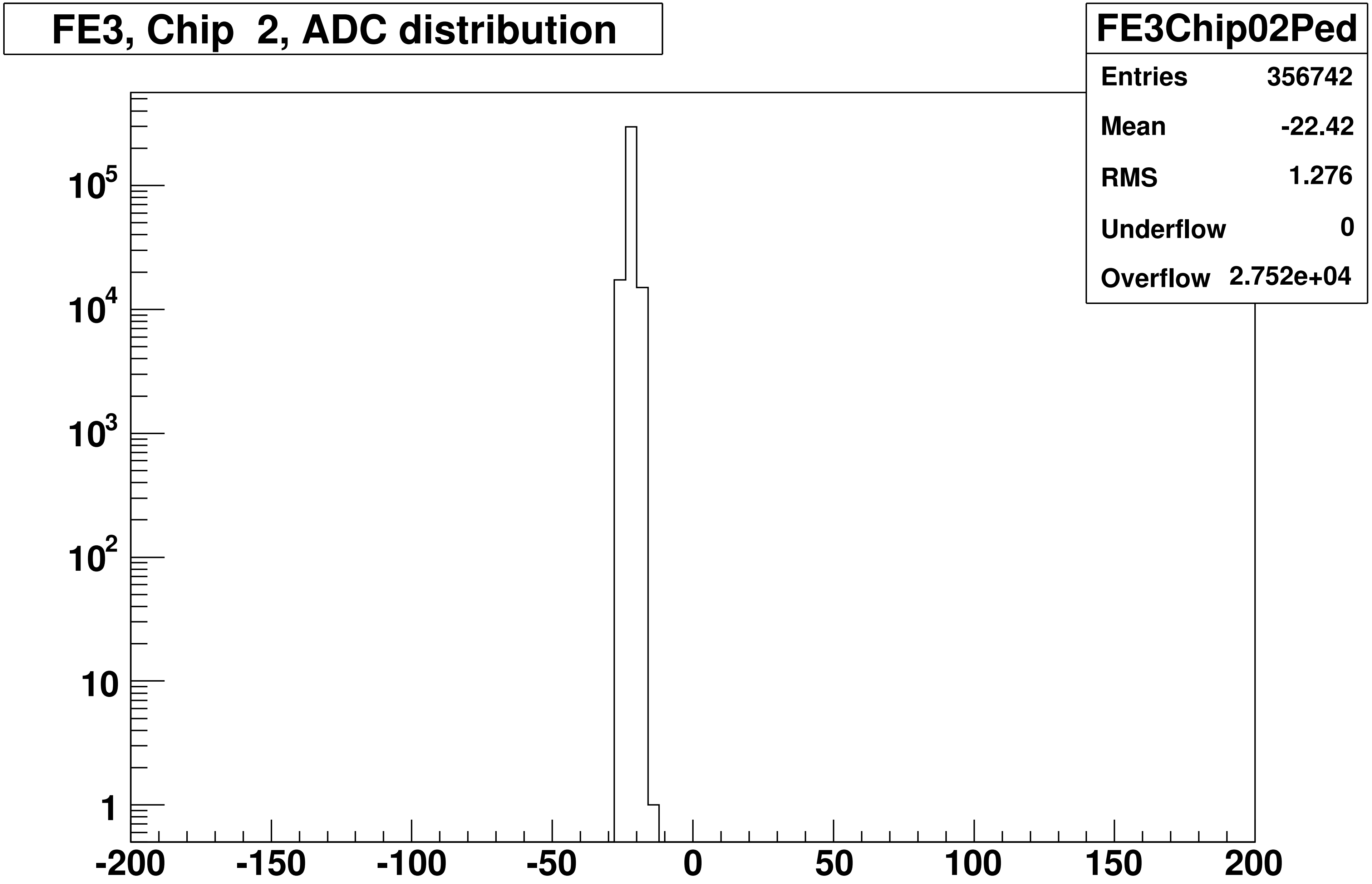
25000


FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 356742
Mean -22.42
RMS 1.276
Underflow 0
Overflow 2.752e+04
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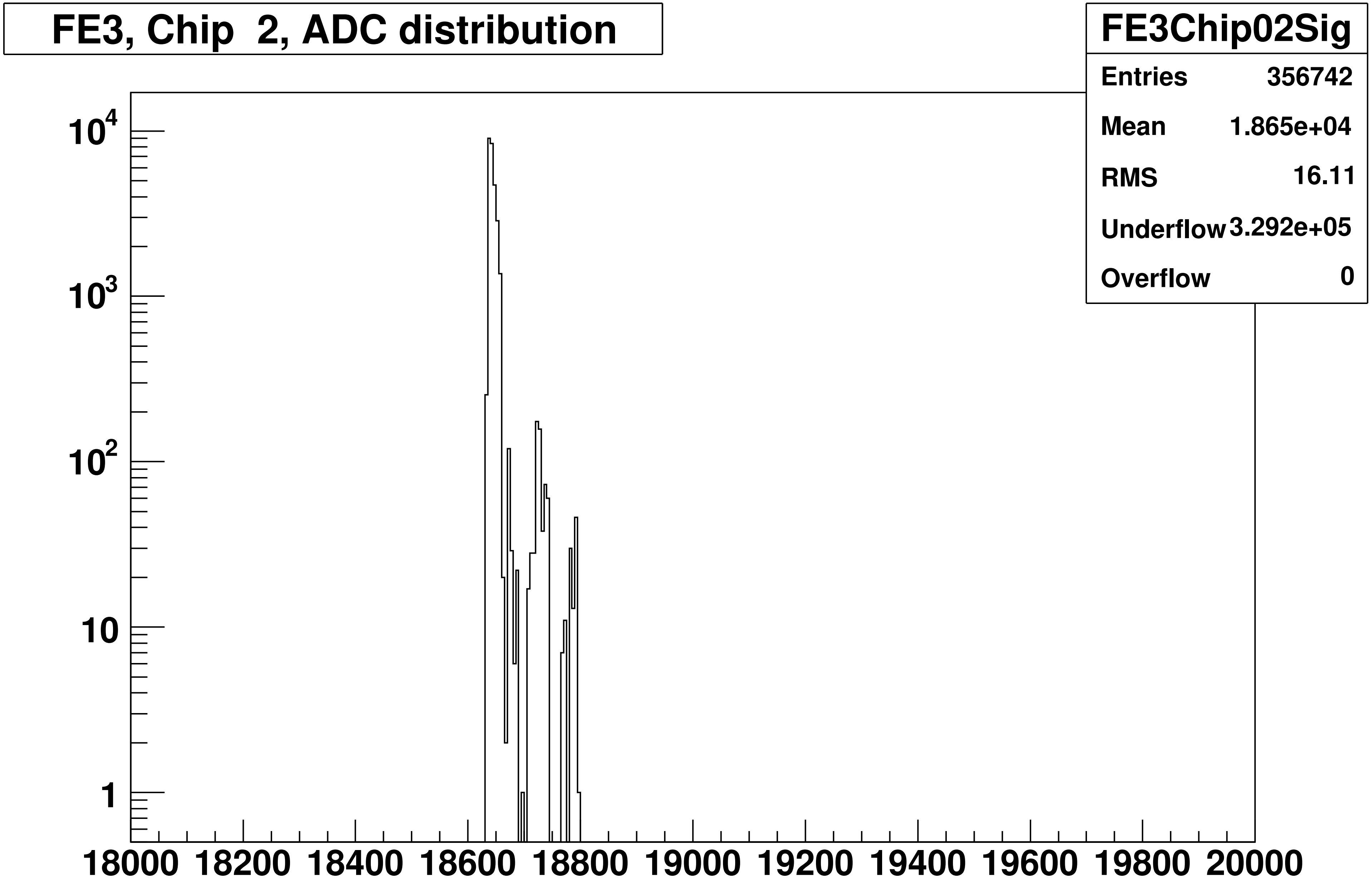
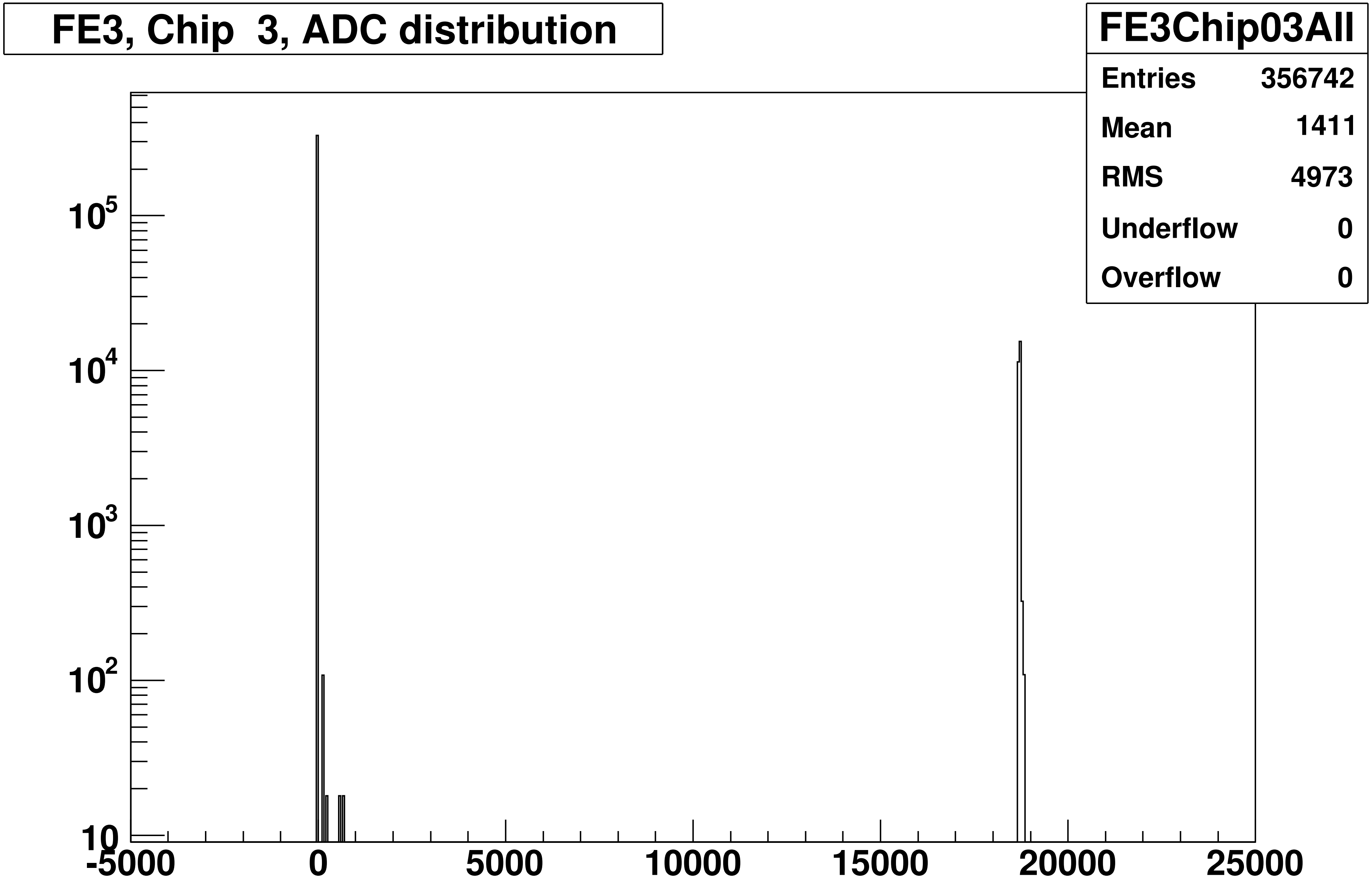
10^4
10^3
10^2
10
1
-200 -150 -100 -50 0 50 100 150 200


FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 356742
Mean 1.865e+04
RMS 16.11
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 356742
Mean 1411
RMS 4973
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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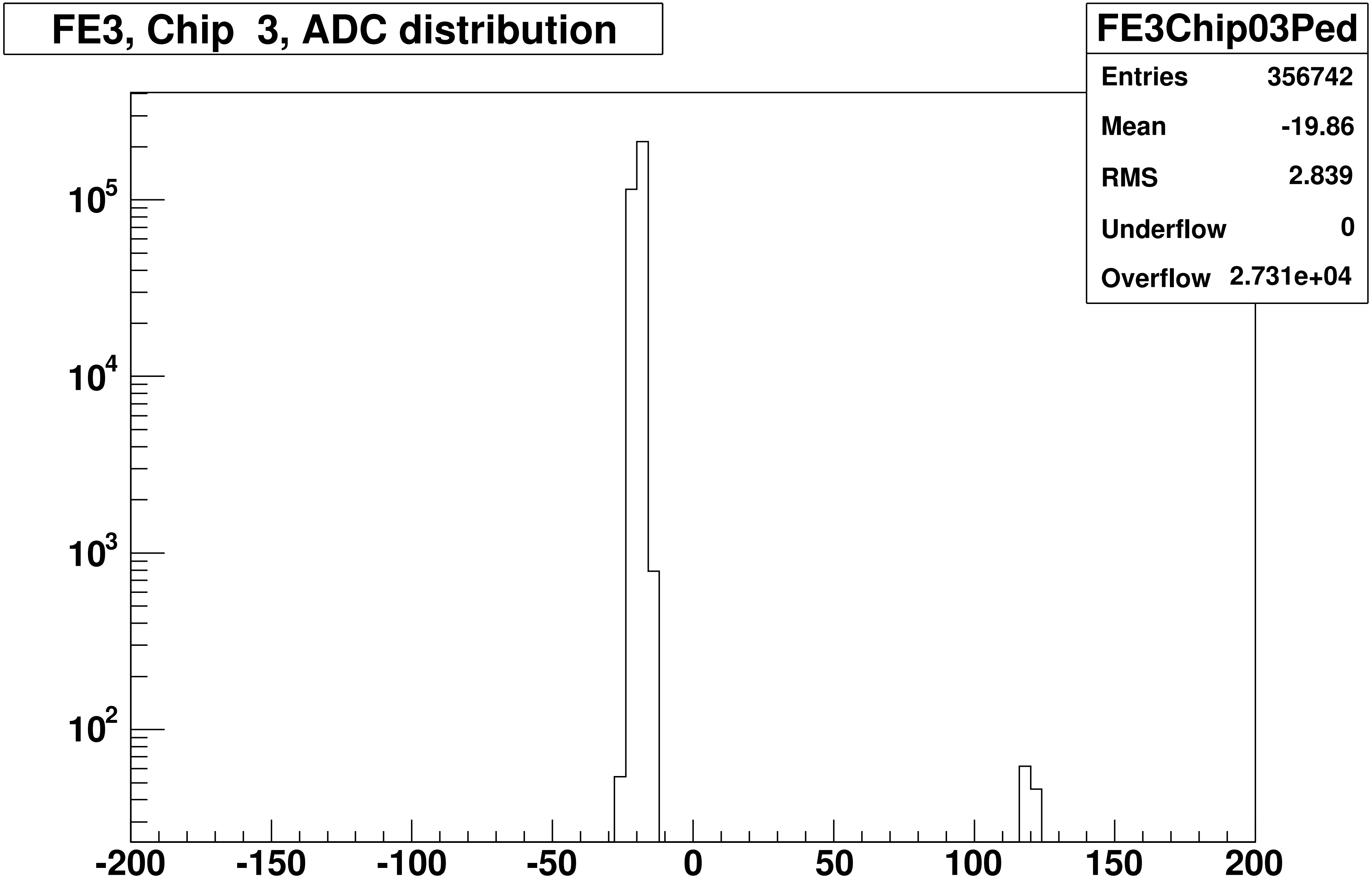
10000
15000
20000
25000


FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 356742
Mean -19.86
RMS 2.839
Underflow 0
Overflow 2.731e+04
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10^4
10^3
10^2
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-150
-100
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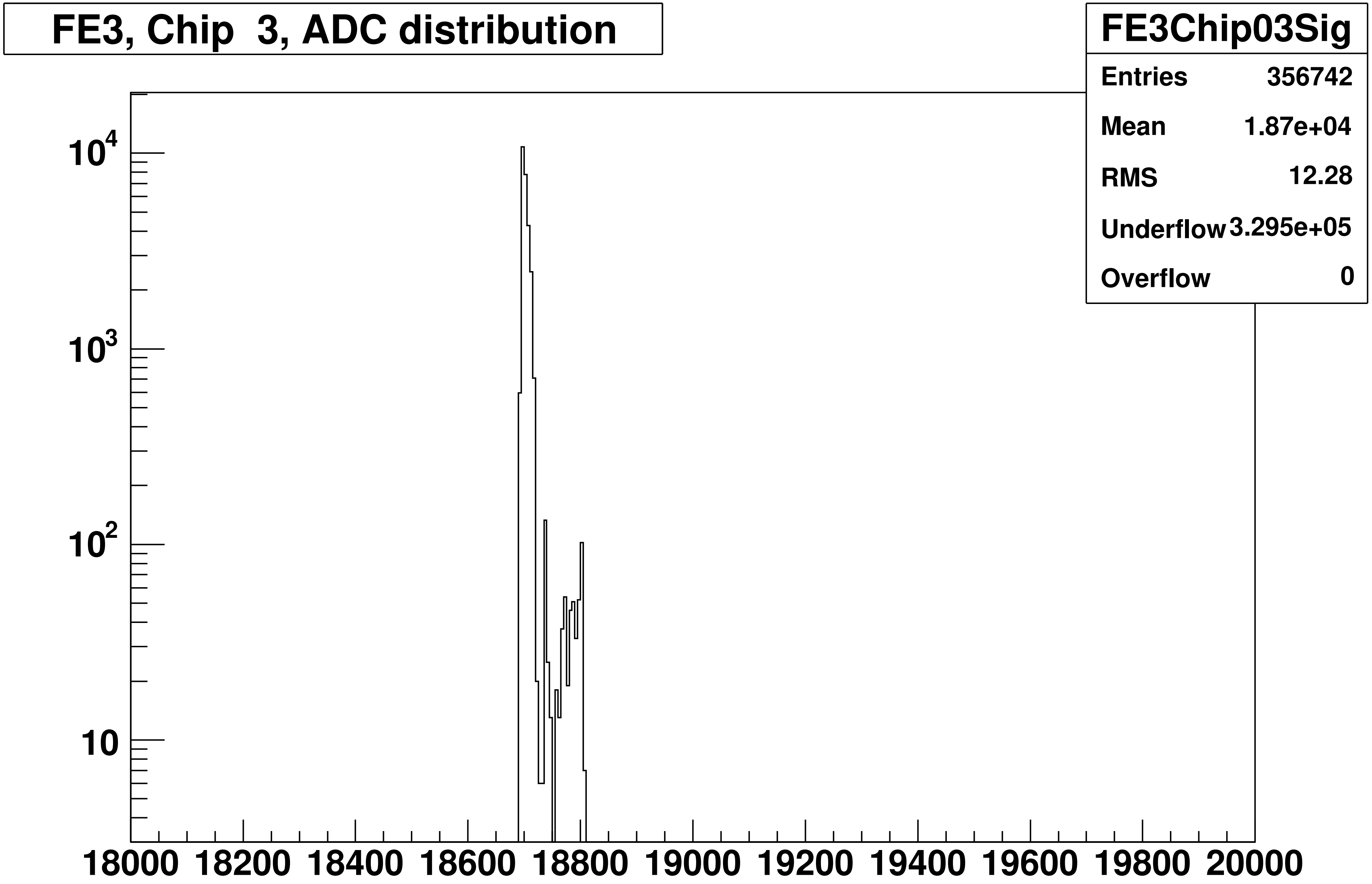
0
50
100
150
200


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 356742
Mean 1.87e+04
RMS 12.28
Underflow 3.295e+05
Overflow 0
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10^3
10^2
10
18000
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18400
18600
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19000
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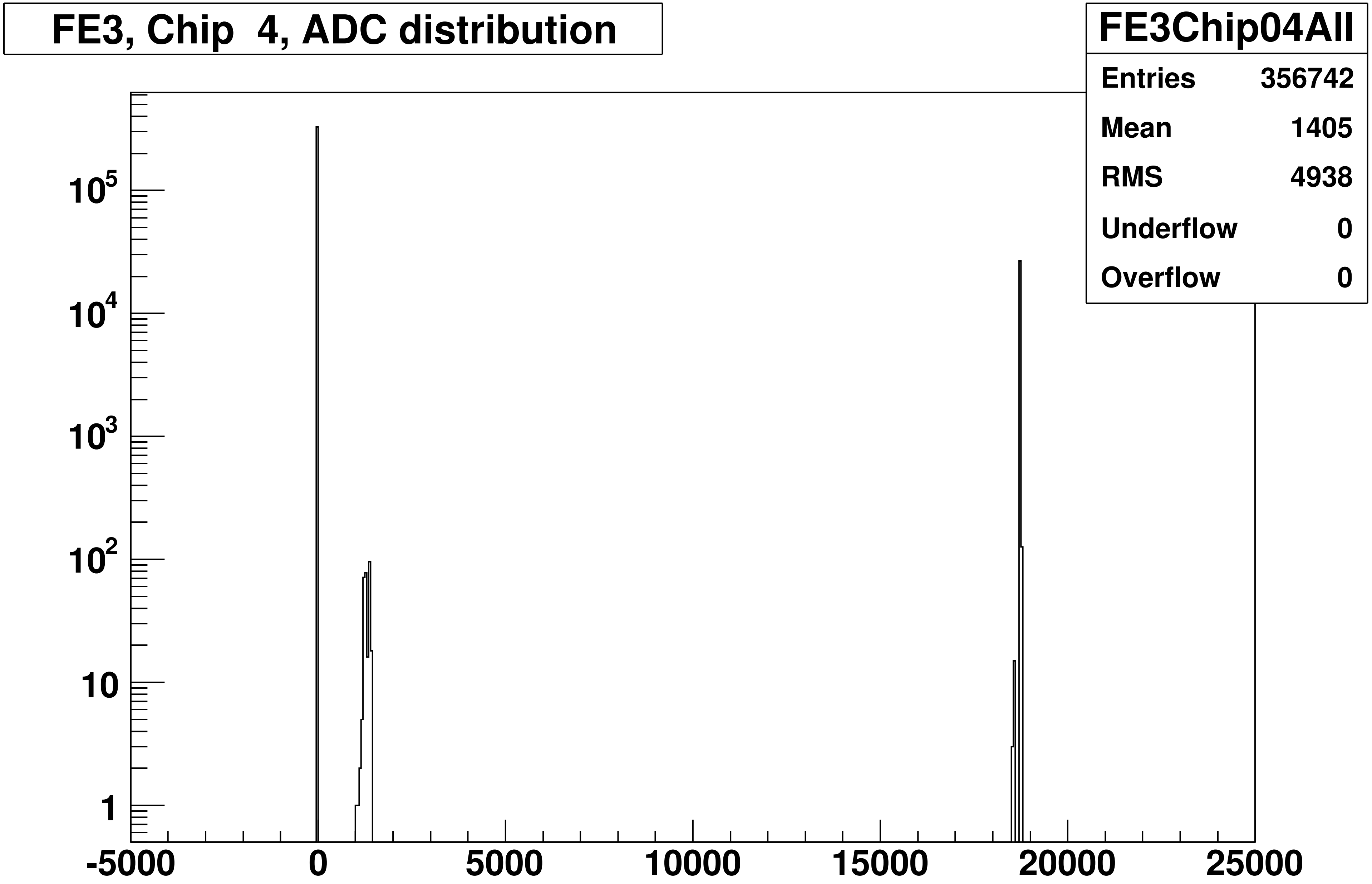
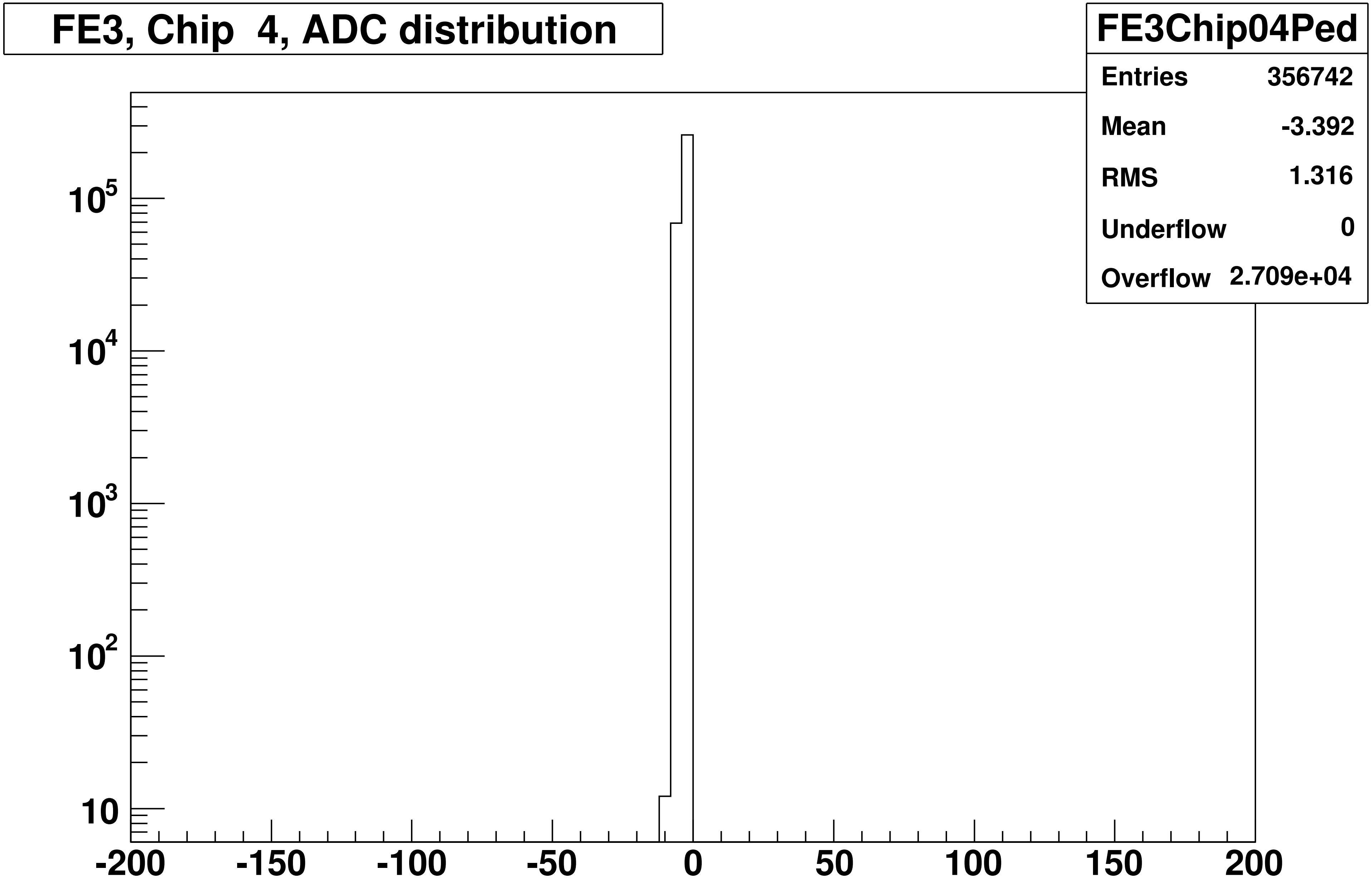
19600
19800
20000


FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 356742
Mean 1405
RMS 4938
Underflow 0
Overflow 0
1
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 356742
Mean -3.392
RMS 1.316
Underflow 0
Overflow 2.709e+04
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10^3
10^4
10^5
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150
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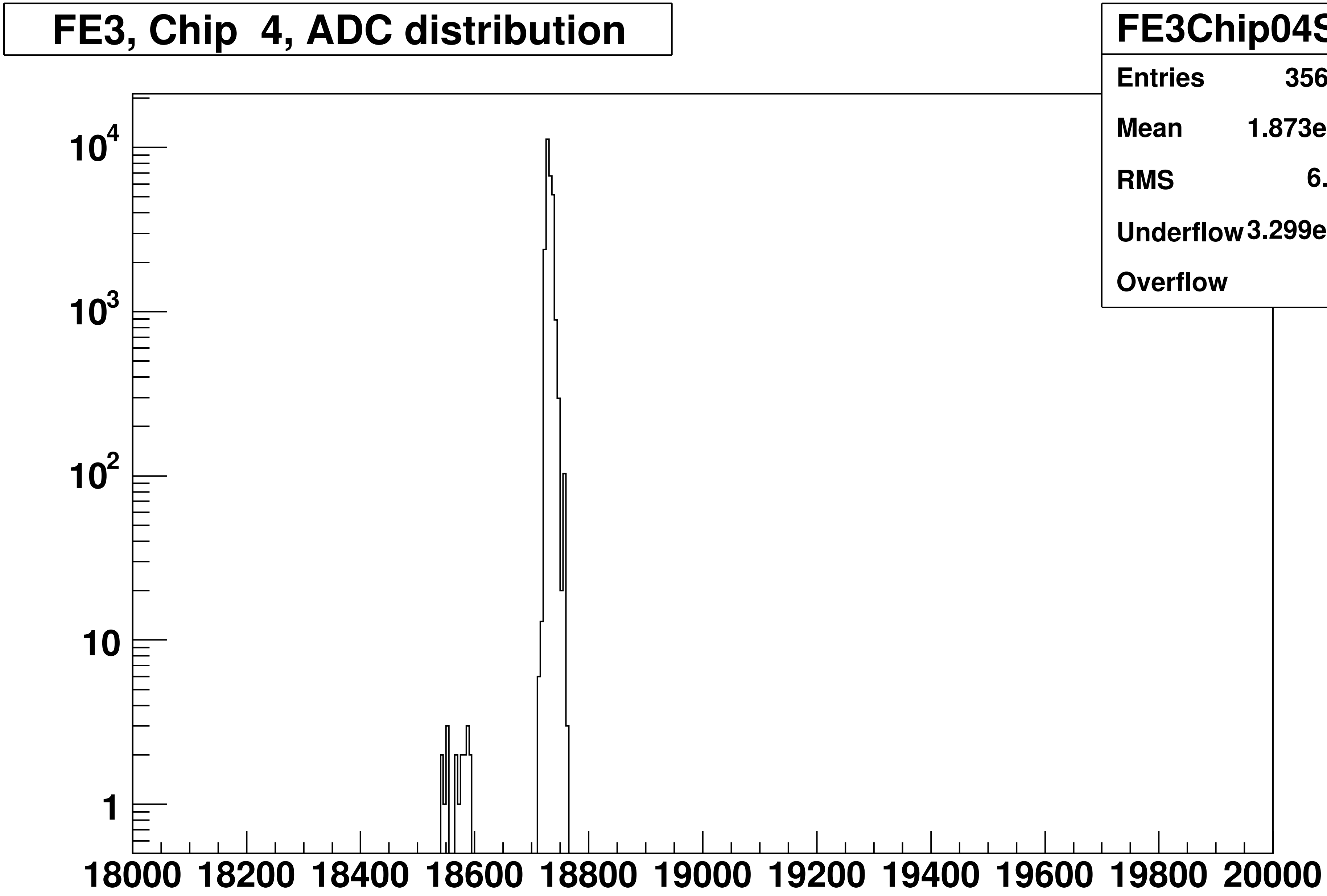
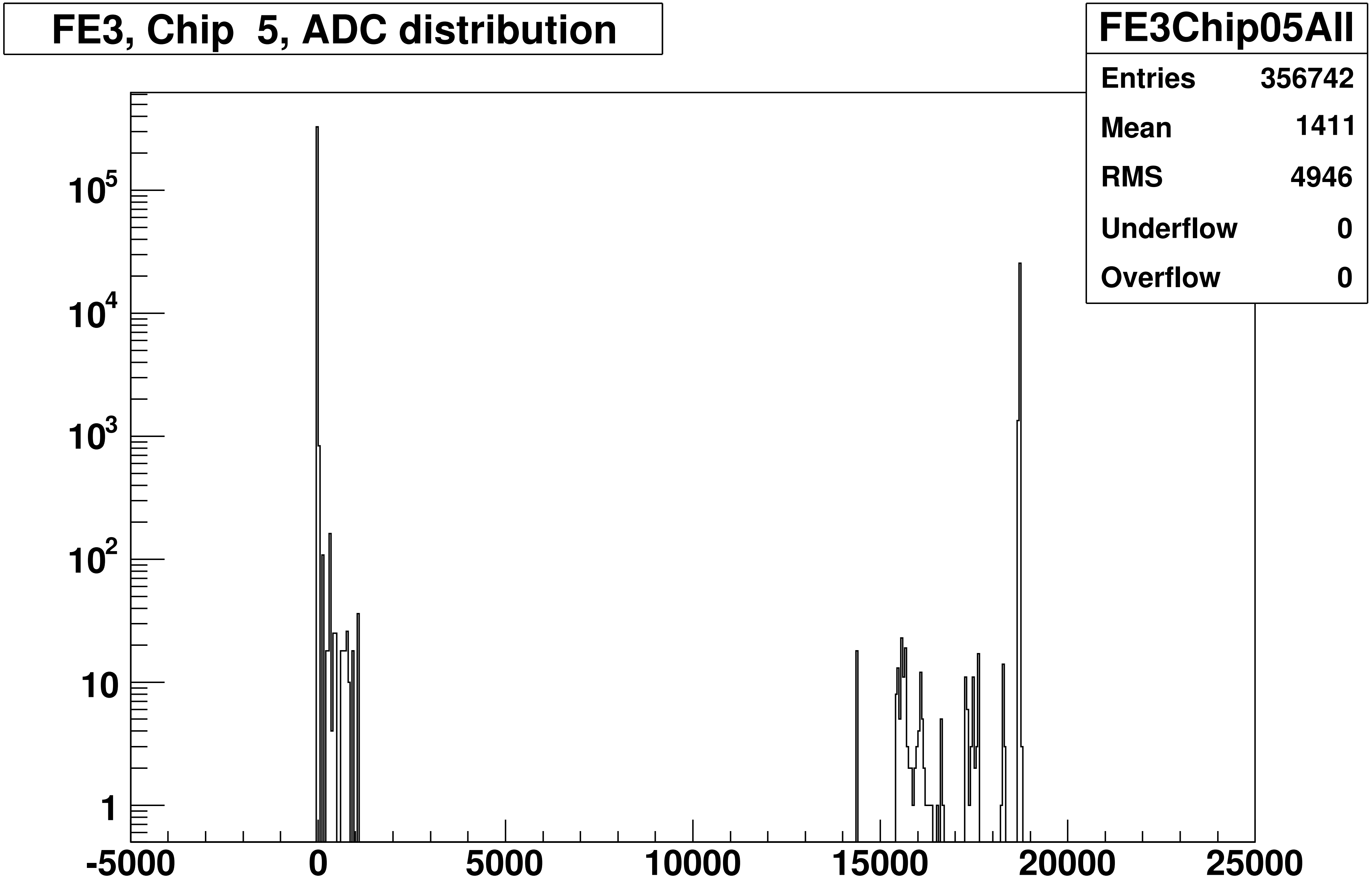


FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 356742
Mean 1.873e+04
RMS 6.847
Underflow 3.299e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 356742
Mean 1411
RMS 4946
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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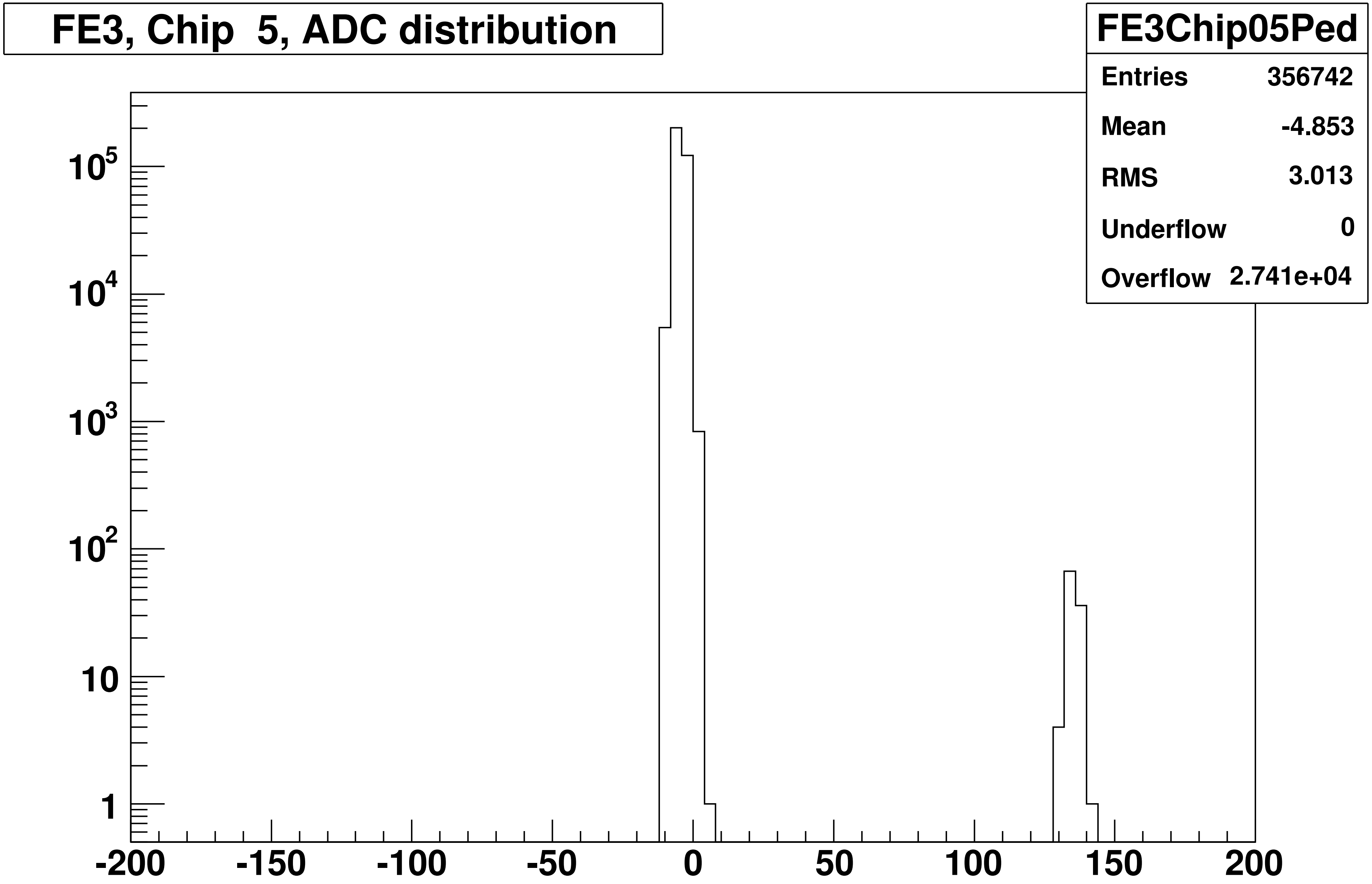
10000
15000
20000
25000


FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 356742
Mean -4.853
RMS 3.013
Underflow 0
Overflow 2.741e+04
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10^3
10^2
10
1
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-150
-100
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100
150
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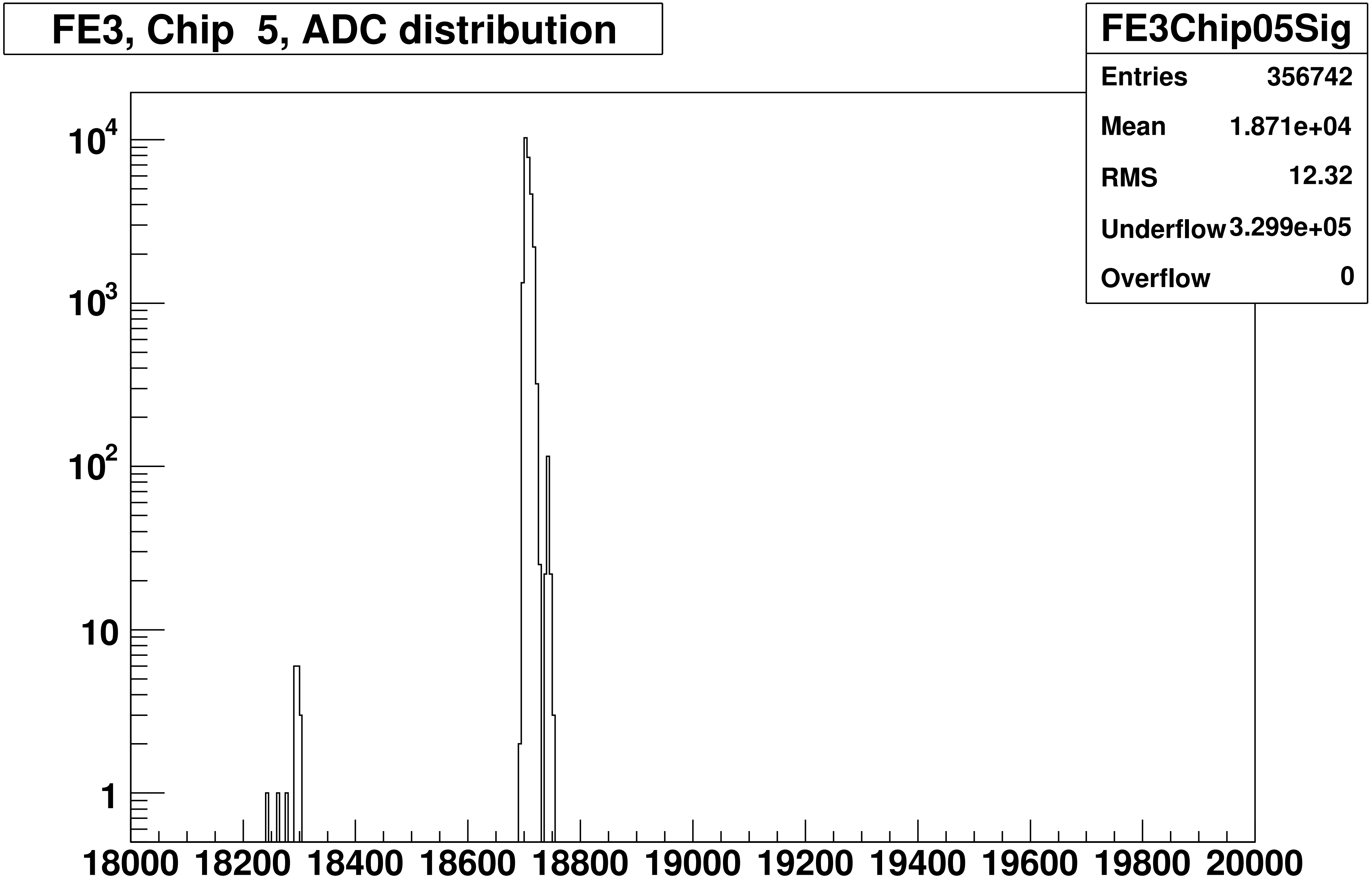
FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 356742
Mean 1.871e+04
RMS 12.32
Underflow 3.299e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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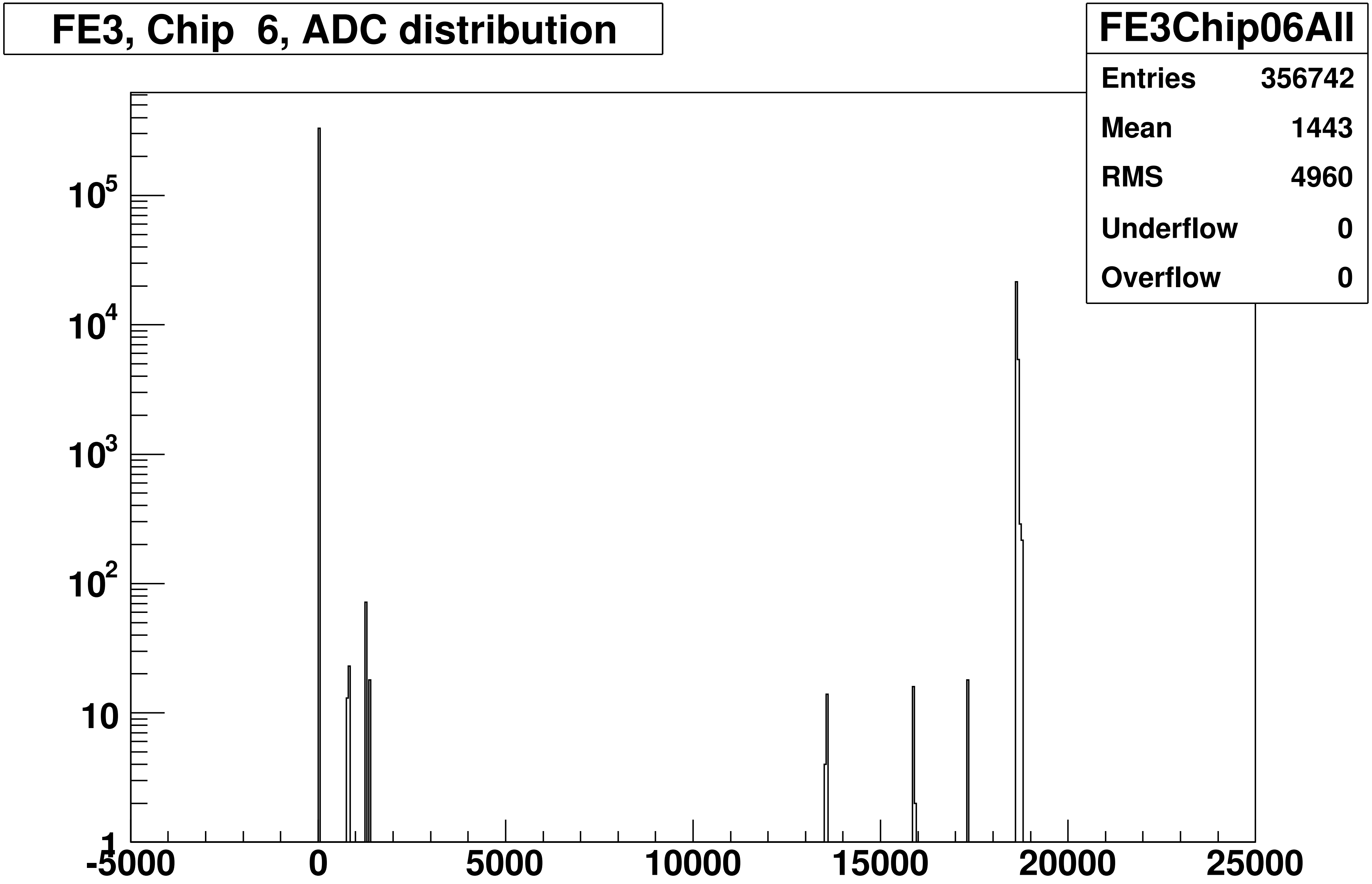
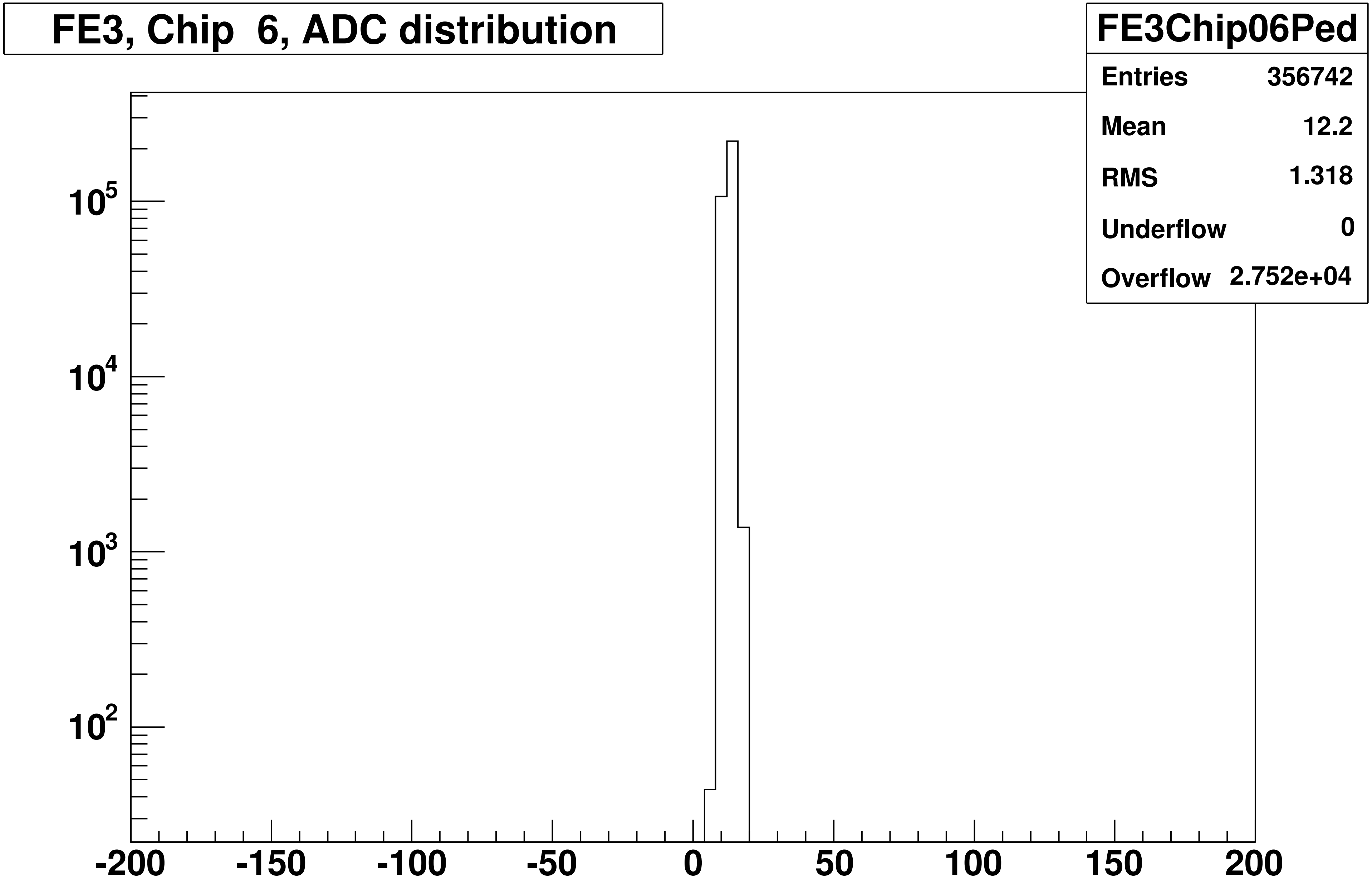
19400
19600
19800
20000



FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 356742
Mean 1443
RMS 4960
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 356742
Mean 12.2
RMS 1.318
Underflow 0
Overflow 2.752e+04
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10^4
10^3
10^2
-200
-150
-100
-50
0
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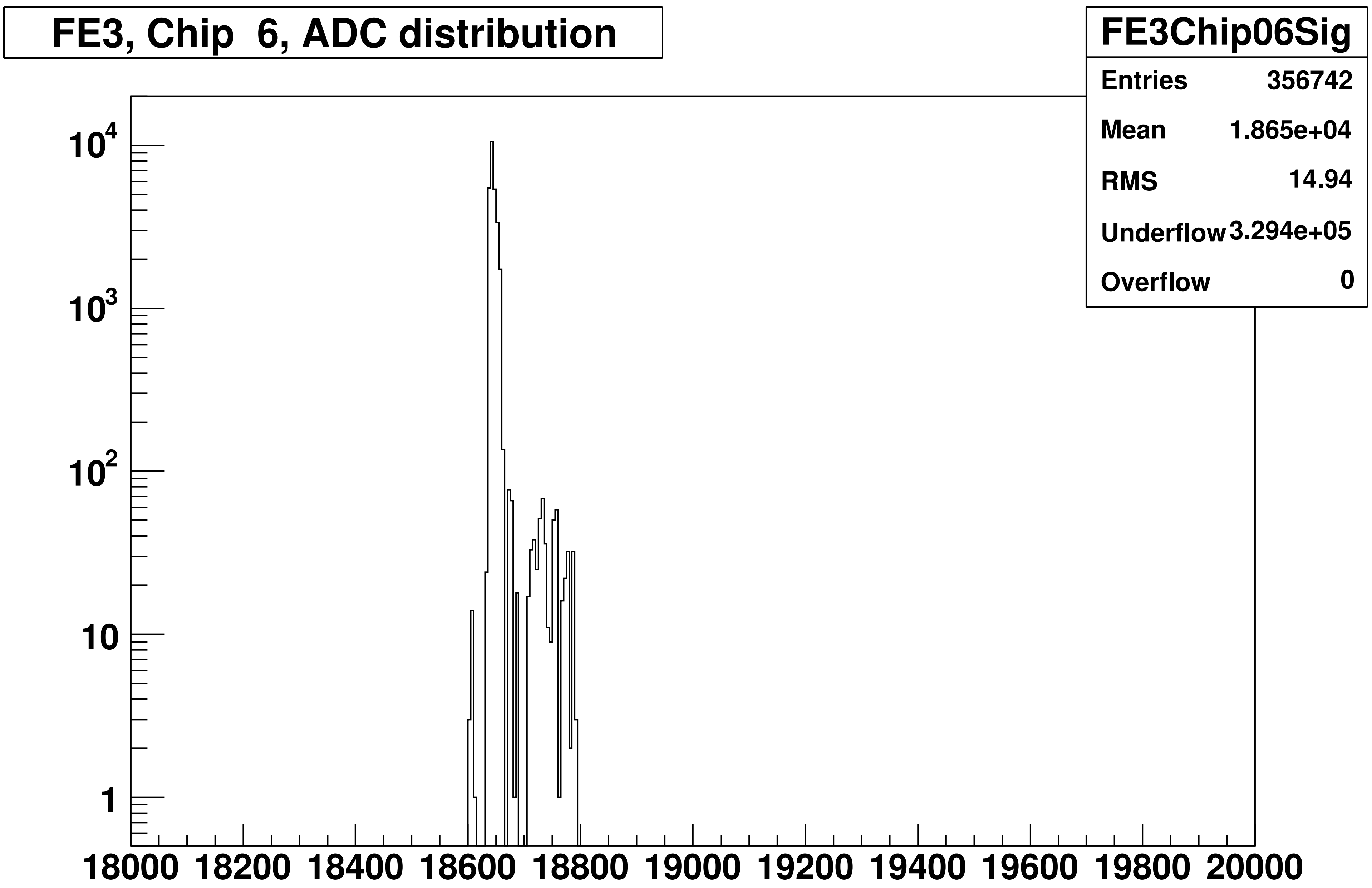
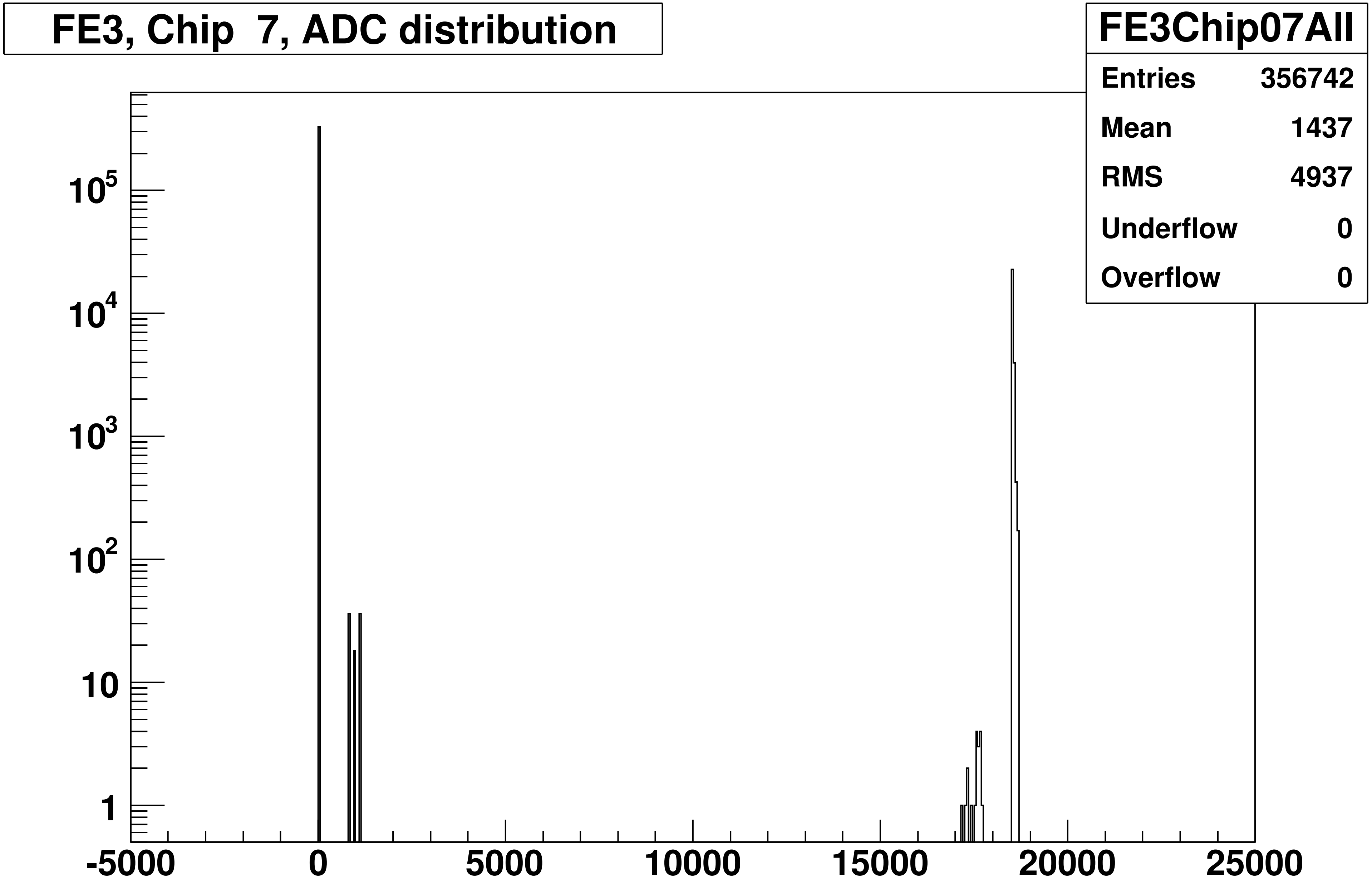
100
150
200


FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 356742
Mean 1.865e+04
RMS 14.94
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 356742
Mean 1437
RMS 4937
Underflow 0
Overflow 0
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10
10^2
10^3
10^4
10^5
-5000
0
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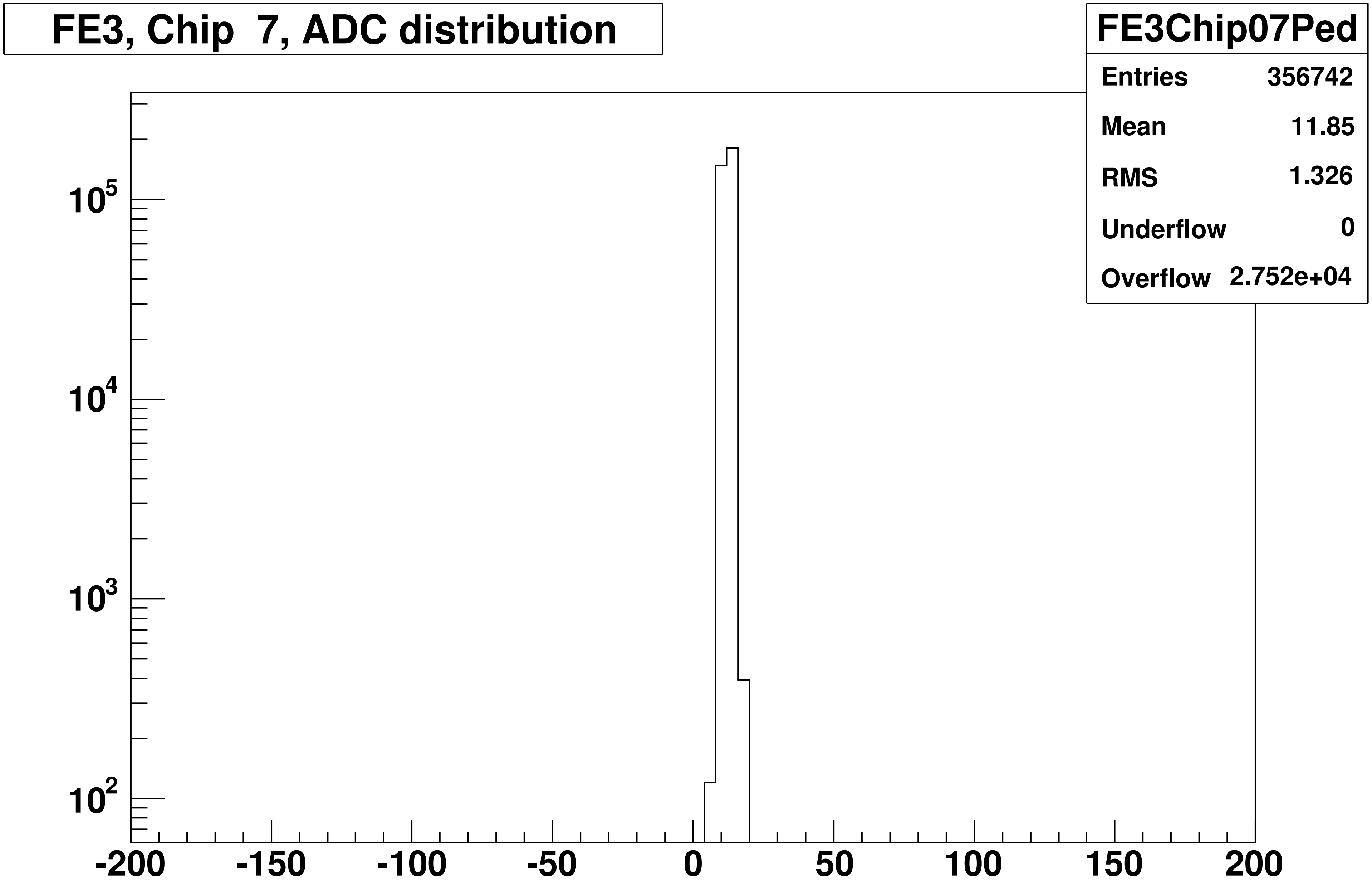
10000
15000
20000
25000


FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 356742
Mean 11.85
RMS 1.326
Underflow 0
Overflow 2.752e+04
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10^4
10^3
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0
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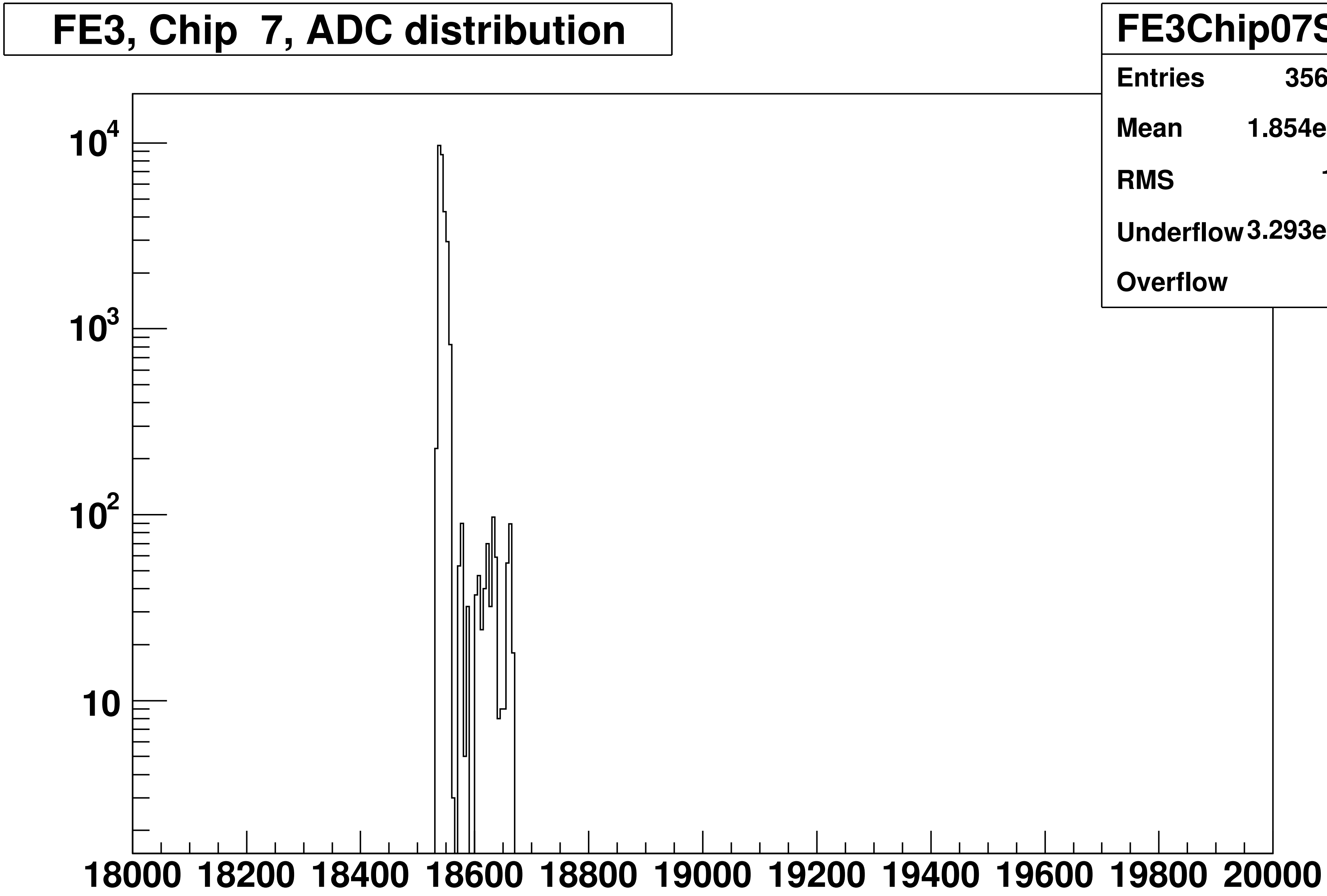
100
150
200


FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 356742
Mean 1.854e+04
RMS 14.9
Underflow 3.293e+05
Overflow 0
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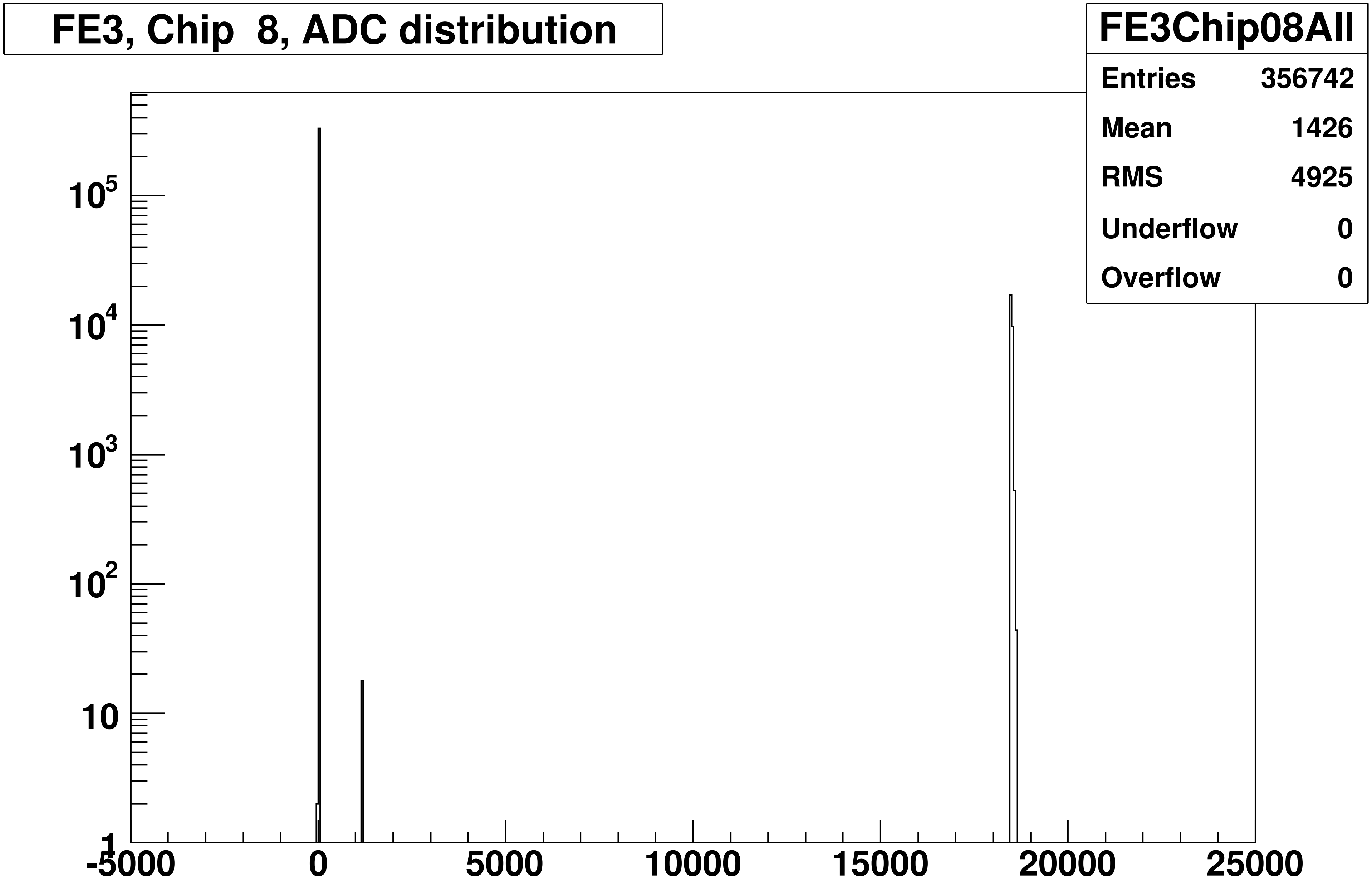
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 356742
Mean 1426
RMS 4925
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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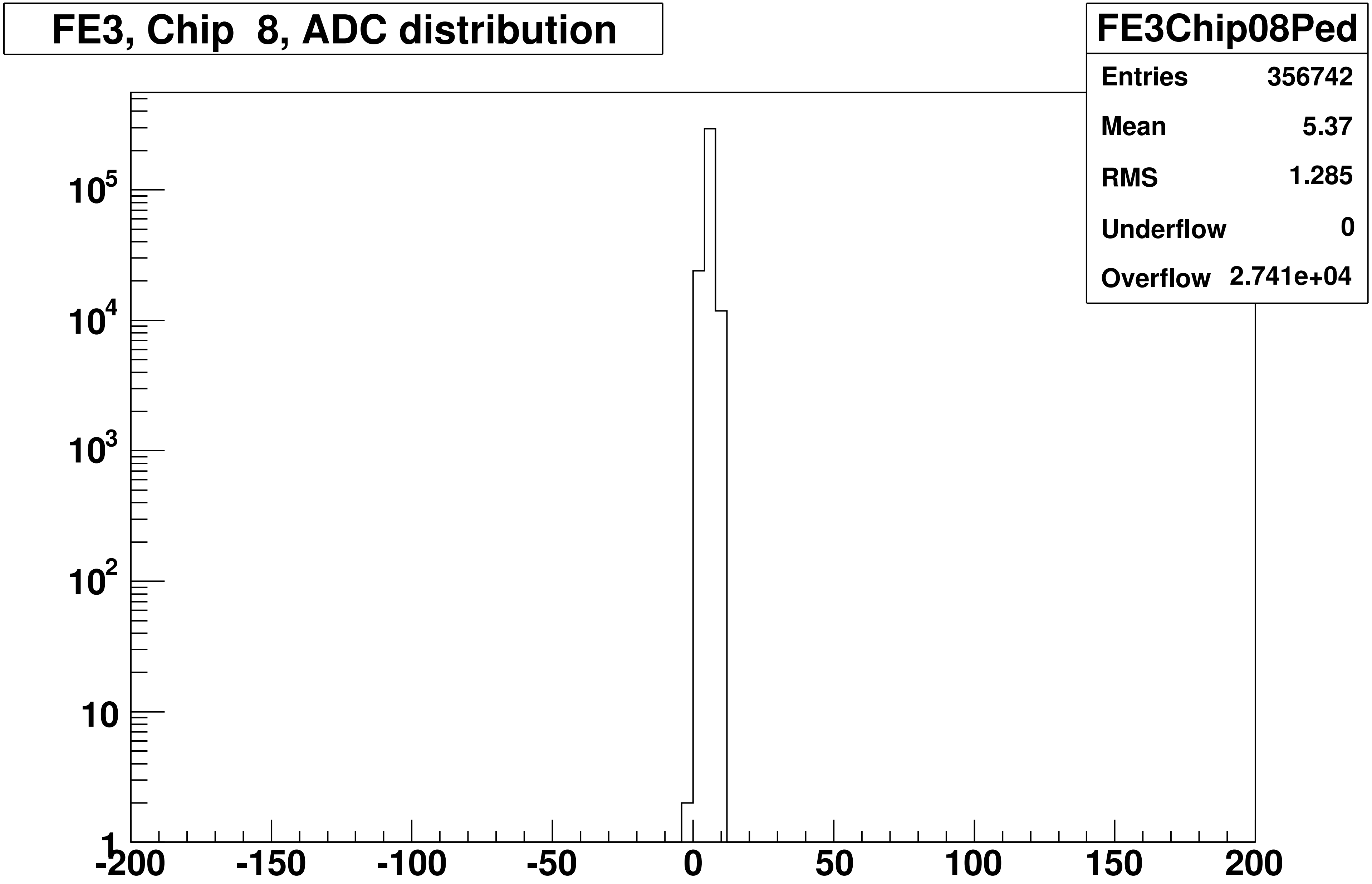
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 356742
Mean 5.37
RMS 1.285
Underflow 0
Overflow 2.741e+04
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10^2
10^3
10^4
10^5
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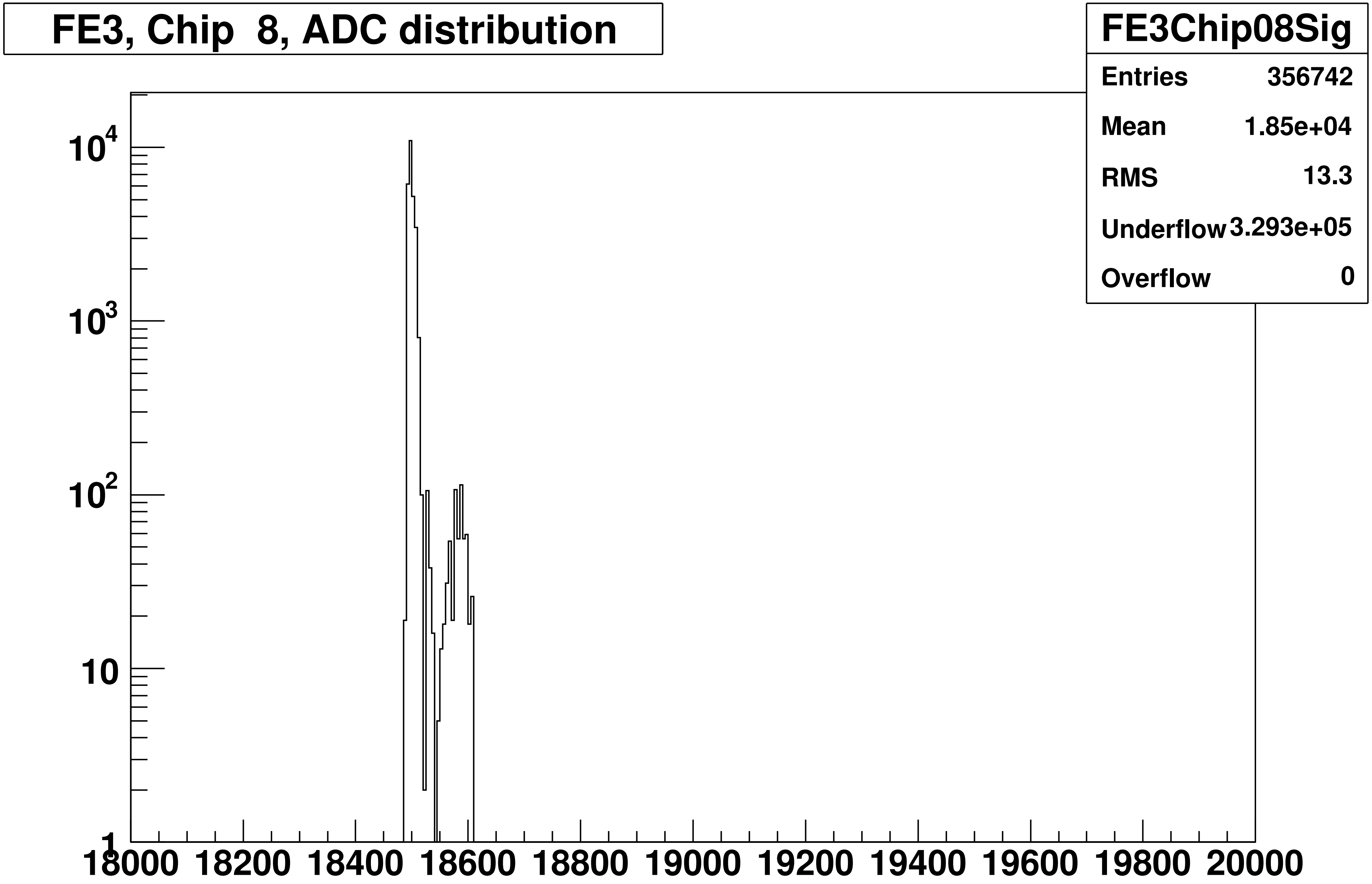
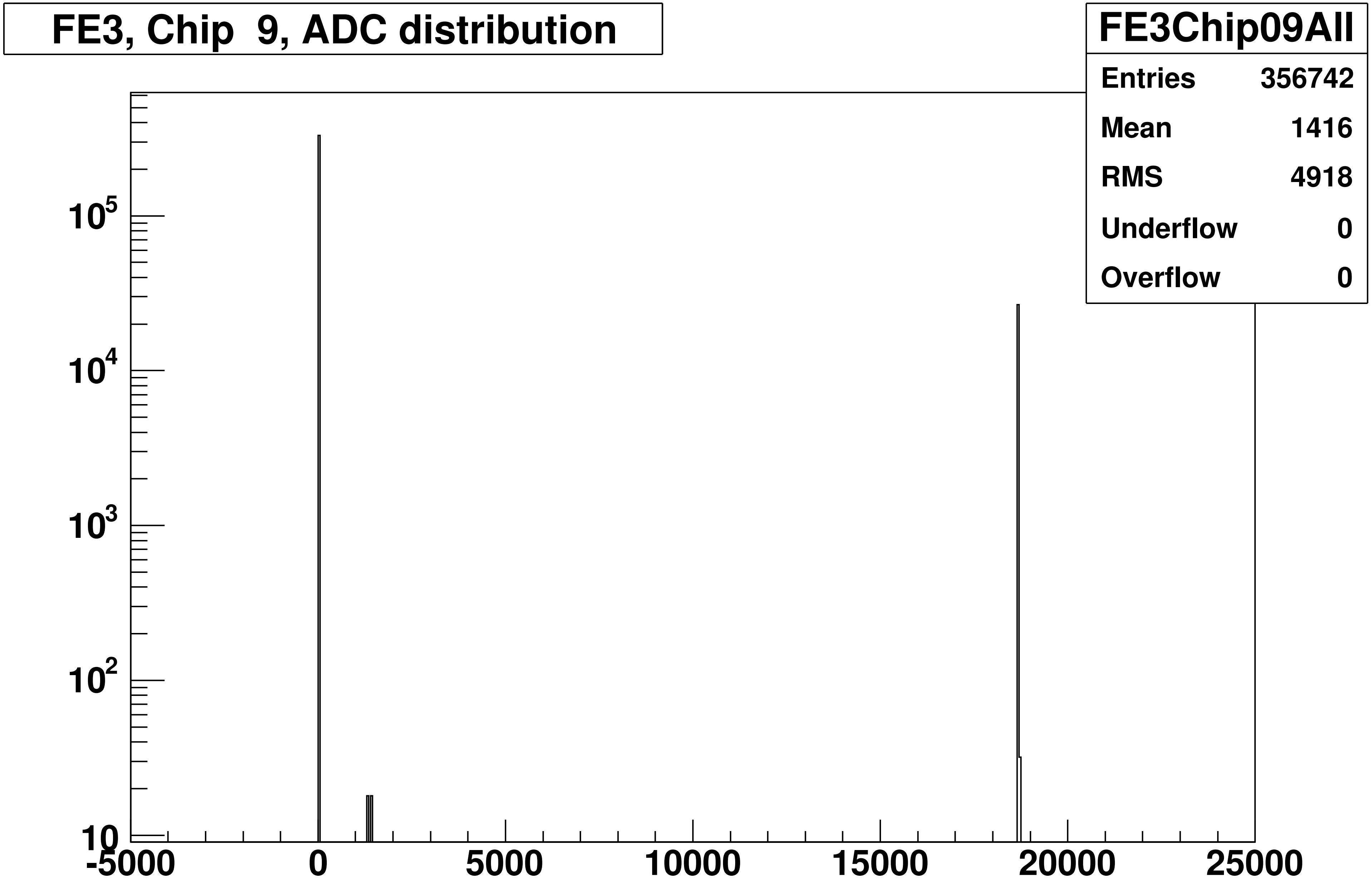
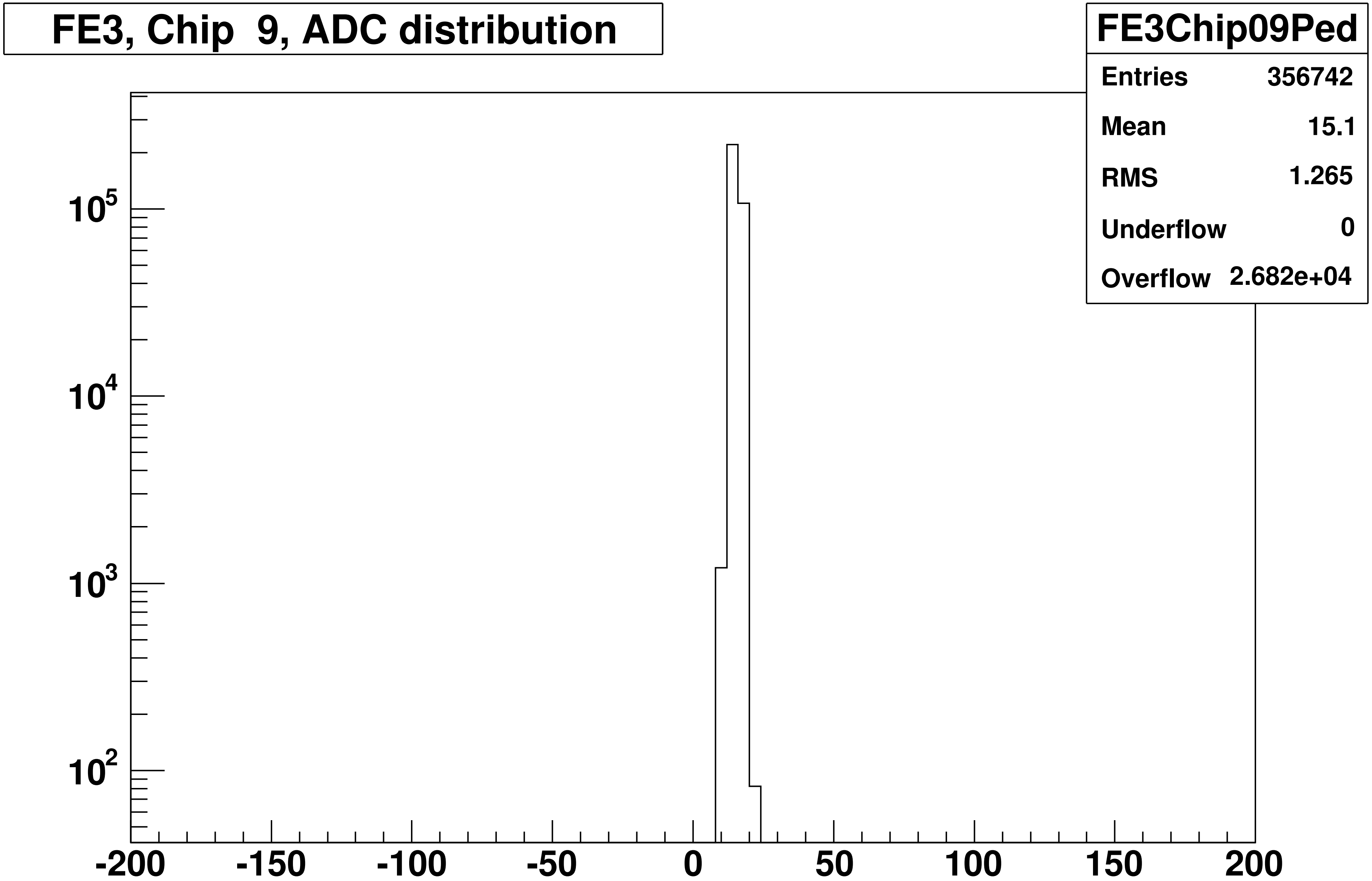
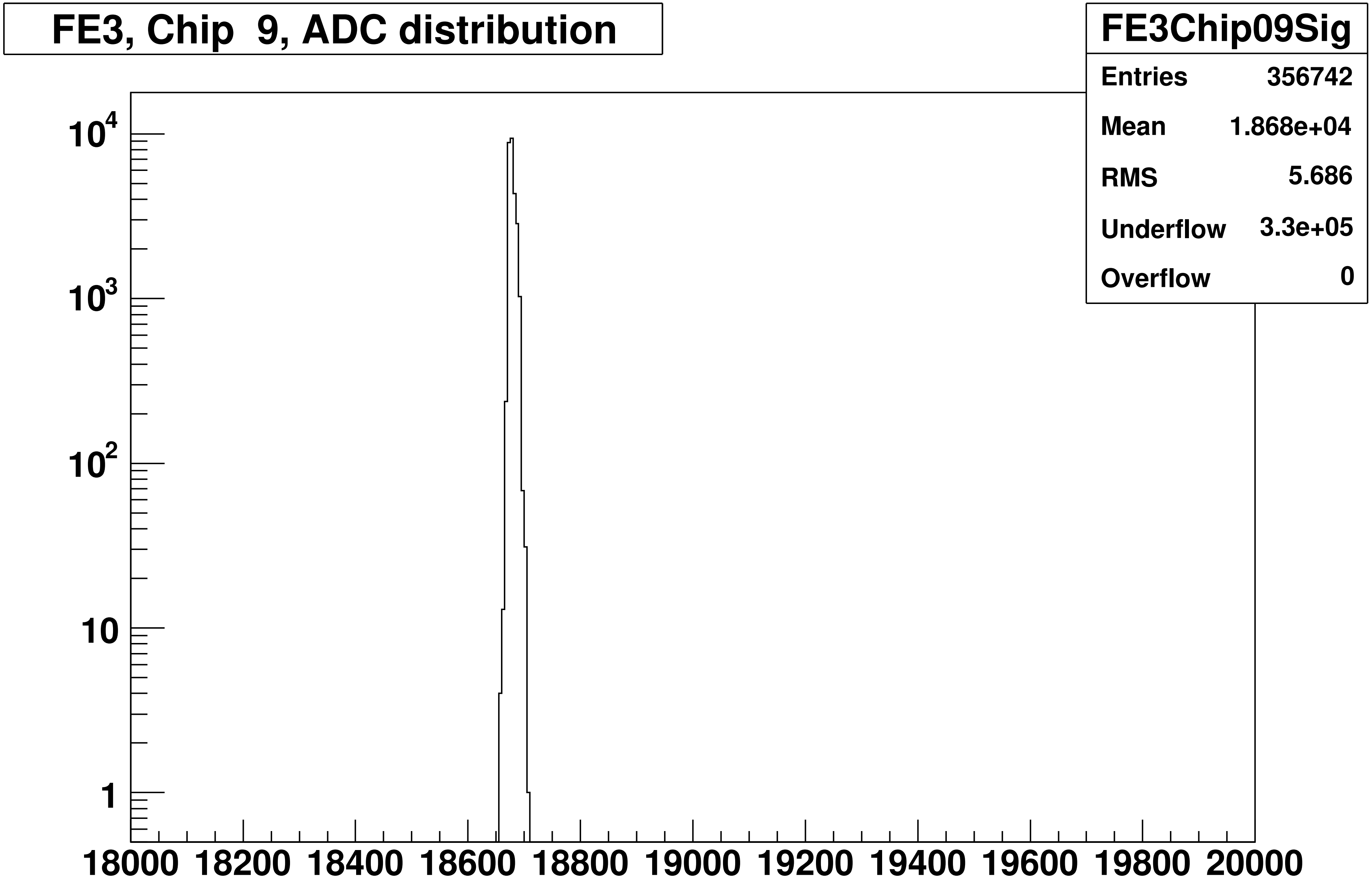
-150
-100
-50
0
50
100
150
200

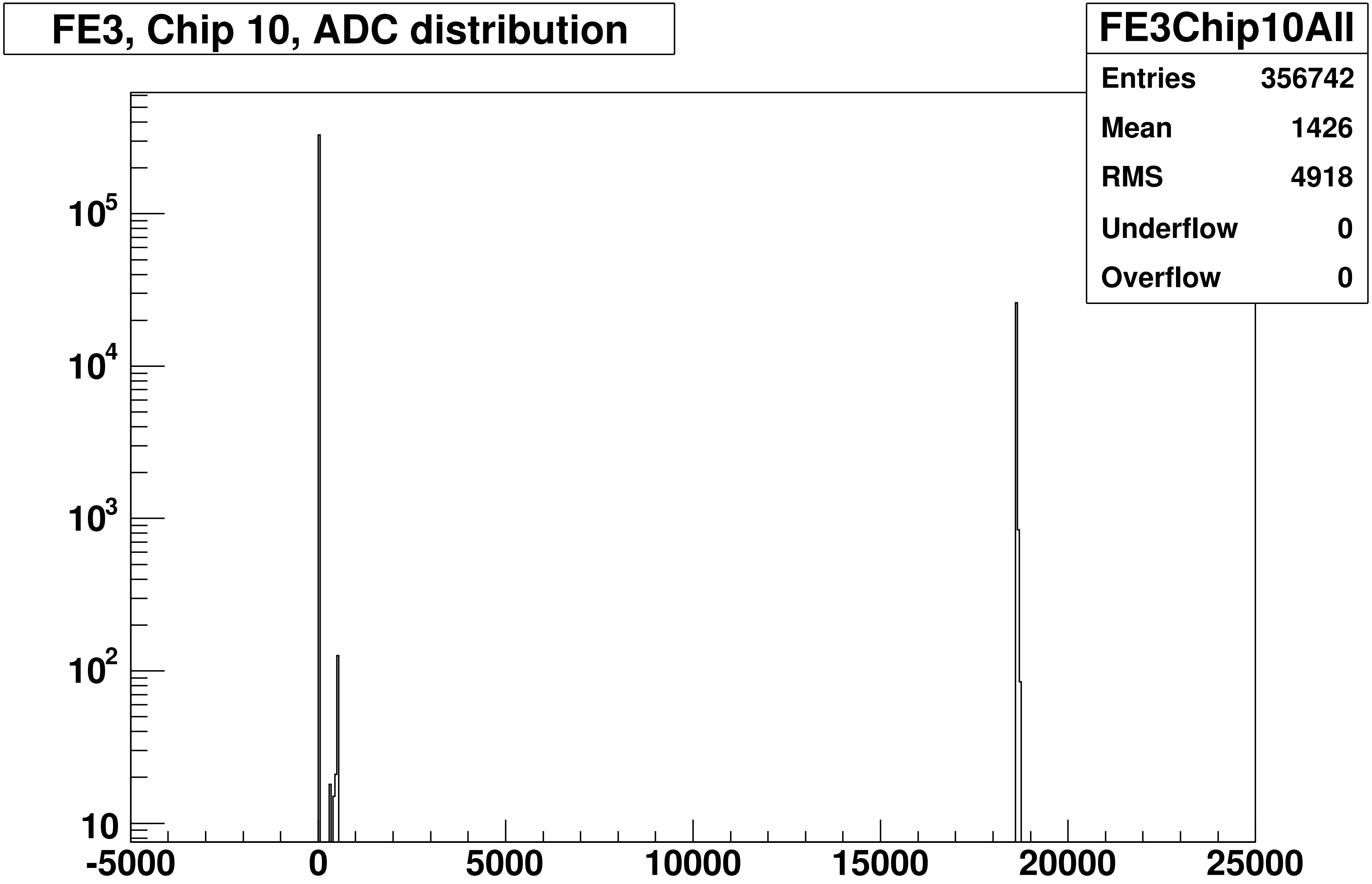

FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 356742
Mean 1.85e+04
RMS 13.3
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



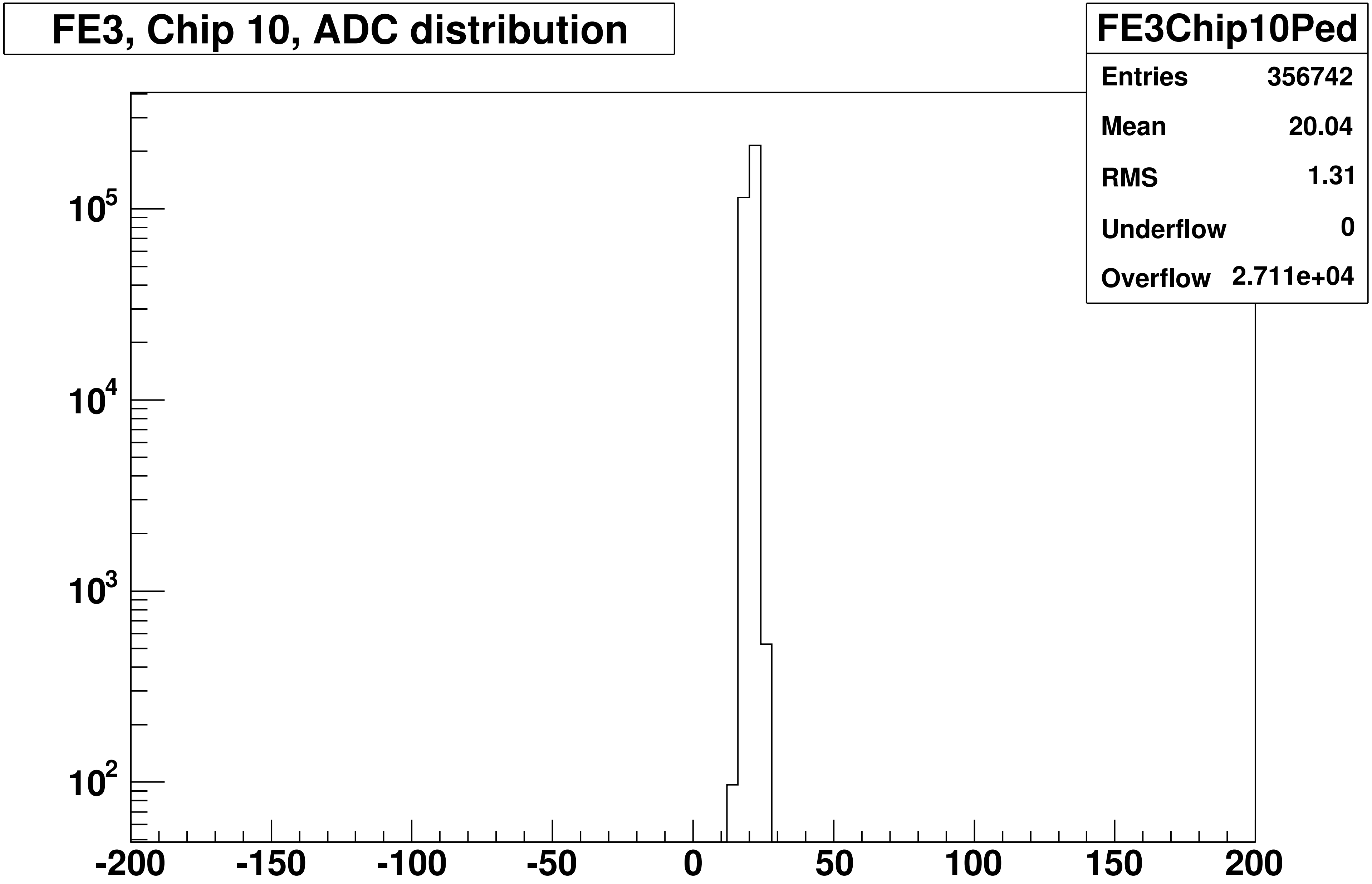
FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 356742
Mean 1416
RMS 4918
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 356742
Mean 15.1
RMS 1.265
Underflow 0
Overflow 2.682e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 356742
Mean 1.868e+04
RMS 5.686
Underflow 3.3e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 356742
Mean 1426
RMS 4918
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 356742
Mean 20.04
RMS 1.31
Underflow 0
Overflow 2.711e+04
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10^4
10^3
10^2
-200
-150
-100
-50
0
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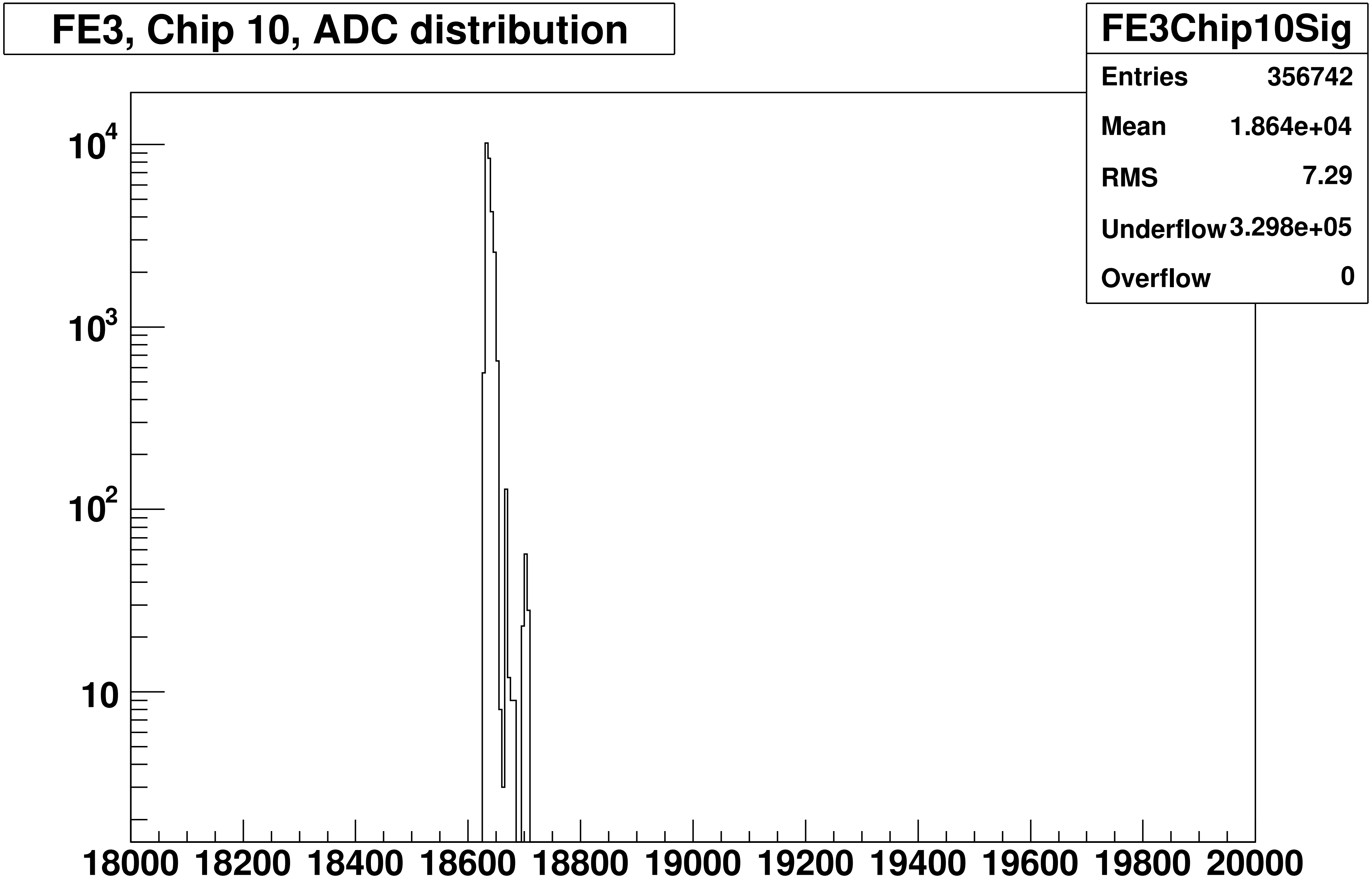
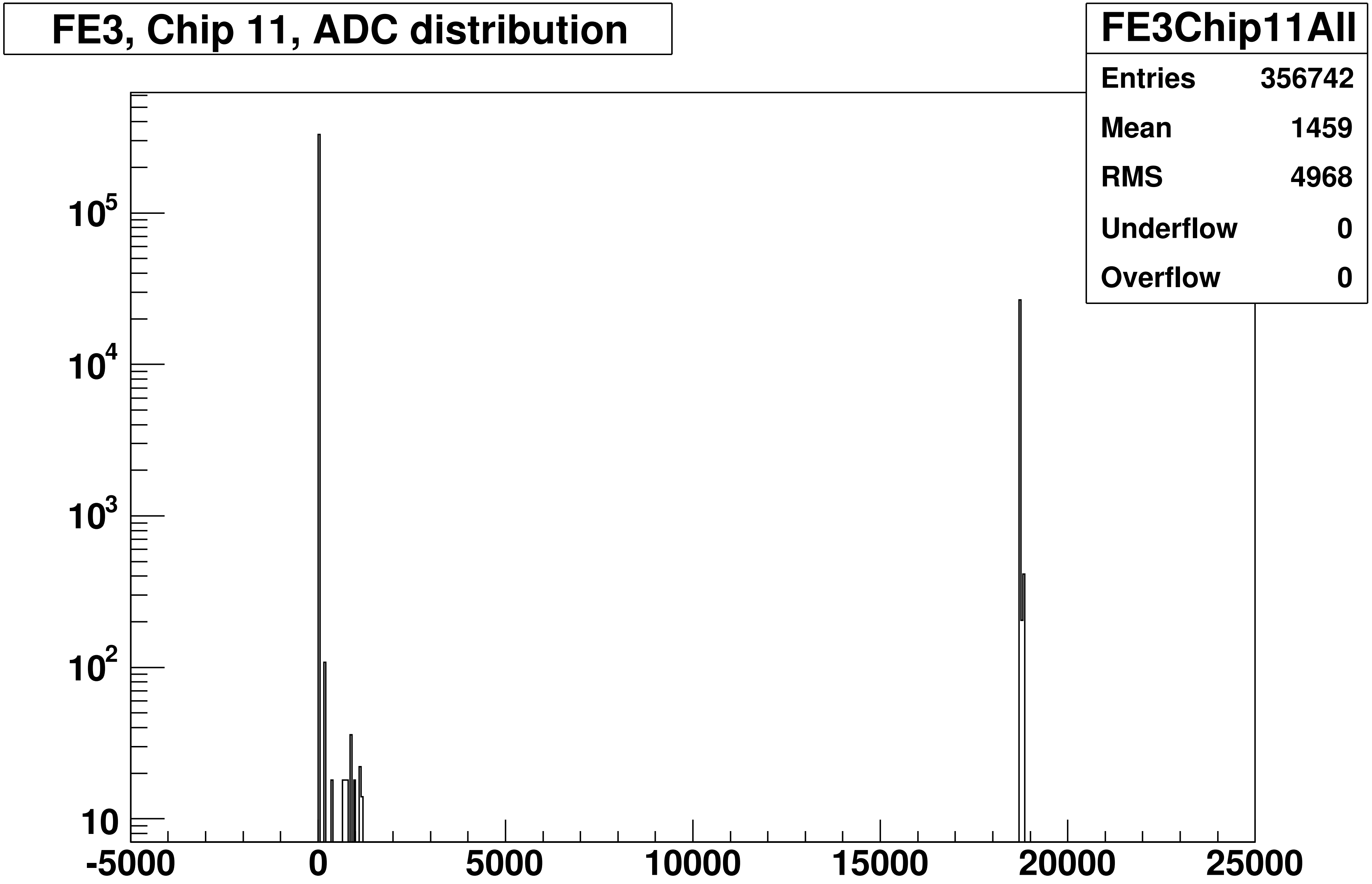
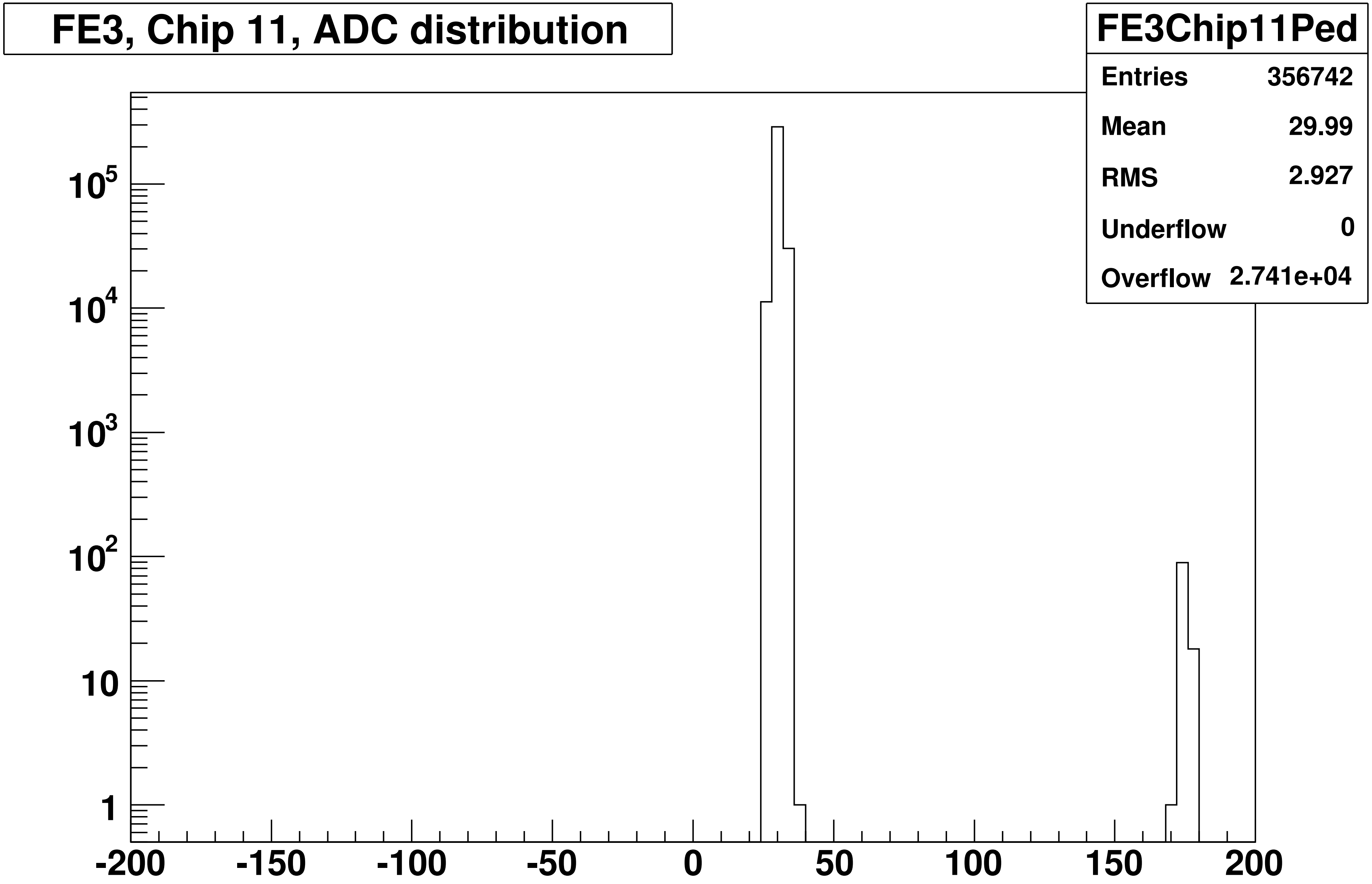
100
150
200


FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 356742
Mean 1.864e+04
RMS 7.29
Underflow 3.298e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 356742
Mean 1459
RMS 4968
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 356742
Mean 29.99
RMS 2.927
Underflow 0
Overflow 2.741e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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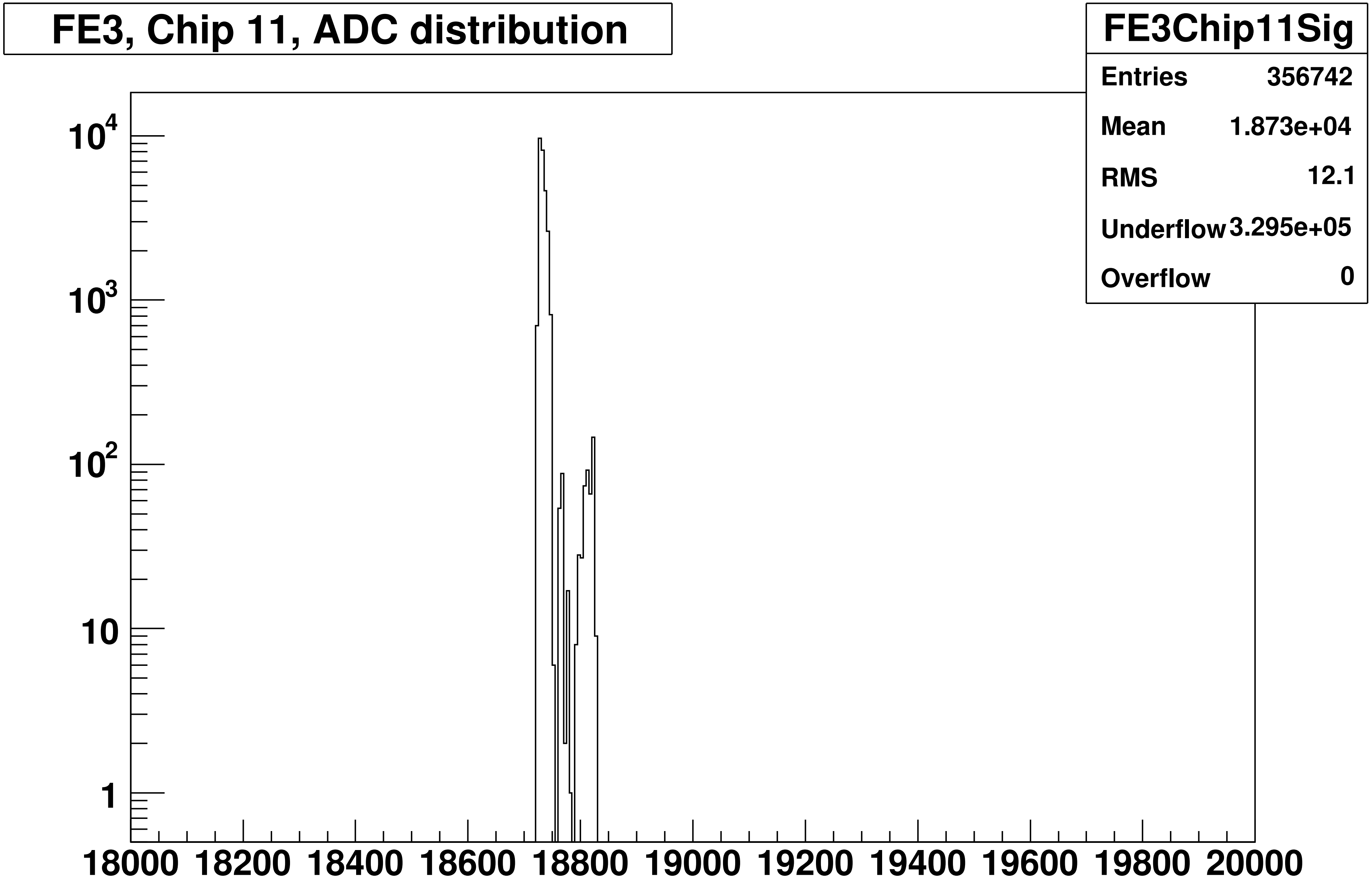
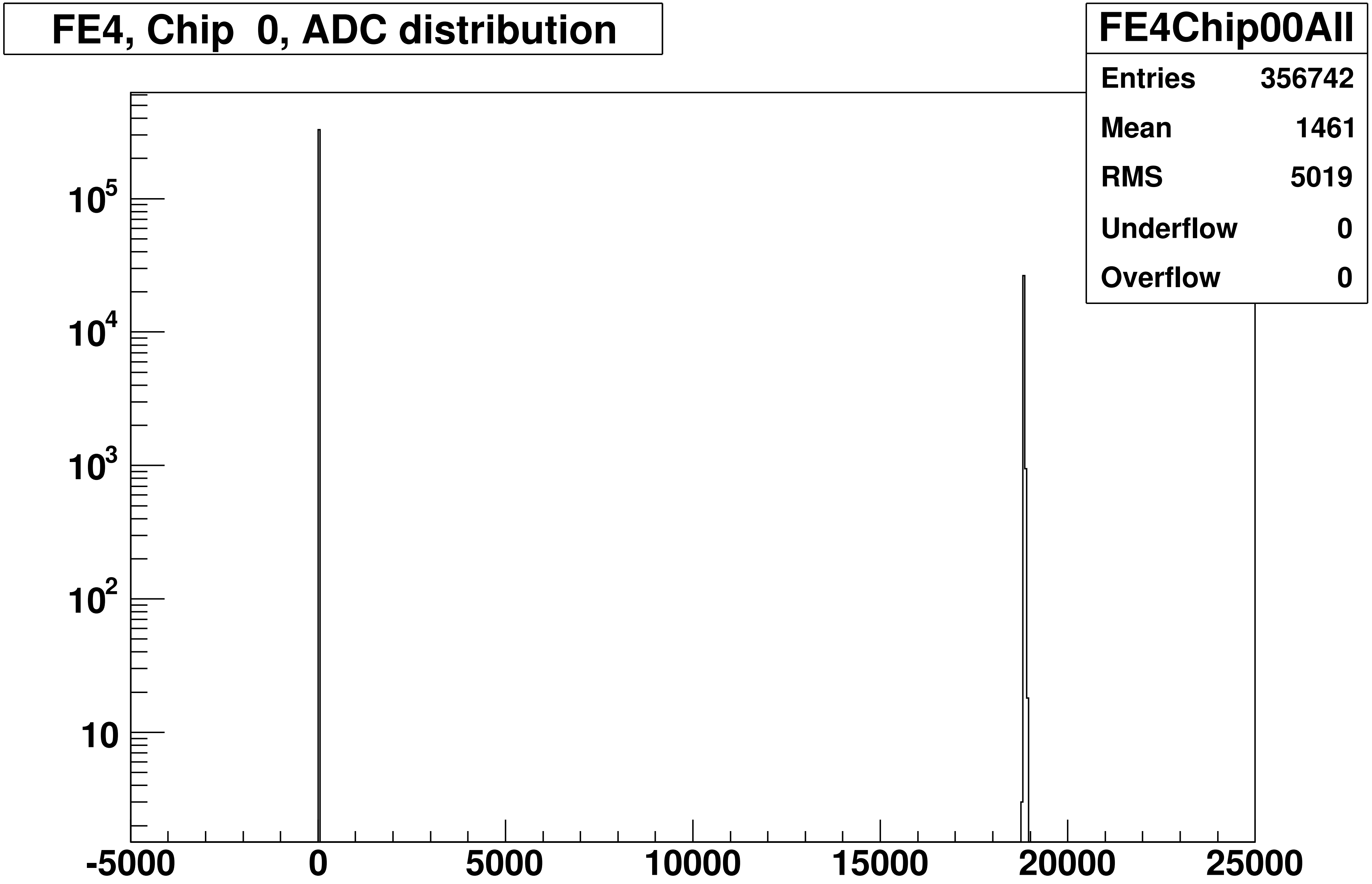
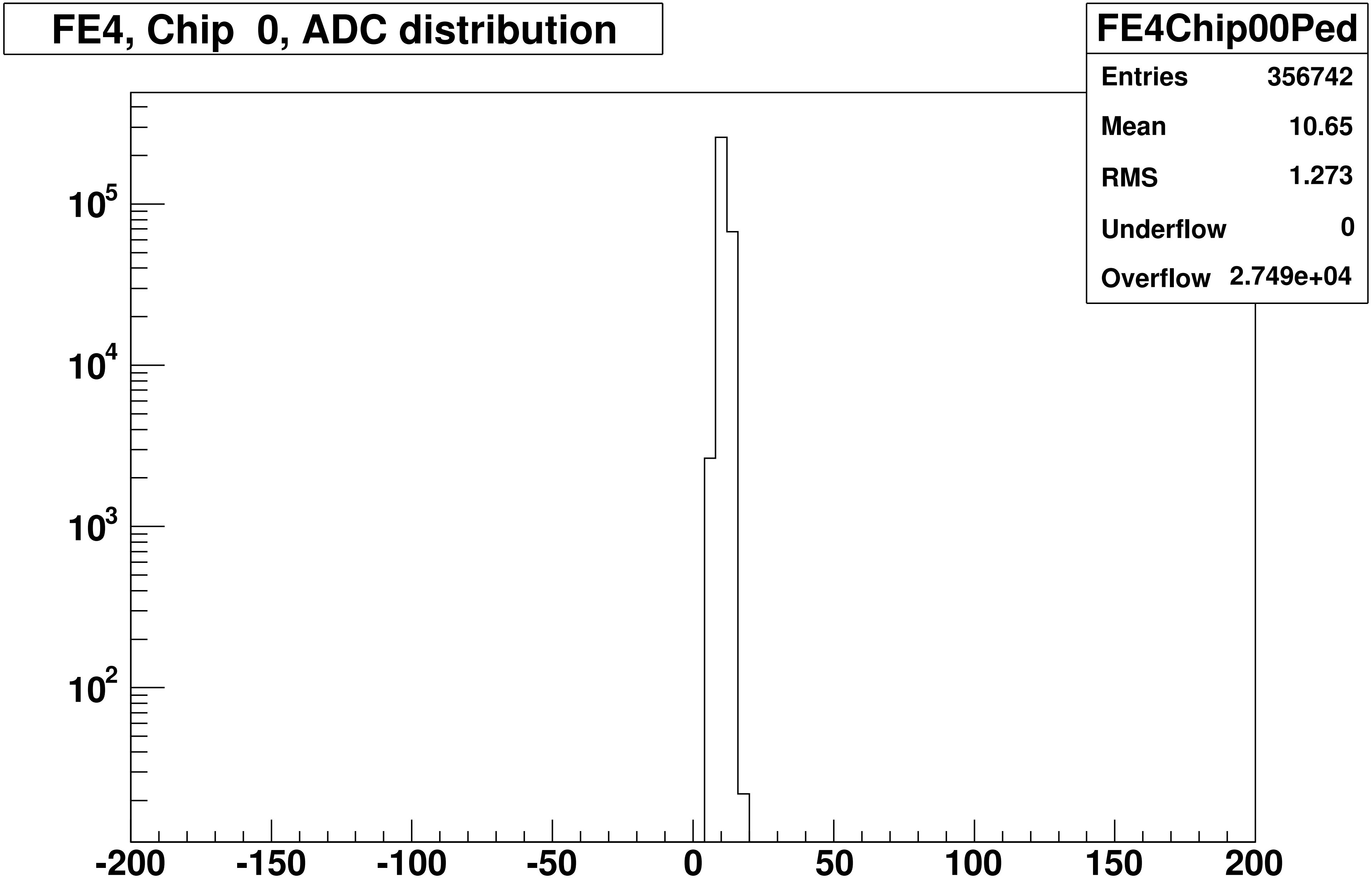
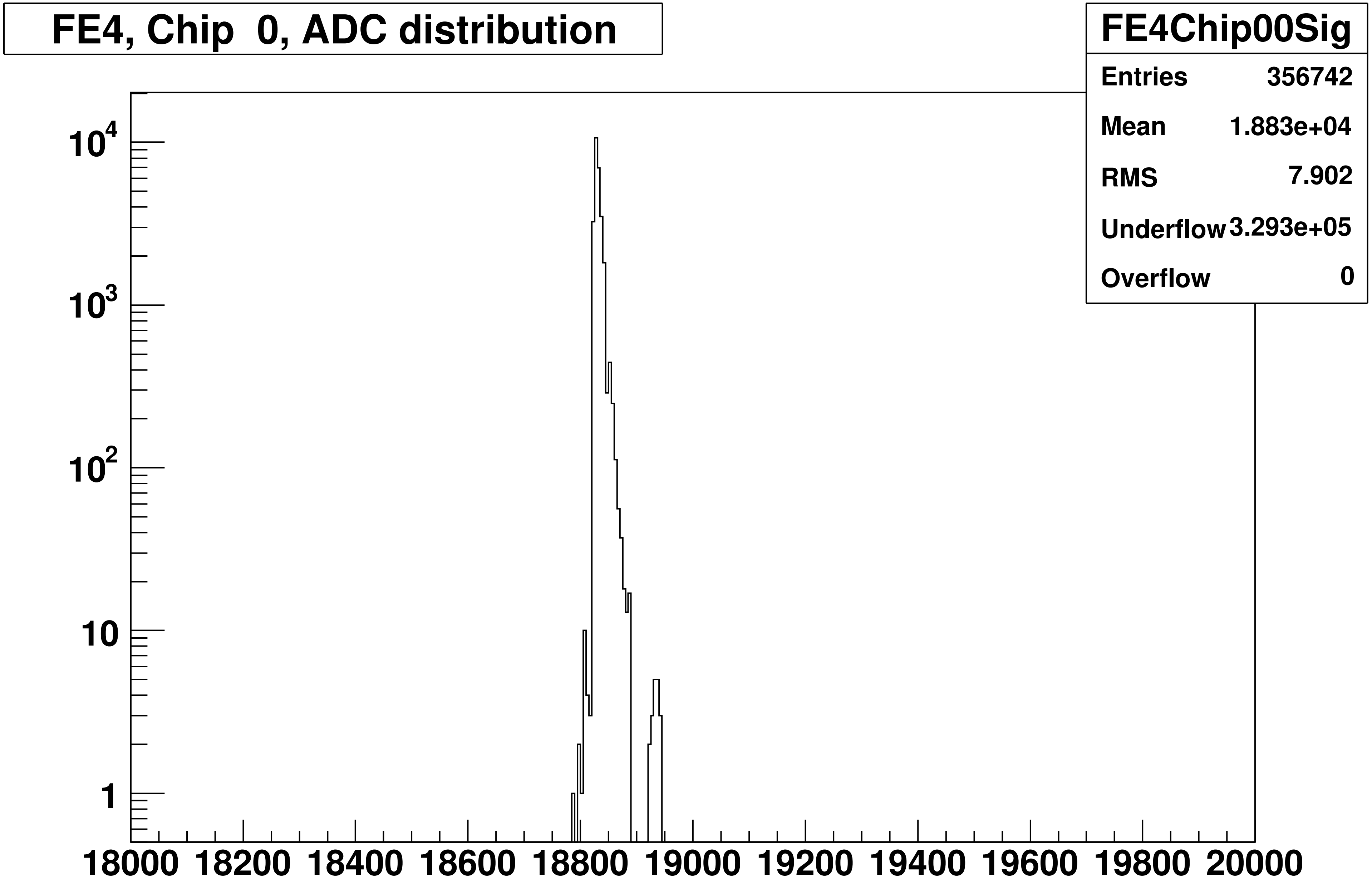
0
50
100
150
200

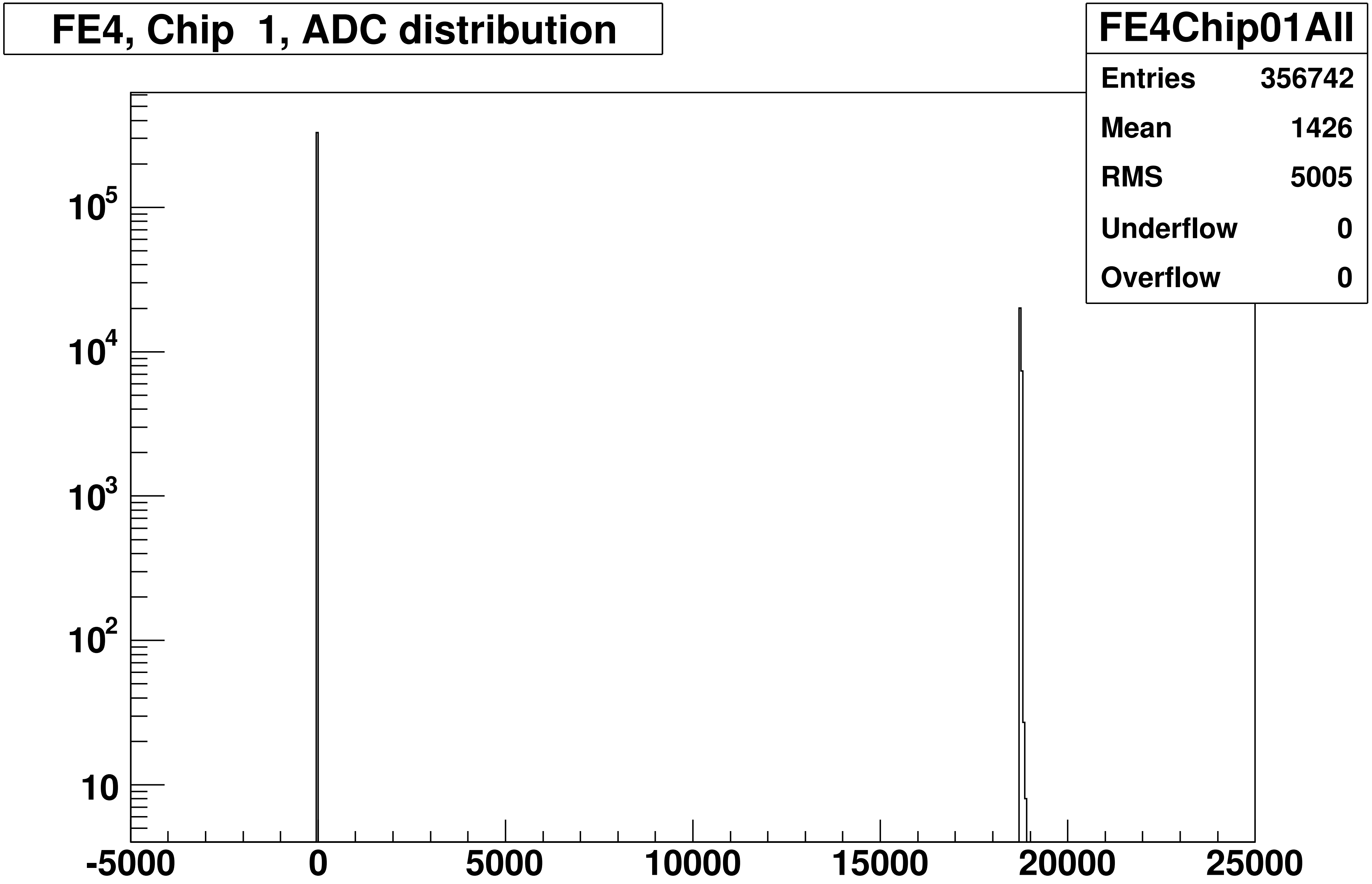

FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 356742
Mean 1.873e+04
RMS 12.1
Underflow 3.295e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 356742
Mean 1461
RMS 5019
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 356742
Mean 10.65
RMS 1.273
Underflow 0
Overflow 2.749e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 356742
Mean 1.883e+04
RMS 7.902
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 356742
Mean 1426
RMS 5005
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
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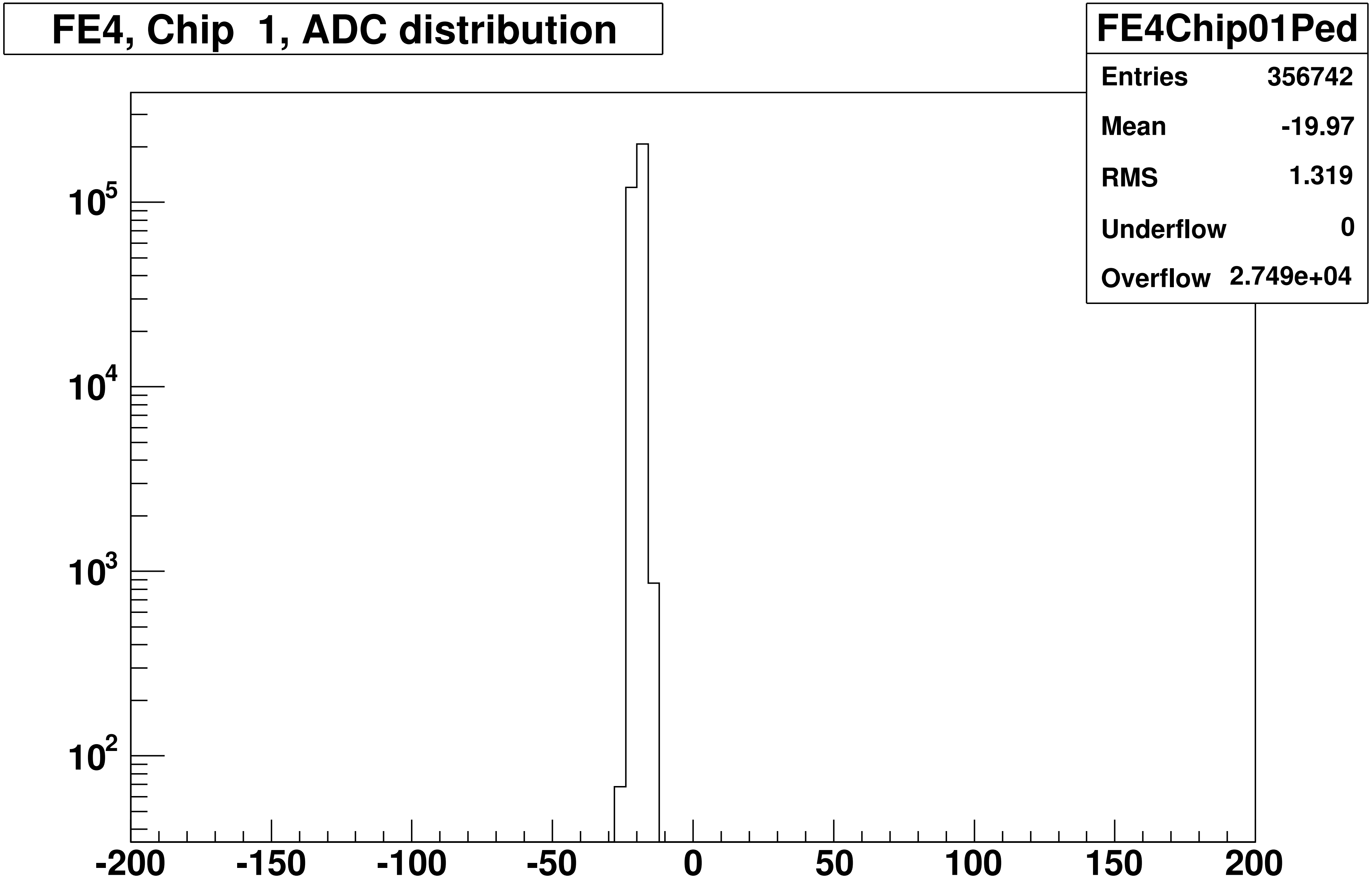
15000
20000
25000



FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 356742
Mean -19.97
RMS 1.319
Underflow 0
Overflow 2.749e+04
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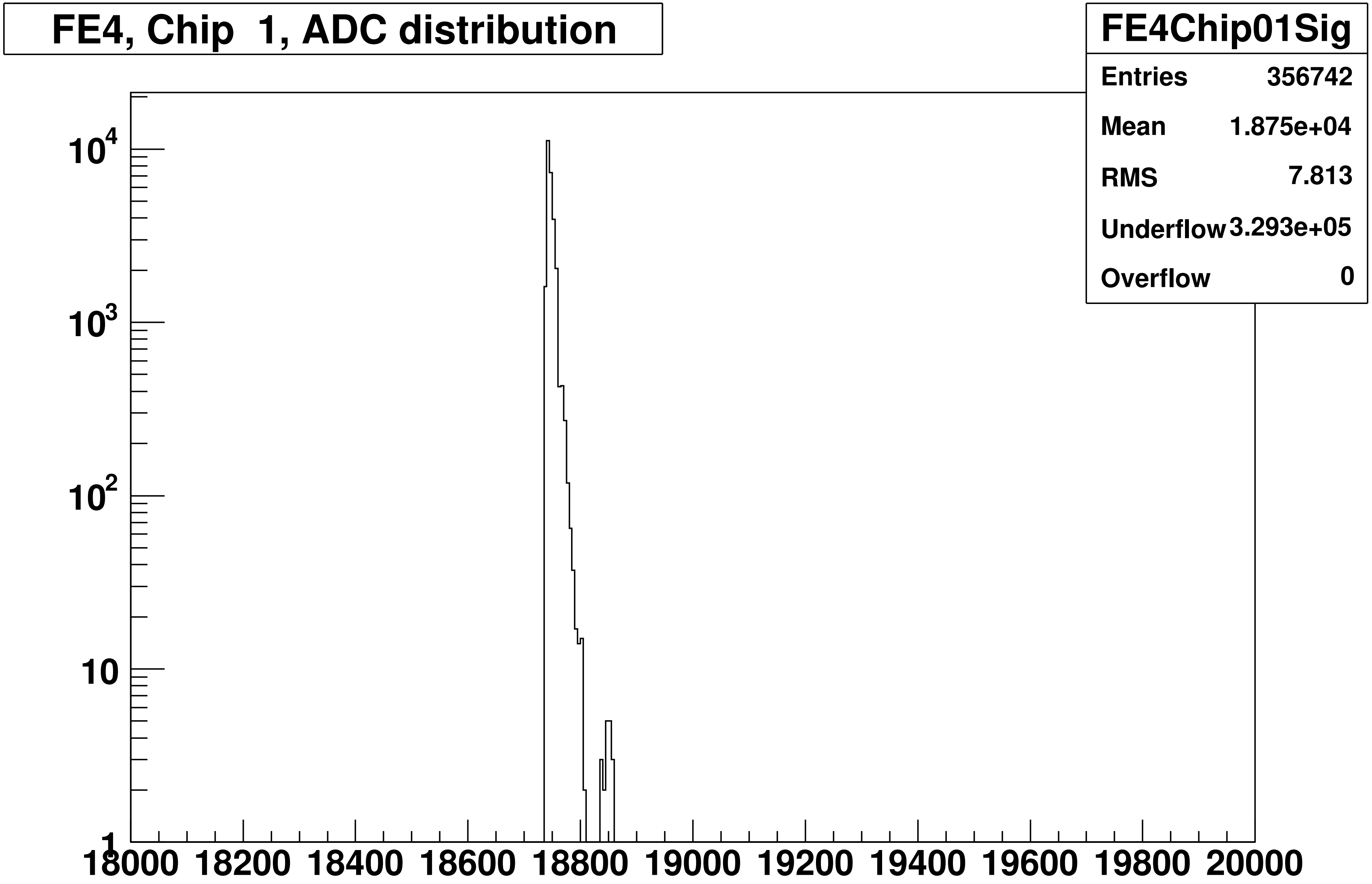
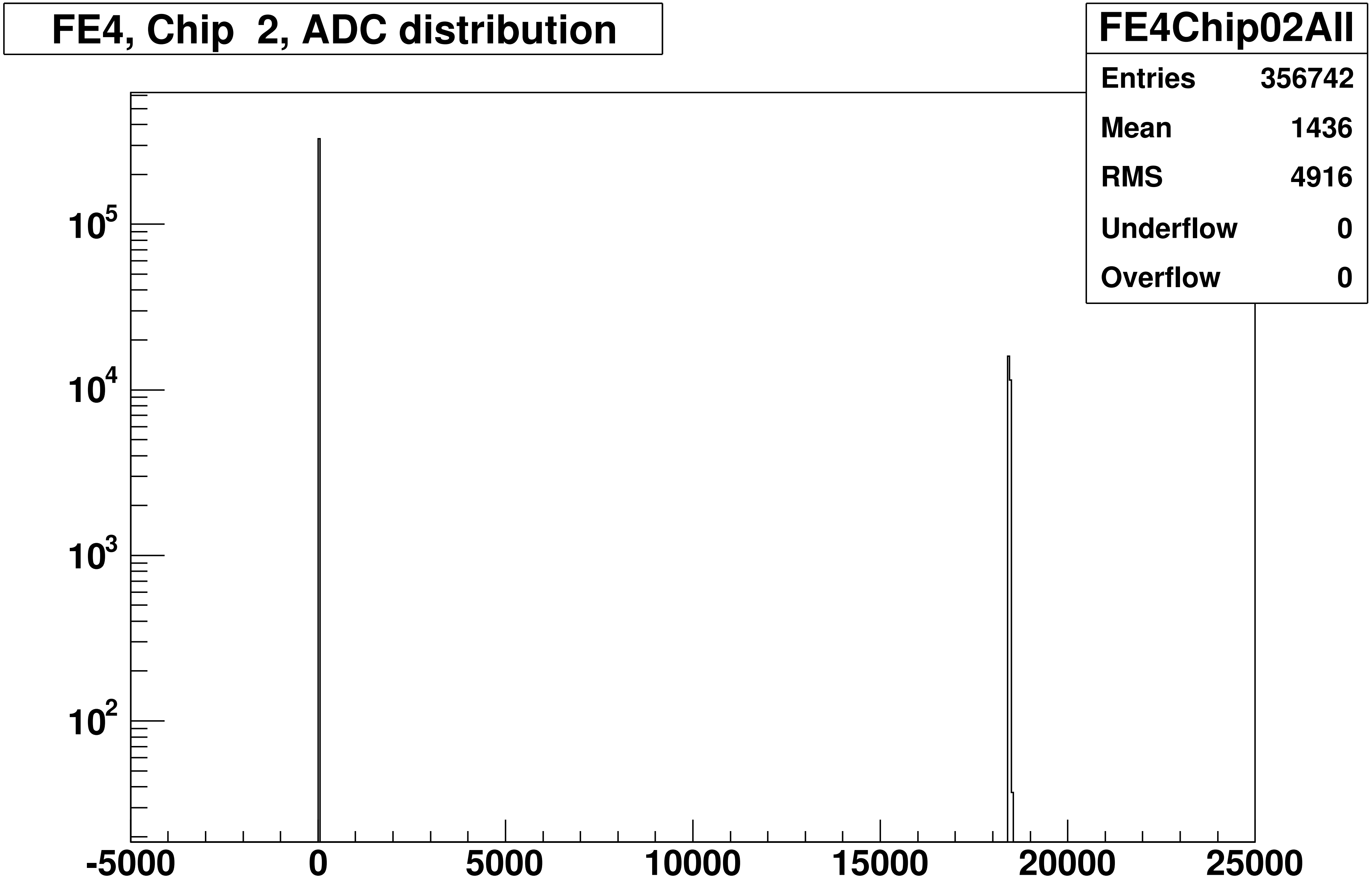
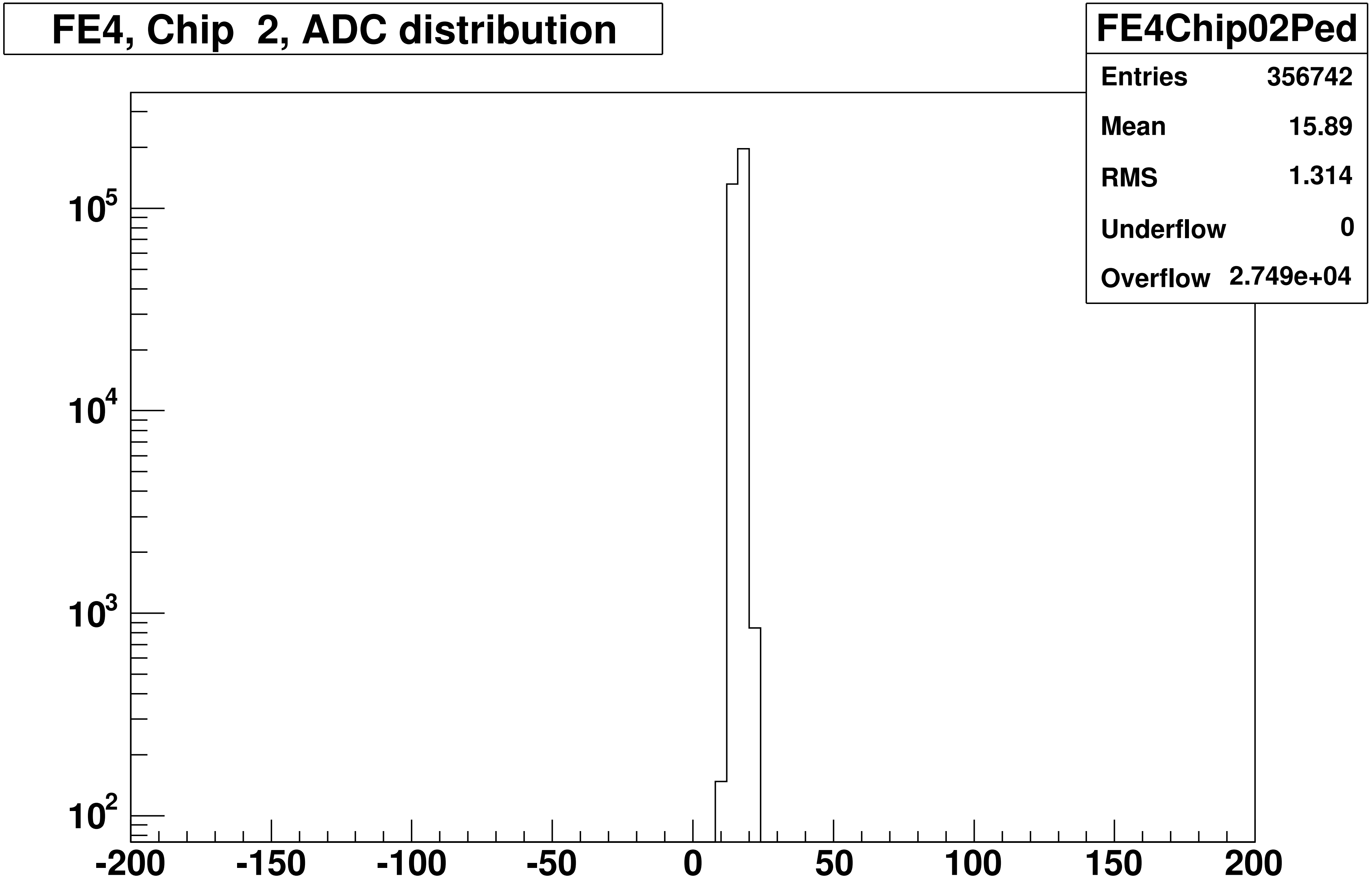
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 356742
Mean 1.875e+04
RMS 7.813
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 356742
Mean 1436
RMS 4916
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 356742
Mean 15.89
RMS 1.314
Underflow 0
Overflow 2.749e+04
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10^4
10^3
10^2
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-150
-100
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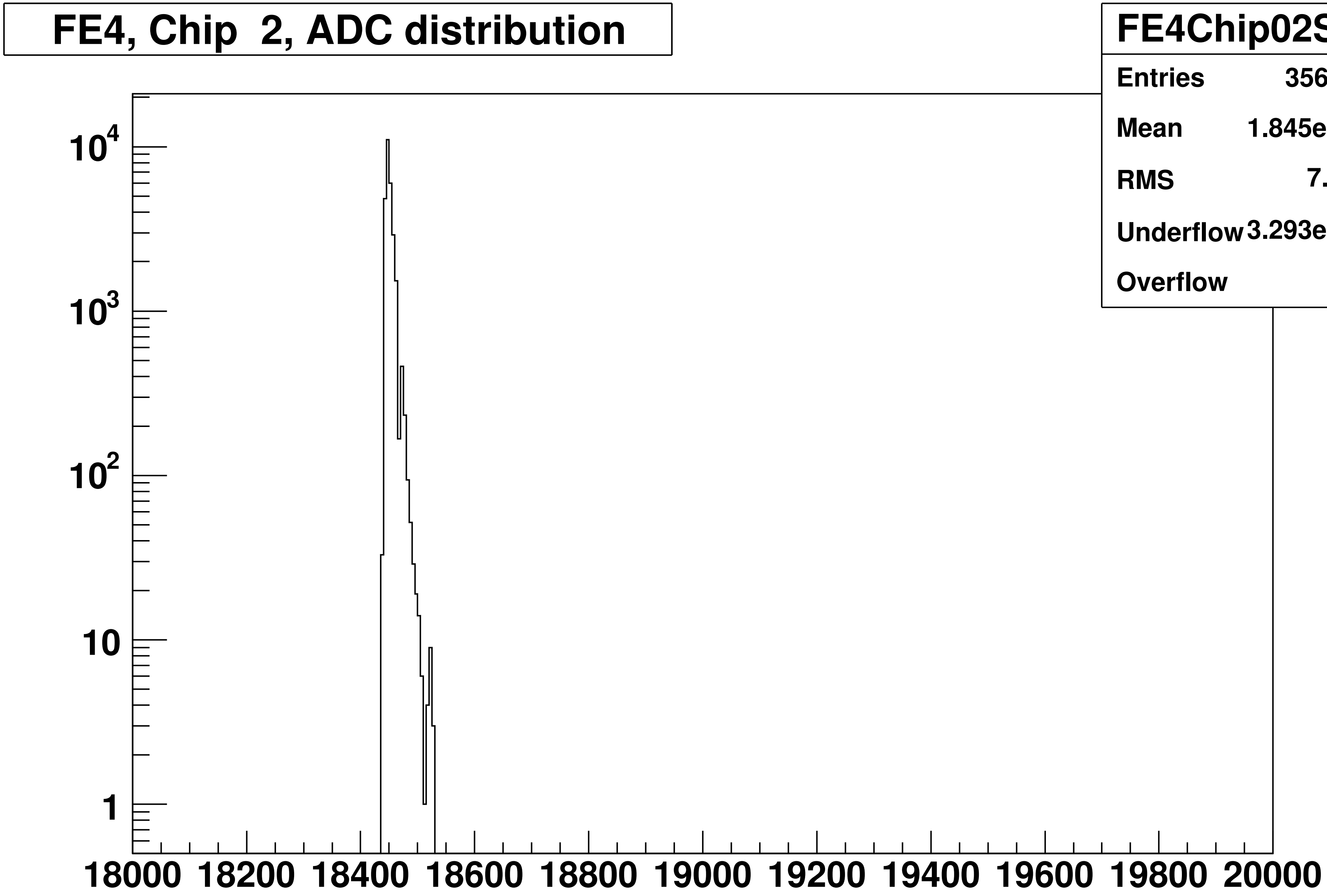
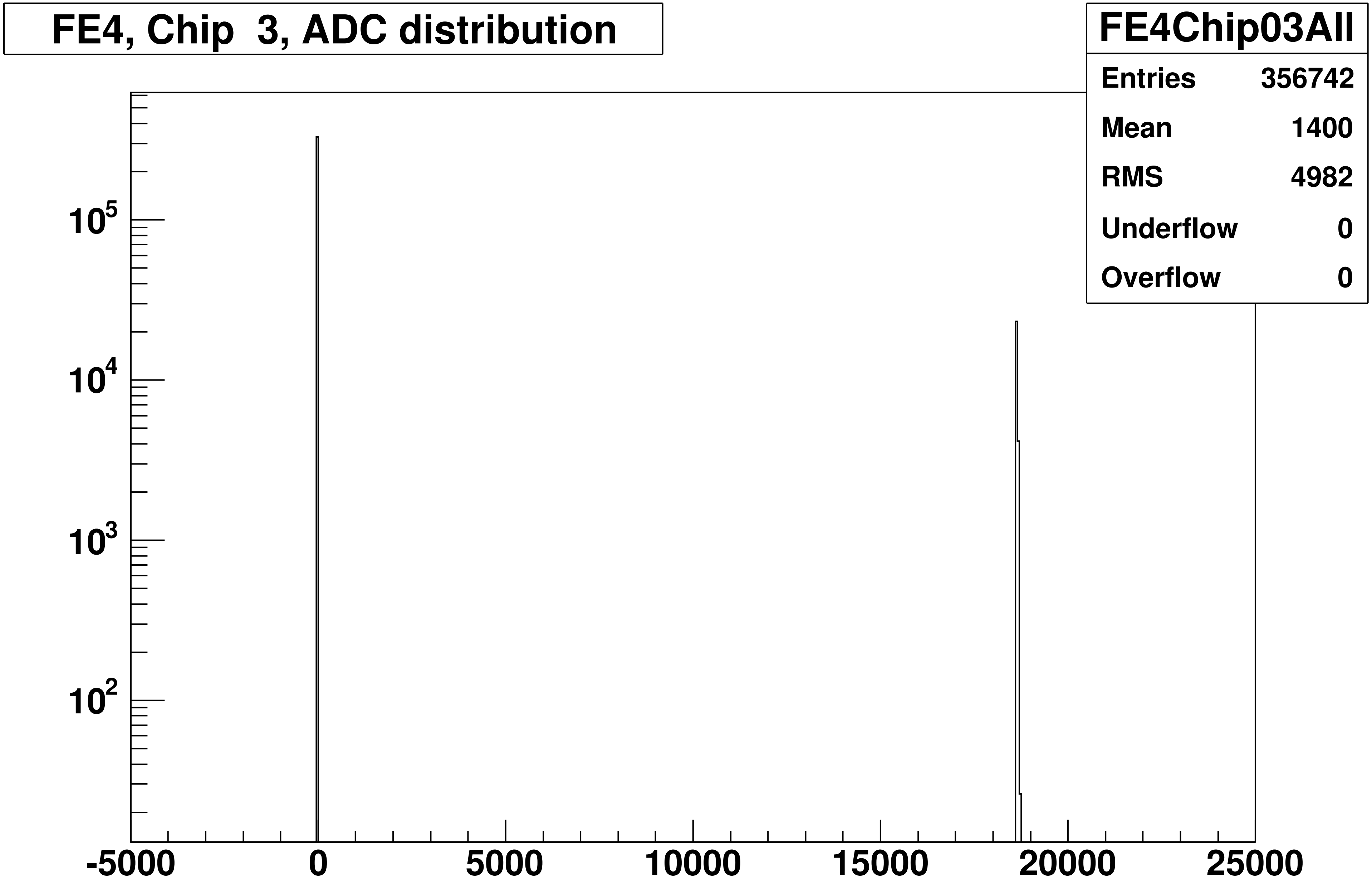
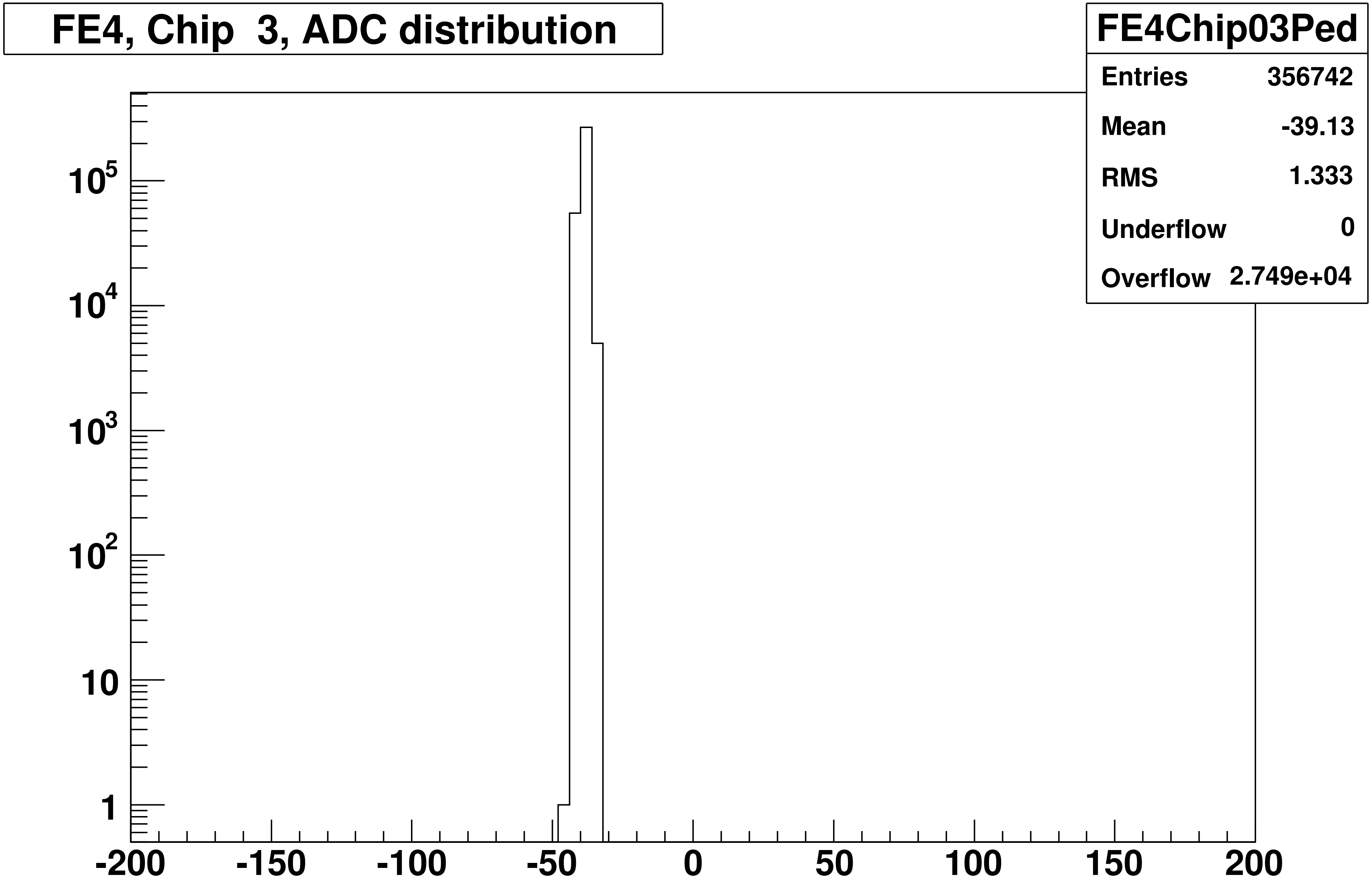
0
50
100
150
200


FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 356742
Mean 1.845e+04
RMS 7.549
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 356742
Mean 1400
RMS 4982
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 356742
Mean -39.13
RMS 1.333
Underflow 0
Overflow 2.749e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
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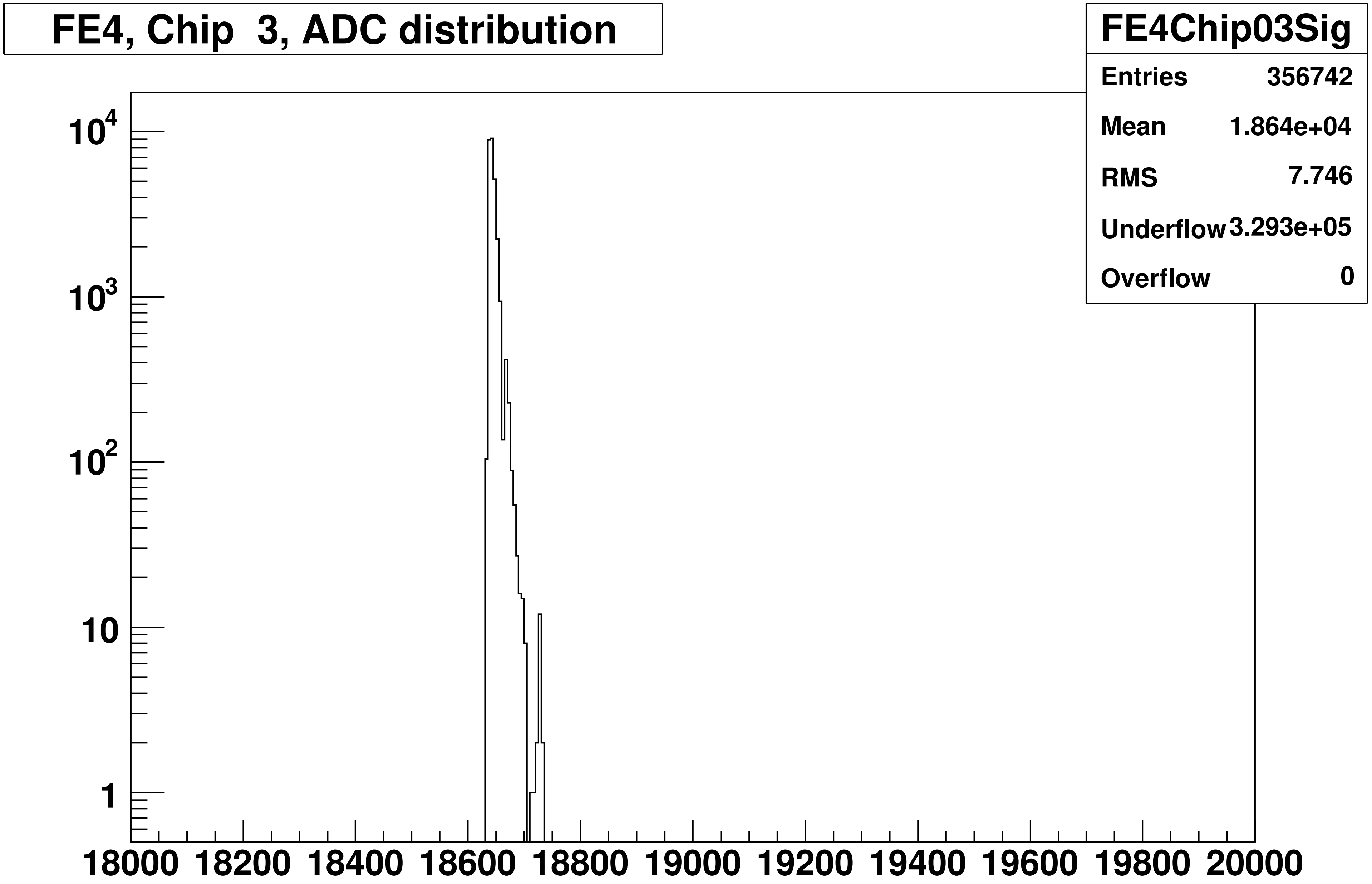
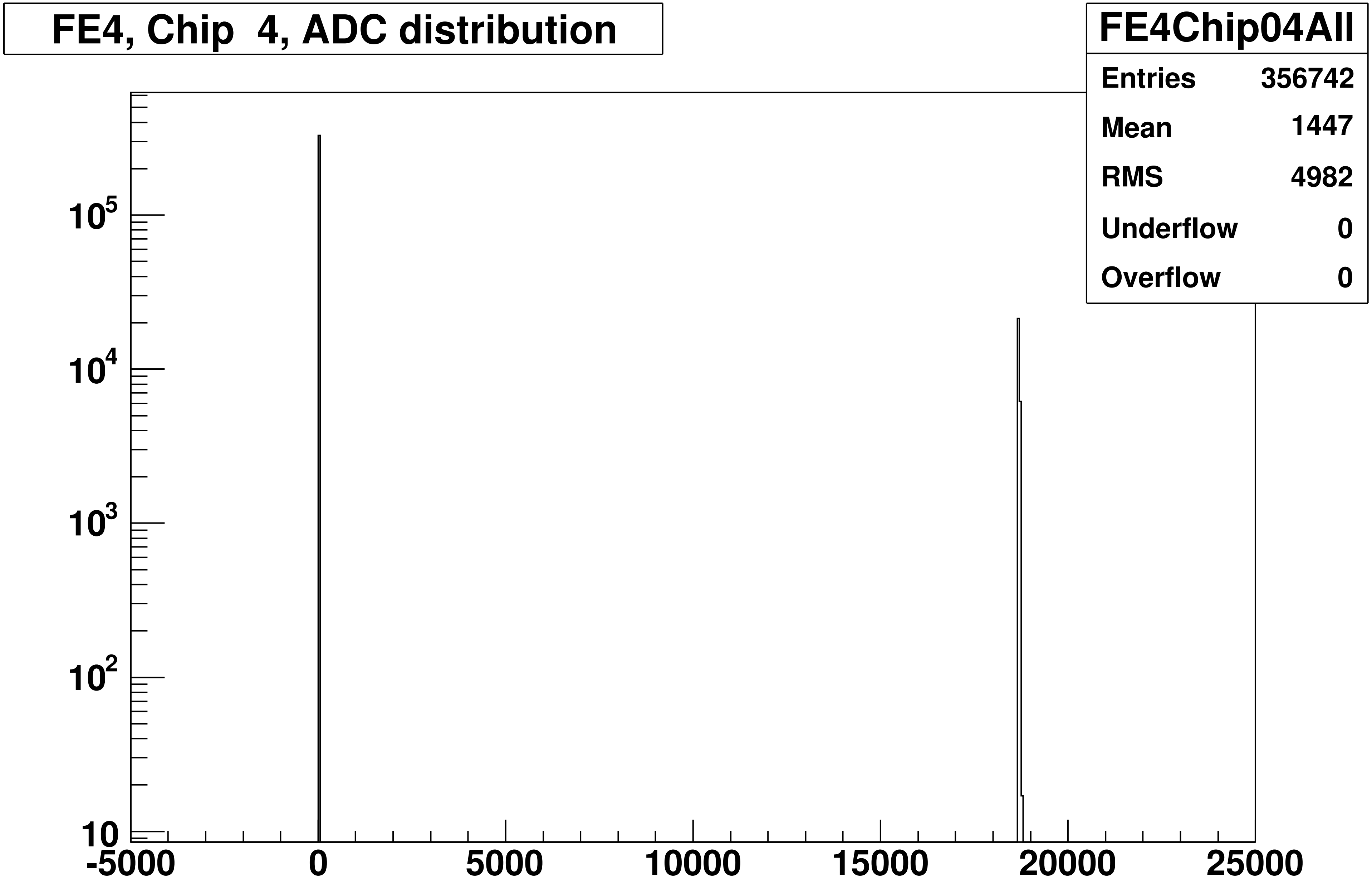
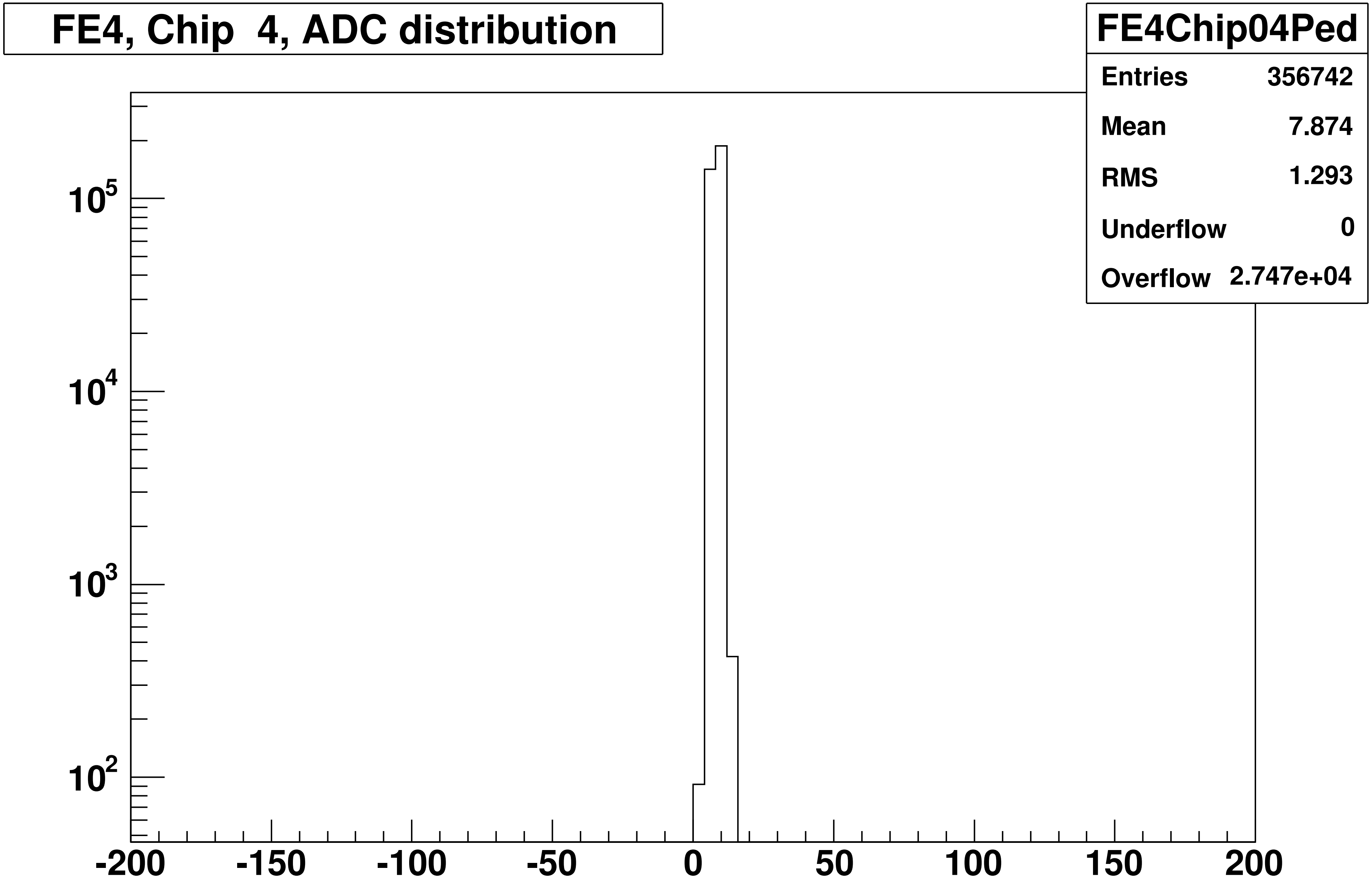
0
50
100
150
200



FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 356742
Mean 1.864e+04
RMS 7.746
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 356742
Mean 1447
RMS 4982
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 356742
Mean 7.874
RMS 1.293
Underflow 0
Overflow 2.747e+04
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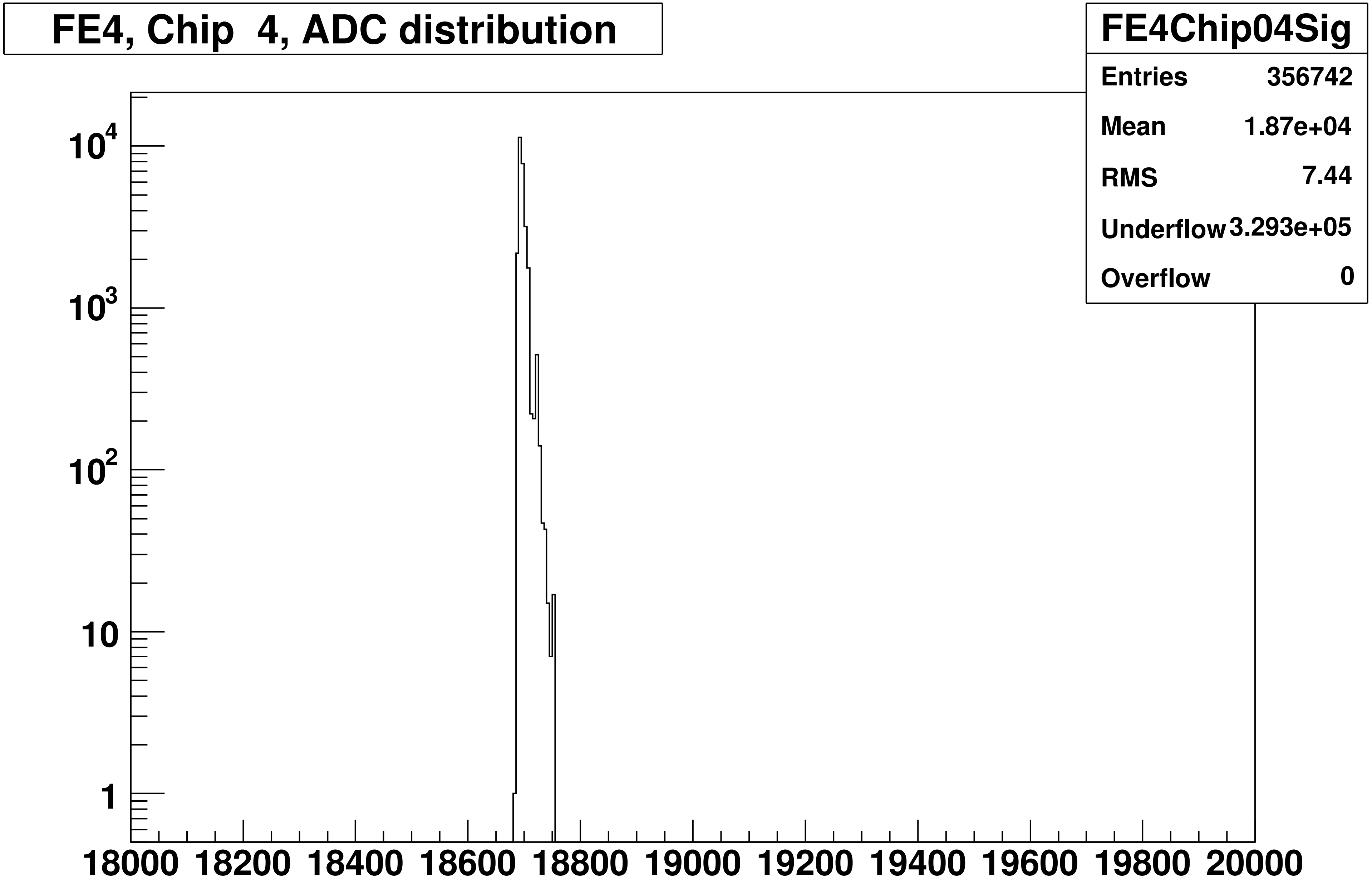
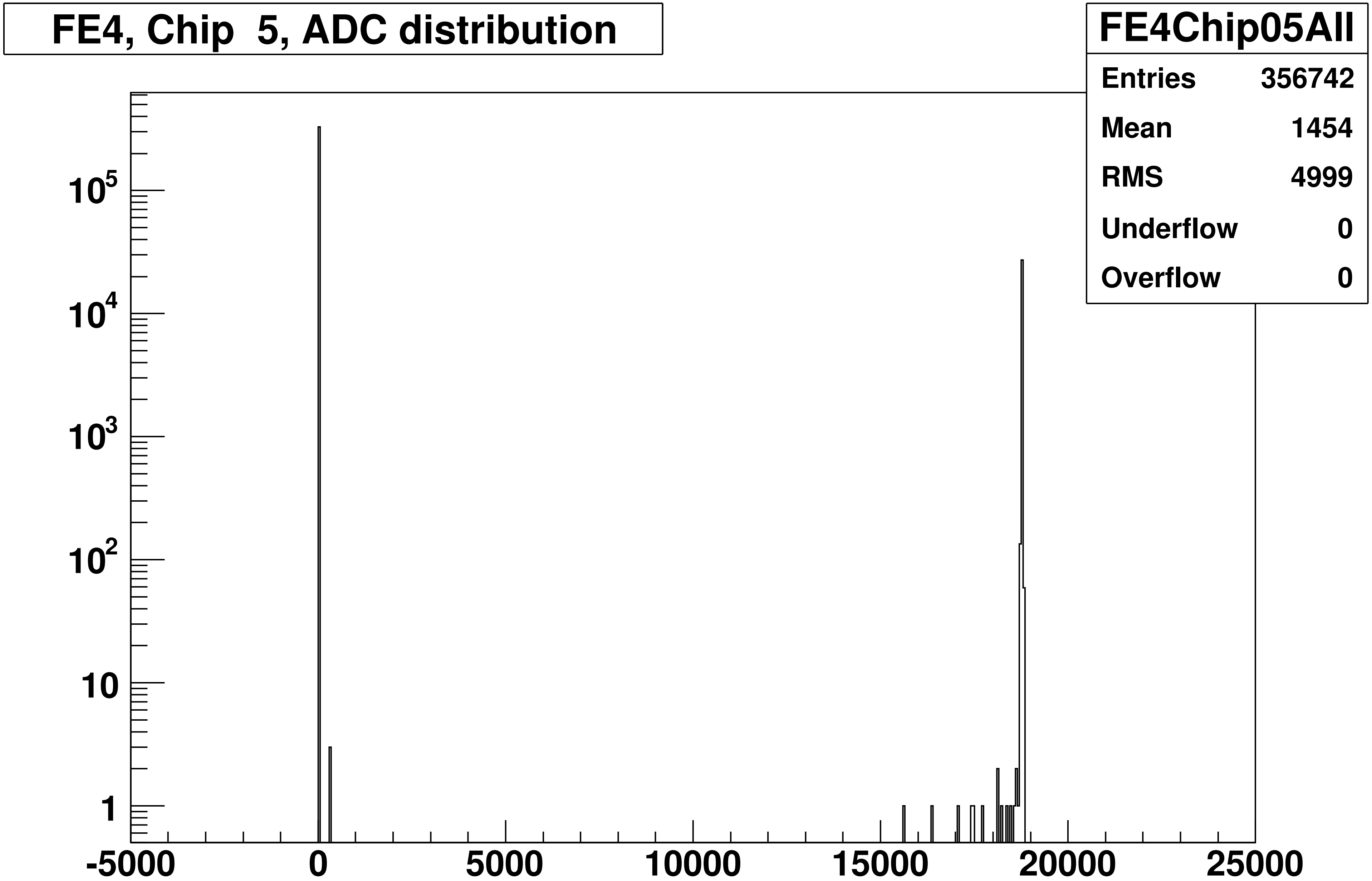
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 356742
Mean 1.87e+04
RMS 7.44
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 356742
Mean 1454
RMS 4999
Underflow 0
Overflow 0
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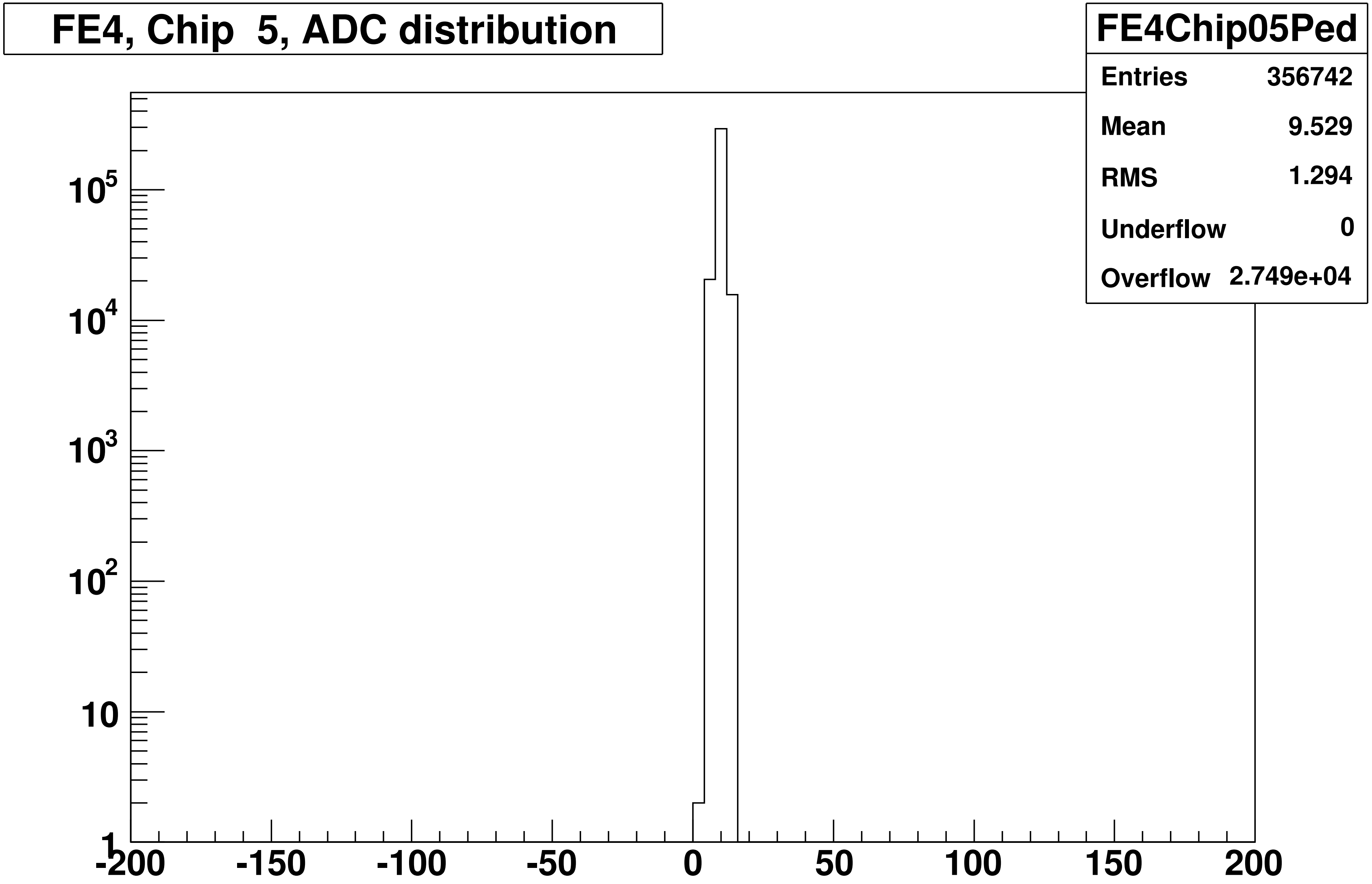
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 356742
Mean 9.529
RMS 1.294
Underflow 0
Overflow 2.749e+04
10^5
10^4
10^3
10^2
10
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-200
-150
-100
-50
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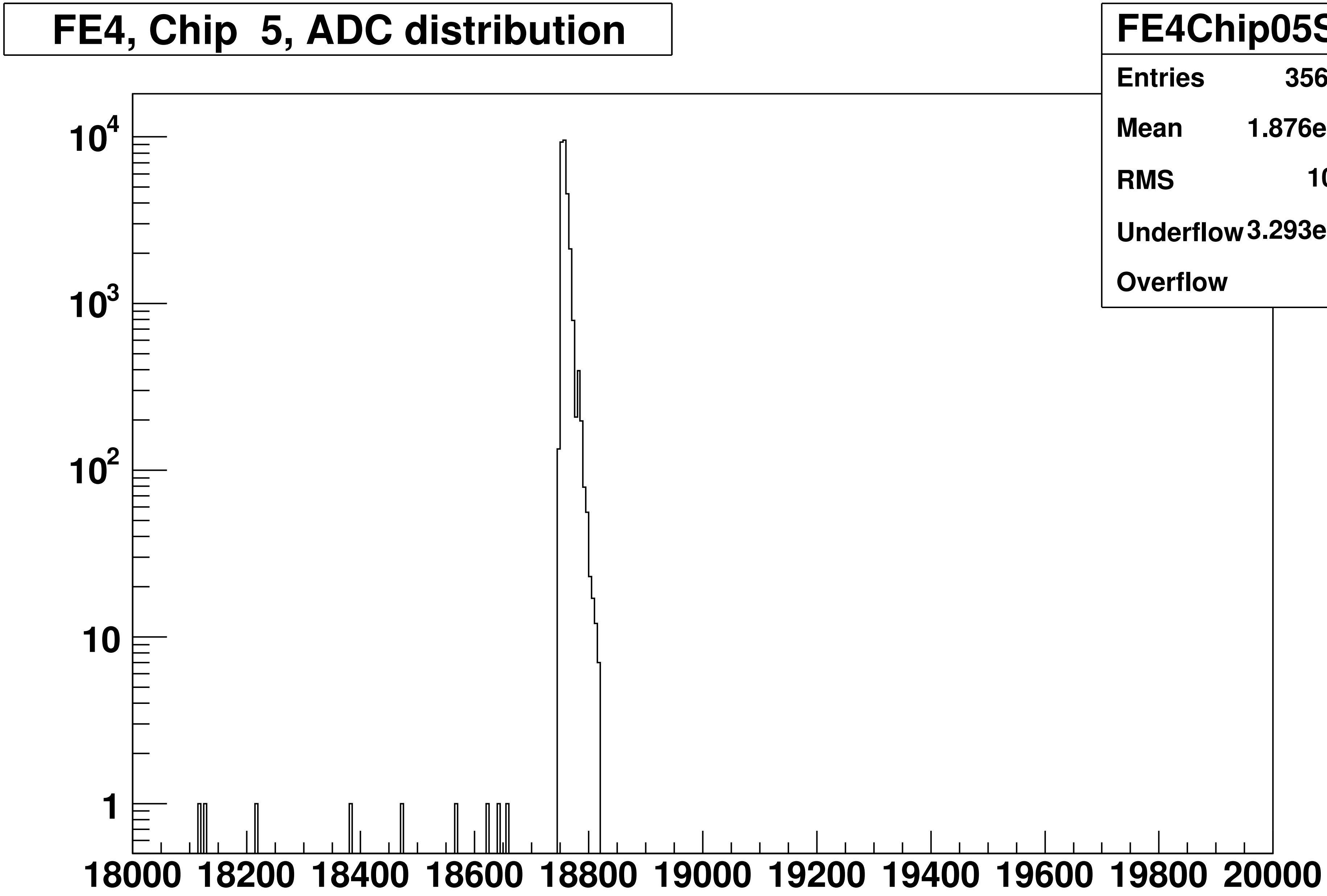
100
150
200



FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 356742
Mean 1.876e+04
RMS 10.28
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
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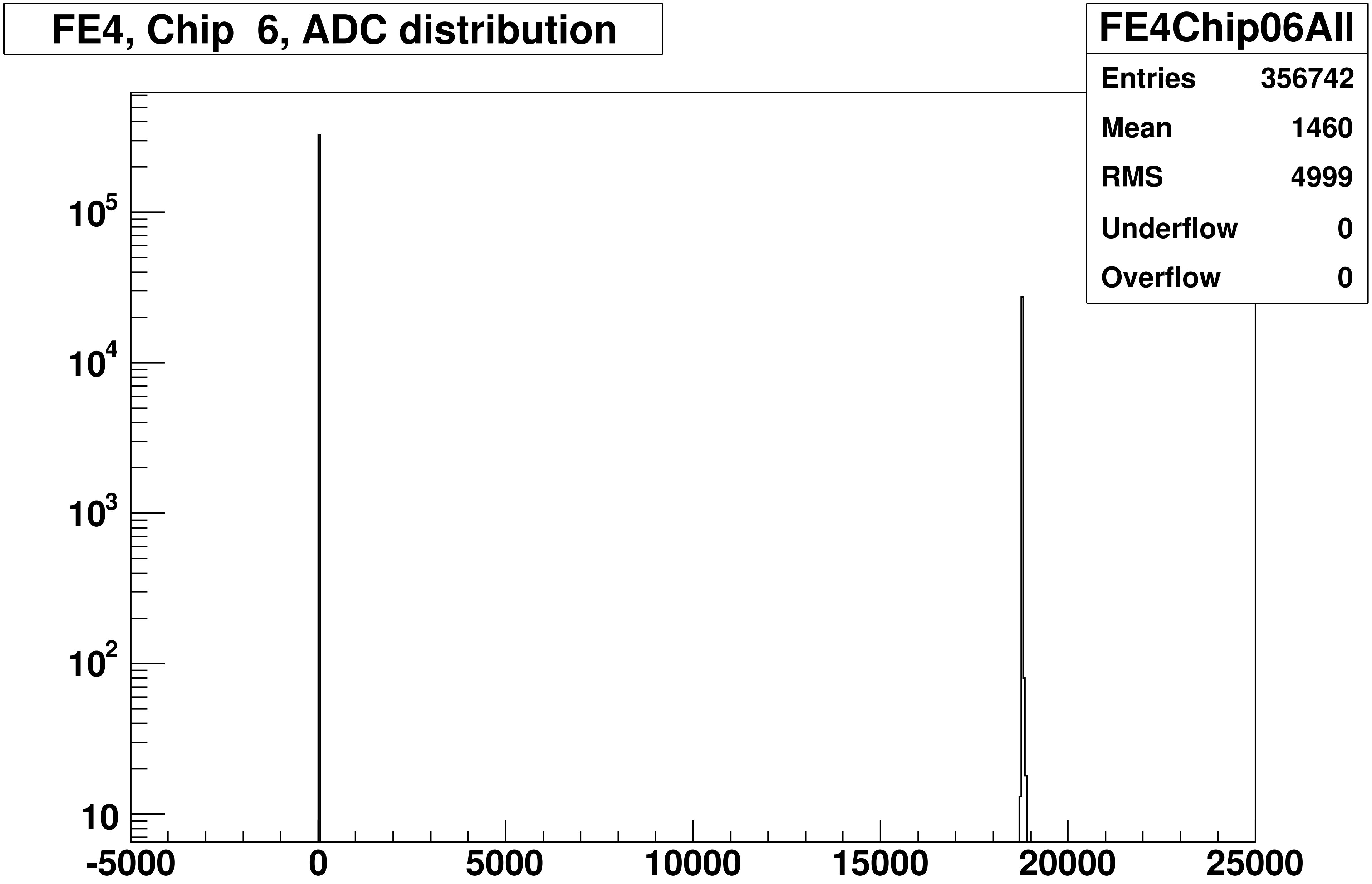
FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 356742
Mean 1460
RMS 4999
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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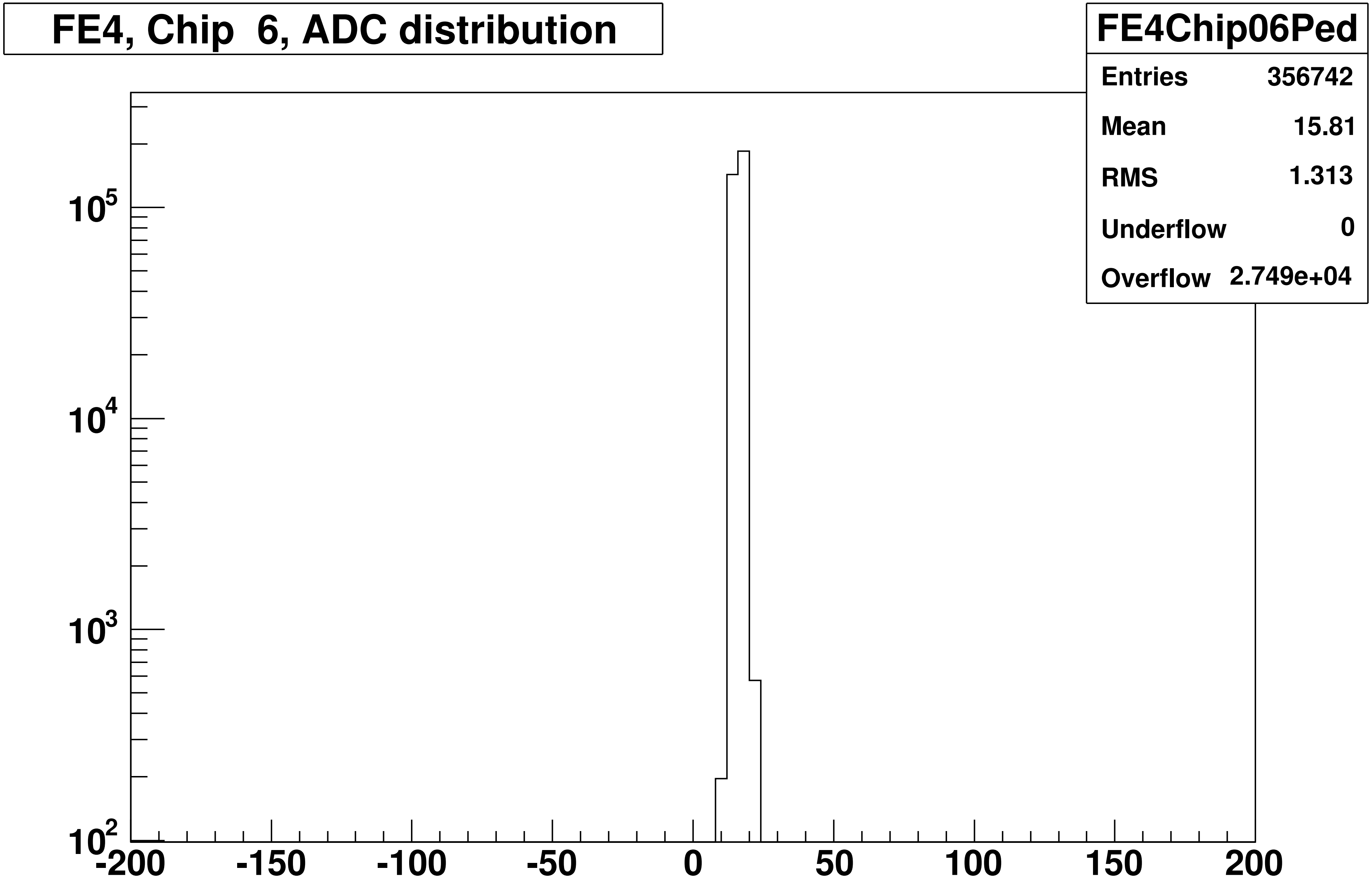

FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 356742
Mean 15.81
RMS 1.313
Underflow 0
Overflow 2.749e+04
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10^4
10^3
10^2
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-100
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0
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150
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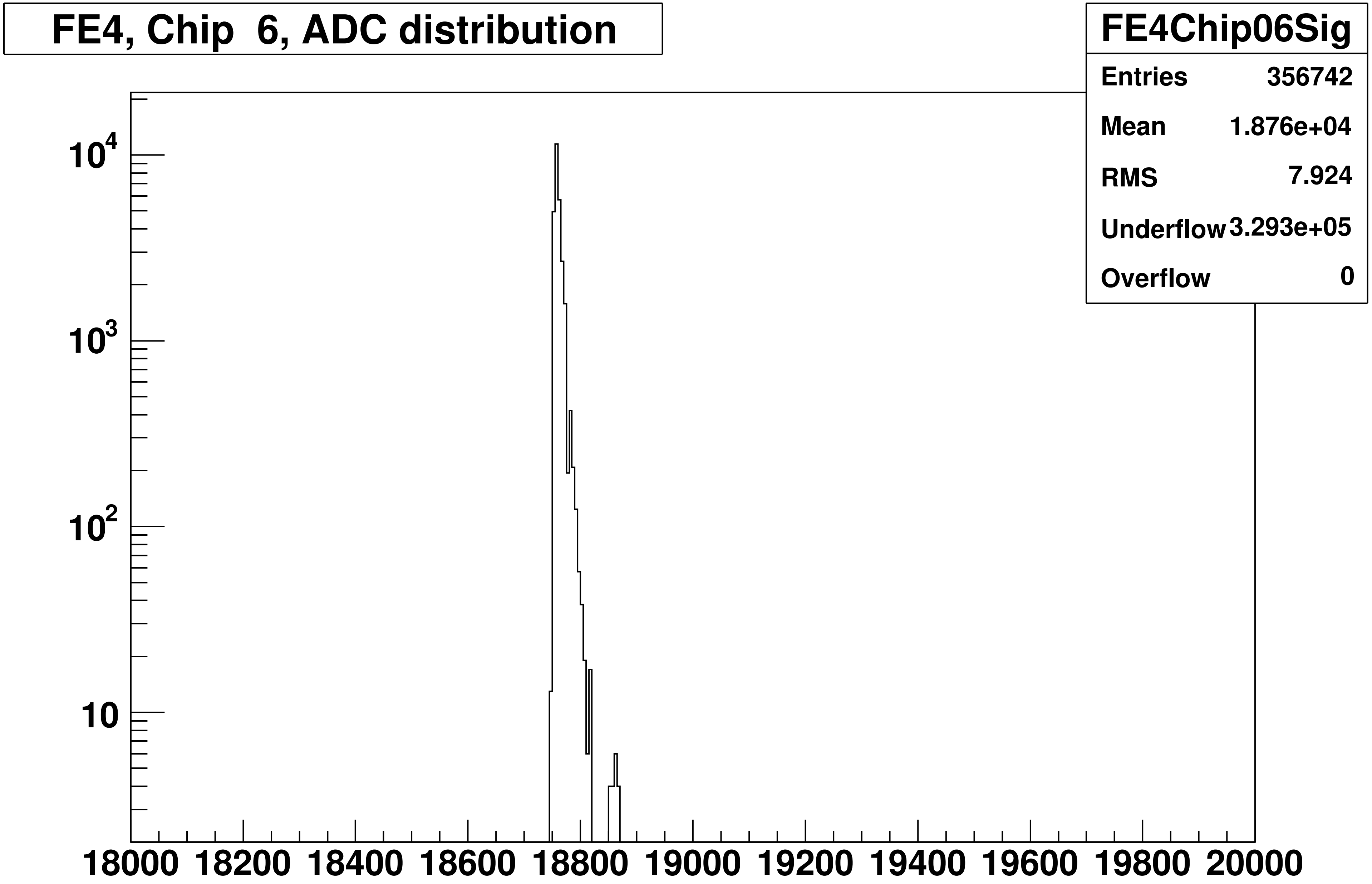

FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 356742
Mean 1.876e+04
RMS 7.924
Underflow 3.293e+05
Overflow 0
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10^3
10^2
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18000
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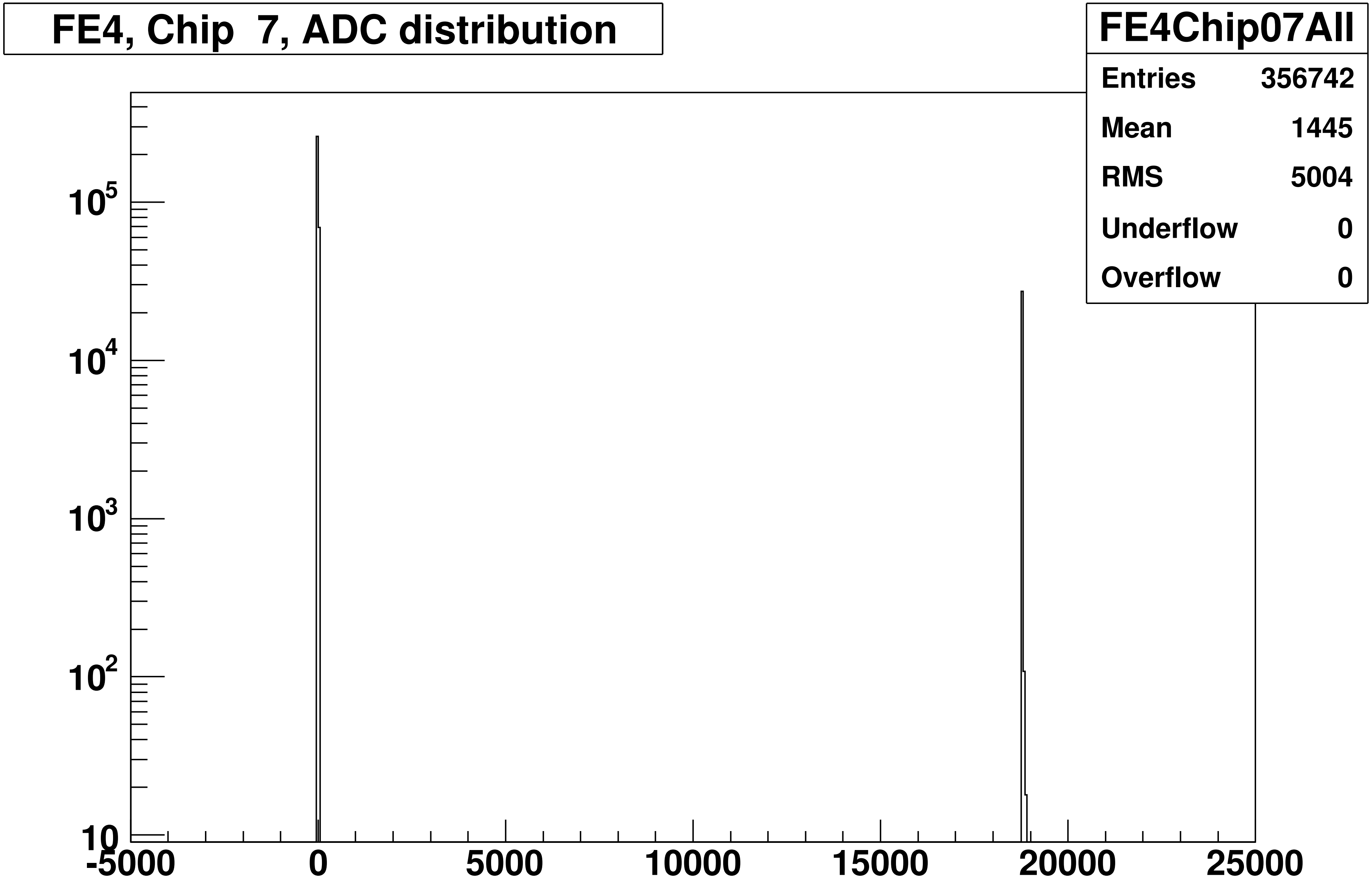

FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 356742
Mean 1445
RMS 5004
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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0
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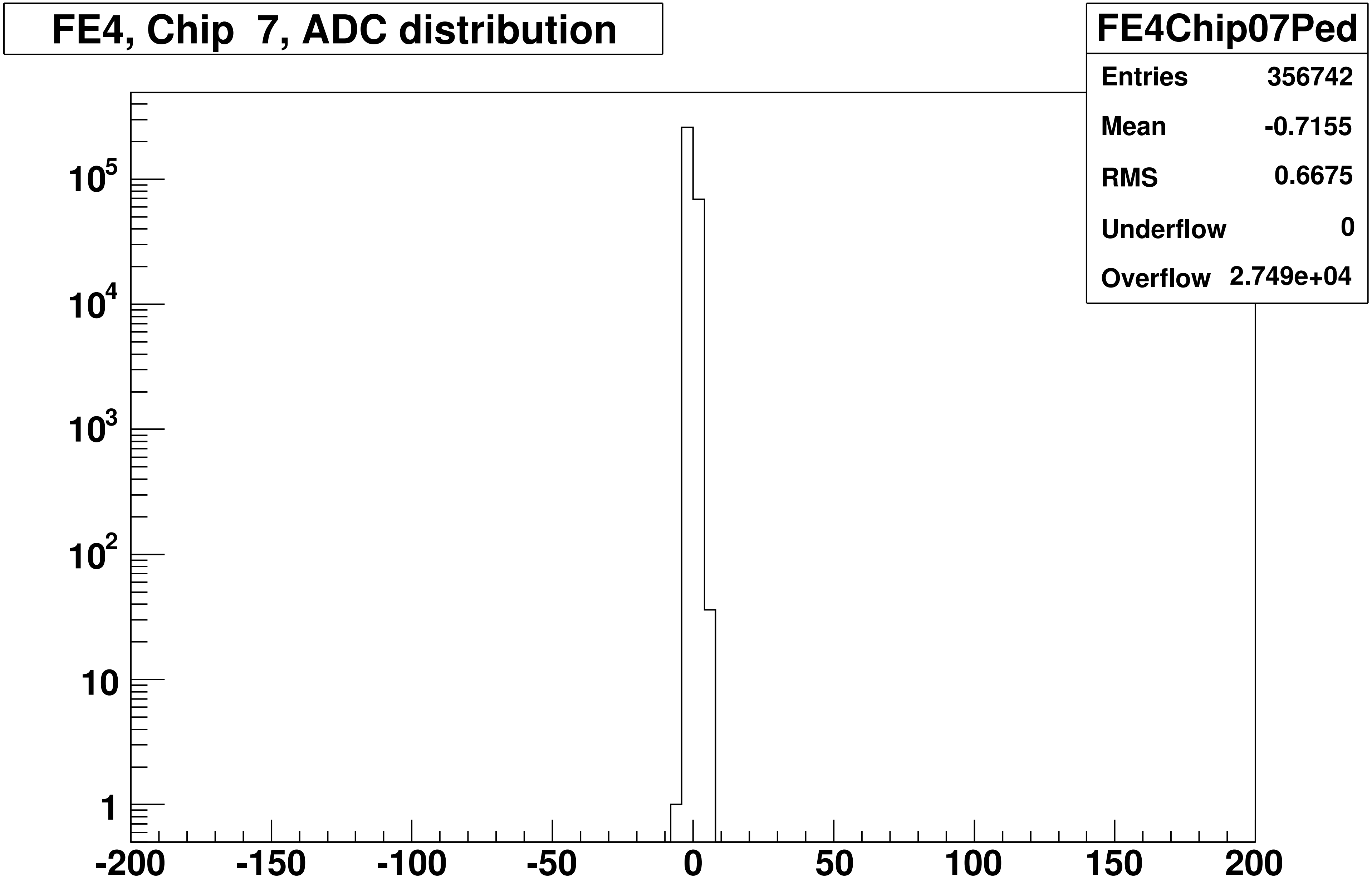
FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 356742
Mean -0.7155
RMS 0.6675
Underflow 0
Overflow 2.749e+04
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10^4
10^3
10^2
10
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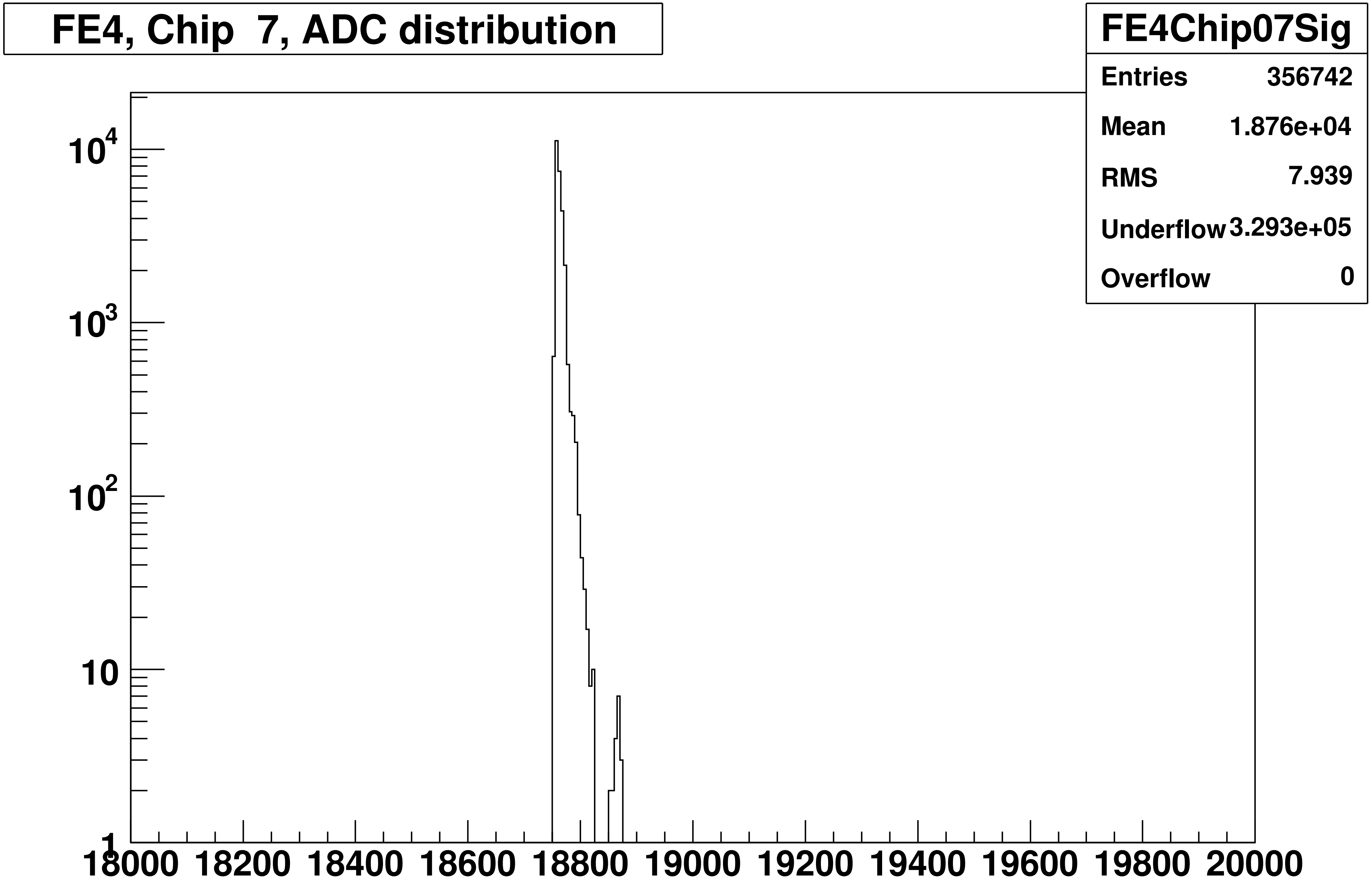
FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 356742
Mean 1.876e+04
RMS 7.939
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
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1
18000
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19000
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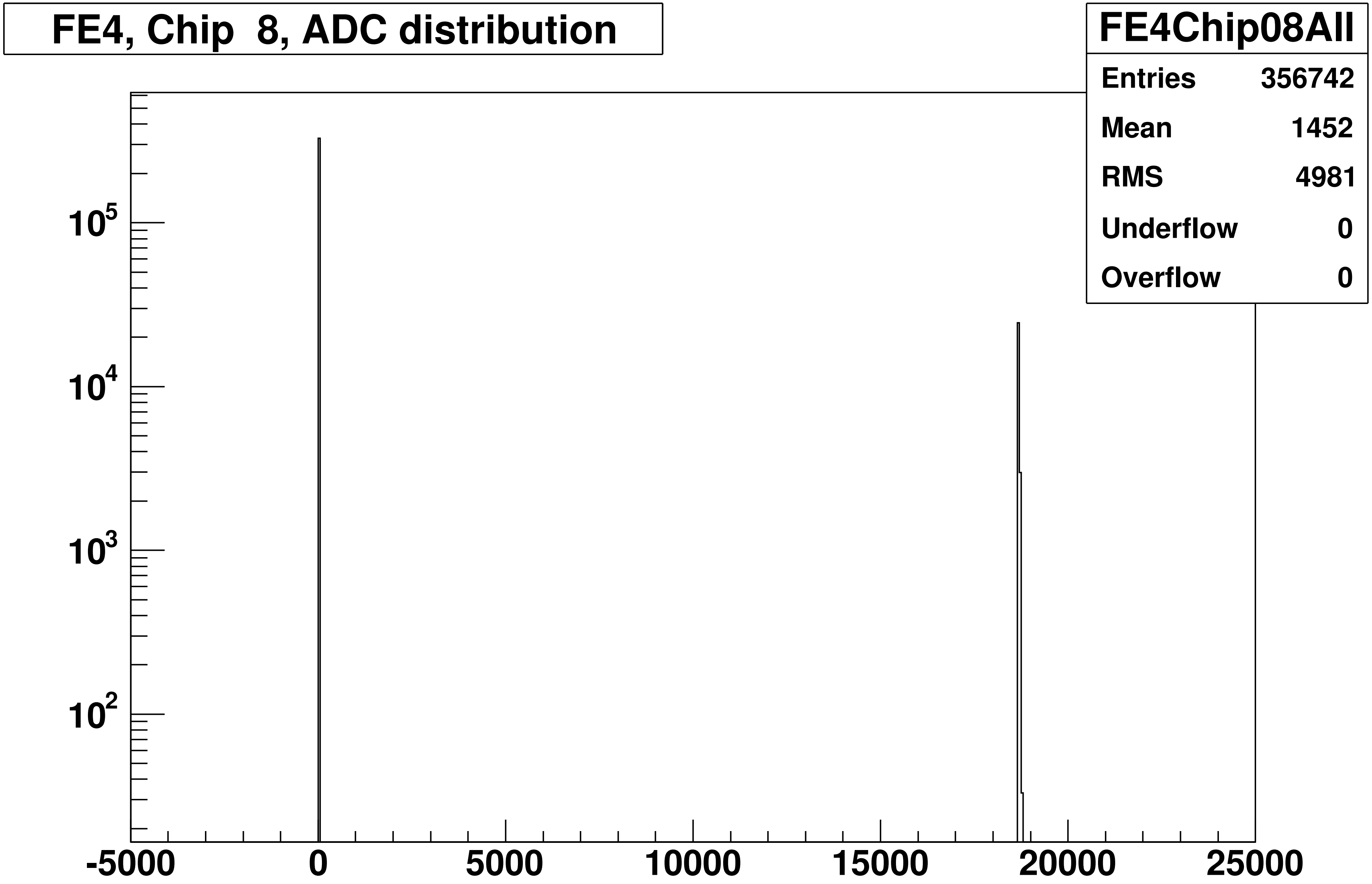
19400
19600
19800
20000


FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 356742
Mean 1452
RMS 4981
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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0
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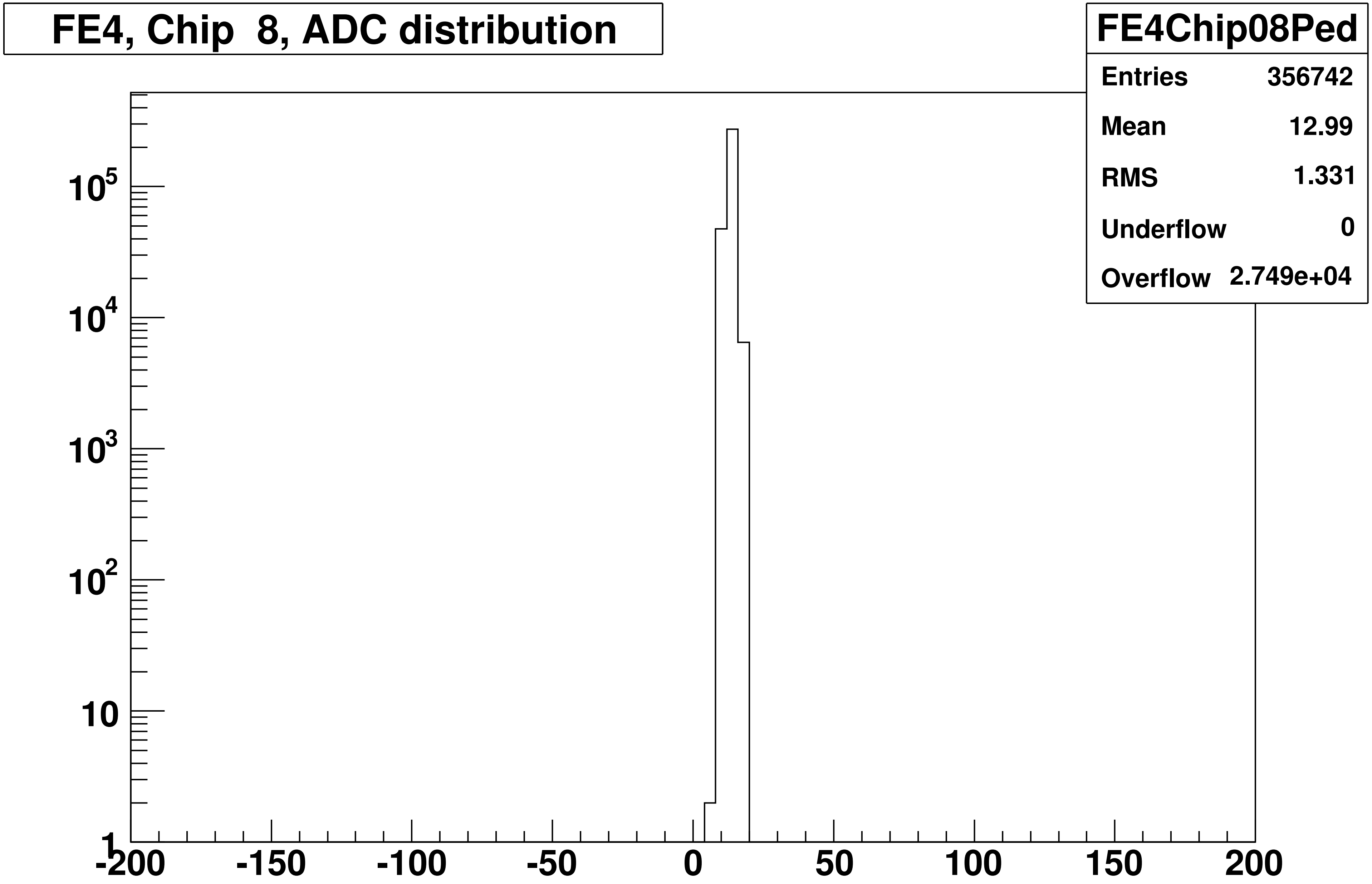
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 356742
Mean 12.99
RMS 1.331
Underflow 0
Overflow 2.749e+04
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10^4
10^3
10^2
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150
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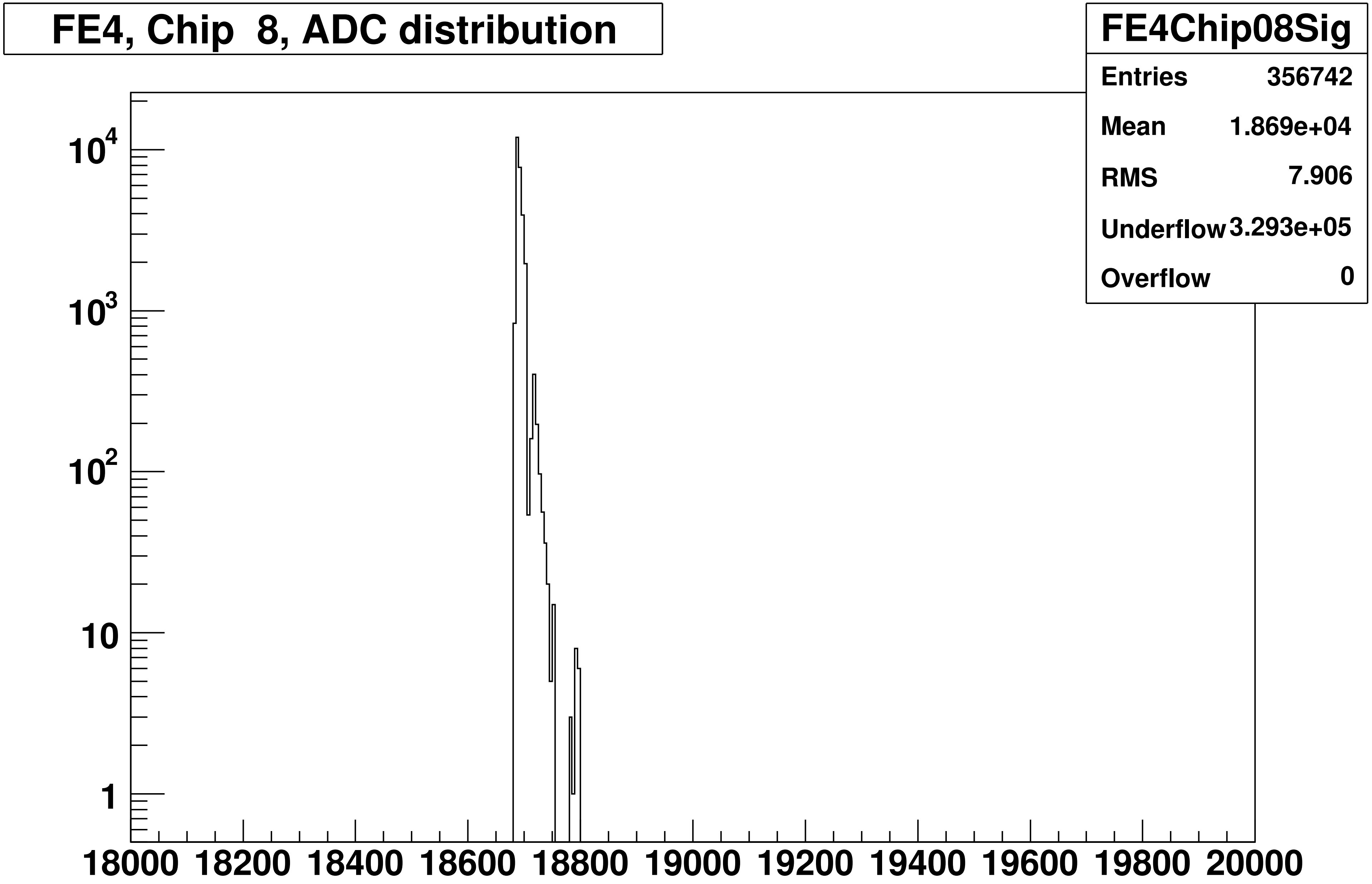

FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 356742
Mean 1.869e+04
RMS 7.906
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
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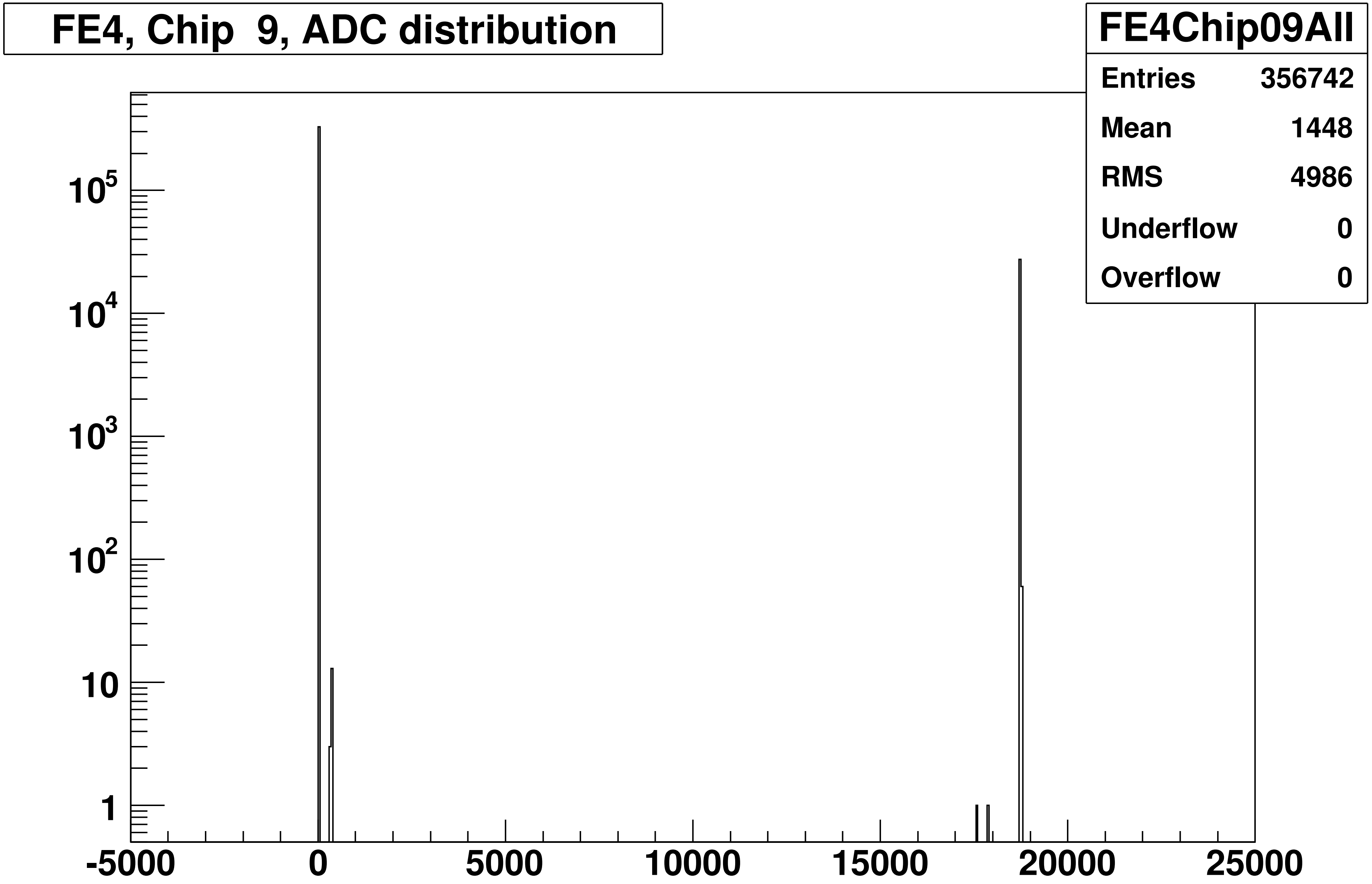
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 356742
Mean 1448
RMS 4986
Underflow 0
Overflow 0
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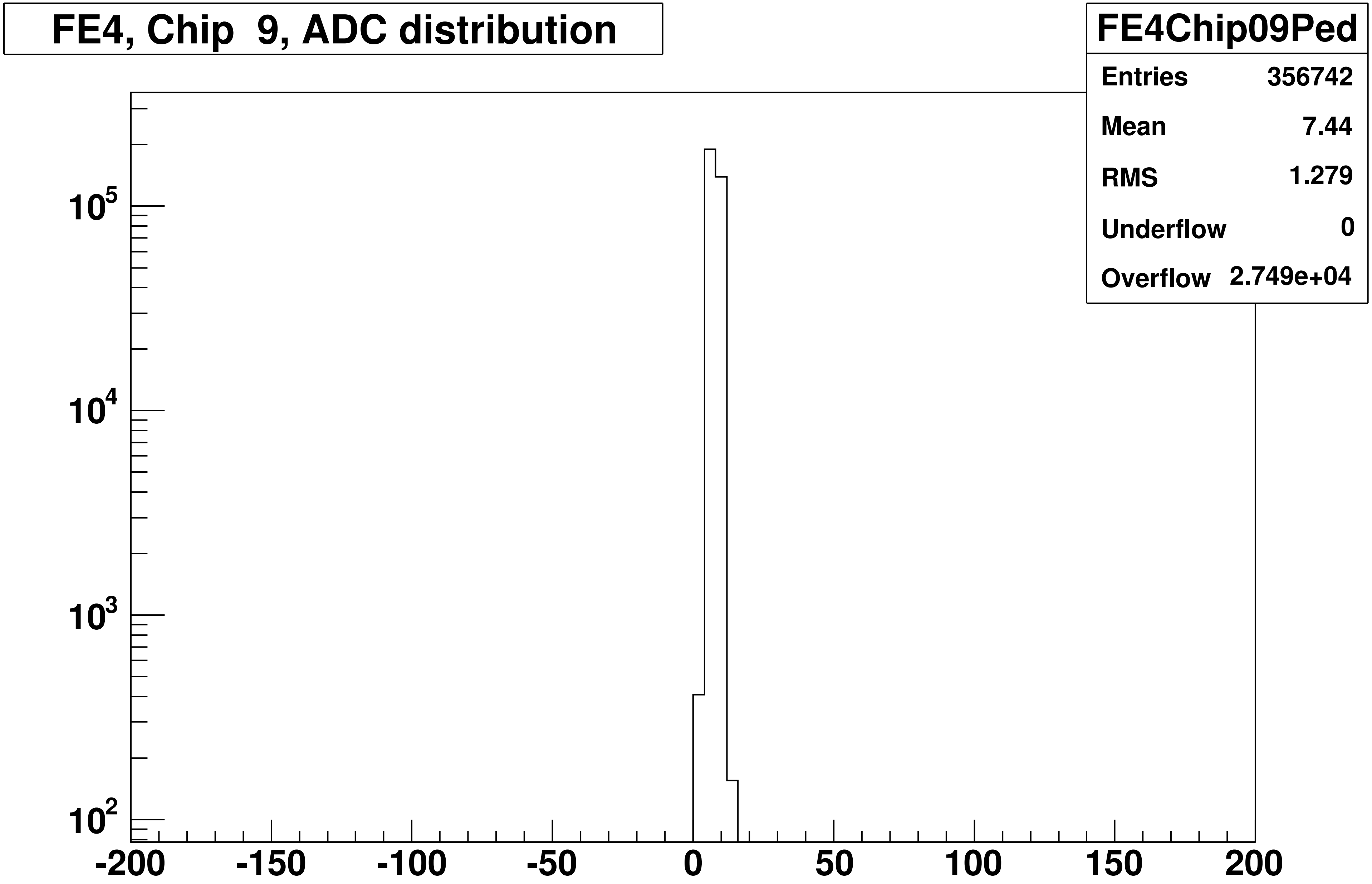
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 356742
Mean 7.44
RMS 1.279
Underflow 0
Overflow 2.749e+04
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10^4
10^3
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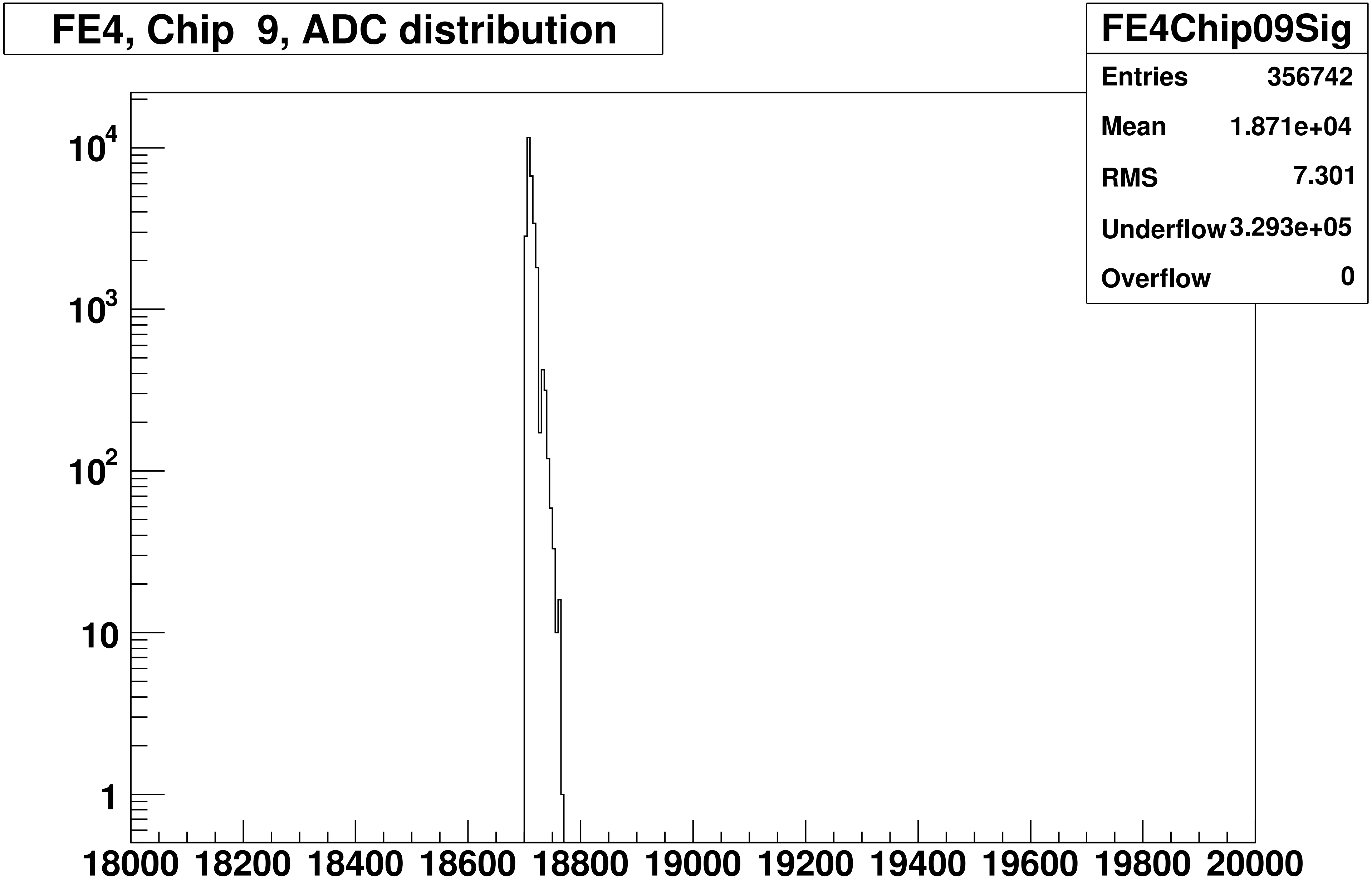
150
200



FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 356742
Mean 1.871e+04
RMS 7.301
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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19400
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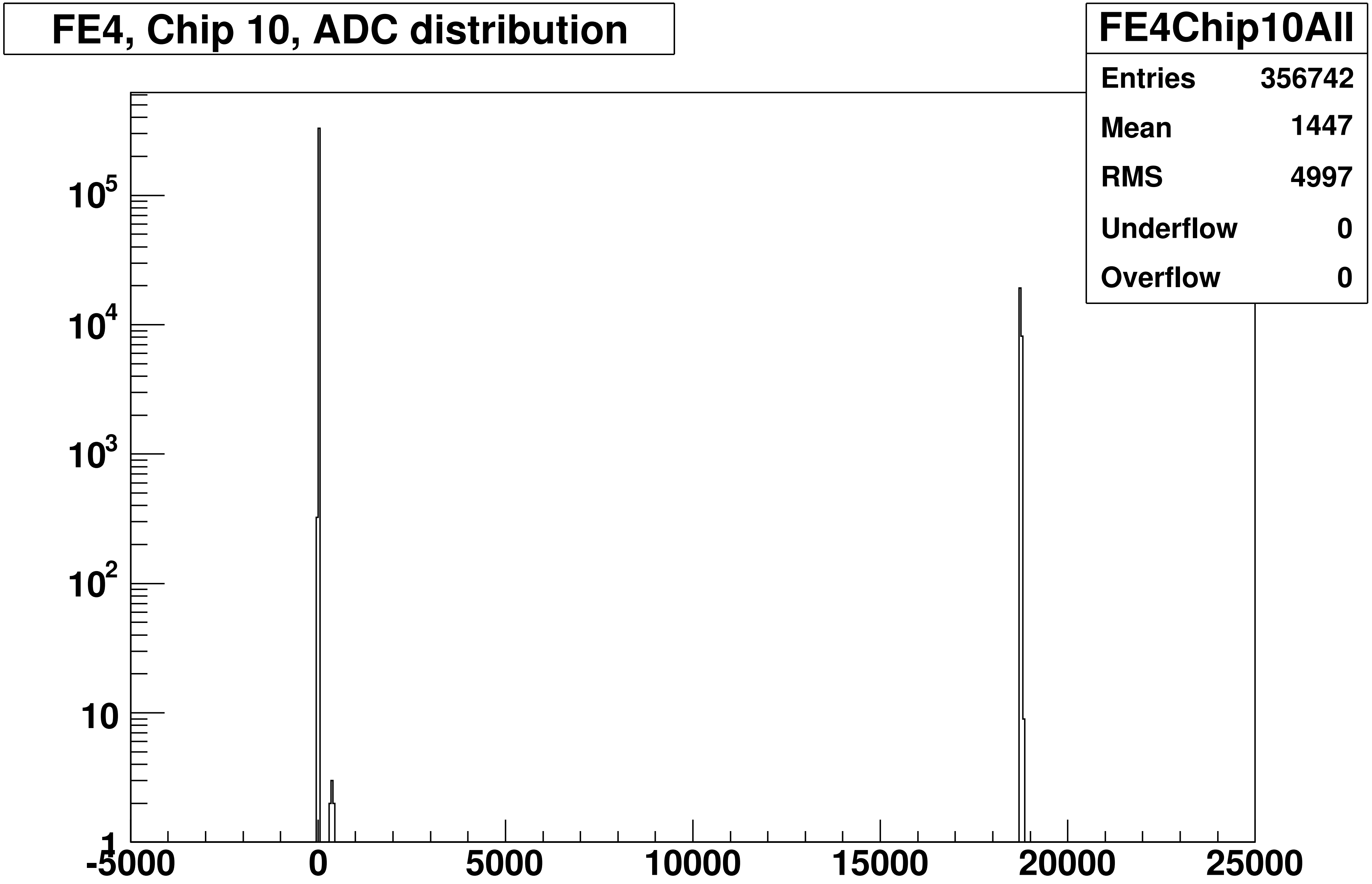
19800
20000



FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 356742
Mean 1447
RMS 4997
Underflow 0
Overflow 0
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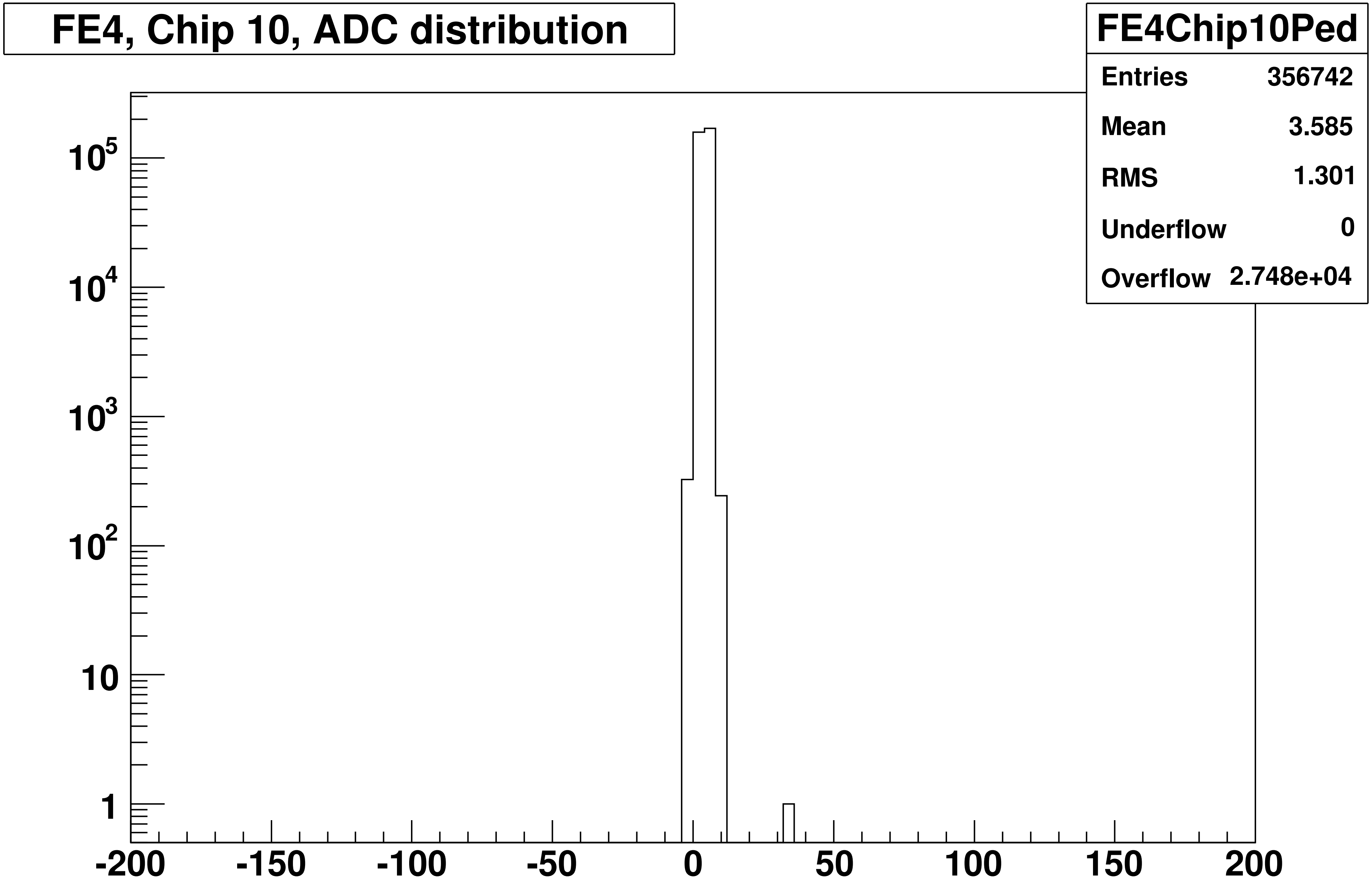
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 356742
Mean 3.585
RMS 1.301
Underflow 0
Overflow 2.748e+04
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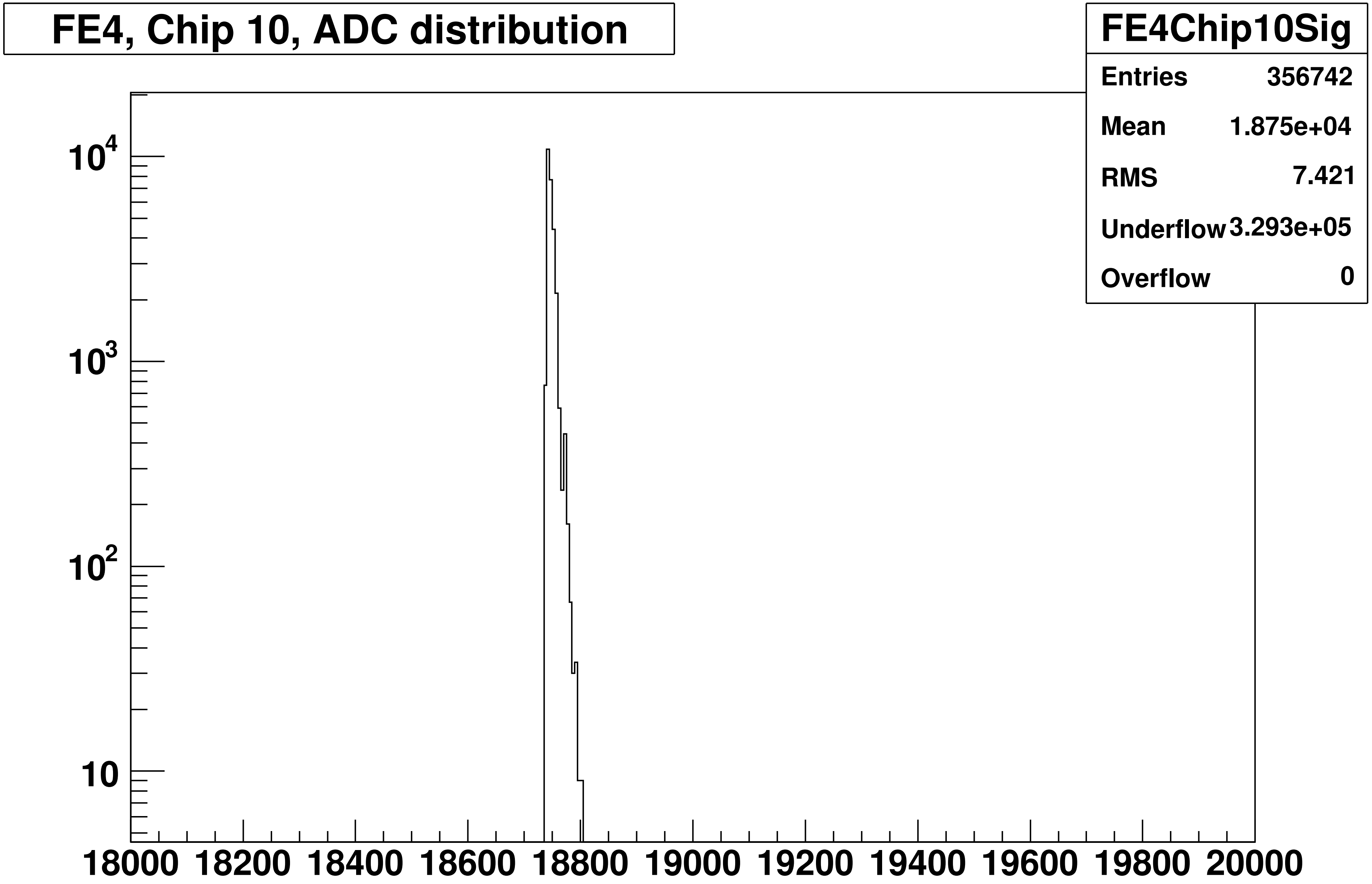
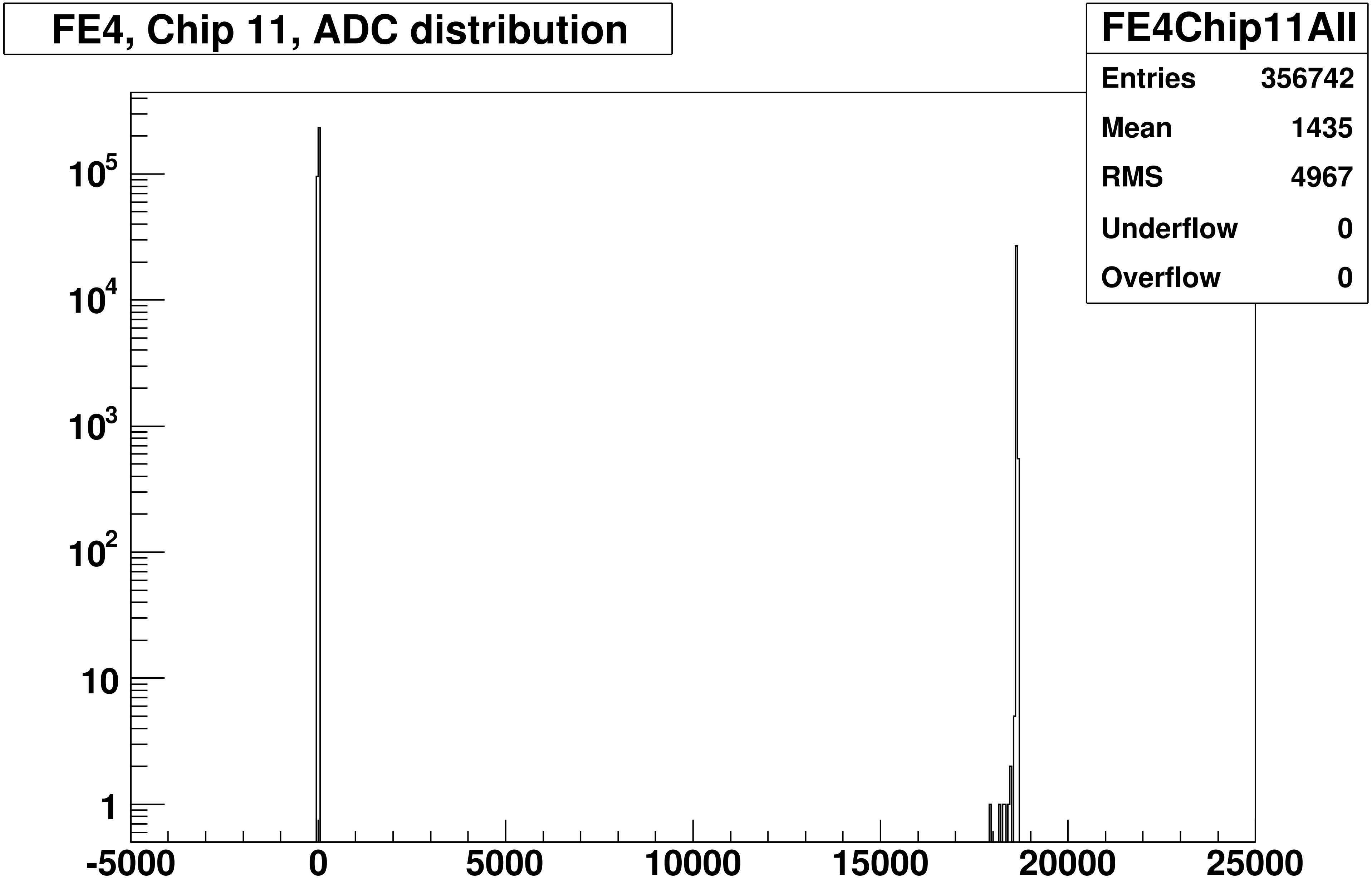
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 356742
Mean 1.875e+04
RMS 7.421
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 356742
Mean 1435
RMS 4967
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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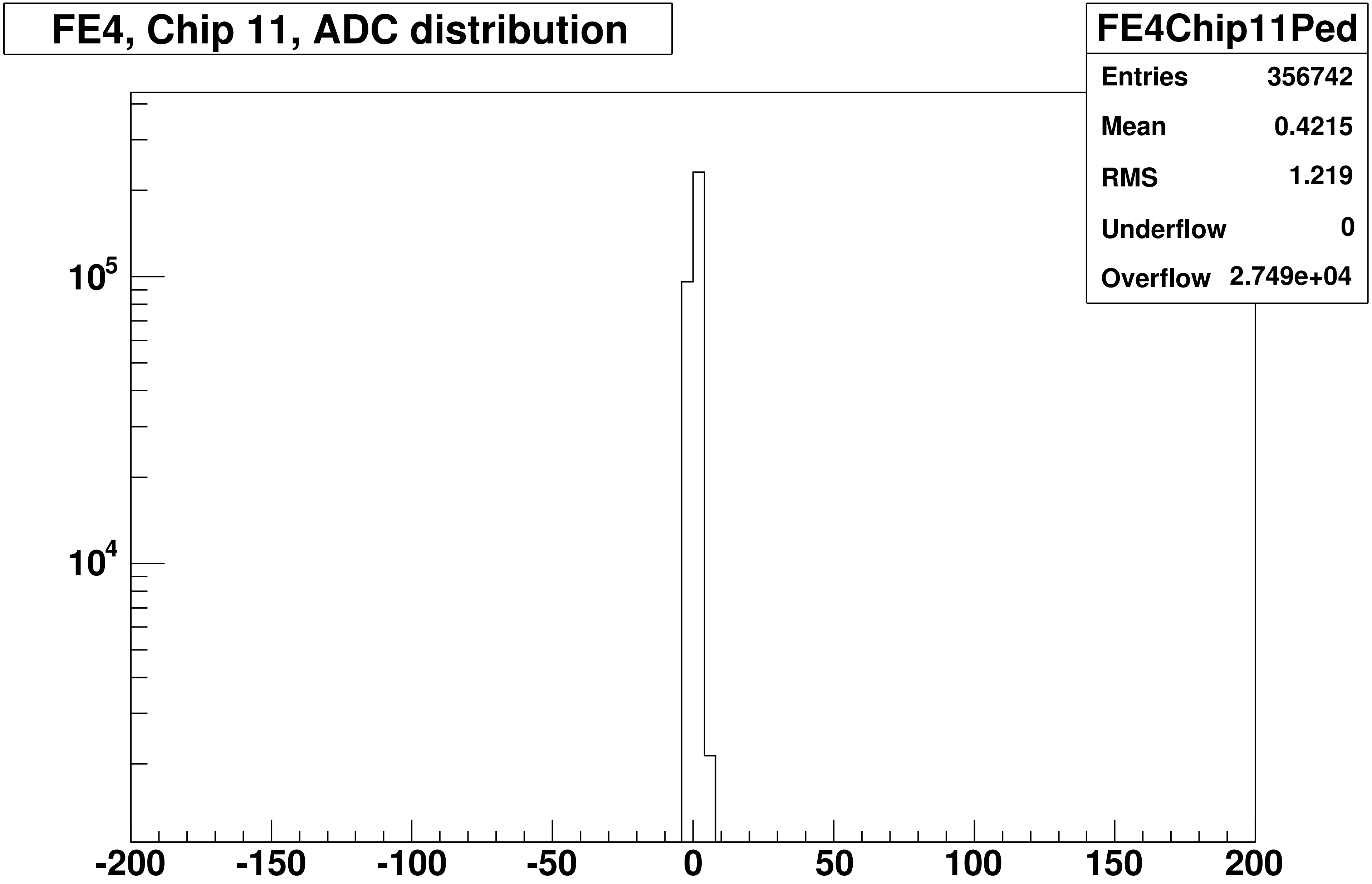
10000
15000
20000
25000


FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 356742
Mean 0.4215
RMS 1.219
Underflow 0
Overflow 2.749e+04
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10^4
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-100
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0
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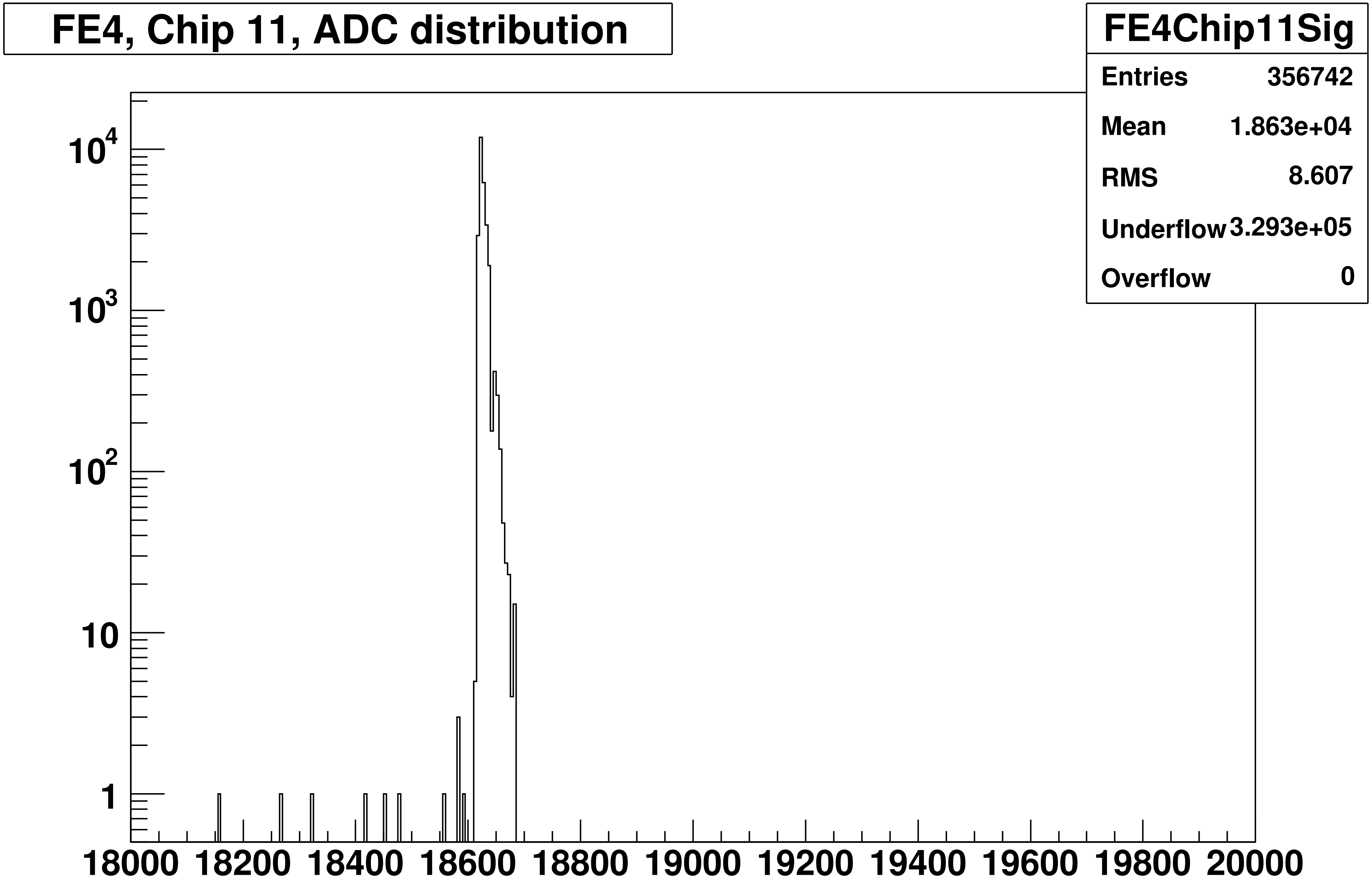
100
150
200


FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 356742
Mean 1.863e+04
RMS 8.607
Underflow 3.293e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
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19000
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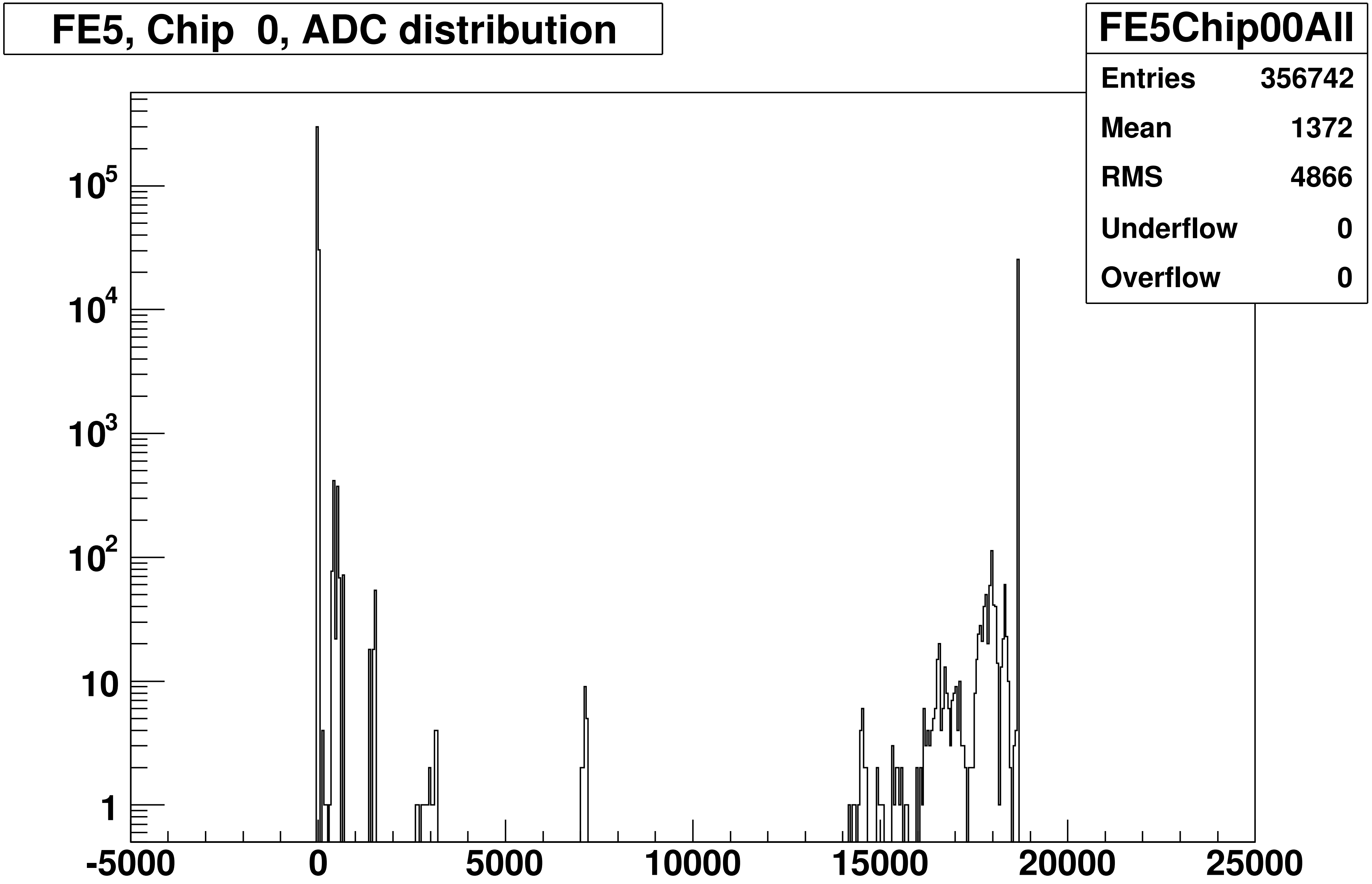
19400
19600
19800
20000



FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 356742
Mean 1372
RMS 4866
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
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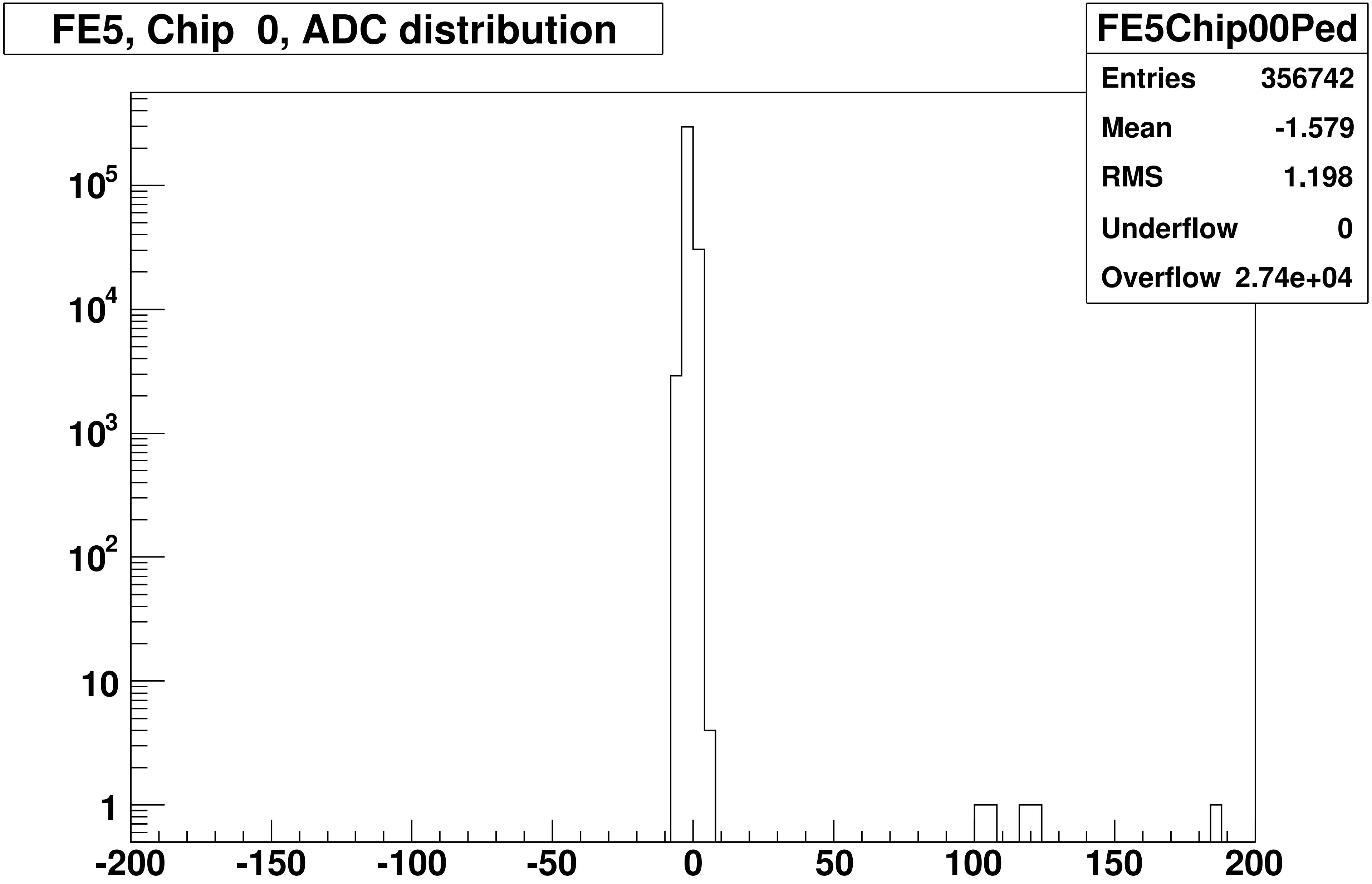
25000



FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 356742
Mean -1.579
RMS 1.198
Underflow 0
Overflow 2.74e+04
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10^3
10^2
10
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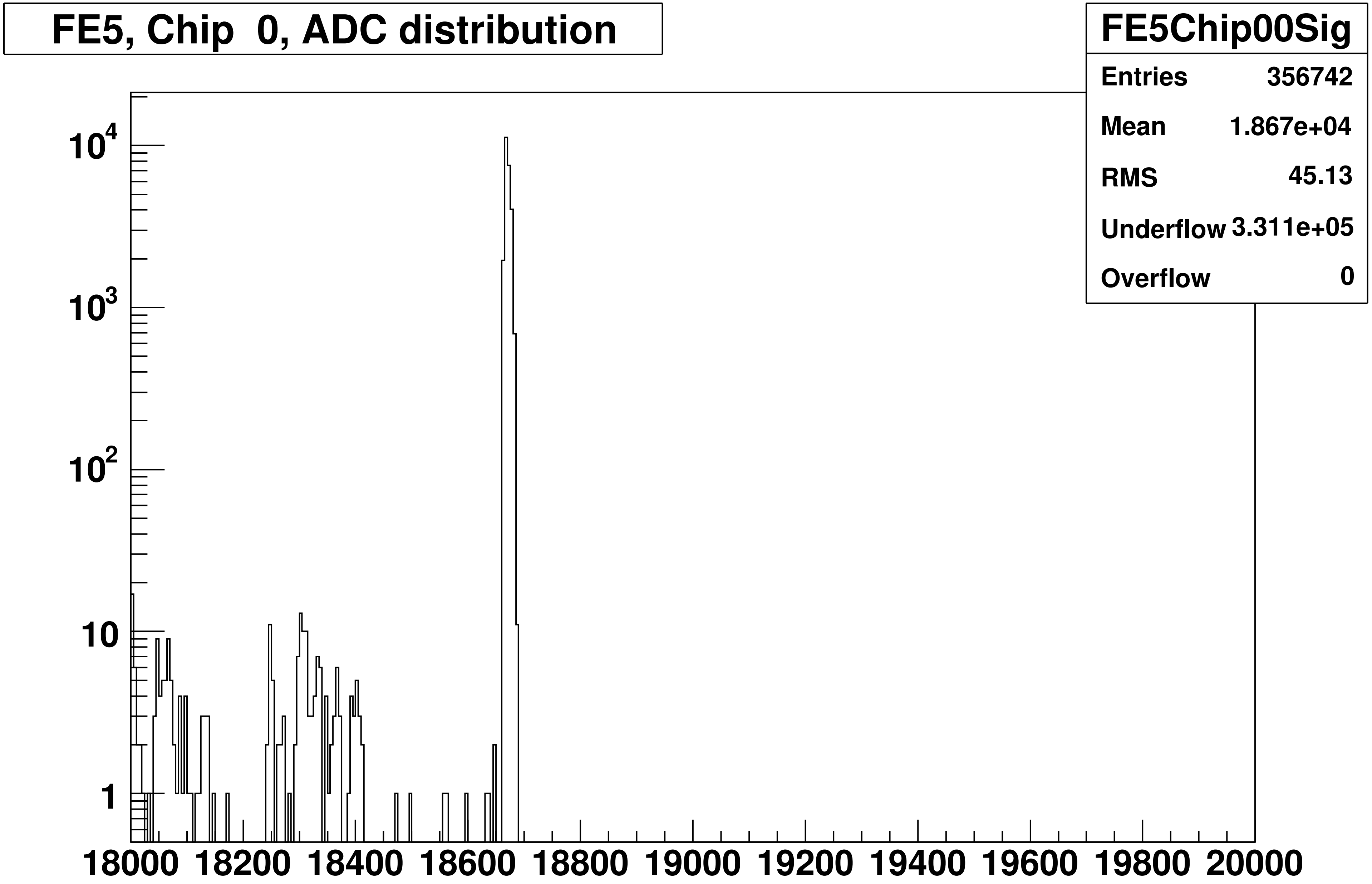
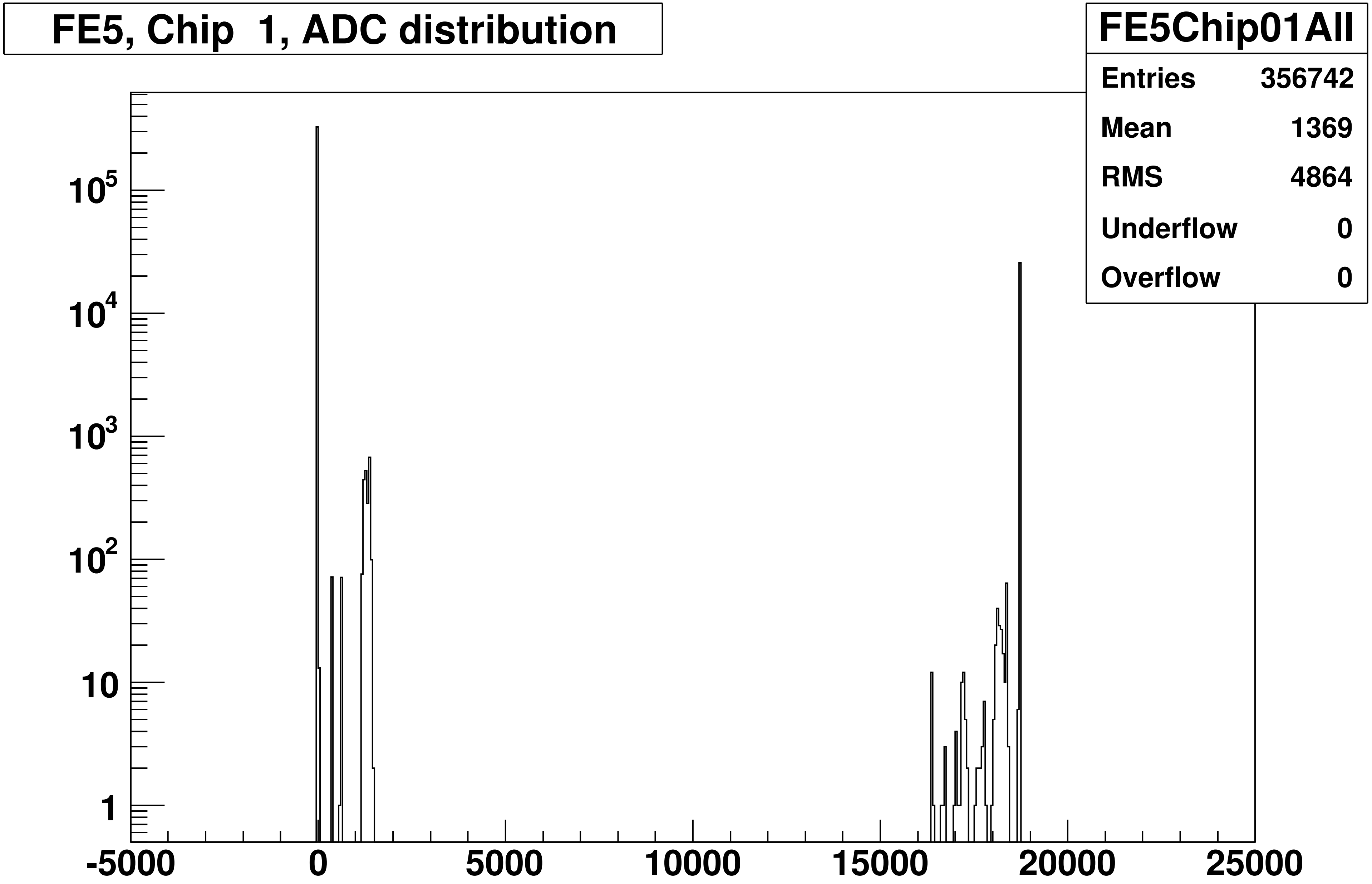
100
150
200


FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 356742
Mean 1.867e+04
RMS 45.13
Underflow 3.311e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 356742
Mean 1369
RMS 4864
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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10000
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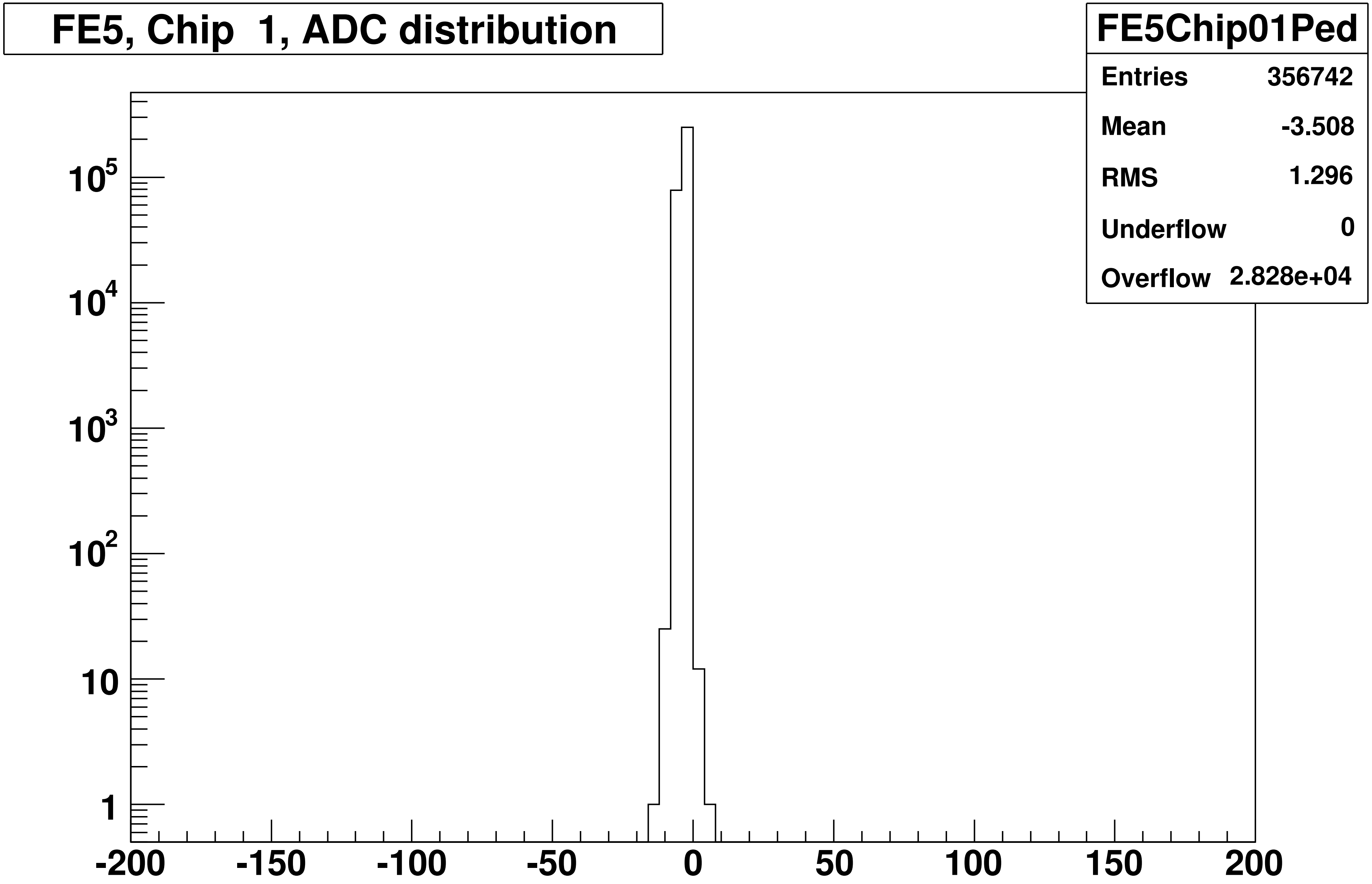
20000
25000


FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 356742
Mean -3.508
RMS 1.296
Underflow 0
Overflow 2.828e+04
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10^4
10^3
10^2
10
1
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-100
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150
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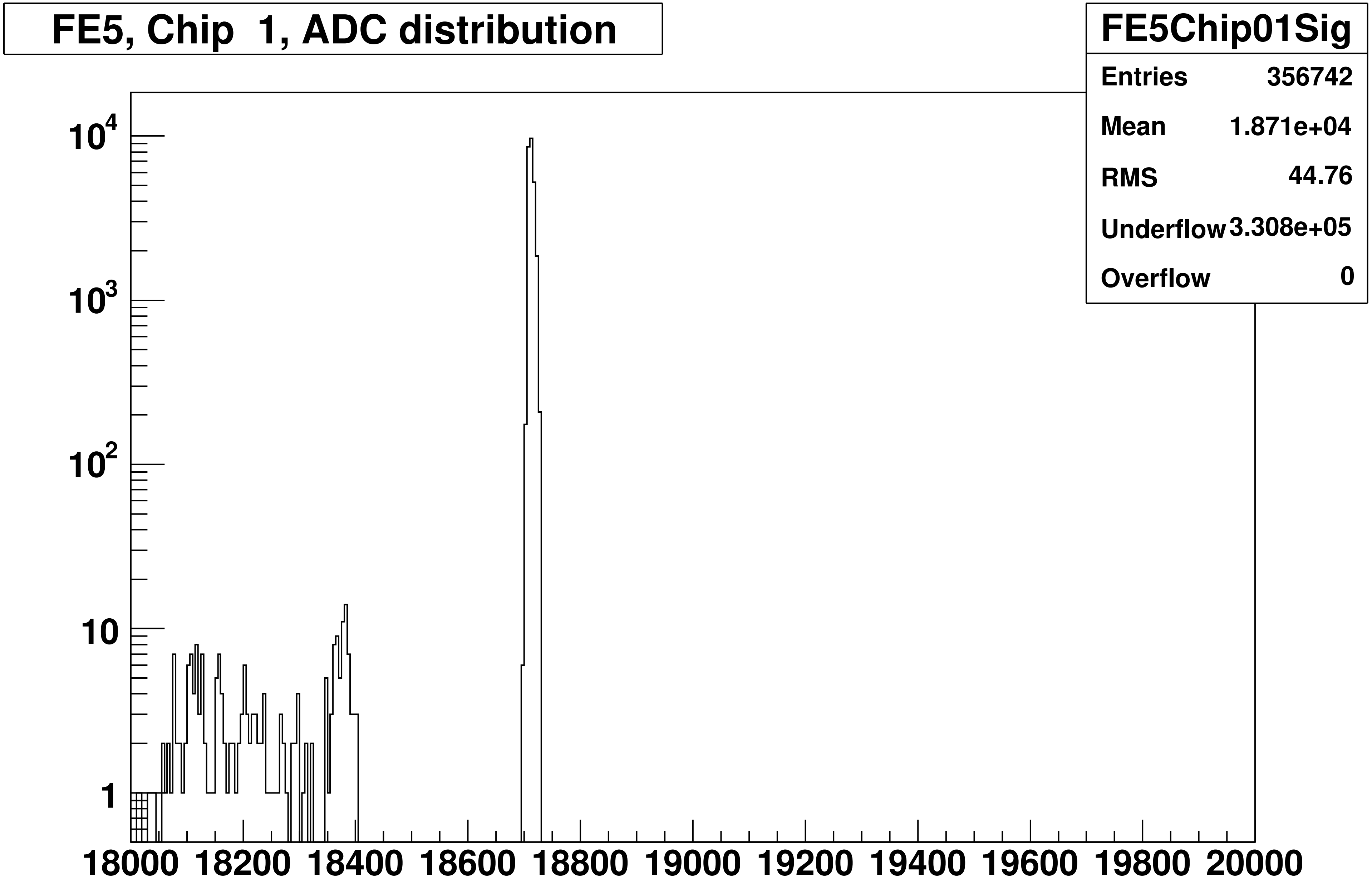
FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 356742
Mean 1.871e+04
RMS 44.76
Underflow 3.308e+05
Overflow 0
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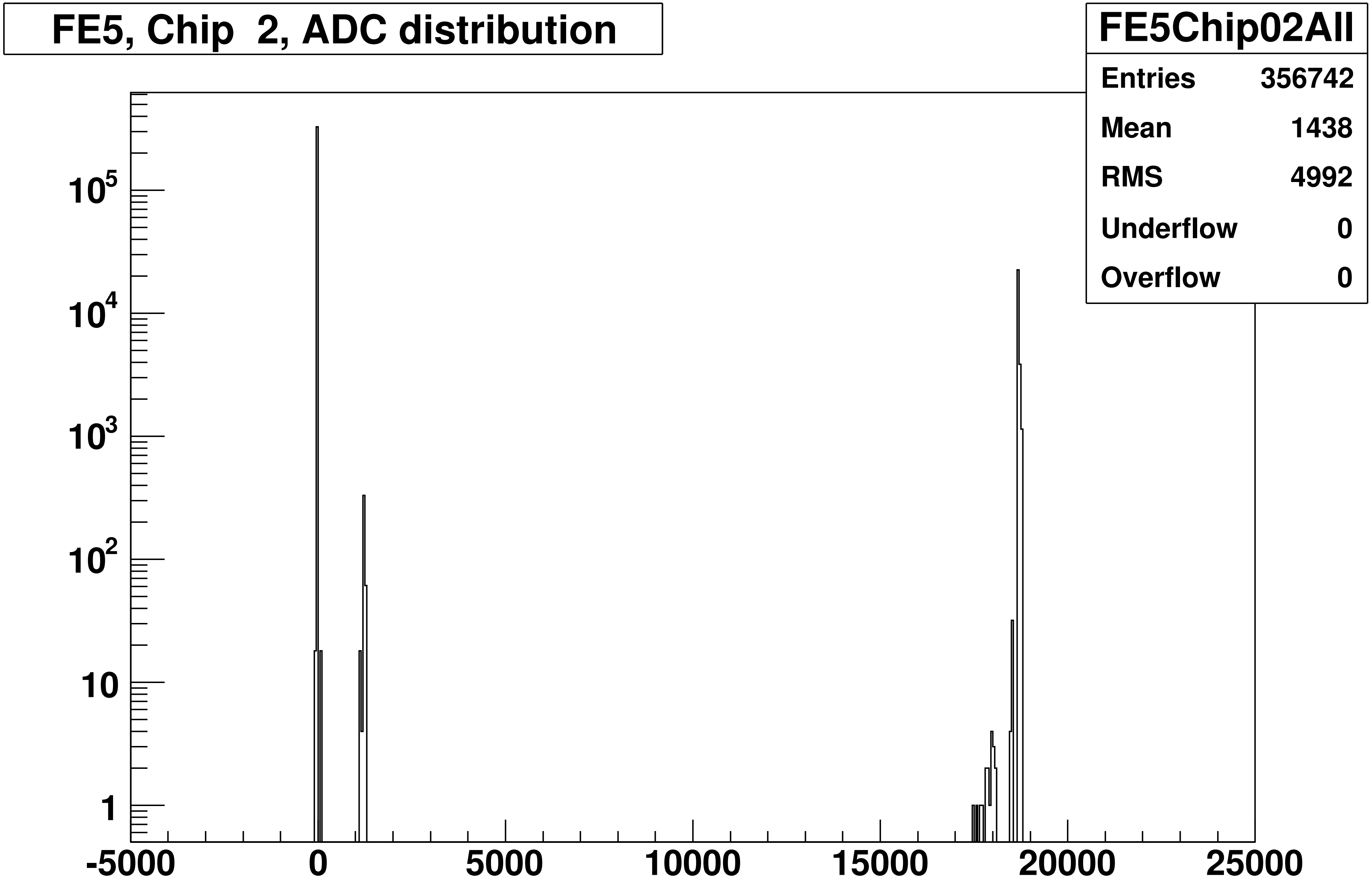
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 356742
Mean 1438
RMS 4992
Underflow 0
Overflow 0
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10^3
10^2
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1
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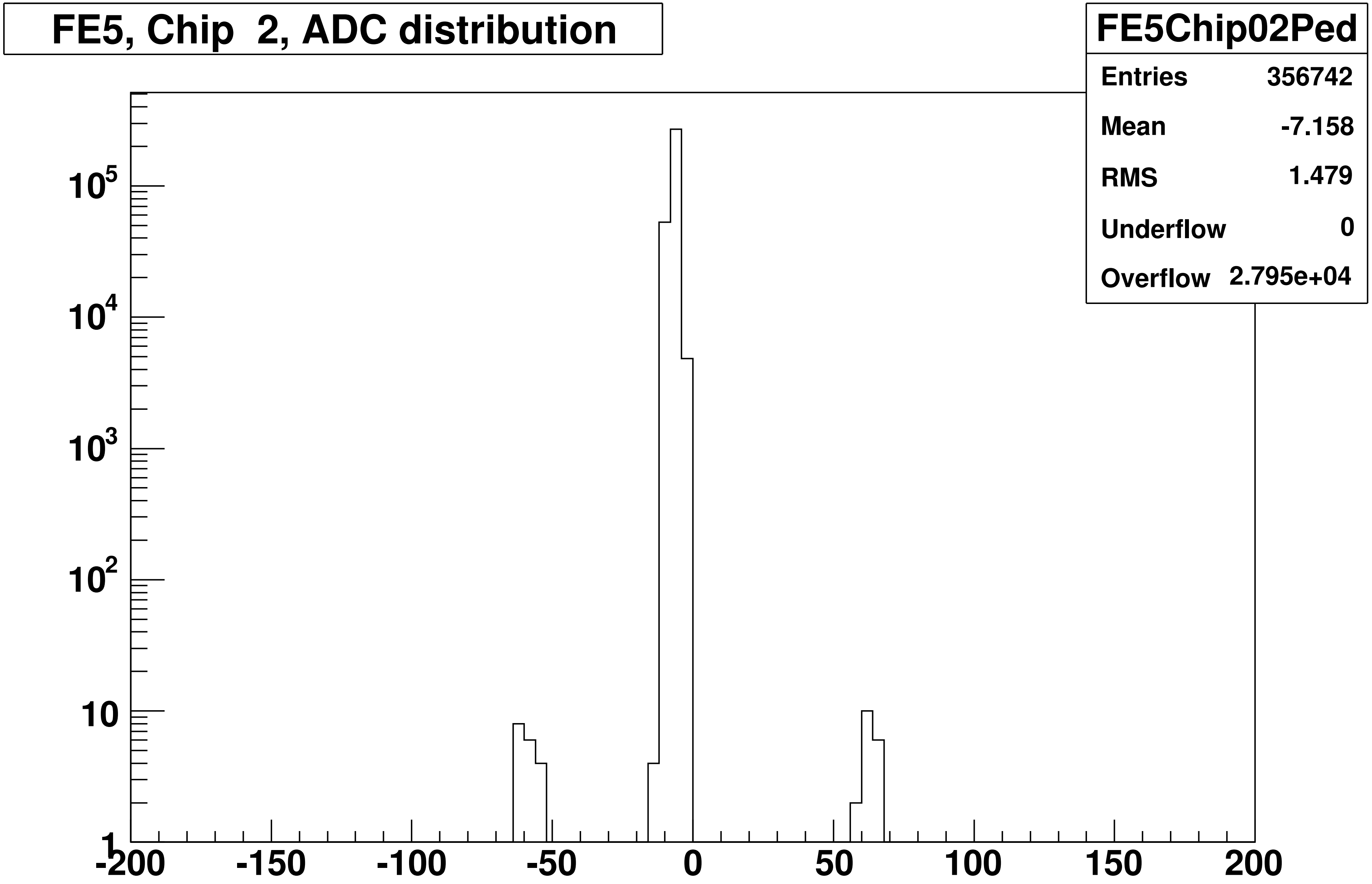
FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 356742
Mean -7.158
RMS 1.479
Underflow 0
Overflow 2.795e+04
10^5
10^4
10^3
10^2
10
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-100
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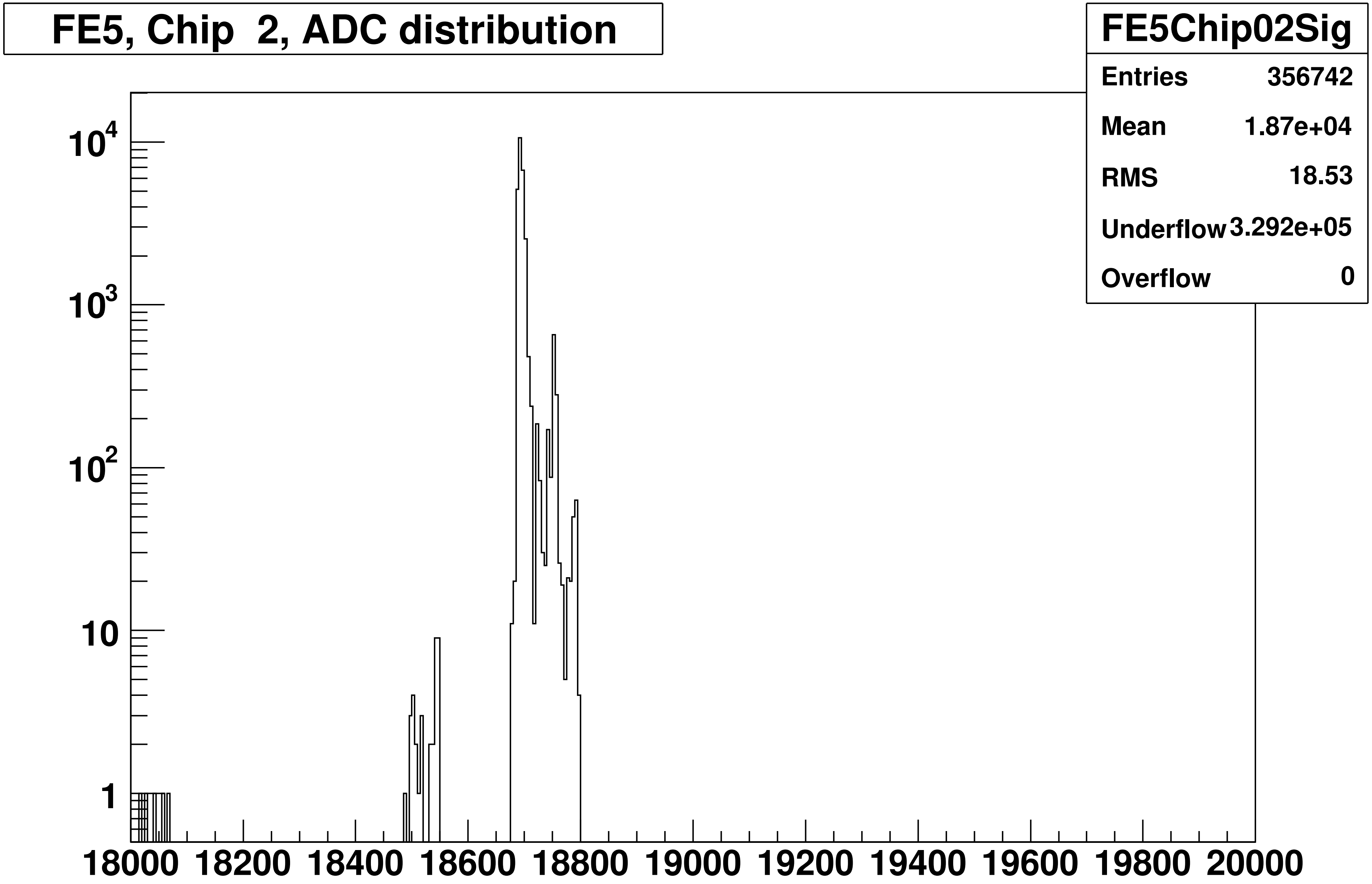
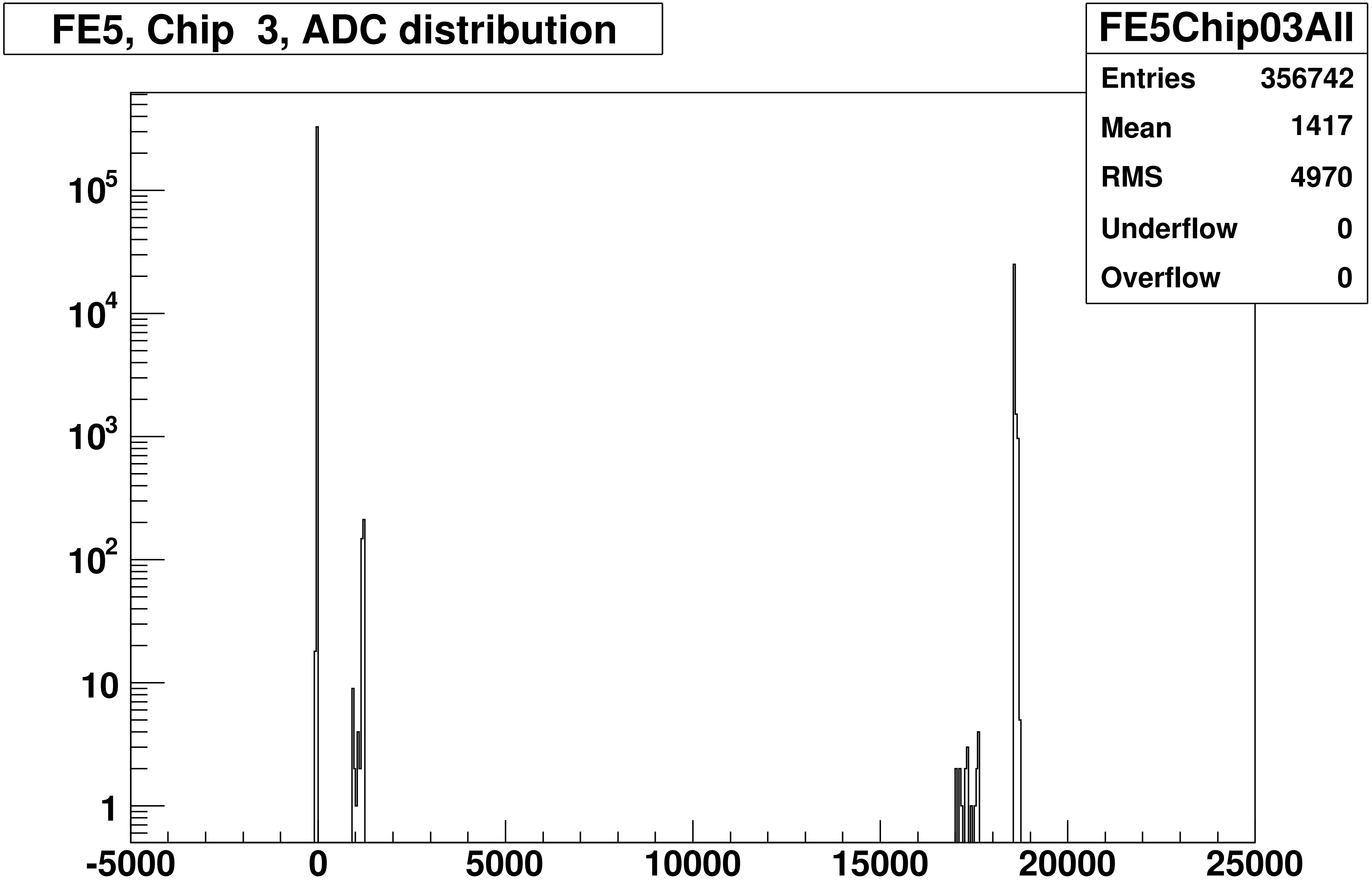
100
150
200



FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 356742
Mean 1.87e+04
RMS 18.53
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 356742
Mean 1417
RMS 4970
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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1
-5000
0
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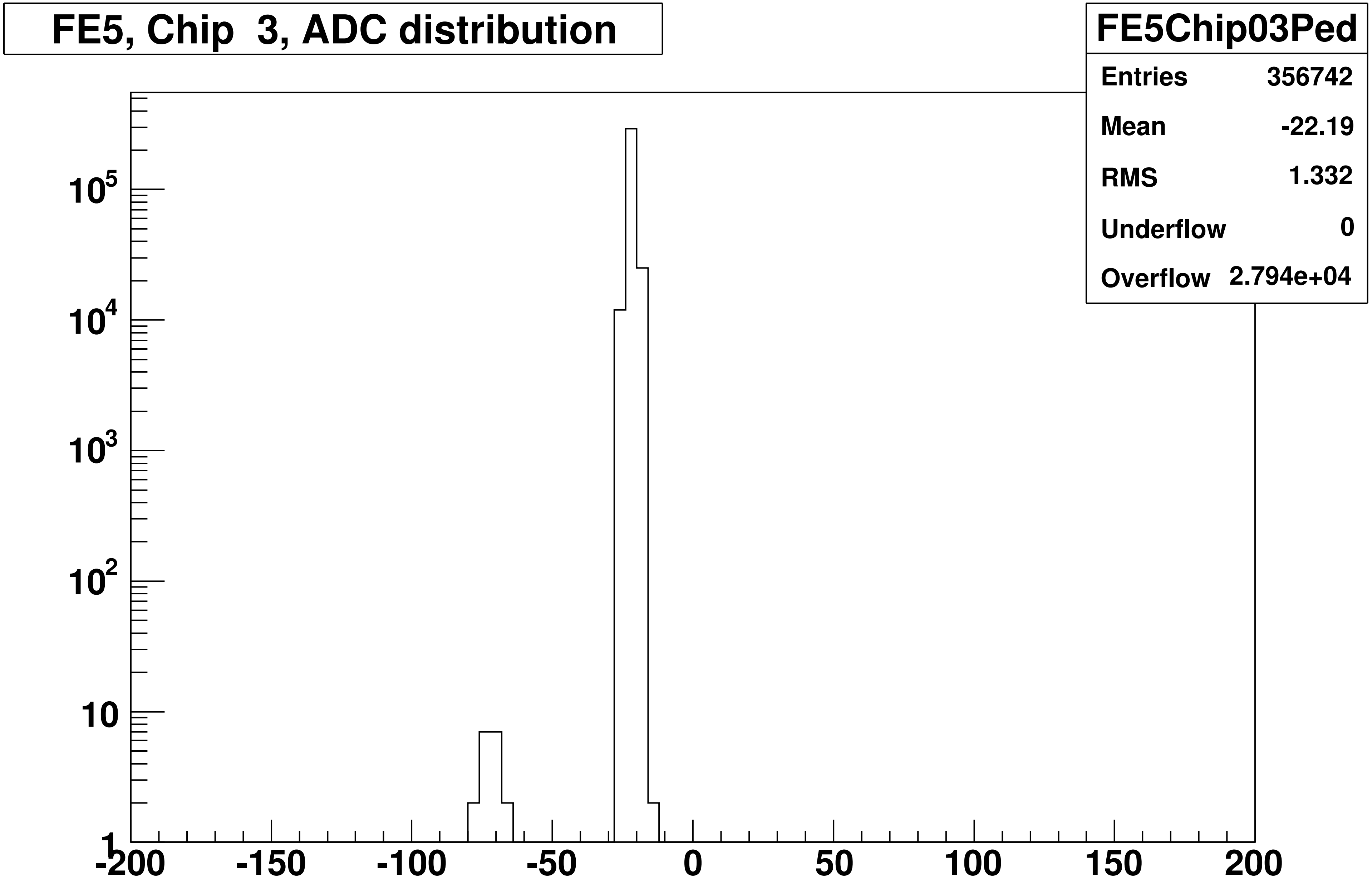
10000
15000
20000
25000


FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 356742
Mean -22.19
RMS 1.332
Underflow 0
Overflow 2.794e+04
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10^4
10^3
10^2
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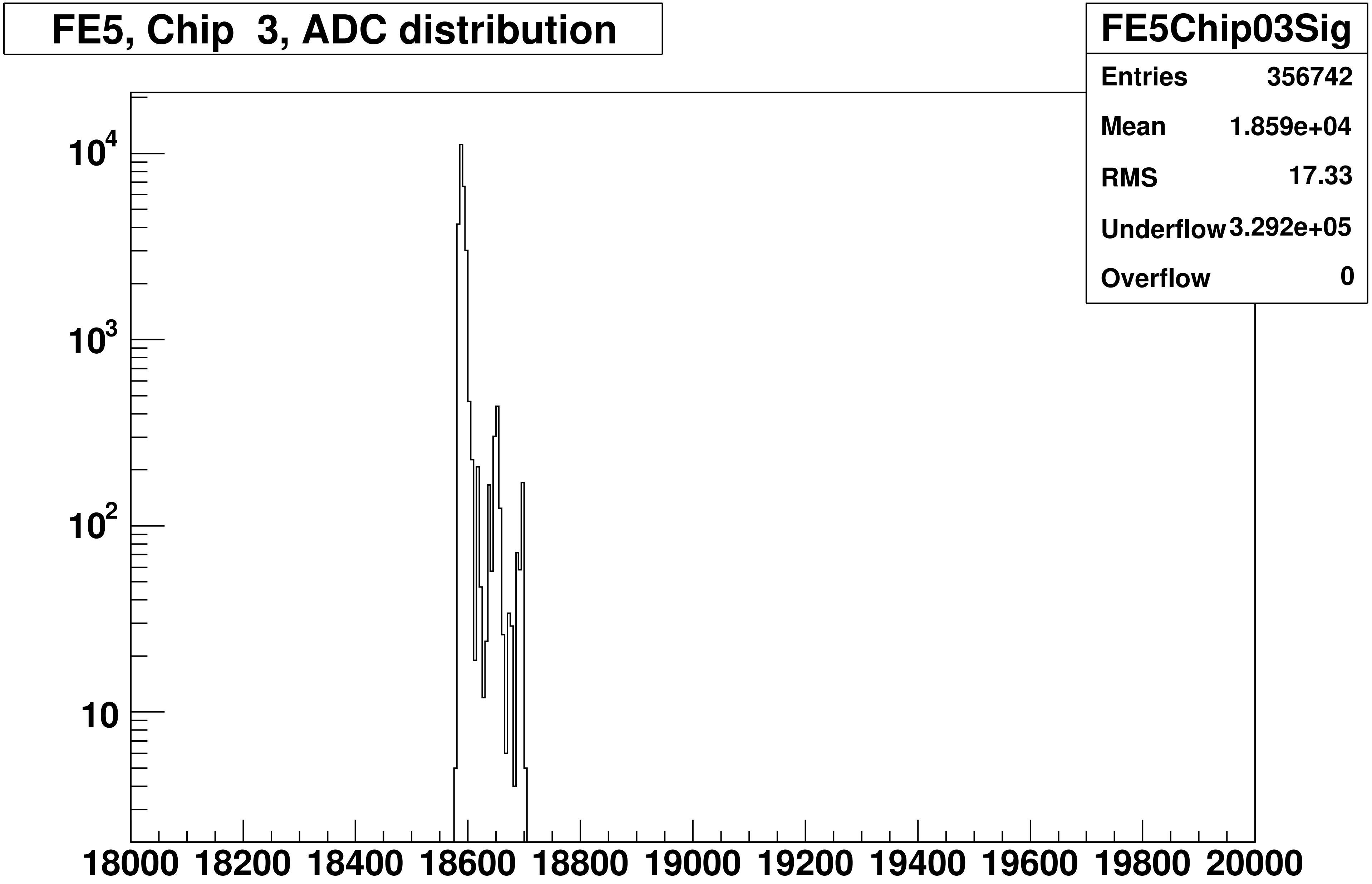
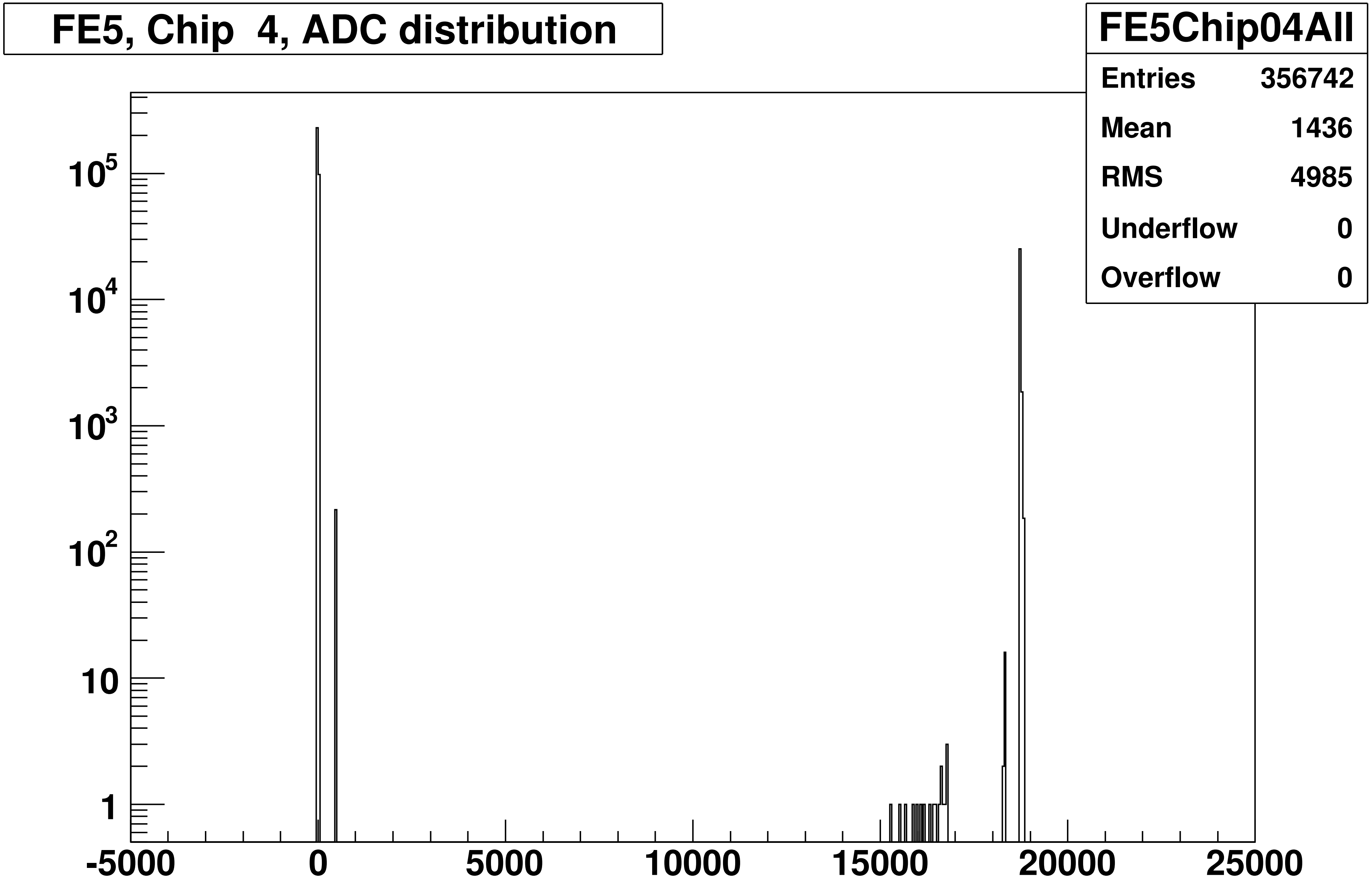
100
150
200



FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 356742
Mean 1.859e+04
RMS 17.33
Underflow 3.292e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 356742
Mean 1436
RMS 4985
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
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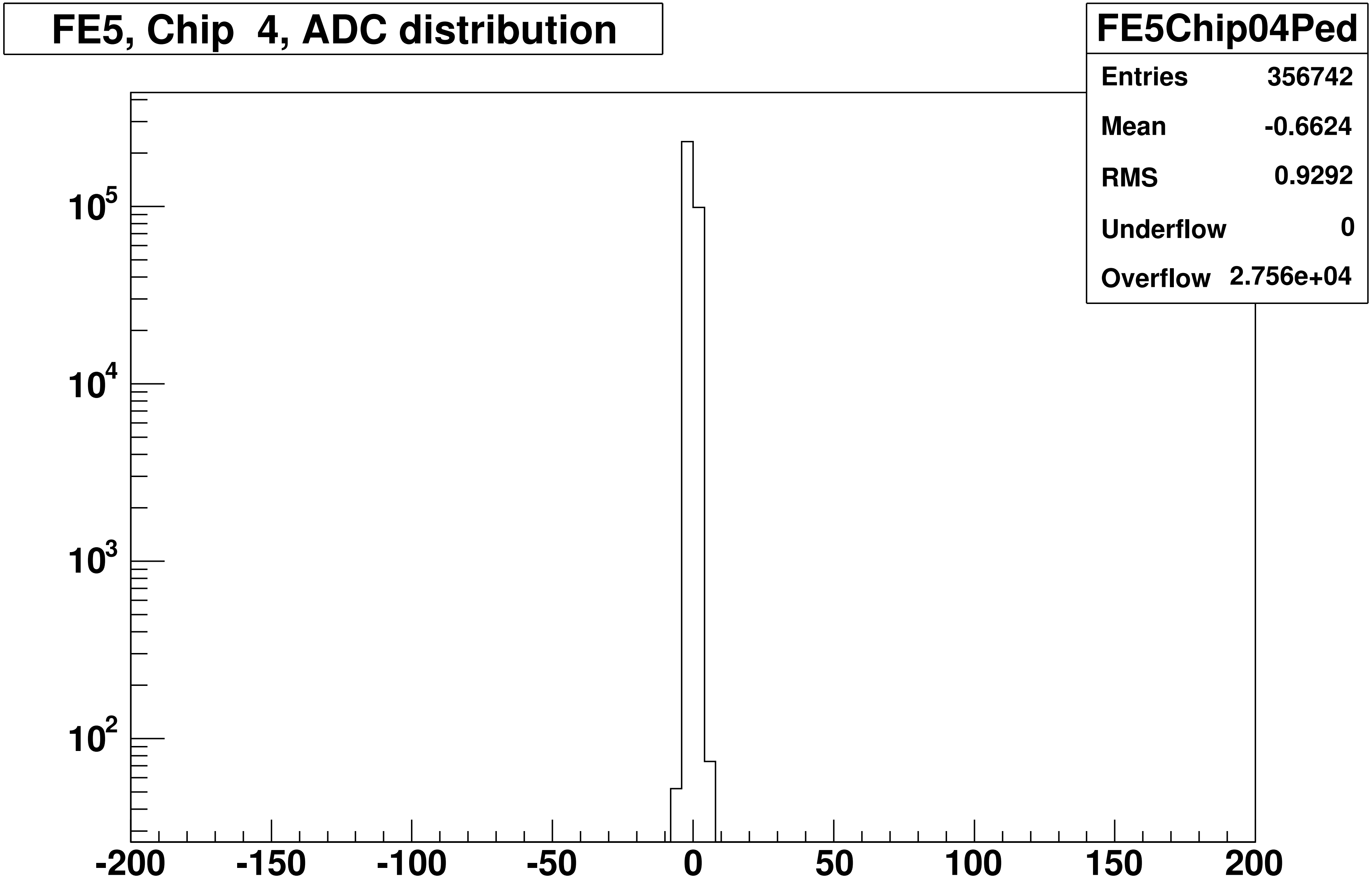
20000
25000


FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 356742
Mean -0.6624
RMS 0.9292
Underflow 0
Overflow 2.756e+04
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10^4
10^3
10^2
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-100
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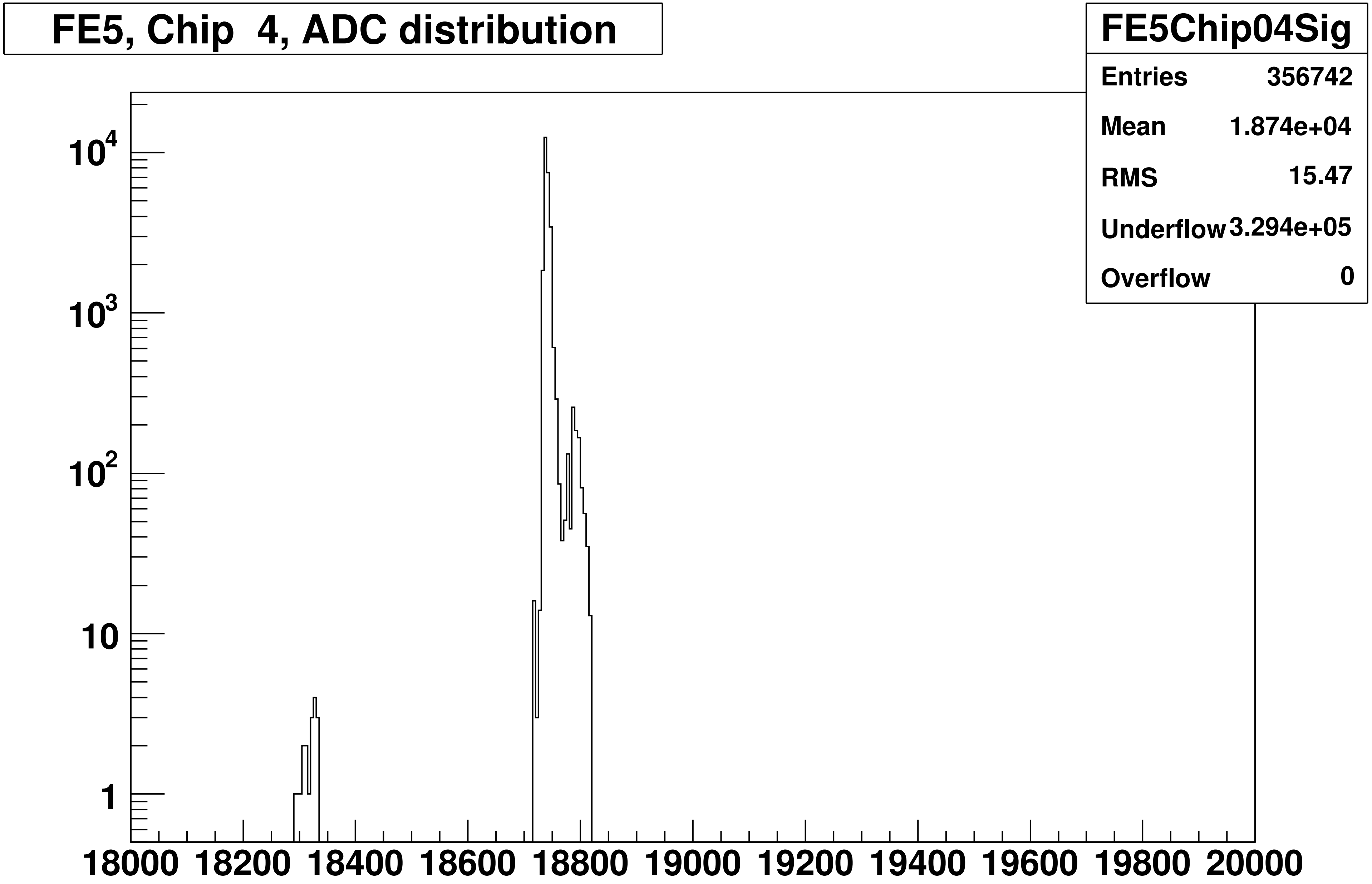
0
50
100
150
200


FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 356742
Mean 1.874e+04
RMS 15.47
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
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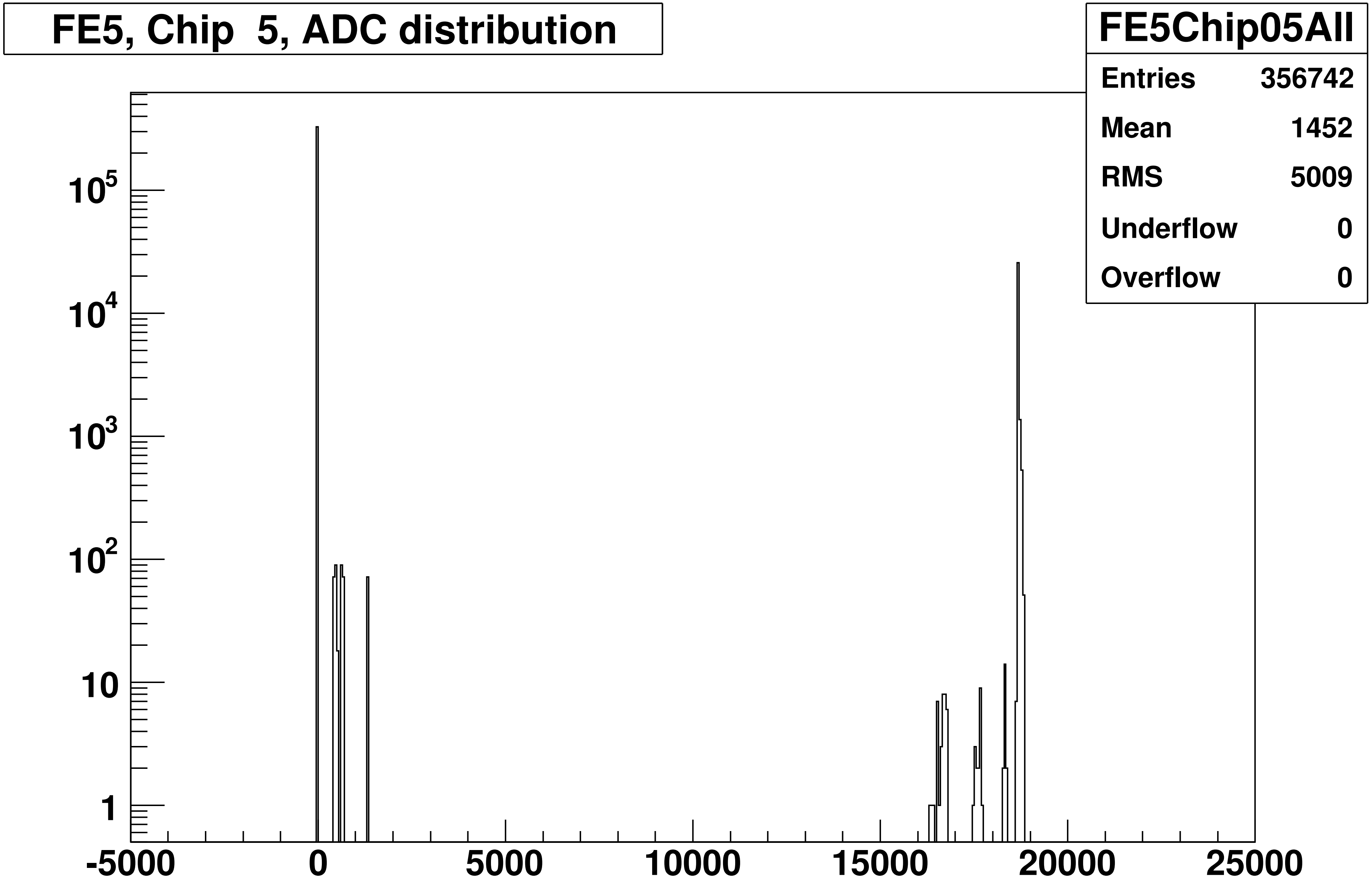
19800
20000



FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 356742
Mean 1452
RMS 5009
Underflow 0
Overflow 0
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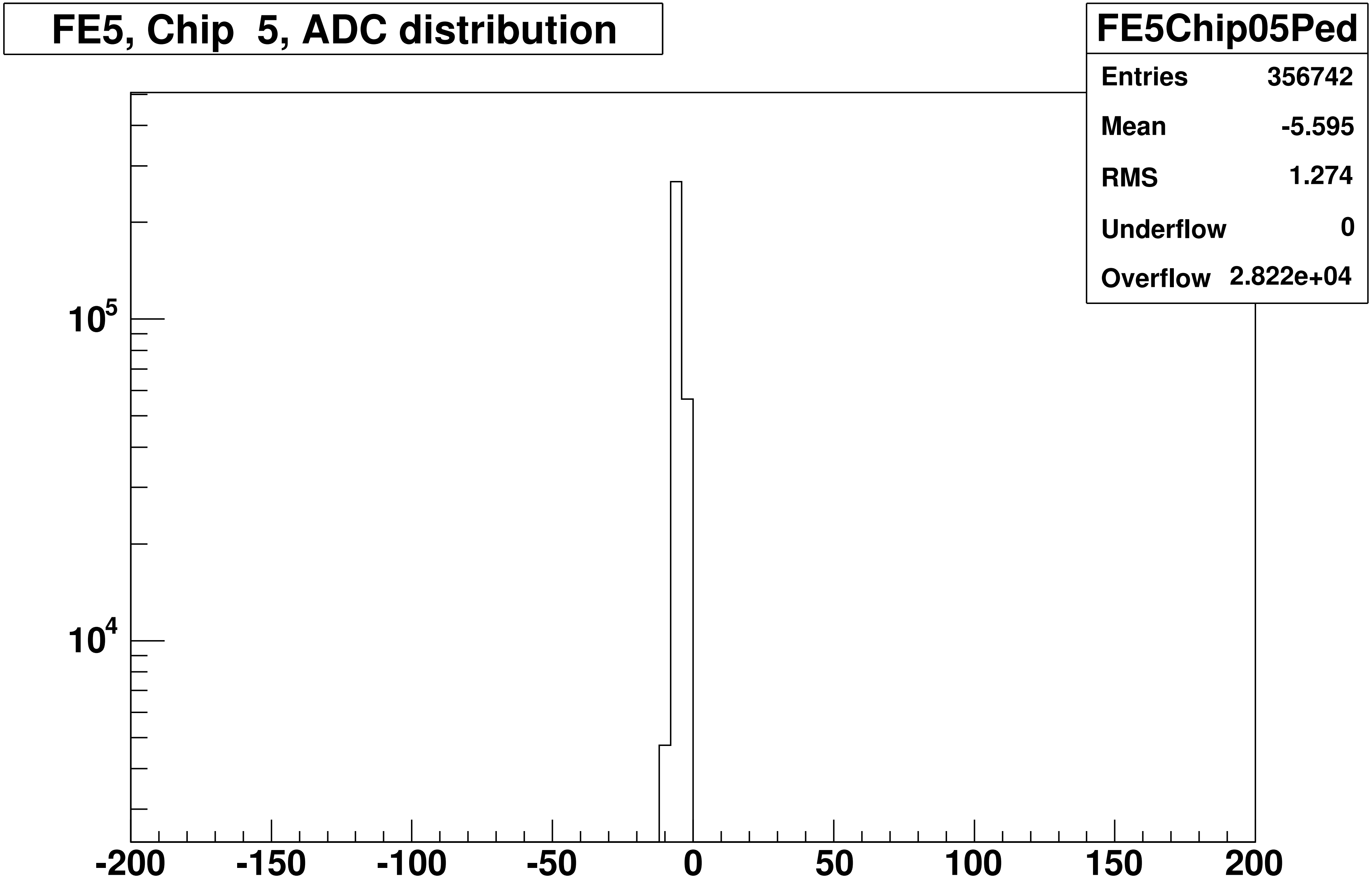
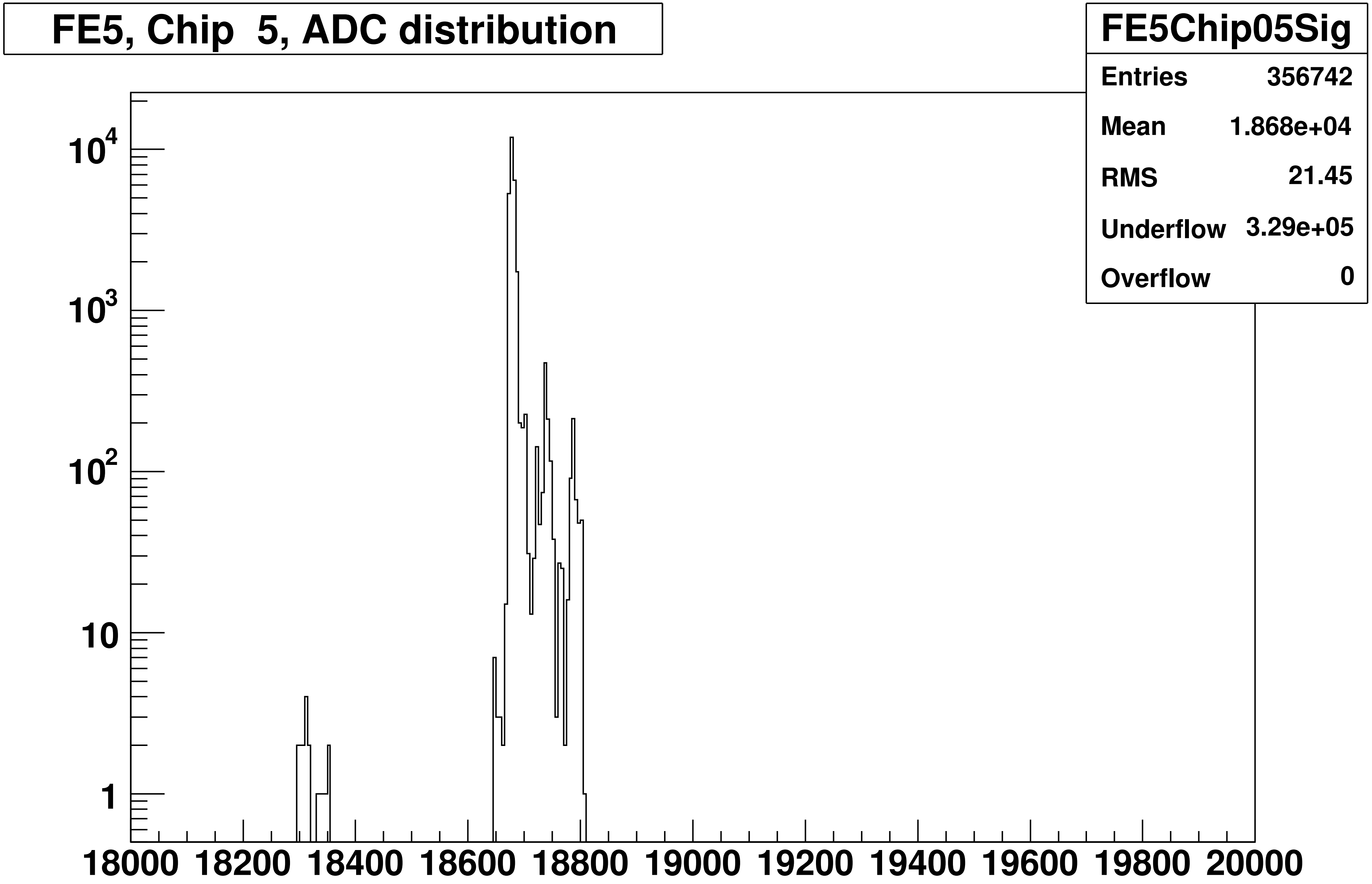
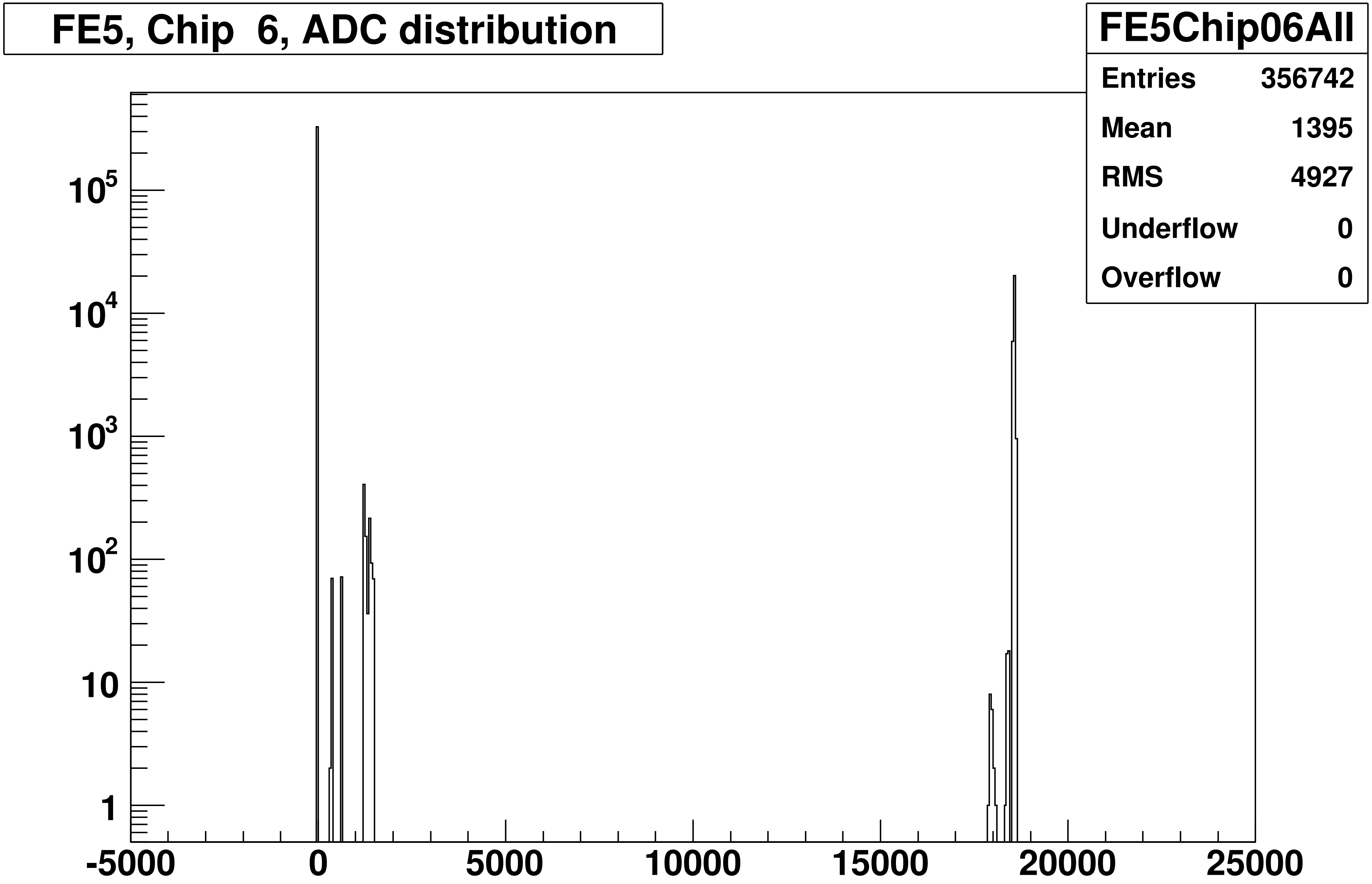
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 356742
Mean -5.595
RMS 1.274
Underflow 0
Overflow 2.822e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200



FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 356742
Mean 1.868e+04
RMS 21.45
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 356742
Mean 1395
RMS 4927
Underflow 0
Overflow 0
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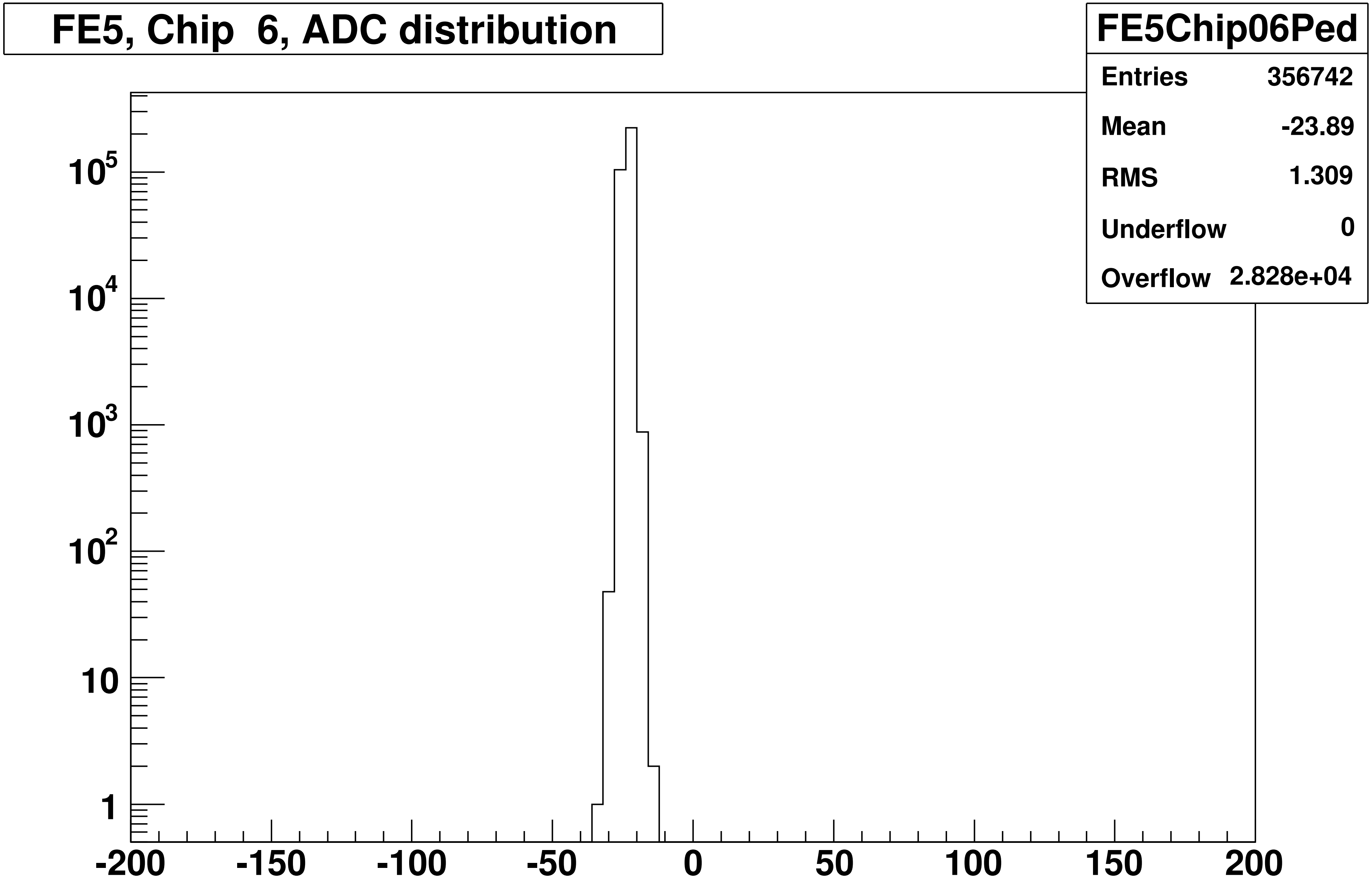
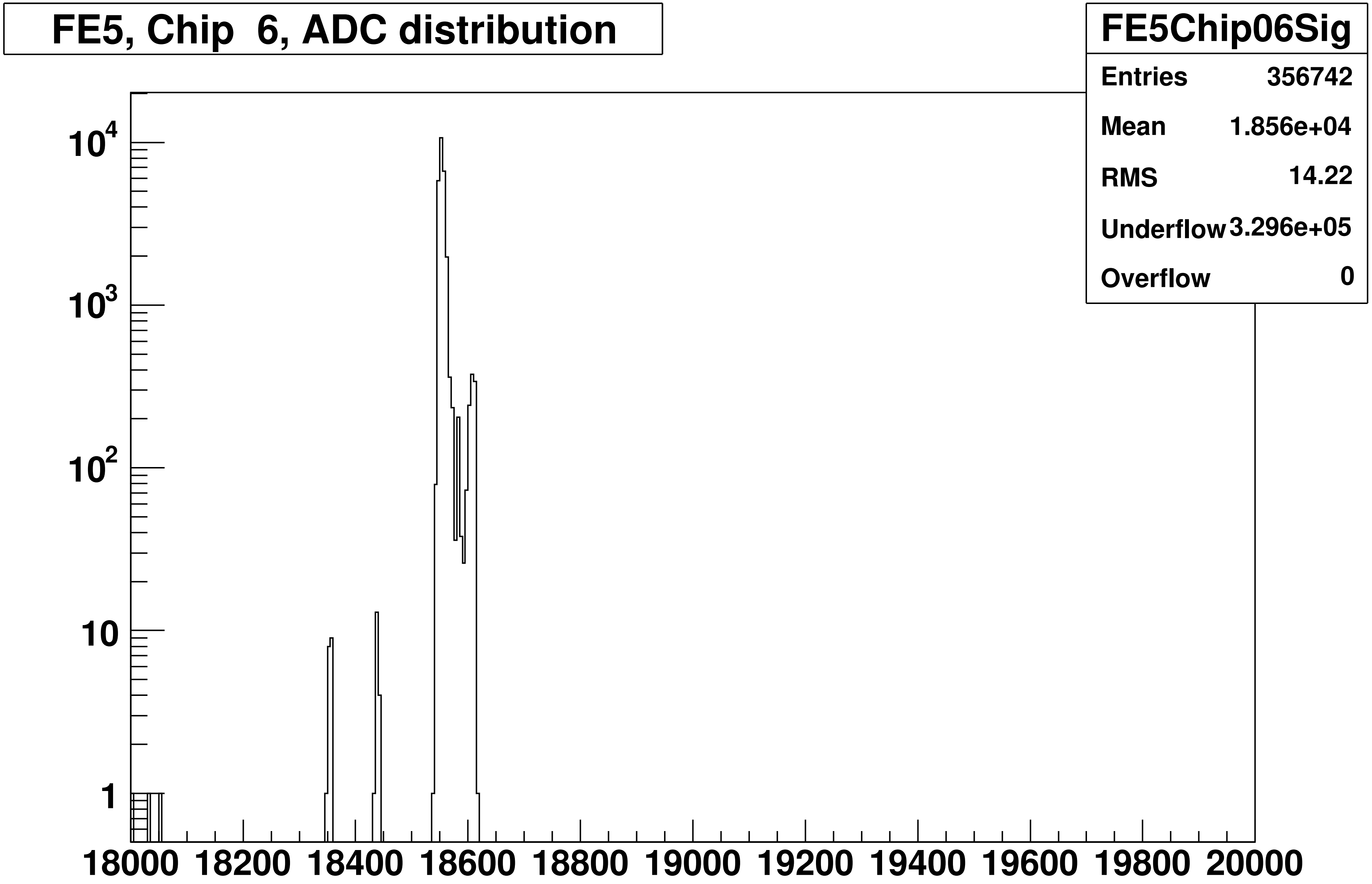
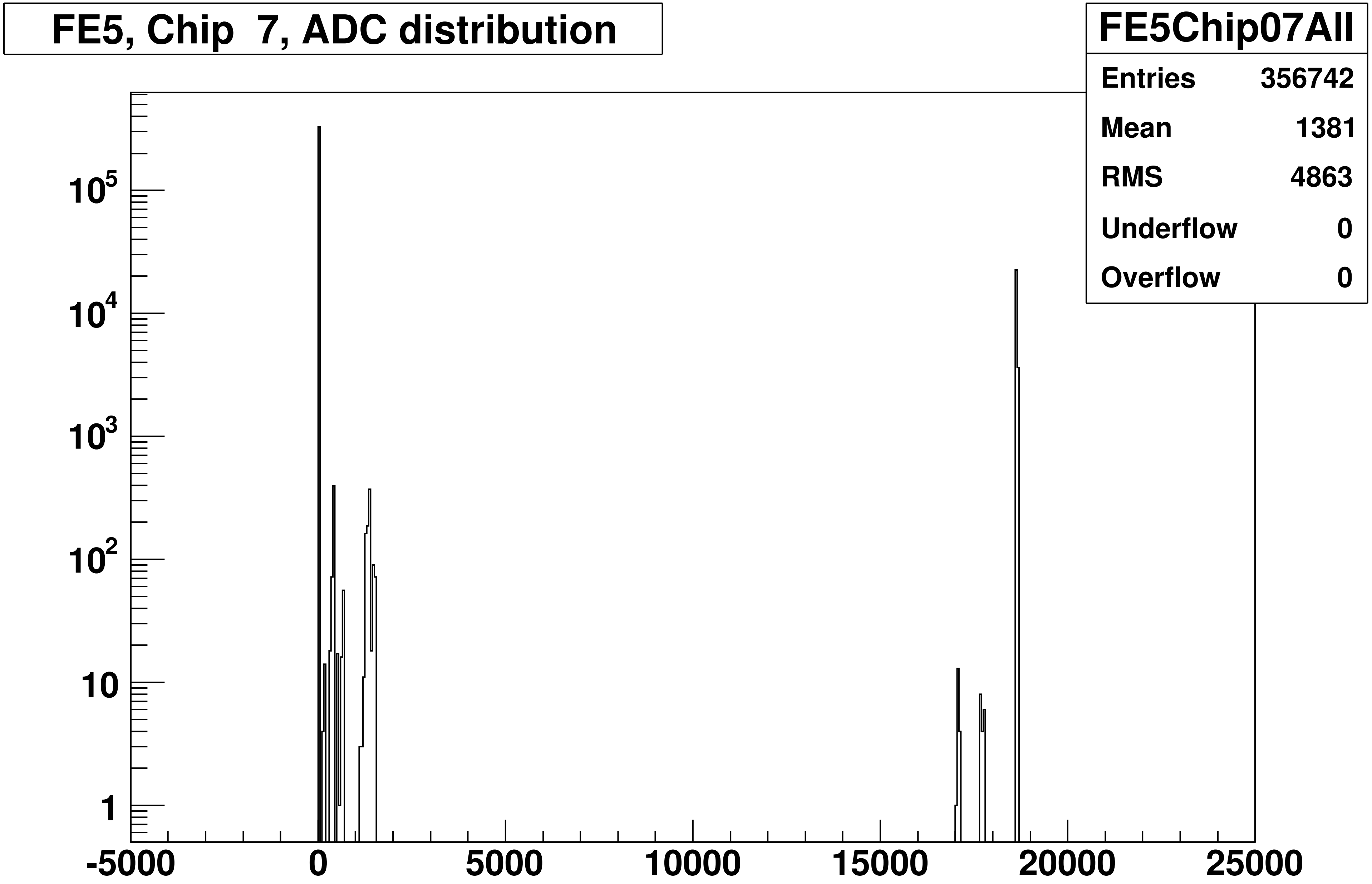
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 356742
Mean -23.89
RMS 1.309
Underflow 0
Overflow 2.828e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 356742
Mean 1.856e+04
RMS 14.22
Underflow 3.296e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 356742
Mean 1381
RMS 4863
Underflow 0
Overflow 0
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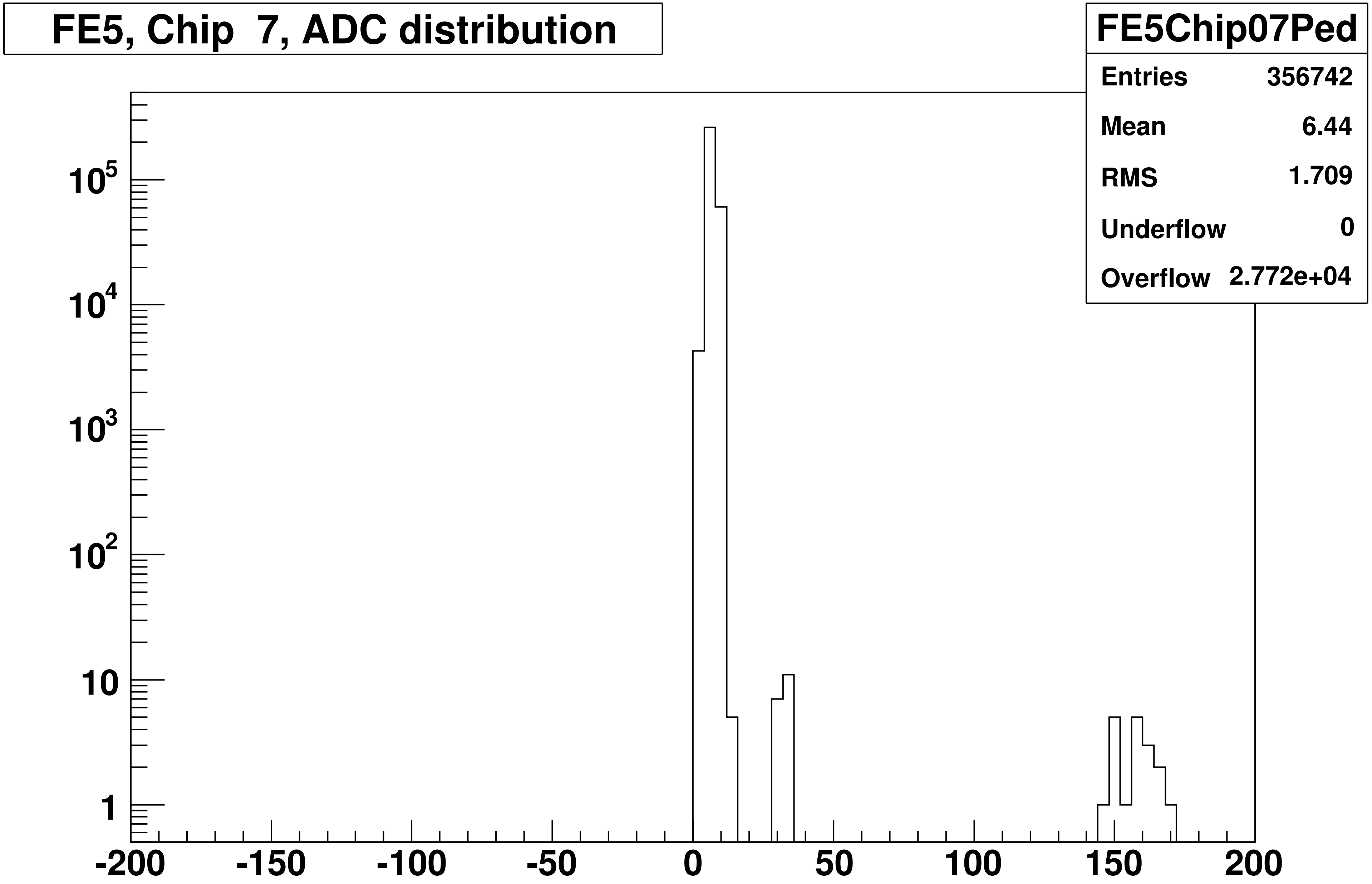
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 356742
Mean 6.44
RMS 1.709
Underflow 0
Overflow 2.772e+04
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10^4
10^3
10^2
10
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-200
-150
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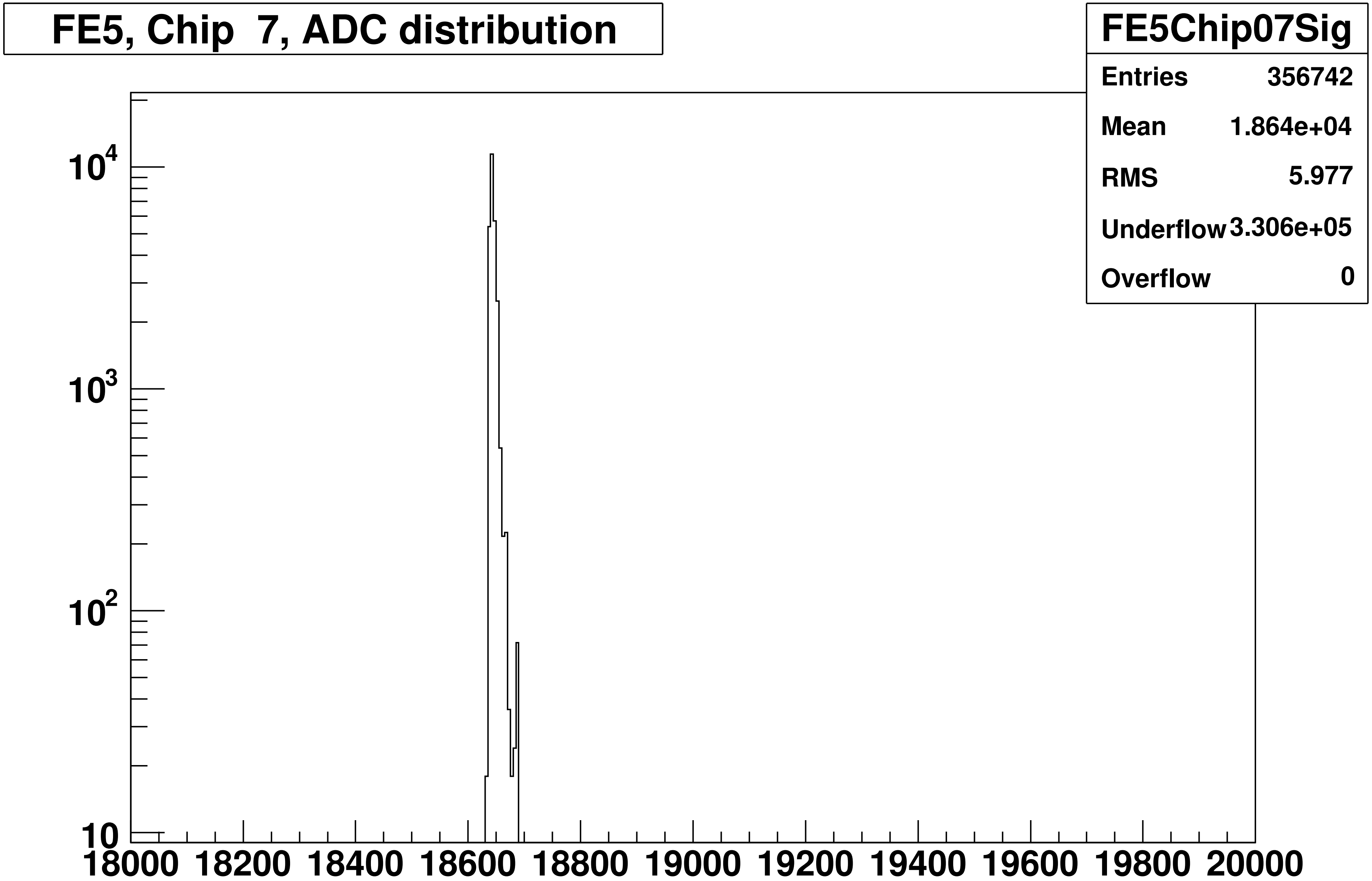
100
150
200



FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 356742
Mean 1.864e+04
RMS 5.977
Underflow 3.306e+05
Overflow 0
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10^3
10^2
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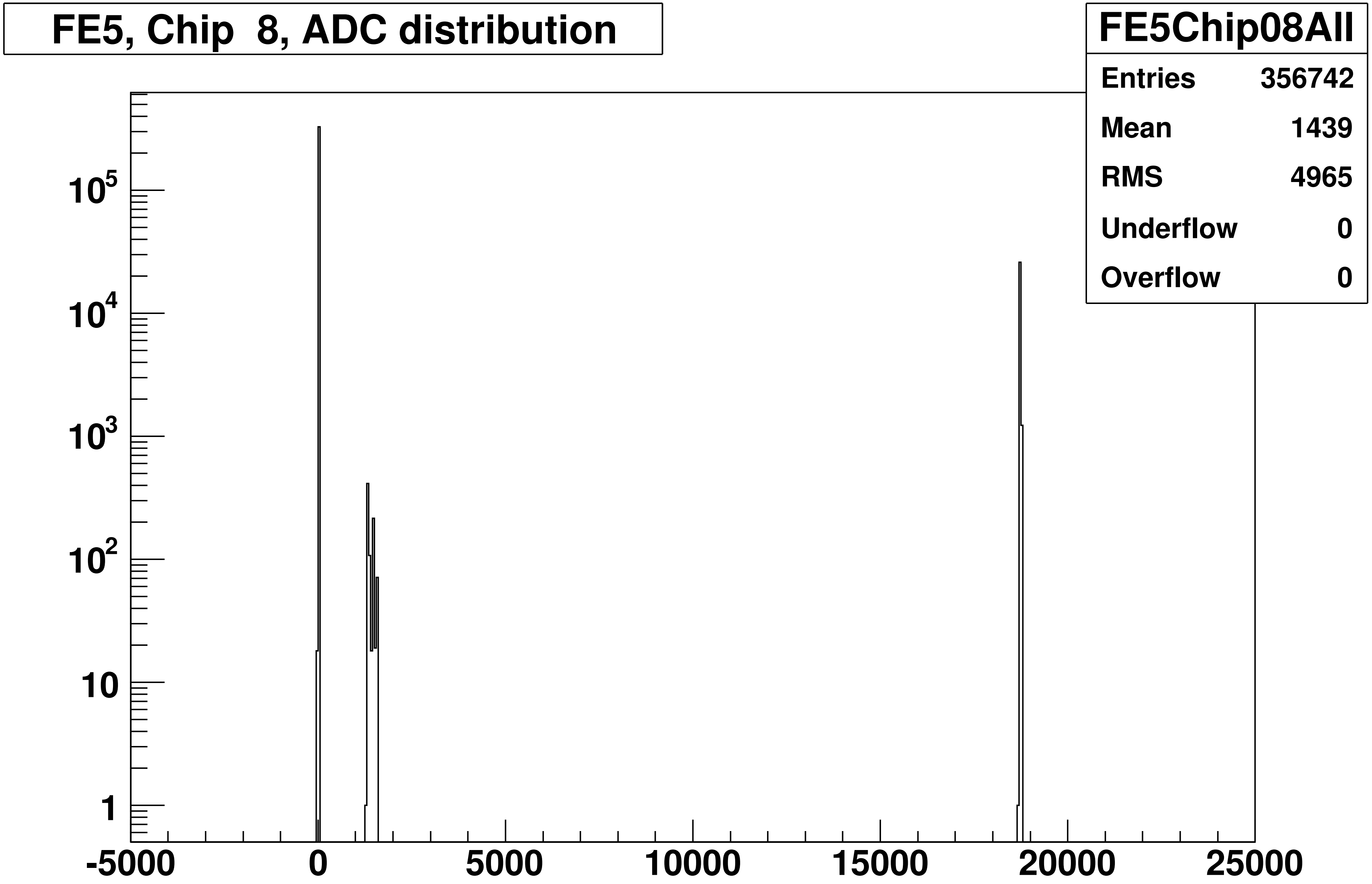
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 356742
Mean 1439
RMS 4965
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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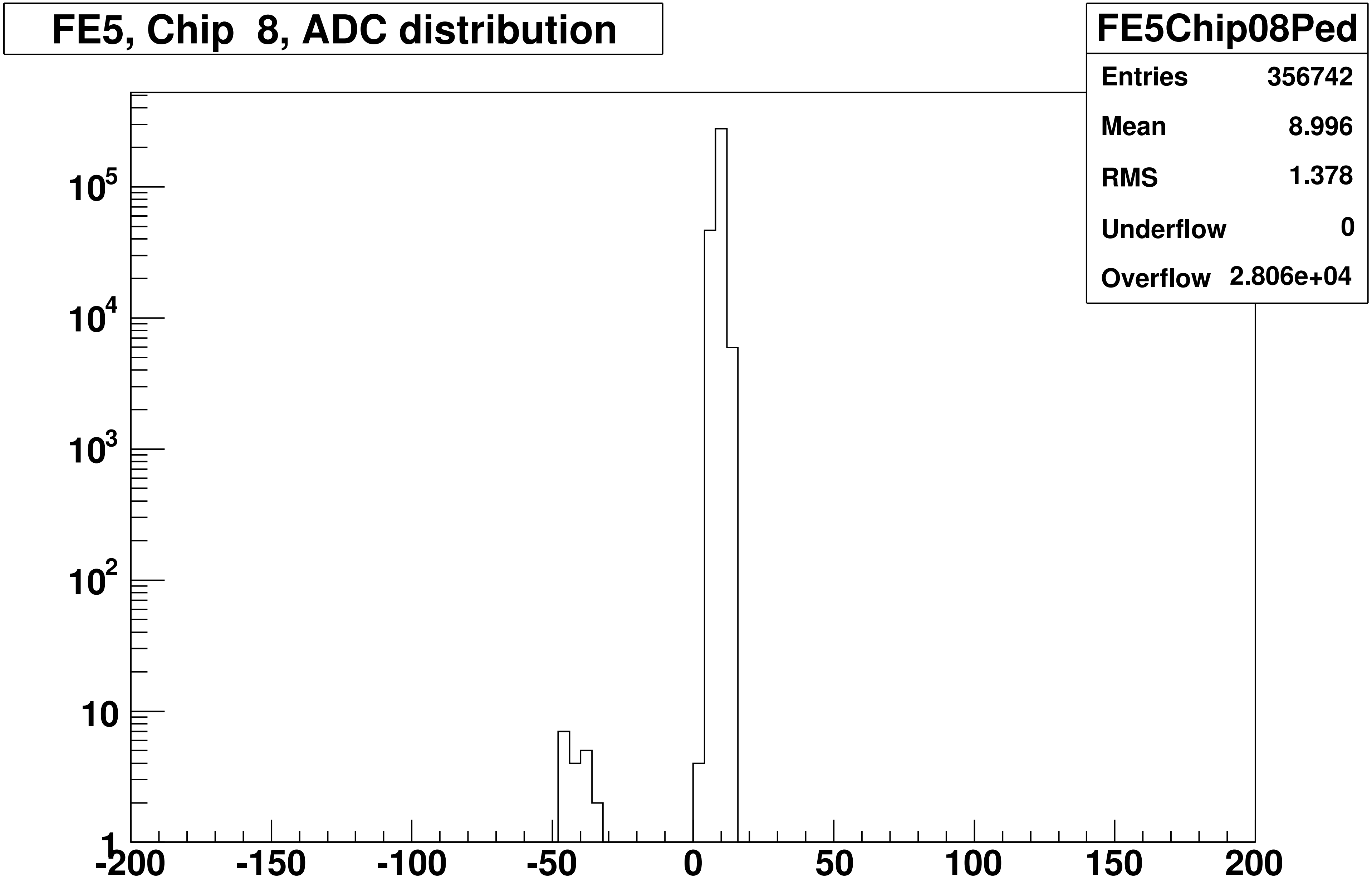
10000
15000
20000
25000



FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 356742
Mean 8.996
RMS 1.378
Underflow 0
Overflow 2.806e+04
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10^3
10^2
10
1
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-150
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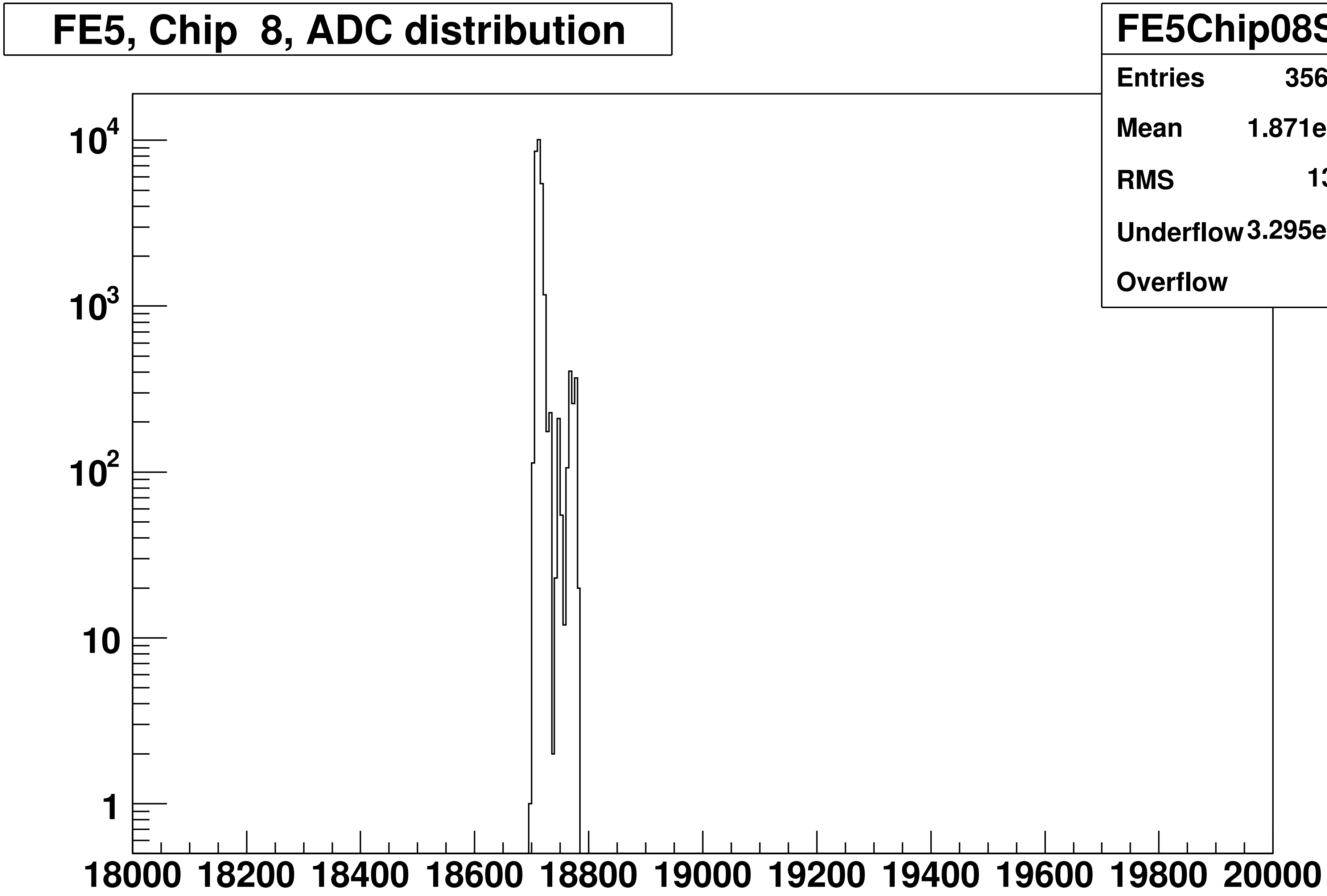
0
50
100
150
200



FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 356742
Mean 1.871e+04
RMS 13.26
Underflow 3.295e+05
Overflow 0
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10^3
10^2
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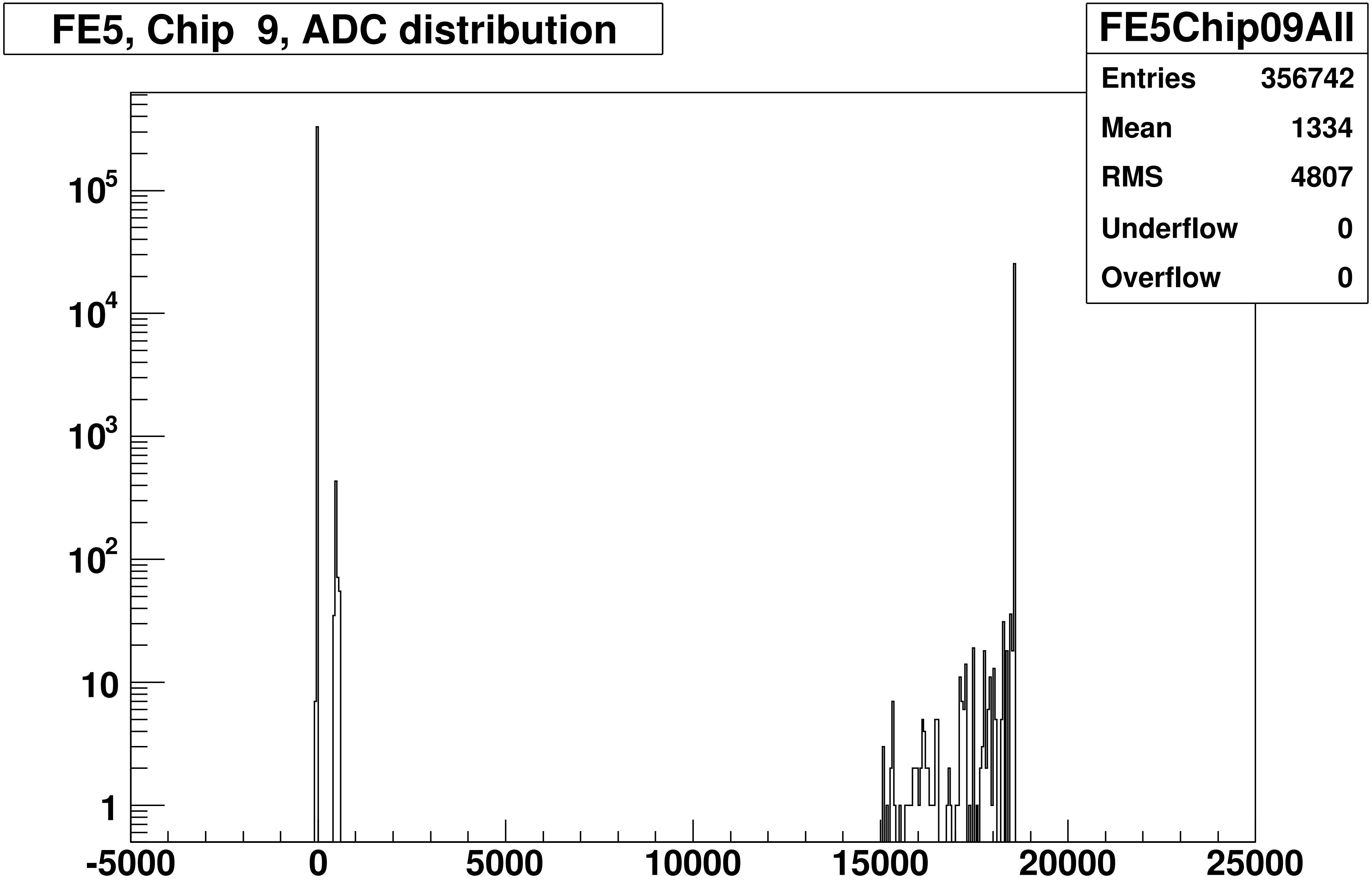
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 356742
Mean 1334
RMS 4807
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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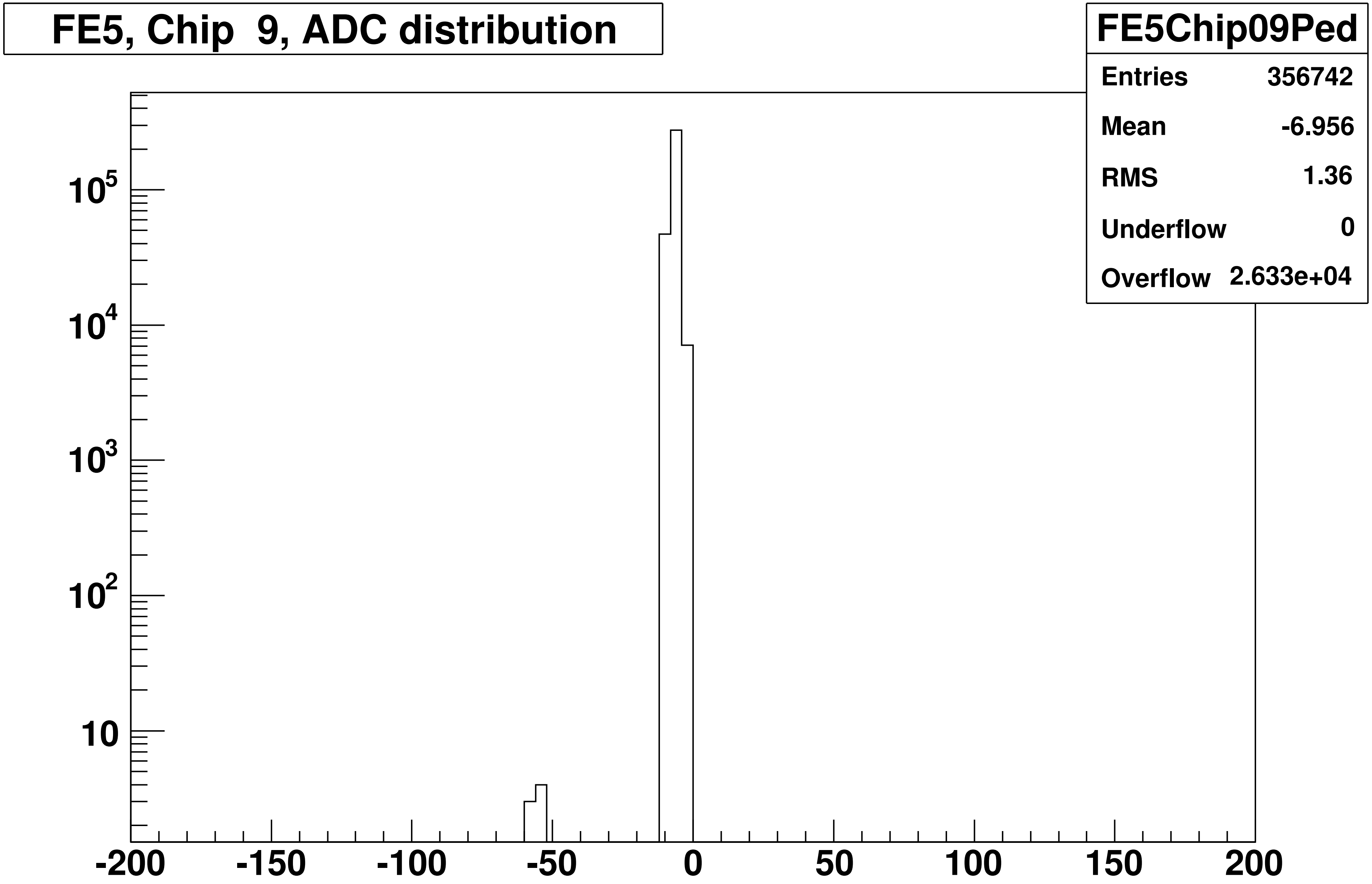
10000
15000
20000
25000


FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 356742
Mean -6.956
RMS 1.36
Underflow 0
Overflow 2.633e+04
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10^4
10^3
10^2
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-100
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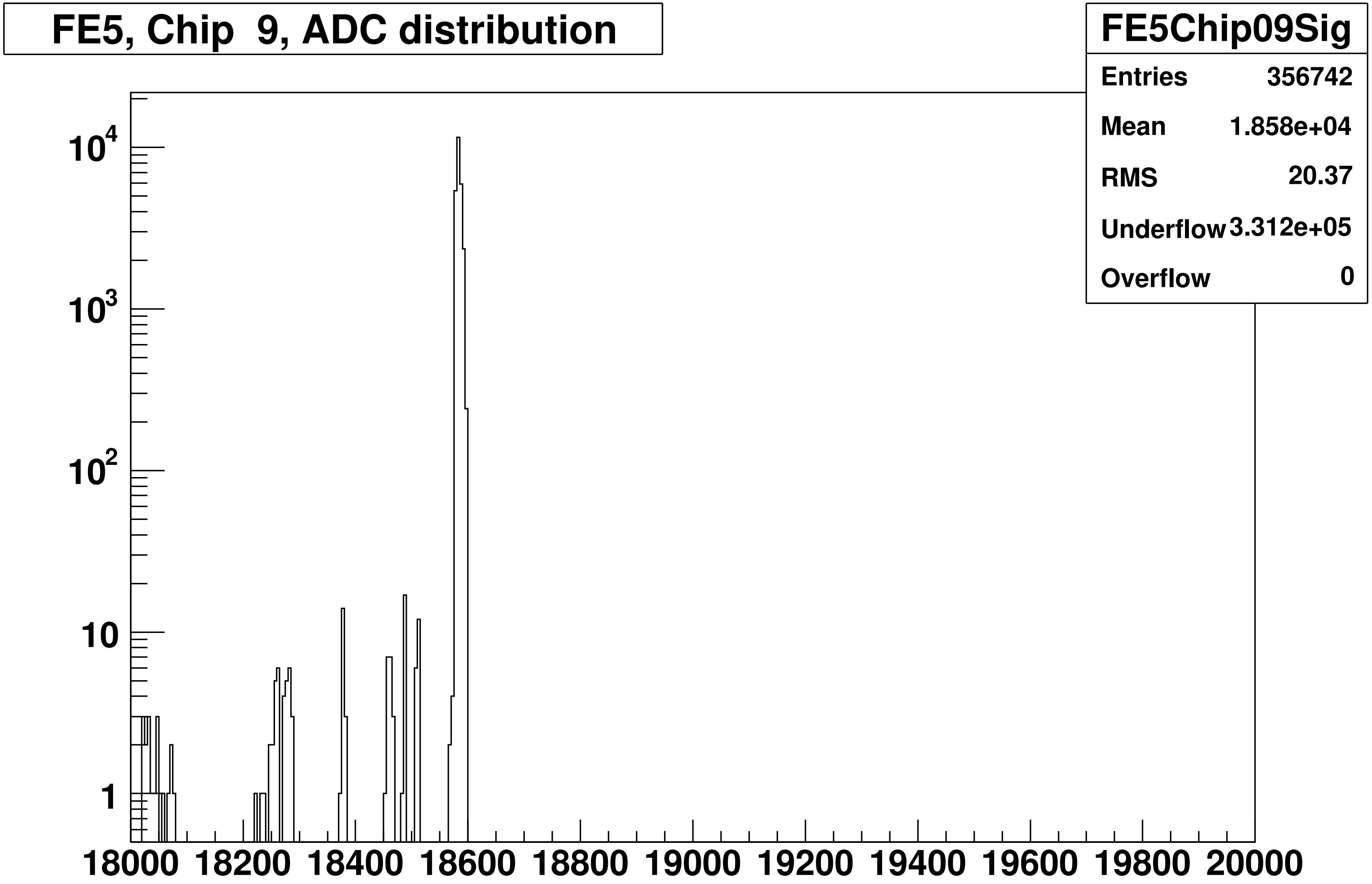
150
200



FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 356742
Mean 1.858e+04
RMS 20.37
Underflow 3.312e+05
Overflow 0
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10^3
10^2
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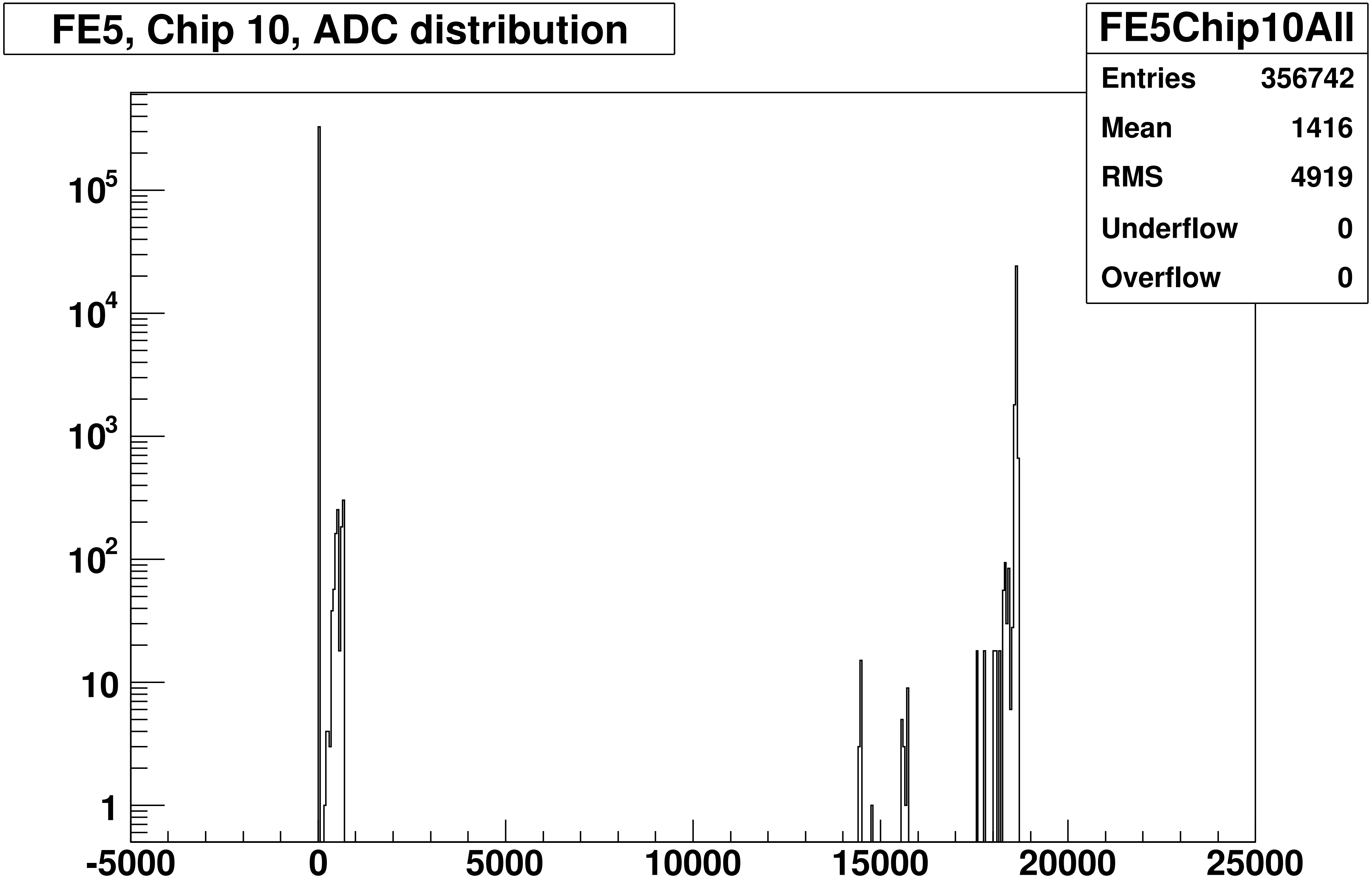
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 356742
Mean 1416
RMS 4919
Underflow 0
Overflow 0
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10^3
10^2
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20000
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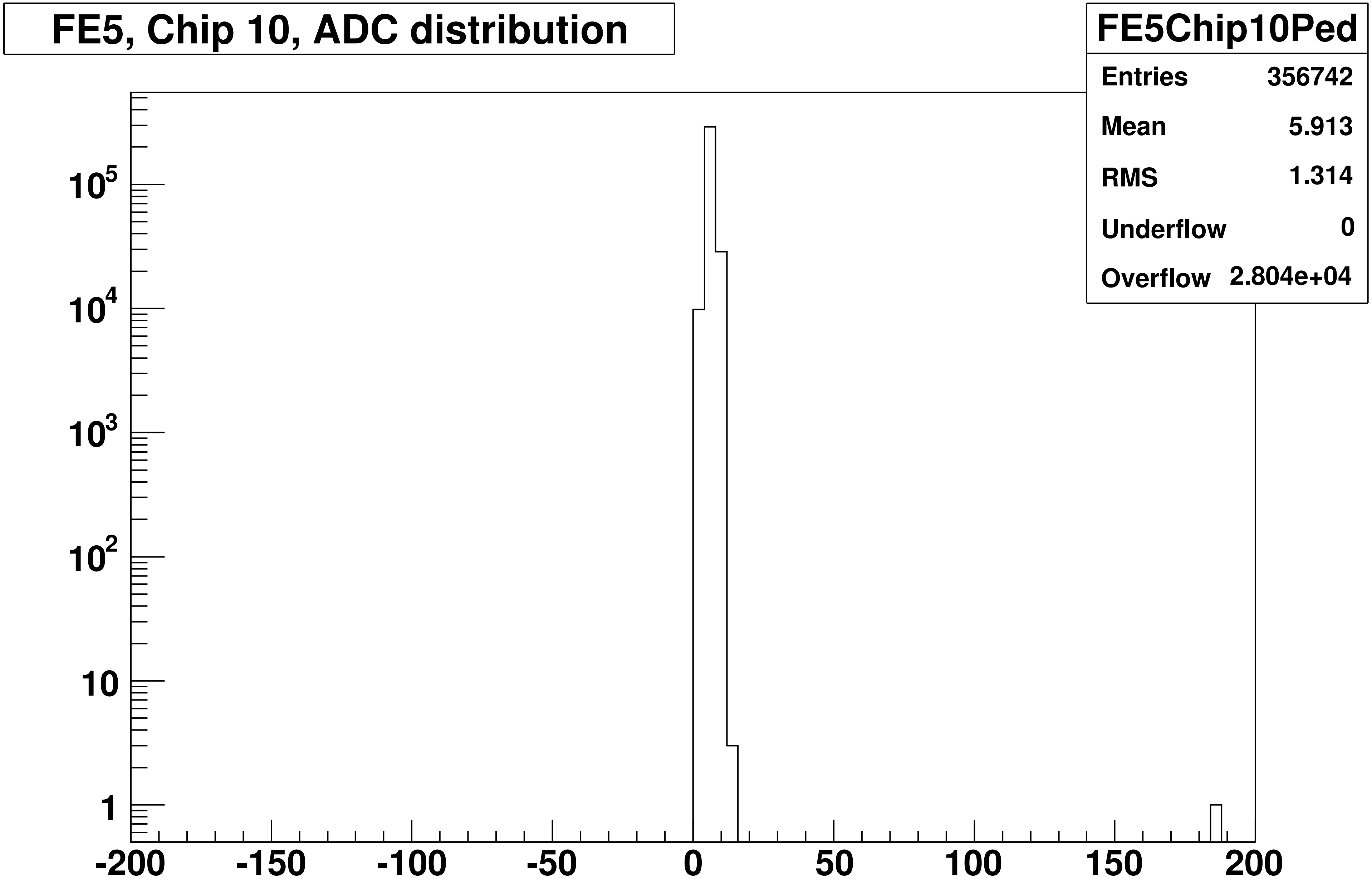

FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 356742
Mean 5.913
RMS 1.314
Underflow 0
Overflow 2.804e+04
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0
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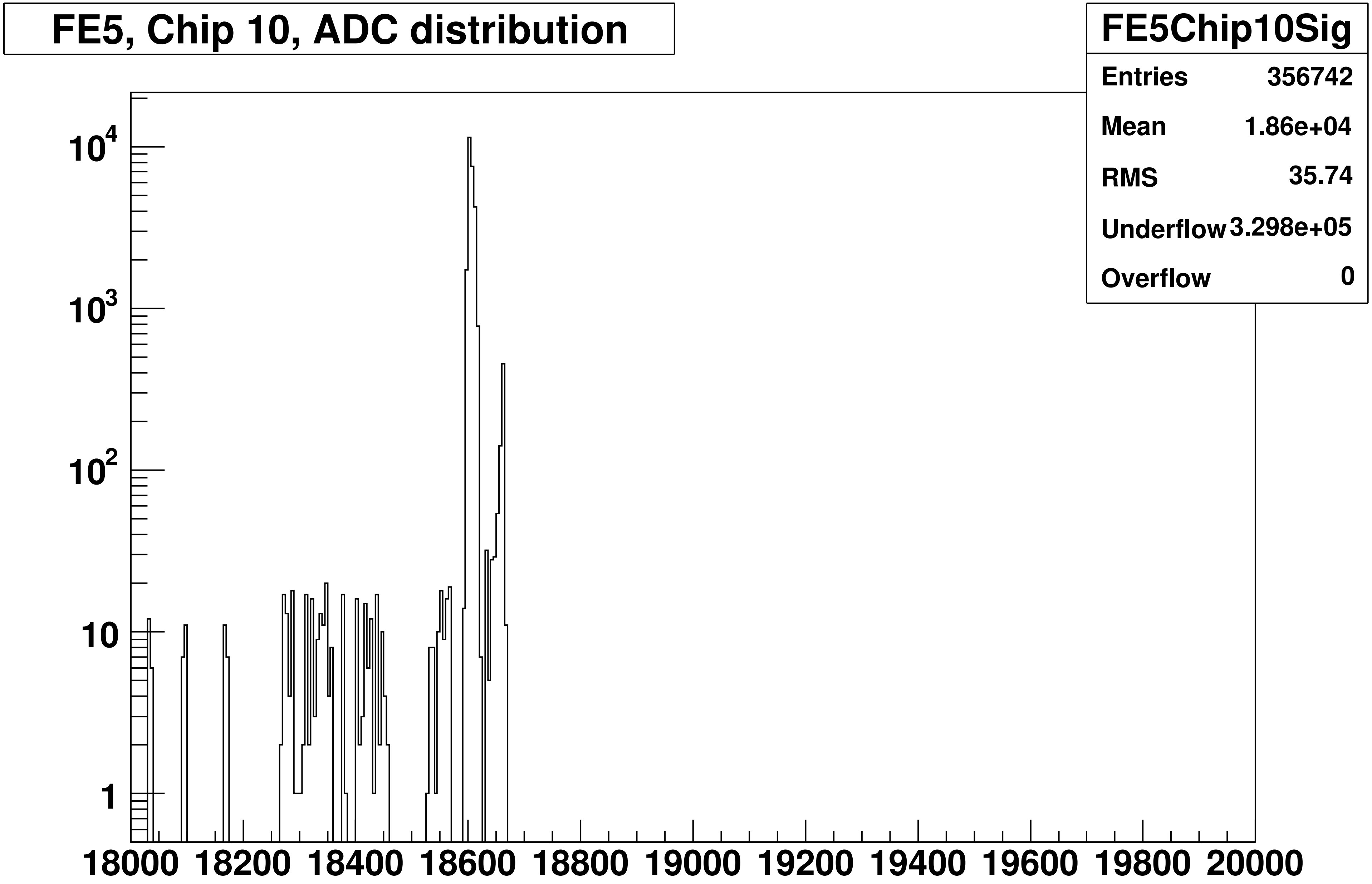
100
150
200



FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 356742
Mean 1.86e+04
RMS 35.74
Underflow 3.298e+05
Overflow 0
10^4
10^3
10^2
10
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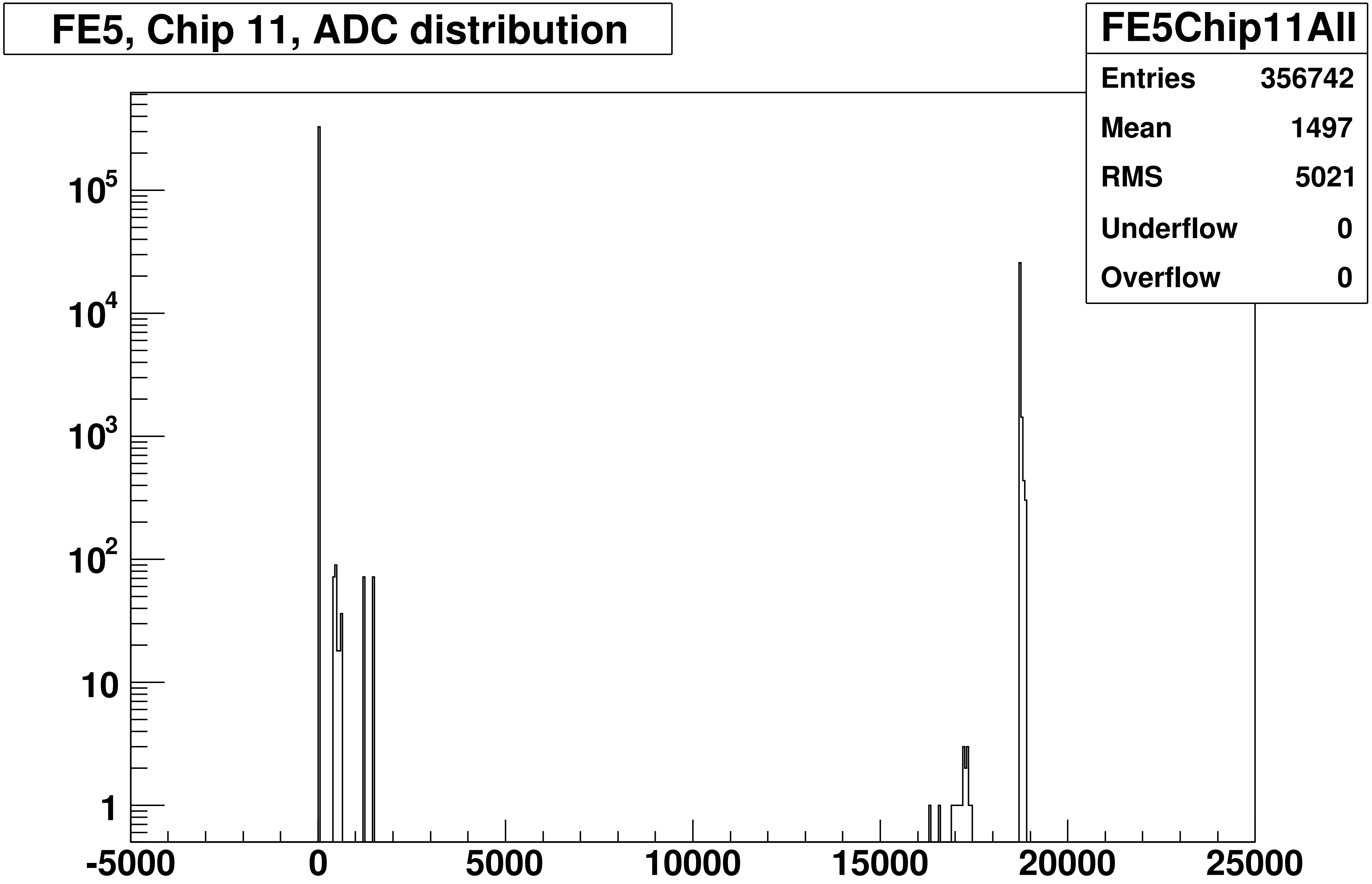
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 356742
Mean 1497
RMS 5021
Underflow 0
Overflow 0
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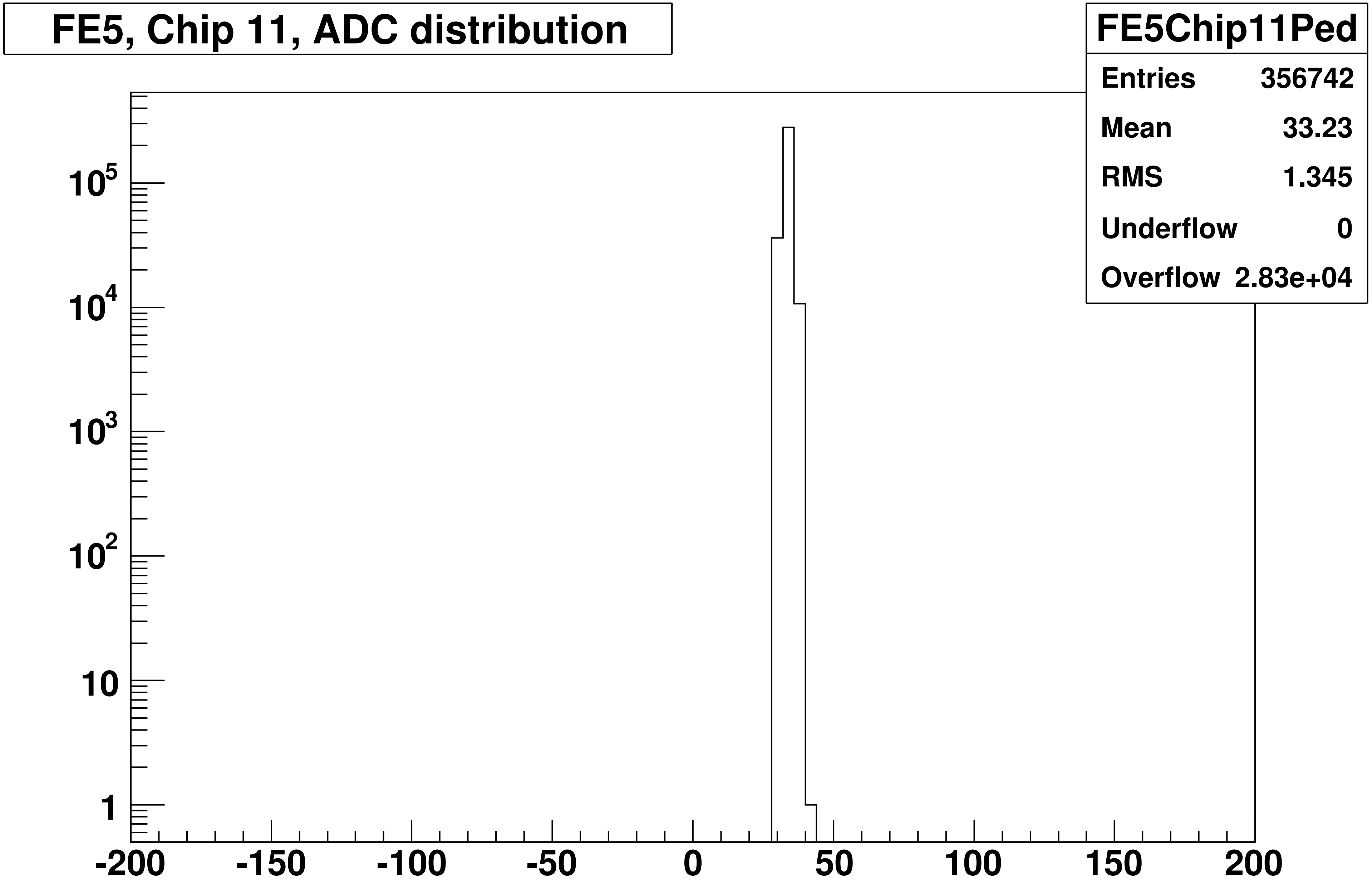
FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 356742
Mean 33.23
RMS 1.345
Underflow 0
Overflow 2.83e+04
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10^3
10^2
10
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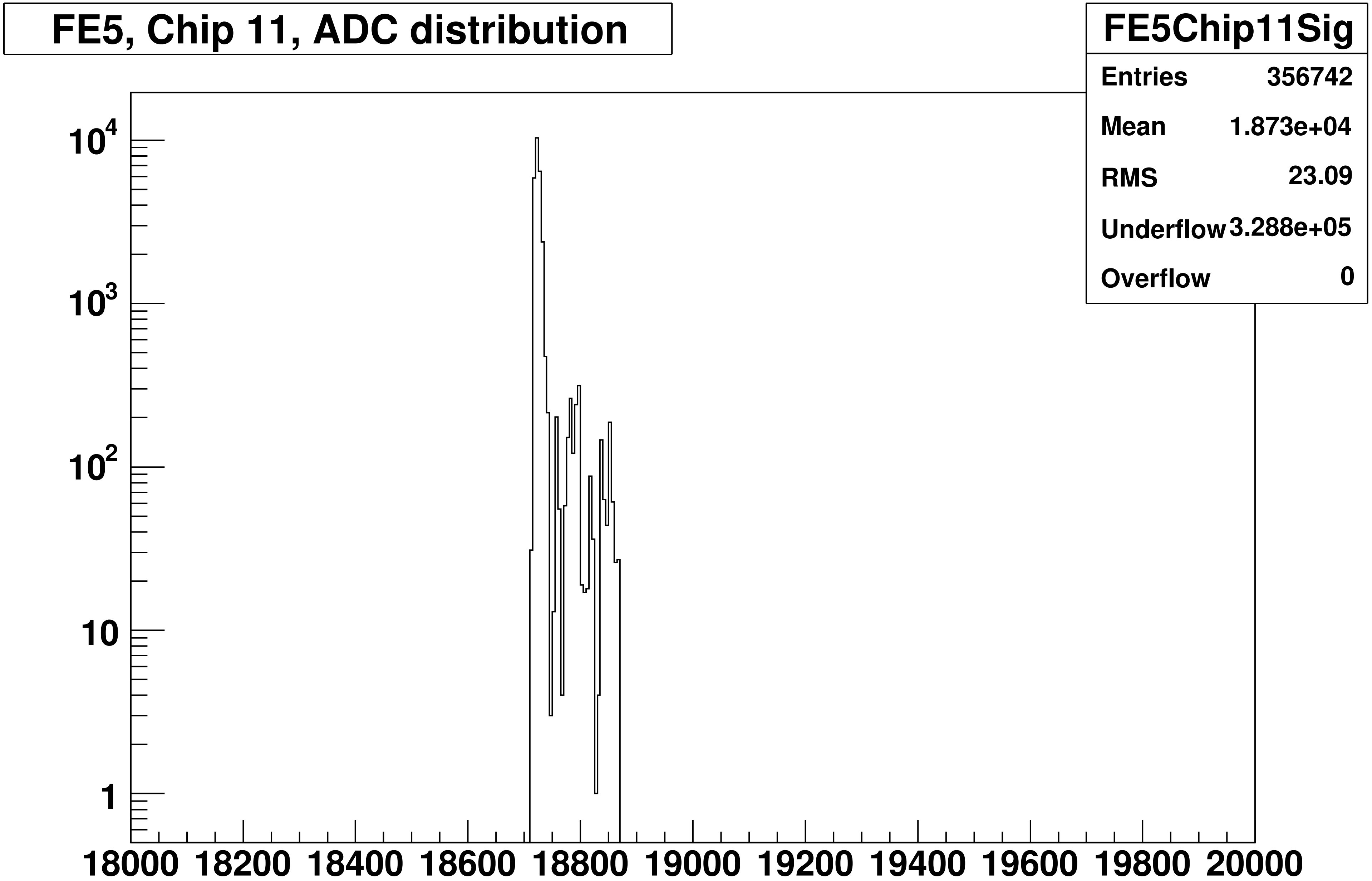
100
150
200


FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 356742
Mean 1.873e+04
RMS 23.09
Underflow 3.288e+05
Overflow 0
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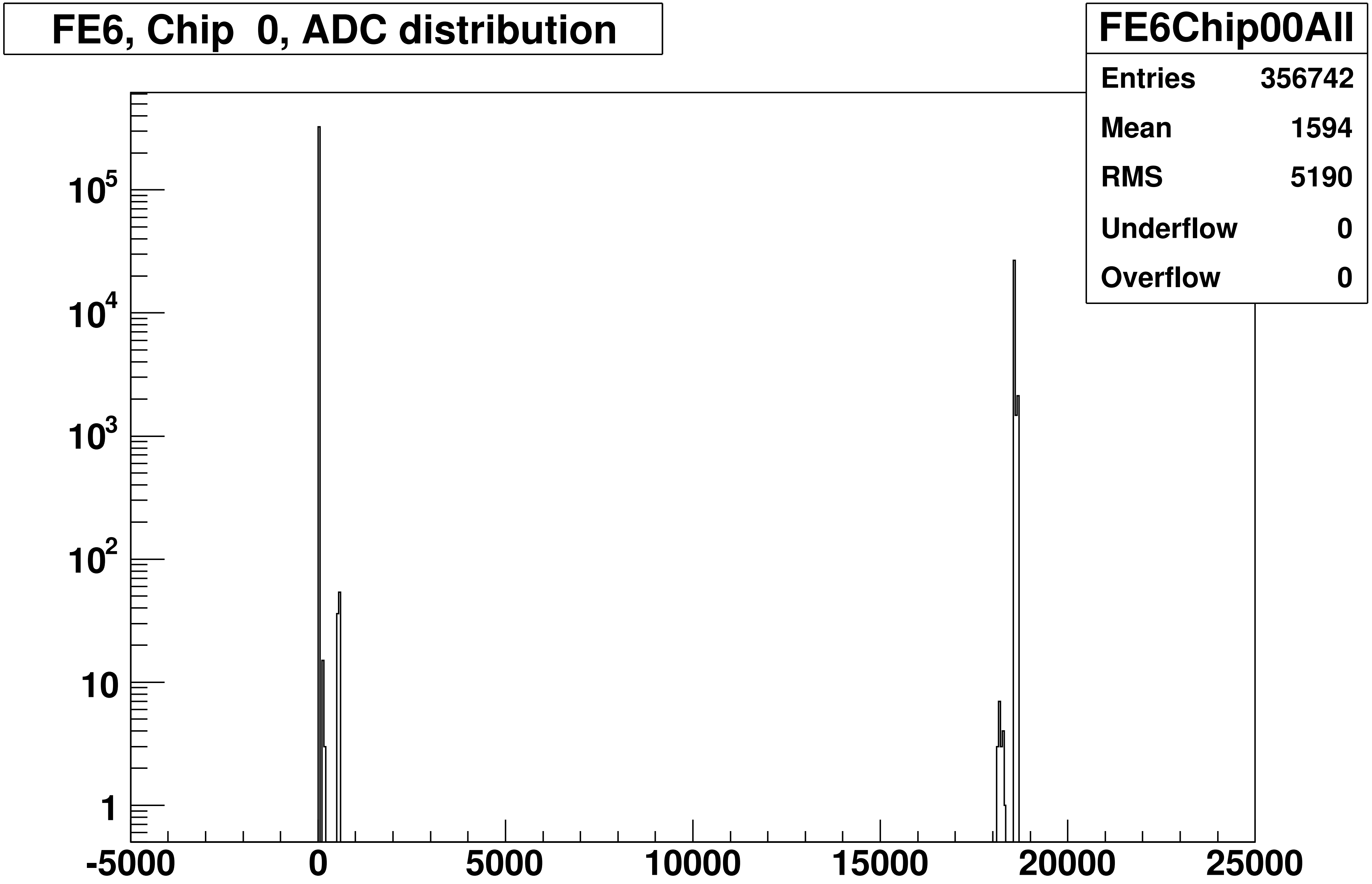
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 356742
Mean 1594
RMS 5190
Underflow 0
Overflow 0
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10^3
10^2
10
1
-5000
0
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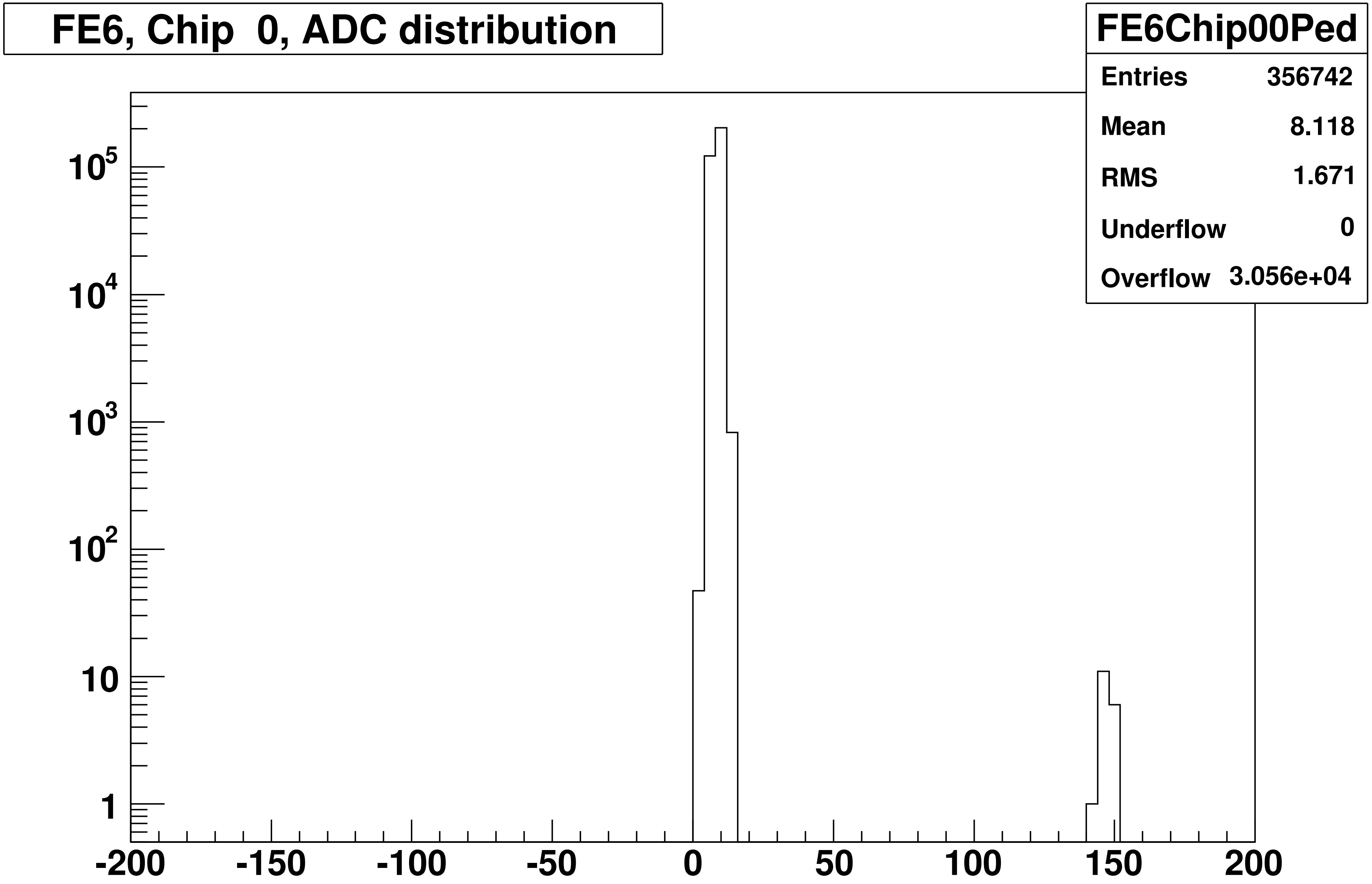
10000
15000
20000
25000


FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 356742
Mean 8.118
RMS 1.671
Underflow 0
Overflow 3.056e+04
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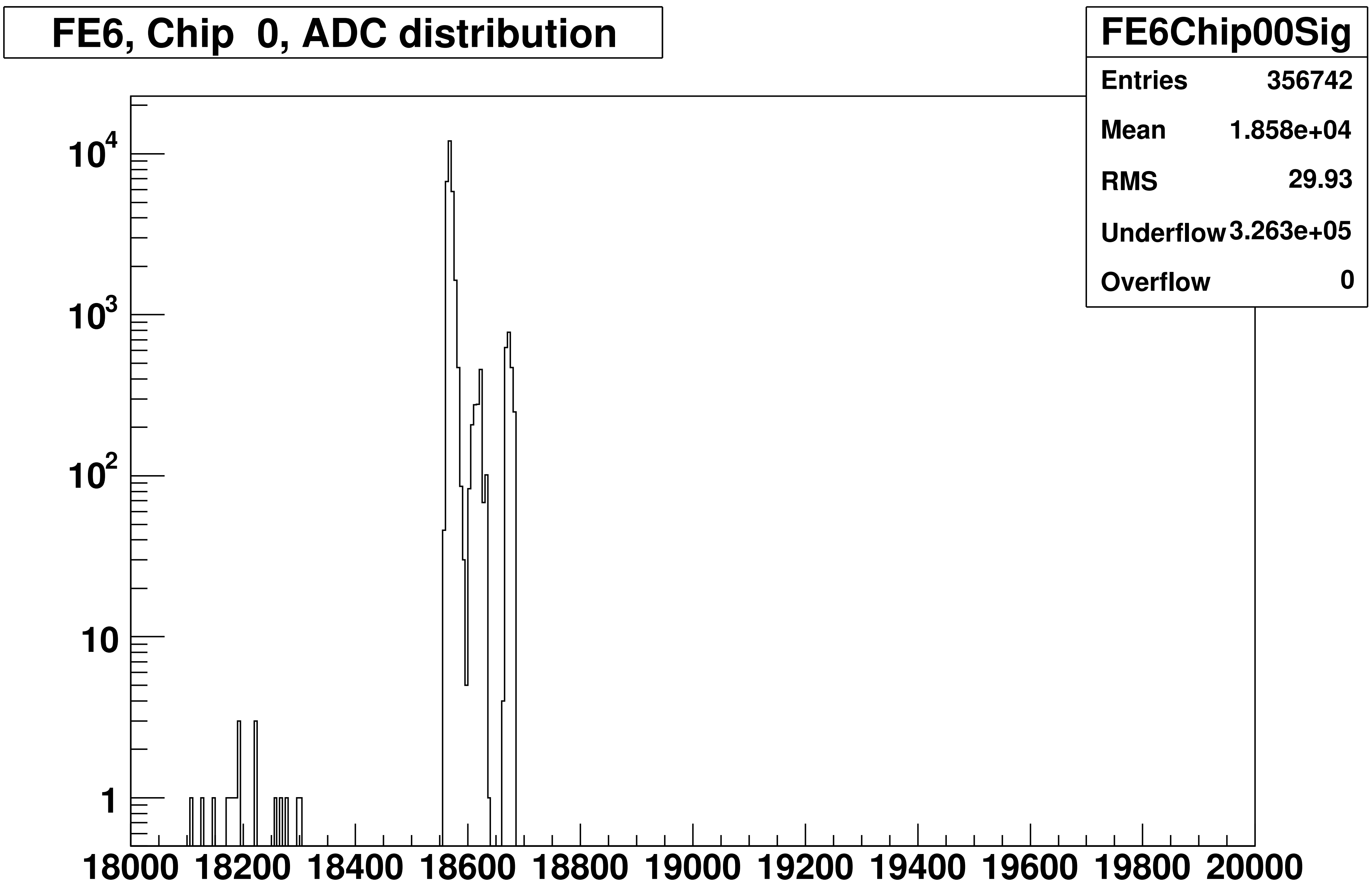
-50
0
50
100
150
200
1
10
10^2
10^3
10^4
10^5


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 356742
Mean 1.858e+04
RMS 29.93
Underflow 3.263e+05
Overflow 0
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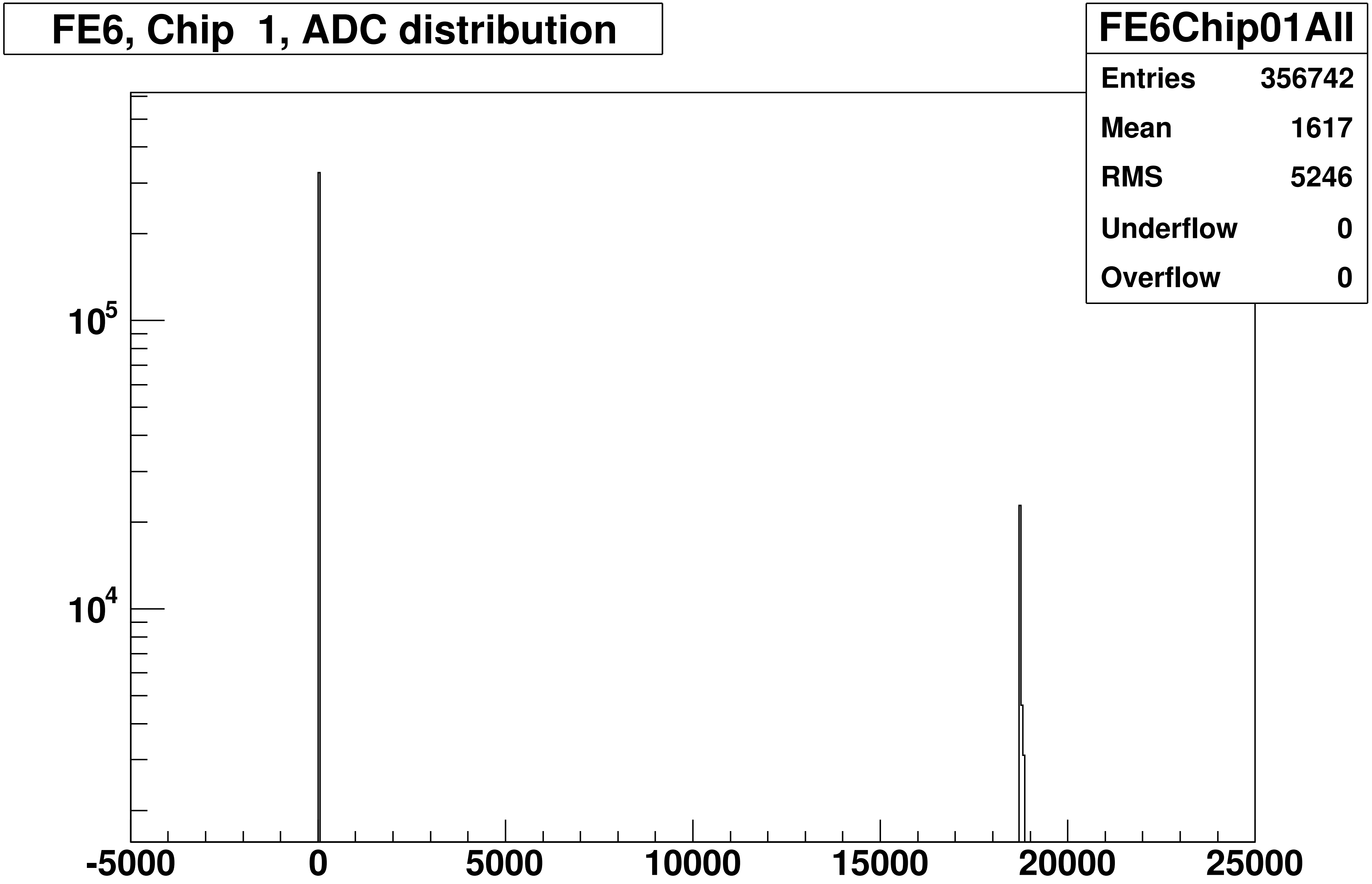
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 356742
Mean 1617
RMS 5246
Underflow 0
Overflow 0
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10^4
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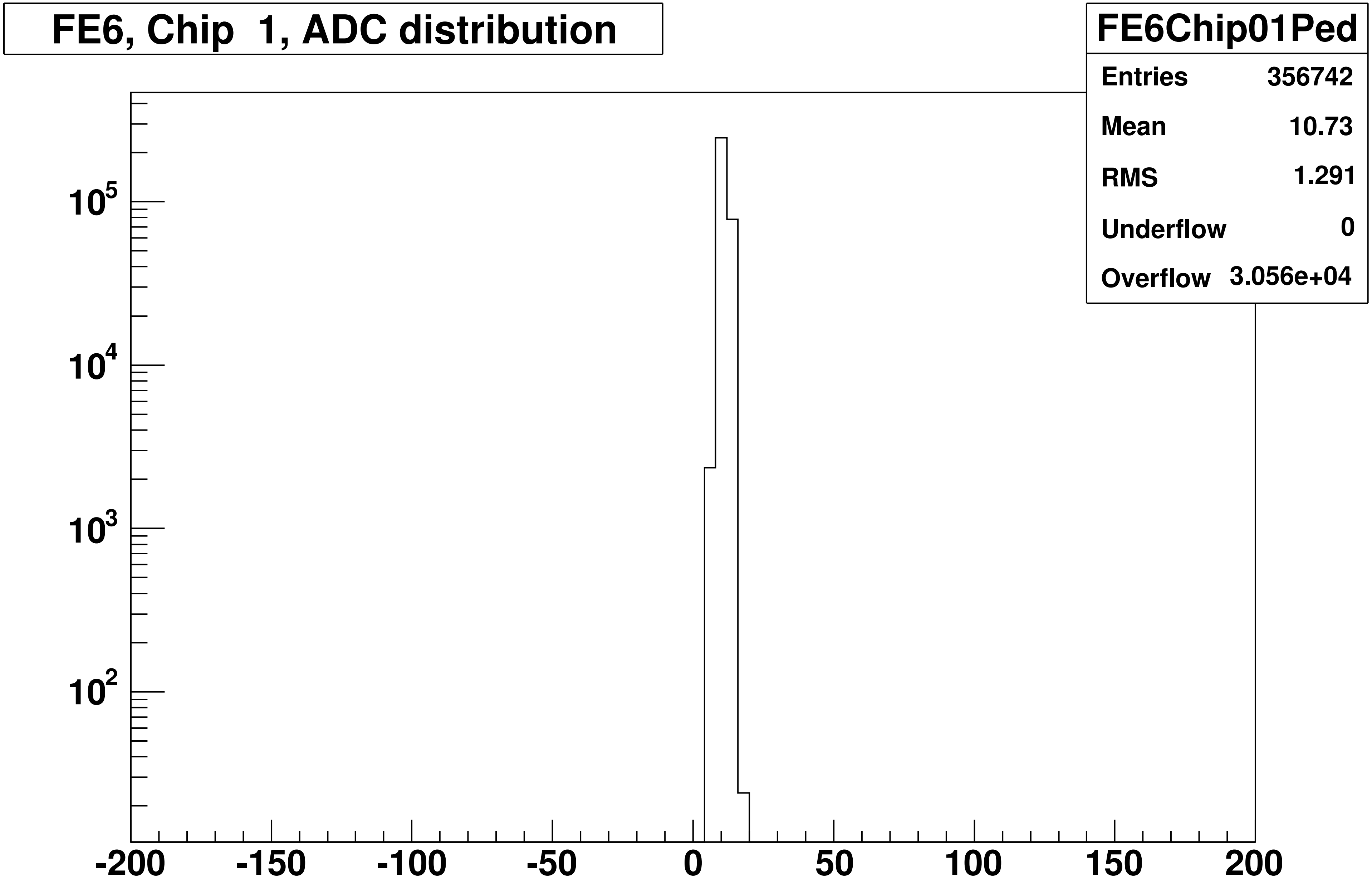
5000
10000
15000
20000
25000


FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 356742
Mean 10.73
RMS 1.291
Underflow 0
Overflow 3.056e+04
10^5
10^4
10^3
10^2
-200
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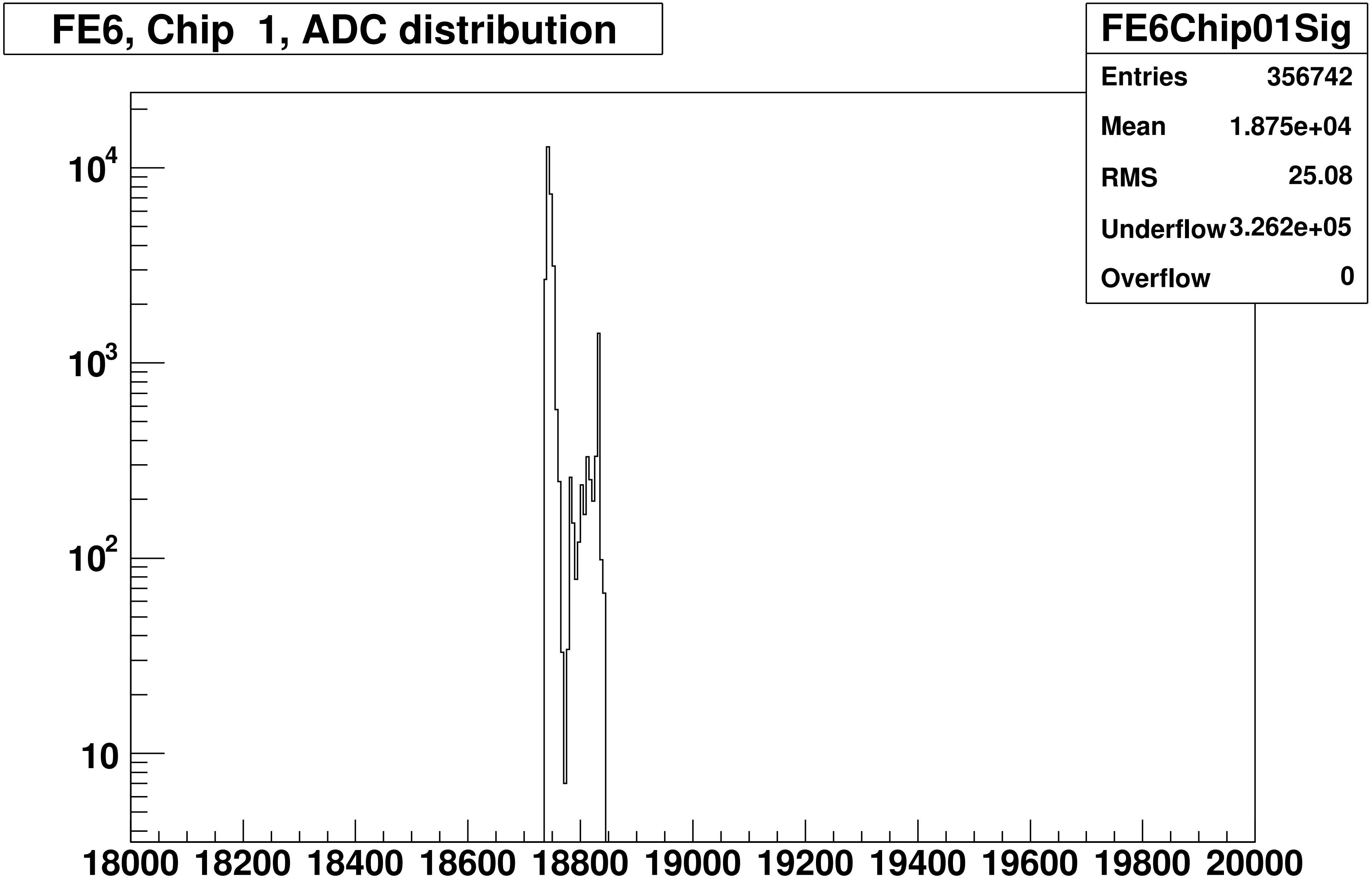
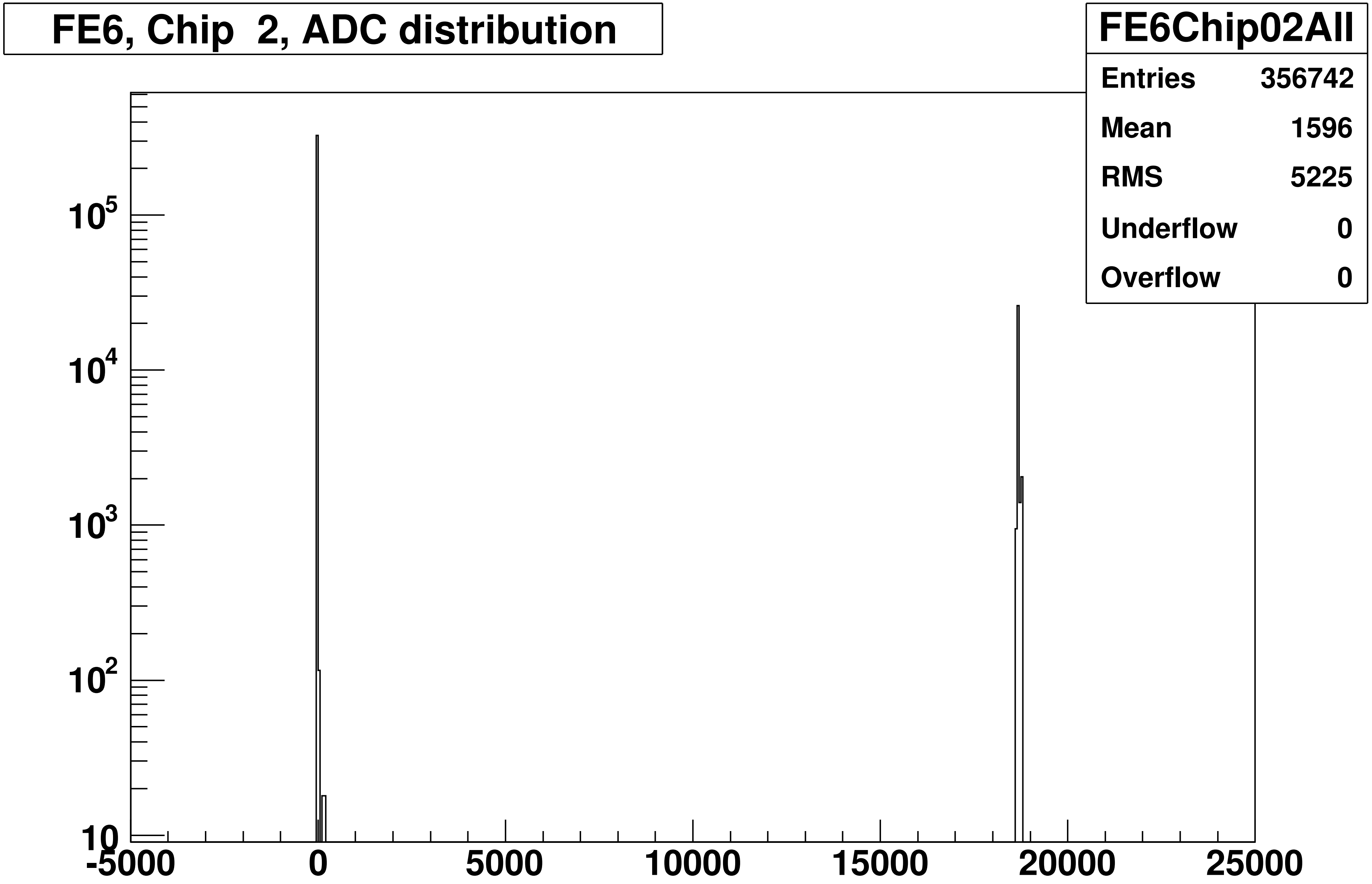
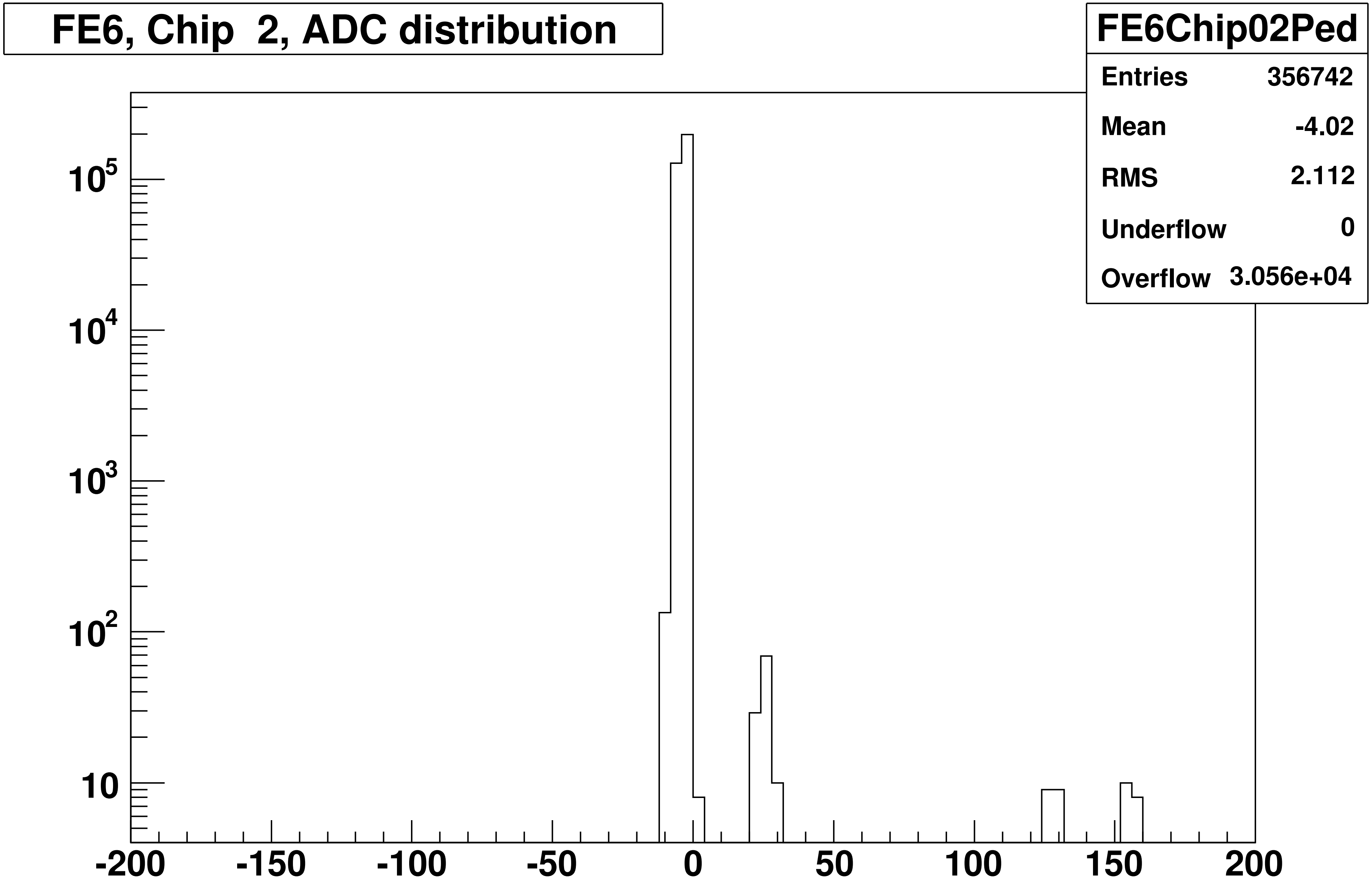
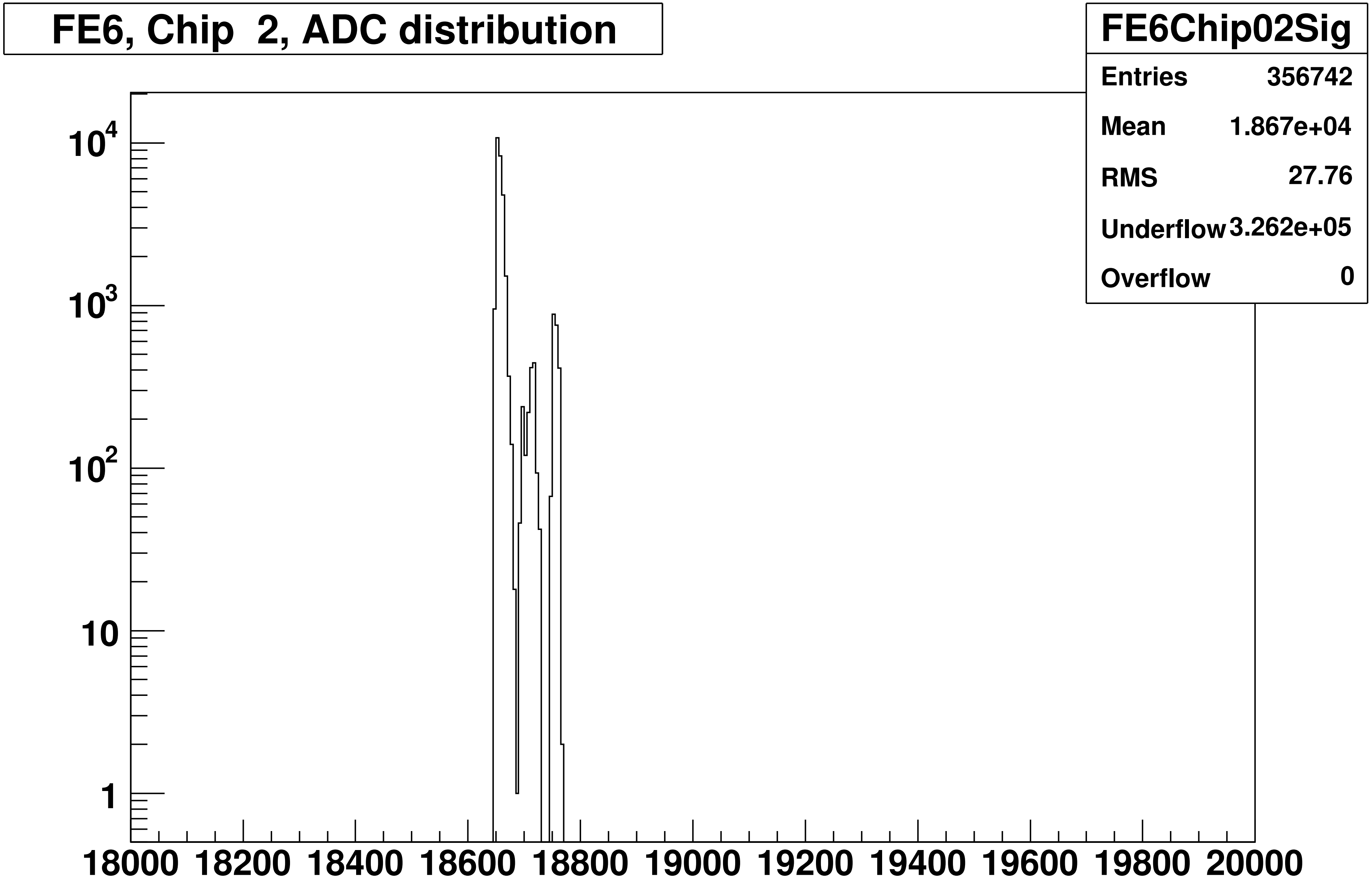
-100
-50
0
50
100
150
200


FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 356742
Mean 1.875e+04
RMS 25.08
Underflow 3.262e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 356742
Mean 1596
RMS 5225
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 356742
Mean -4.02
RMS 2.112
Underflow 0
Overflow 3.056e+04
10
10^2
10^3
10^4
10^5
-200 -150 -100 -50 0 50 100 150 200


FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 356742
Mean 1.867e+04
RMS 27.76
Underflow 3.262e+05
Overflow 0
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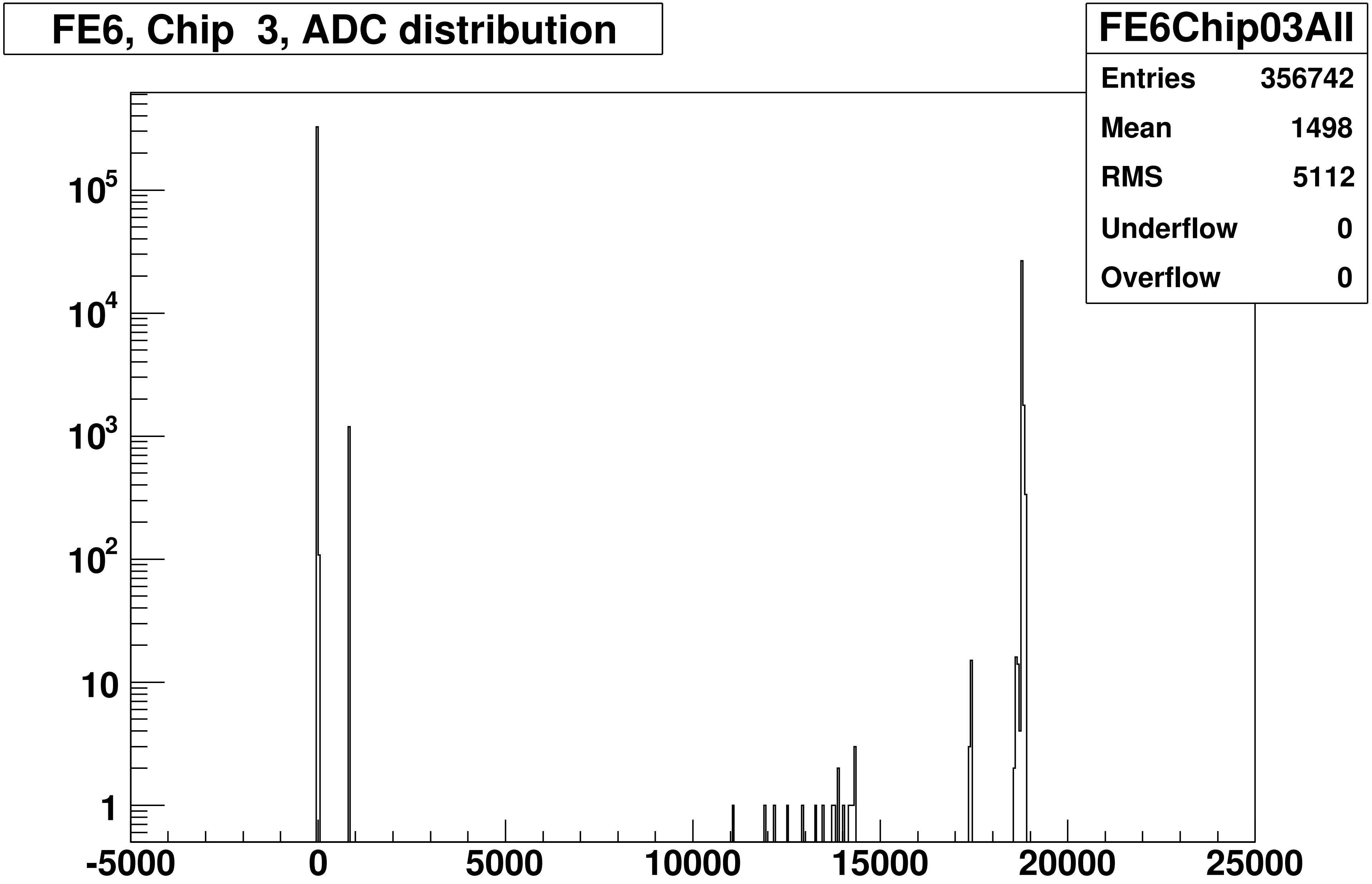
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 356742
Mean 1498
RMS 5112
Underflow 0
Overflow 0
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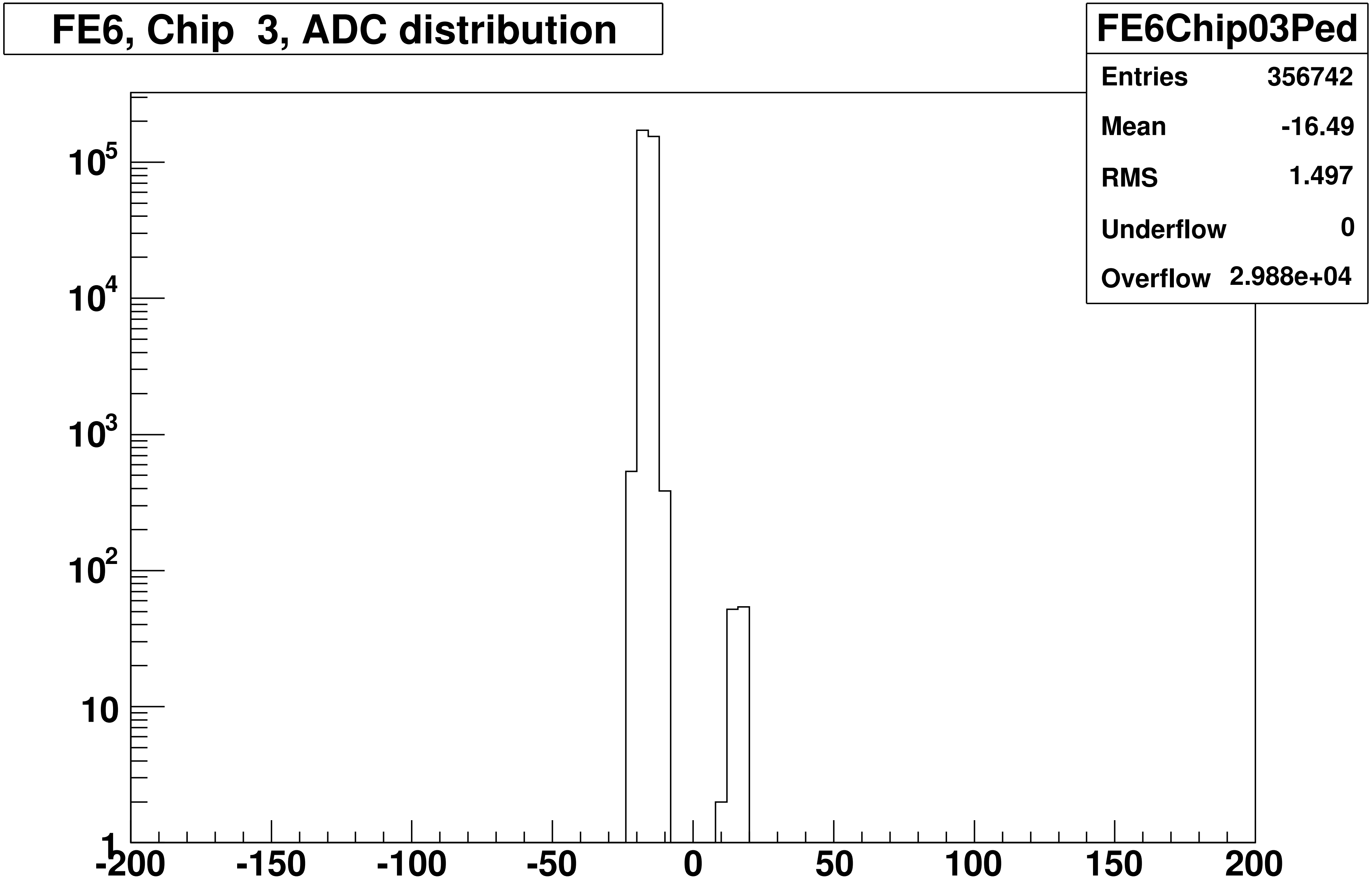
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 356742
Mean -16.49
RMS 1.497
Underflow 0
Overflow 2.988e+04
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10
10^2
10^3
10^4
10^5
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-100
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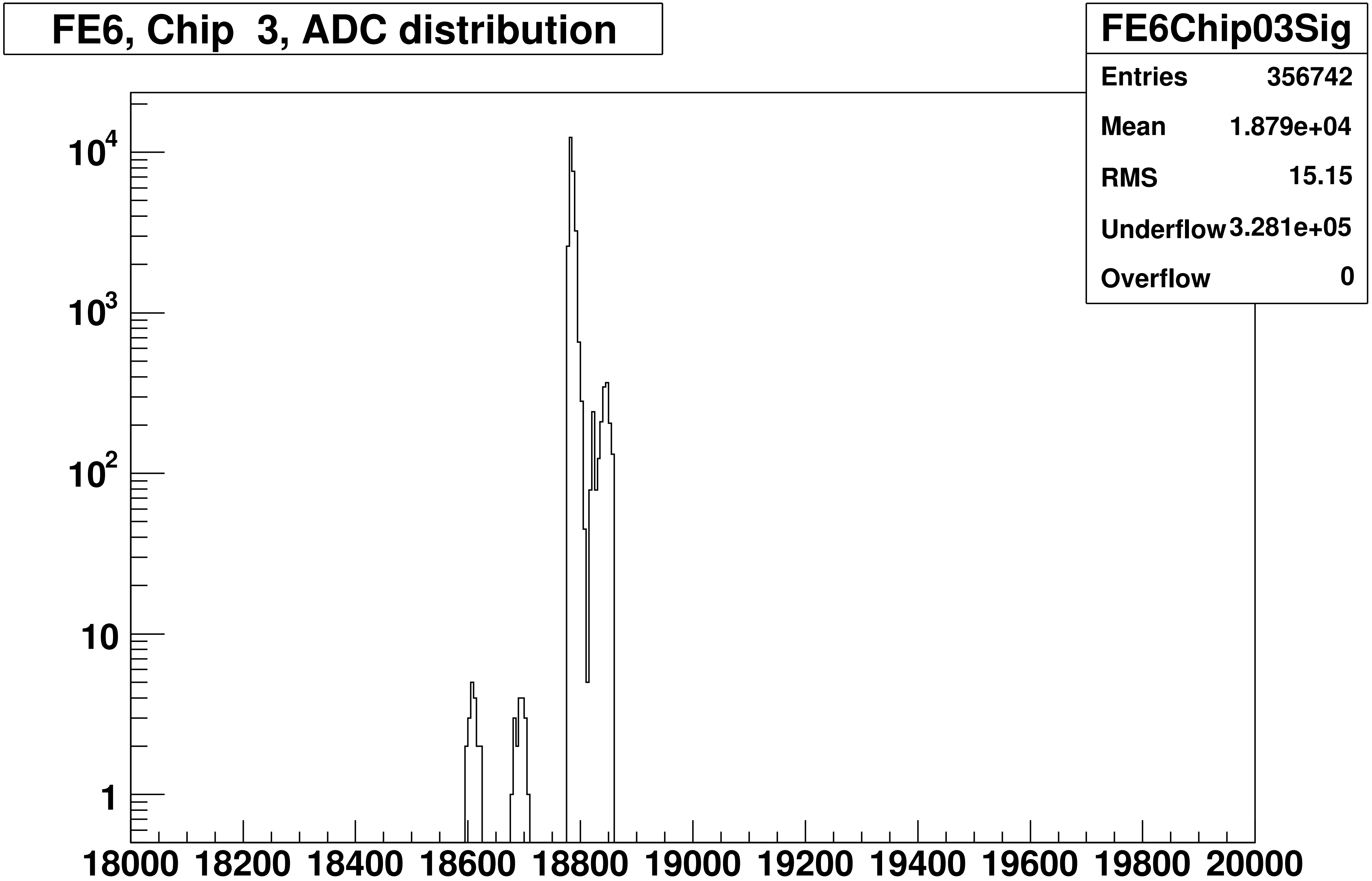
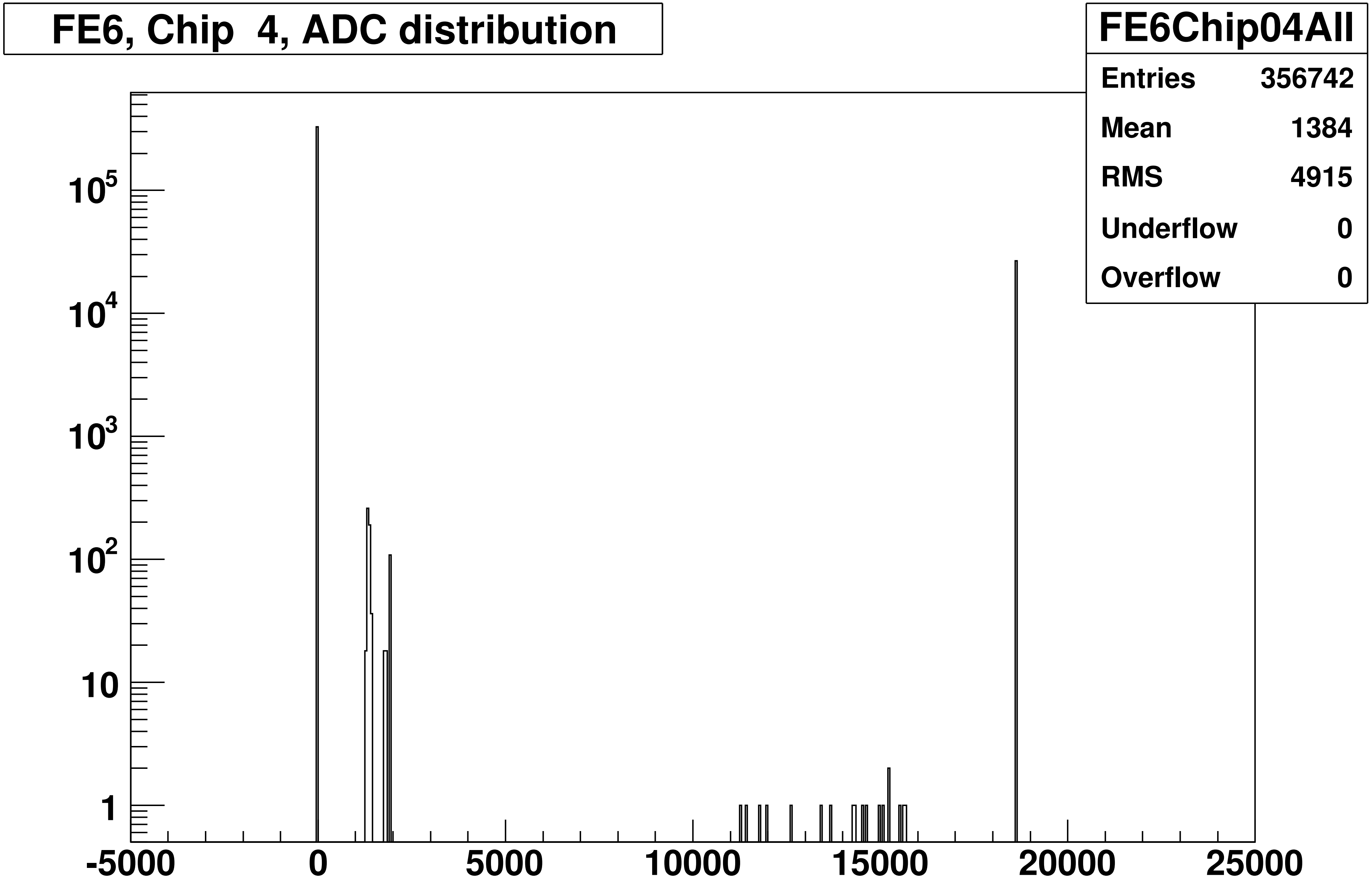
0
50
100
150
200


FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 356742
Mean 1.879e+04
RMS 15.15
Underflow 3.281e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 356742
Mean 1384
RMS 4915
Underflow 0
Overflow 0
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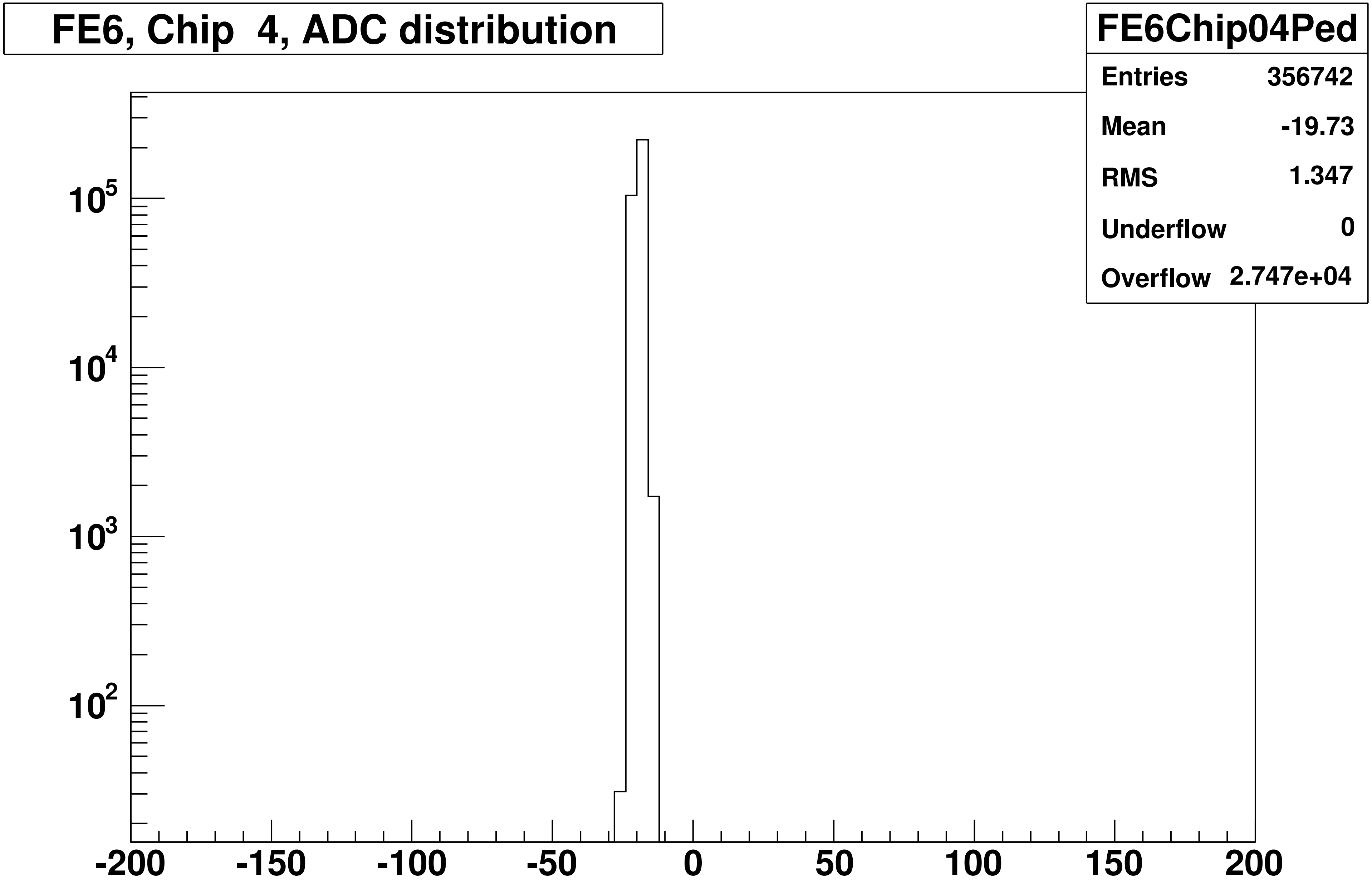
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 356742
Mean -19.73
RMS 1.347
Underflow 0
Overflow 2.747e+04
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10^4
10^3
10^2
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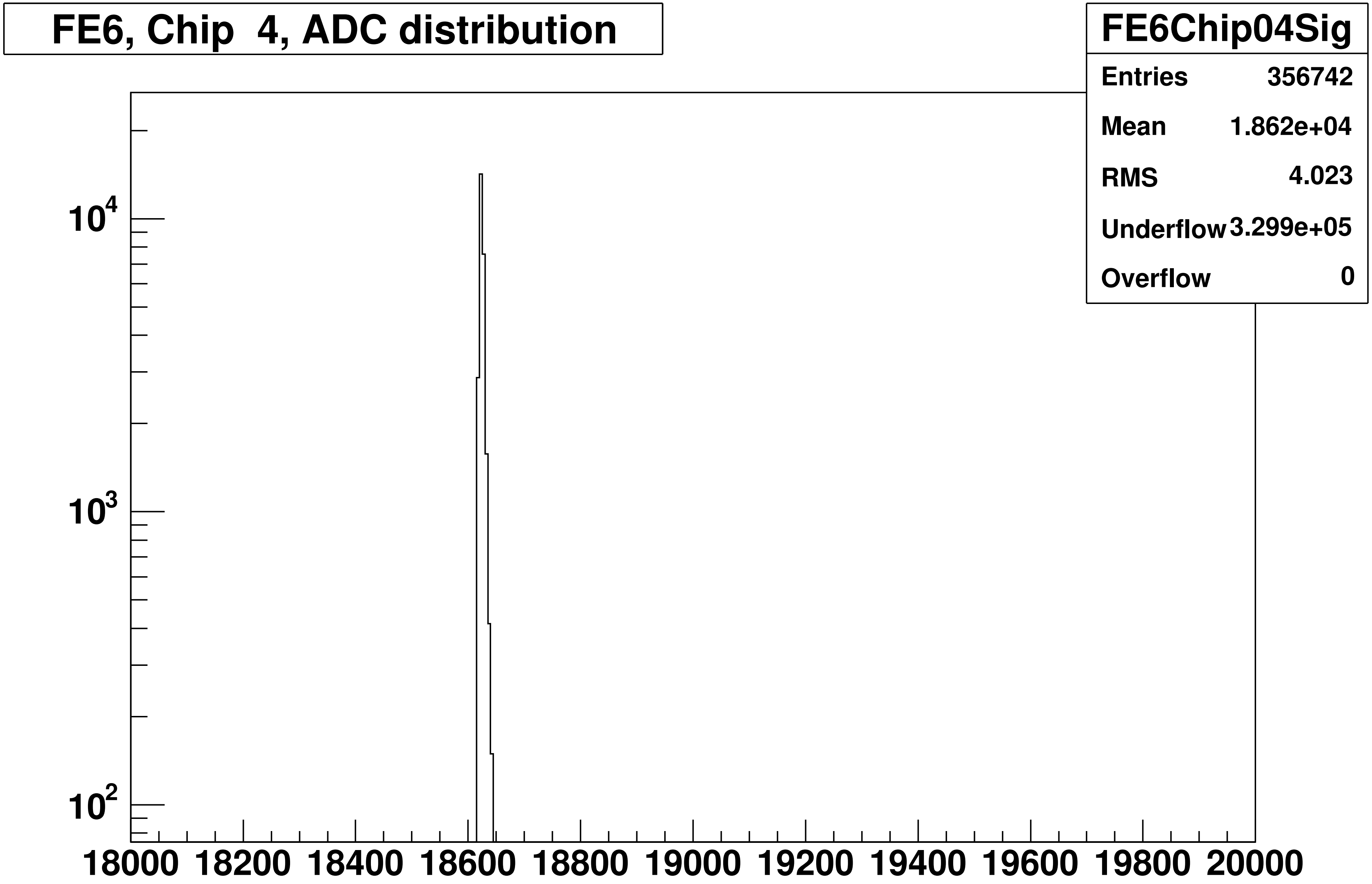
150
200



FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 356742
Mean 1.862e+04
RMS 4.023
Underflow 3.299e+05
Overflow 0
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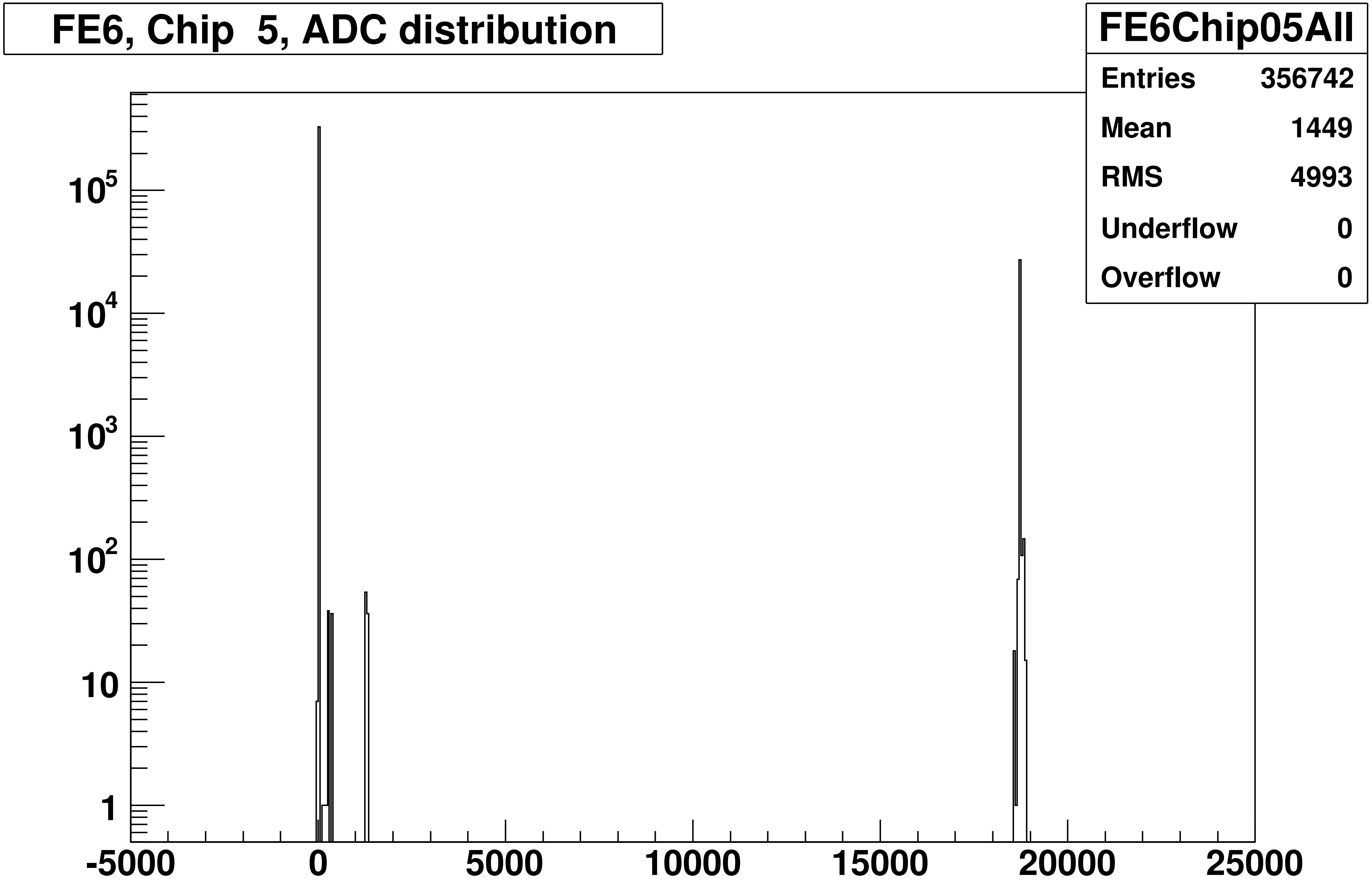
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 356742
Mean 1449
RMS 4993
Underflow 0
Overflow 0
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5000
10000
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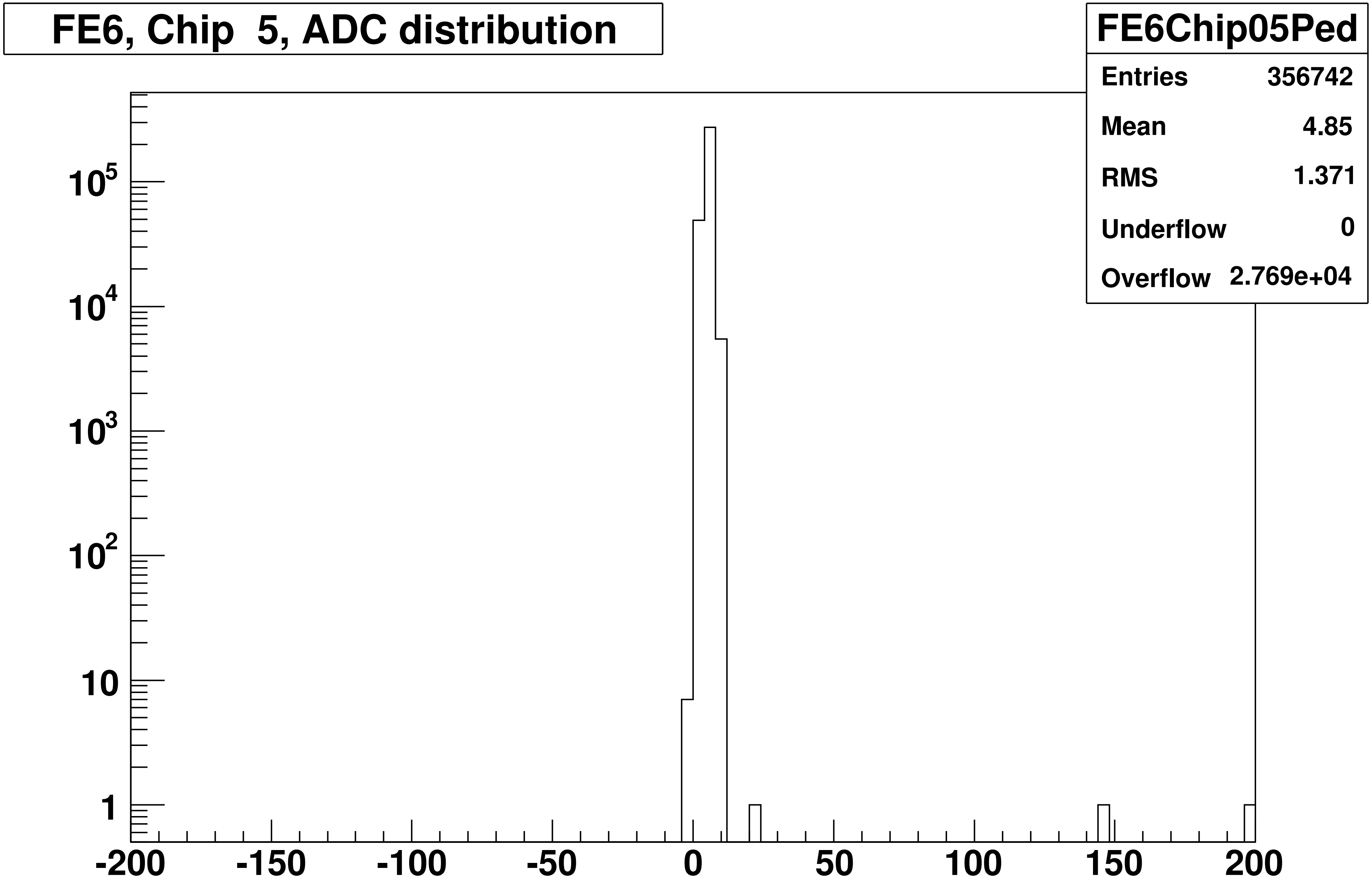
10^2
10^3
10^4
10^5



FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 356742
Mean 4.85
RMS 1.371
Underflow 0
Overflow 2.769e+04
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10^3
10^2
10
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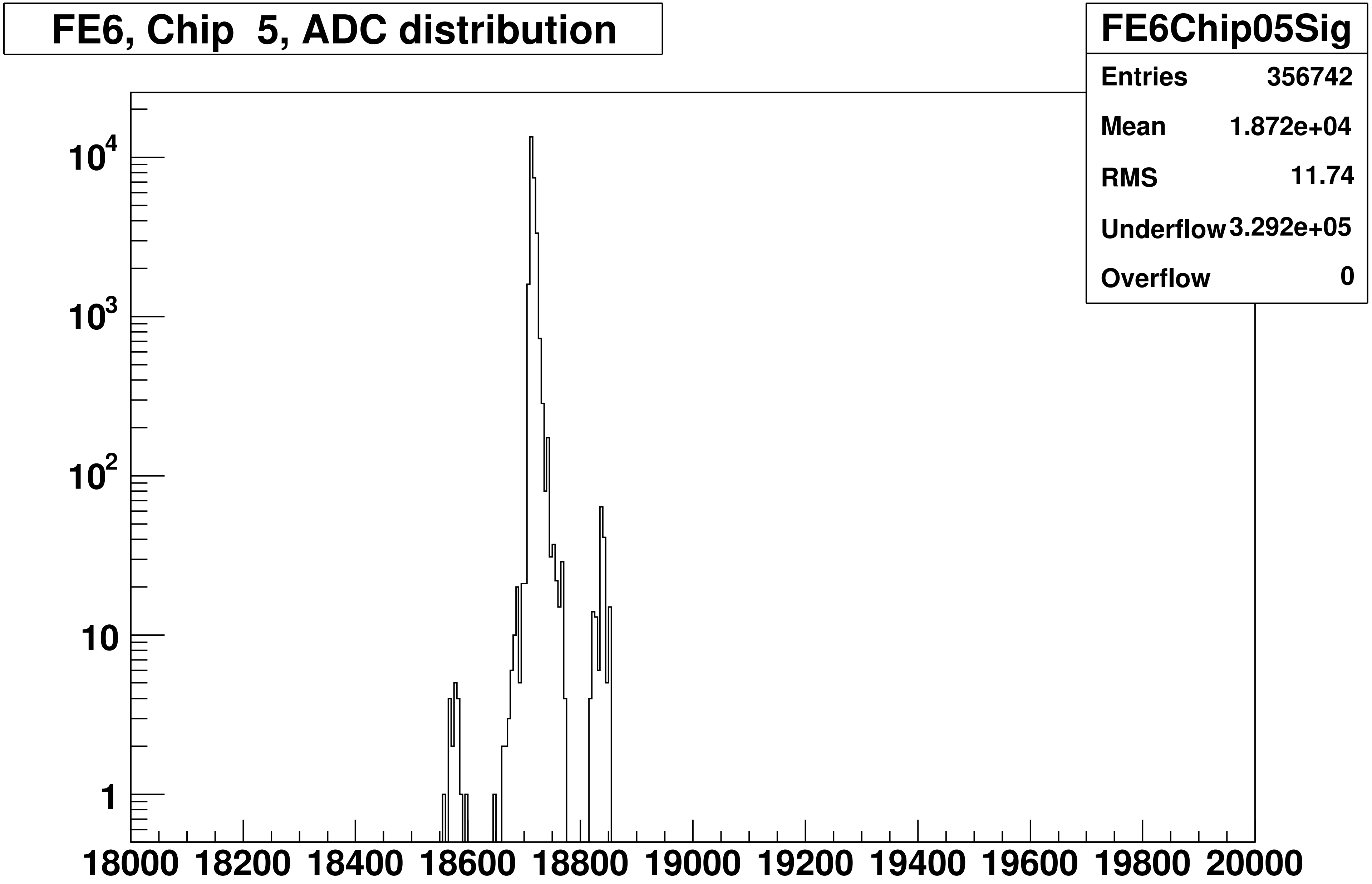
100
150
200



FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 356742
Mean 1.872e+04
RMS 11.74
Underflow 3.292e+05
Overflow 0
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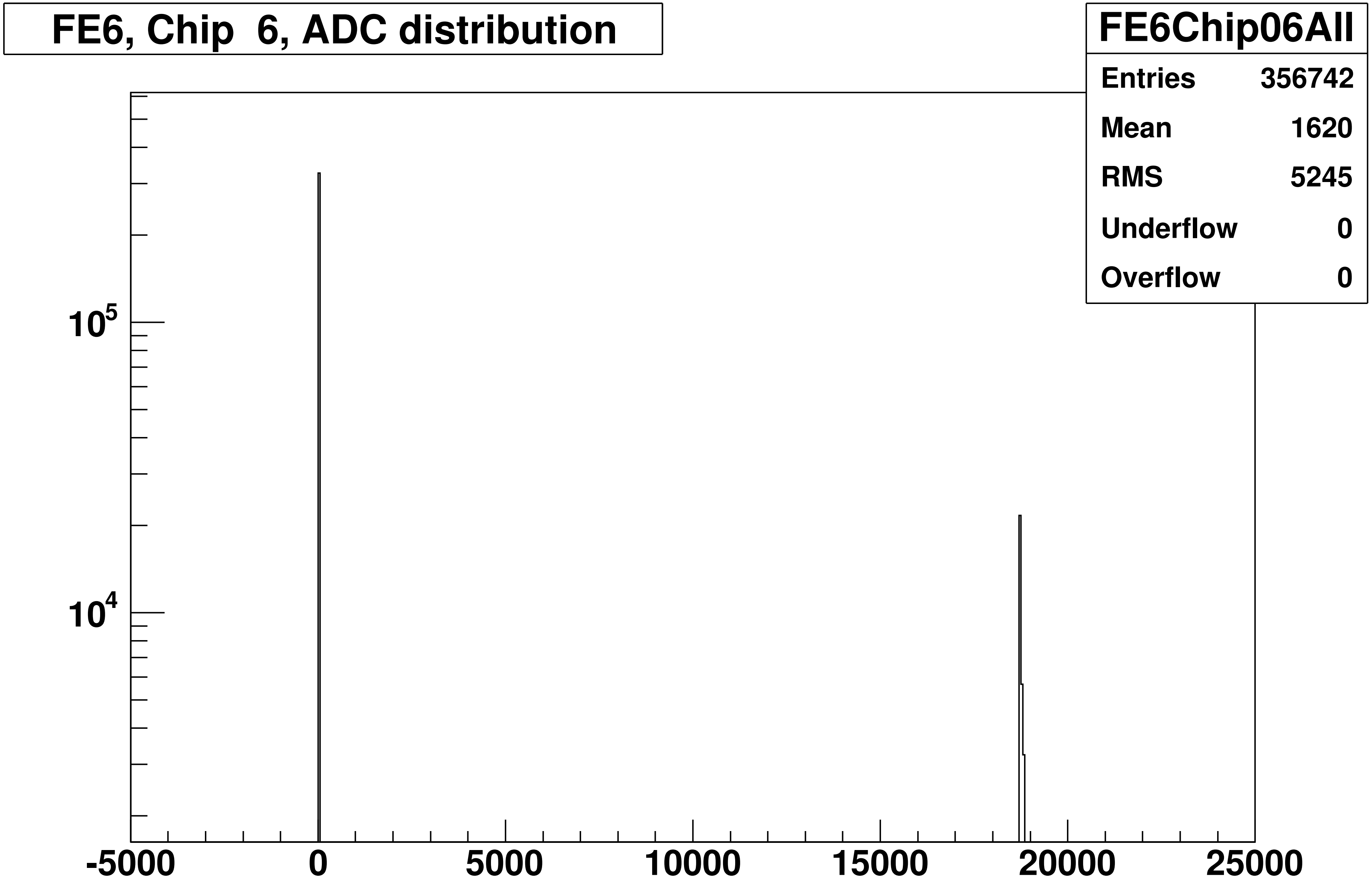
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 356742
Mean 1620
RMS 5245
Underflow 0
Overflow 0
10^5
10^4
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0
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10000
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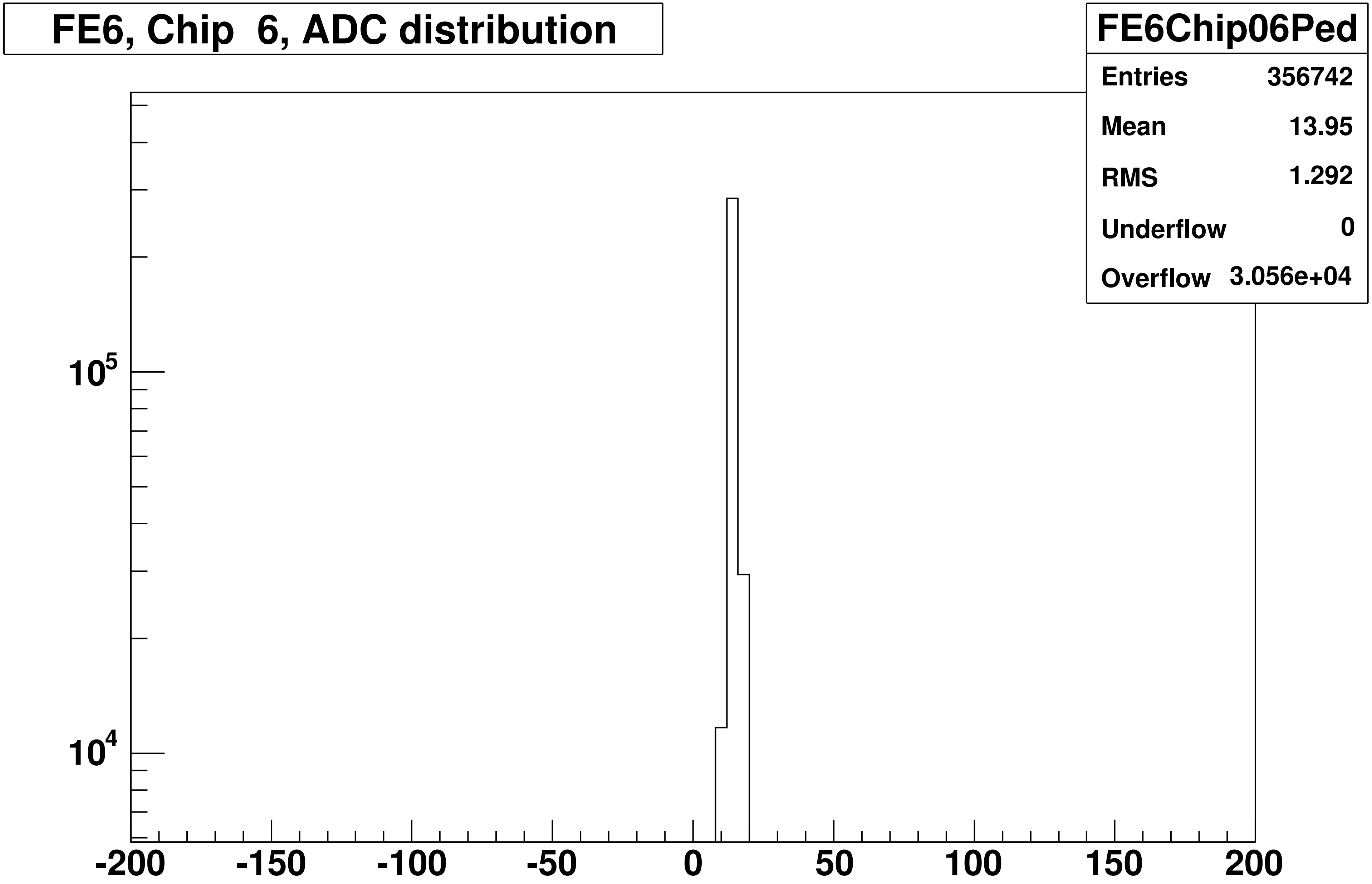
20000
25000


FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 356742
Mean 13.95
RMS 1.292
Underflow 0
Overflow 3.056e+04
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10^4
-200
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-100
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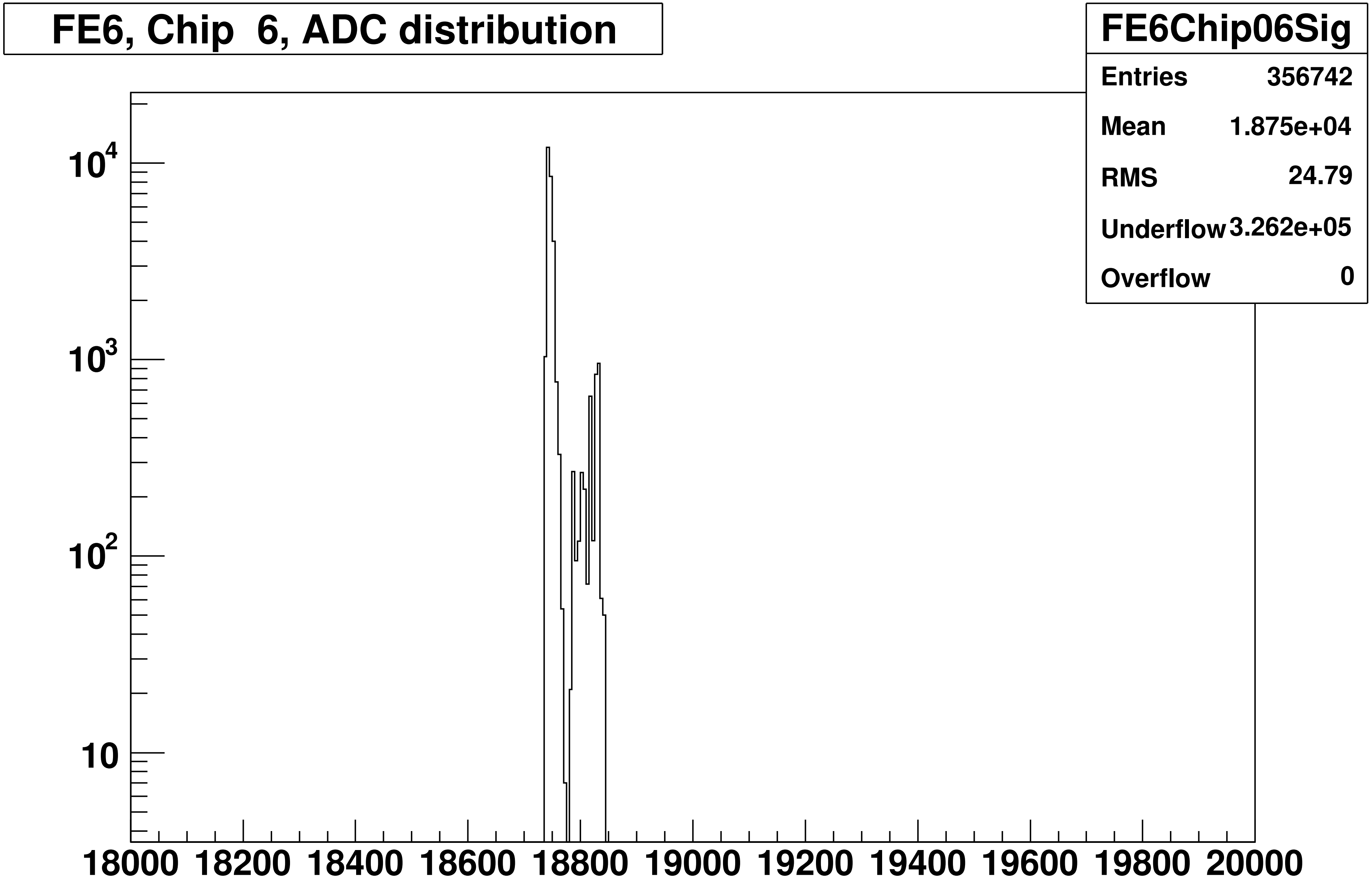
150
200



FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 356742
Mean 1.875e+04
RMS 24.79
Underflow 3.262e+05
Overflow 0
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10^3
10^2
10
18000
18200
18400
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19000
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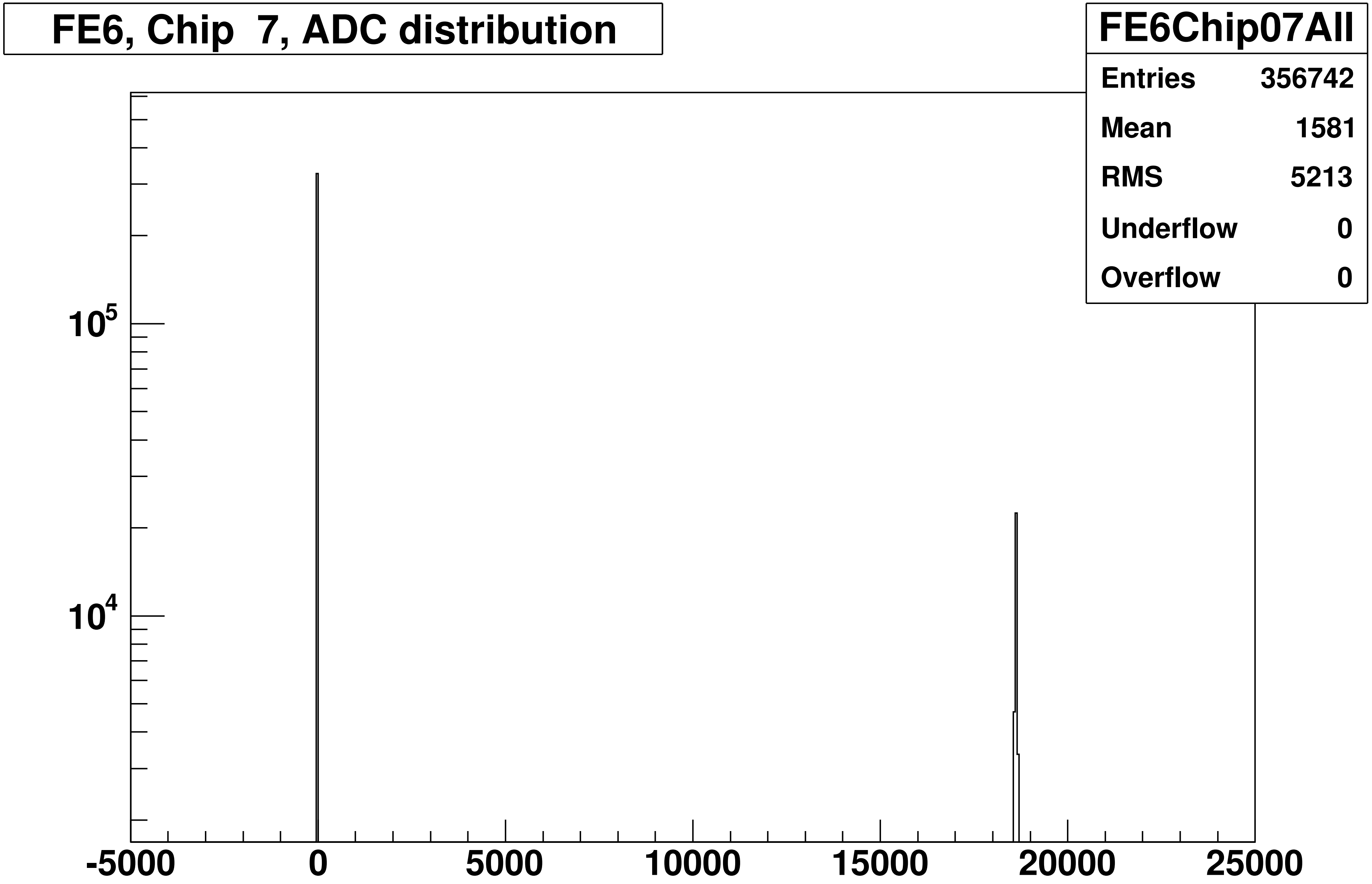
19600
19800
20000



FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 356742
Mean 1581
RMS 5213
Underflow 0
Overflow 0
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10^4
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0
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10000
15000
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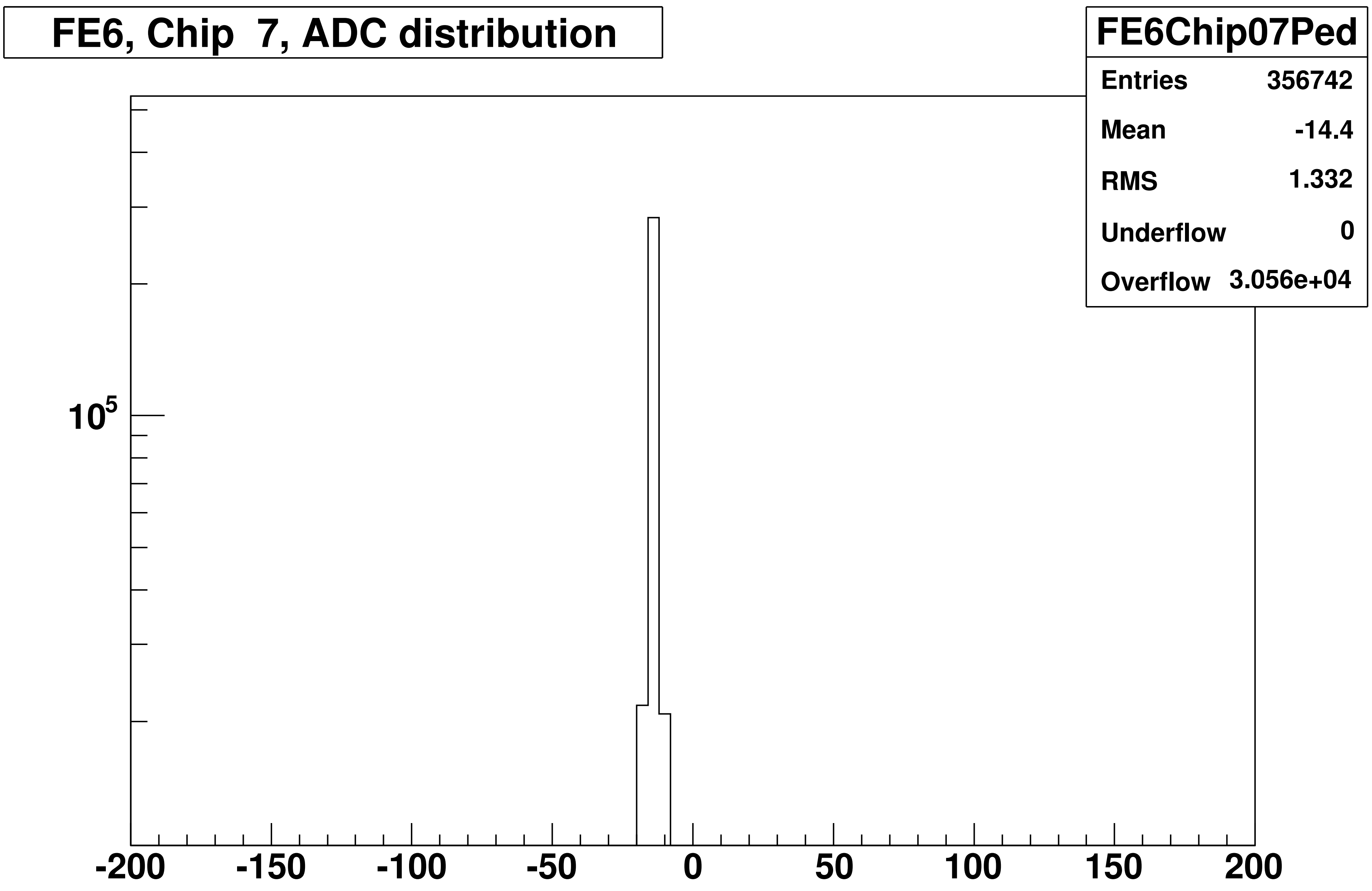
25000



FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 356742
Mean -14.4
RMS 1.332
Underflow 0
Overflow 3.056e+04
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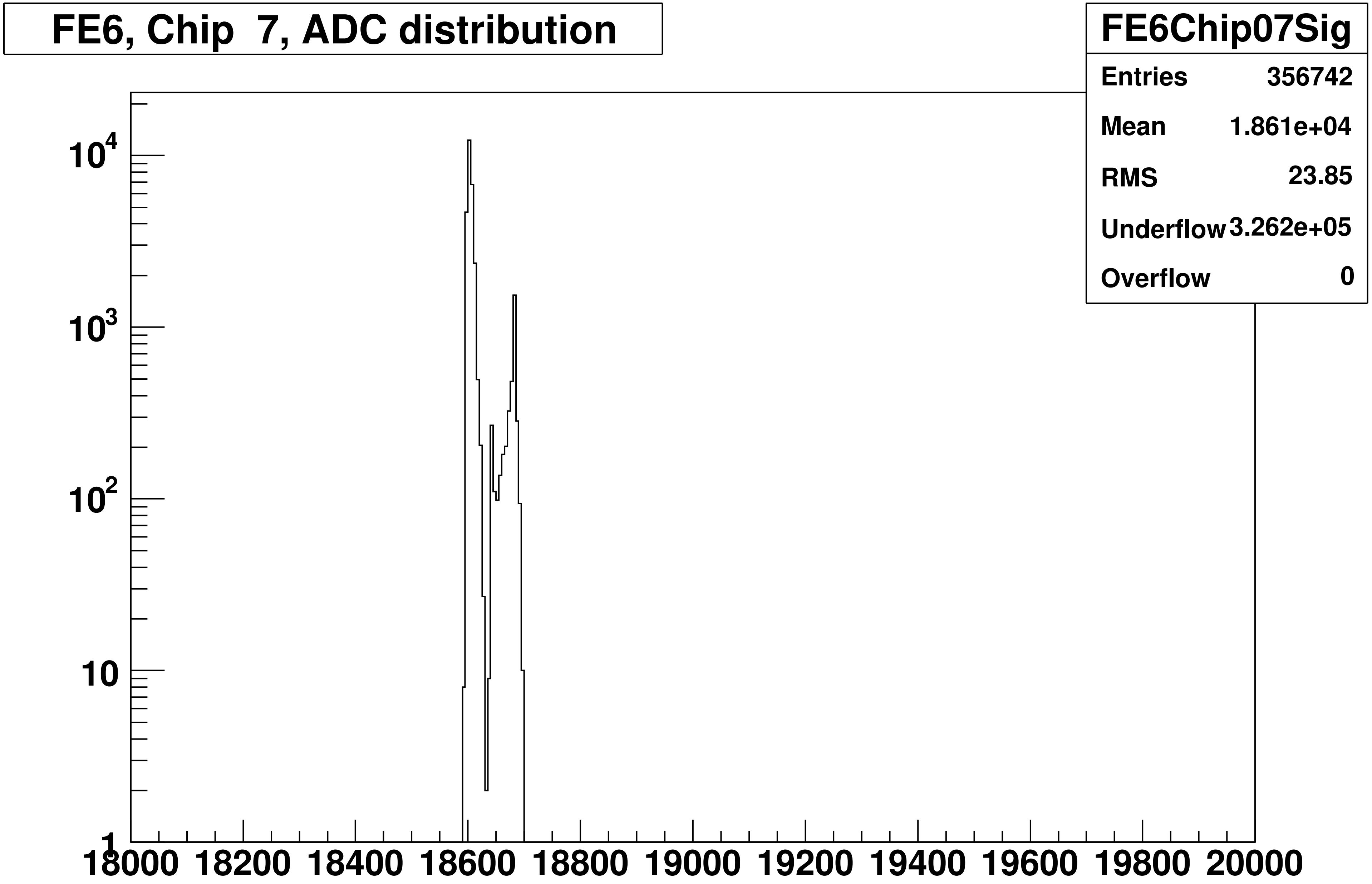
-100
-50
0
50
100
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 356742
Mean 1.861e+04
RMS 23.85
Underflow 3.262e+05
Overflow 0
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10^3
10^2
10
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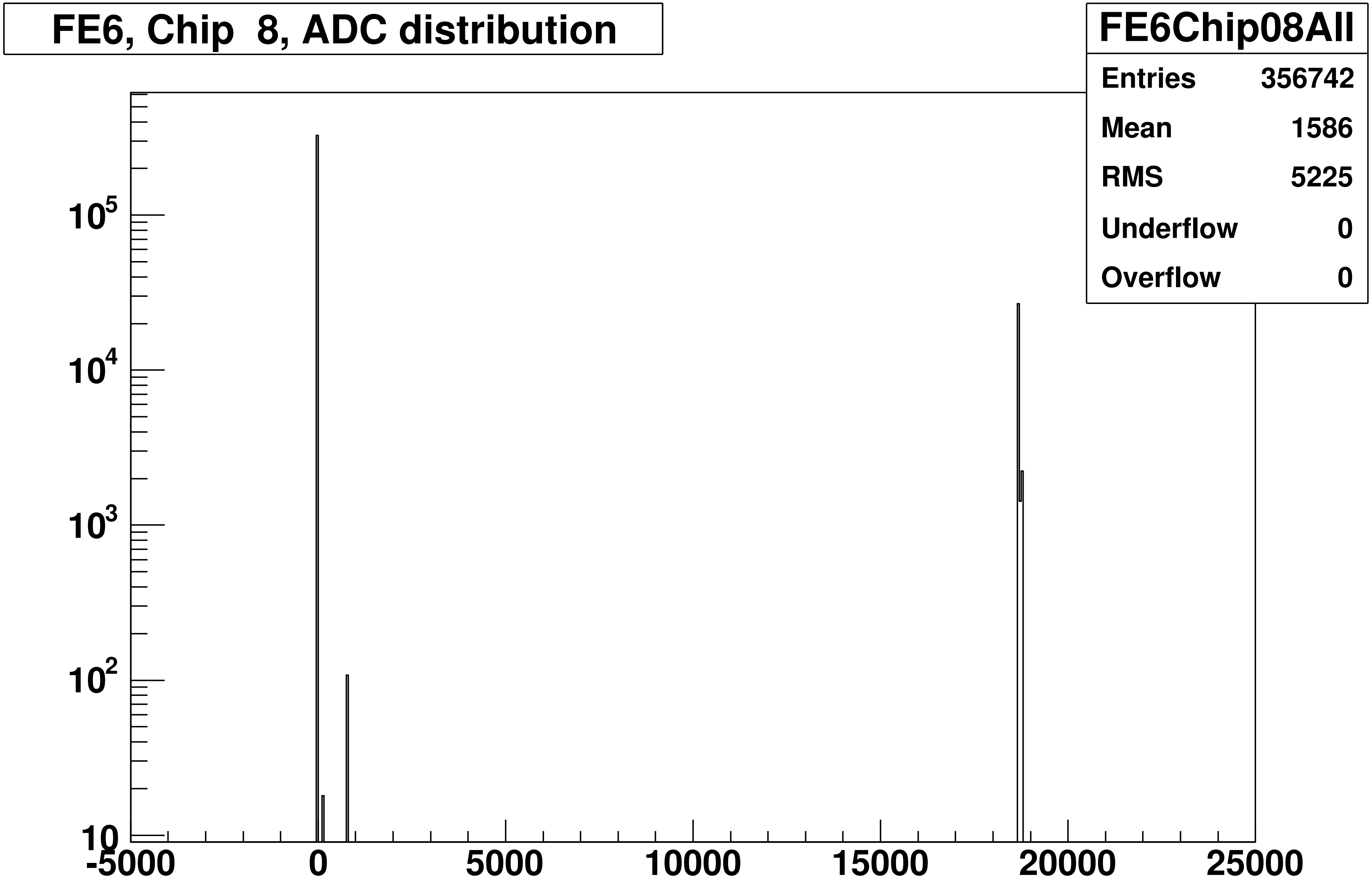
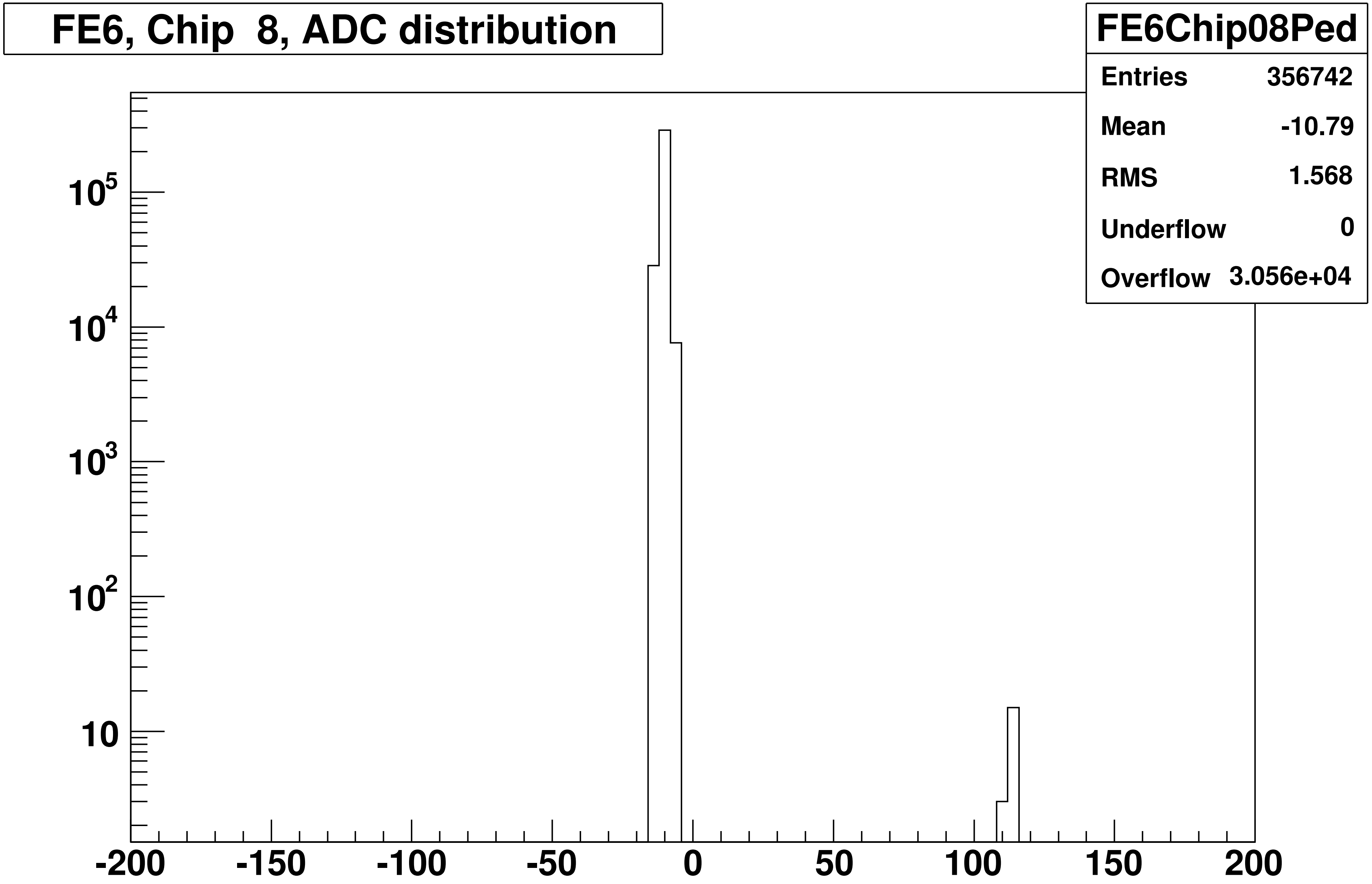
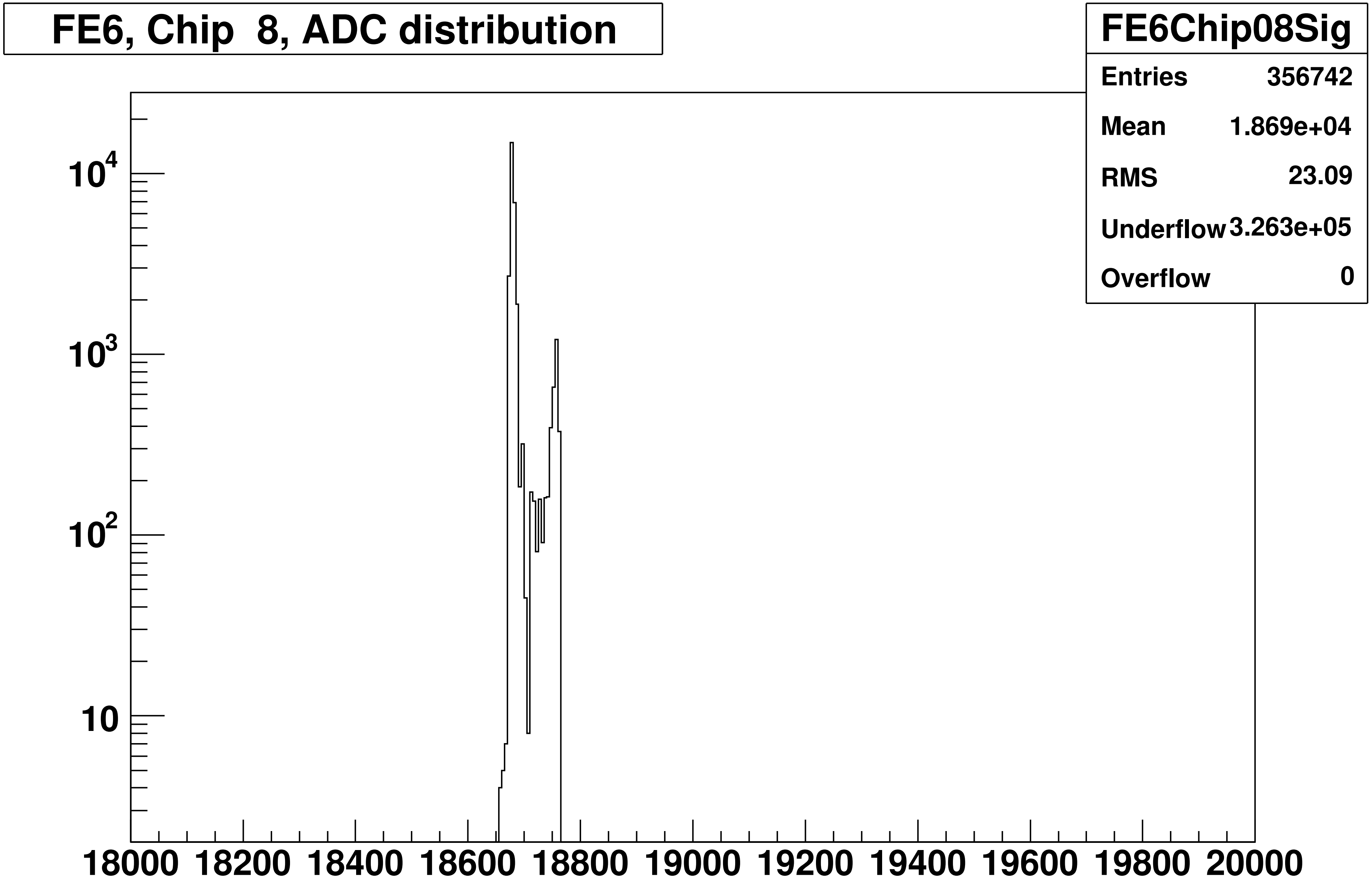
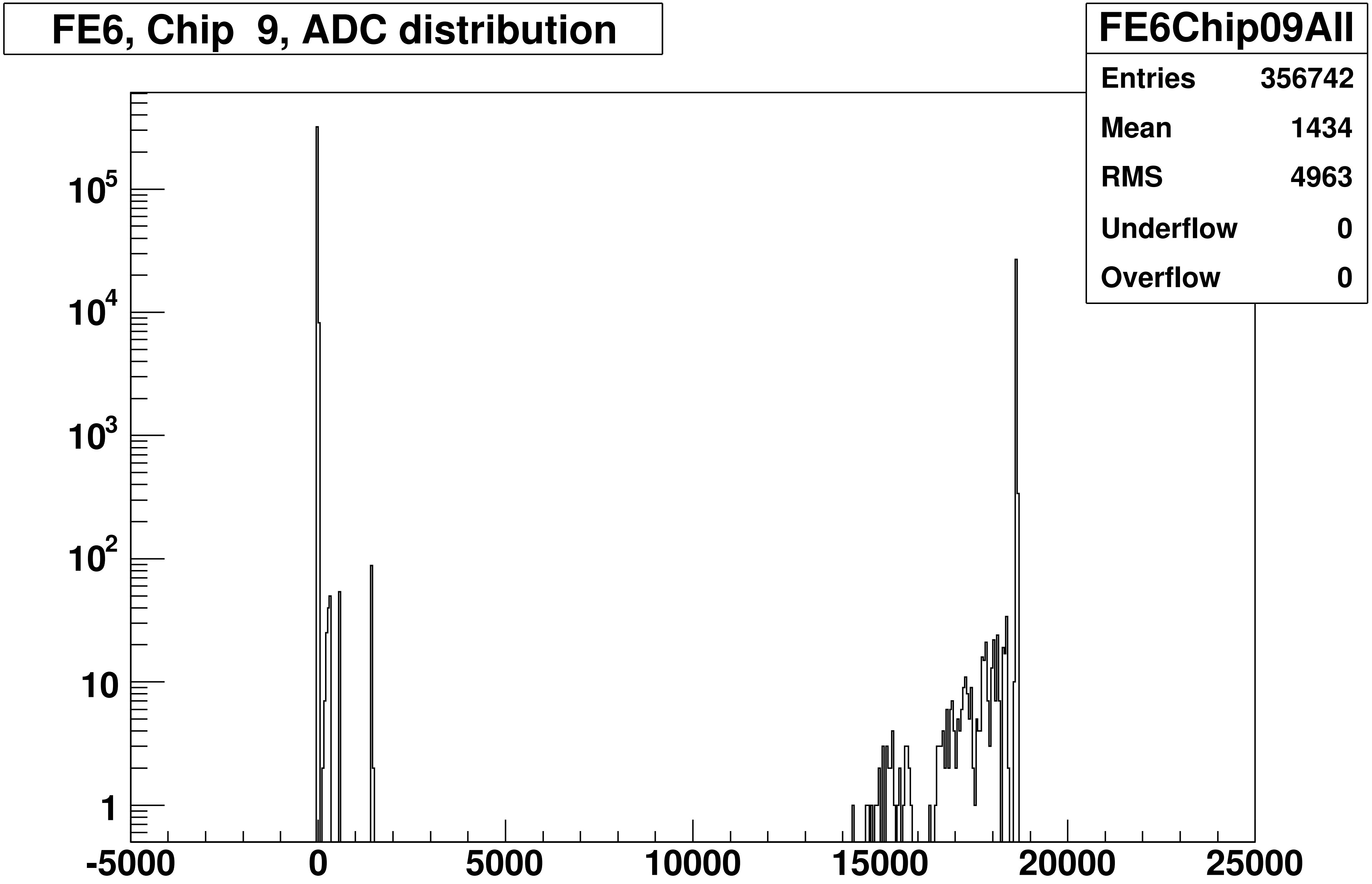
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 356742
Mean 1586
RMS 5225
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 356742
Mean -10.79
RMS 1.568
Underflow 0
Overflow 3.056e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 356742
Mean 1.869e+04
RMS 23.09
Underflow 3.263e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 356742
Mean 1434
RMS 4963
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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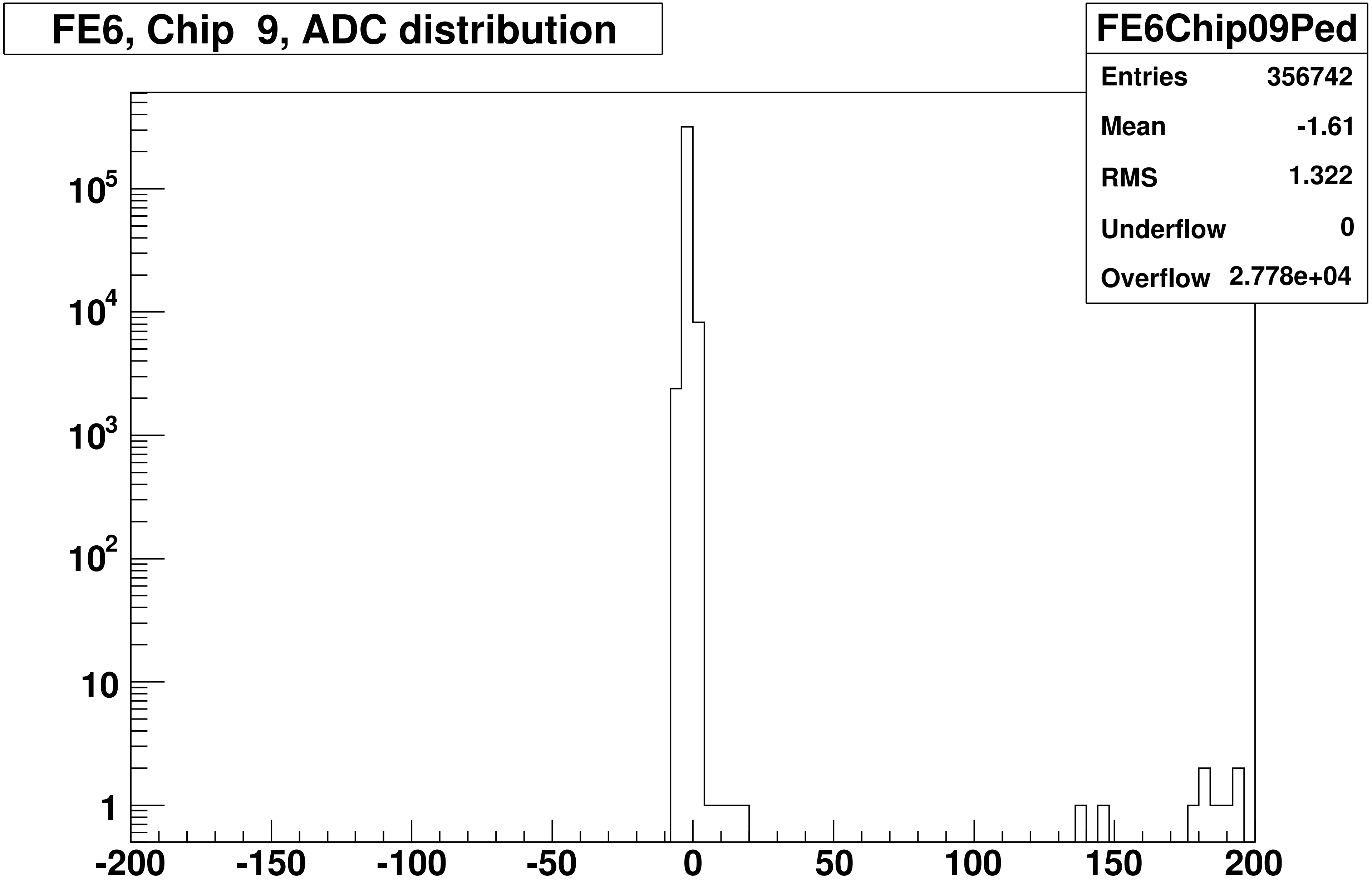
10000
15000
20000
25000


FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 356742
Mean -1.61
RMS 1.322
Underflow 0
Overflow 2.778e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
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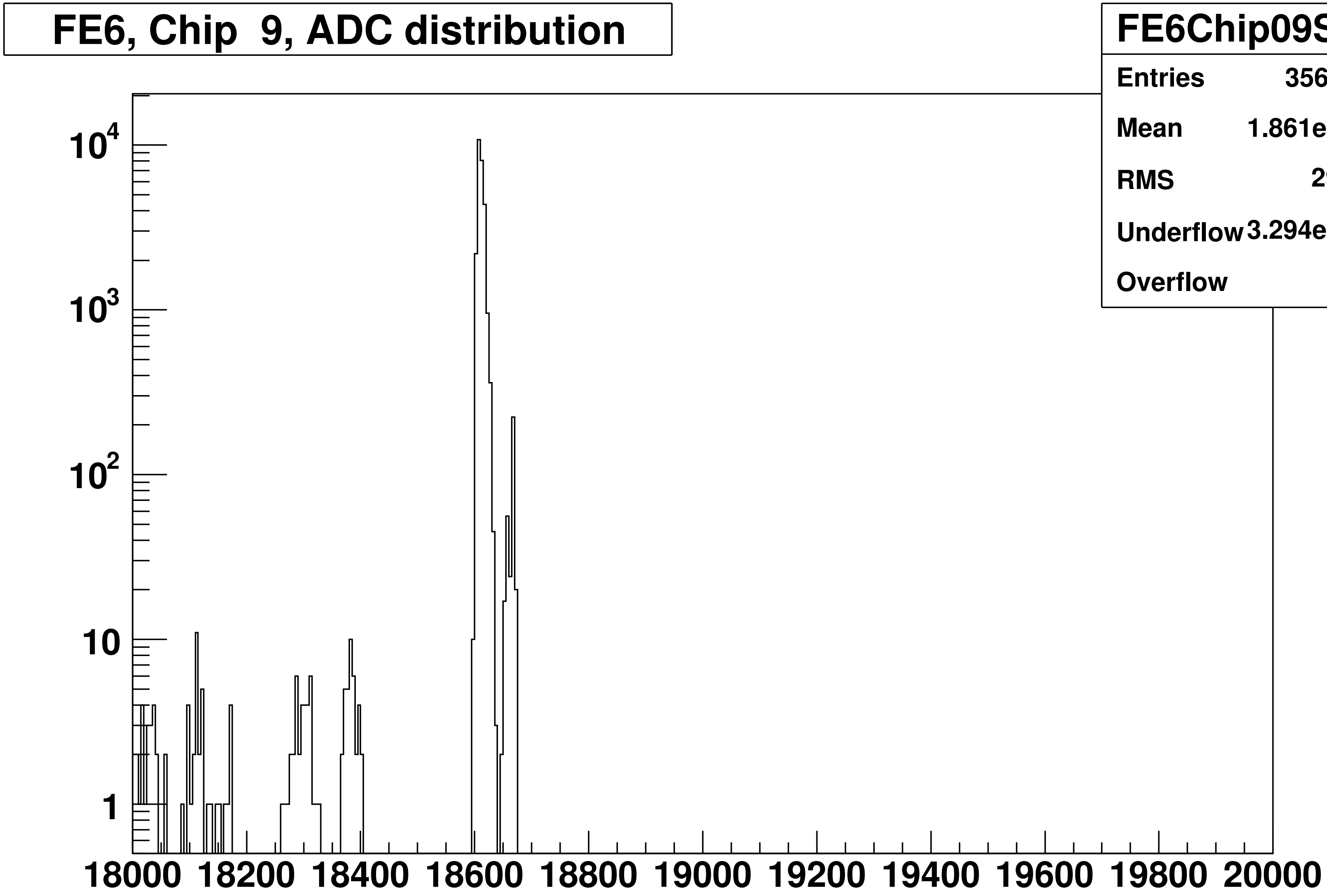
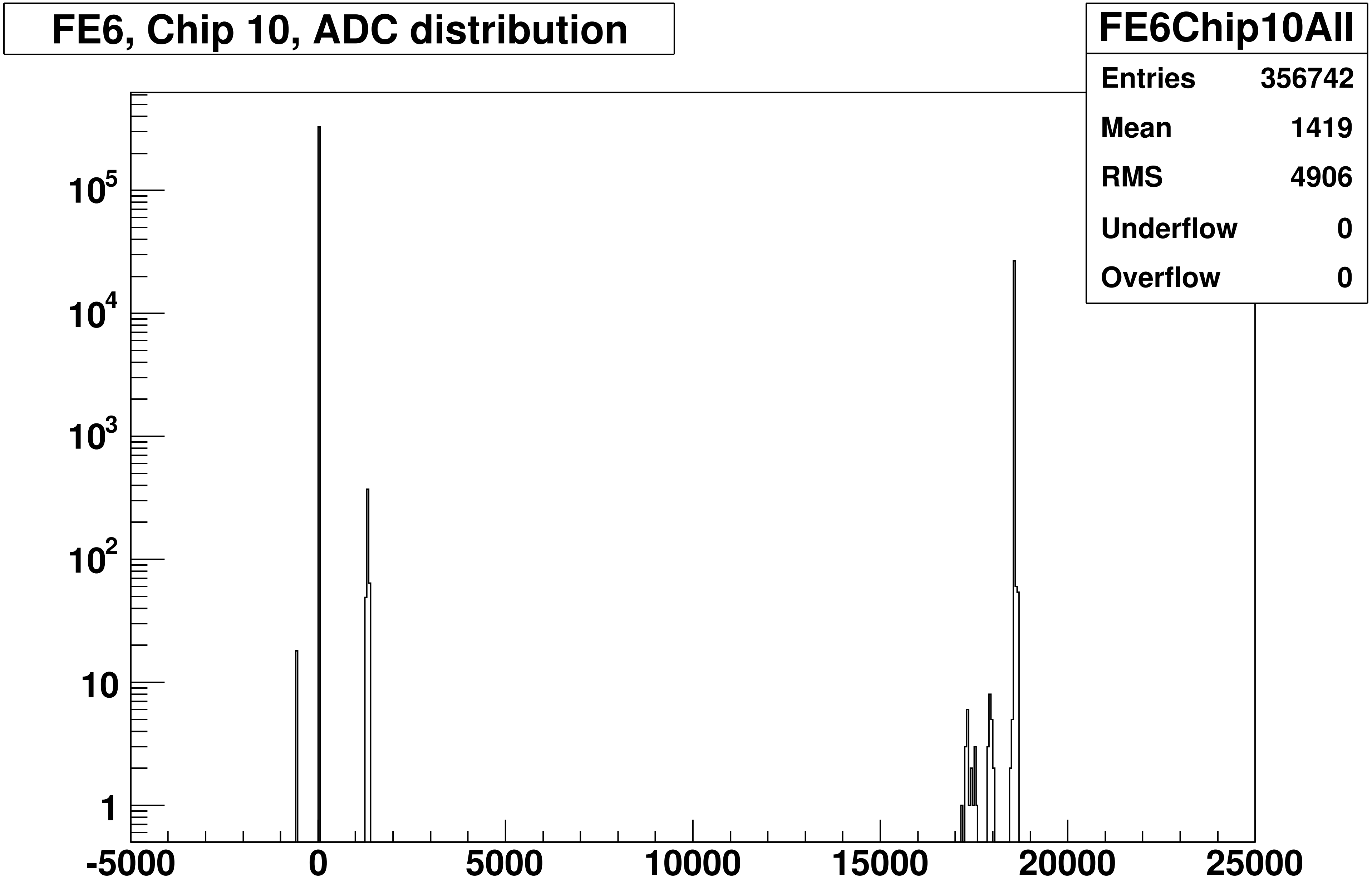
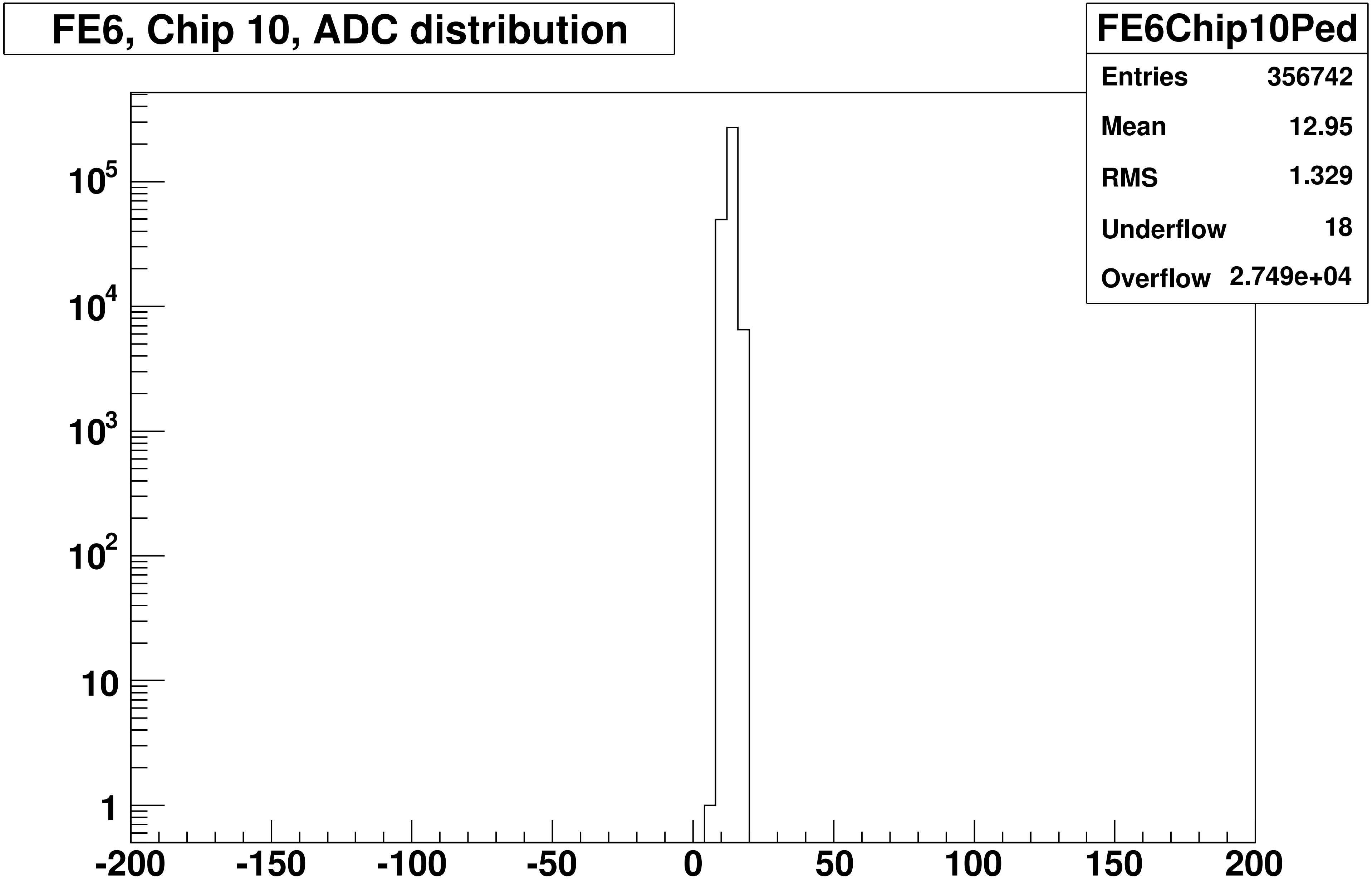
0
50
100
150
200

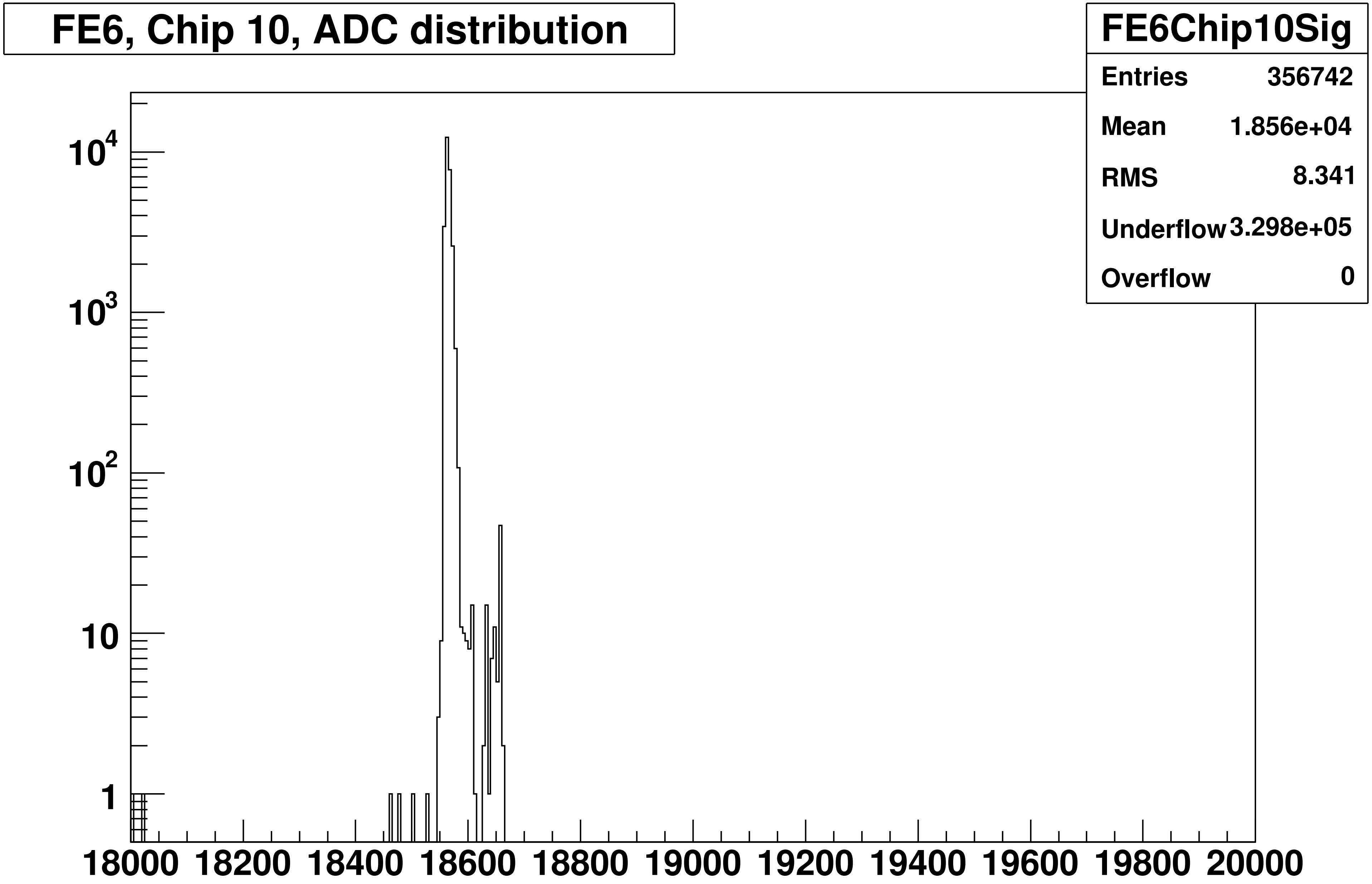


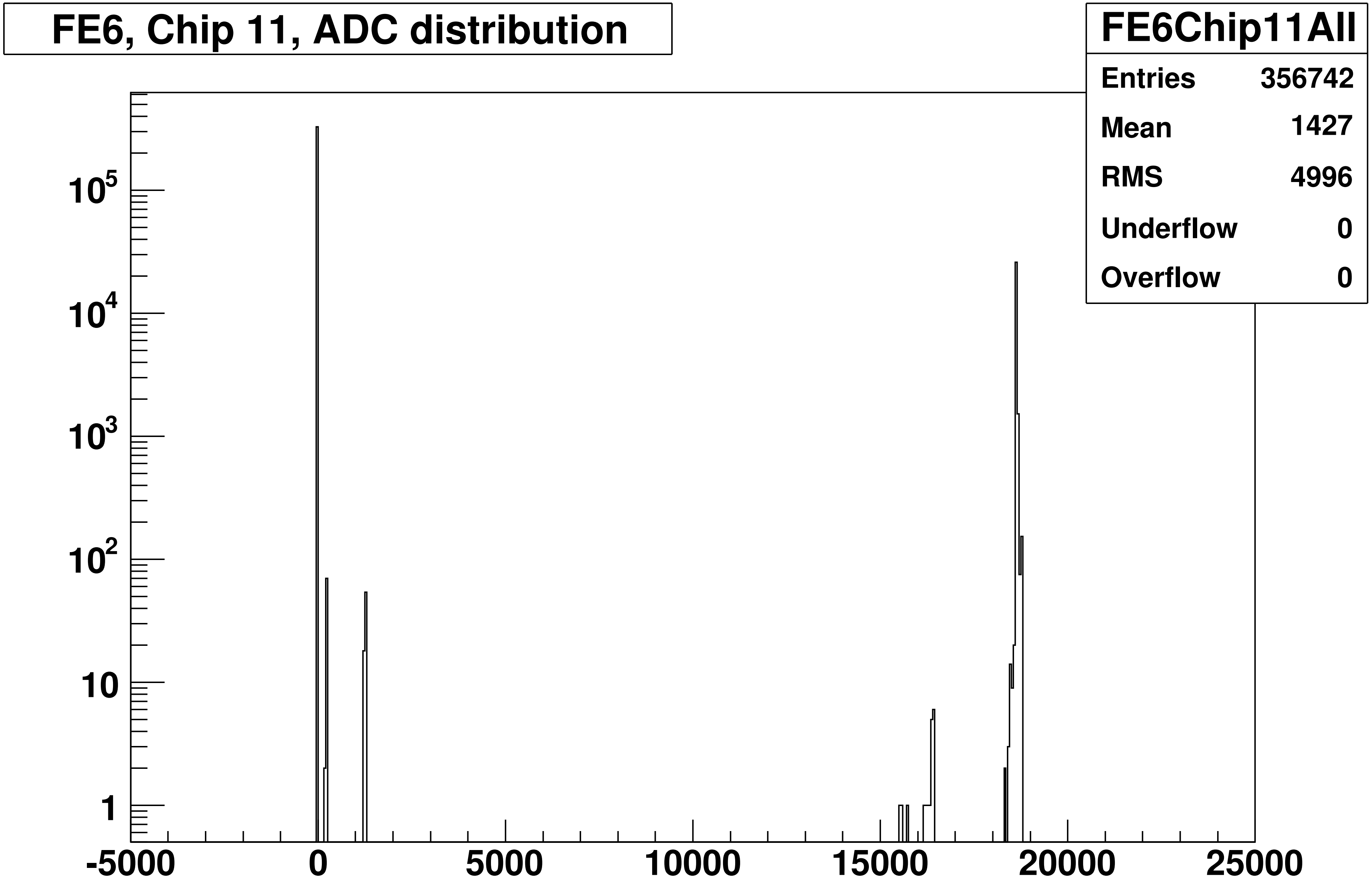
FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 356742
Mean 1.861e+04
RMS 29.51
Underflow 3.294e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

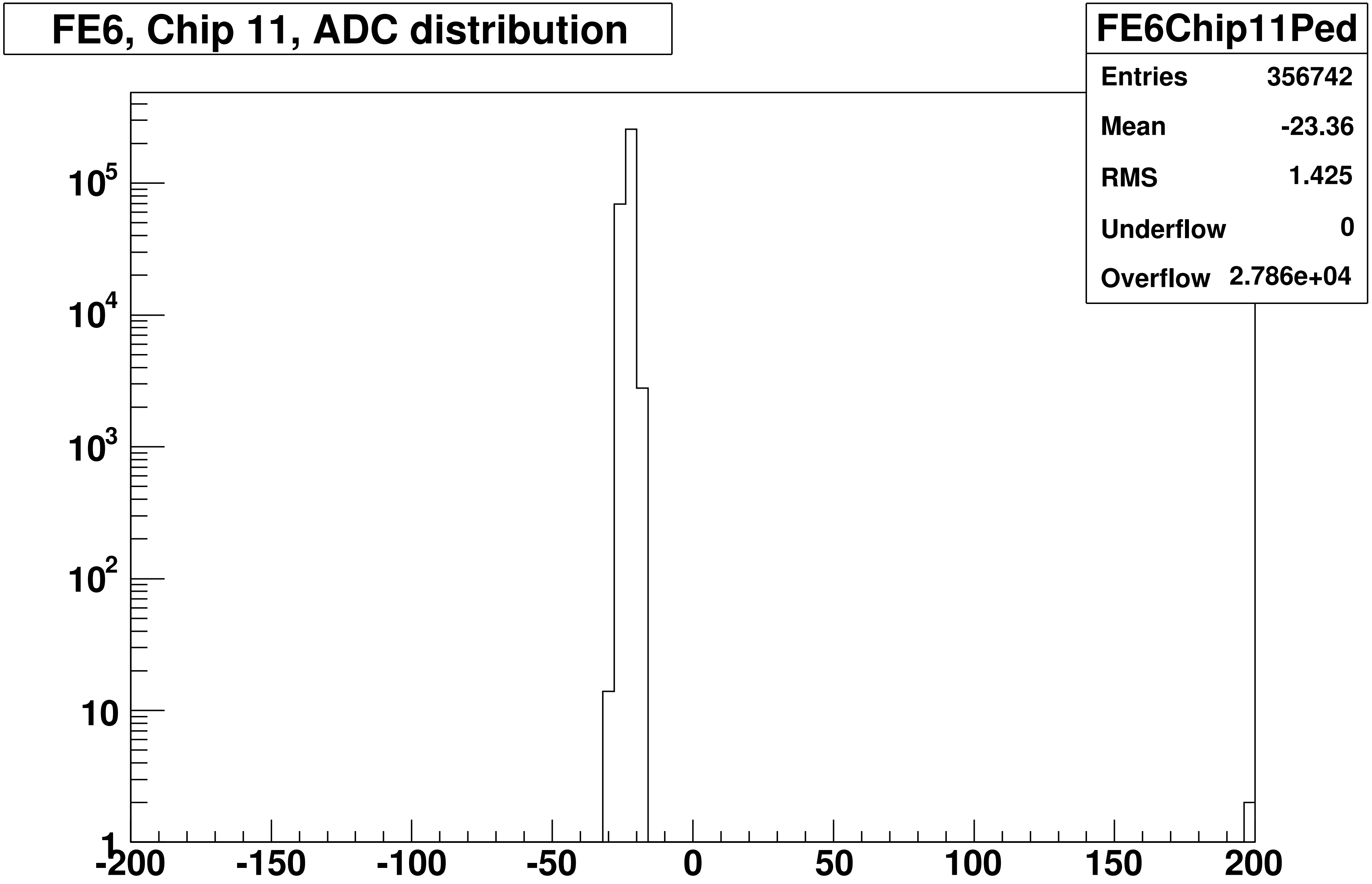

FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 356742
Mean 1419
RMS 4906
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 356742
Mean 12.95
RMS 1.329
Underflow 18
Overflow 2.749e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 356742
Mean 1.856e+04
RMS 8.341
Underflow 3.298e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 356742
Mean 1427
RMS 4996
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 356742
Mean -23.36
RMS 1.425
Underflow 0
Overflow 2.786e+04
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10^4
10^3
10^2
10
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-100
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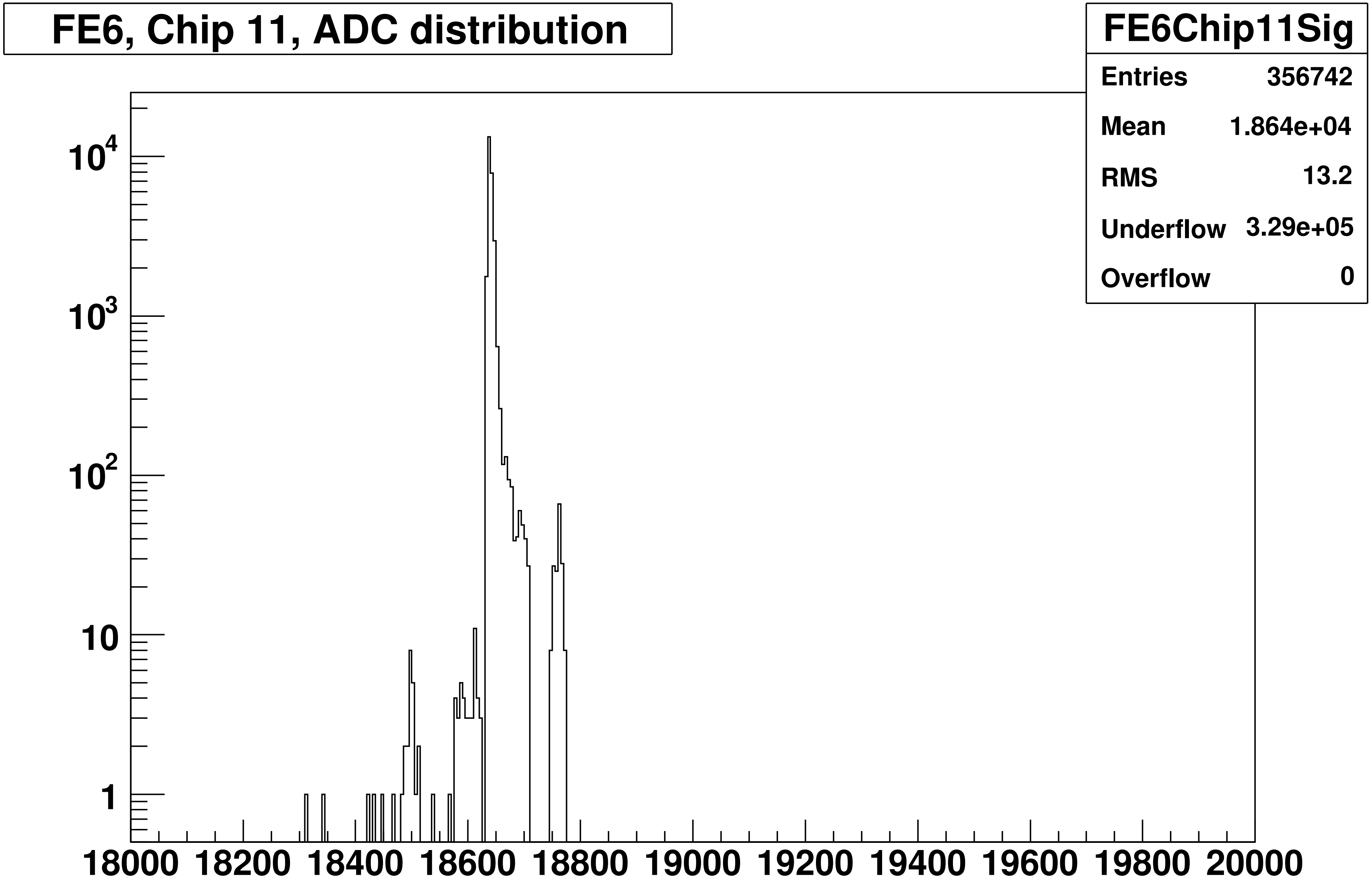
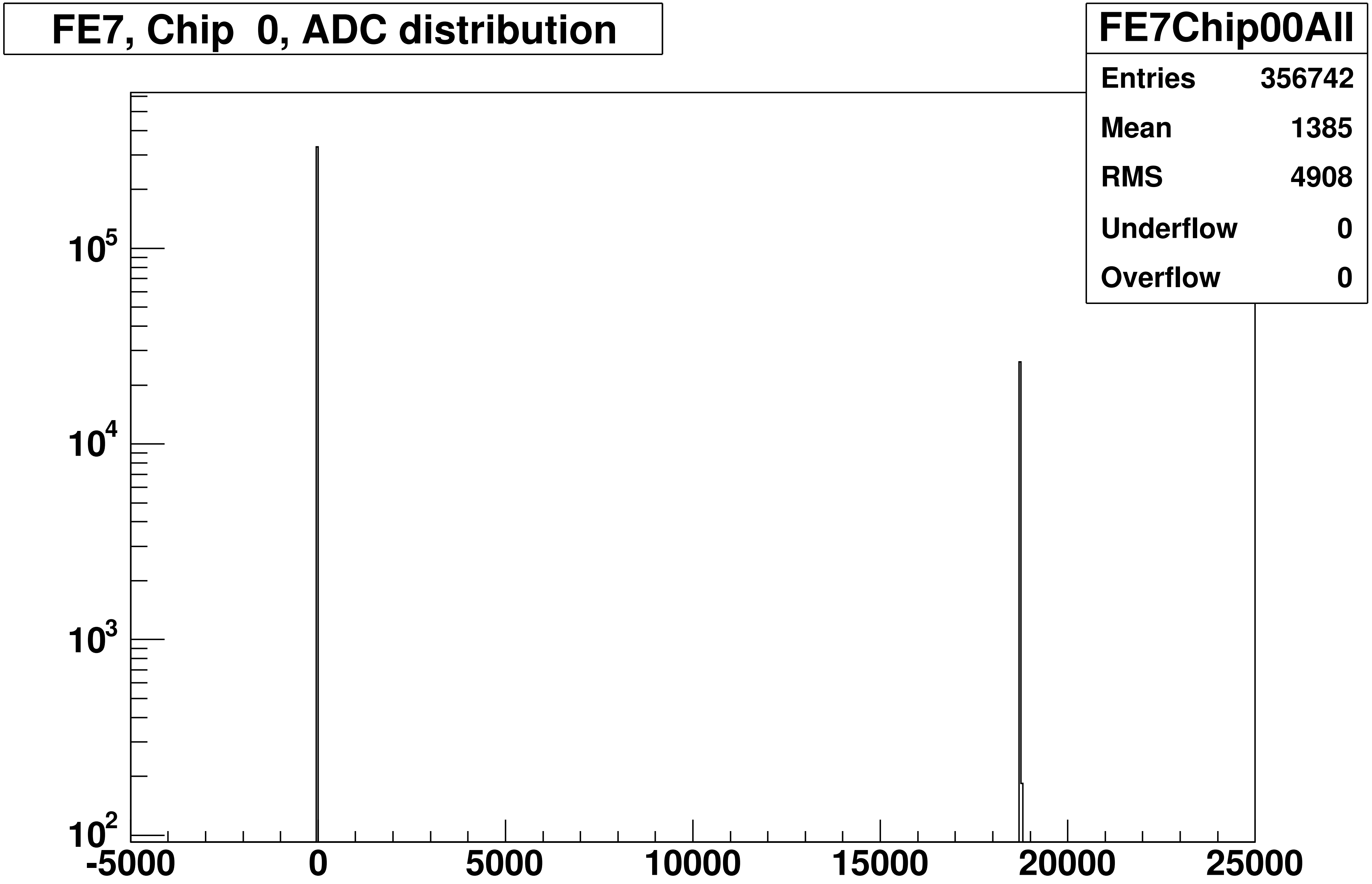
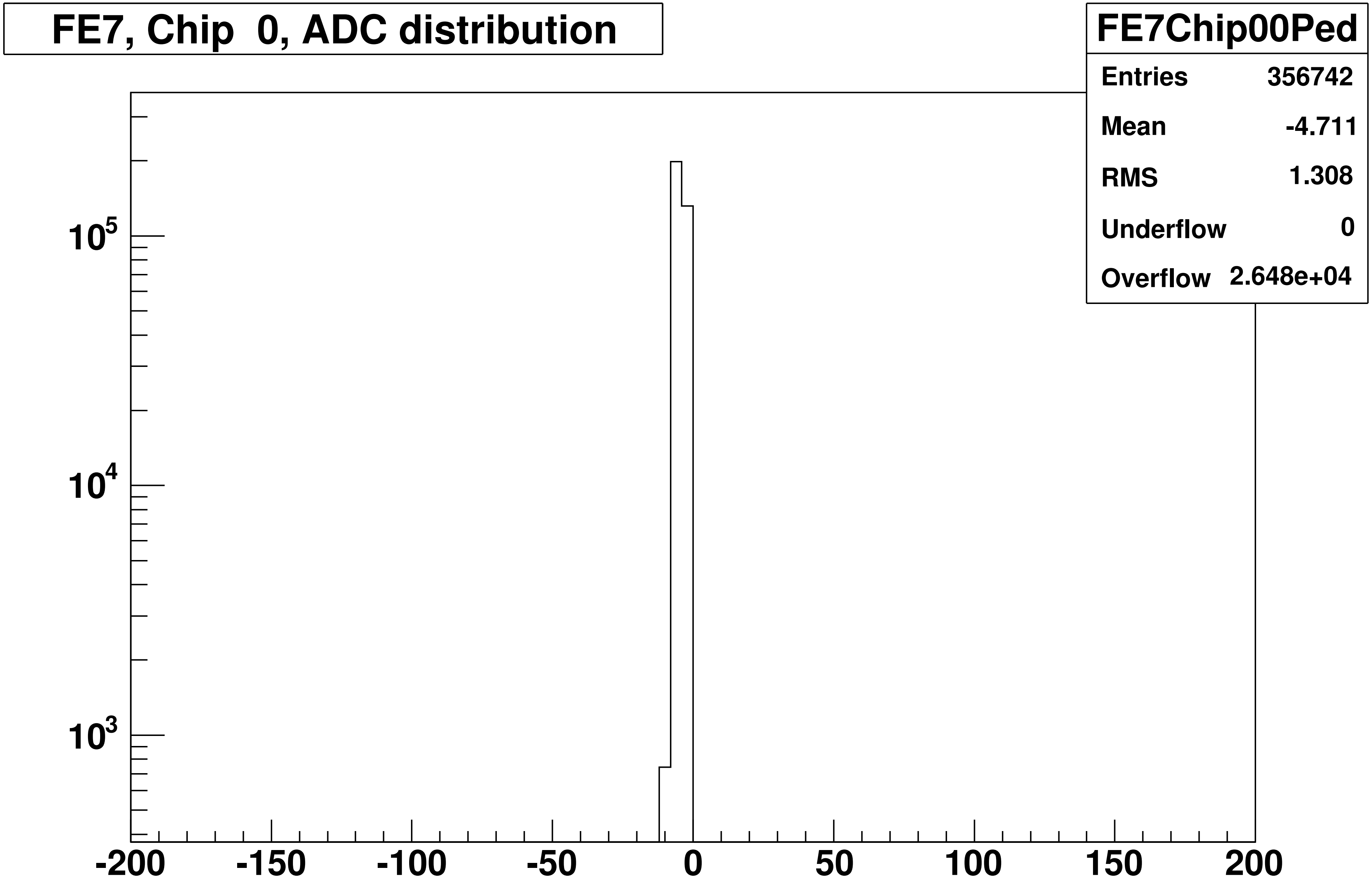
0
50
100
150
200


FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 356742
Mean 1.864e+04
RMS 13.2
Underflow 3.29e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 356742
Mean 1385
RMS 4908
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 356742
Mean -4.711
RMS 1.308
Underflow 0
Overflow 2.648e+04
10^5
10^4
10^3
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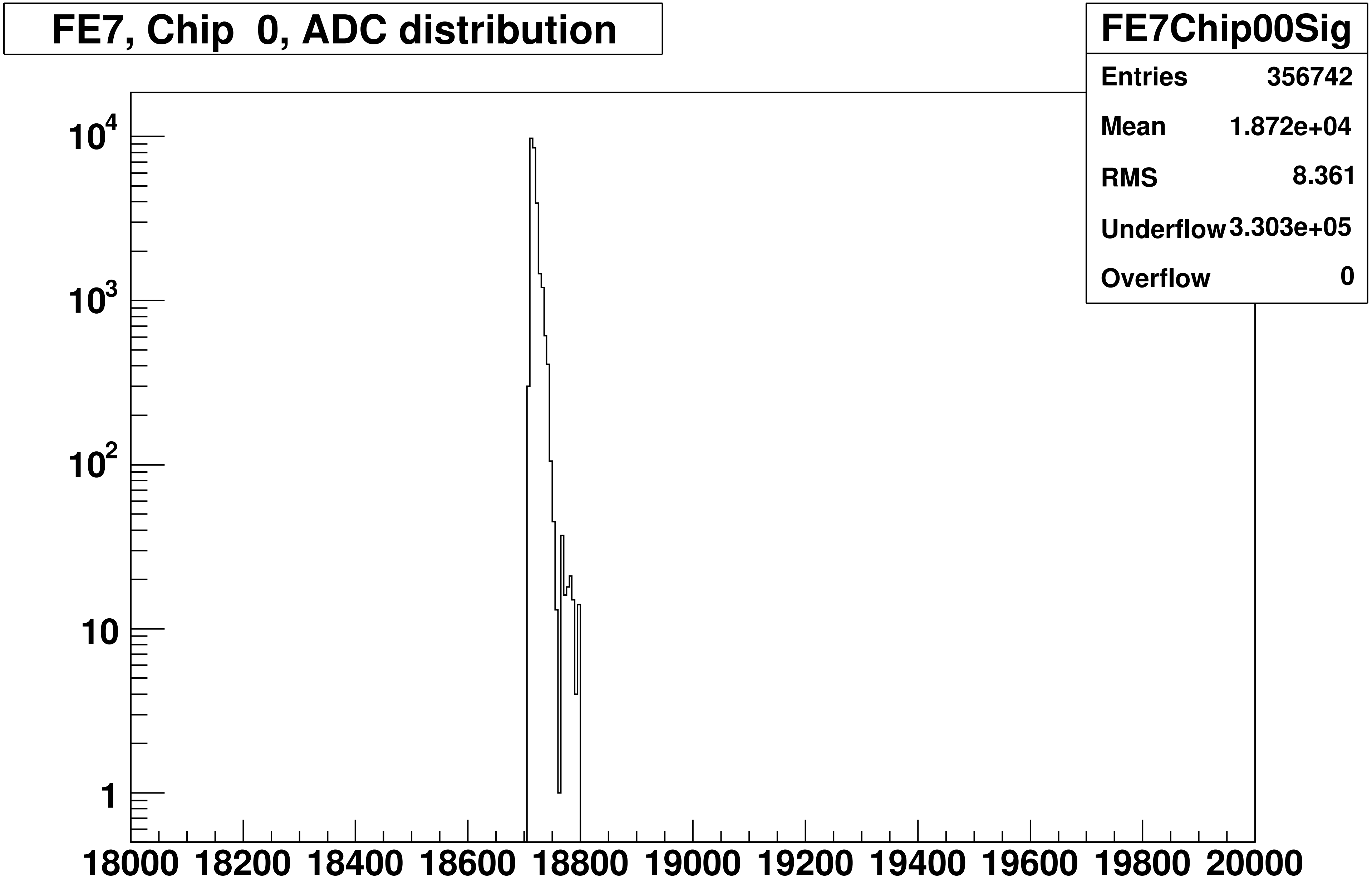
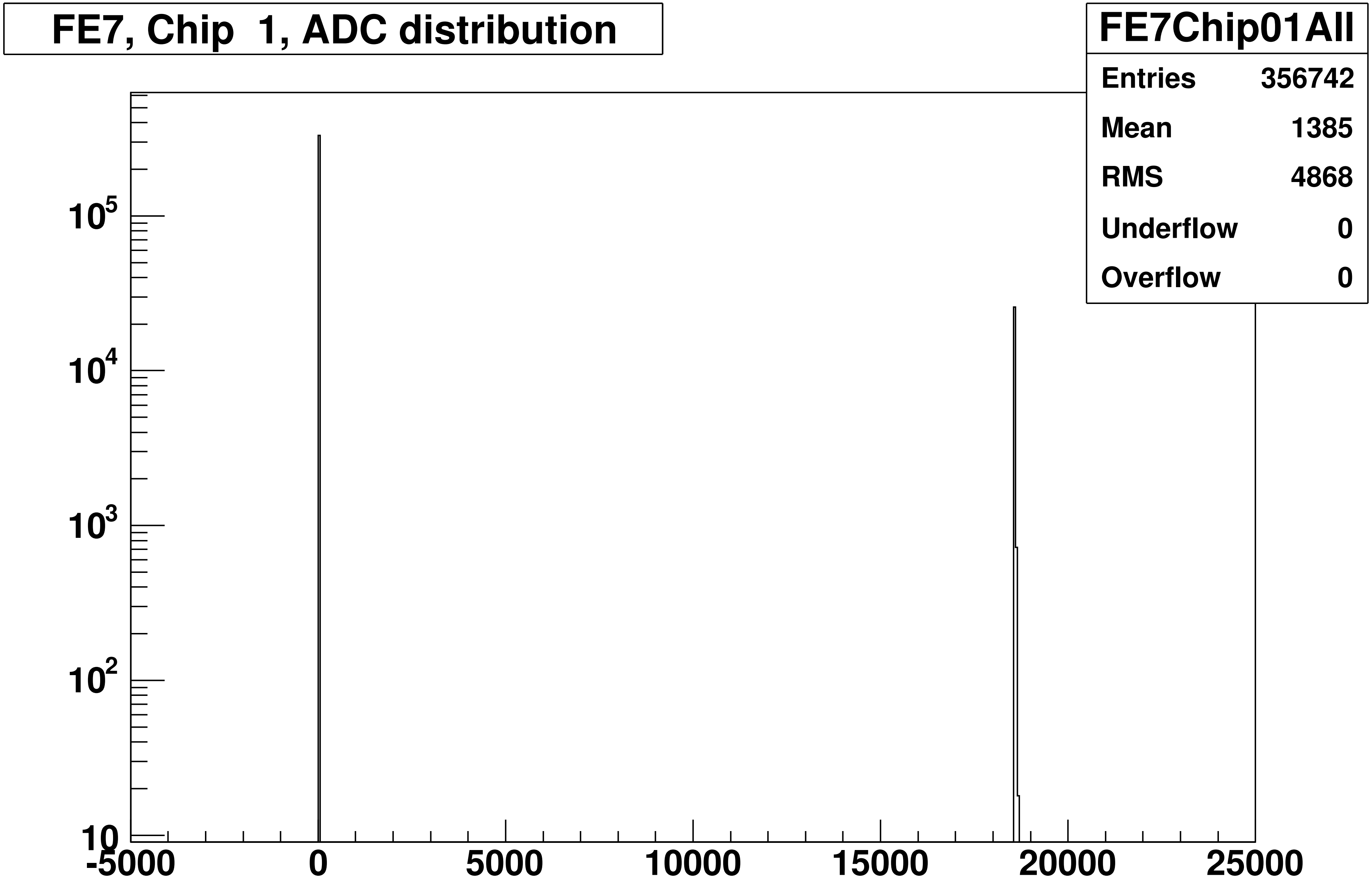
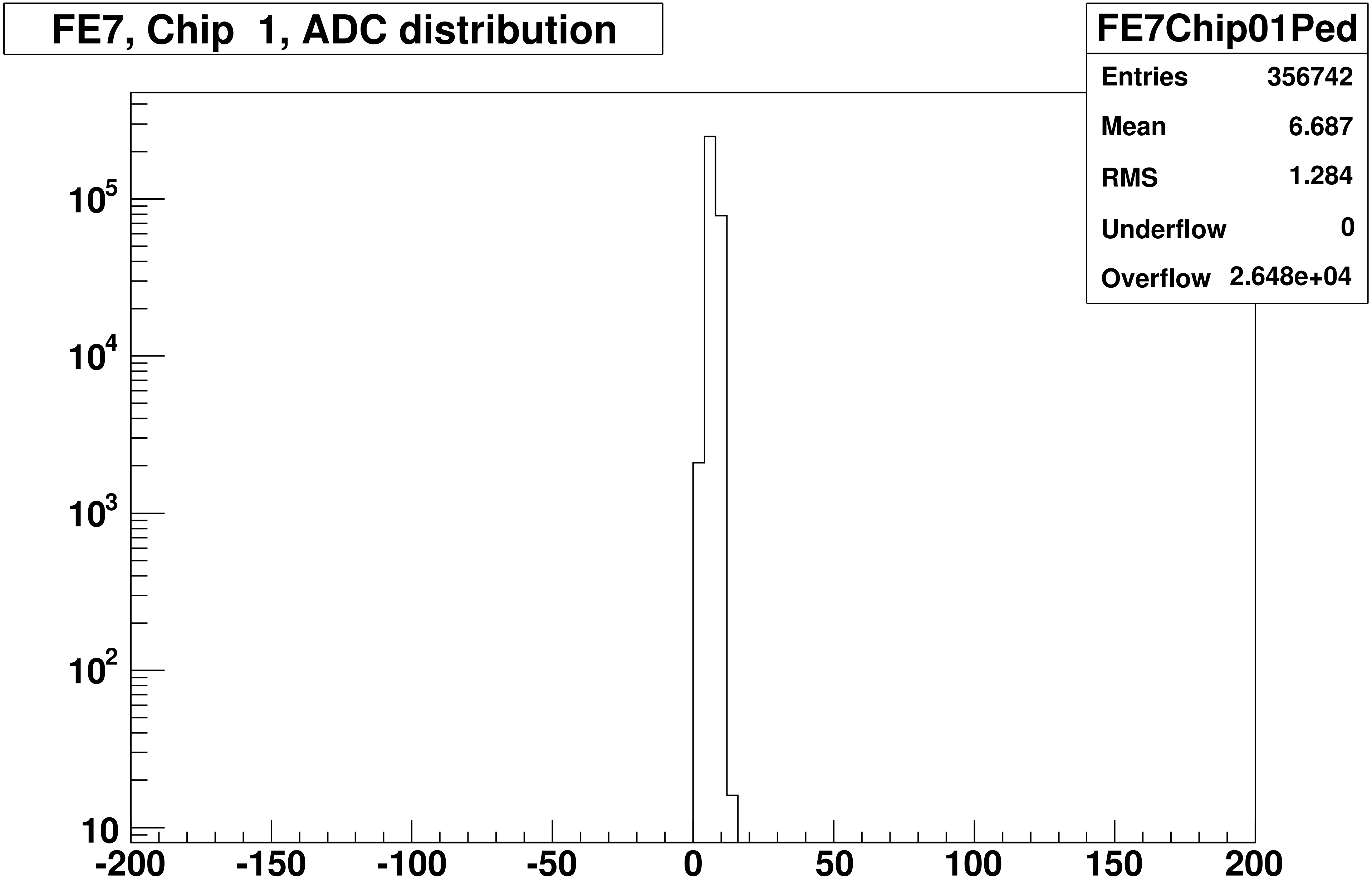
-150
-100
-50
0
50
100
150
200



FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 356742
Mean 1.872e+04
RMS 8.361
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 356742
Mean 1385
RMS 4868
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 356742
Mean 6.687
RMS 1.284
Underflow 0
Overflow 2.648e+04
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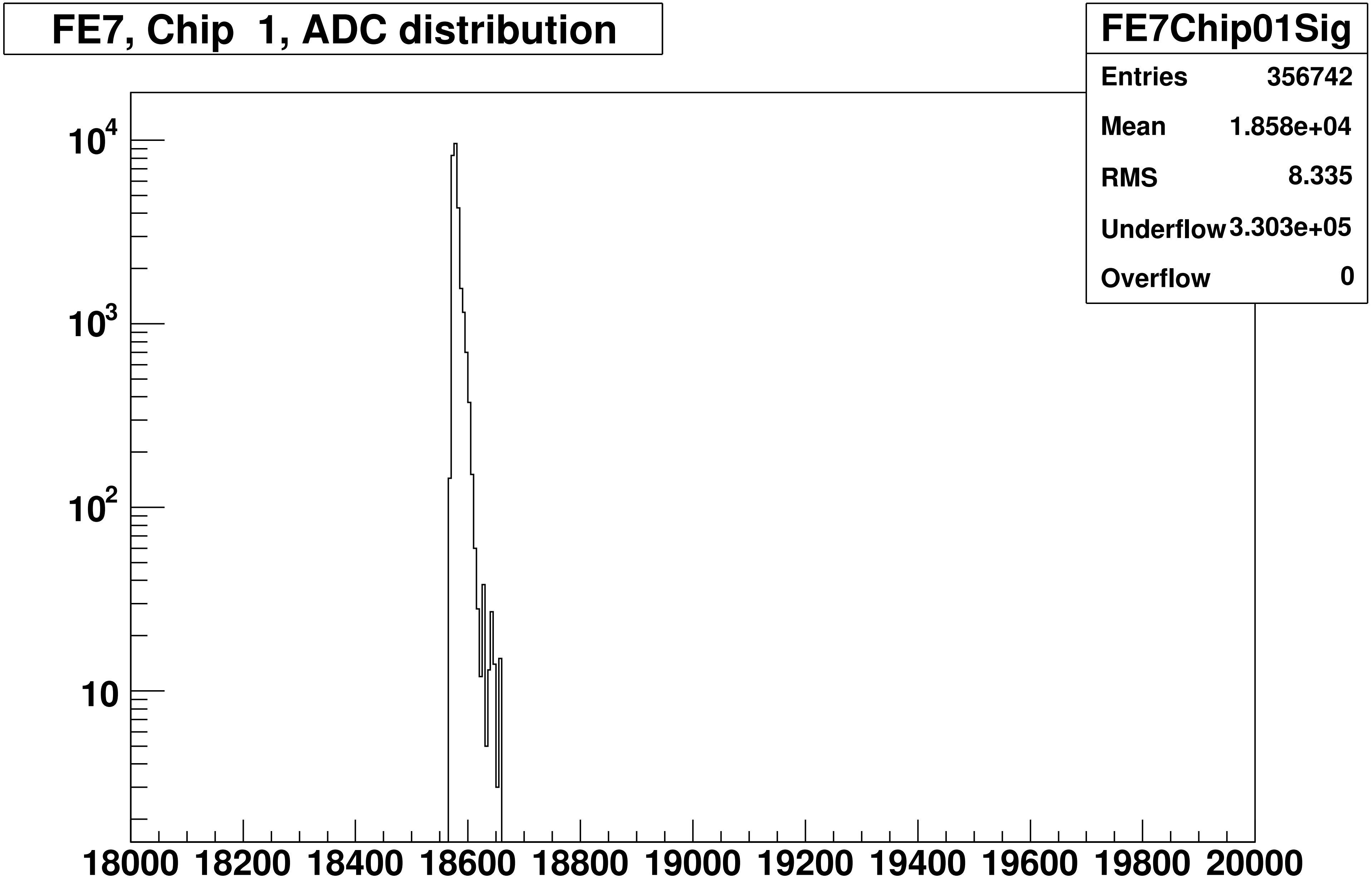
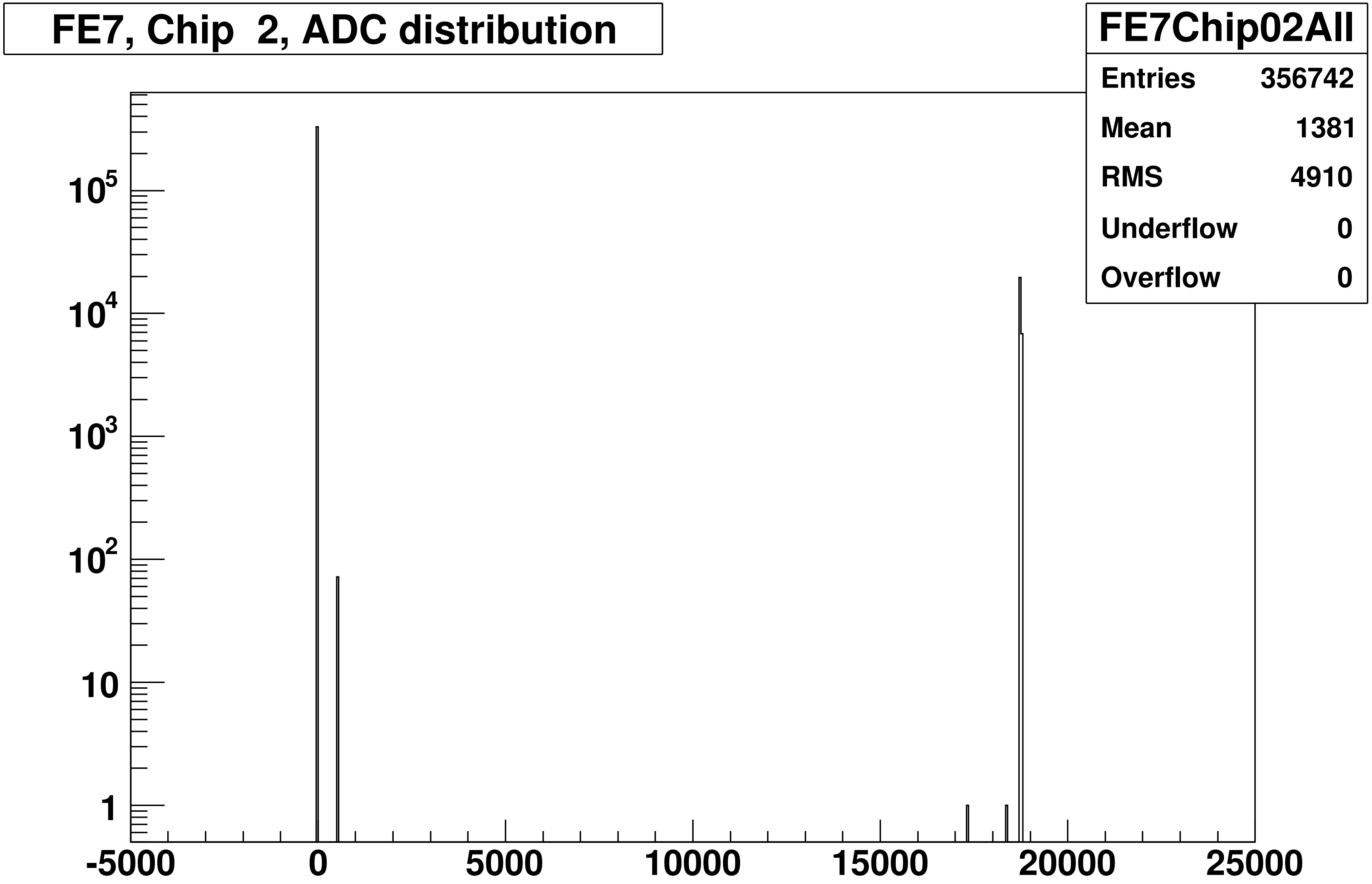
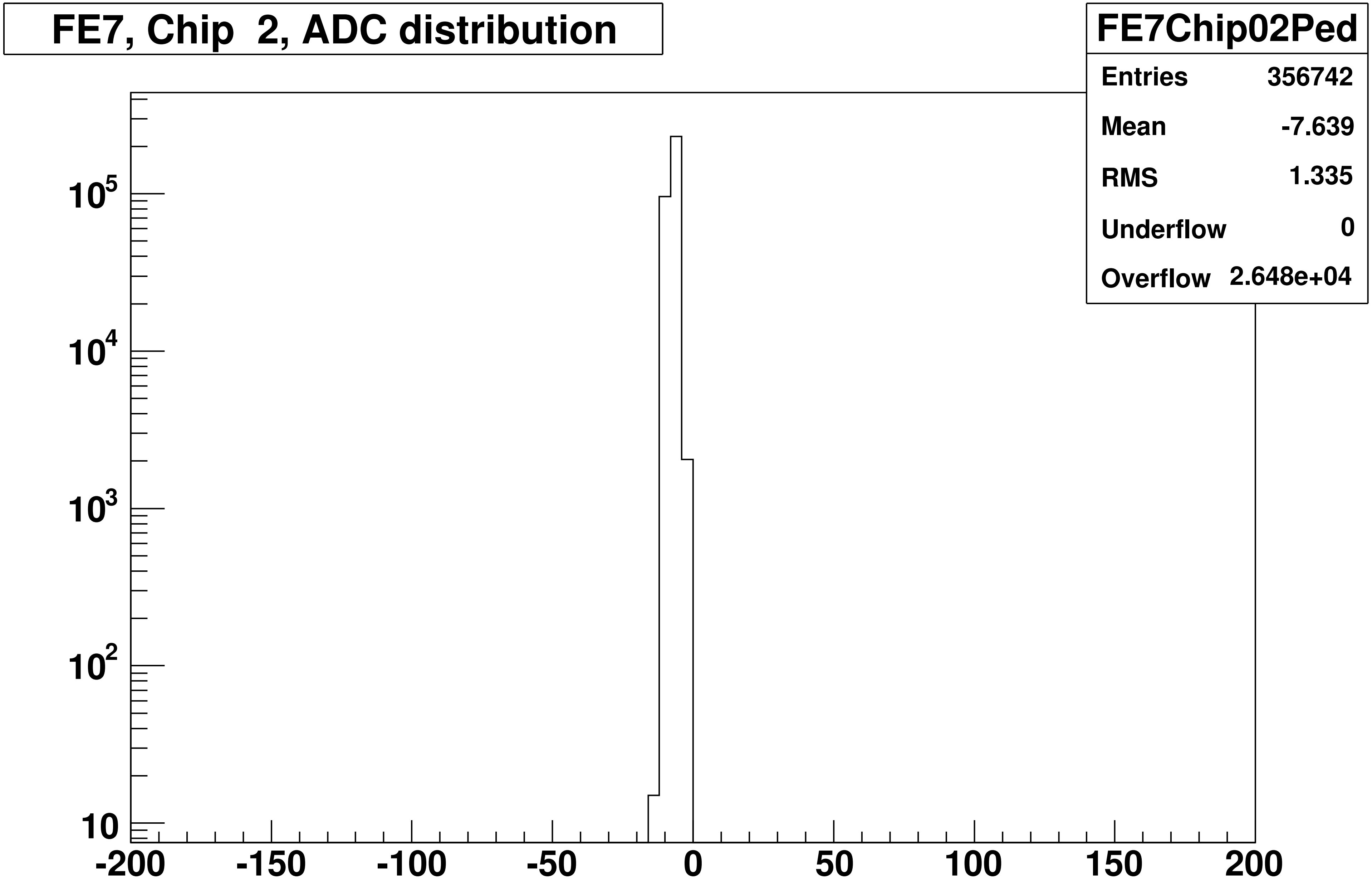
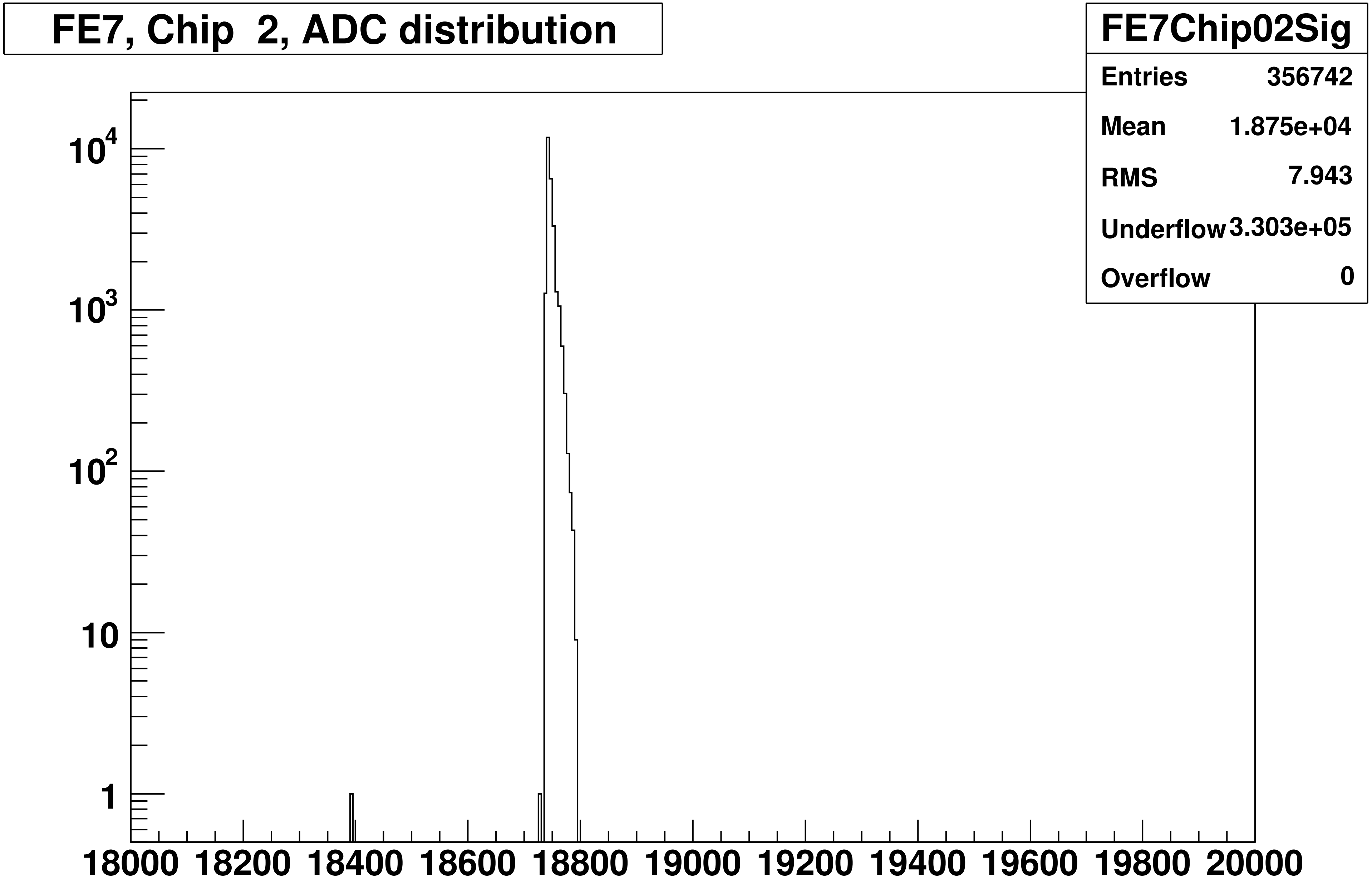
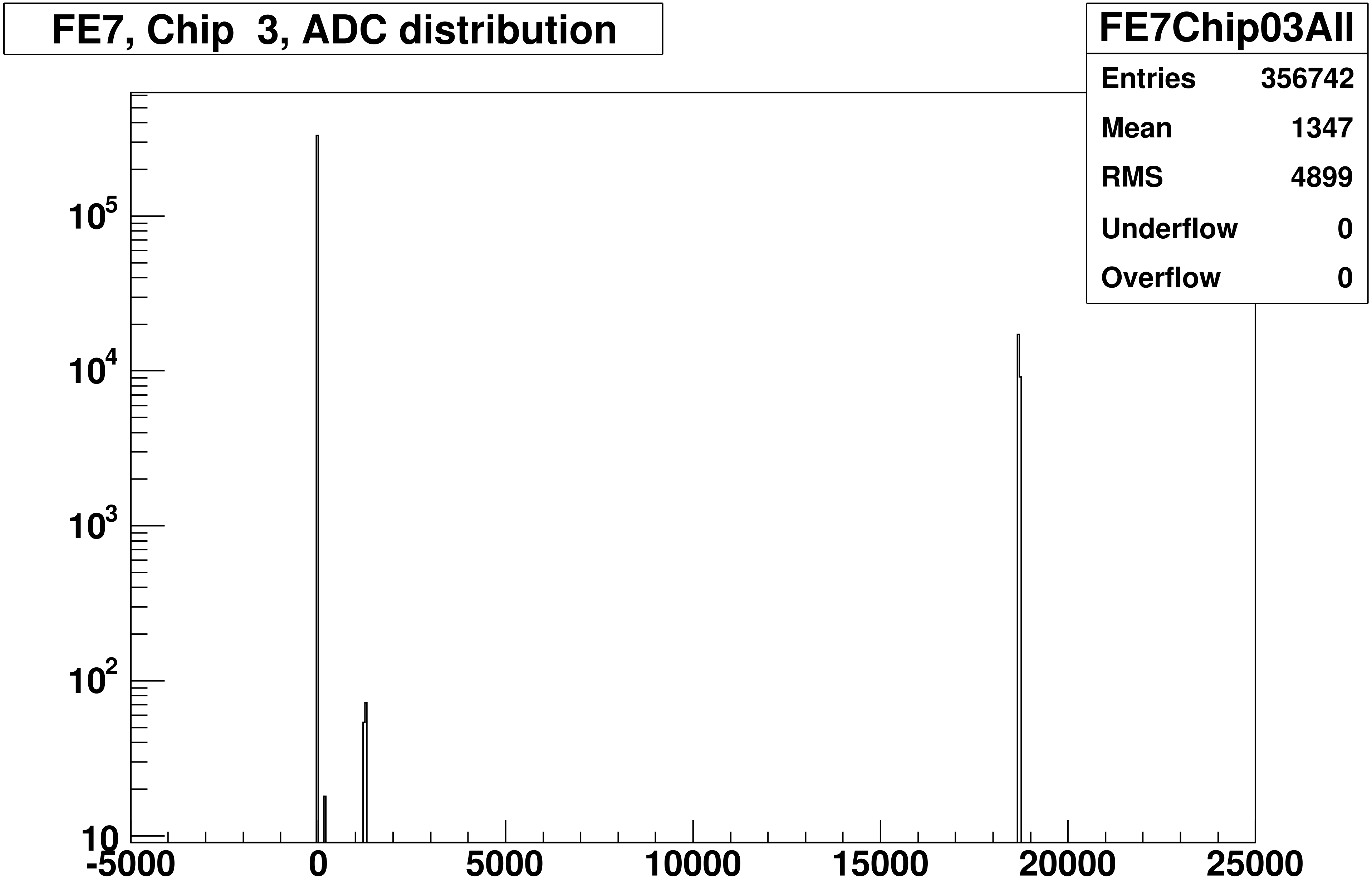
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 356742
Mean 1.858e+04
RMS 8.335
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

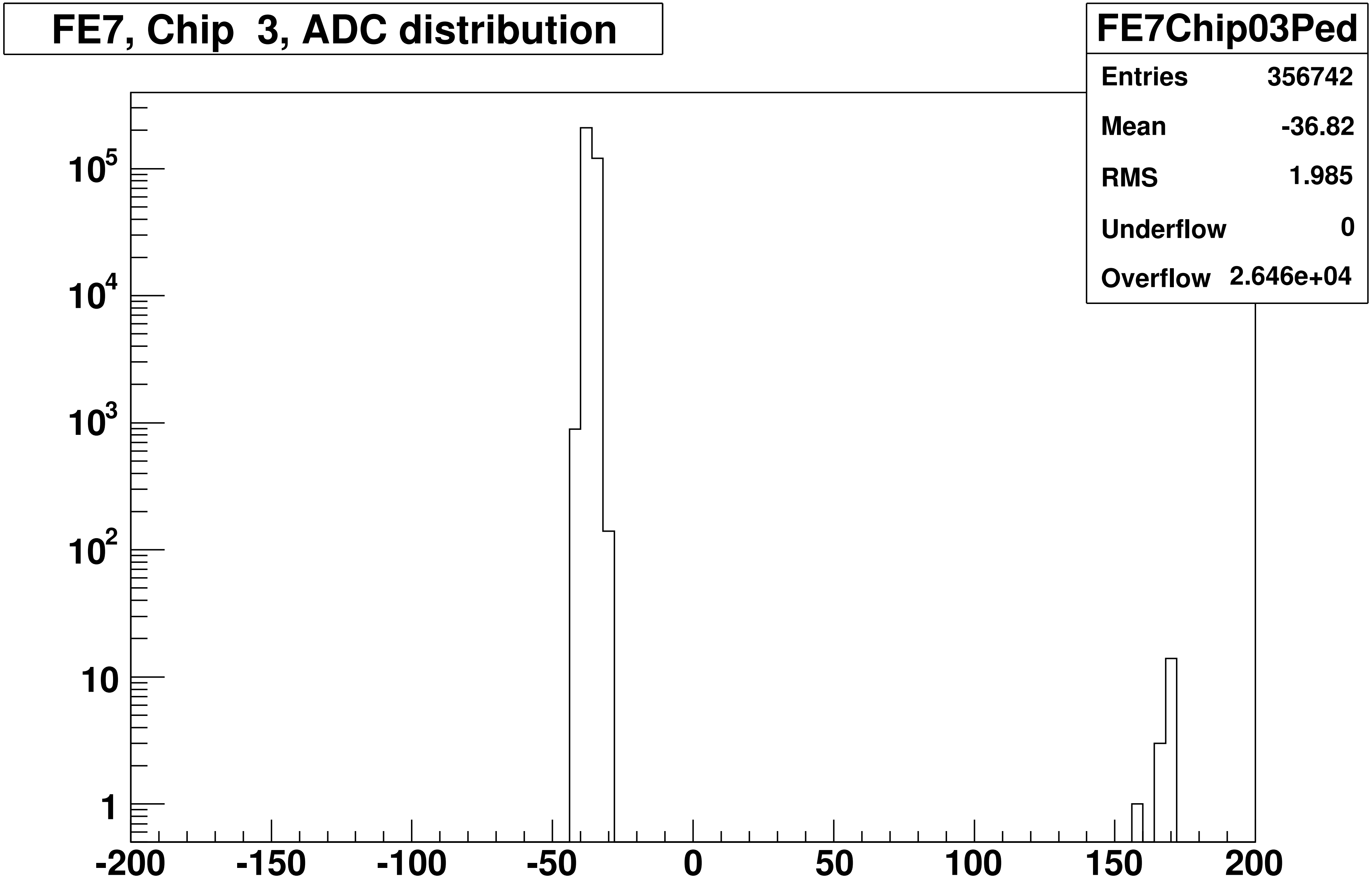

FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 356742
Mean 1381
RMS 4910
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 356742
Mean -7.639
RMS 1.335
Underflow 0
Overflow 2.648e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 356742
Mean 1.875e+04
RMS 7.943
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000



FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 356742
Mean 1347
RMS 4899
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 356742
Mean -36.82
RMS 1.985
Underflow 0
Overflow 2.646e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
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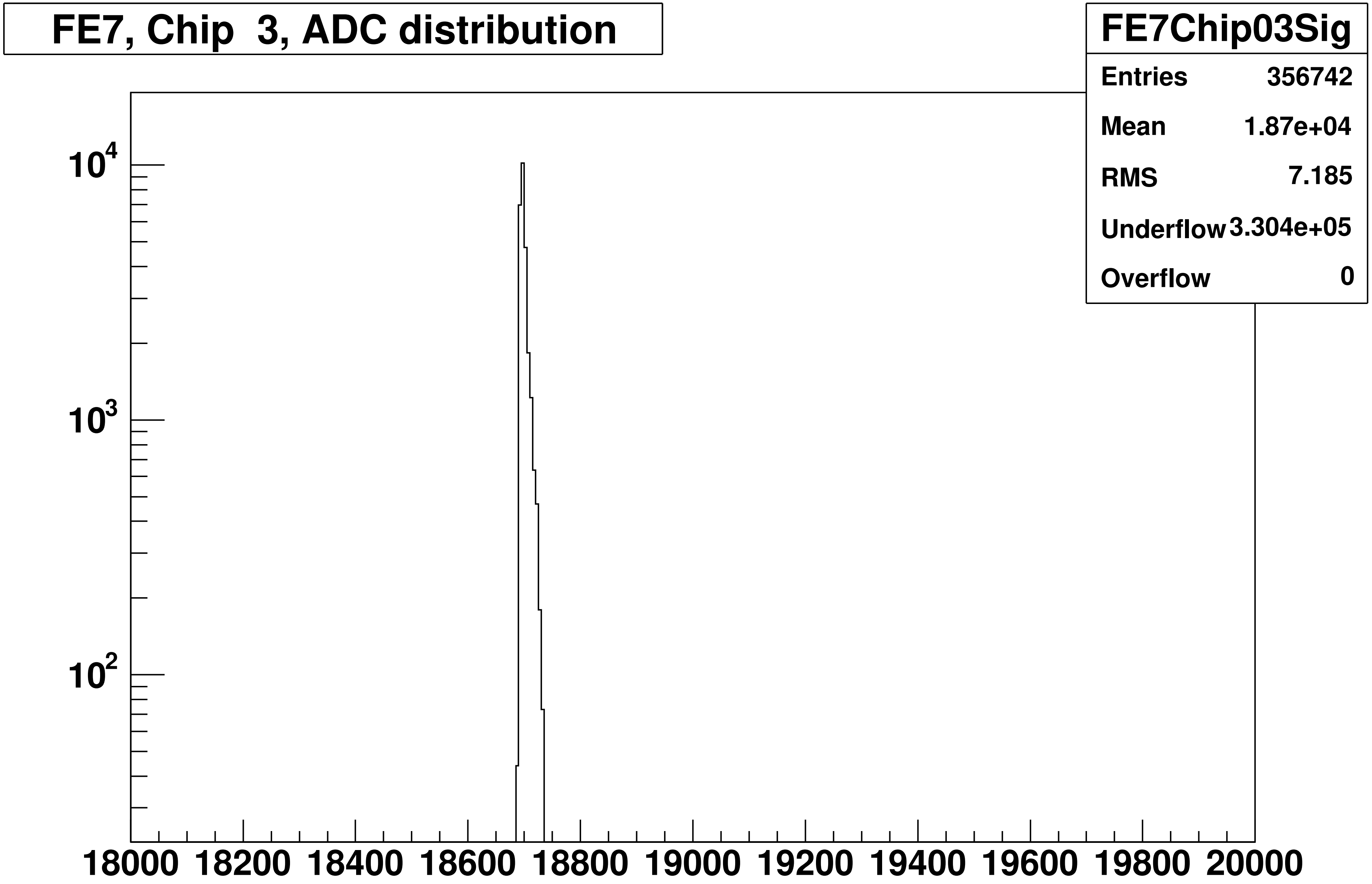
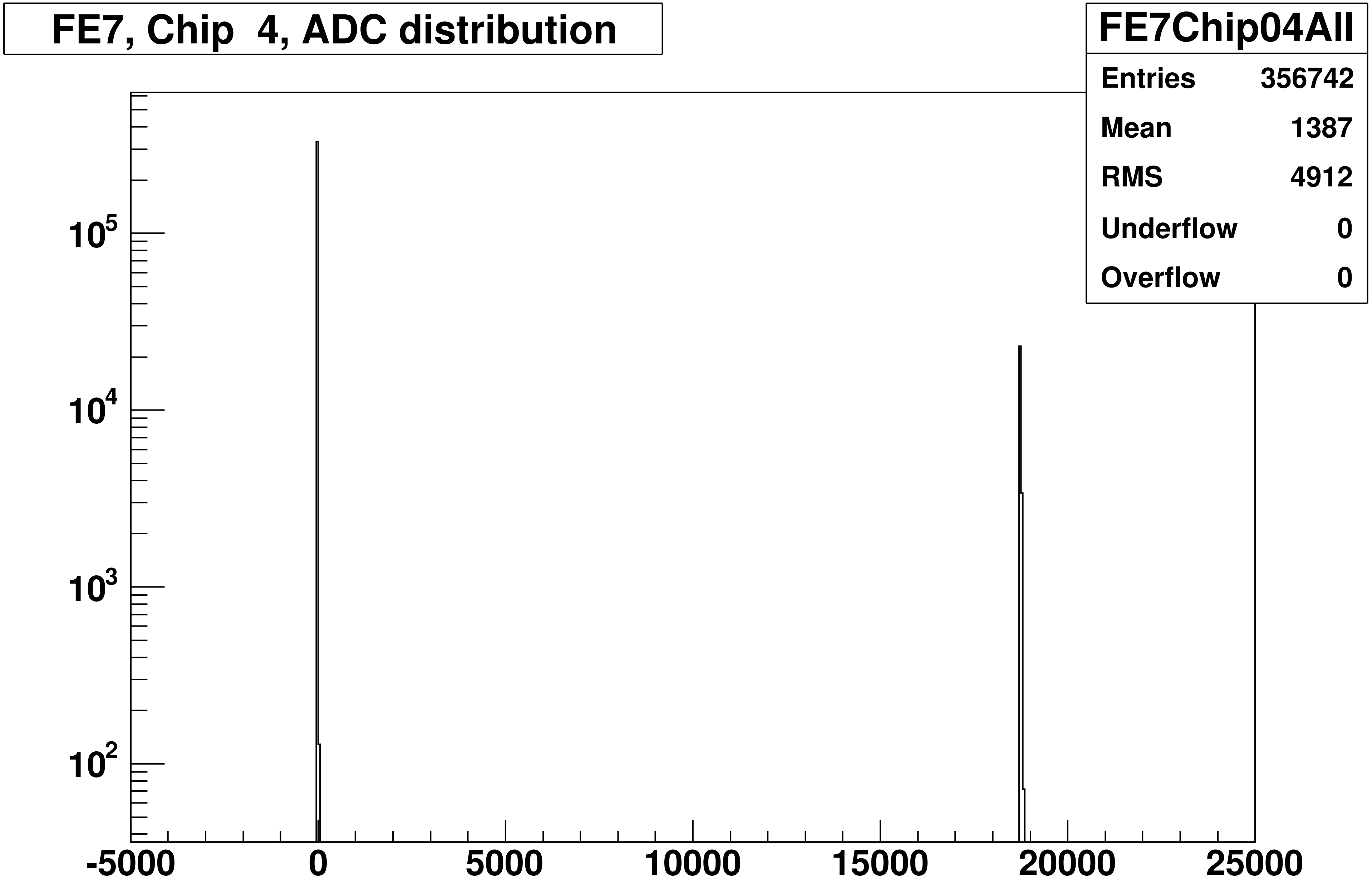
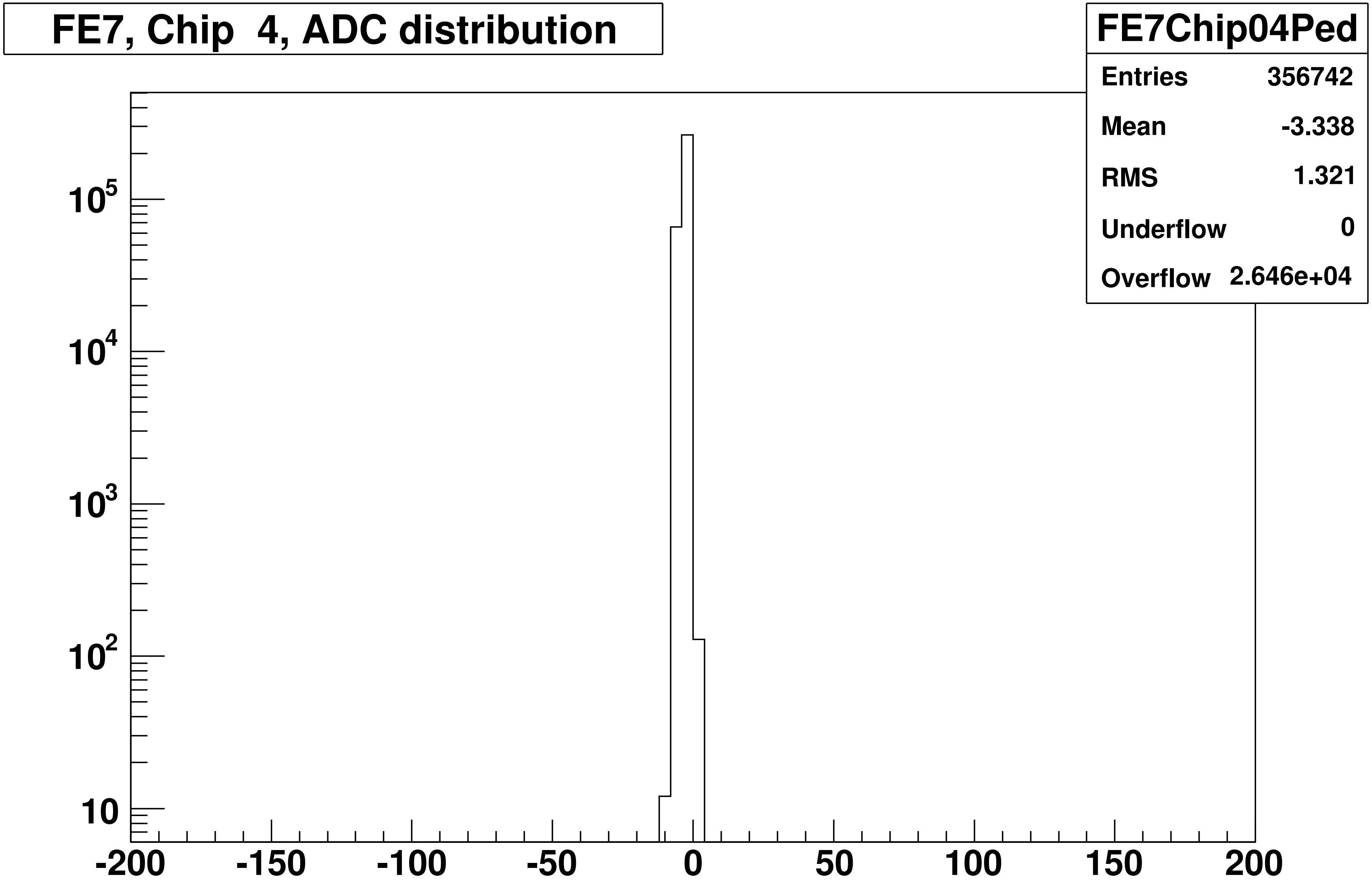
0
50
100
150
200



FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 356742
Mean 1.87e+04
RMS 7.185
Underflow 3.304e+05
Overflow 0
10^4
10^3
10^2
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000



FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 356742
Mean 1387
RMS 4912
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 356742
Mean -3.338
RMS 1.321
Underflow 0
Overflow 2.646e+04
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10^4
10^3
10^2
10
-200
-150
-100
-50
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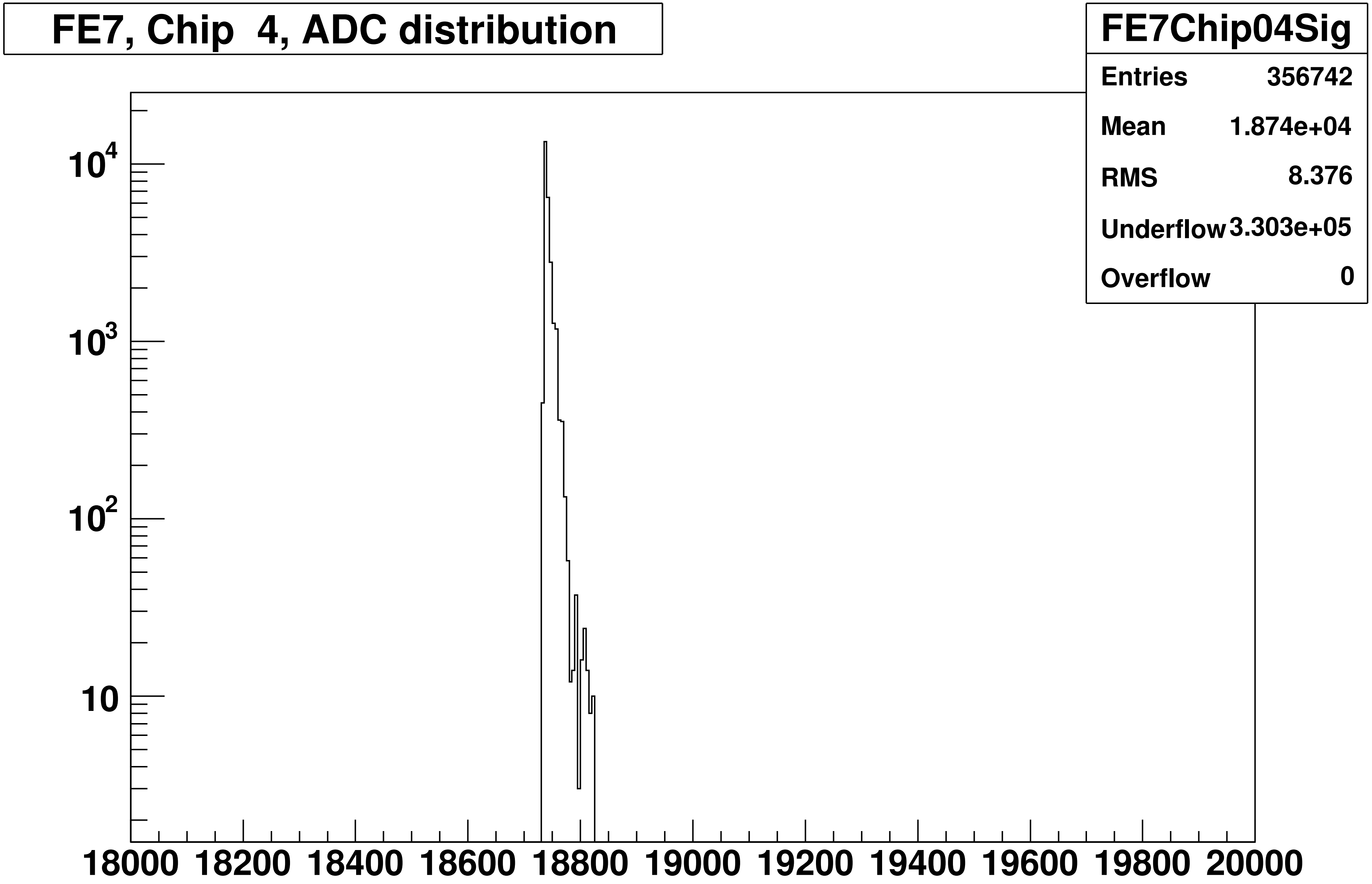
100
150
200


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 356742
Mean 1.874e+04
RMS 8.376
Underflow 3.303e+05
Overflow 0
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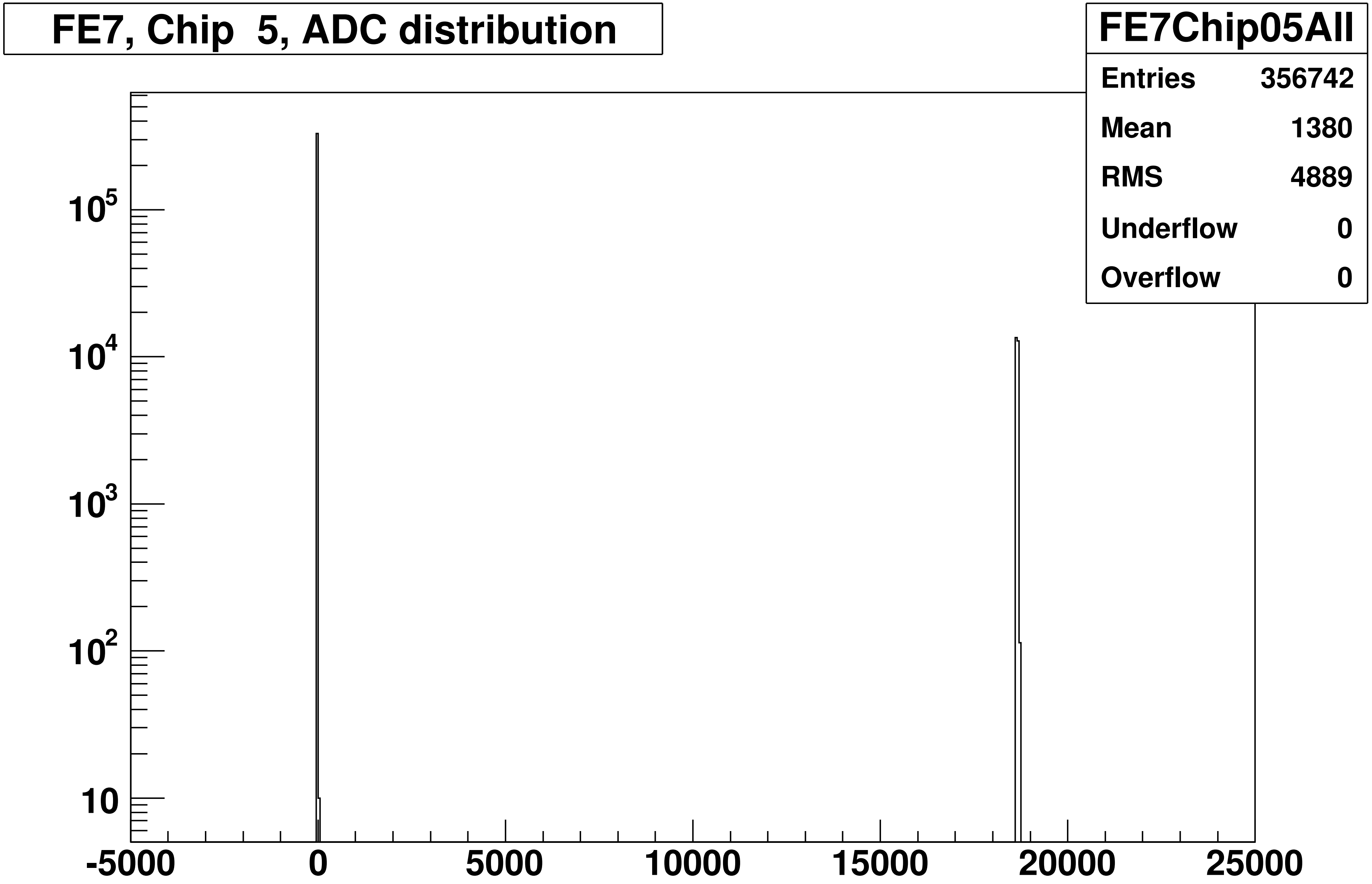
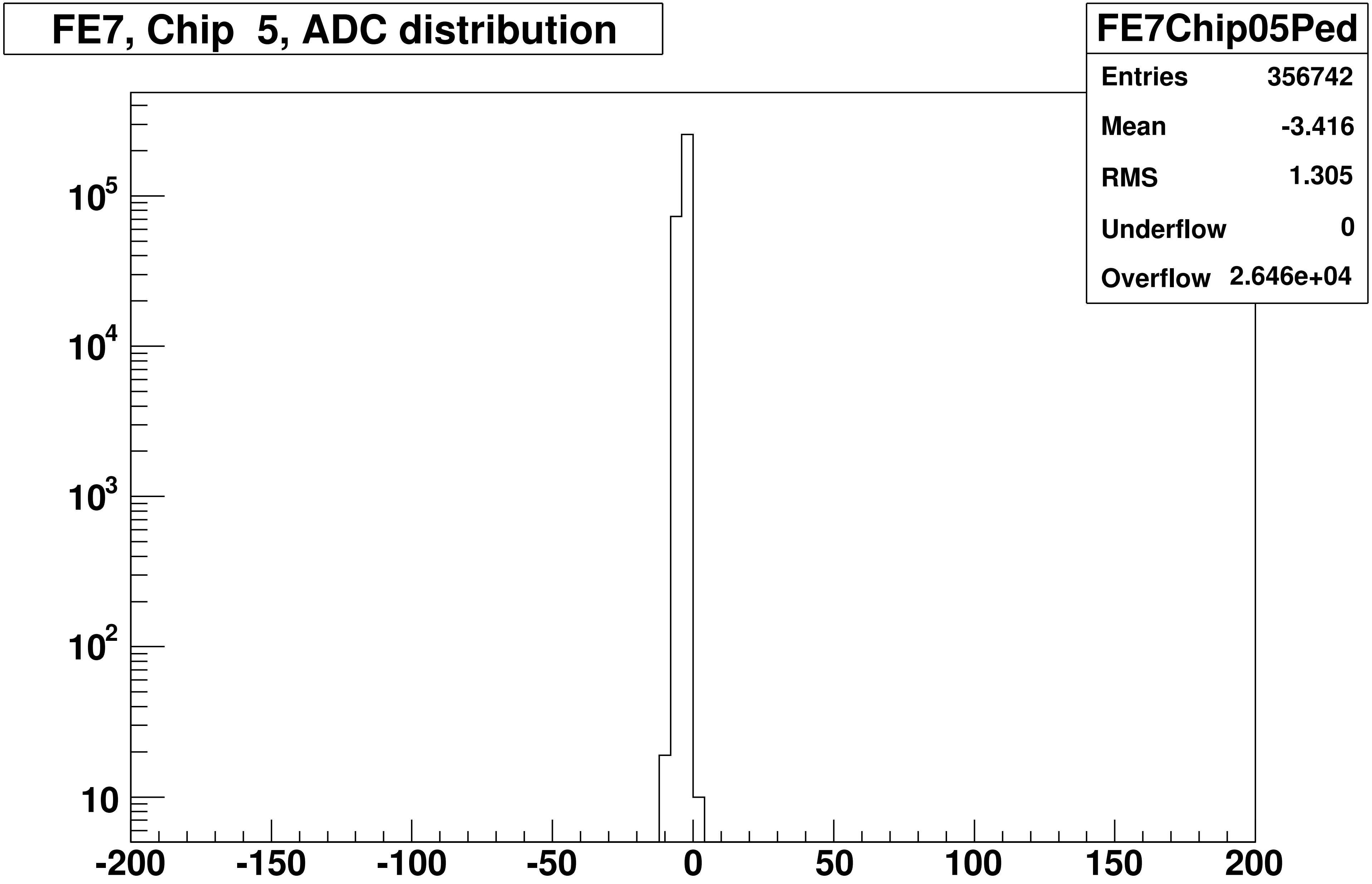
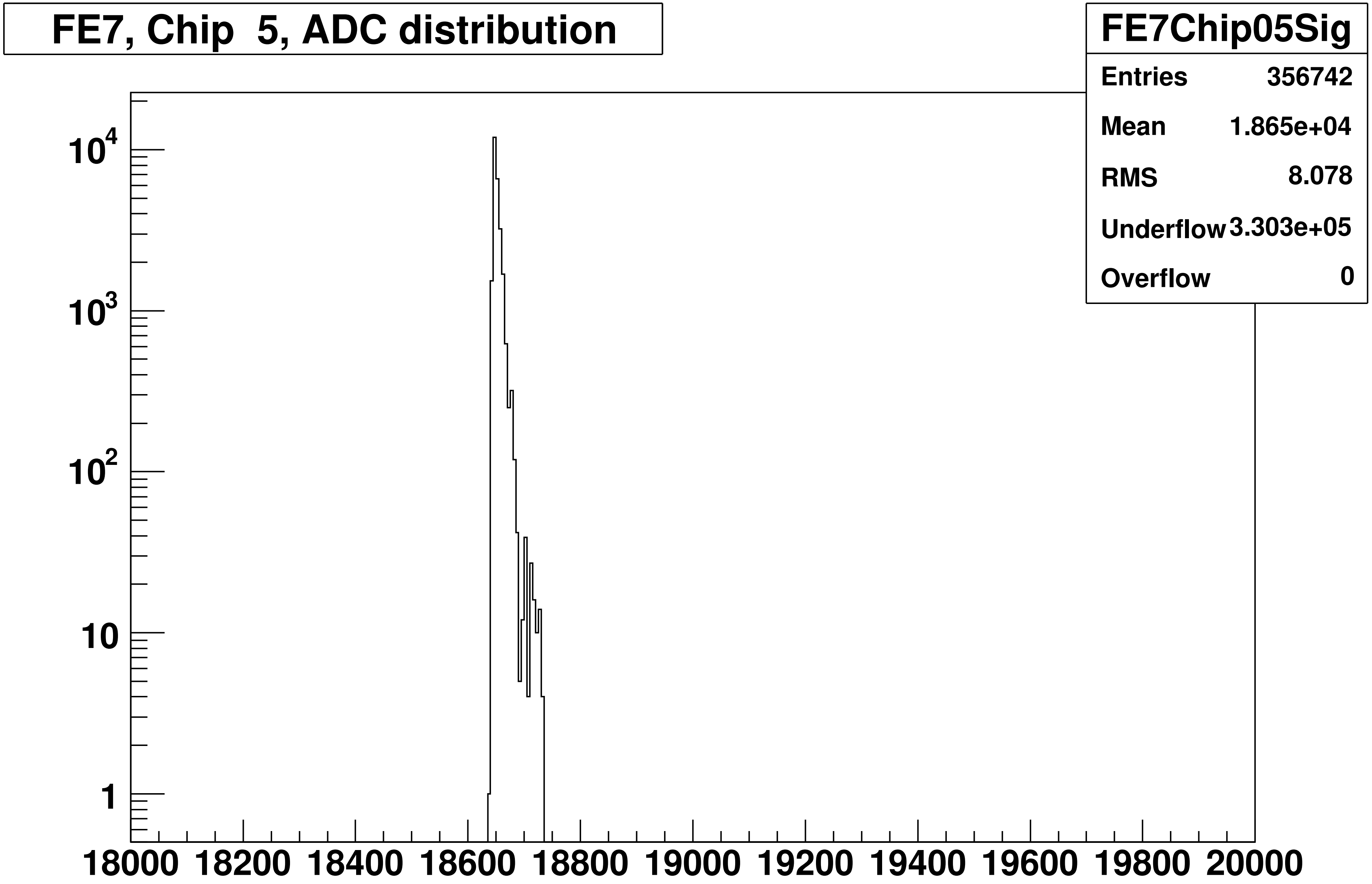
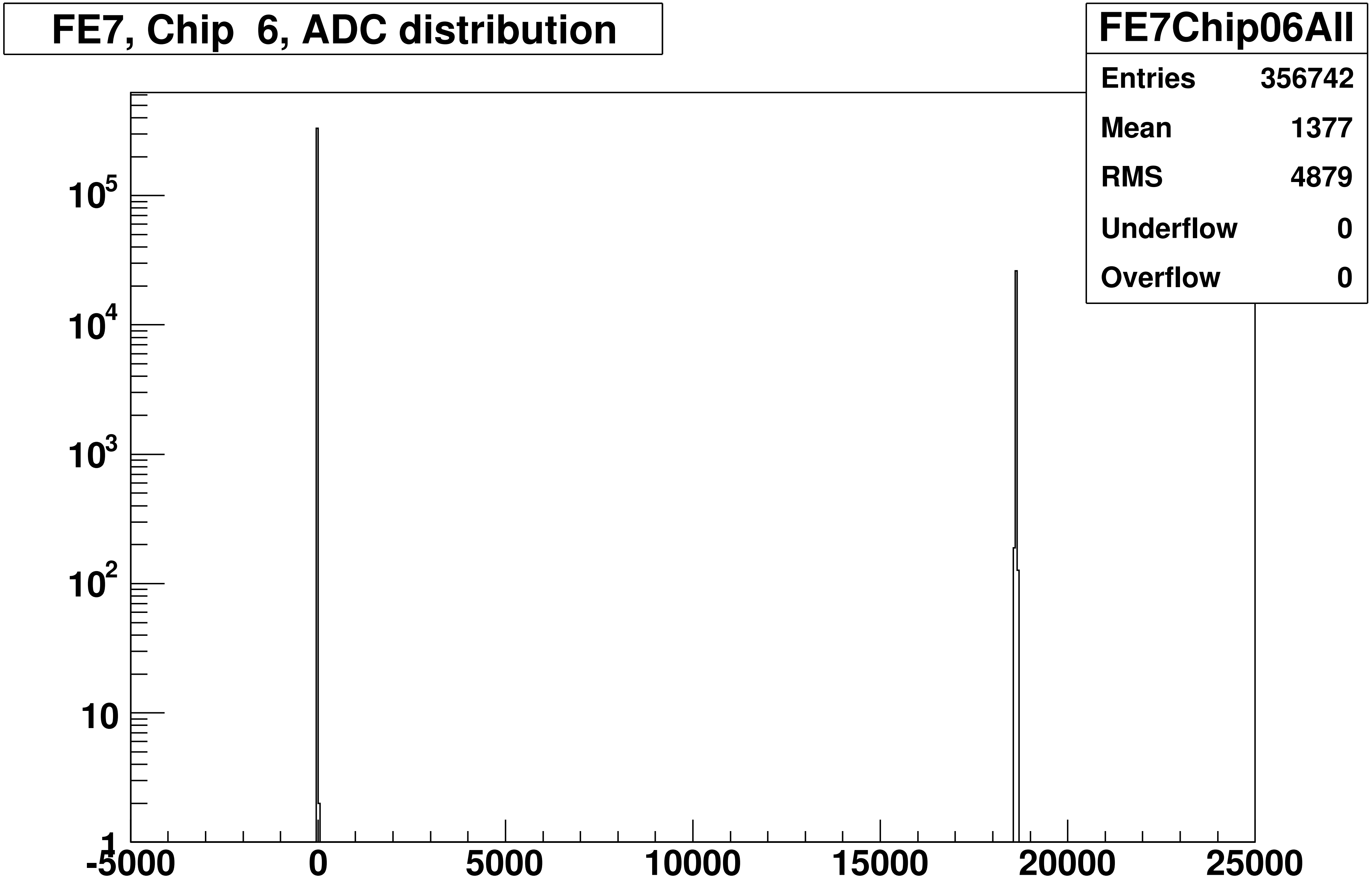
10^3
10^2
10
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 356742
Mean 1380
RMS 4889
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 356742
Mean -3.416
RMS 1.305
Underflow 0
Overflow 2.646e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 356742
Mean 1.865e+04
RMS 8.078
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000


FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 356742
Mean 1377
RMS 4879
Underflow 0
Overflow 0
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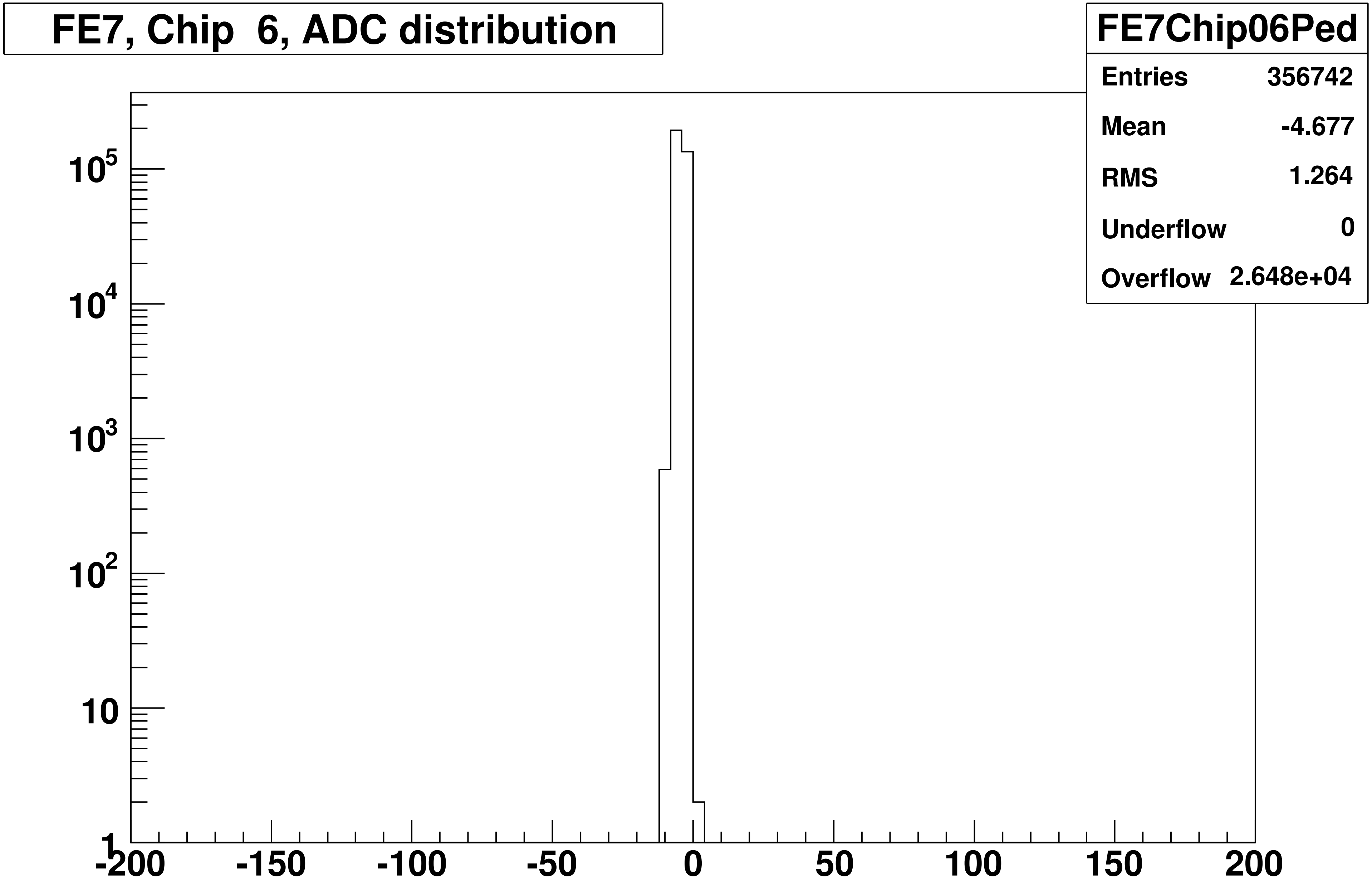
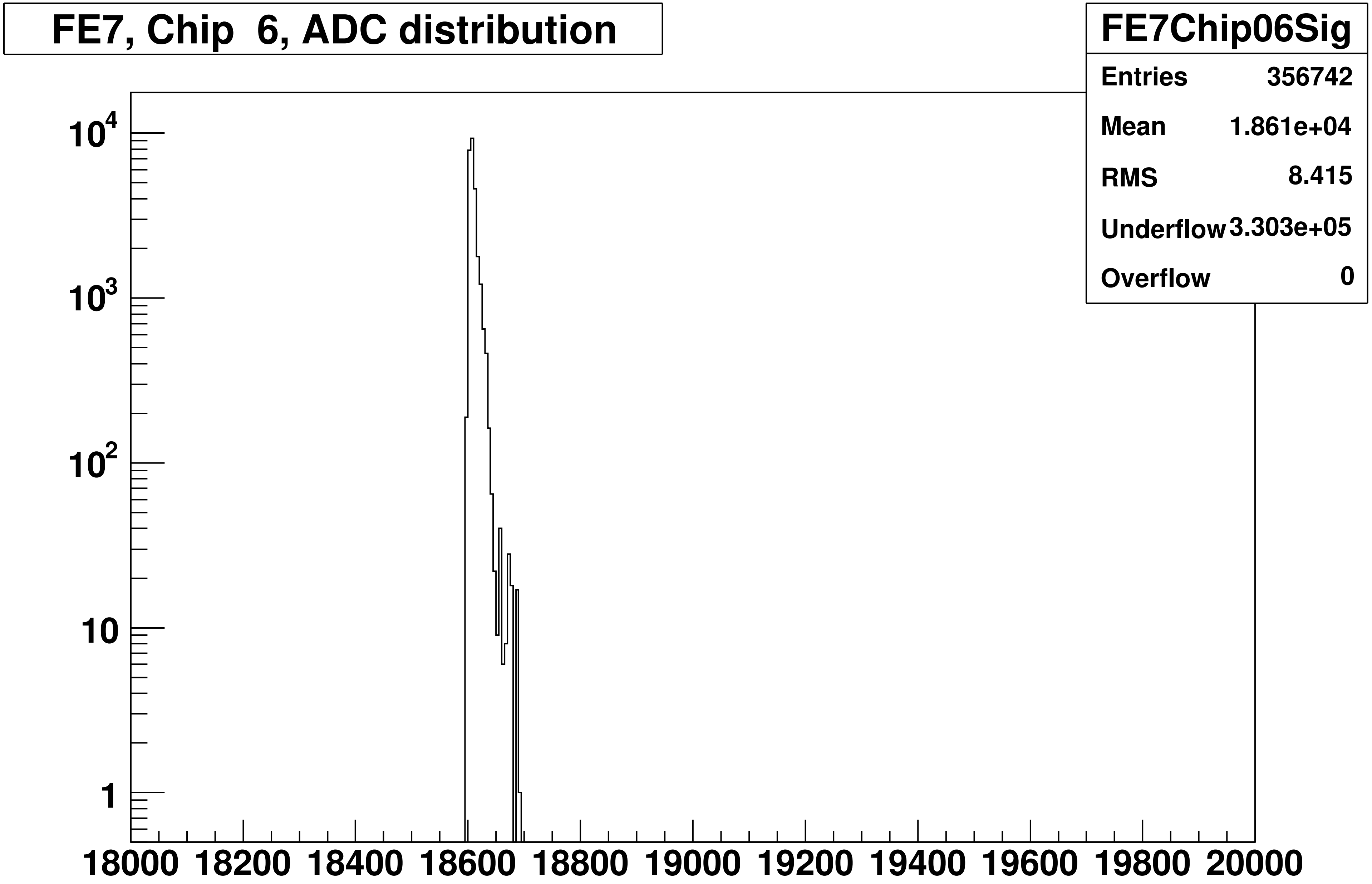
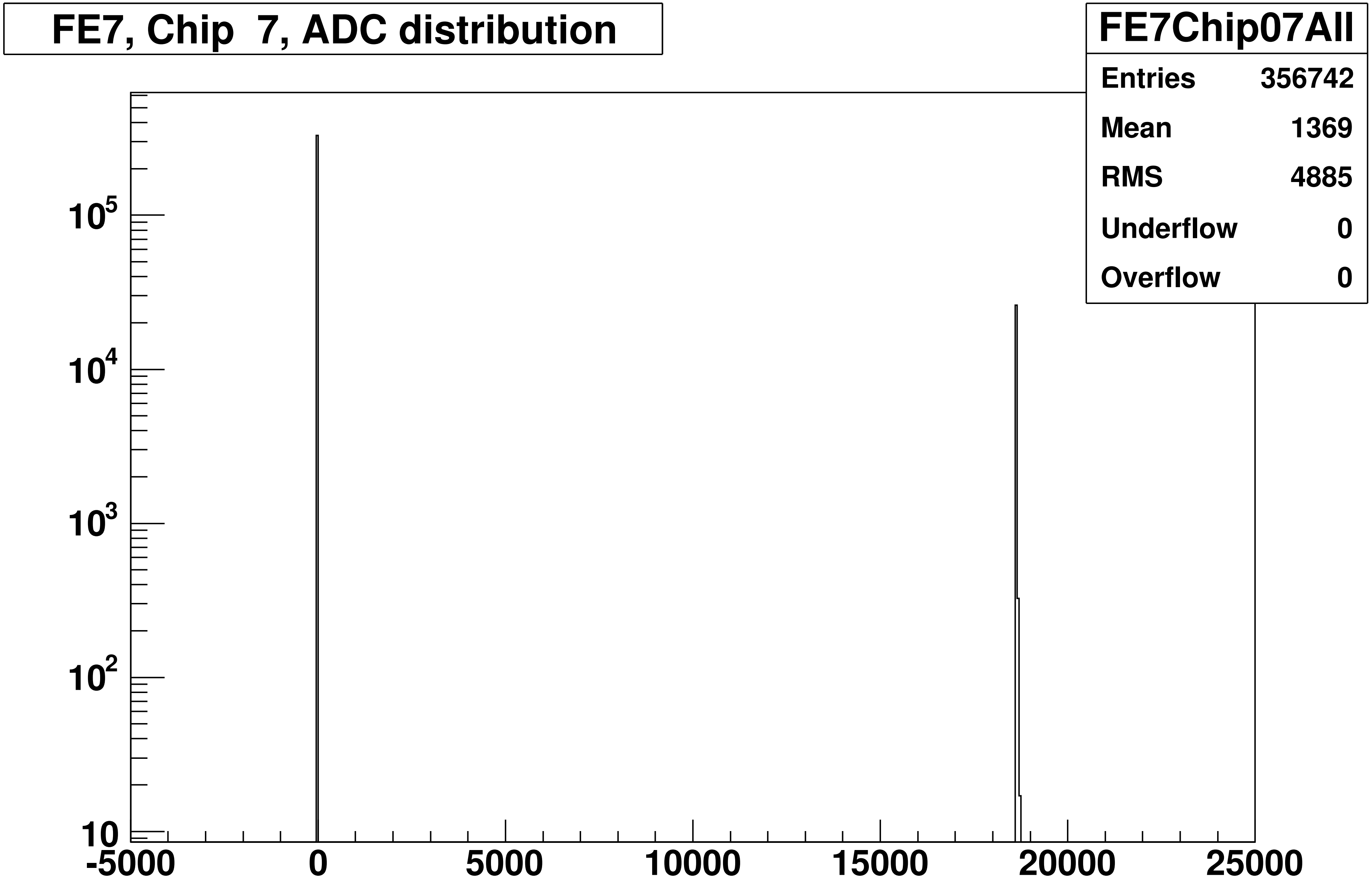
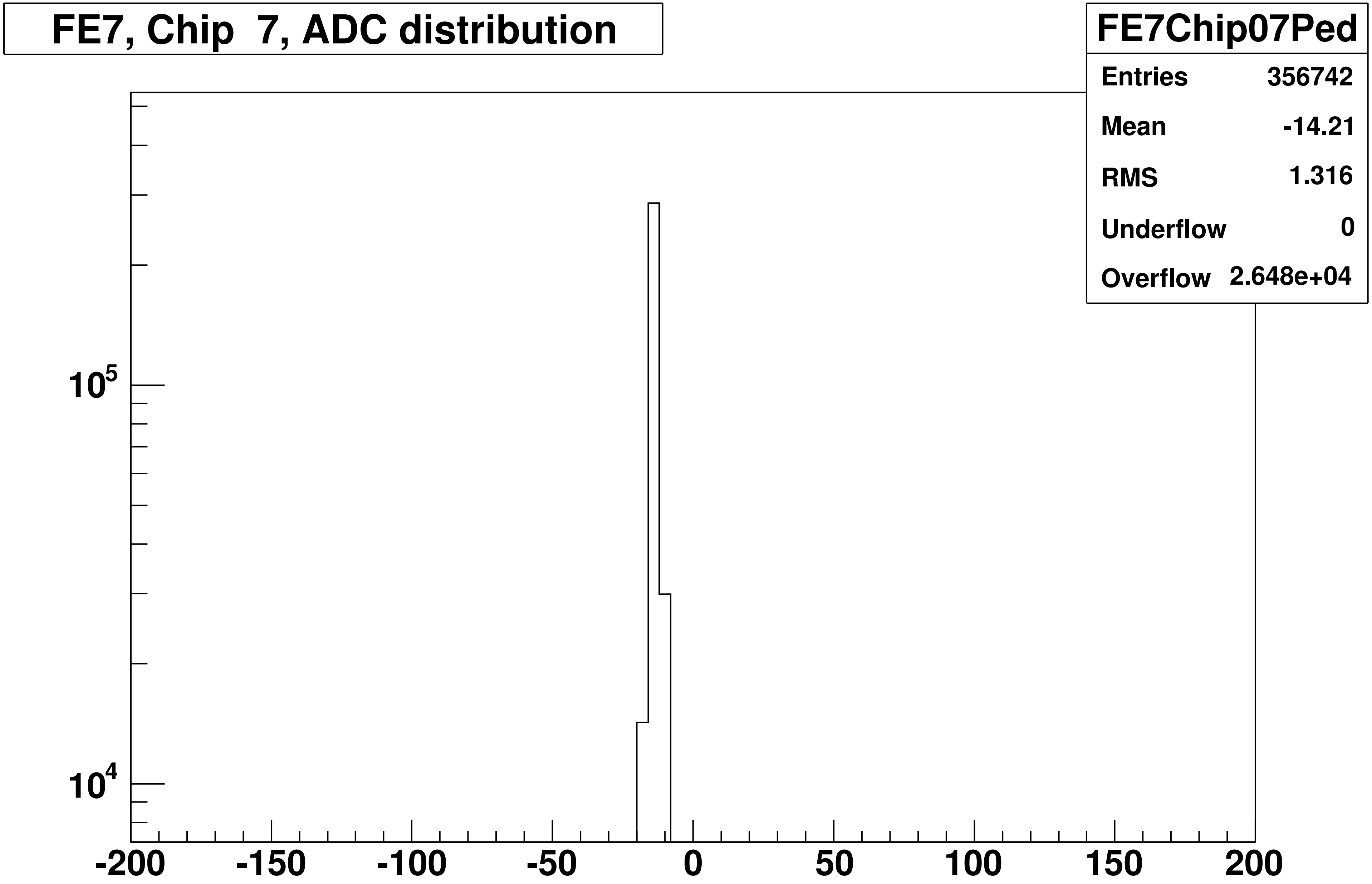
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



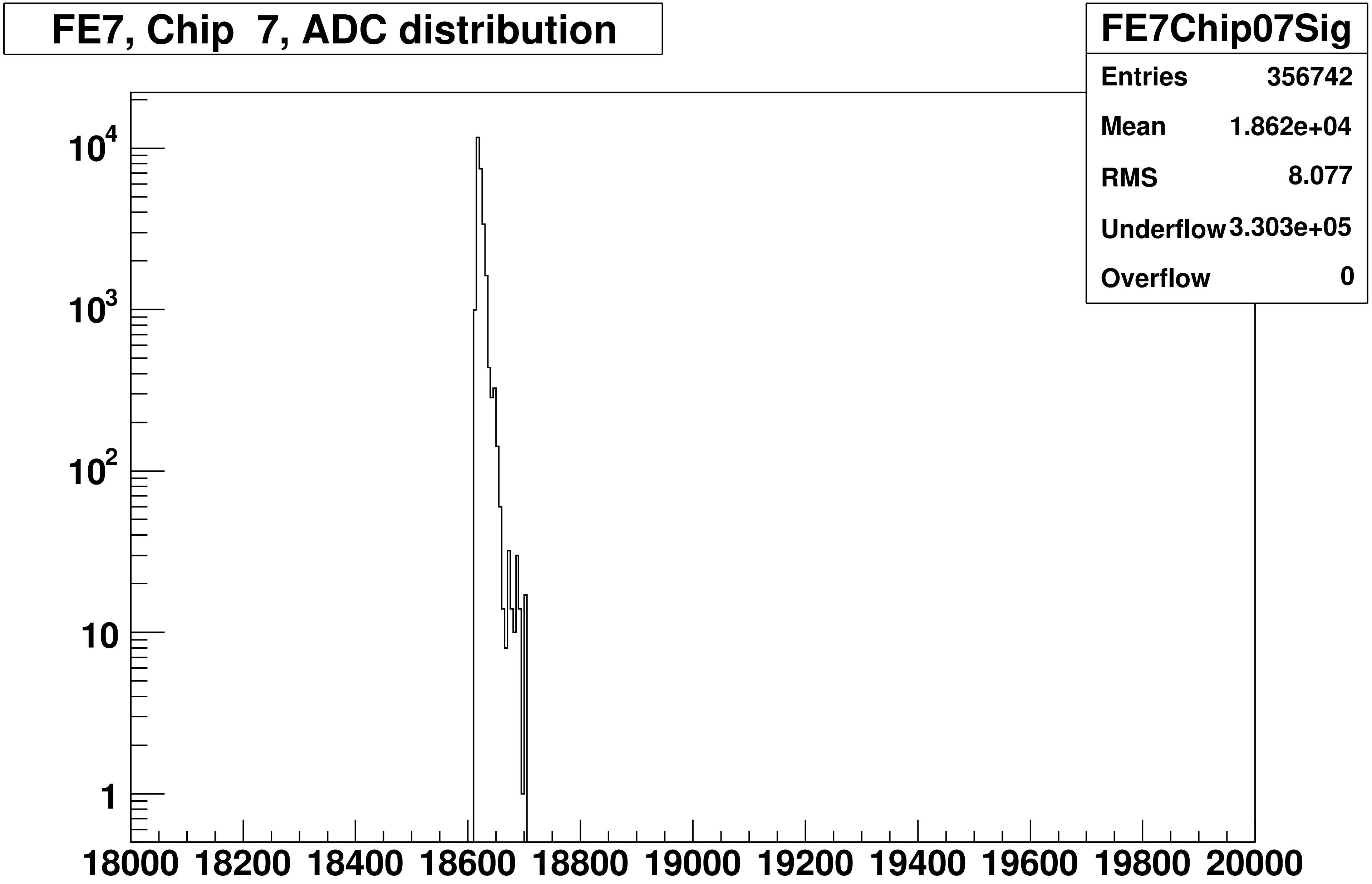
FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 356742
Mean -4.677
RMS 1.264
Underflow 0
Overflow 2.648e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200

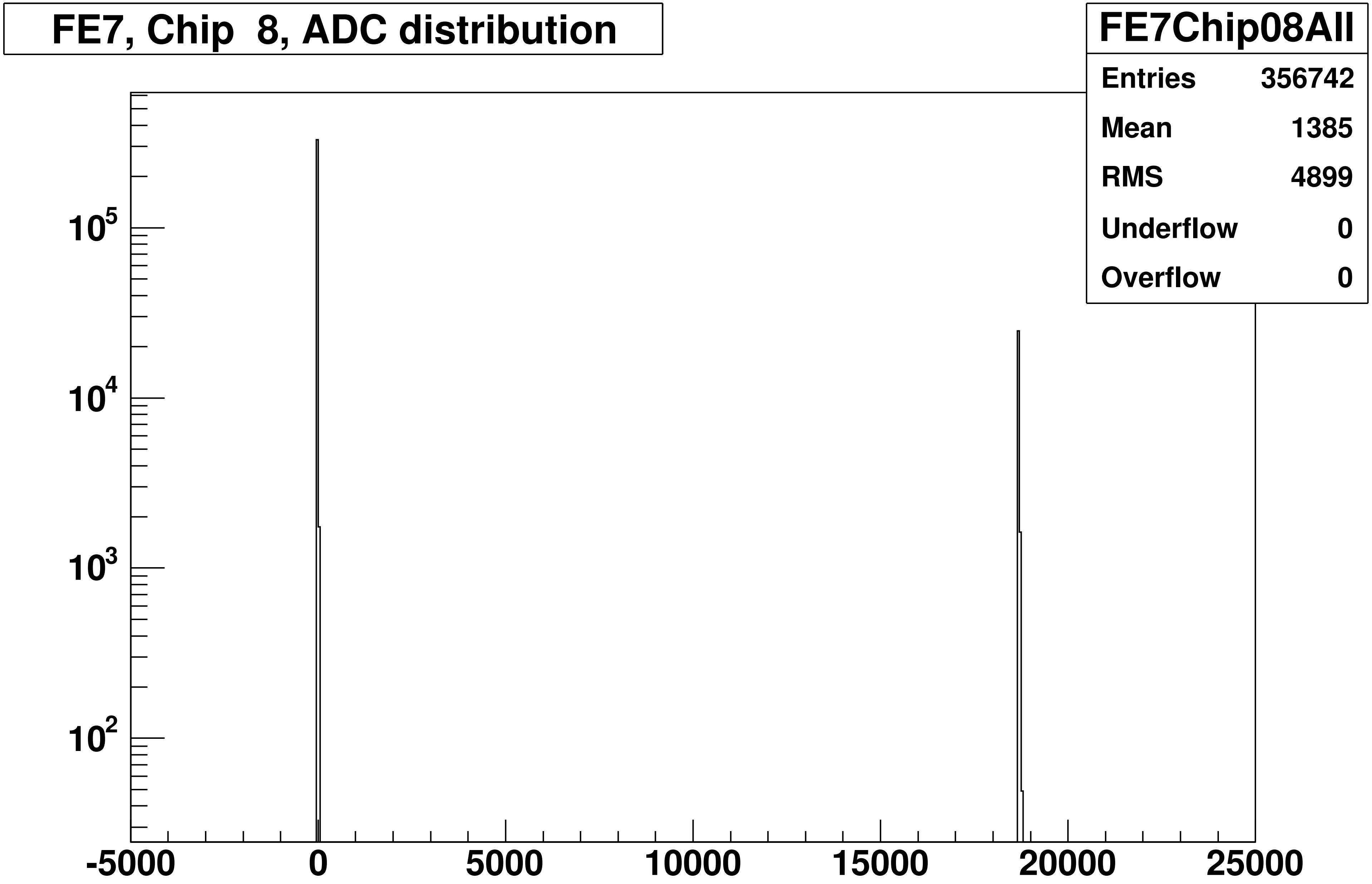

FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 356742
Mean 1.861e+04
RMS 8.415
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

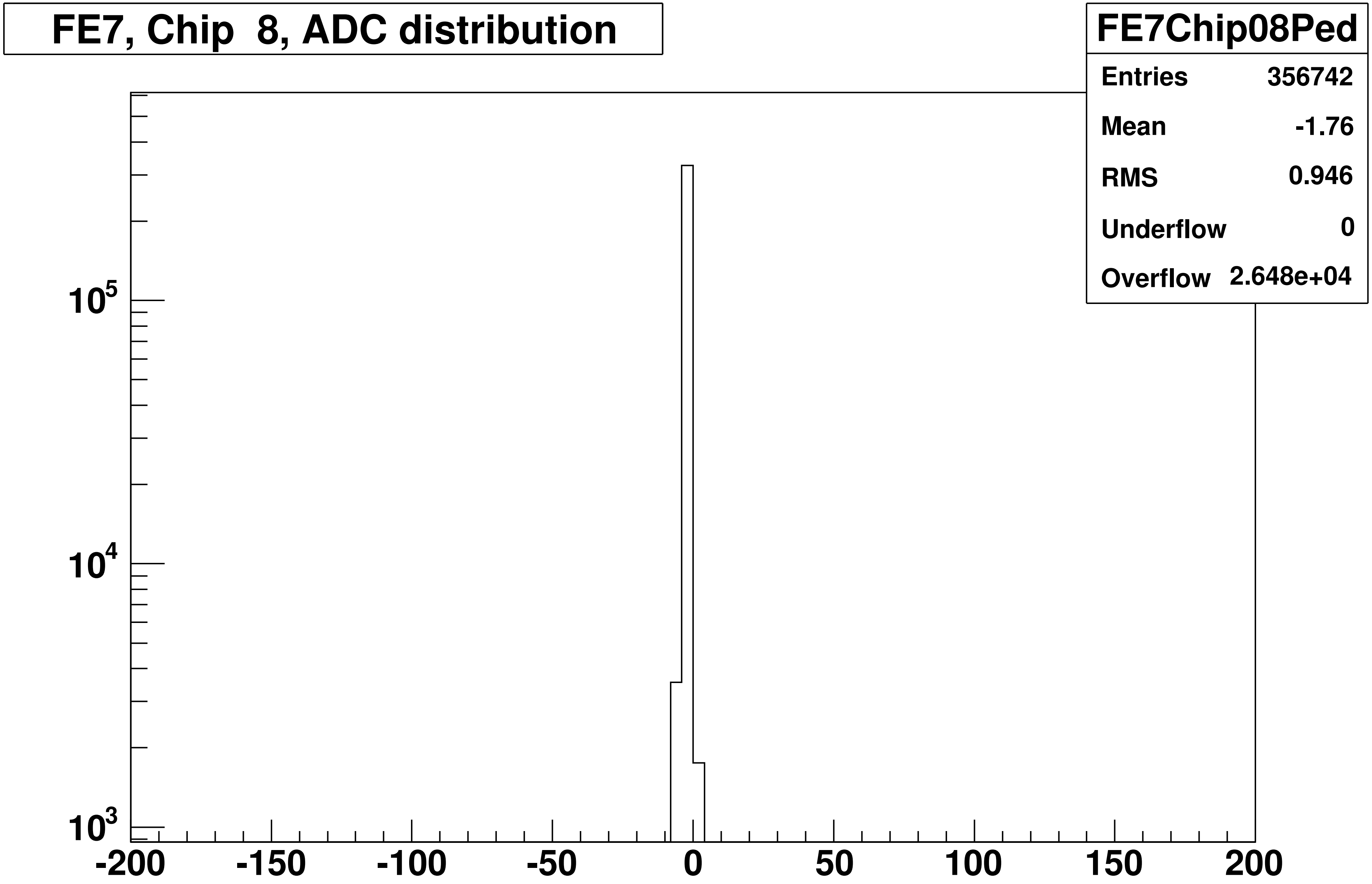

FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 356742
Mean 1369
RMS 4885
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000

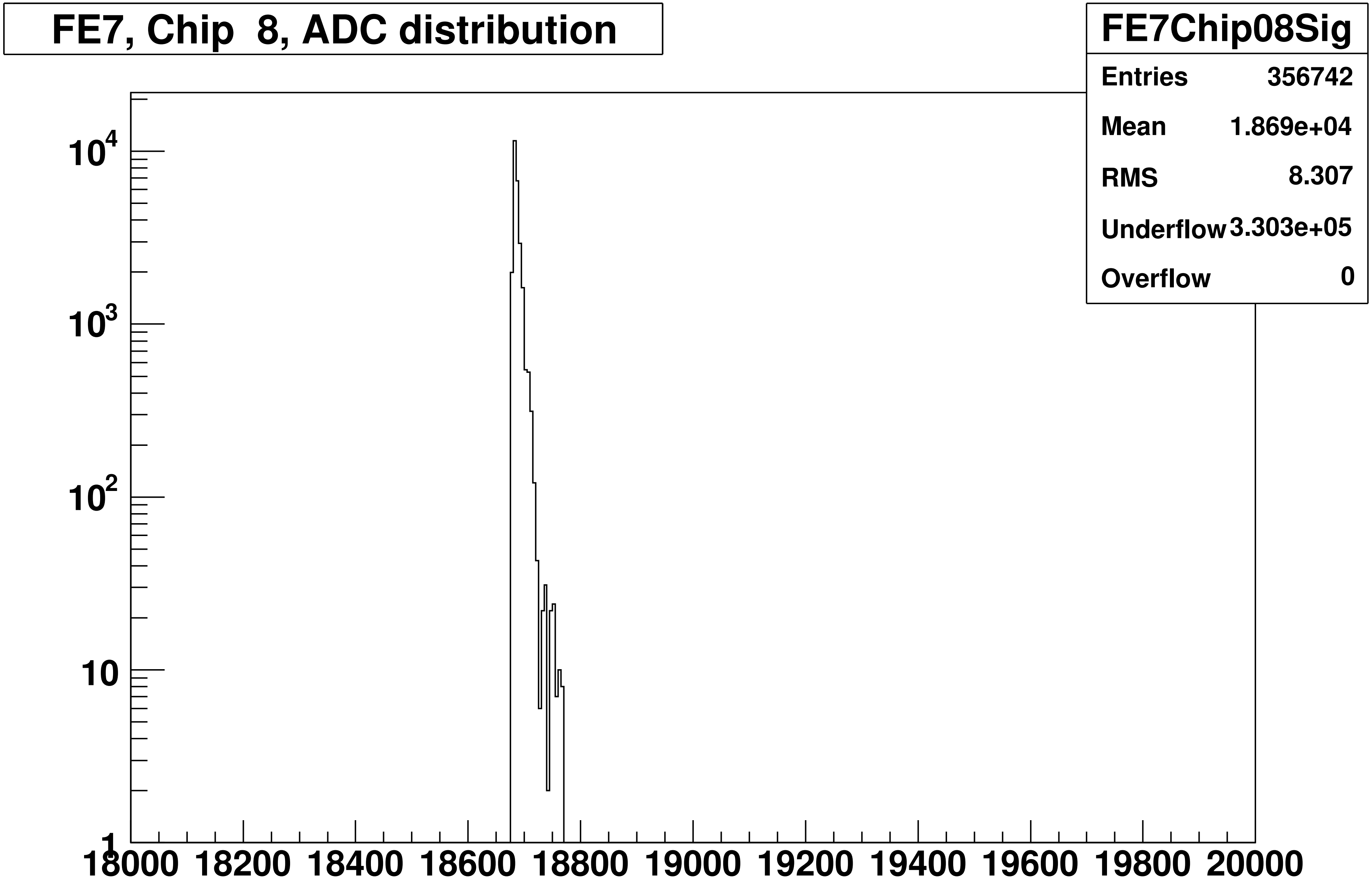


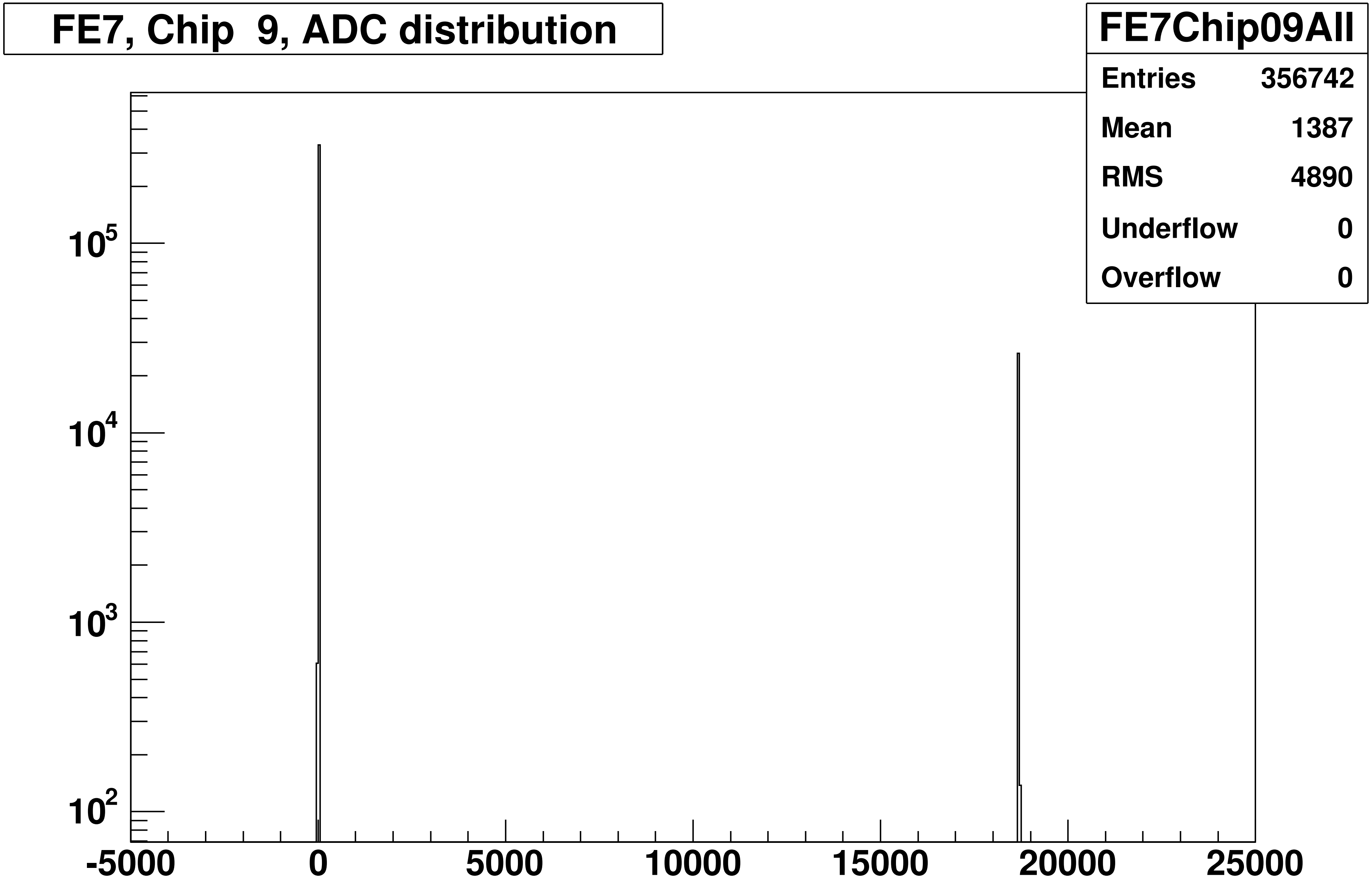
FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 356742
Mean -14.21
RMS 1.316
Underflow 0
Overflow 2.648e+04
10^5
10^4
-200 -150 -100 -50 0 50 100 150 200

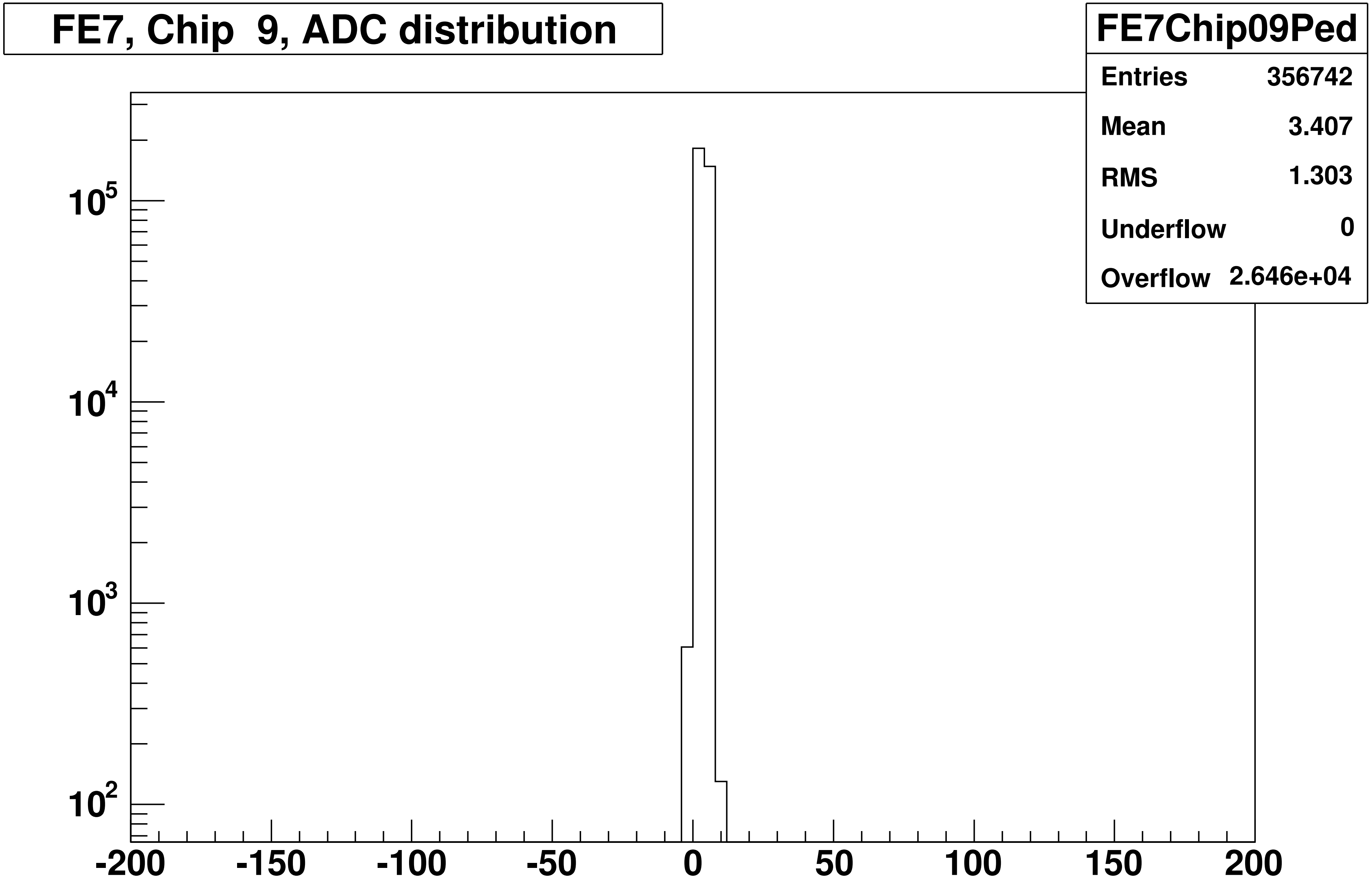

FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 356742
Mean 1.862e+04
RMS 8.077
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 356742
Mean 1385
RMS 4899
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

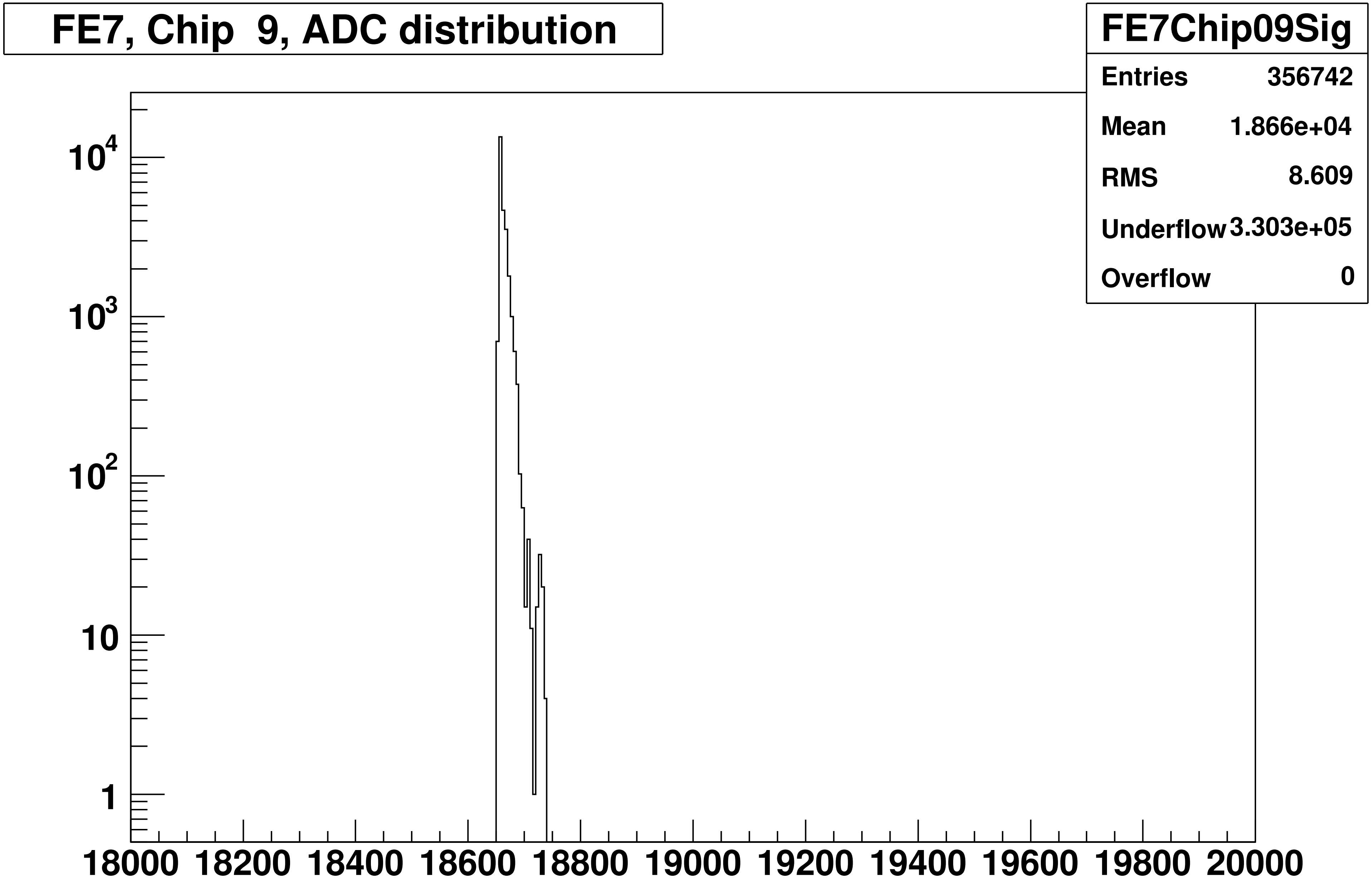

FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 356742
Mean -1.76
RMS 0.946
Underflow 0
Overflow 2.648e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200

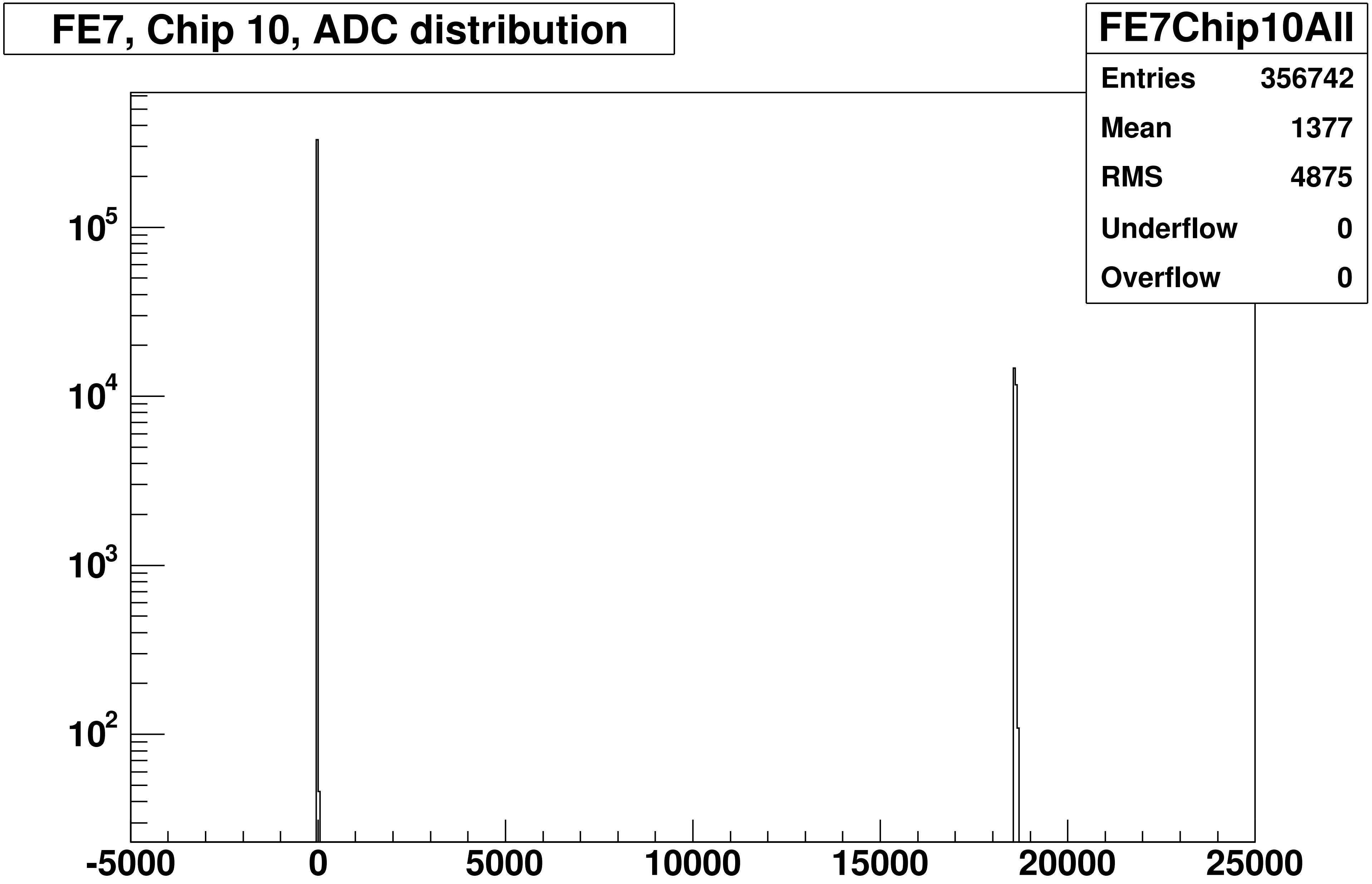

FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 356742
Mean 1.869e+04
RMS 8.307
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

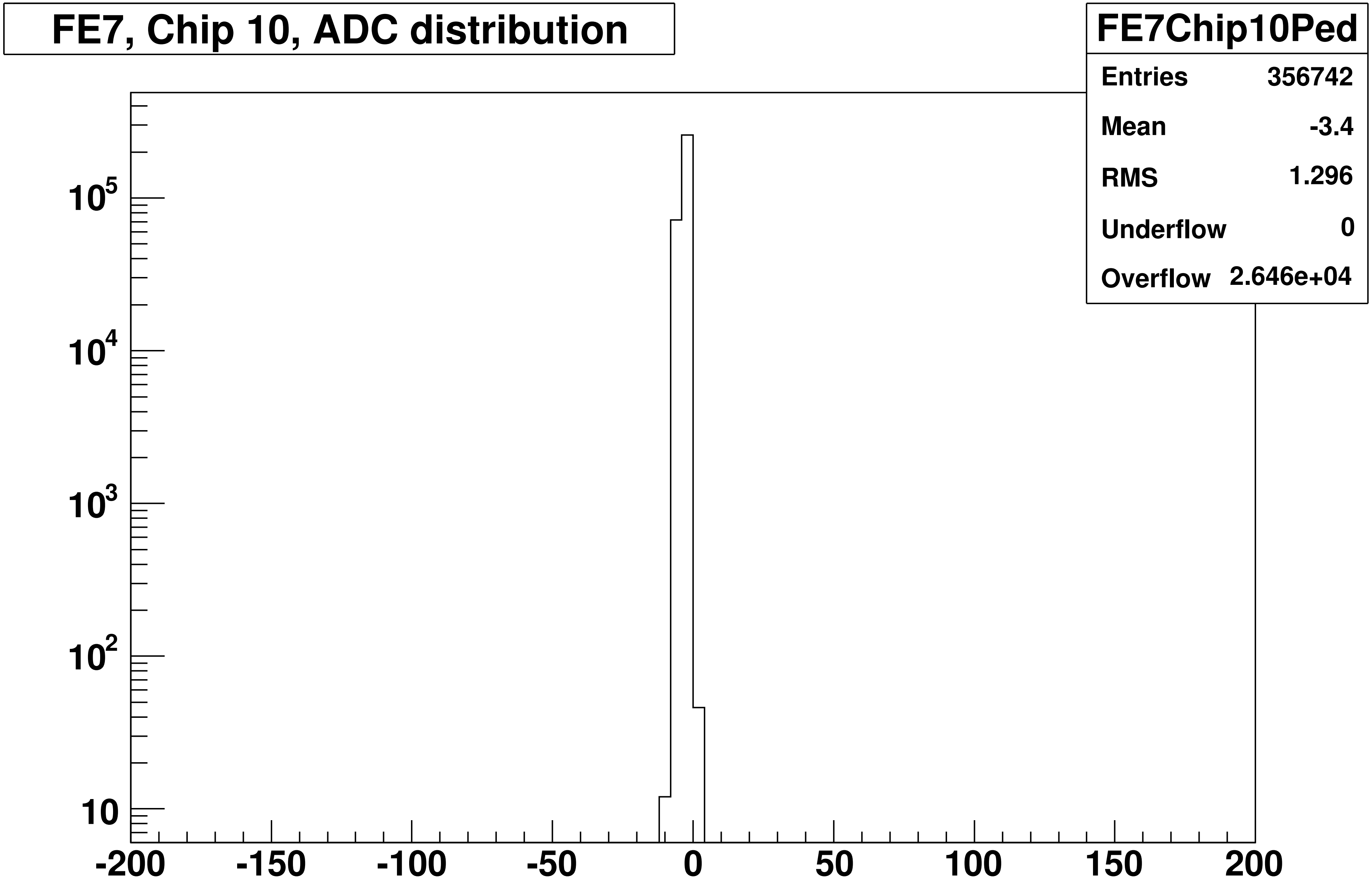

FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 356742
Mean 1387
RMS 4890
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

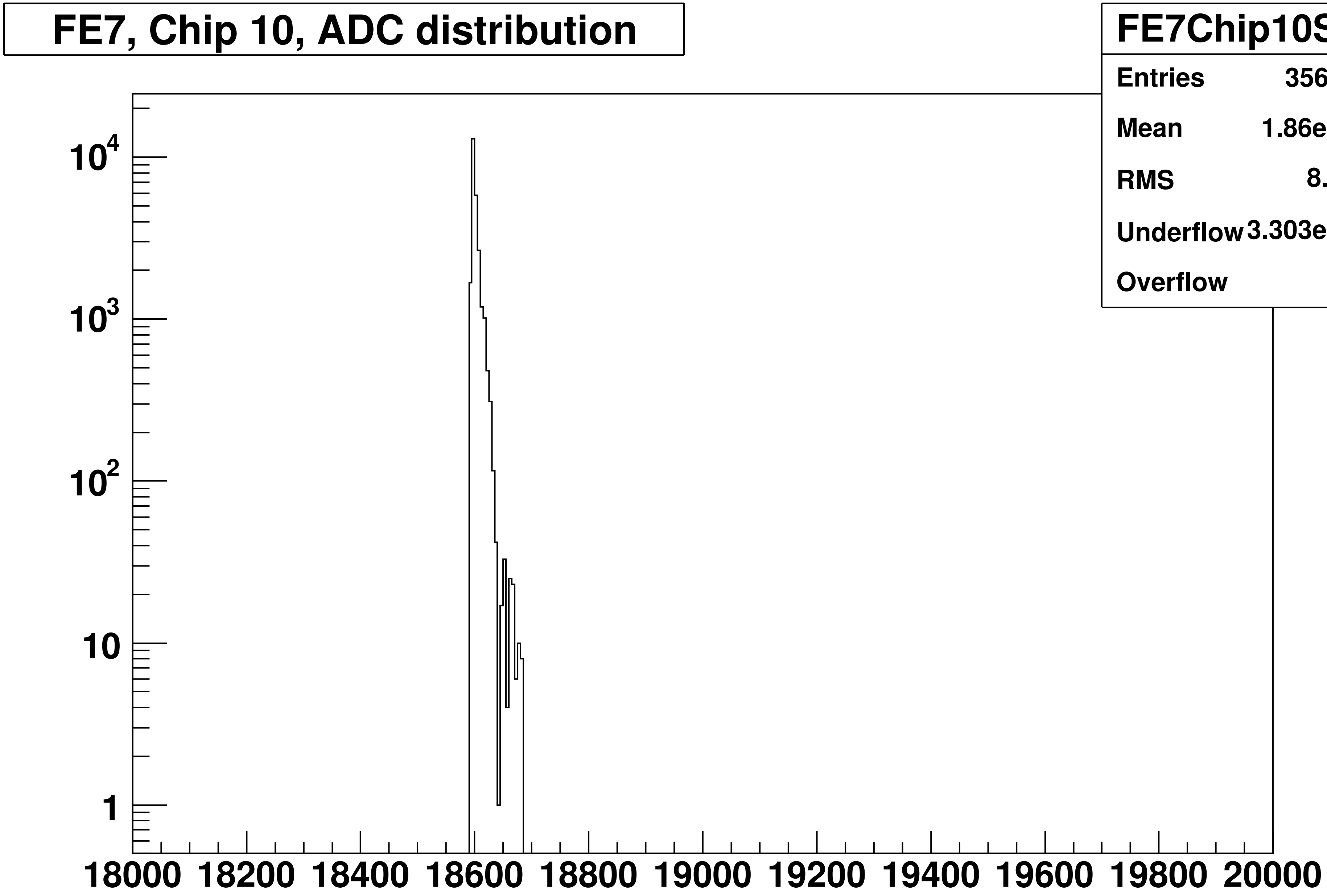


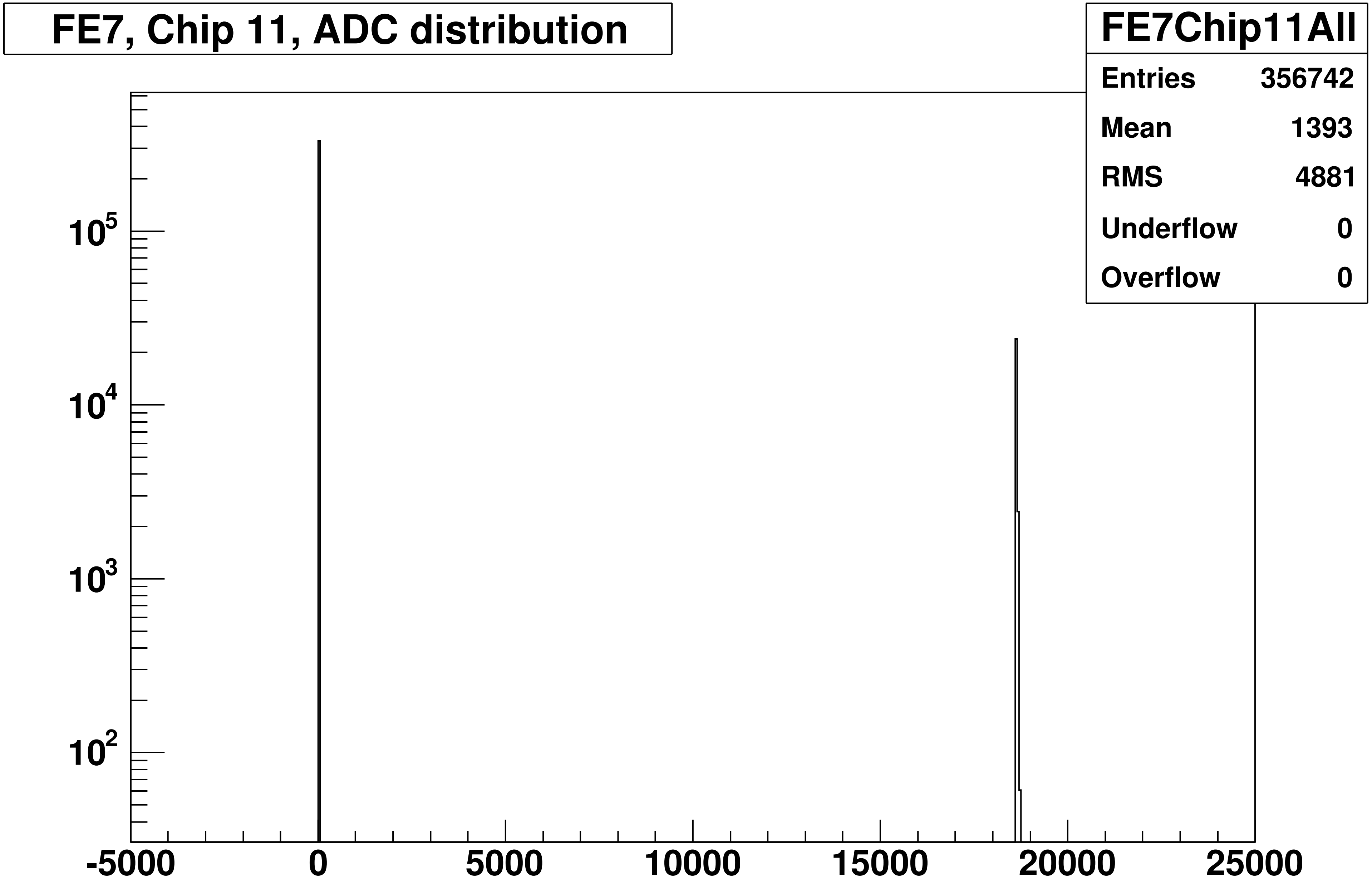
FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 356742
Mean 3.407
RMS 1.303
Underflow 0
Overflow 2.646e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200

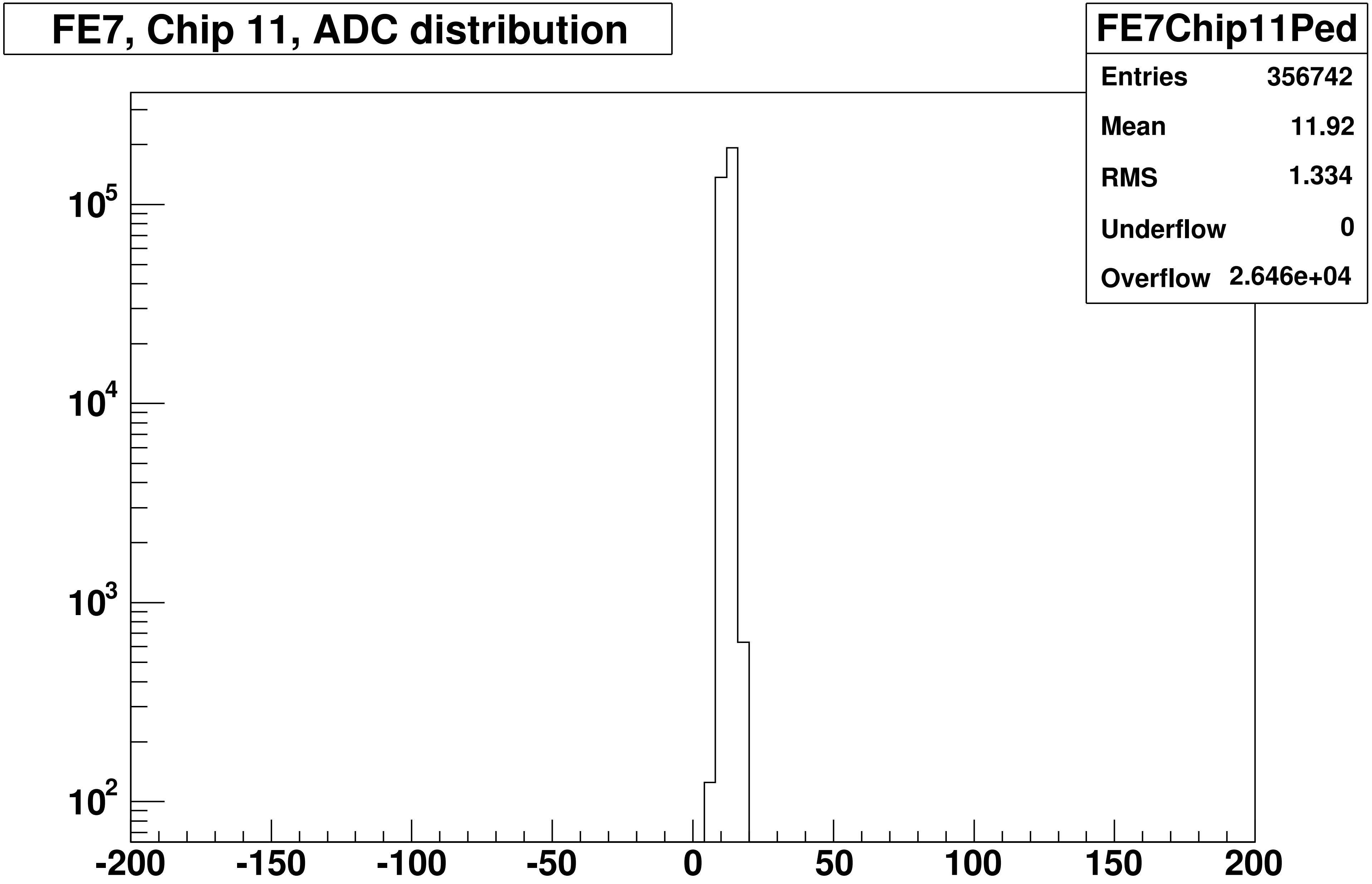

FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 356742
Mean 1.866e+04
RMS 8.609
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000
18200
18400
18600
18800
19000
19200
19400
19600
19800
20000

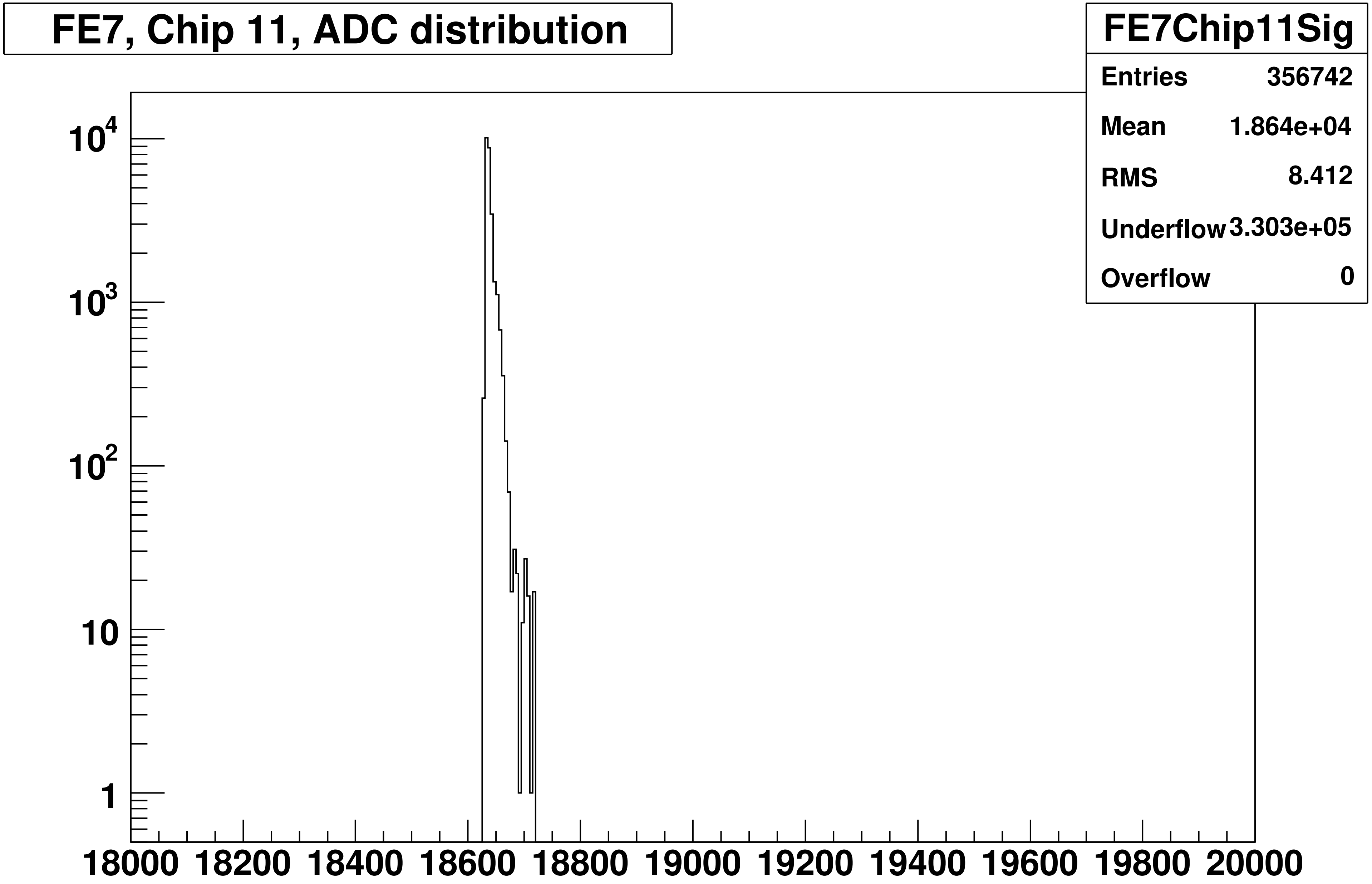

FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 356742
Mean 1377
RMS 4875
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 356742
Mean -3.4
RMS 1.296
Underflow 0
Overflow 2.646e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

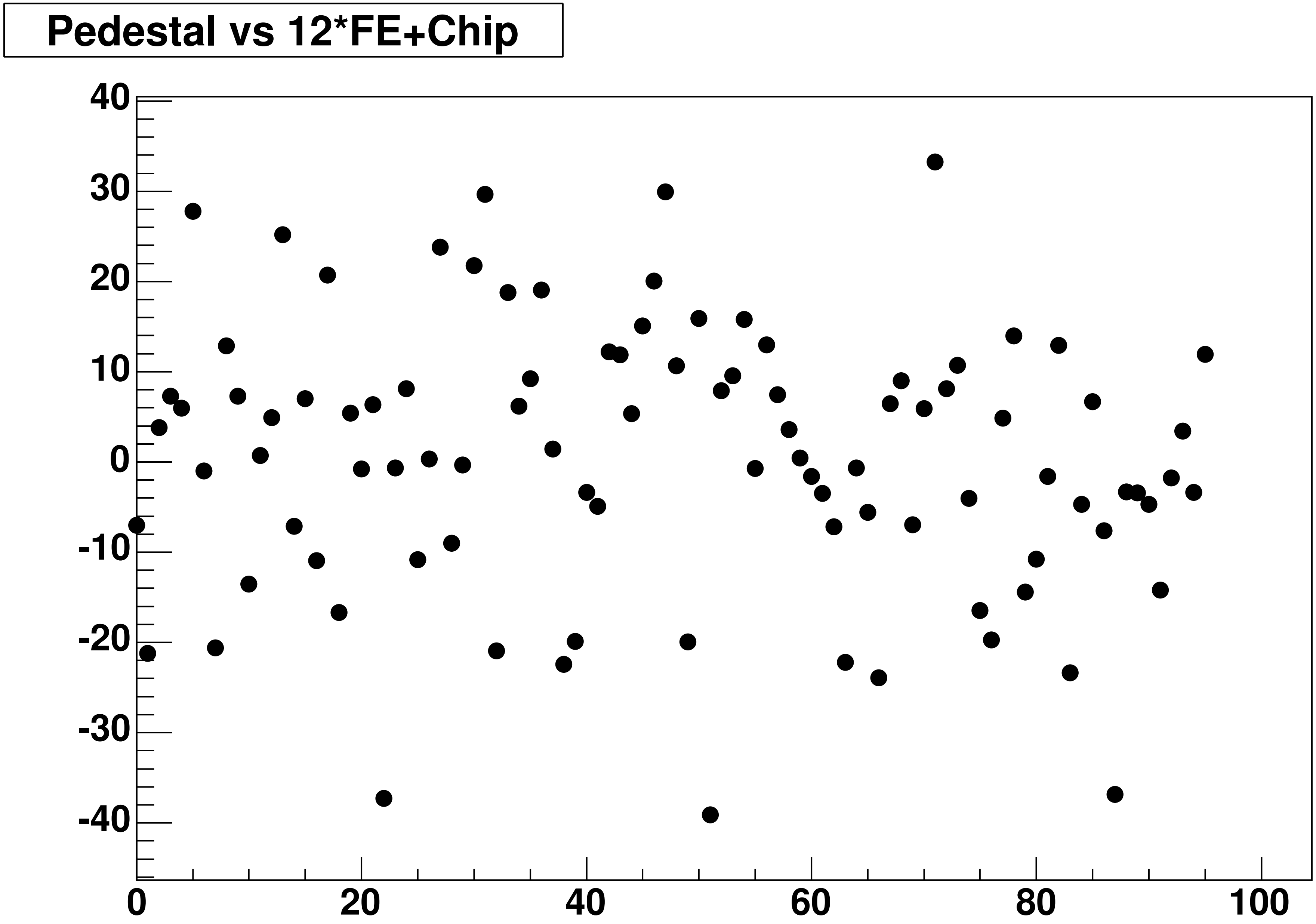

FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 356742
Mean 1.86e+04
RMS 8.422
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000

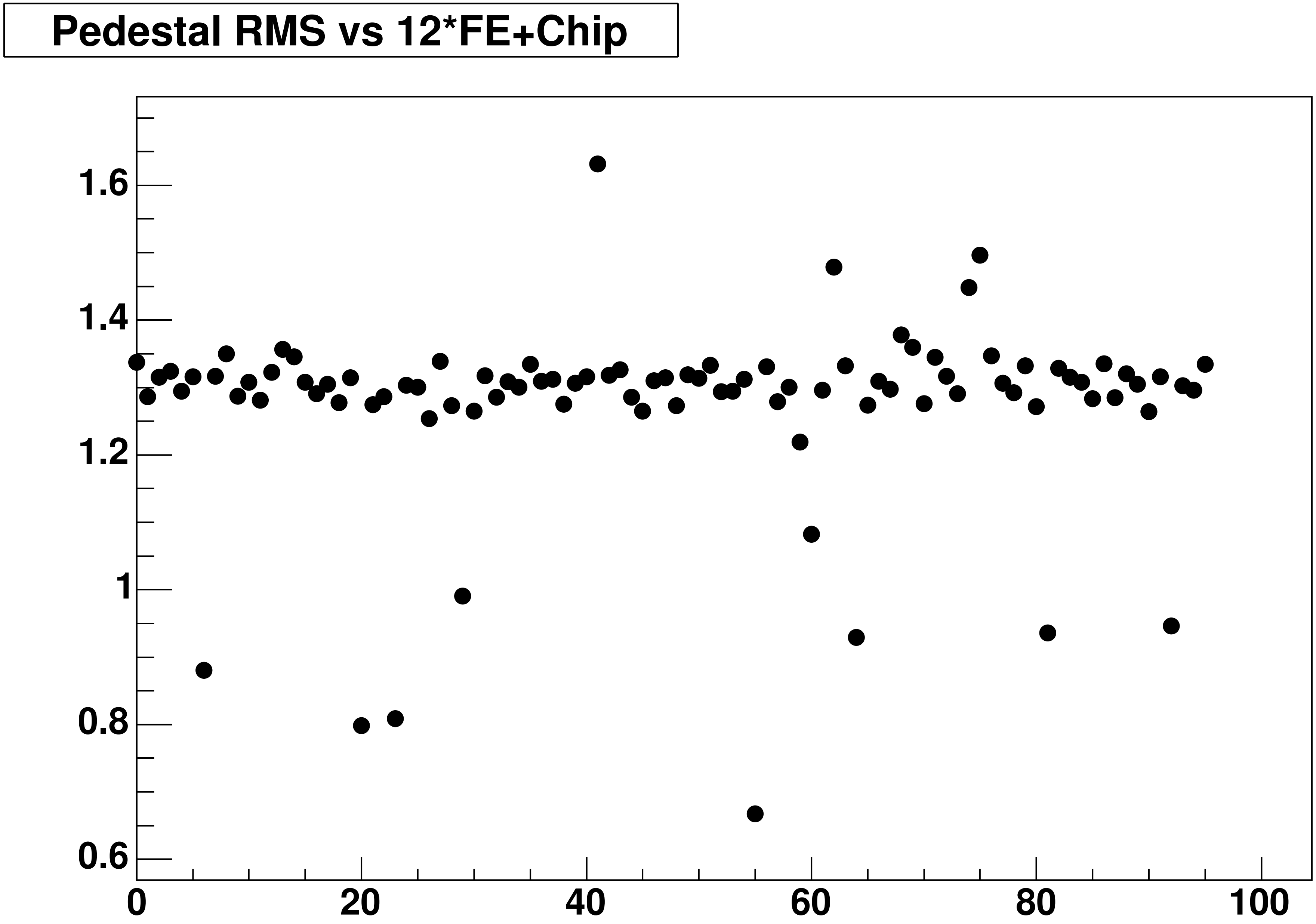

FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 356742
Mean 1393
RMS 4881
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

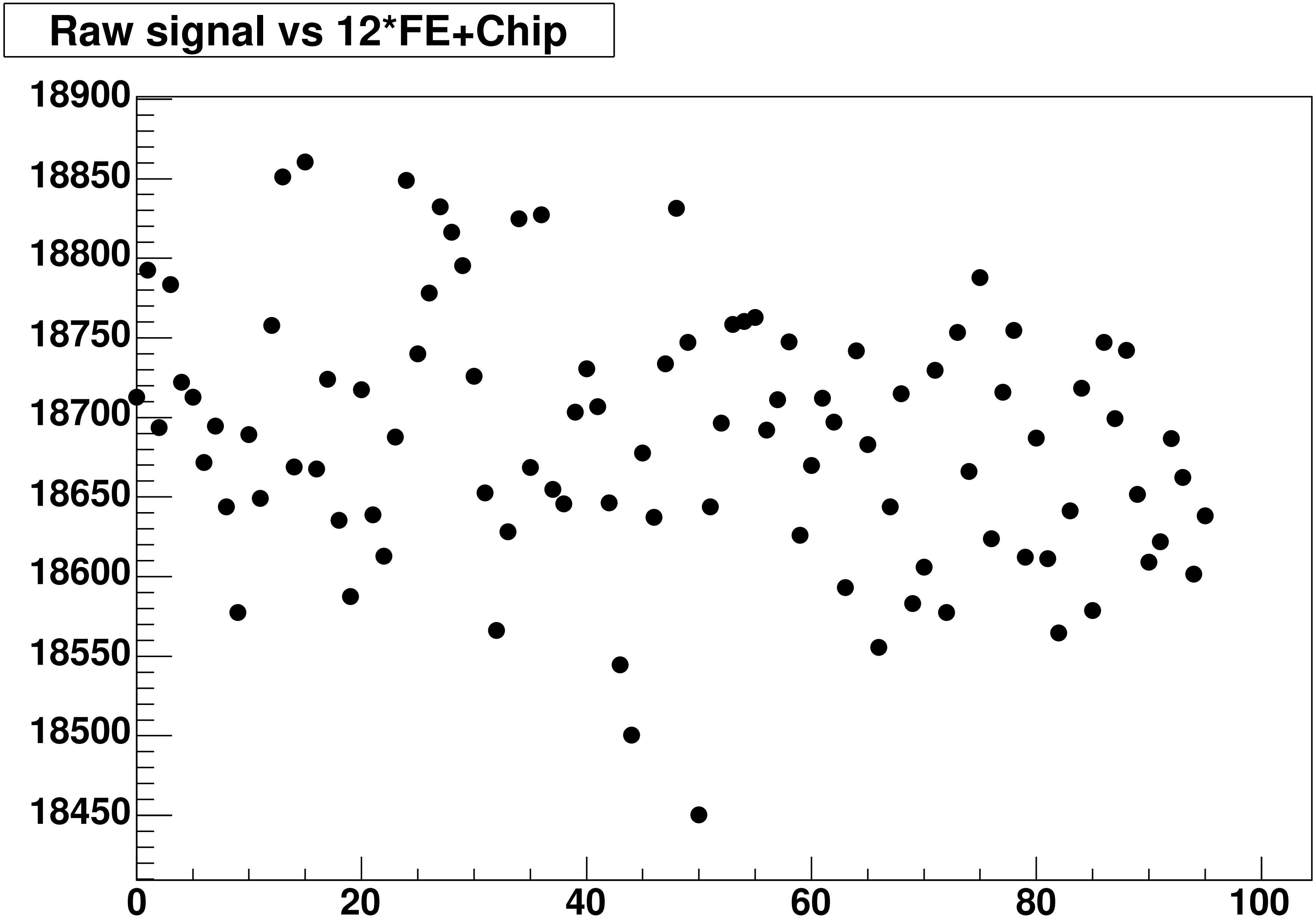

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 356742
Mean 11.92
RMS 1.334
Underflow 0
Overflow 2.646e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

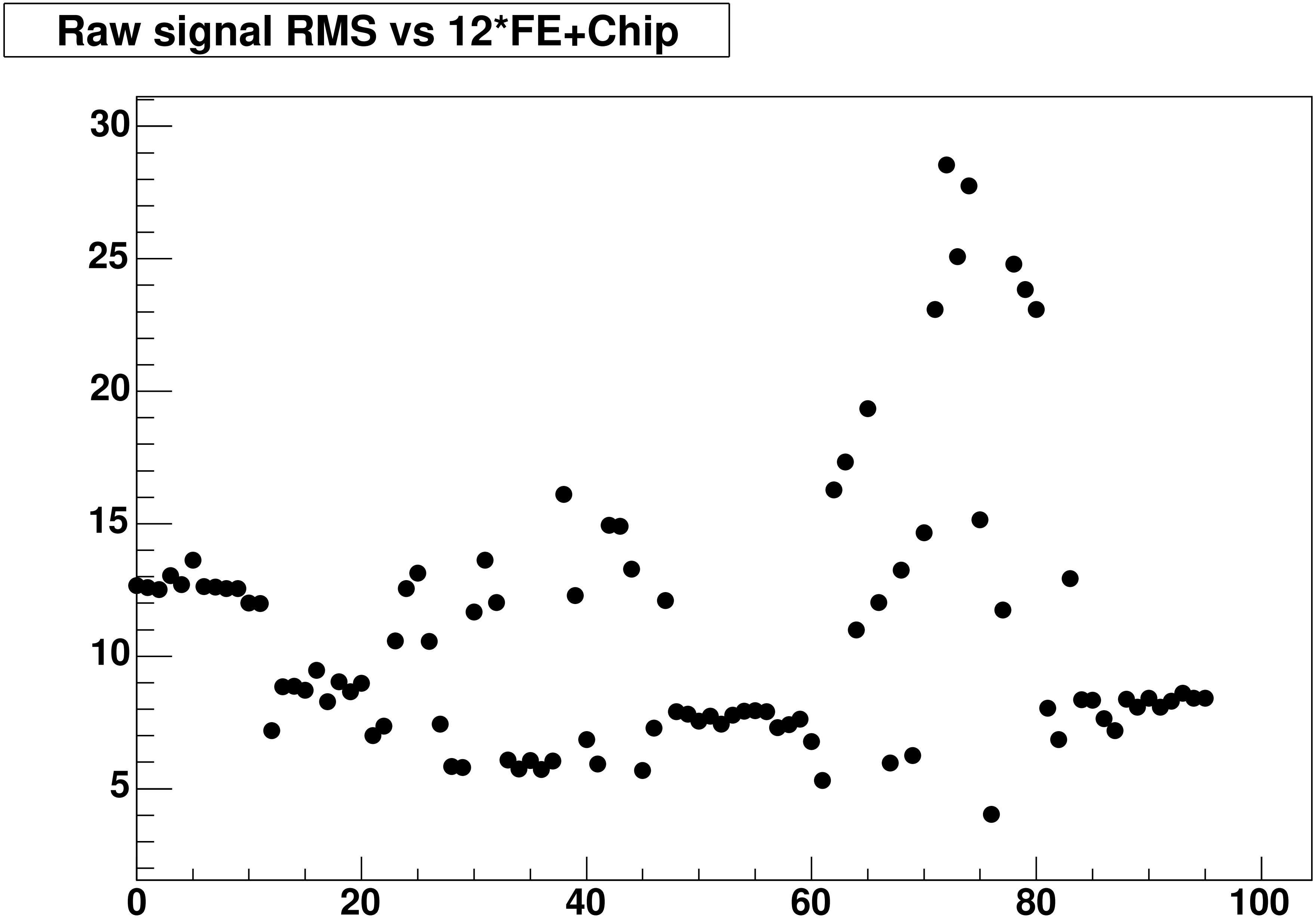


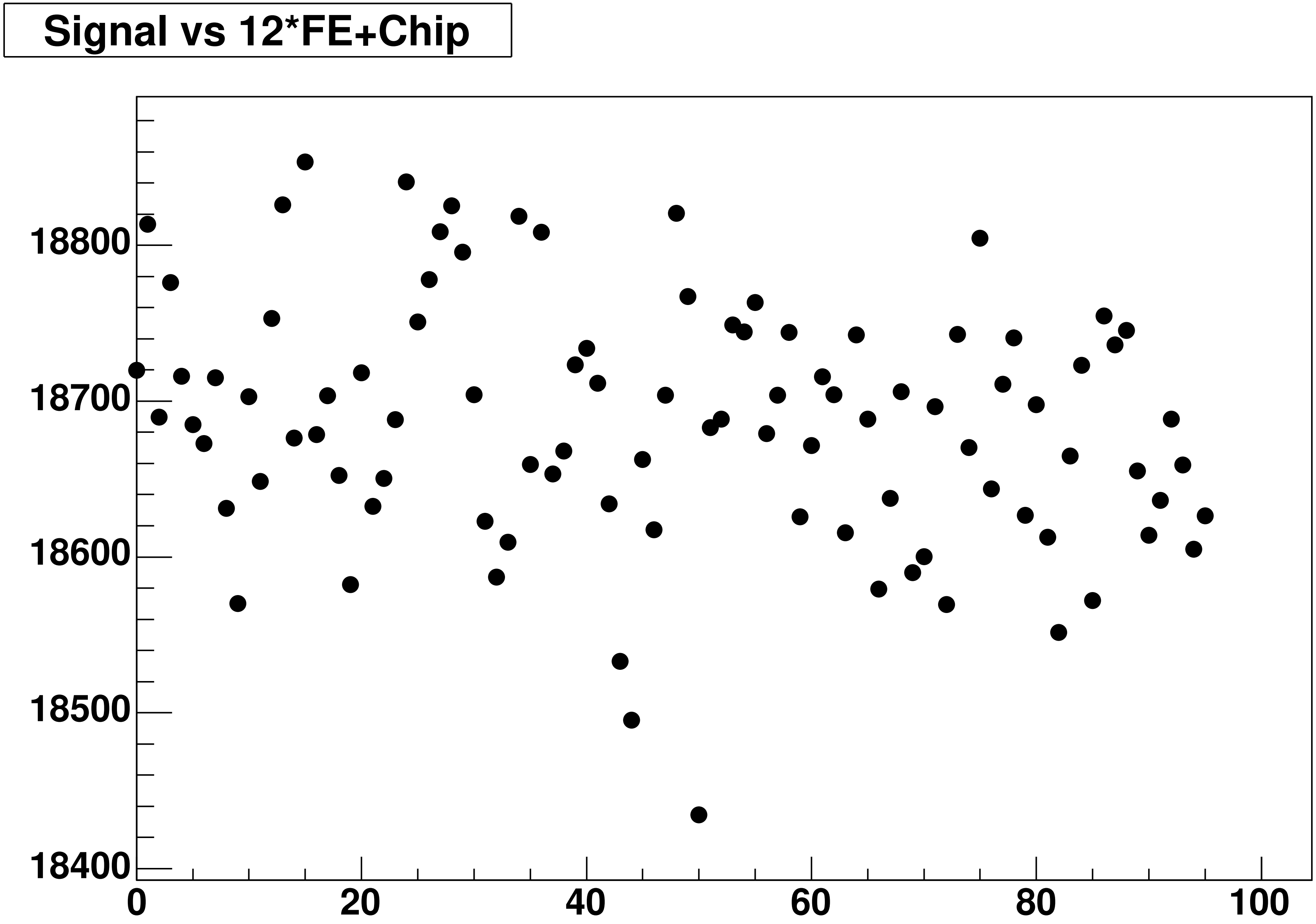
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 356742
Mean 1.864e+04
RMS 8.412
Underflow 3.303e+05
Overflow 0
10^4
10^3
10^2
10
1
18000 18200 18400 18600 18800 19000 19200 19400 19600 19800 20000


Pedestal vs 12*FE+Chip
40
30
20
10
0
-10
-20
-30
-40
0
20
40
60
80
100

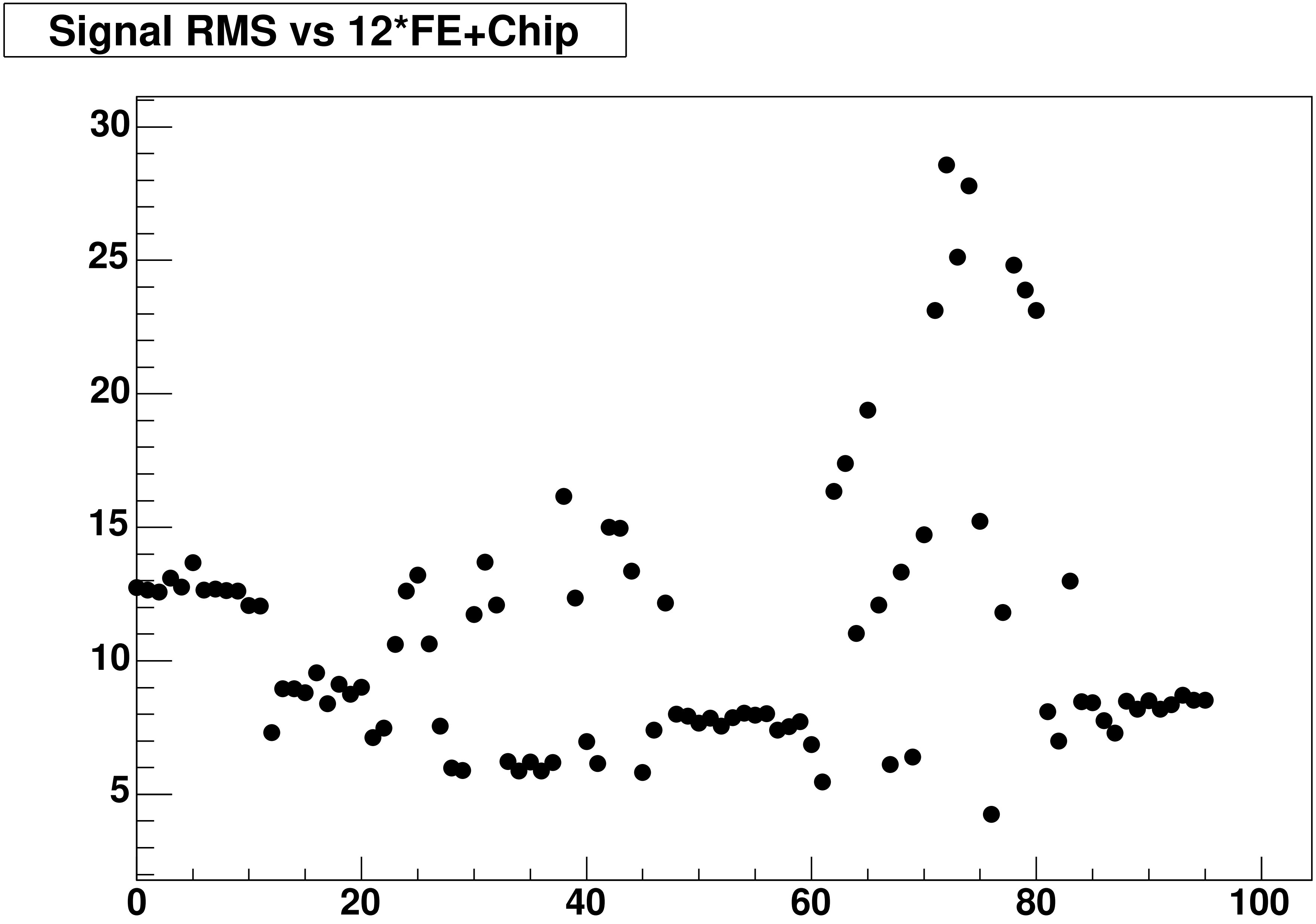

Pedestal RMS vs 12*FE+Chip
1.6
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
18900
18850
18800
18750
18700
18650
18600
18550
18500
18450
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
30
25
20
15
10
5
0
20
40
60
80
100



Signal vs 12*FE+Chip
18400
18500
18600
18700
18800
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
30
25
20
15
10
5
0
20
40
60
80
100