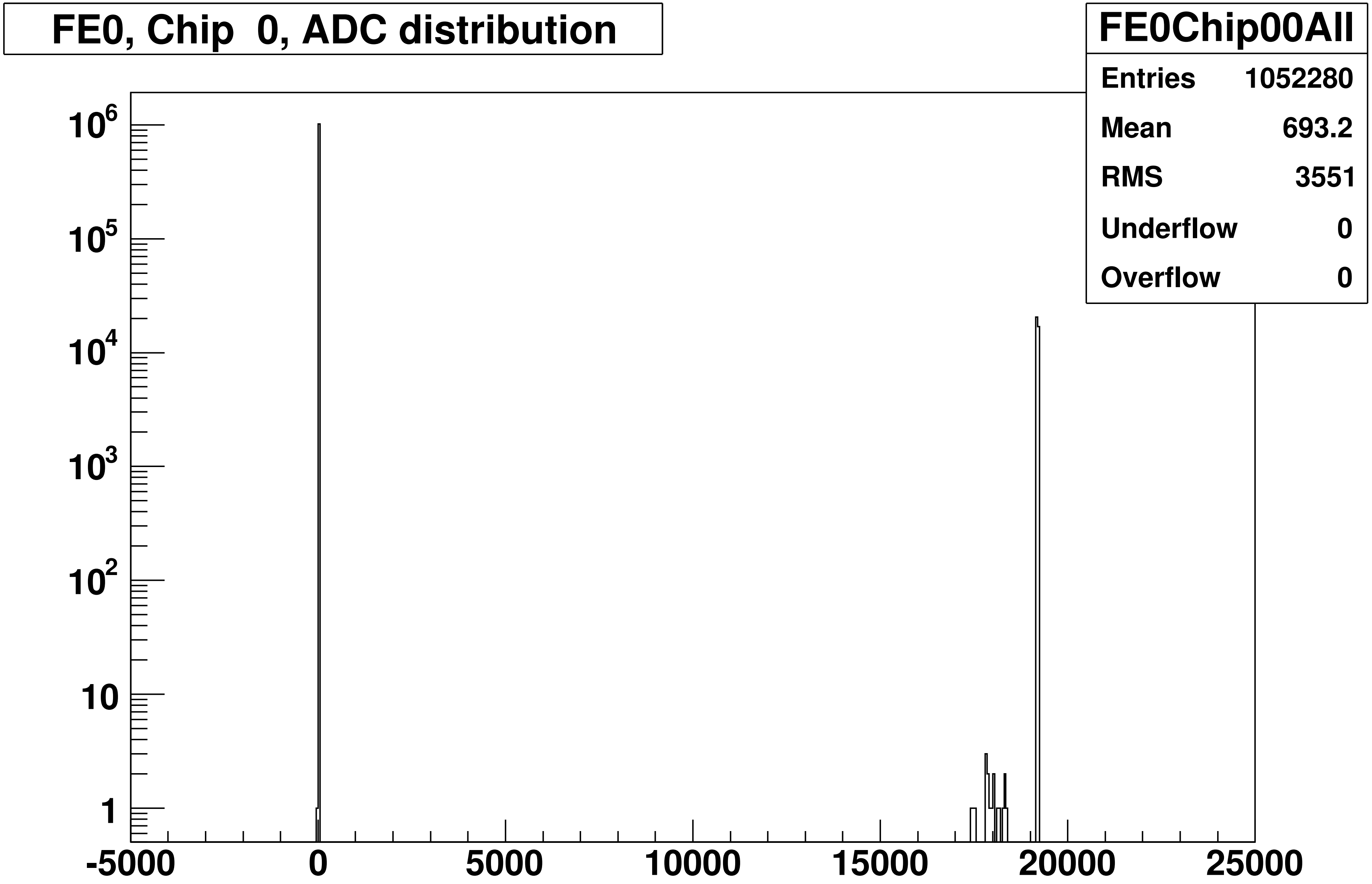
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 1052280
Mean 693.2
RMS 3551
Underflow 0
Overflow 0
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10^4
10^3
10^2
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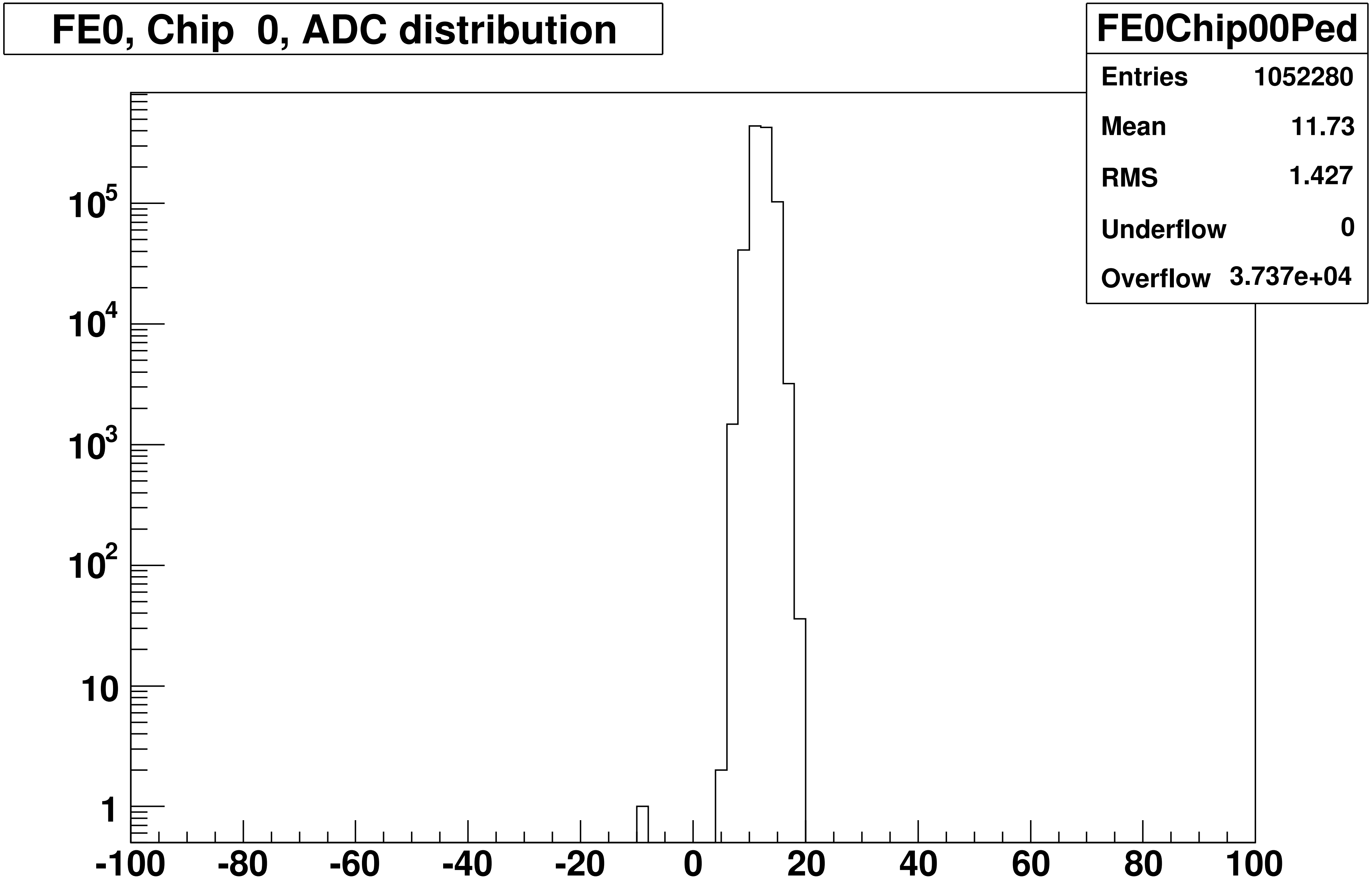
FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 1052280
Mean 11.73
RMS 1.427
Underflow 0
Overflow 3.737e+04
10^5
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10^2
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-40
-20
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80
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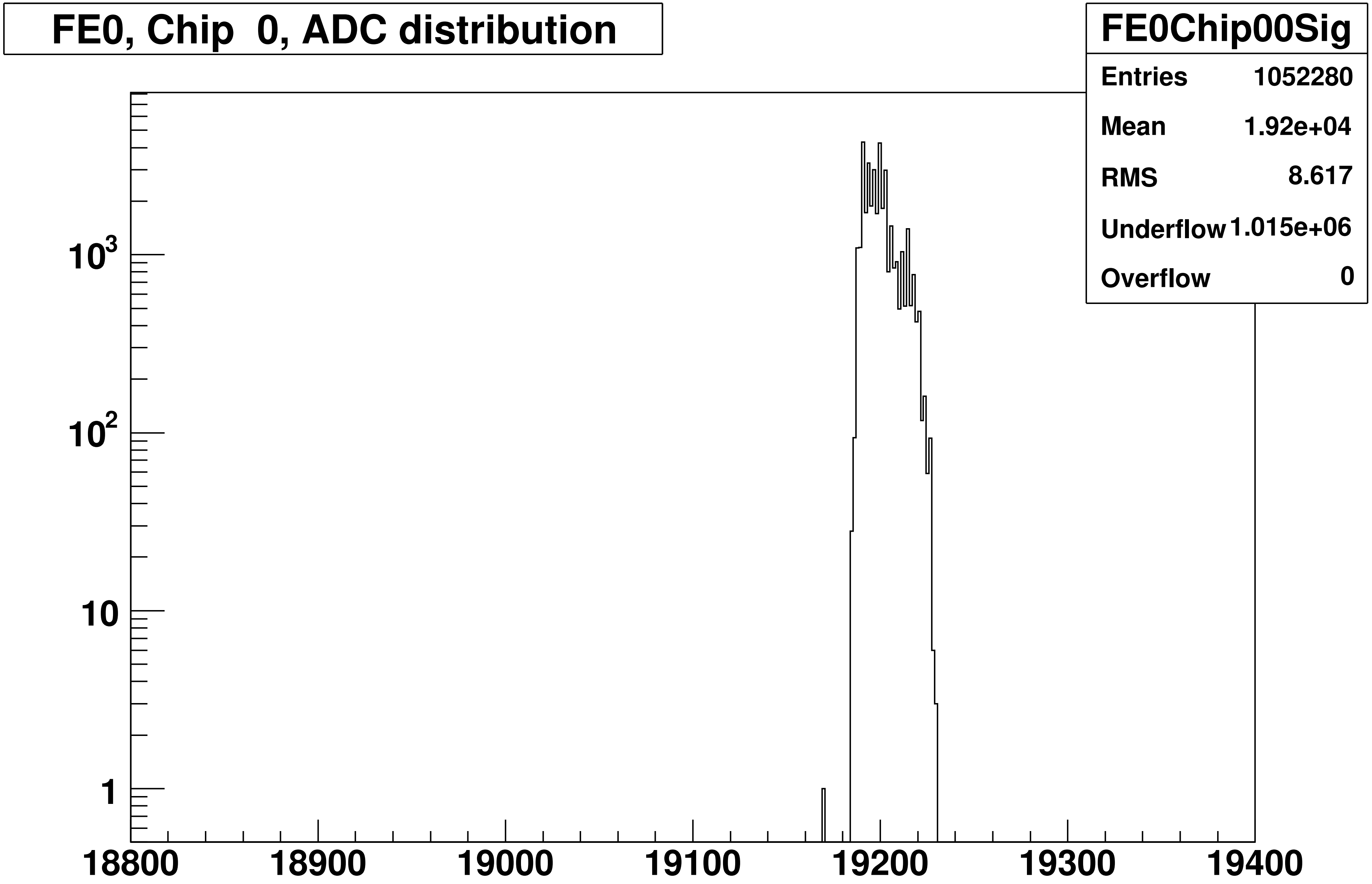
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 1052280
Mean 1.92e+04
RMS 8.617
Underflow 1.015e+06
Overflow 0
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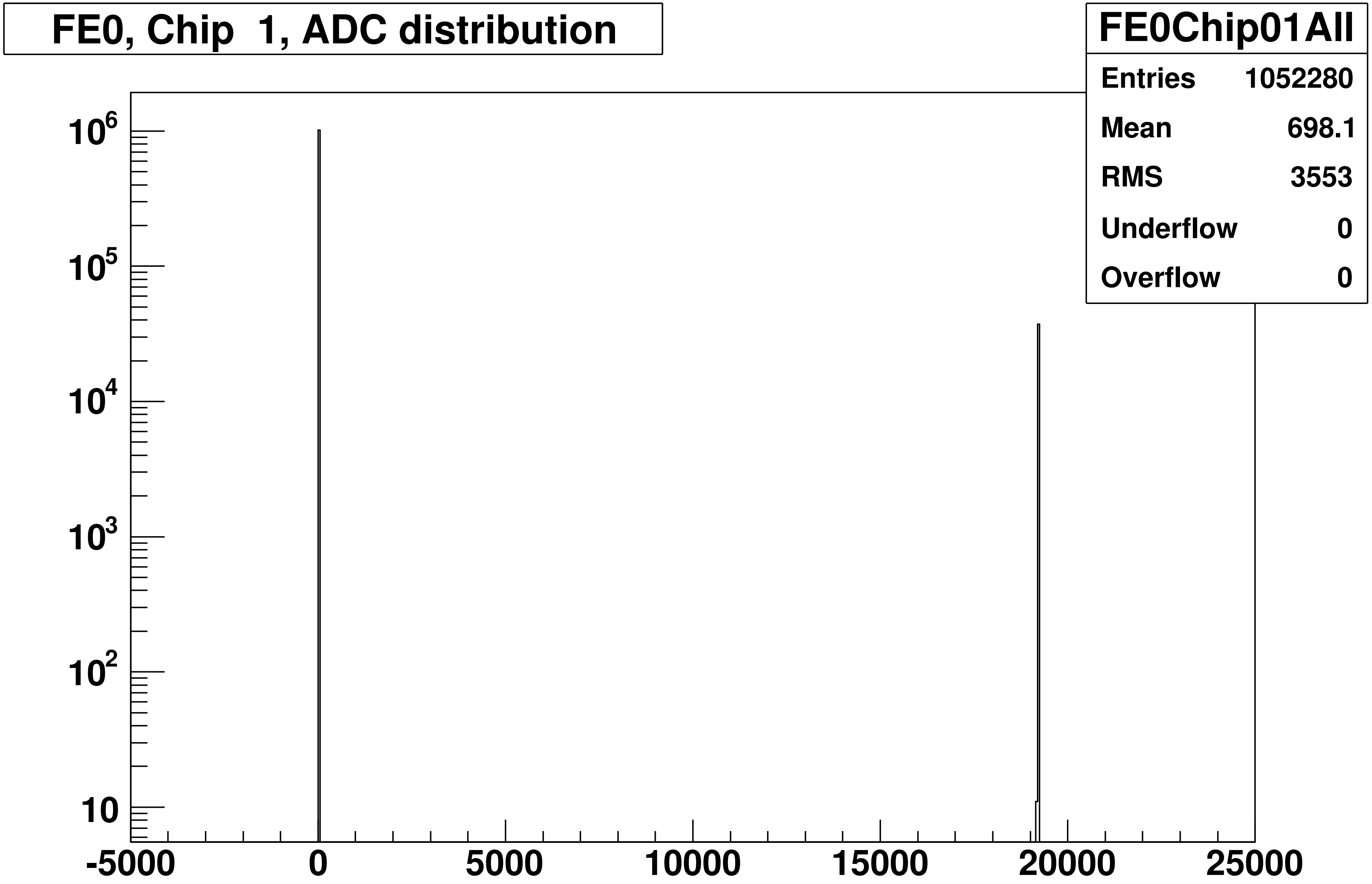

FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 1052280
Mean 698.1
RMS 3553
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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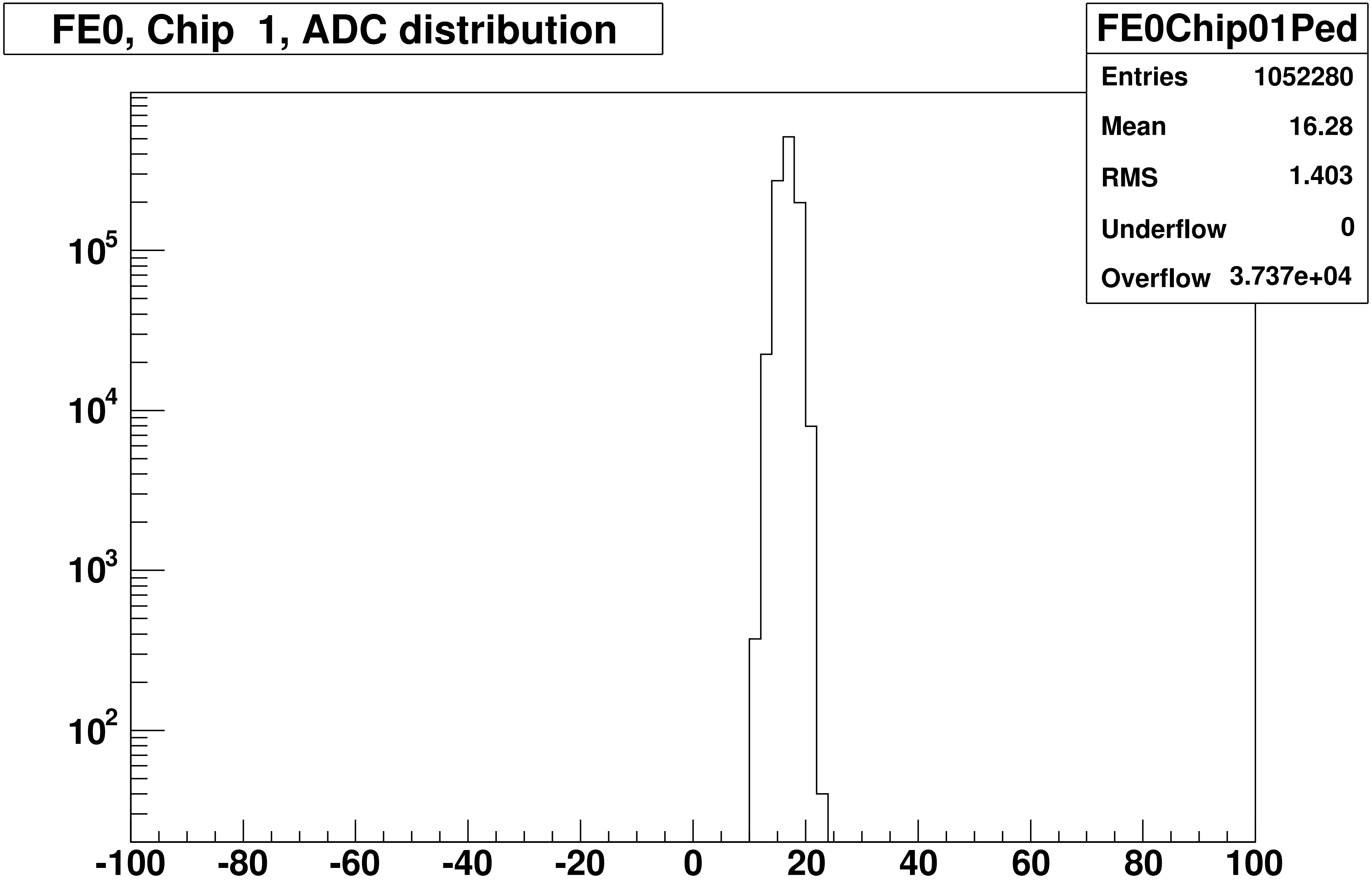

FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 1052280
Mean 16.28
RMS 1.403
Underflow 0
Overflow 3.737e+04
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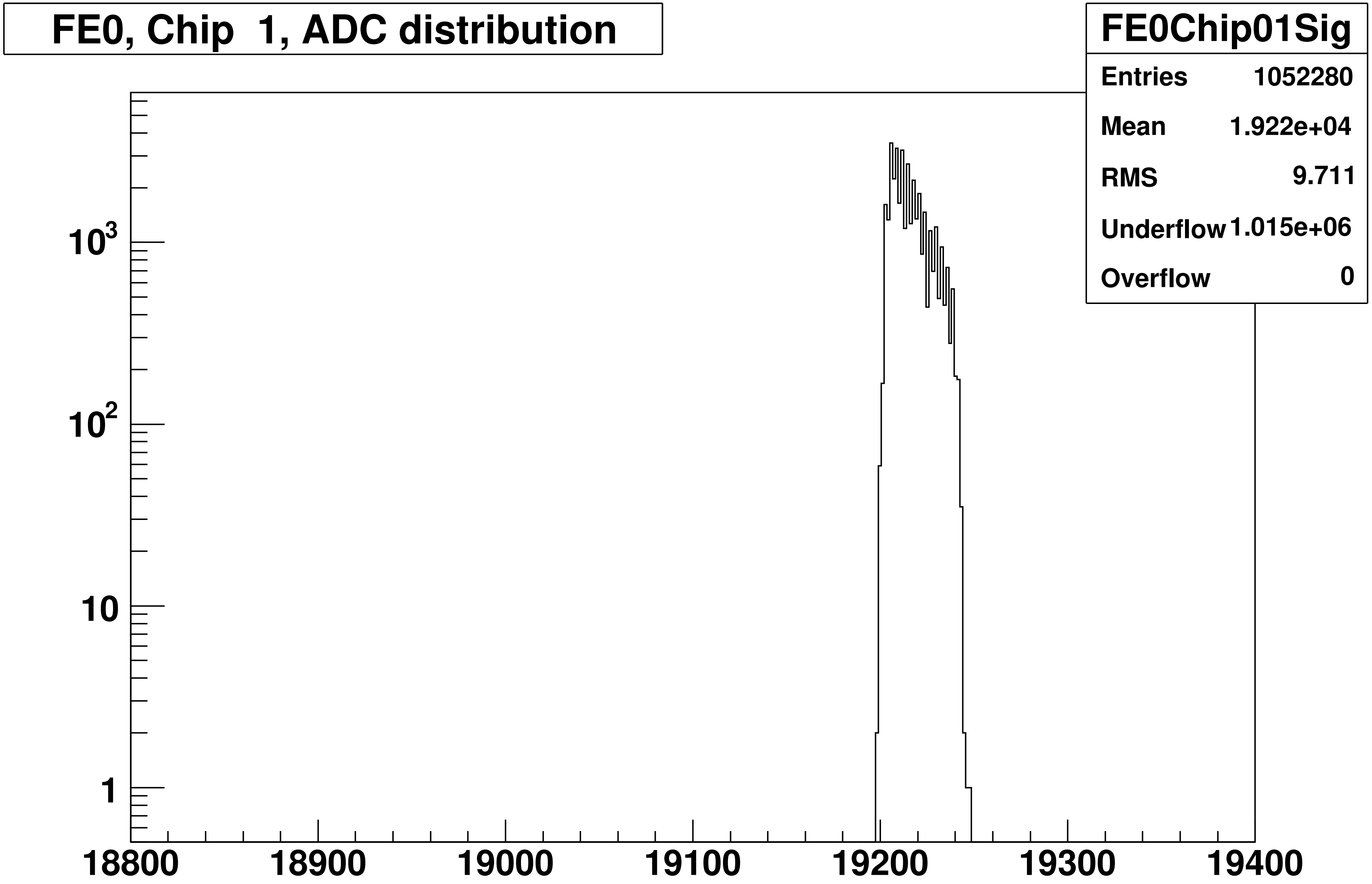
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 1052280
Mean 1.922e+04
RMS 9.711
Underflow 1.015e+06
Overflow 0
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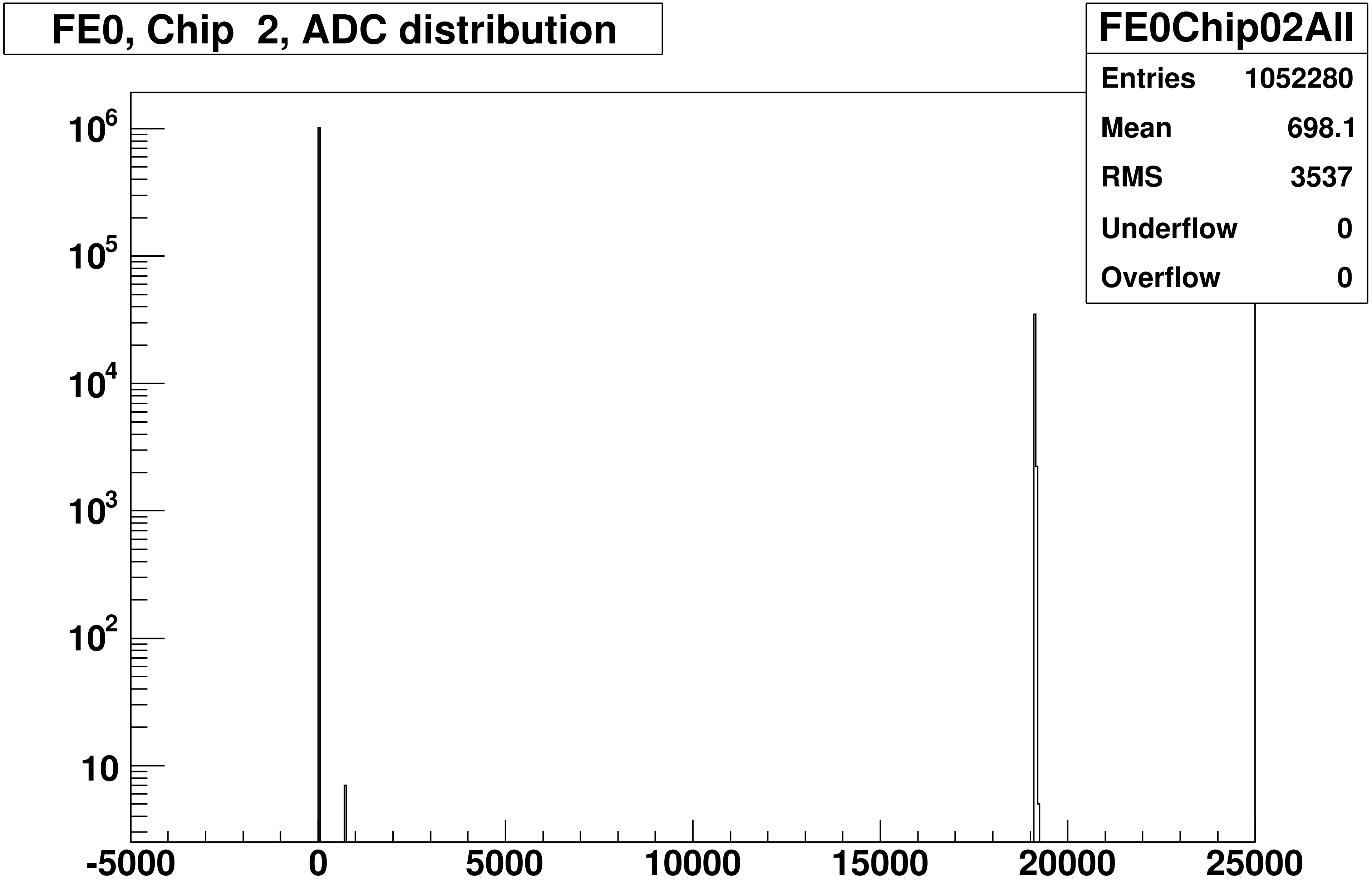

FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 1052280
Mean 698.1
RMS 3537
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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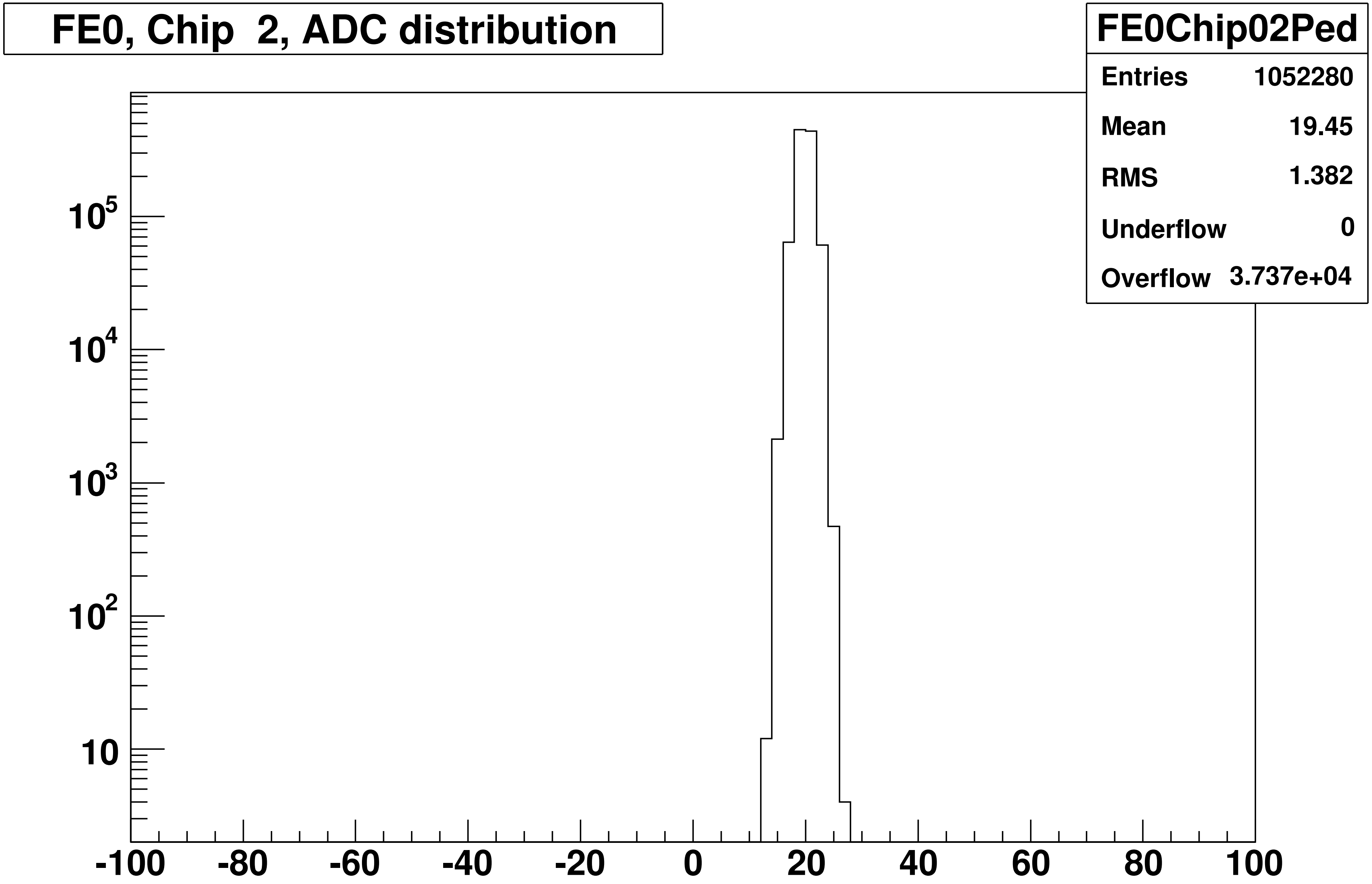
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 1052280
Mean 19.45
RMS 1.382
Underflow 0
Overflow 3.737e+04
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10^2
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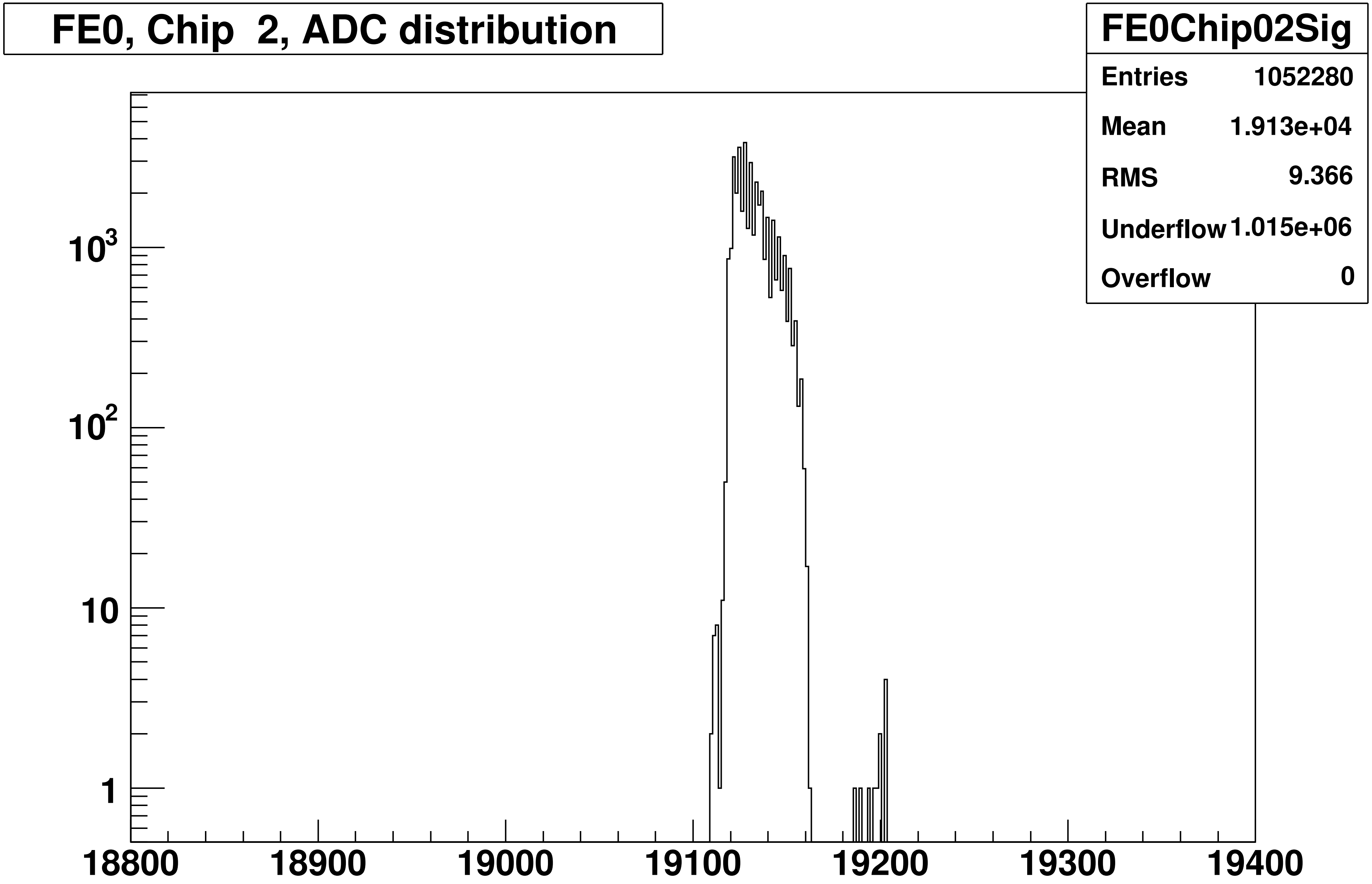
60
80
100


FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 1052280
Mean 1.913e+04
RMS 9.366
Underflow 1.015e+06
Overflow 0
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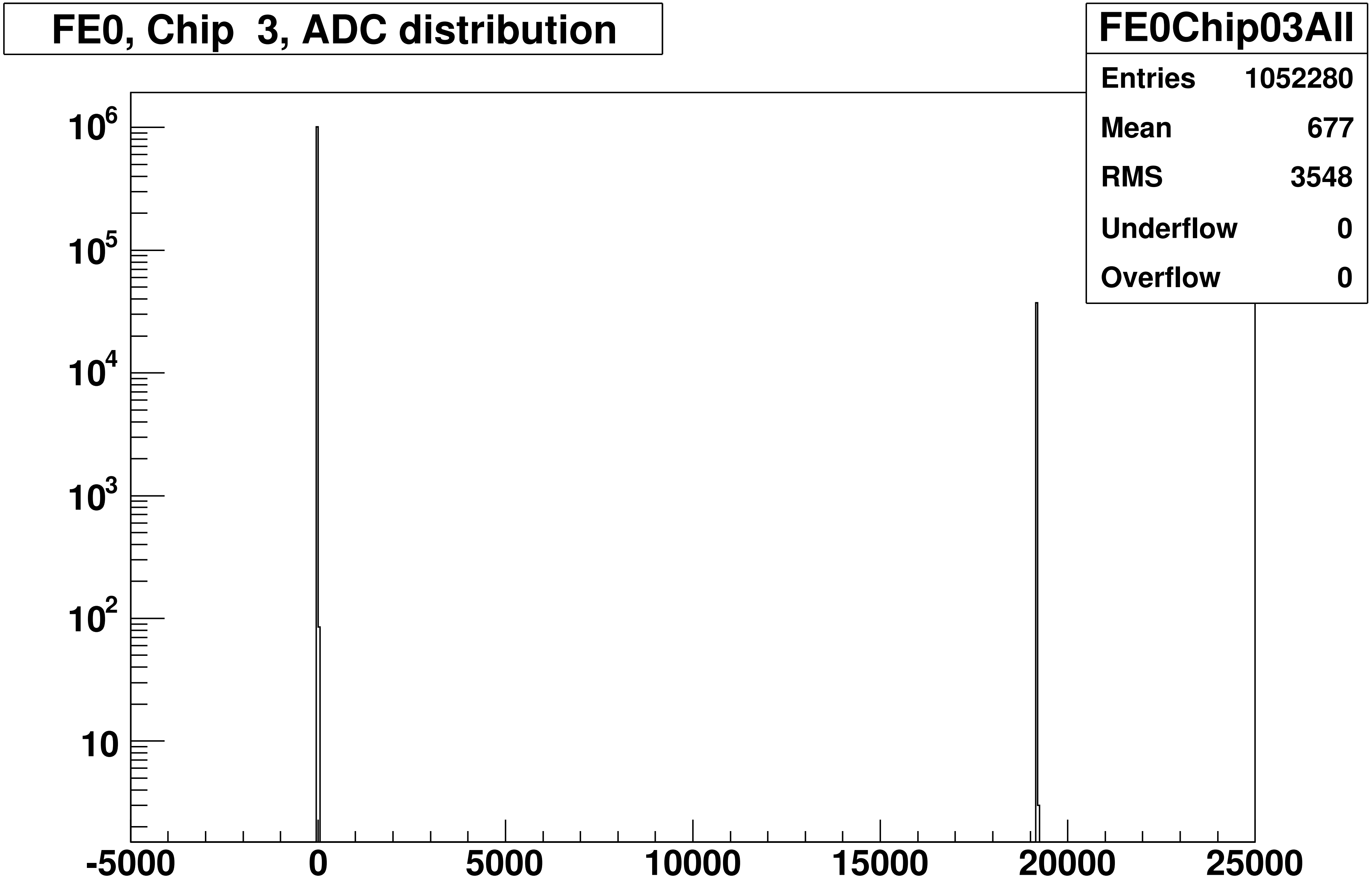
FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 1052280
Mean 677
RMS 3548
Underflow 0
Overflow 0
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10^5
10^4
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10^2
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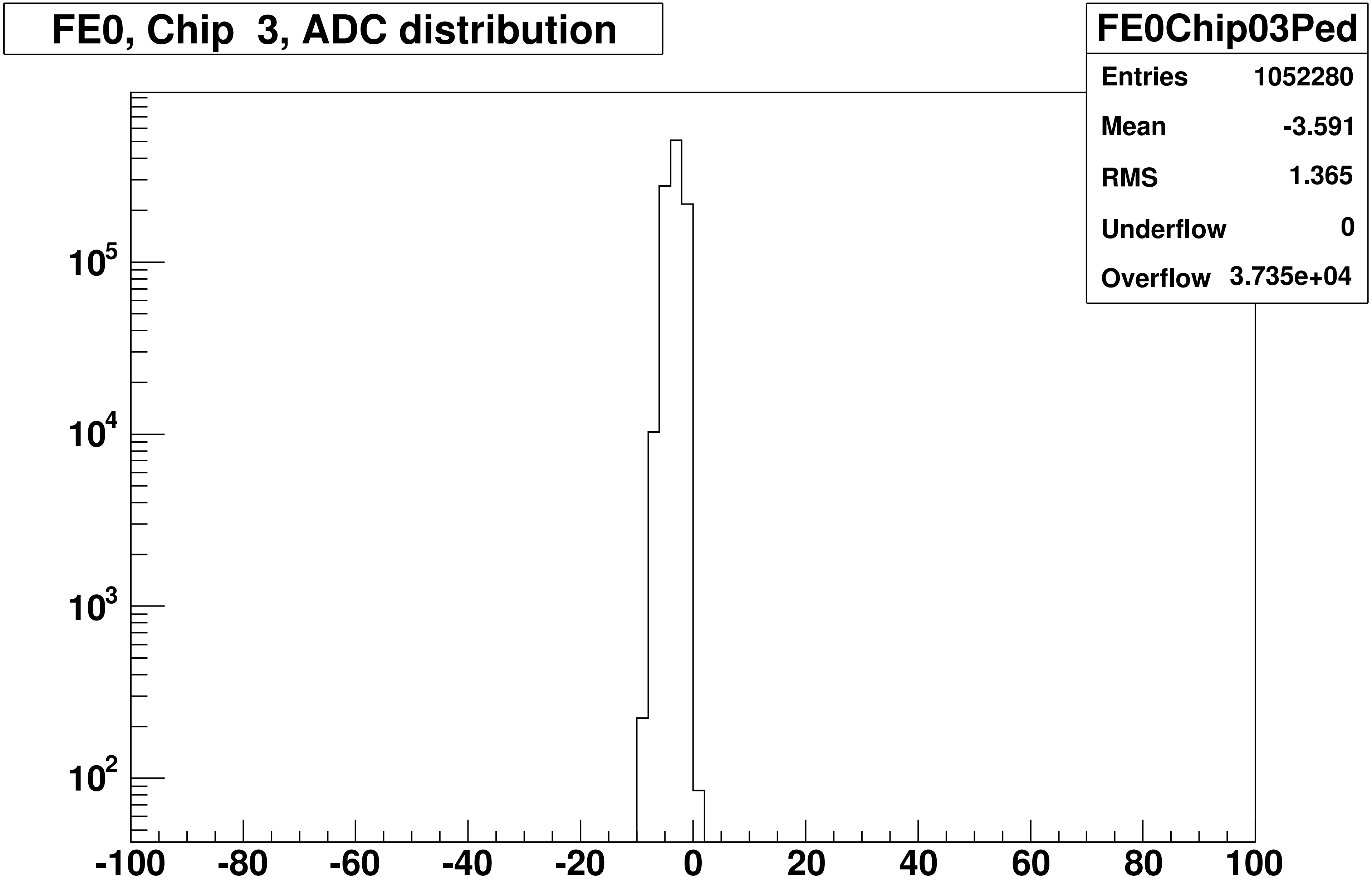
FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 1052280
Mean -3.591
RMS 1.365
Underflow 0
Overflow 3.735e+04
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10^4
10^3
10^2
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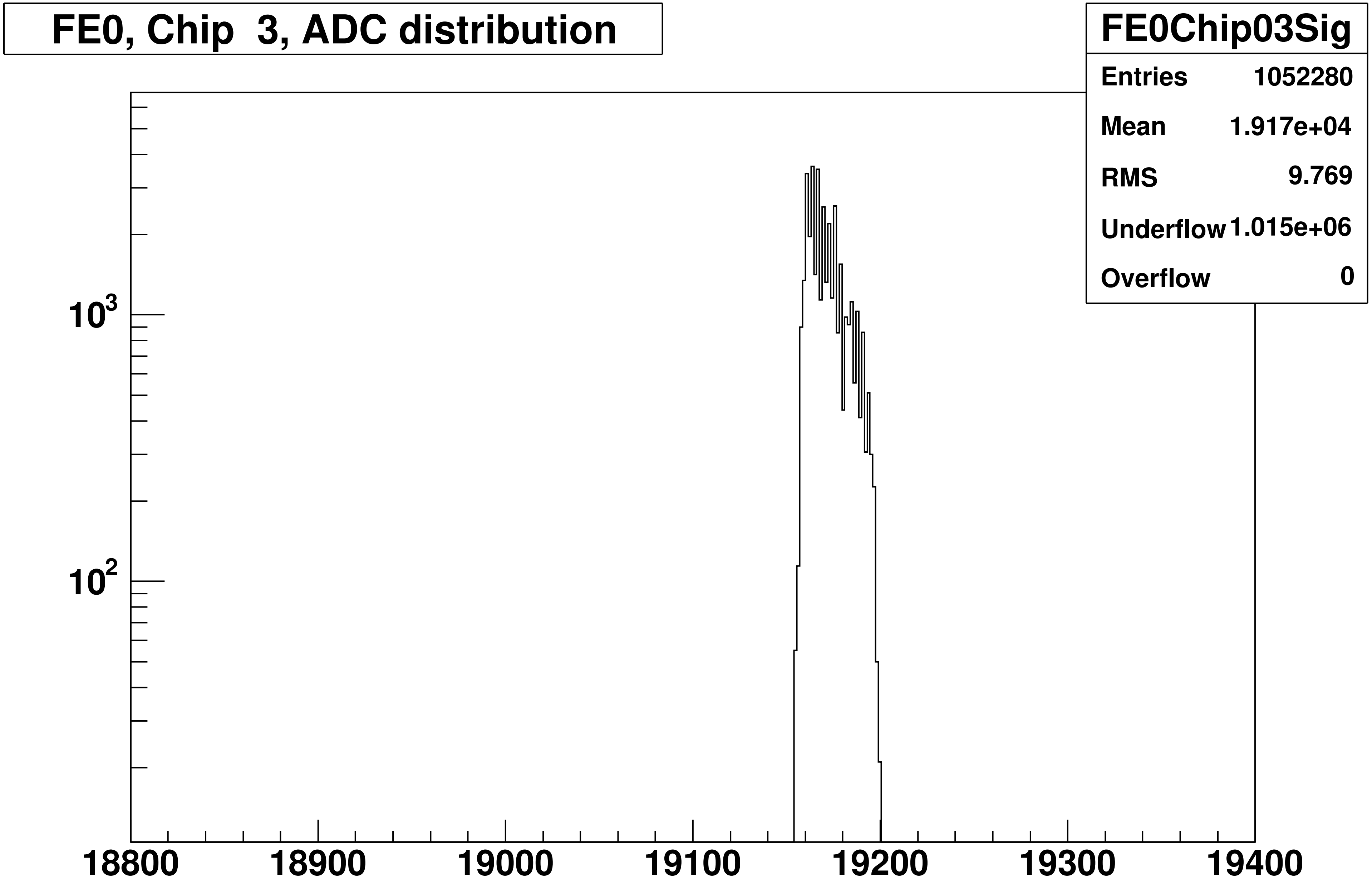
FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 1052280
Mean 1.917e+04
RMS 9.769
Underflow 1.015e+06
Overflow 0
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10^2
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18900
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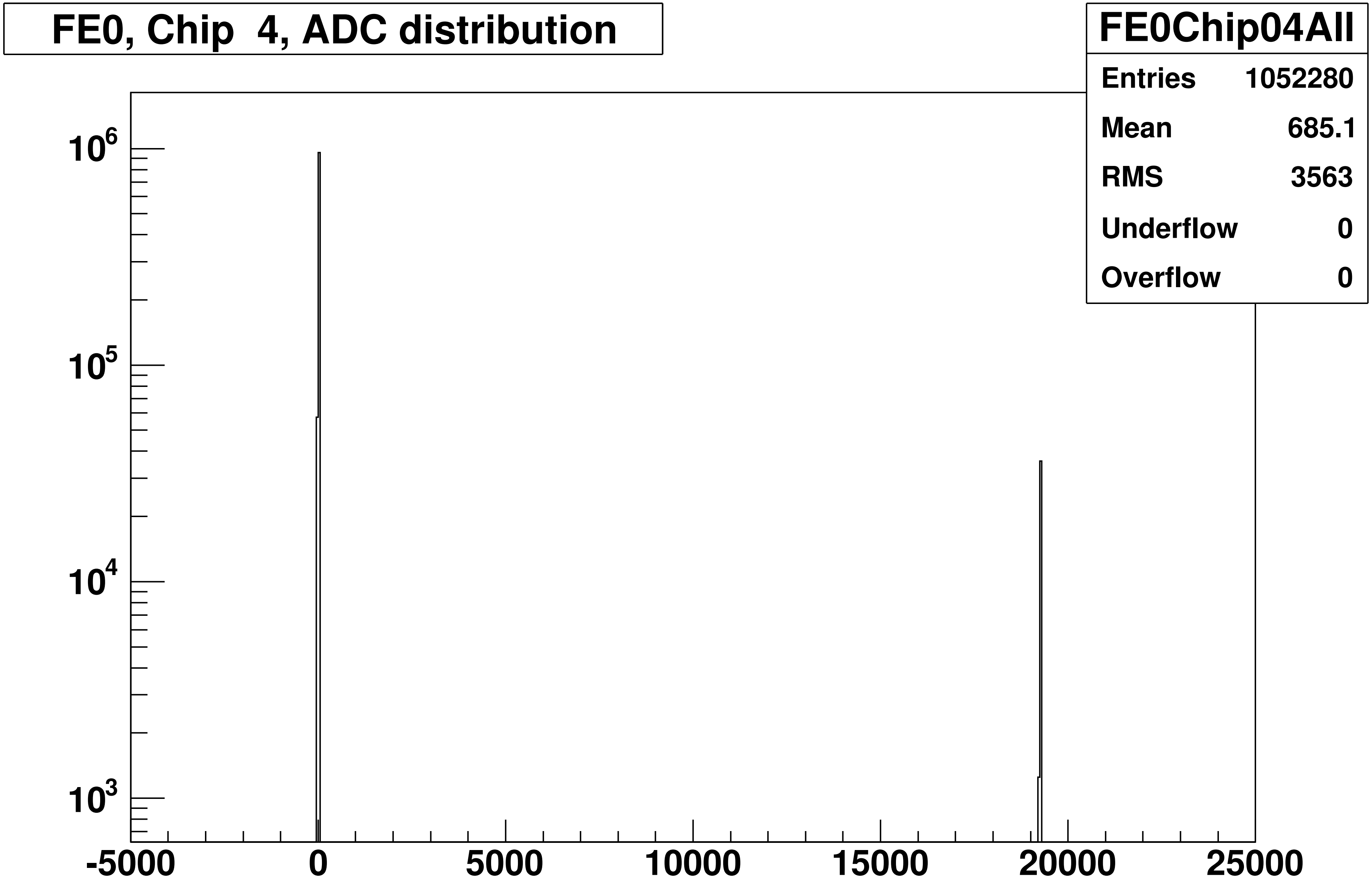
19200
19300
19400


FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 1052280
Mean 685.1
RMS 3563
Underflow 0
Overflow 0
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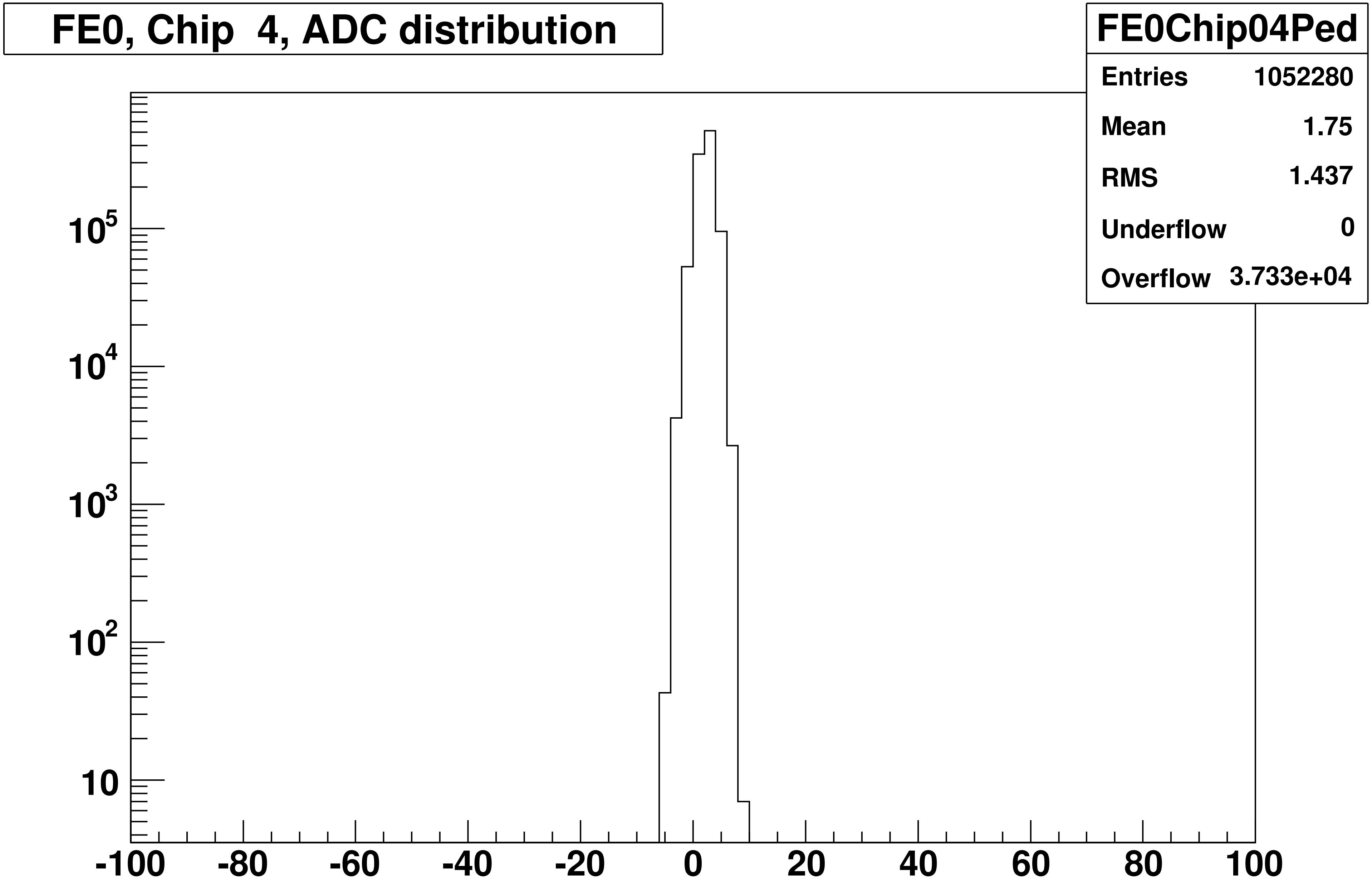
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 1052280
Mean 1.75
RMS 1.437
Underflow 0
Overflow 3.733e+04
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10^3
10^4
10^5
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80
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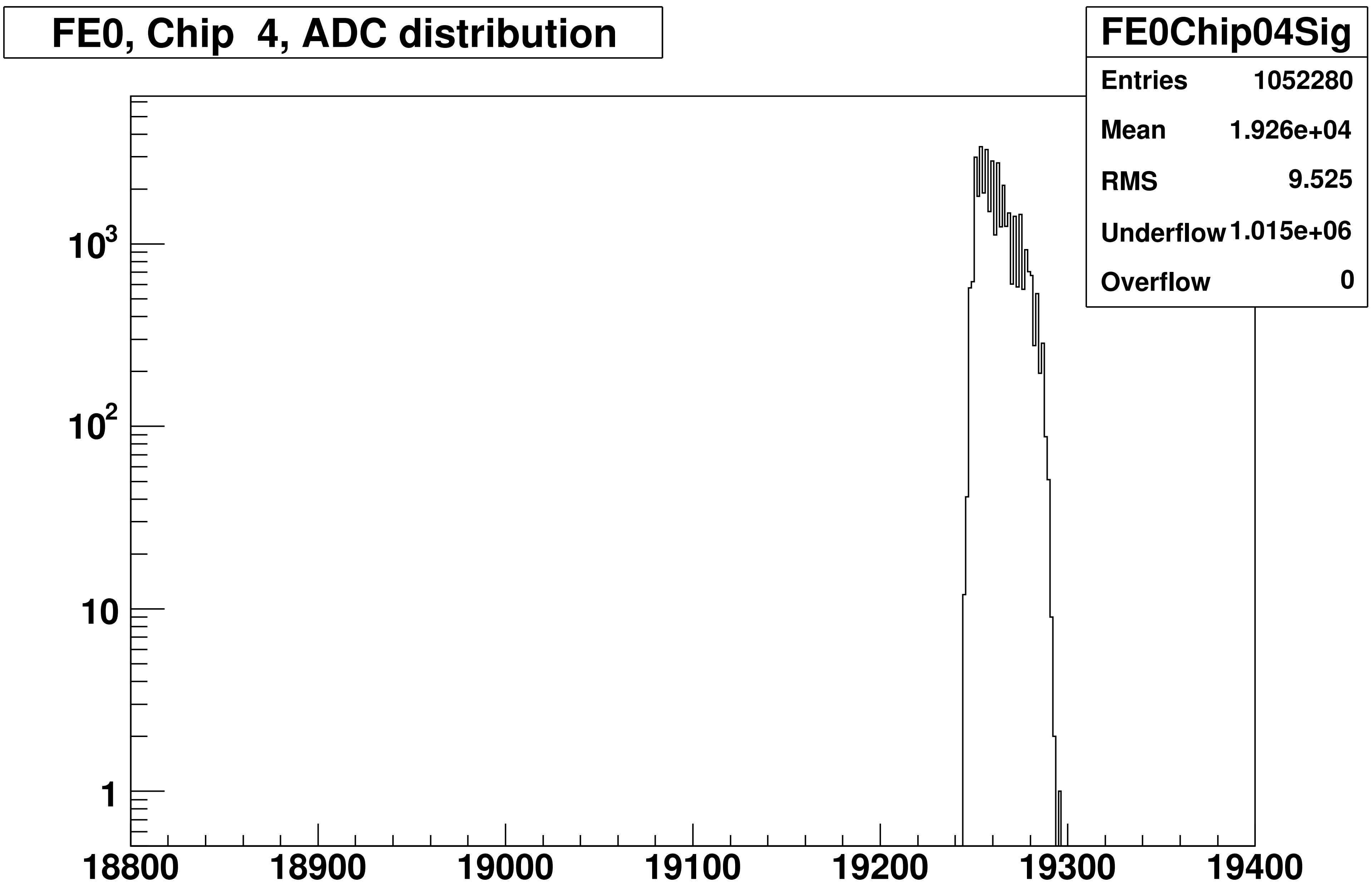

FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 1052280
Mean 1.926e+04
RMS 9.525
Underflow 1.015e+06
Overflow 0
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10^2
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18900
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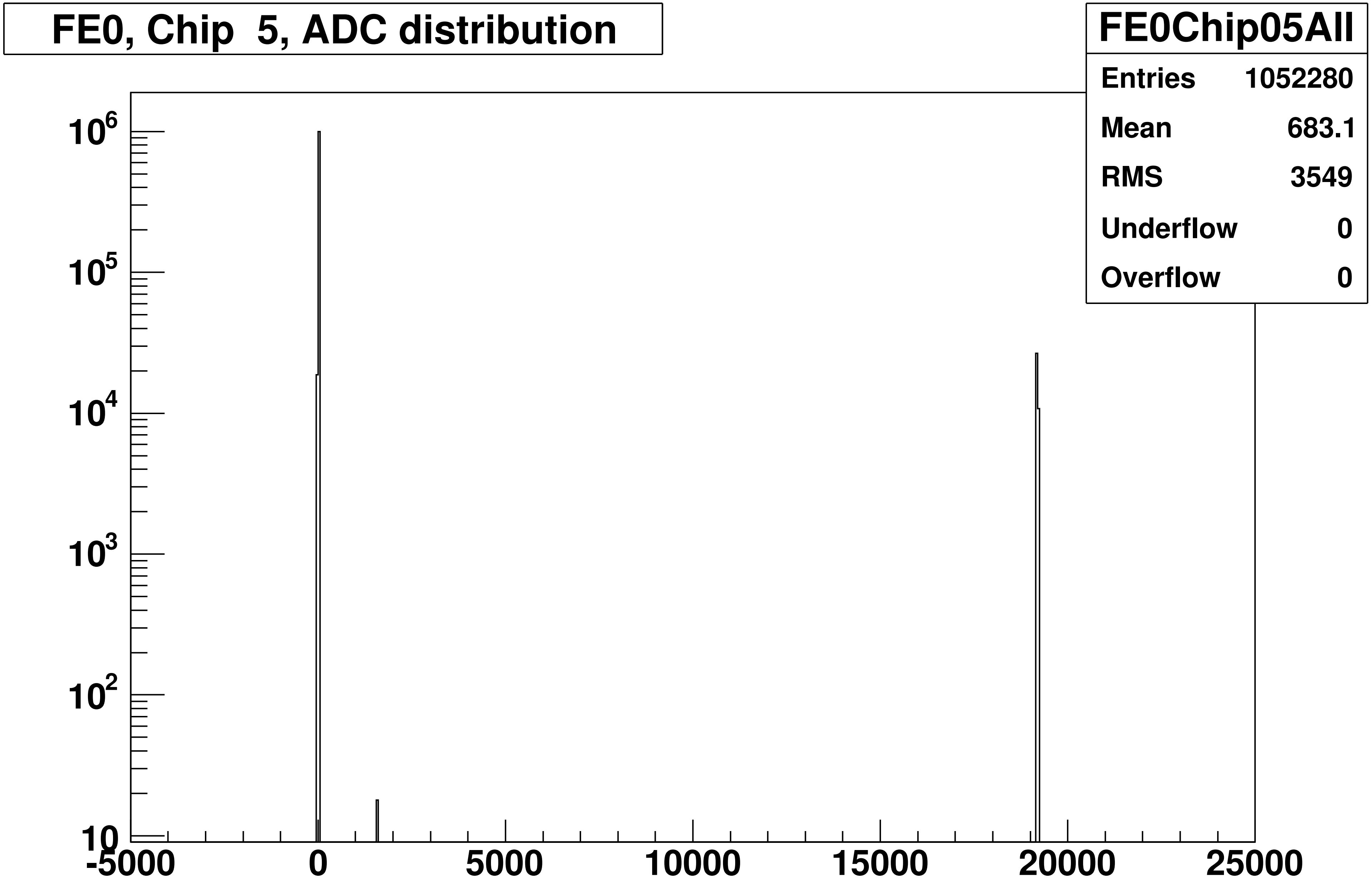
19400


FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 1052280
Mean 683.1
RMS 3549
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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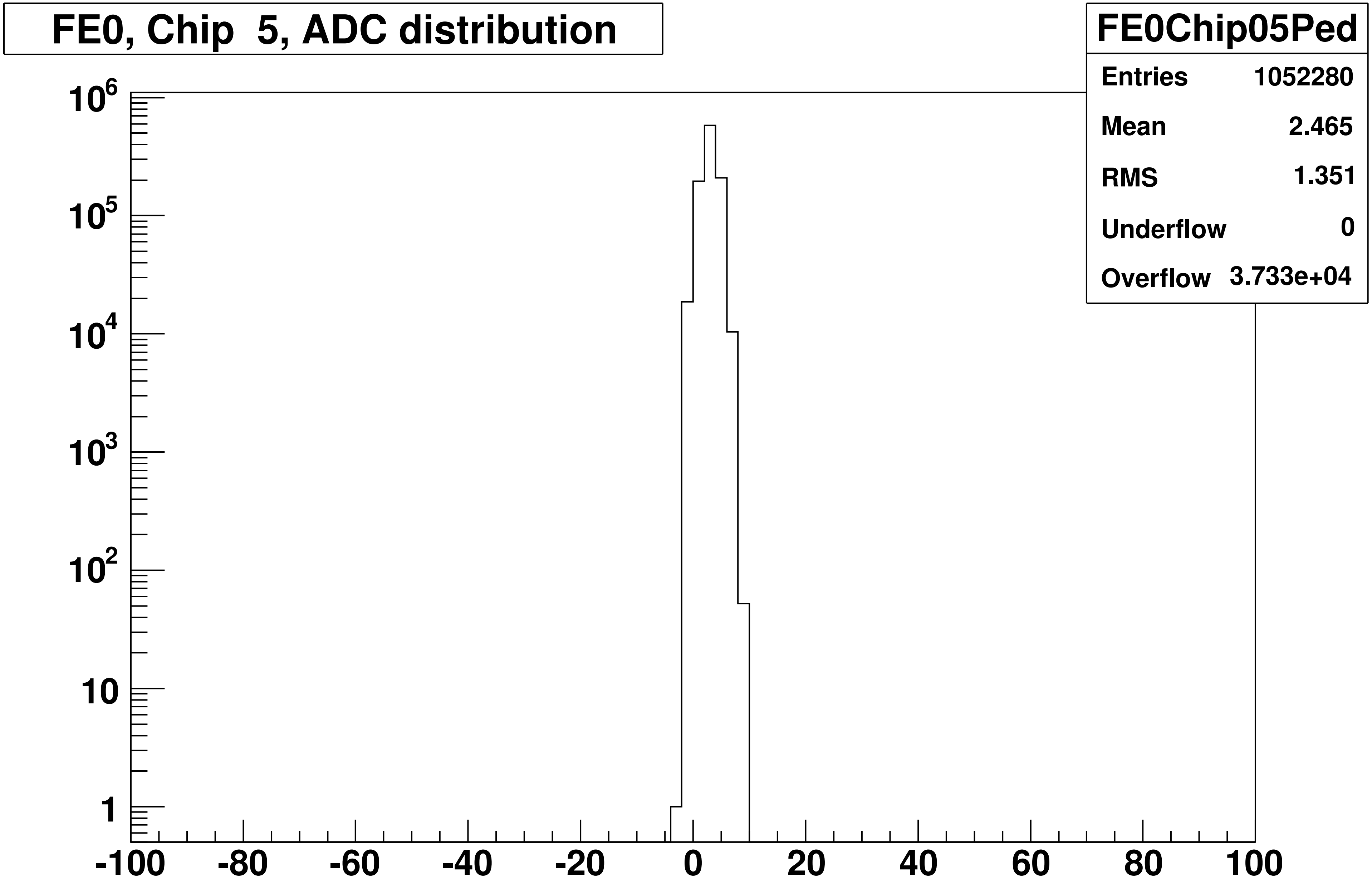
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 1052280
Mean 2.465
RMS 1.351
Underflow 0
Overflow 3.733e+04
10^6
10^5
10^4
10^3
10^2
10
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-100
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-20
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80
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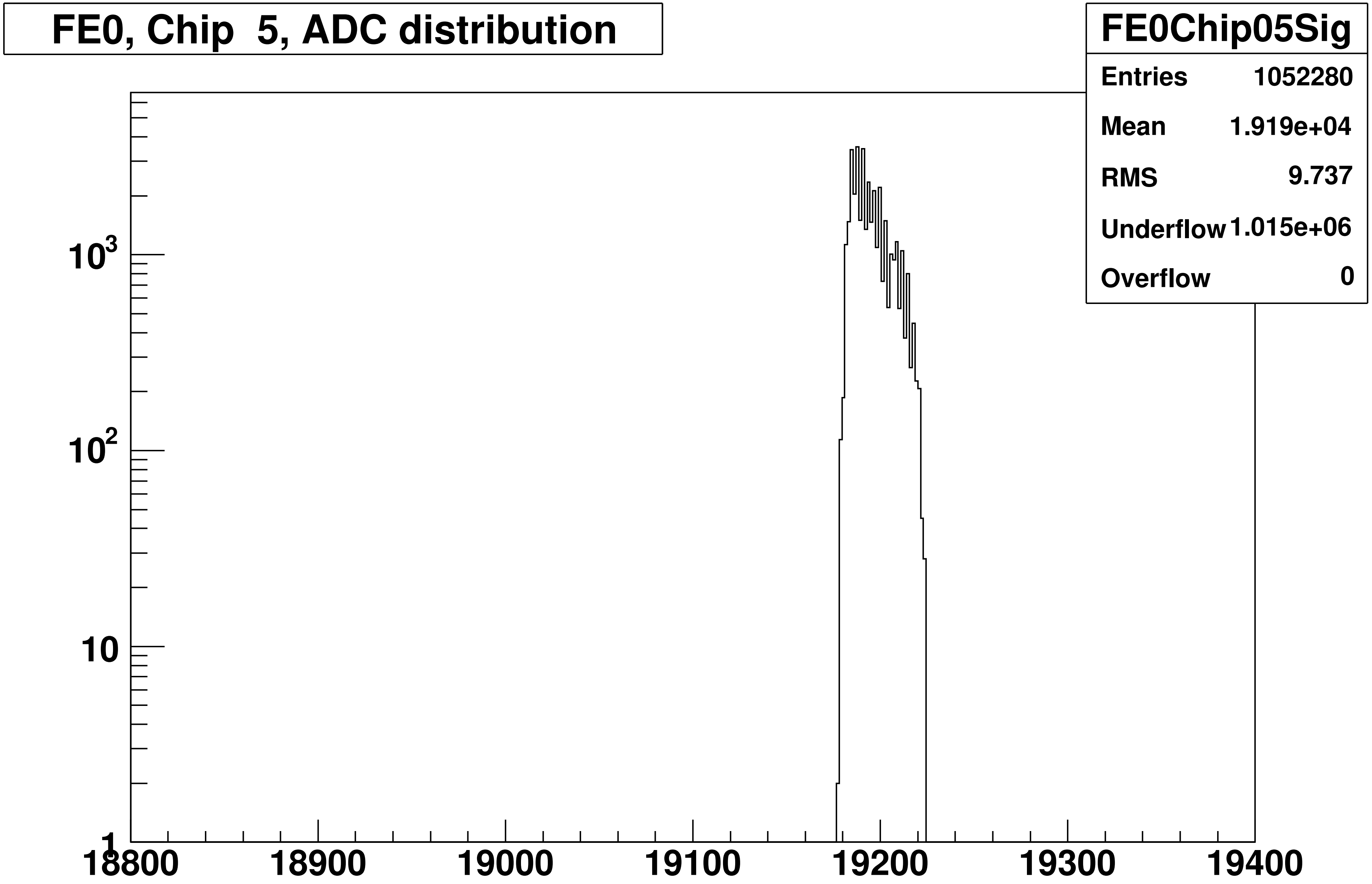
FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 1052280
Mean 1.919e+04
RMS 9.737
Underflow 1.015e+06
Overflow 0
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10^2
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18900
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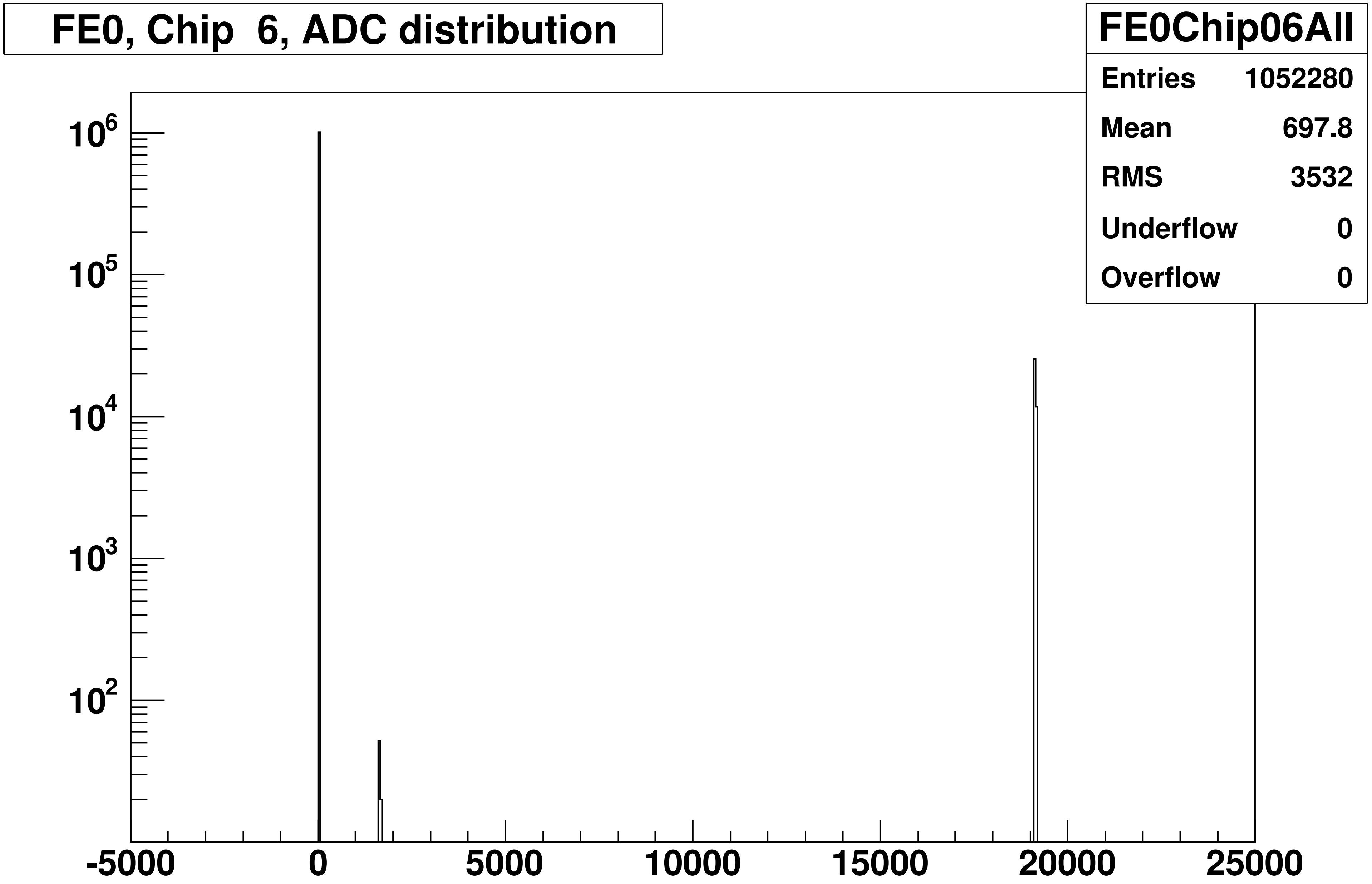
19200
19300
19400


FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 1052280
Mean 697.8
RMS 3532
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
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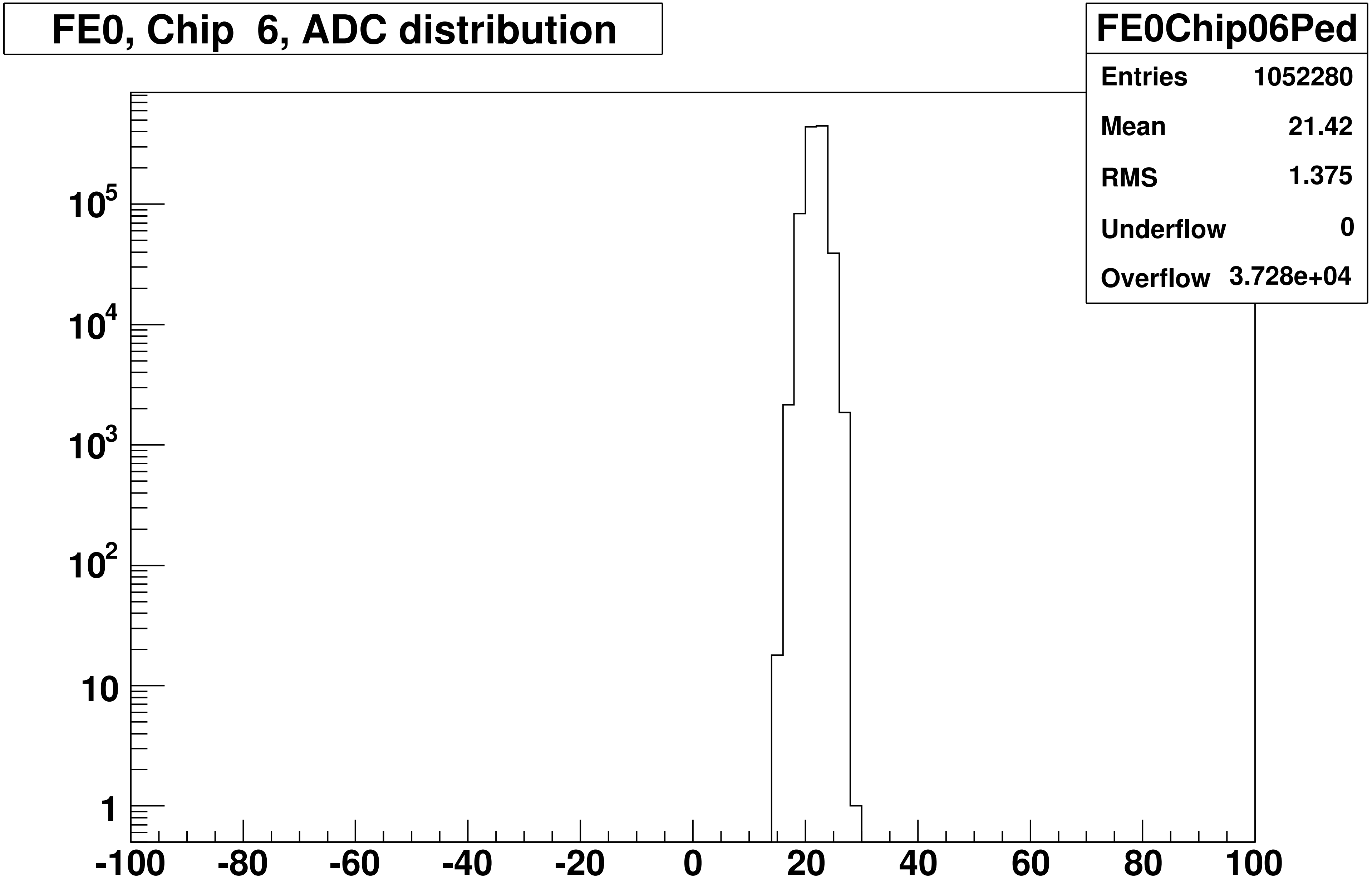
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 1052280
Mean 21.42
RMS 1.375
Underflow 0
Overflow 3.728e+04
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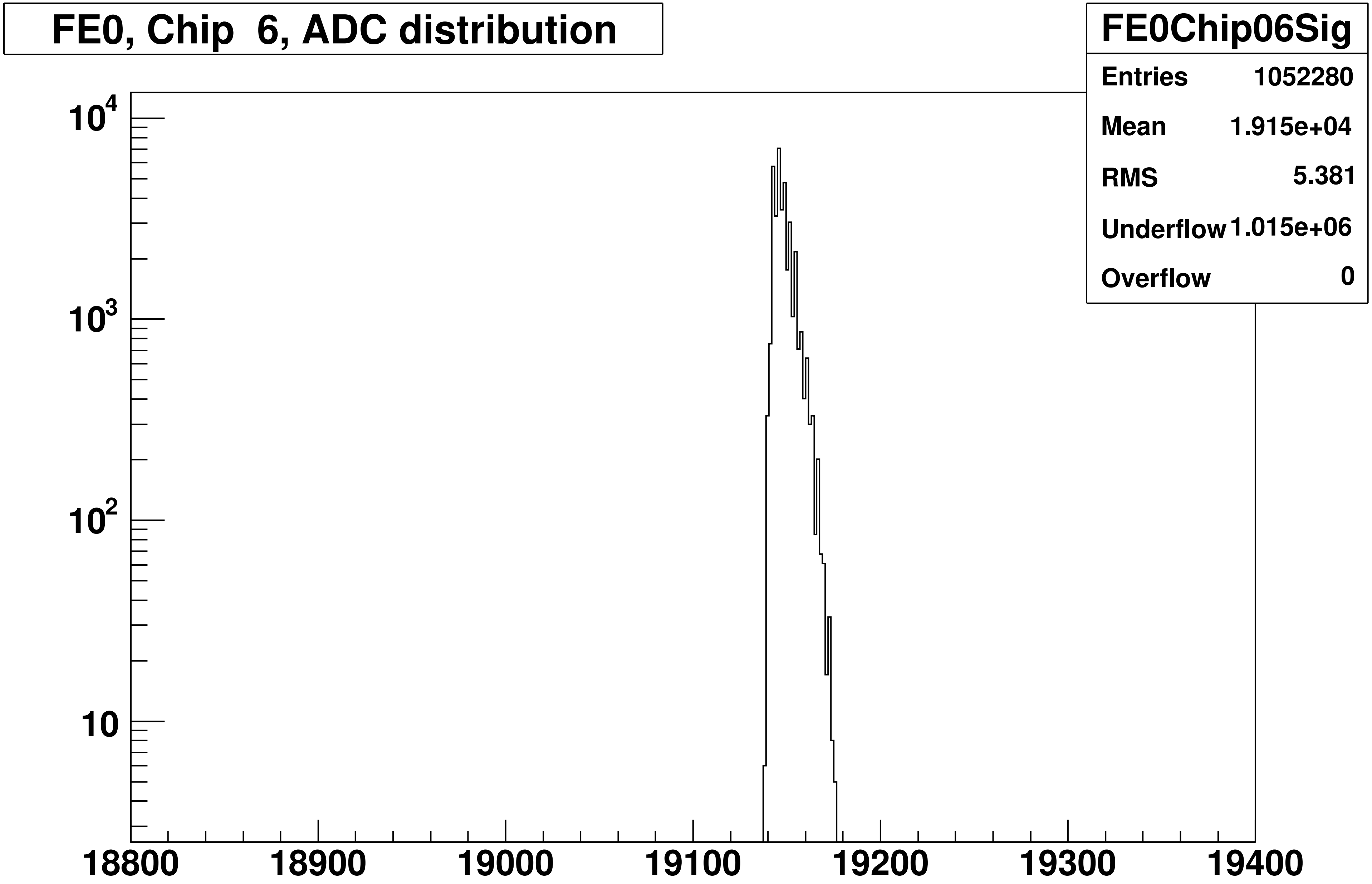
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 1052280
Mean 1.915e+04
RMS 5.381
Underflow 1.015e+06
Overflow 0
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10^3
10^2
10
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19200
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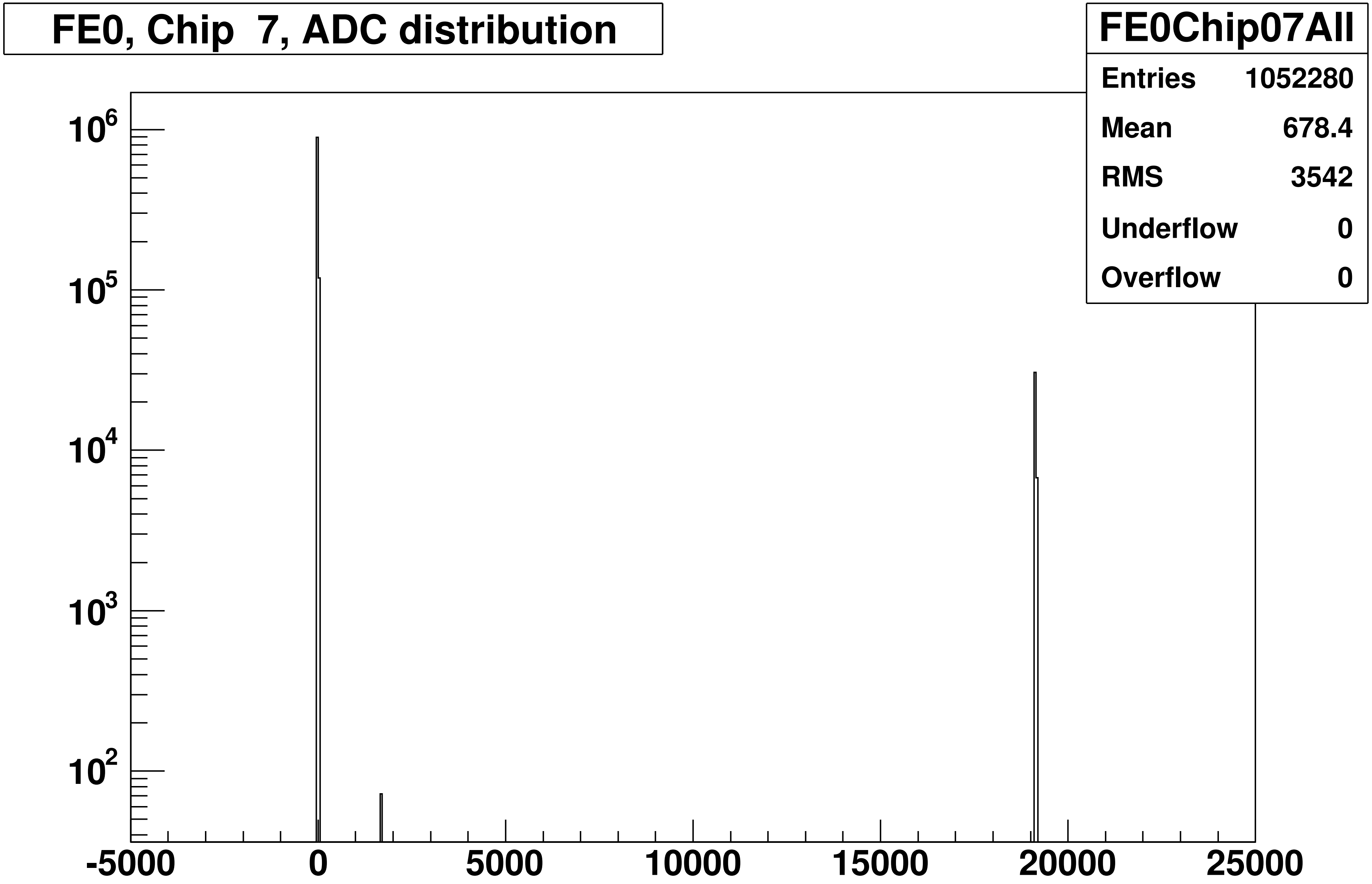
FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 1052280
Mean 678.4
RMS 3542
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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15000
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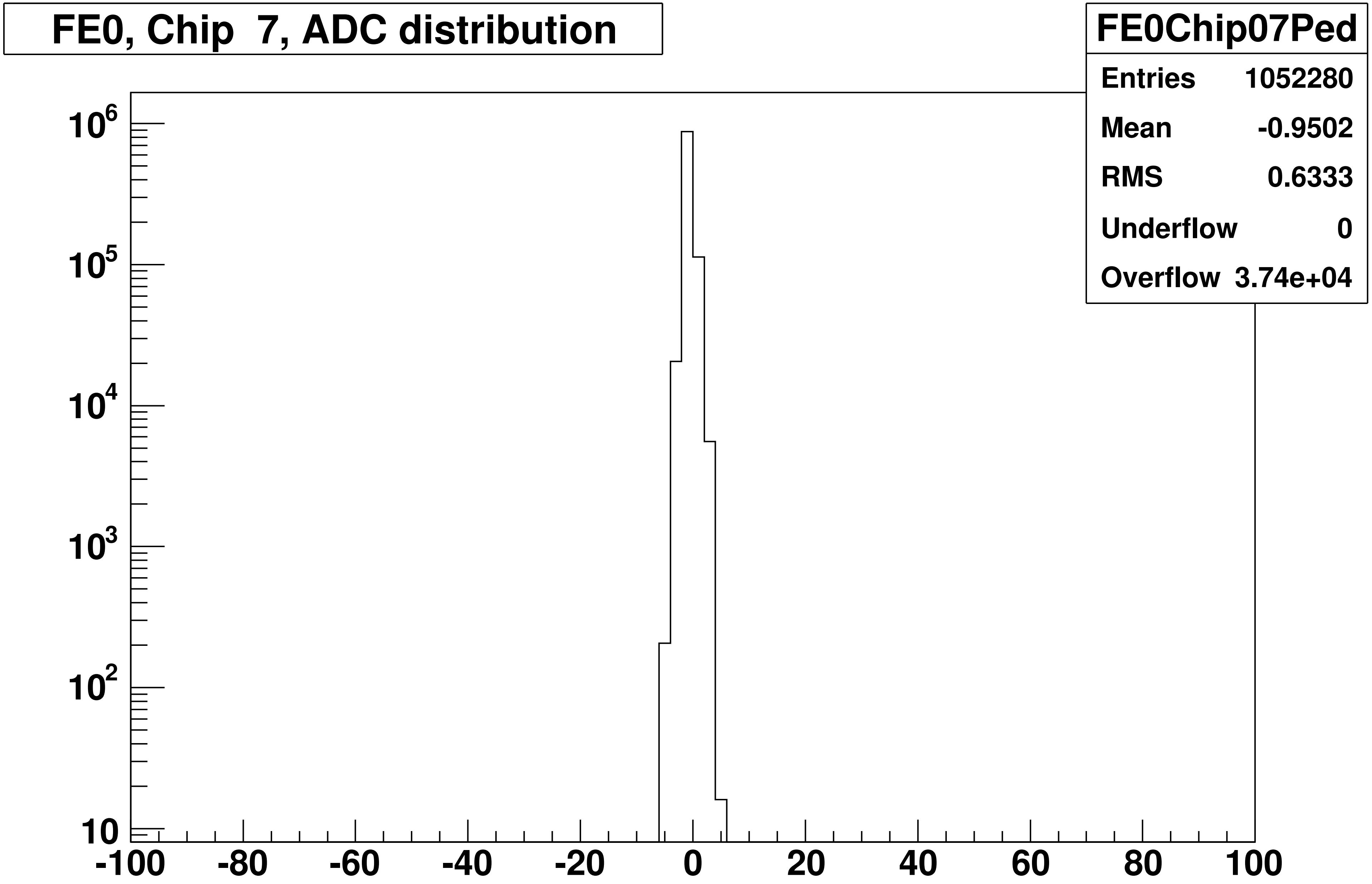
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 1052280
Mean -0.9502
RMS 0.6333
Underflow 0
Overflow 3.74e+04
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10^4
10^3
10^2
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-100
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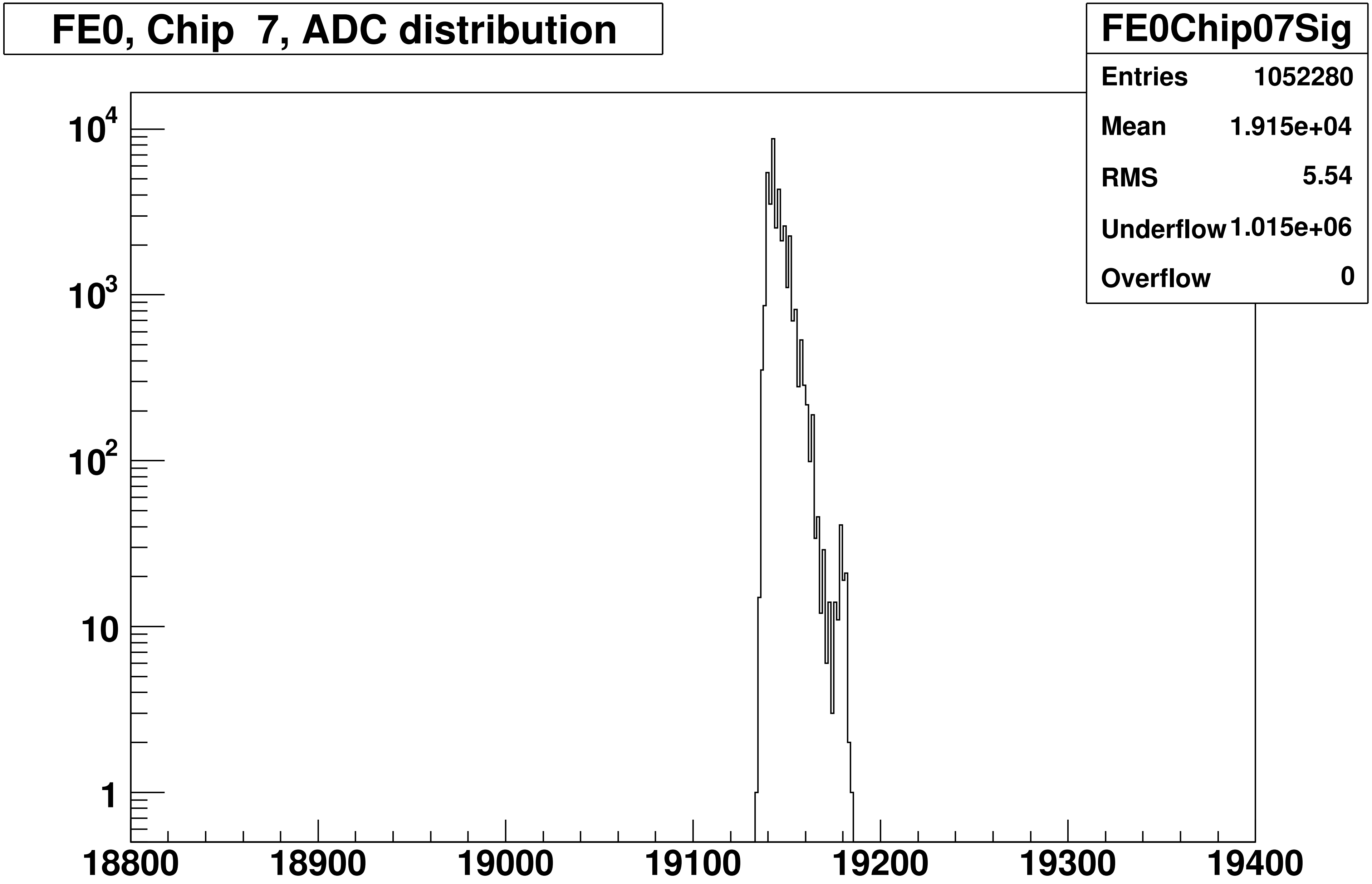
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 1052280
Mean 1.915e+04
RMS 5.54
Underflow 1.015e+06
Overflow 0
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10^3
10^2
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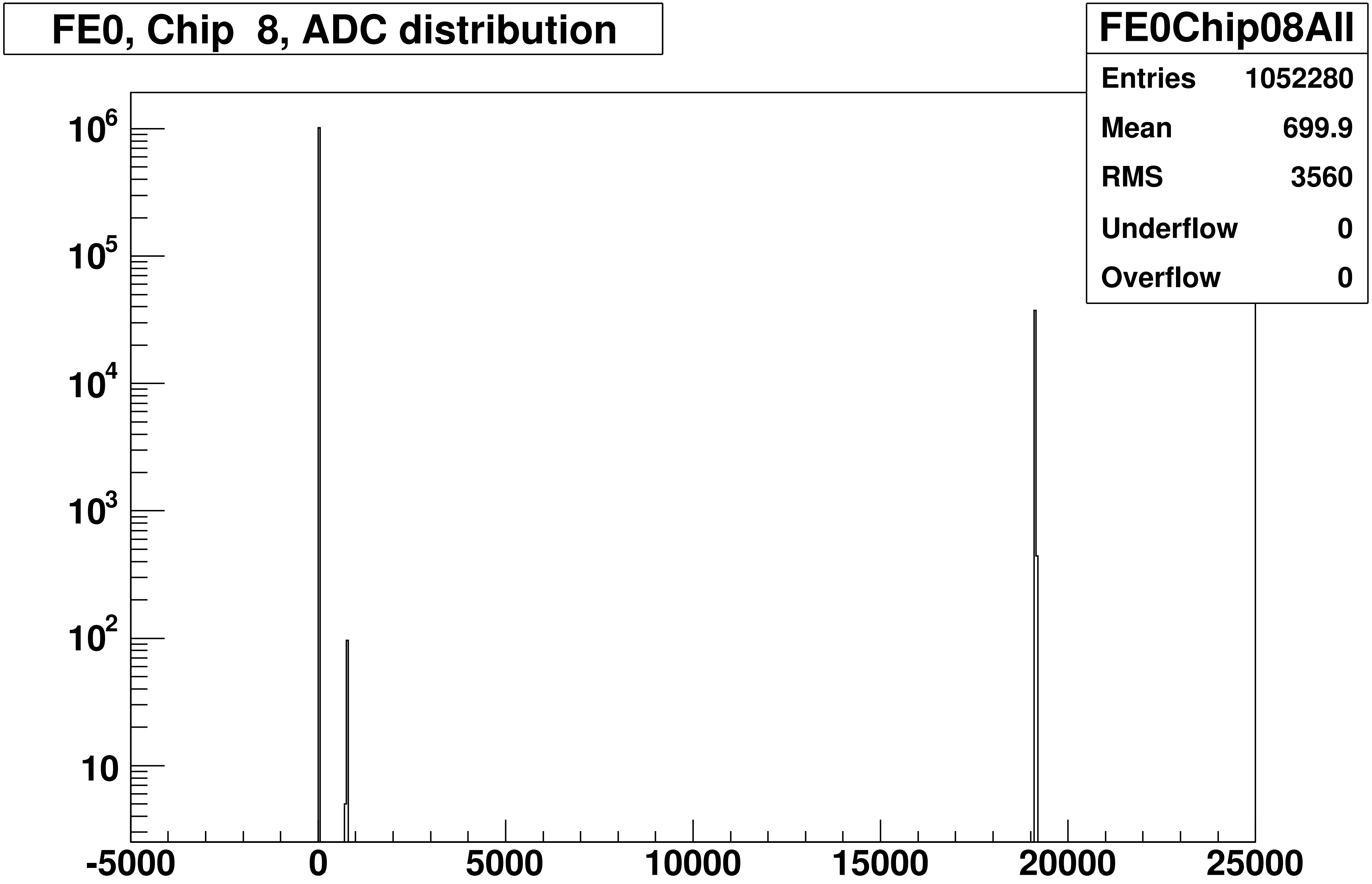

FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 1052280
Mean 699.9
RMS 3560
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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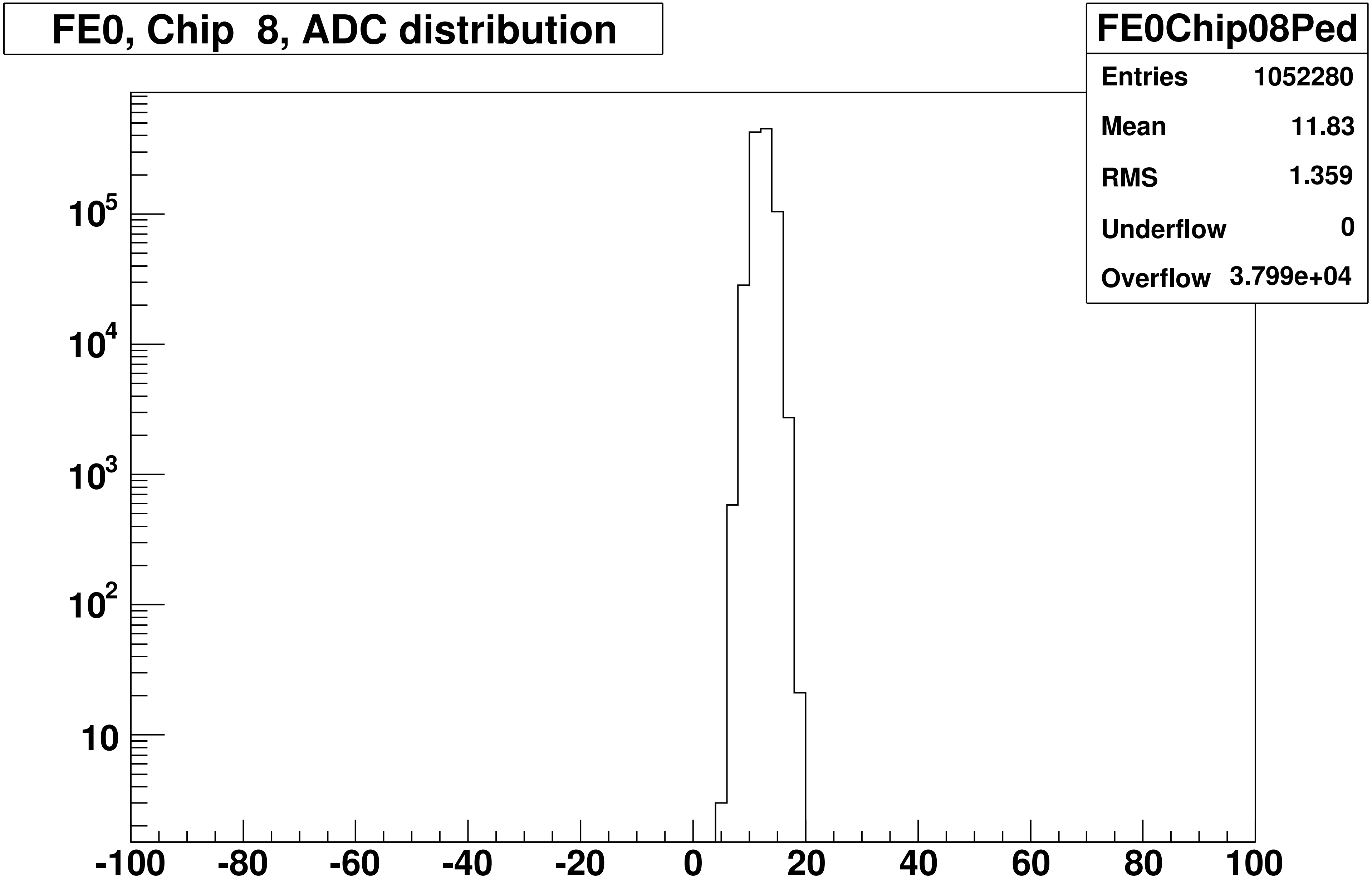
FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 1052280
Mean 11.83
RMS 1.359
Underflow 0
Overflow 3.799e+04
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10^4
10^3
10^2
10
-100
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-60
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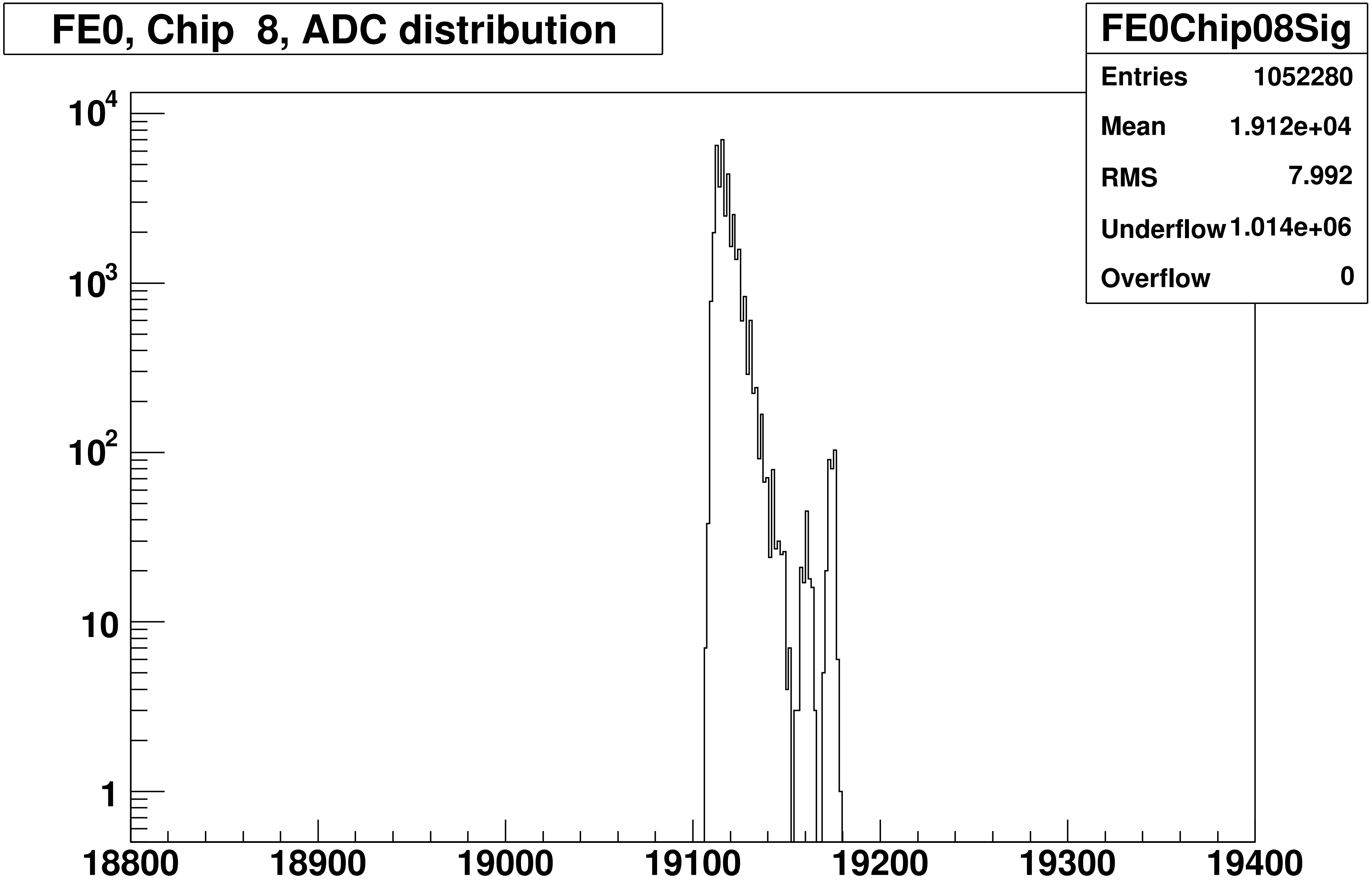
FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 1052280
Mean 1.912e+04
RMS 7.992
Underflow 1.014e+06
Overflow 0
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10^3
10^2
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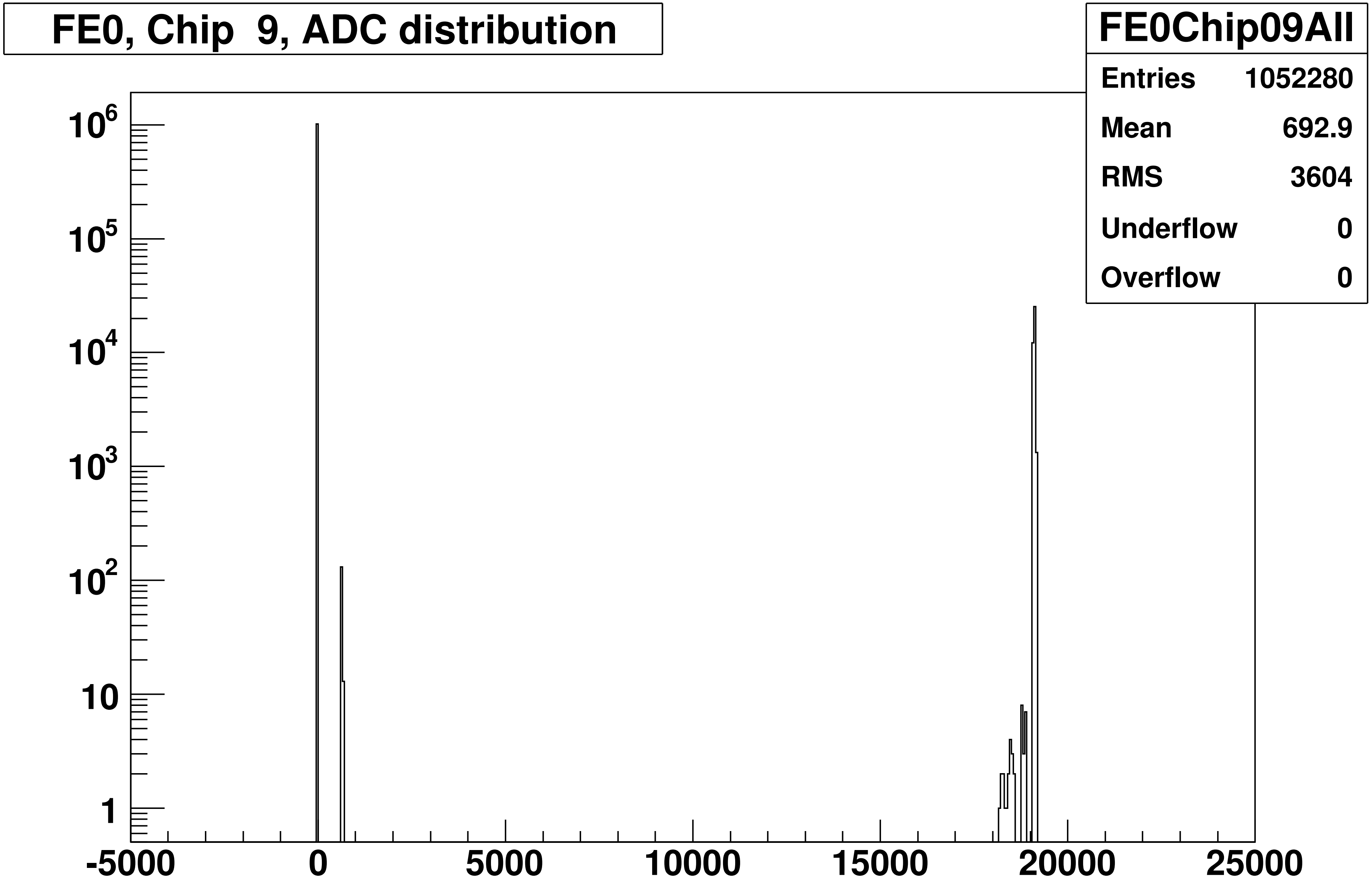
FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 1052280
Mean 692.9
RMS 3604
Underflow 0
Overflow 0
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10^4
10^3
10^2
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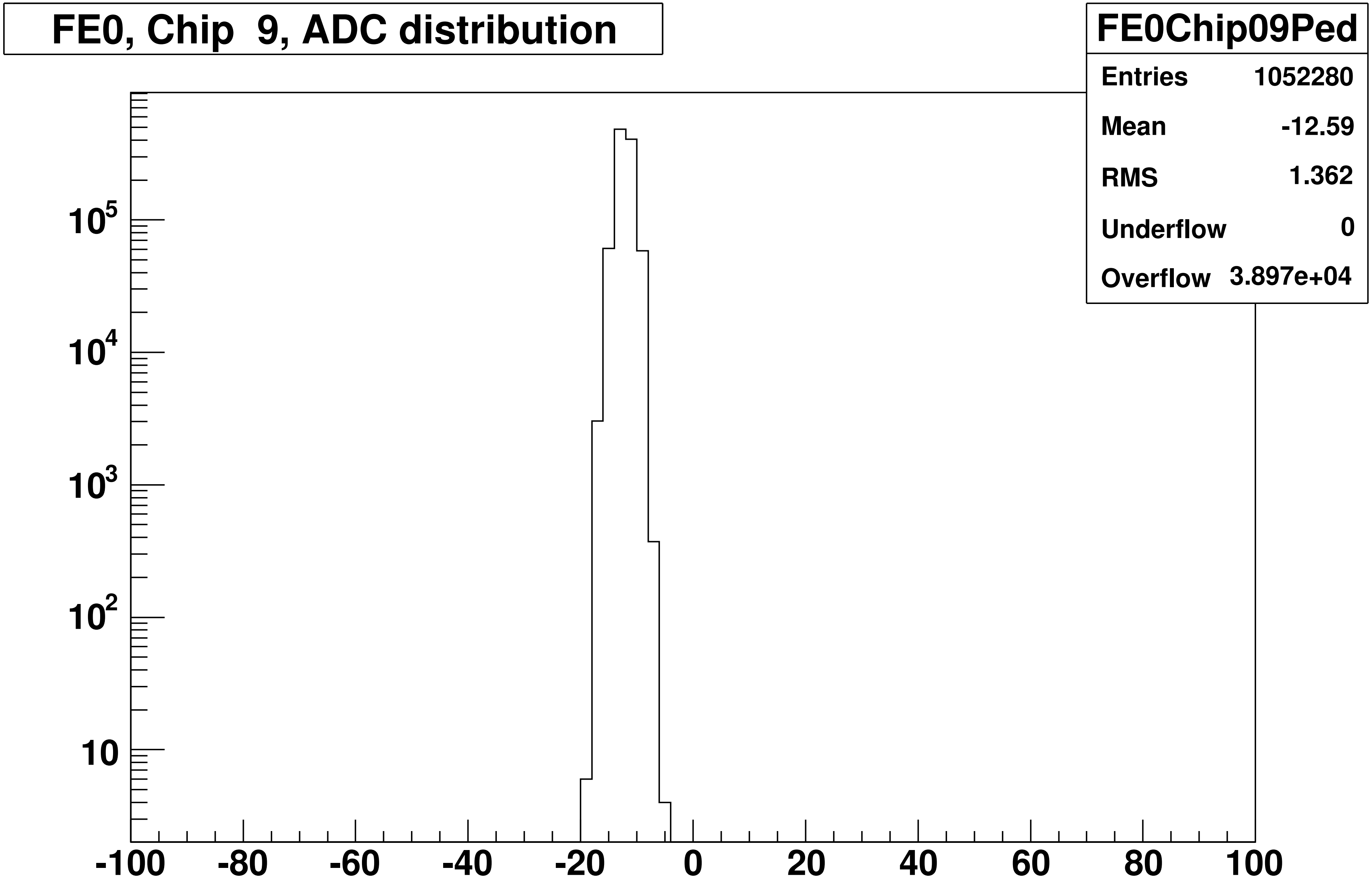

FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 1052280
Mean -12.59
RMS 1.362
Underflow 0
Overflow 3.897e+04
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10^3
10^4
10^5
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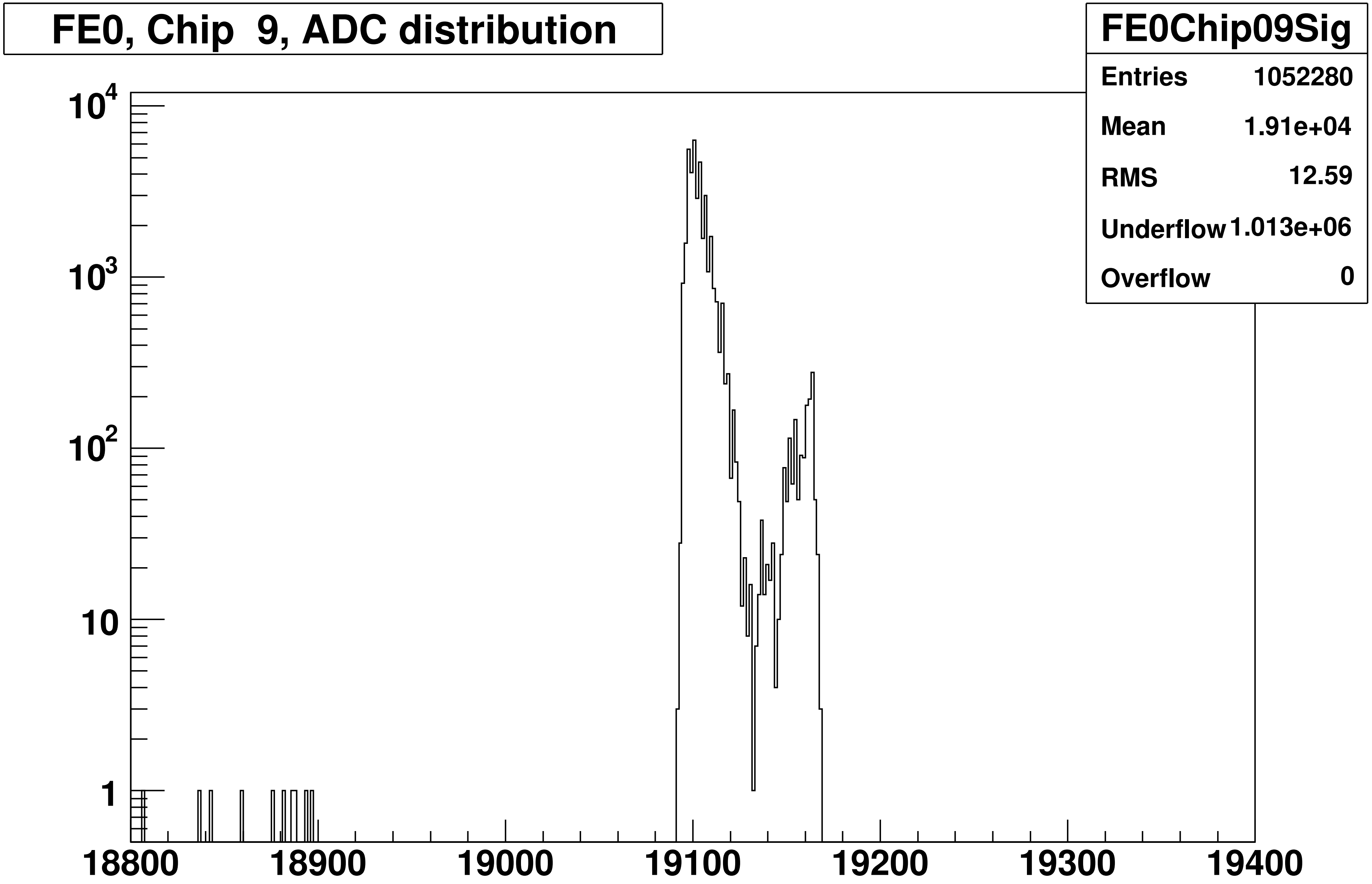
FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 1052280
Mean 1.91e+04
RMS 12.59
Underflow 1.013e+06
Overflow 0
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10^3
10^2
10
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18900
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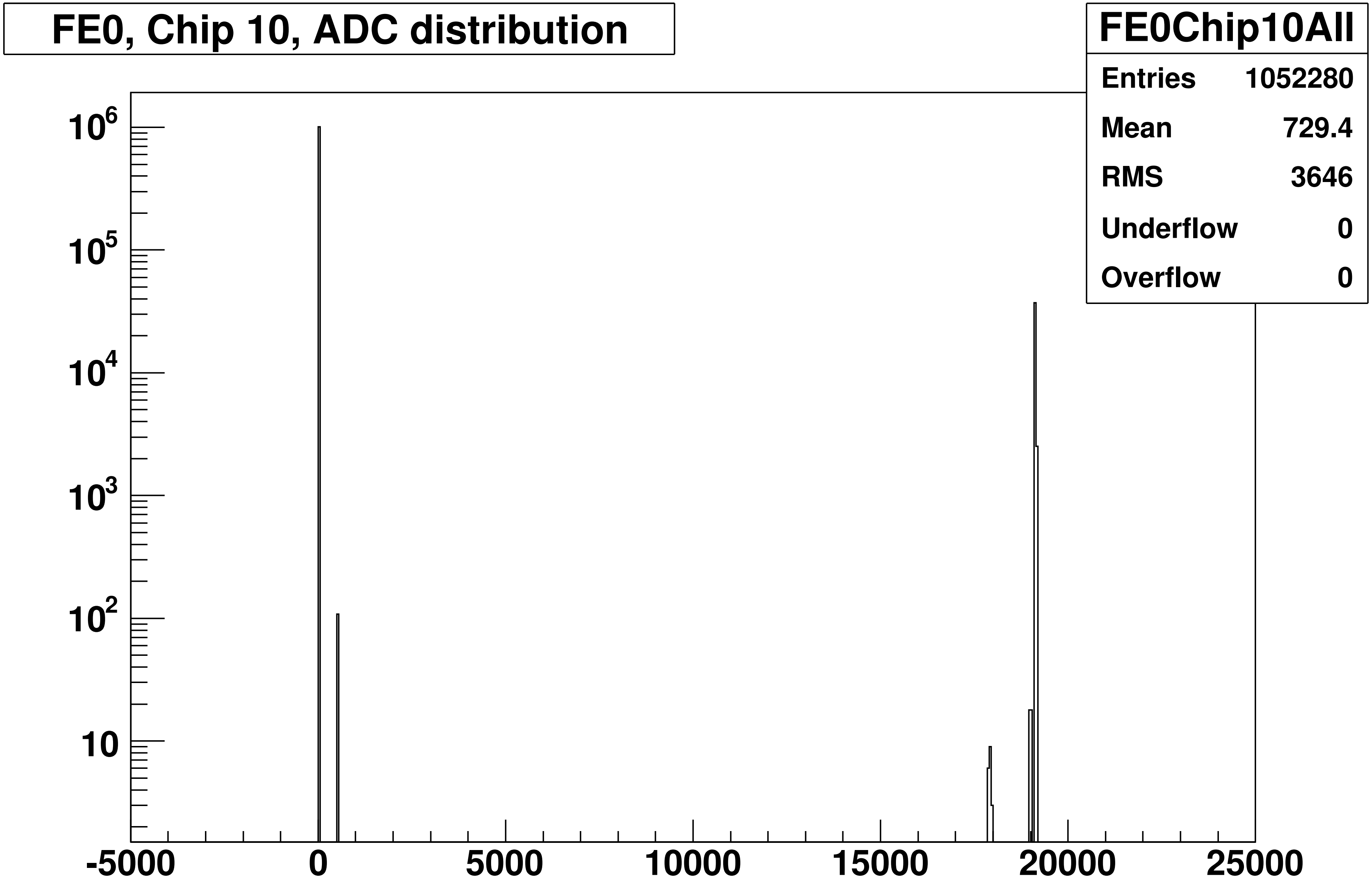

FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 1052280
Mean 729.4
RMS 3646
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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10000
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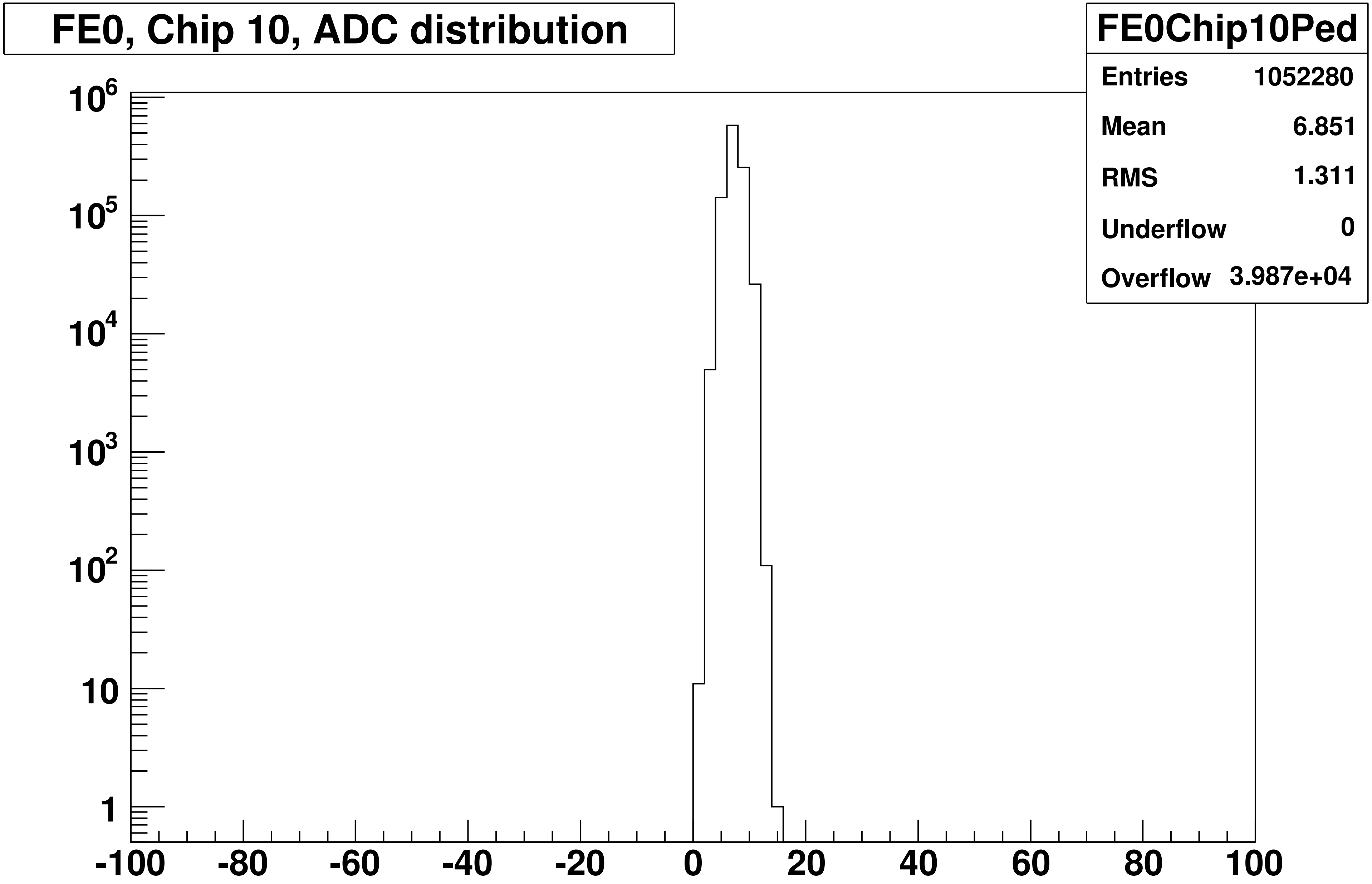
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 1052280
Mean 6.851
RMS 1.311
Underflow 0
Overflow 3.987e+04
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10^5
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10^3
10^2
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-20
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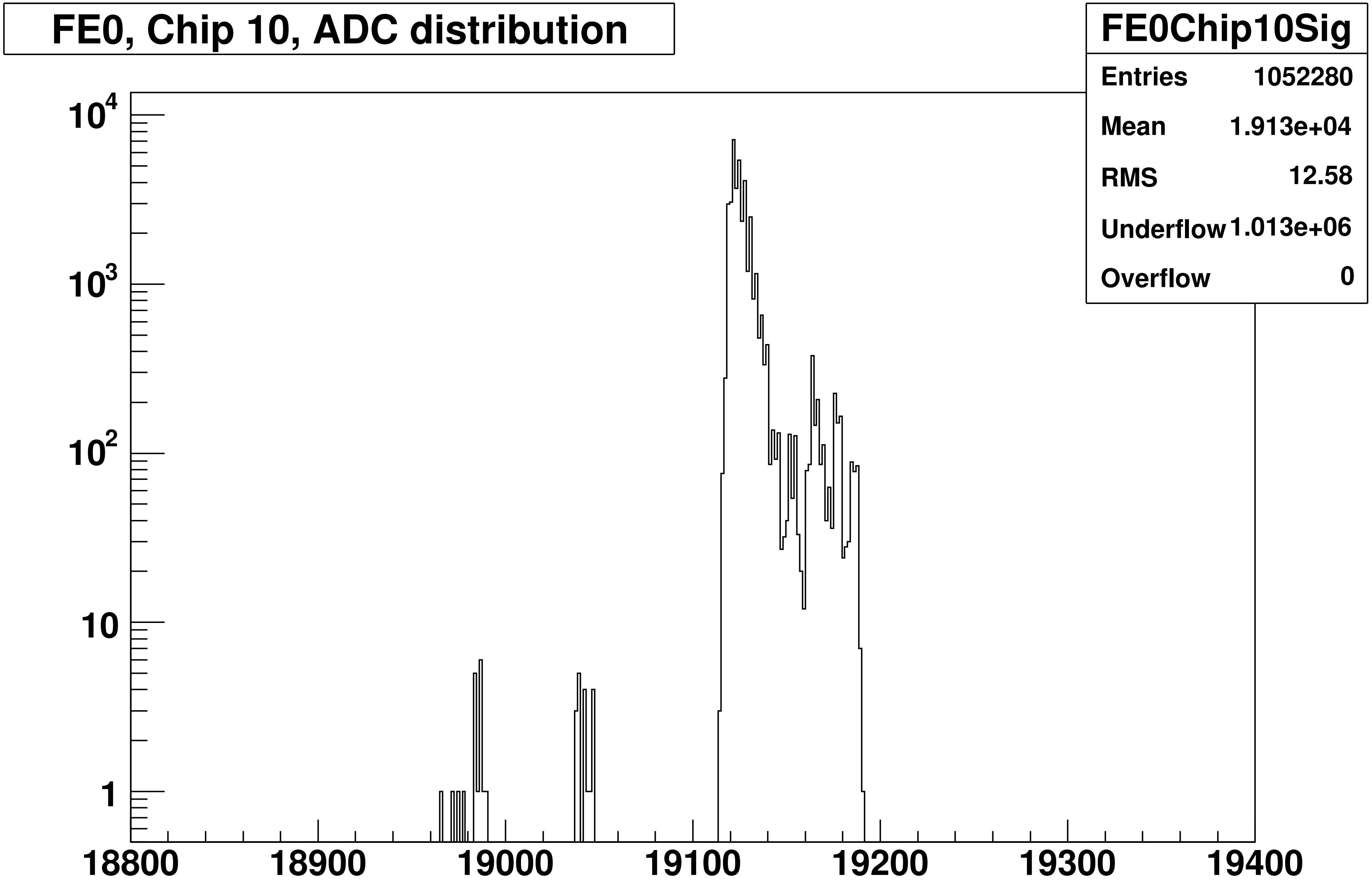

FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 1052280
Mean 1.913e+04
RMS 12.58
Underflow 1.013e+06
Overflow 0
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10^3
10^2
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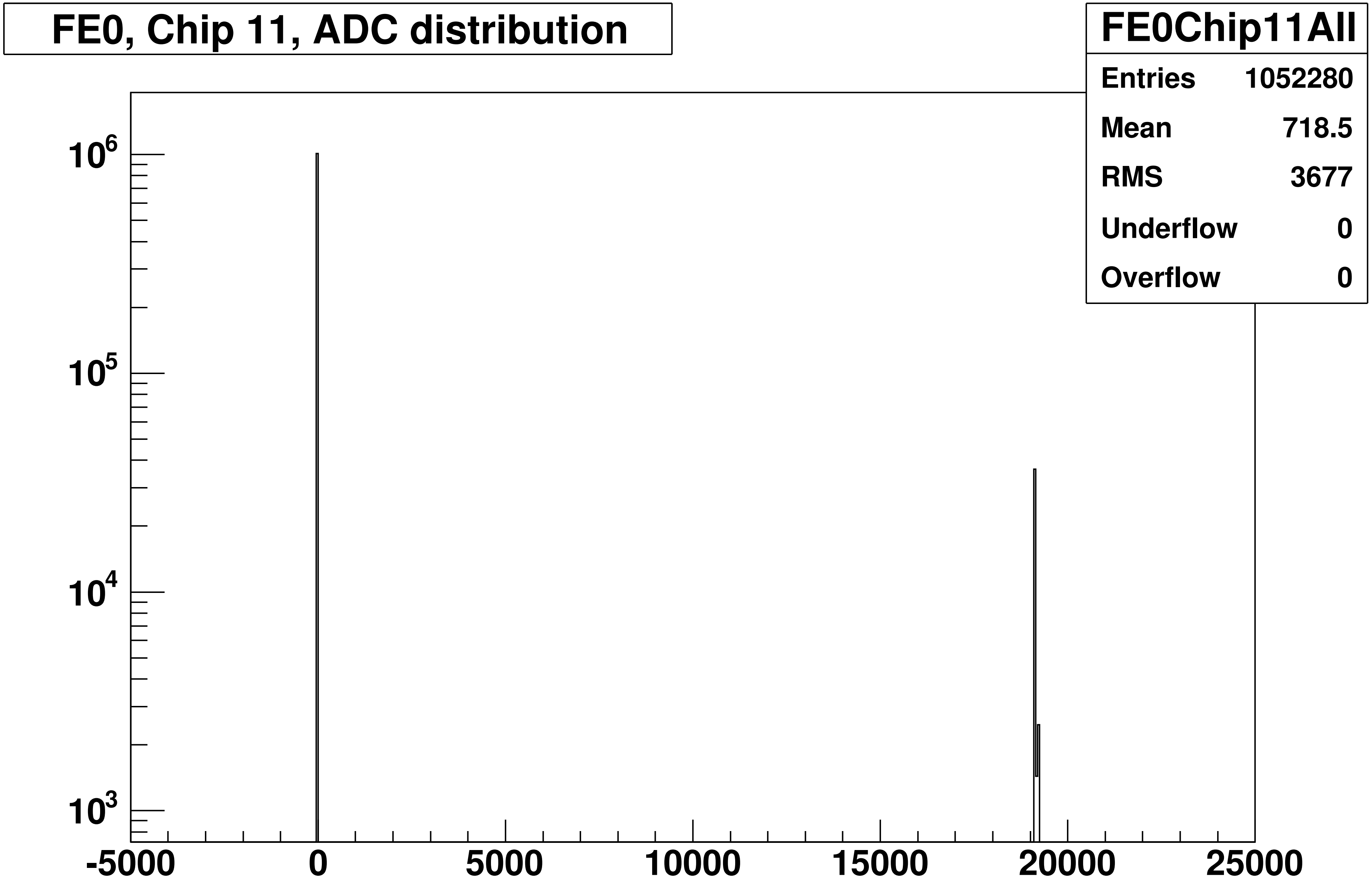
FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 1052280
Mean 718.5
RMS 3677
Underflow 0
Overflow 0
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10^5
10^4
10^3
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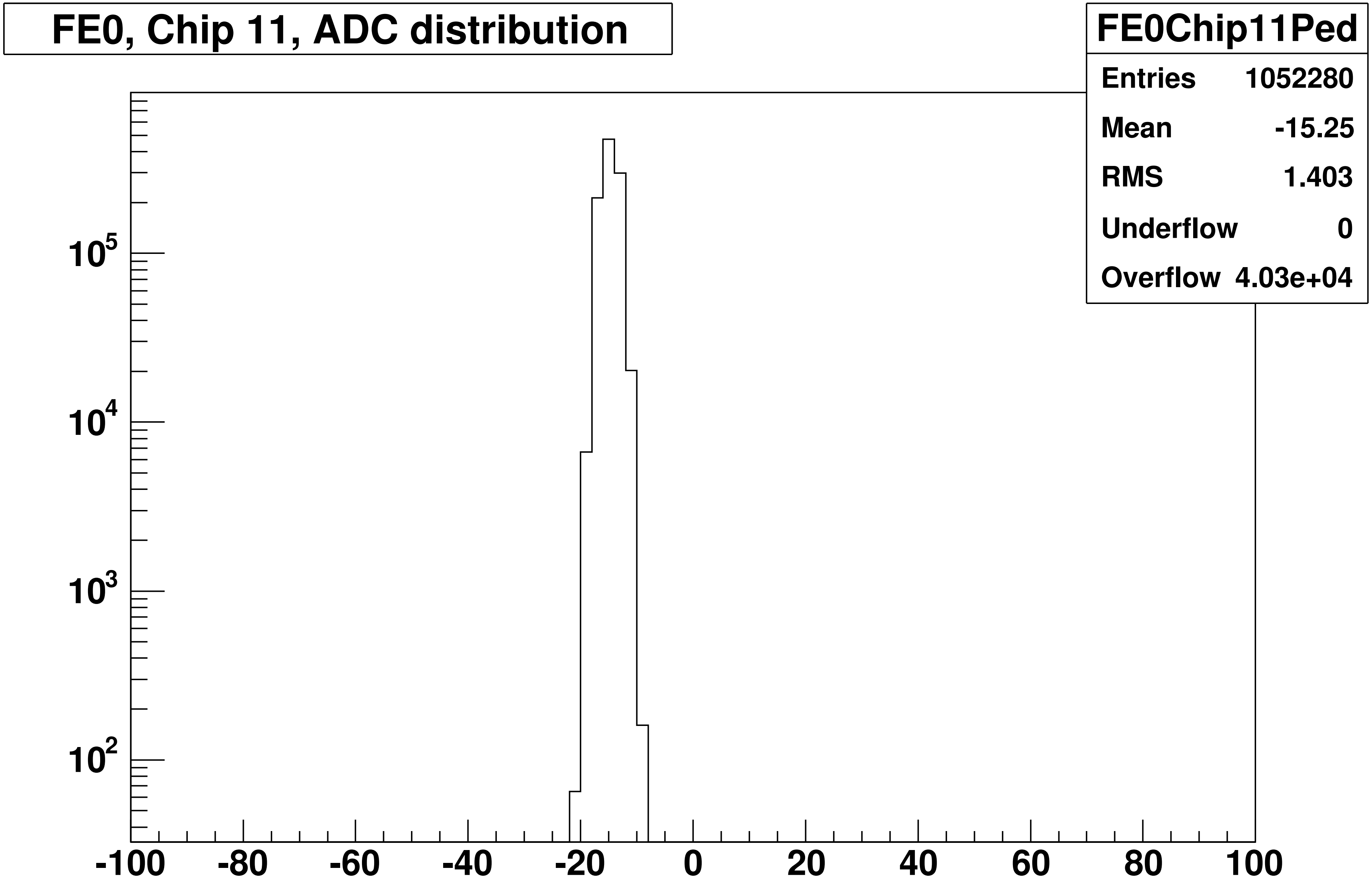
20000
25000


FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 1052280
Mean -15.25
RMS 1.403
Underflow 0
Overflow 4.03e+04
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10^2
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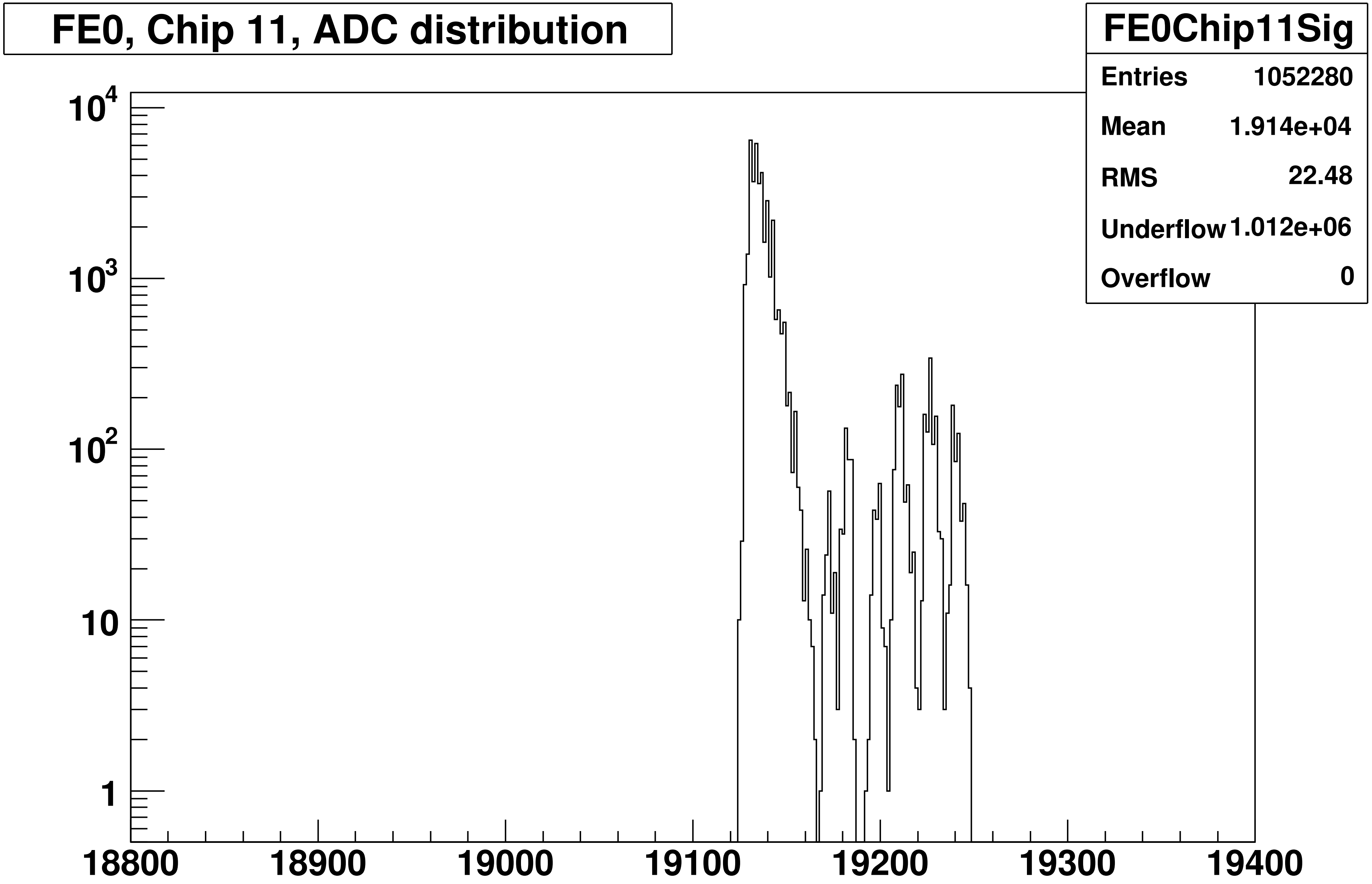
FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 1052280
Mean 1.914e+04
RMS 22.48
Underflow 1.012e+06
Overflow 0
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10^3
10^2
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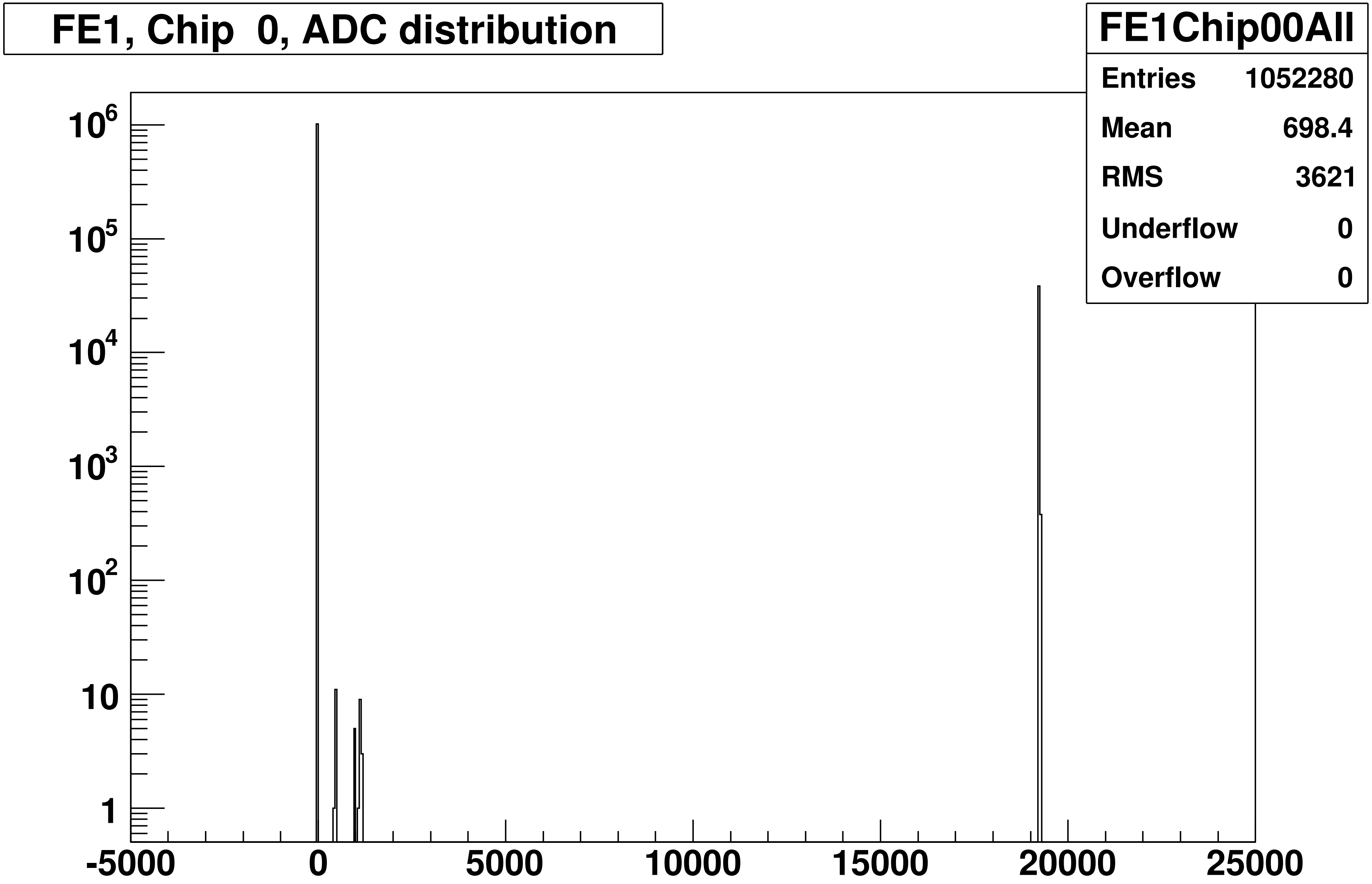
FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 1052280
Mean 698.4
RMS 3621
Underflow 0
Overflow 0
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10^2
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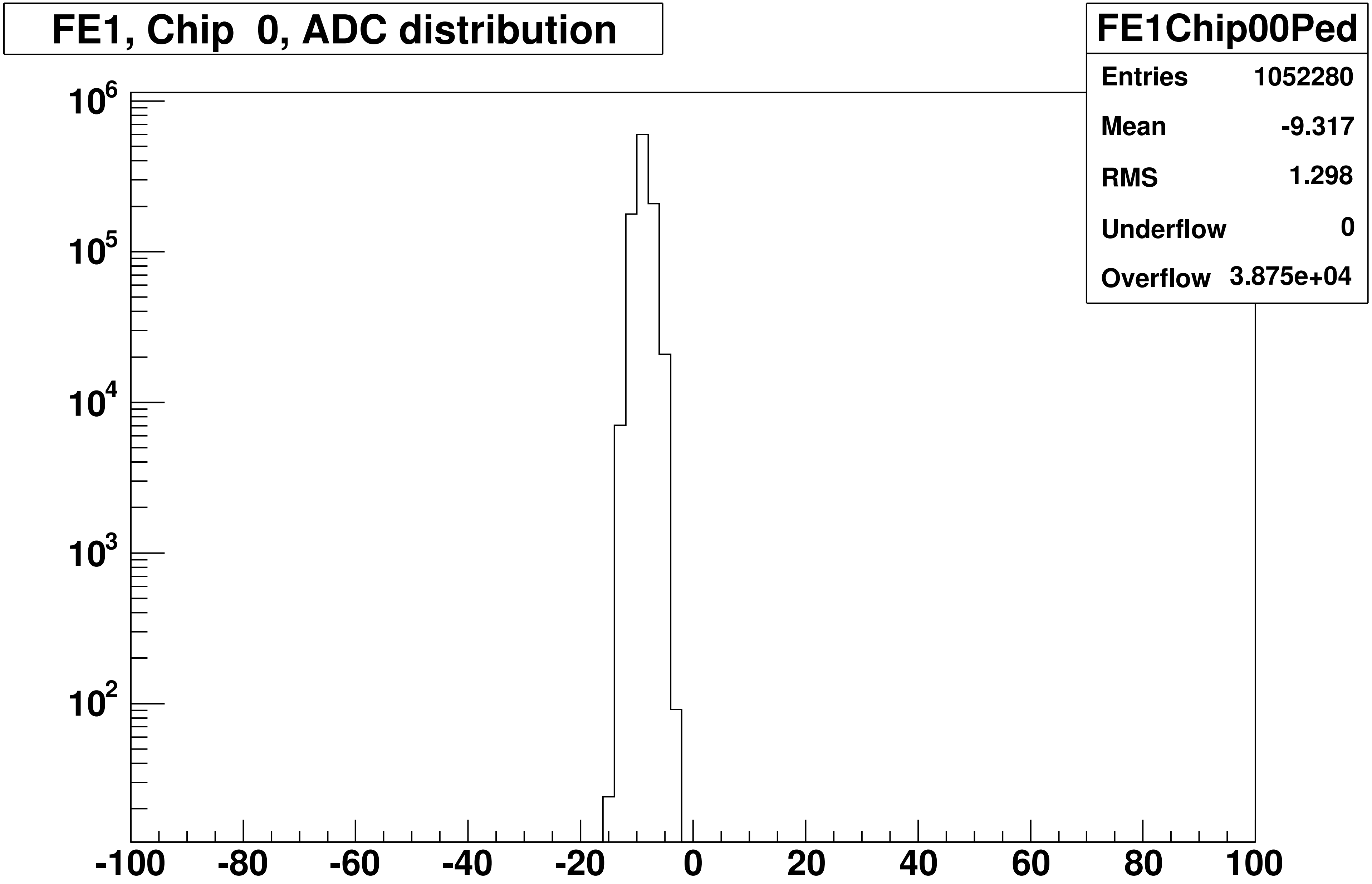
FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 1052280
Mean -9.317
RMS 1.298
Underflow 0
Overflow 3.875e+04
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10^4
10^3
10^2
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-20
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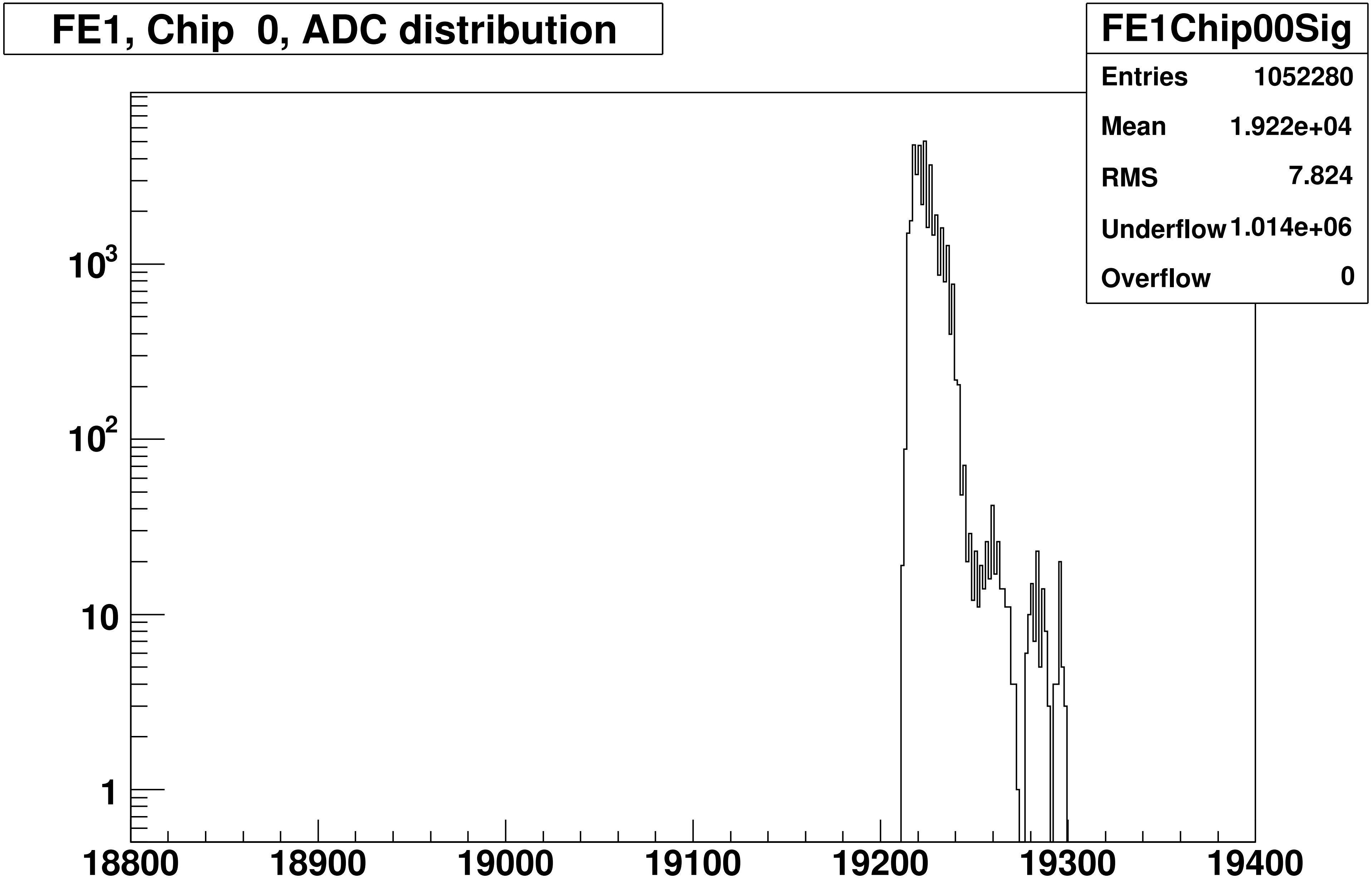

FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 1052280
Mean 1.922e+04
RMS 7.824
Underflow 1.014e+06
Overflow 0
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10^2
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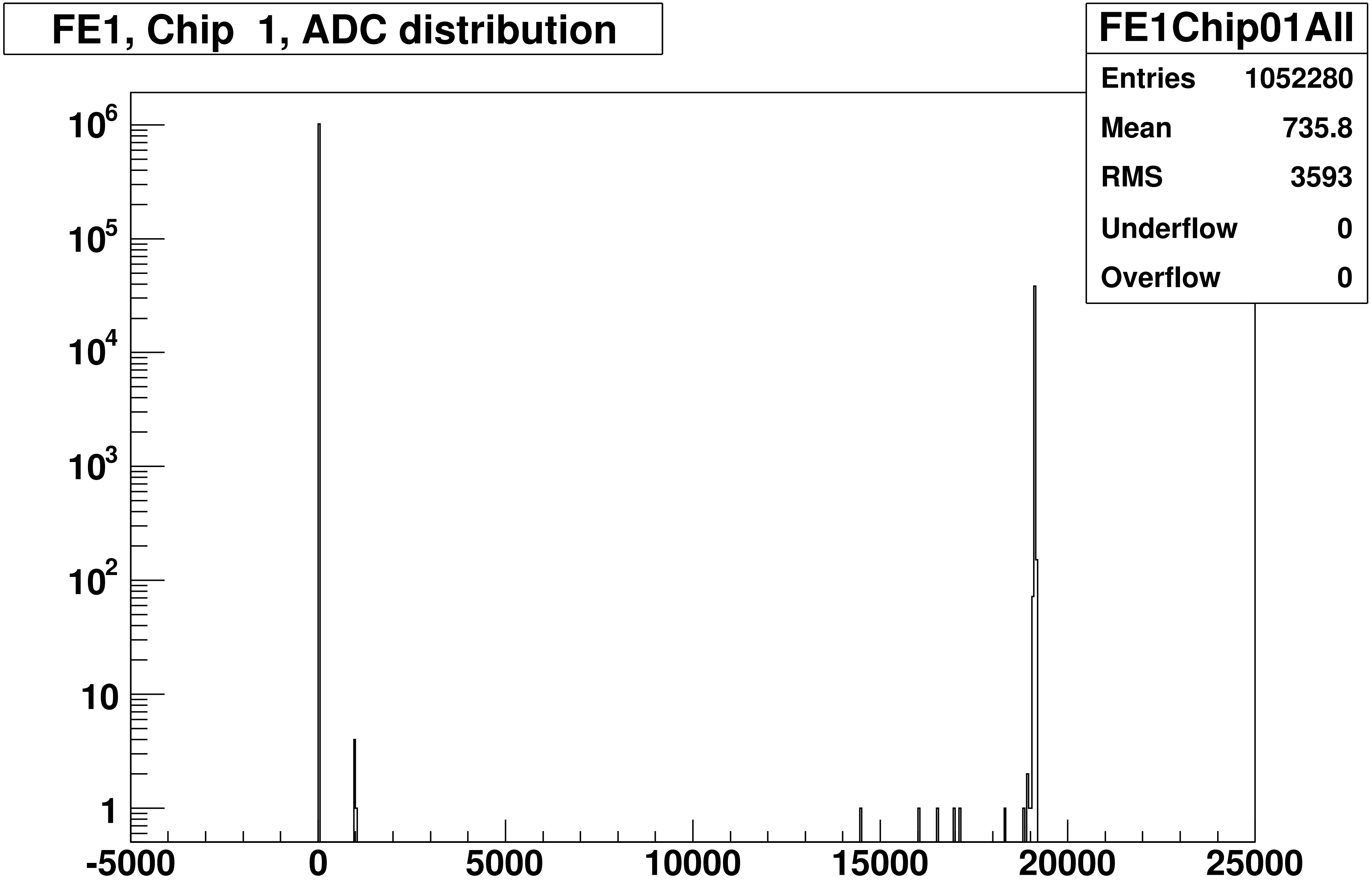
FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 1052280
Mean 735.8
RMS 3593
Underflow 0
Overflow 0
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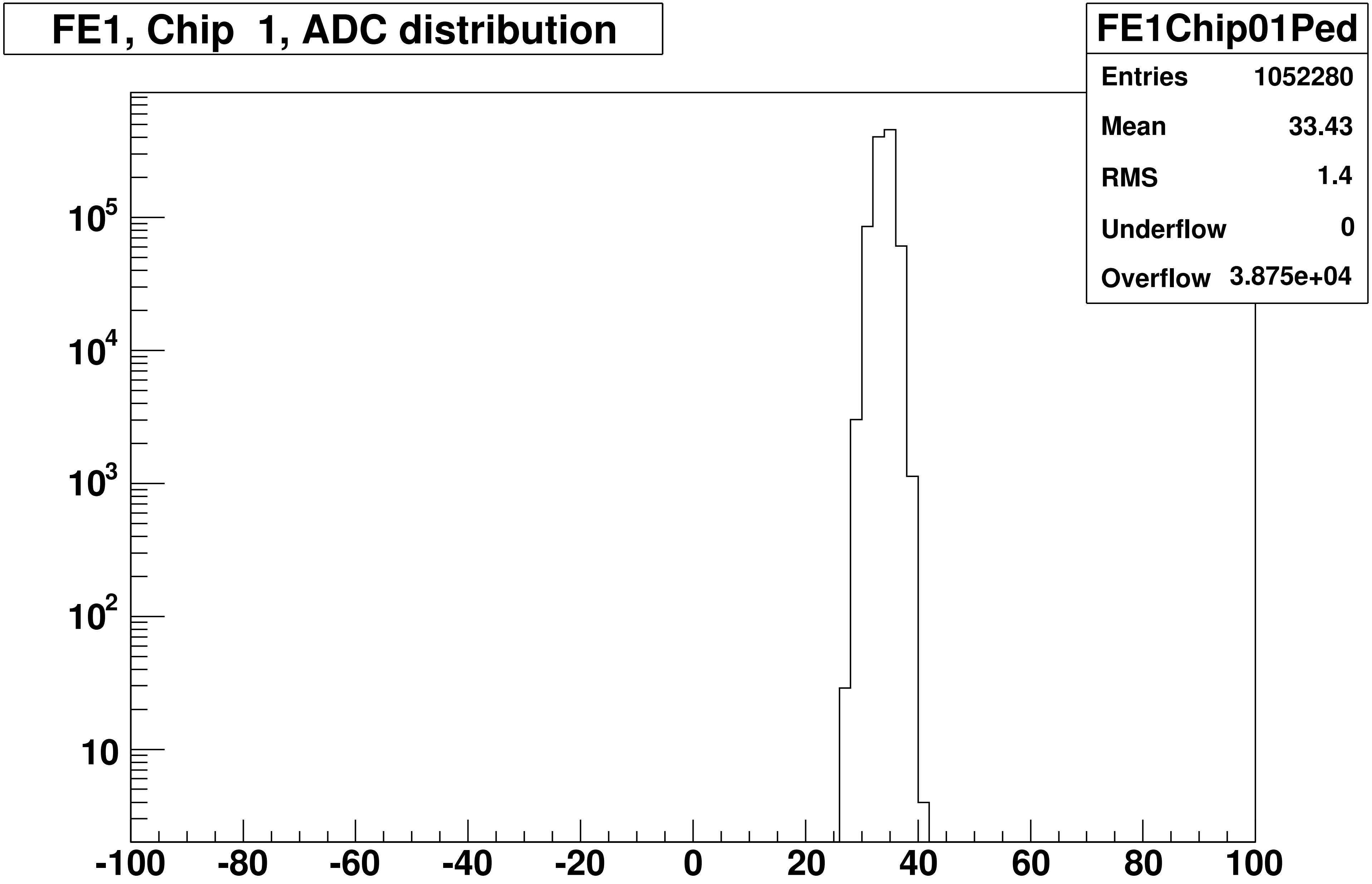
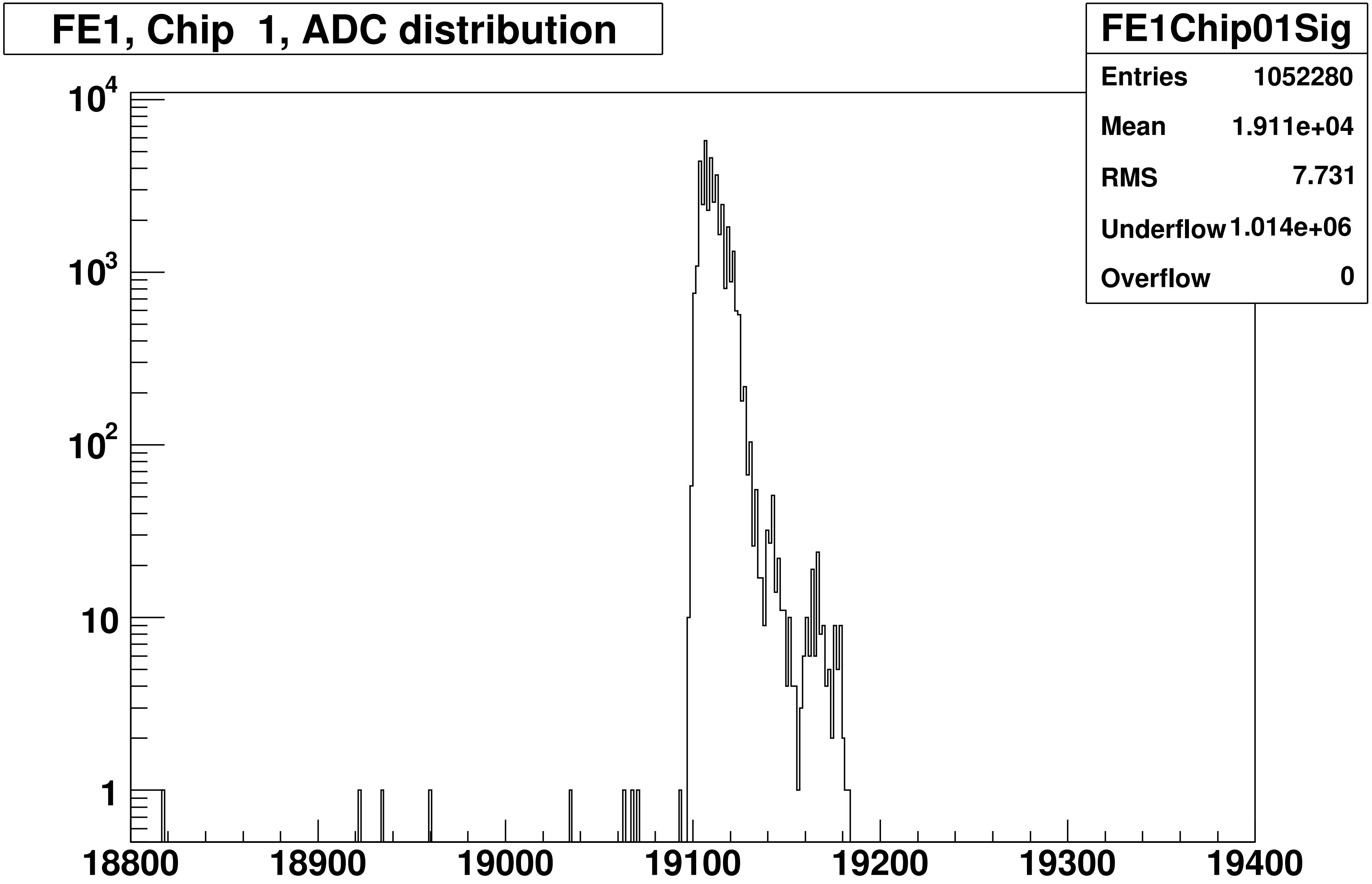
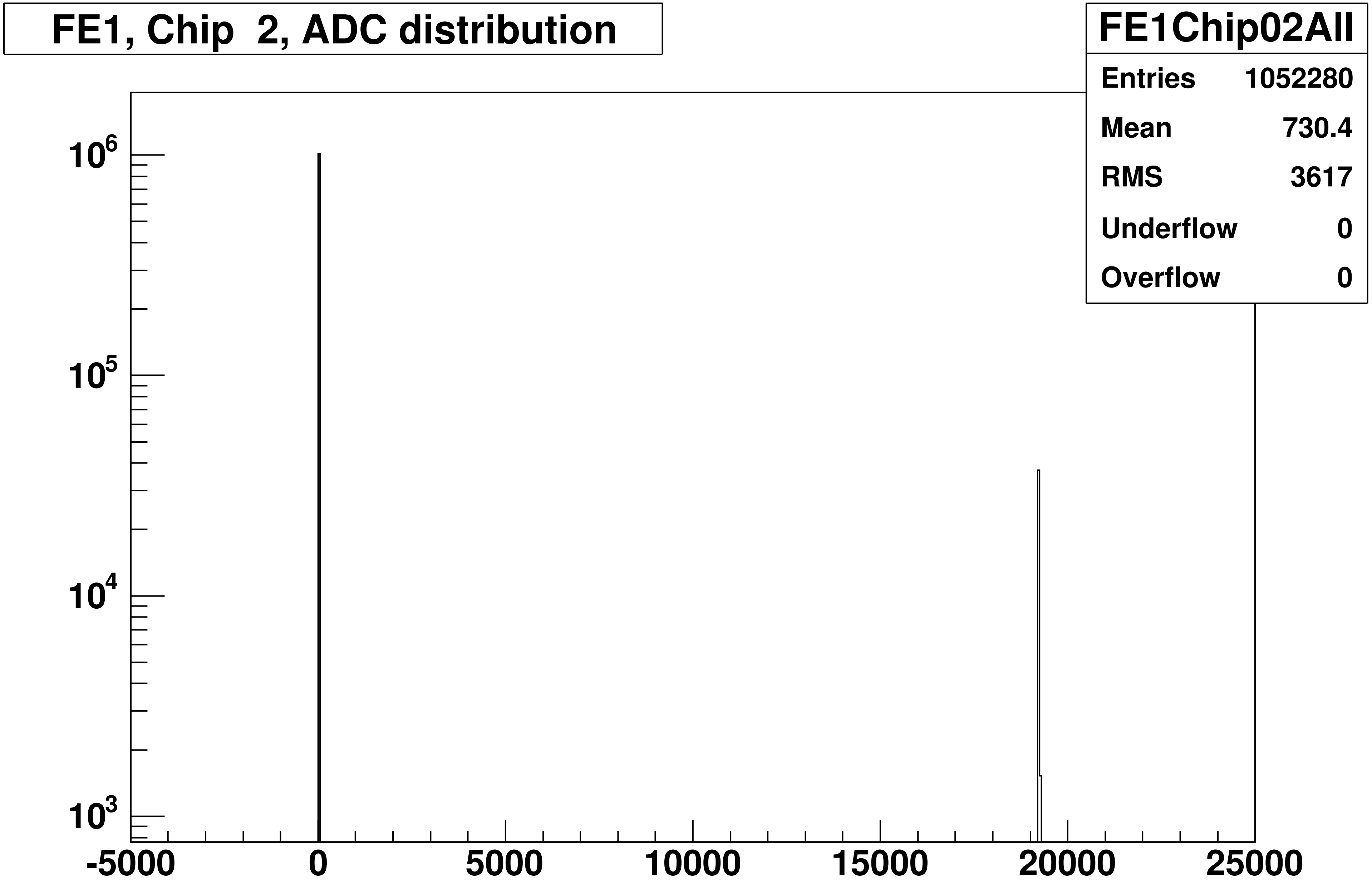
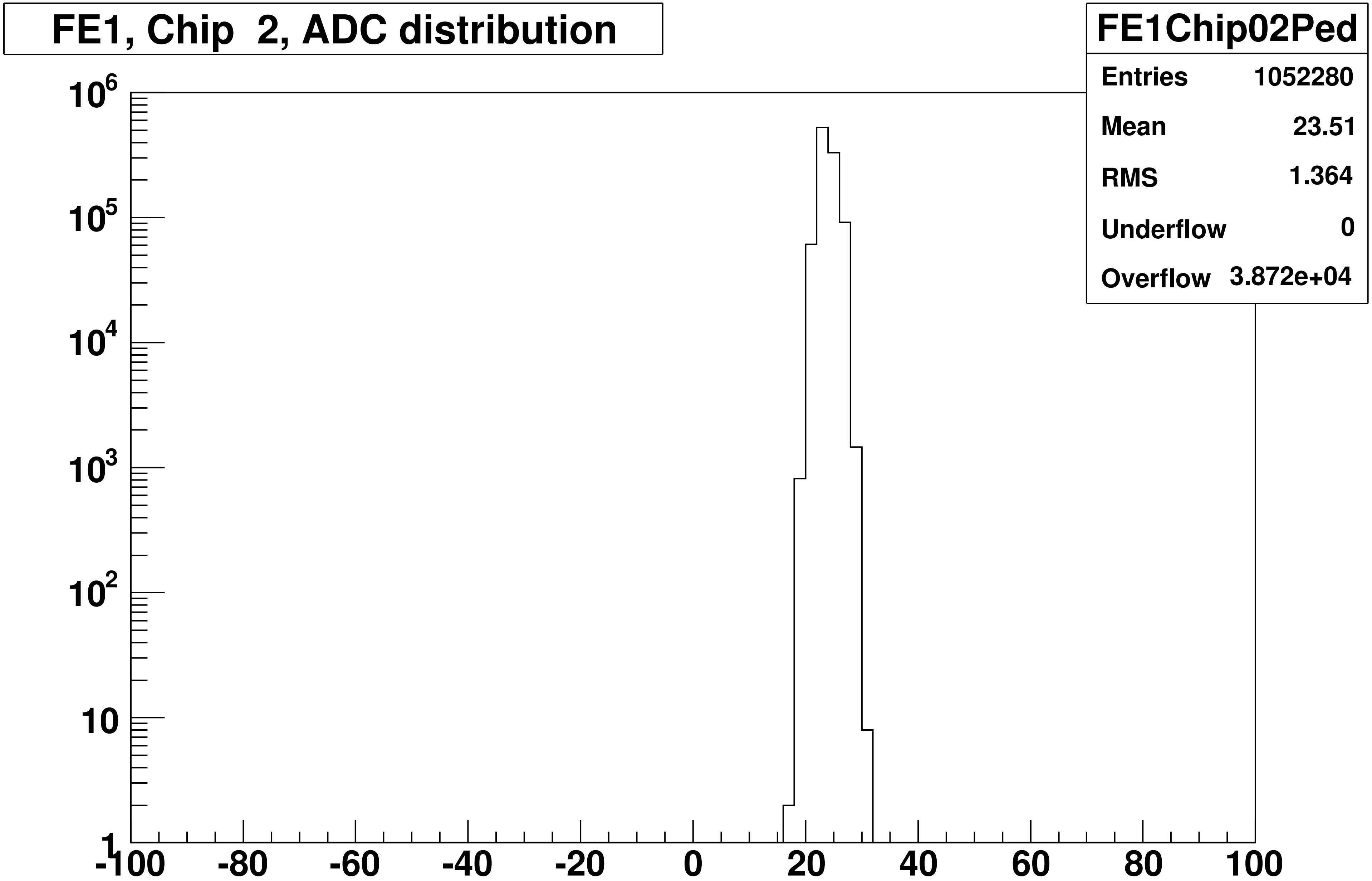
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 1052280
Mean 33.43
RMS 1.4
Underflow 0
Overflow 3.875e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 1052280
Mean 1.911e+04
RMS 7.731
Underflow 1.014e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 1052280
Mean 730.4
RMS 3617
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 1052280
Mean 23.51
RMS 1.364
Underflow 0
Overflow 3.872e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
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-40
-20
0
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40
60
80
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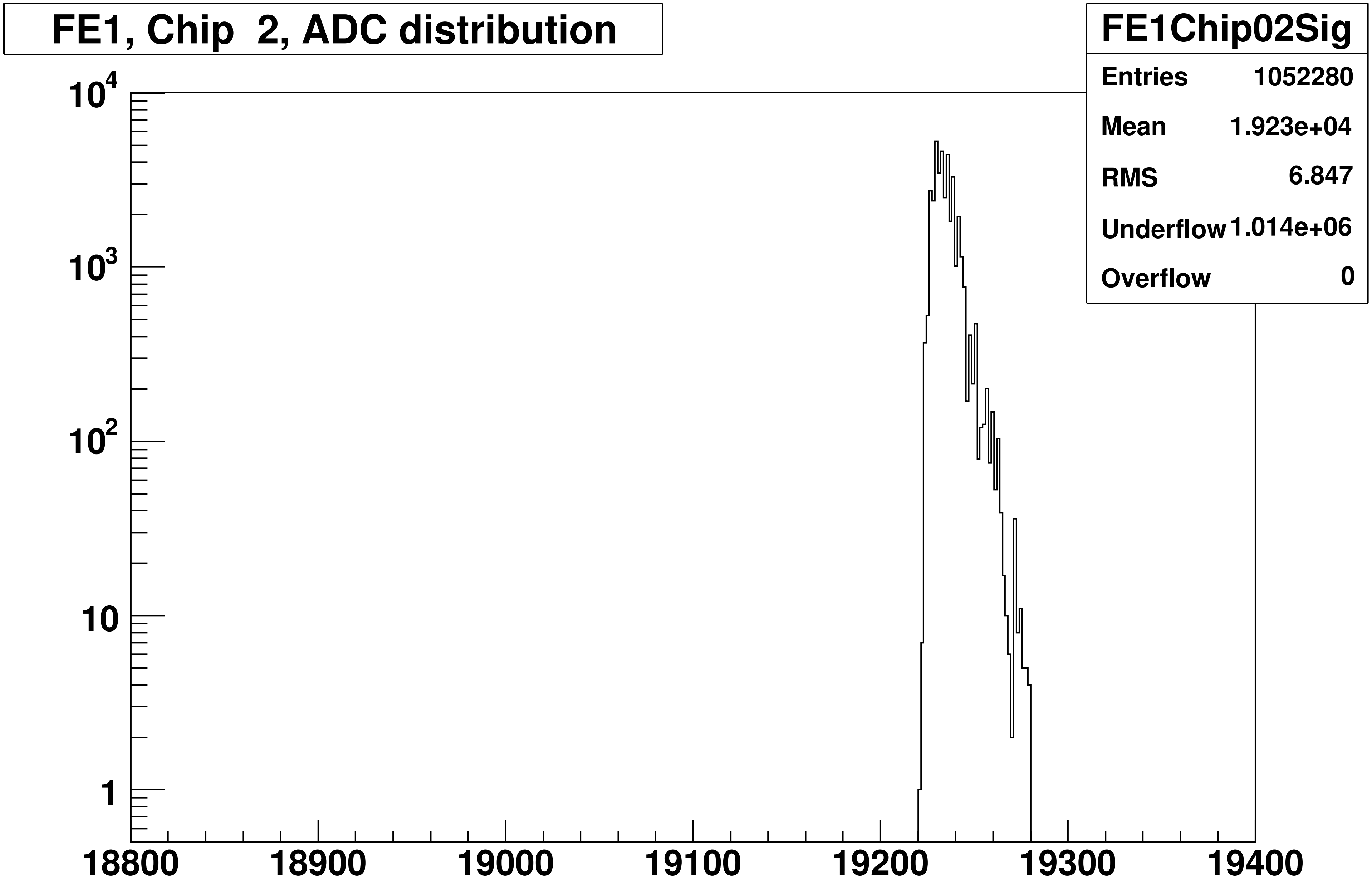
FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 1052280
Mean 1.923e+04
RMS 6.847
Underflow 1.014e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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19100
19200
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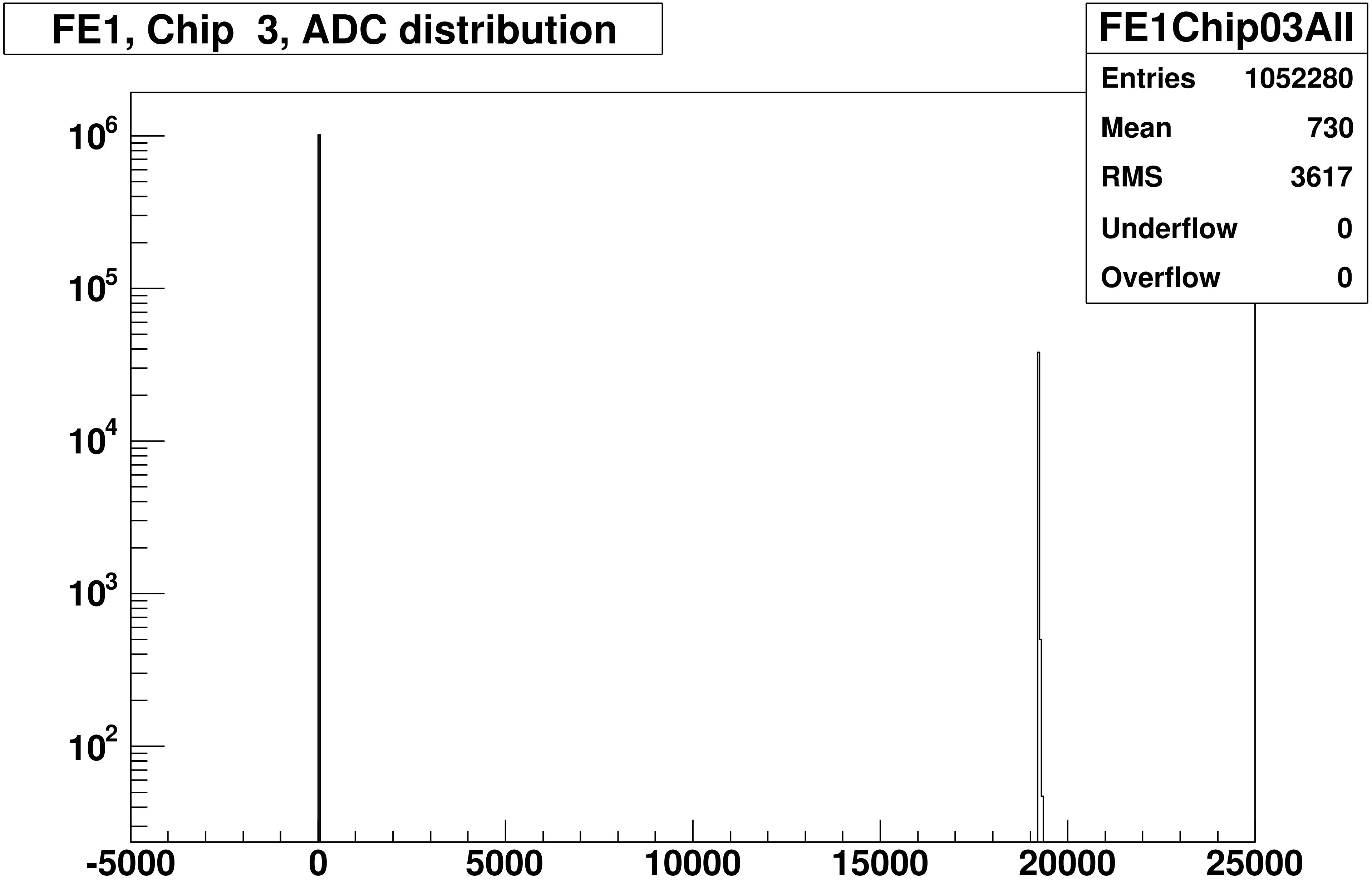
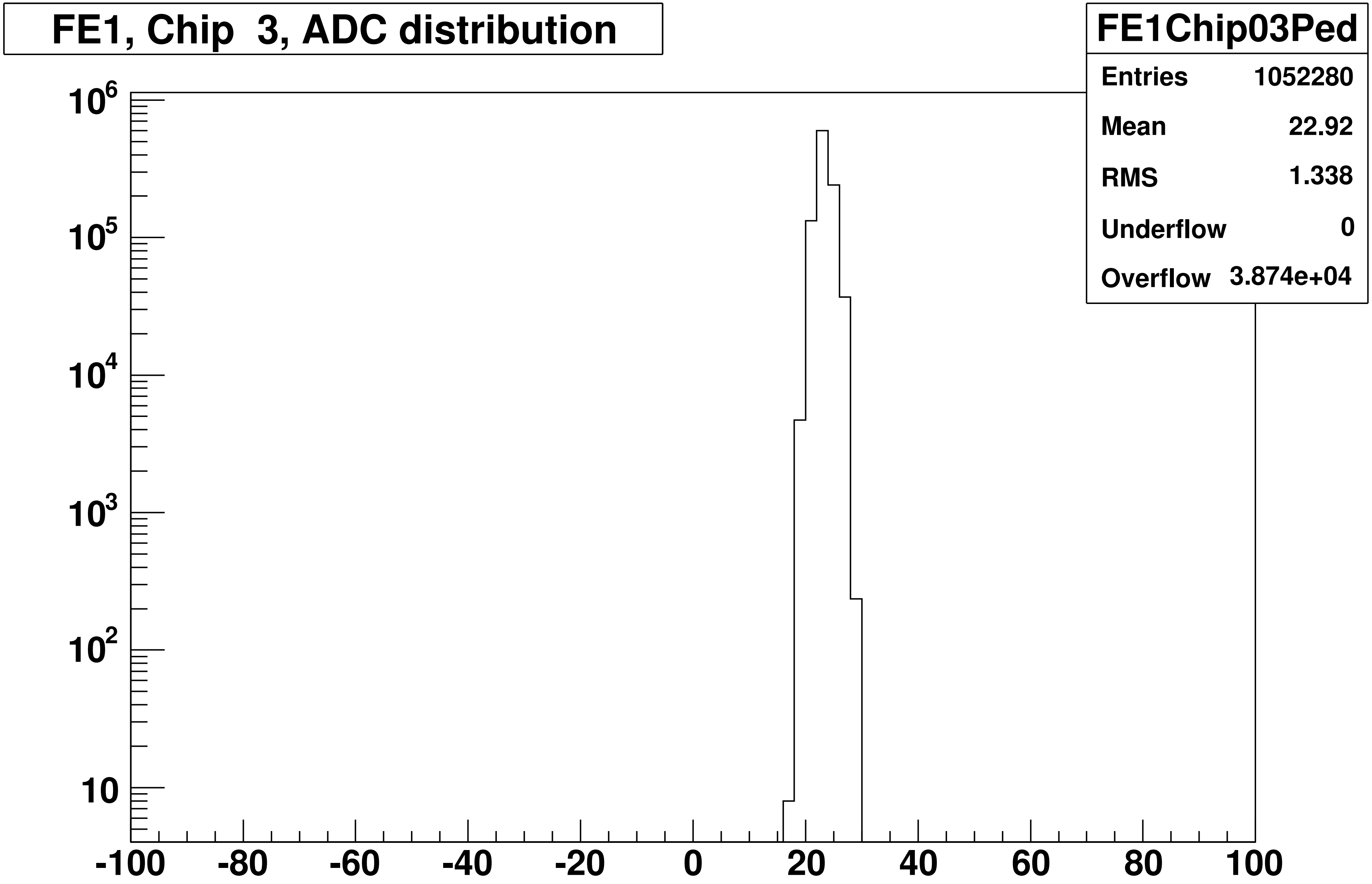
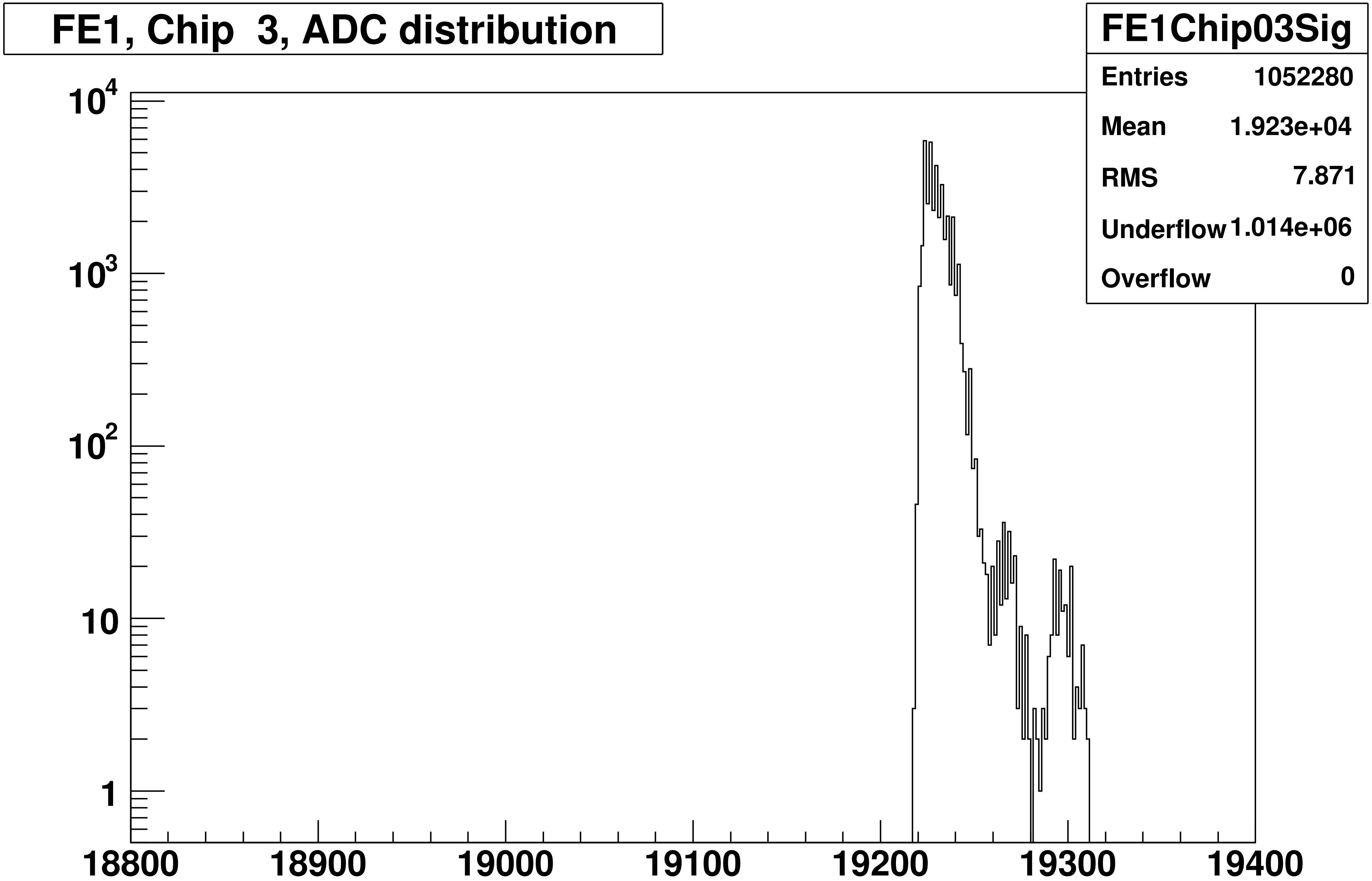
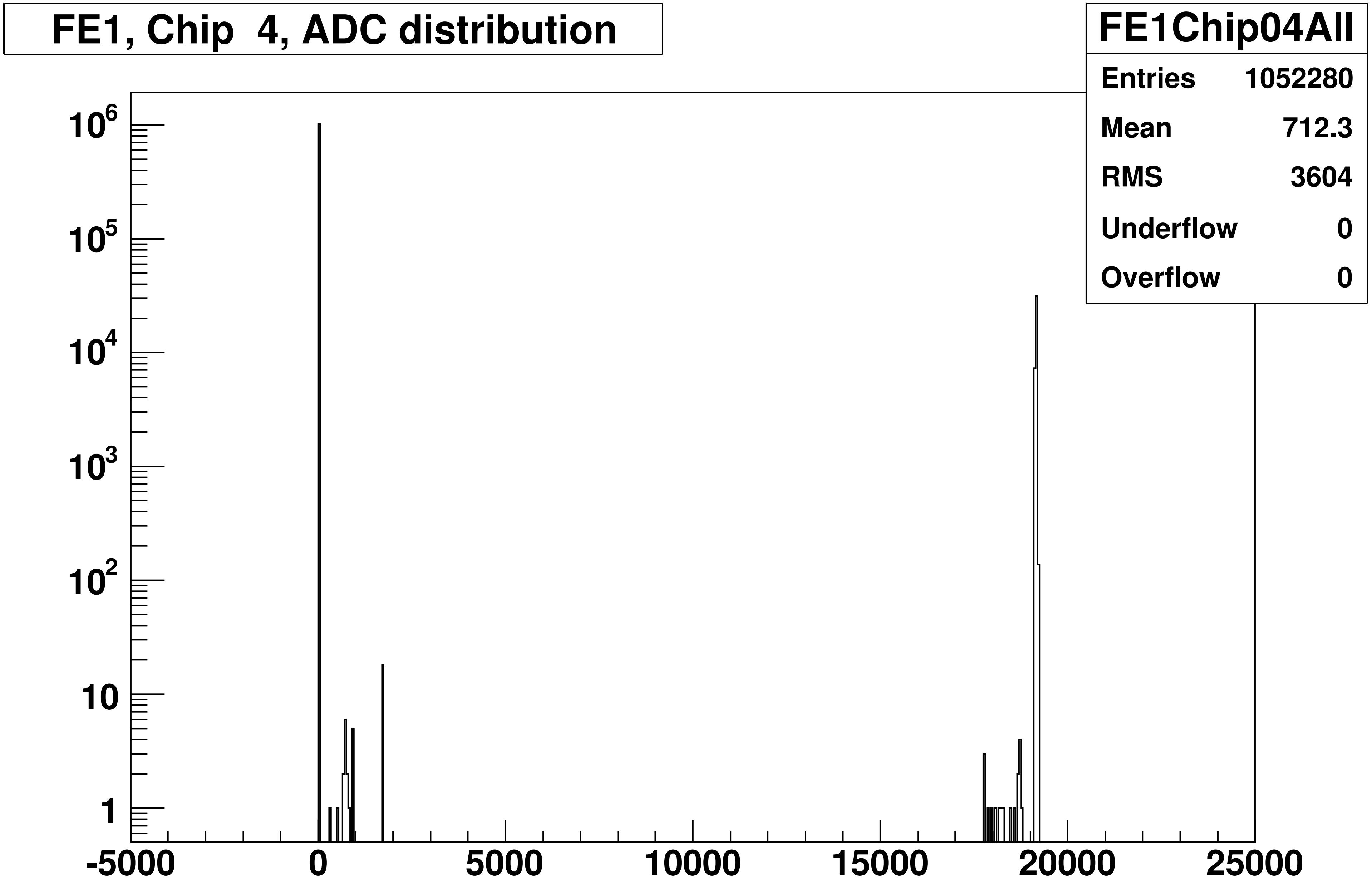
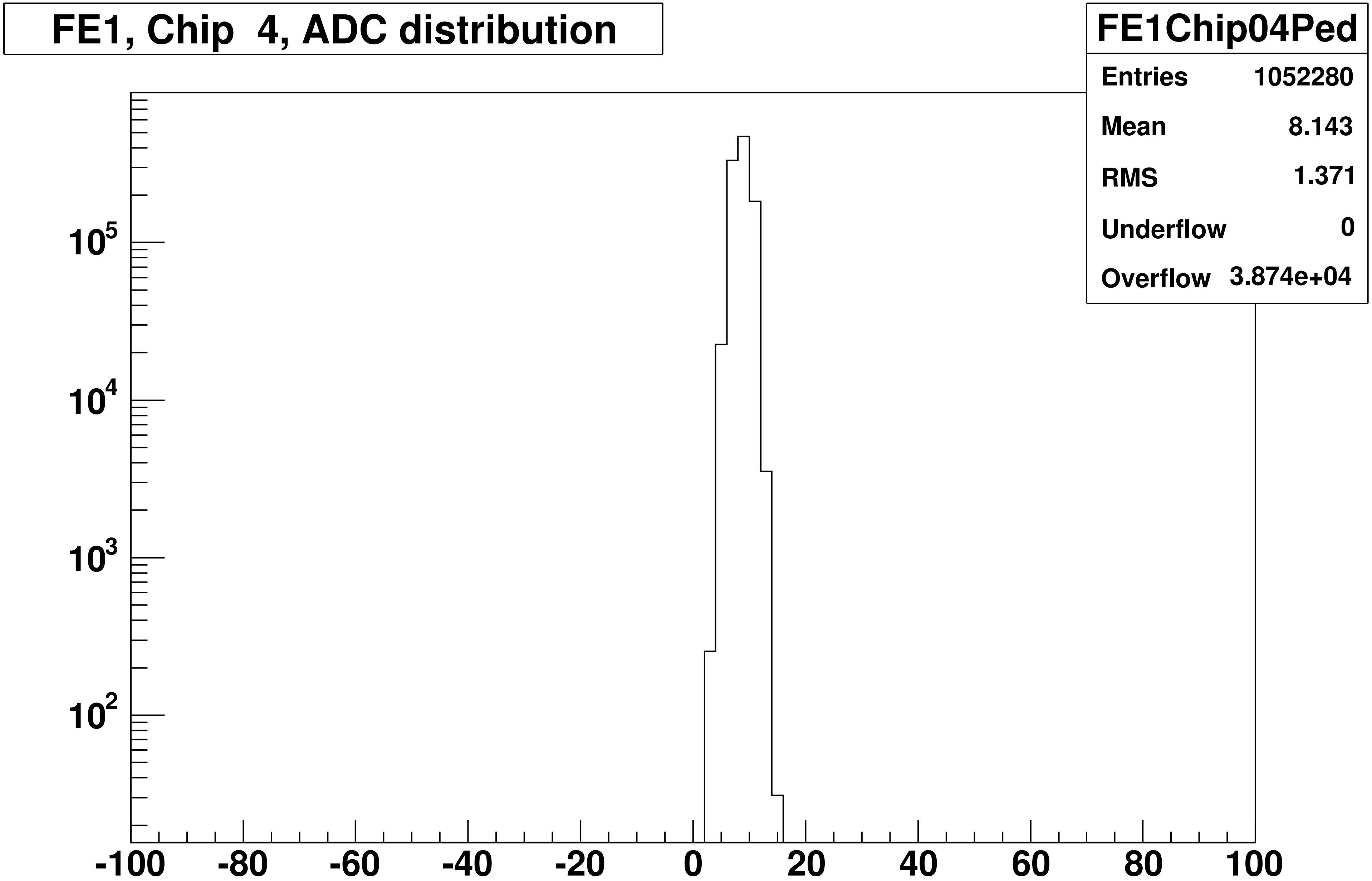

FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 1052280
Mean 730
RMS 3617
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 1052280
Mean 22.92
RMS 1.338
Underflow 0
Overflow 3.874e+04
10^6
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 1052280
Mean 1.923e+04
RMS 7.871
Underflow 1.014e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 1052280
Mean 712.3
RMS 3604
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 1052280
Mean 8.143
RMS 1.371
Underflow 0
Overflow 3.874e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
0
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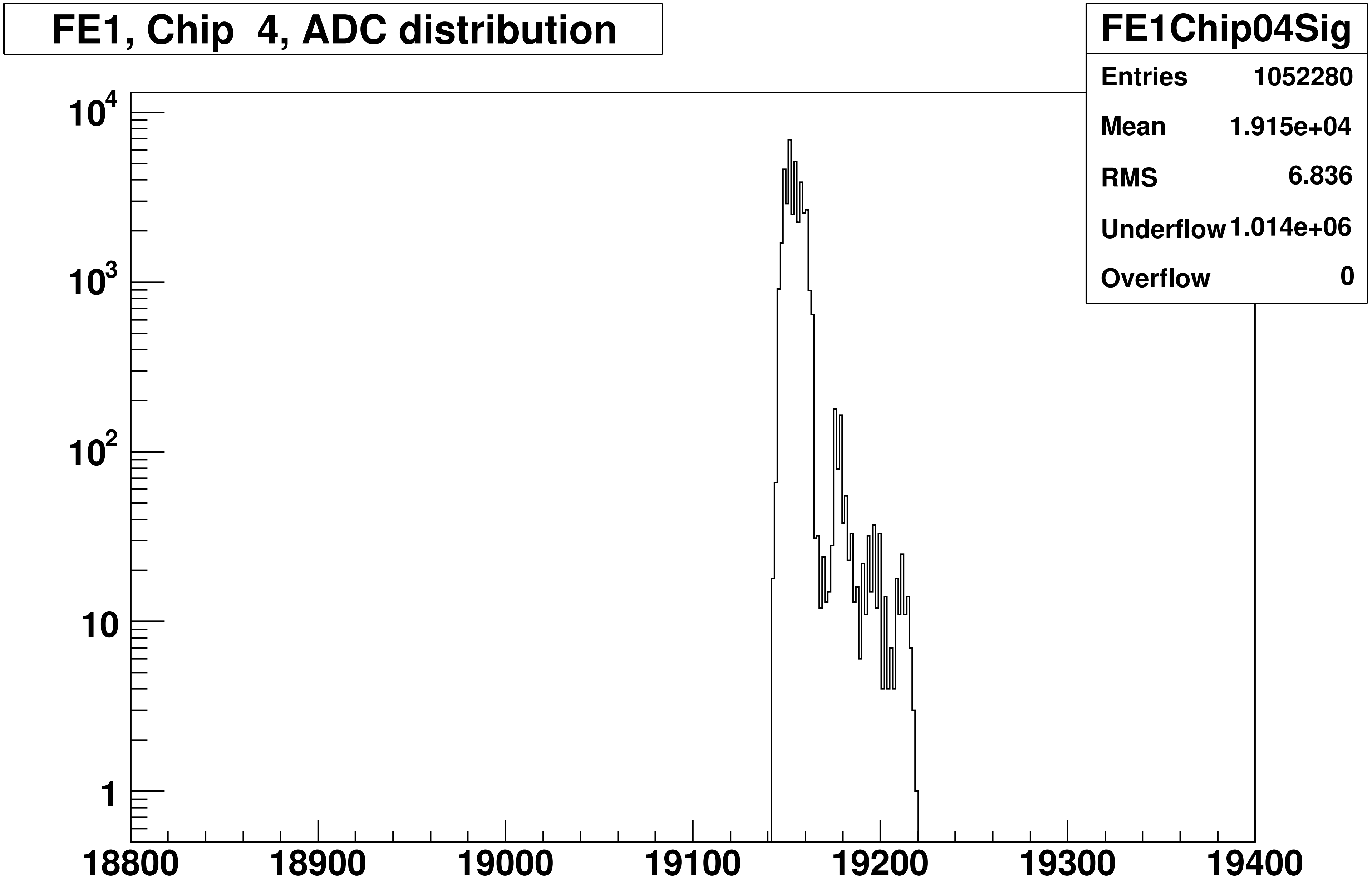
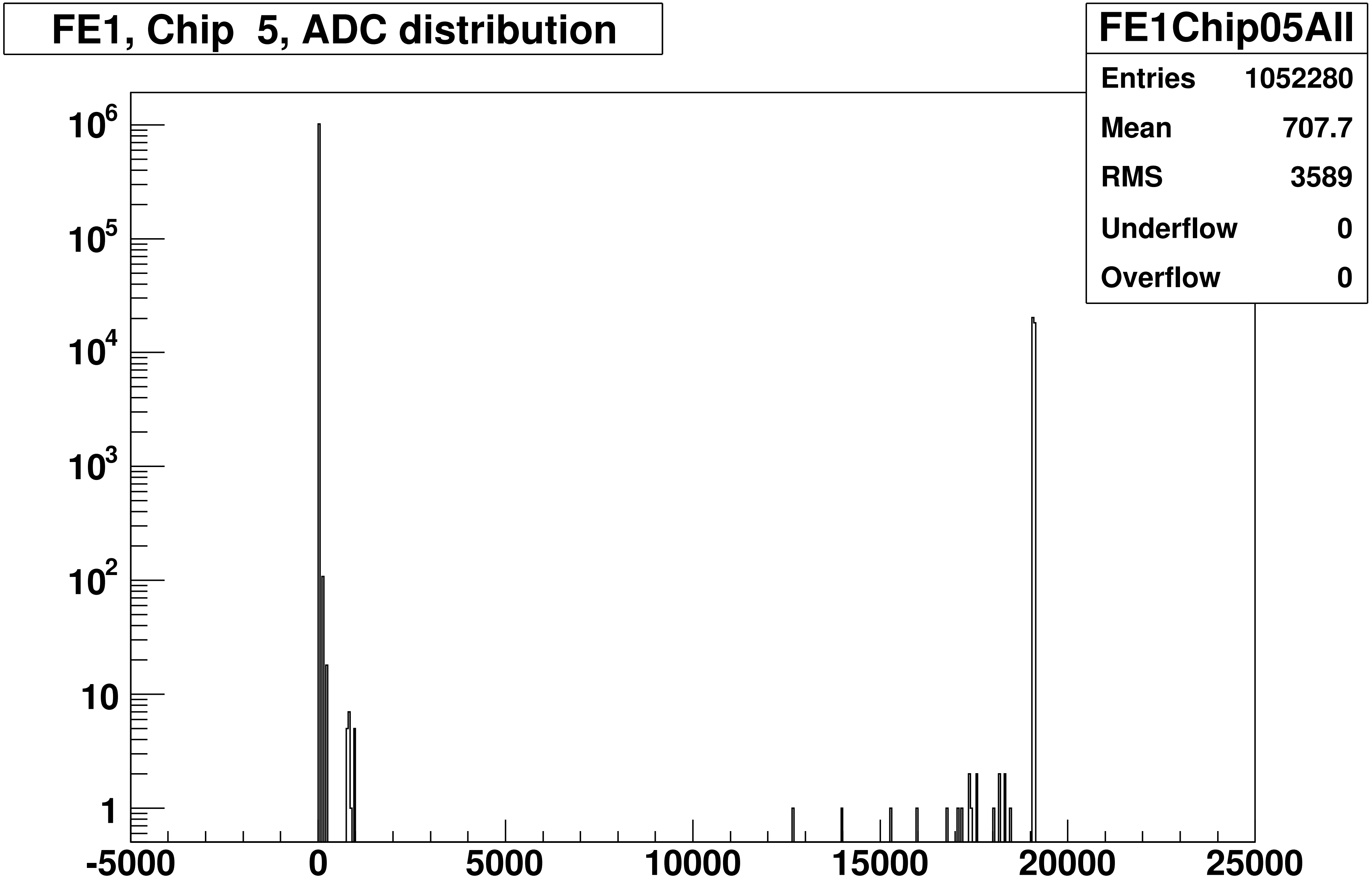
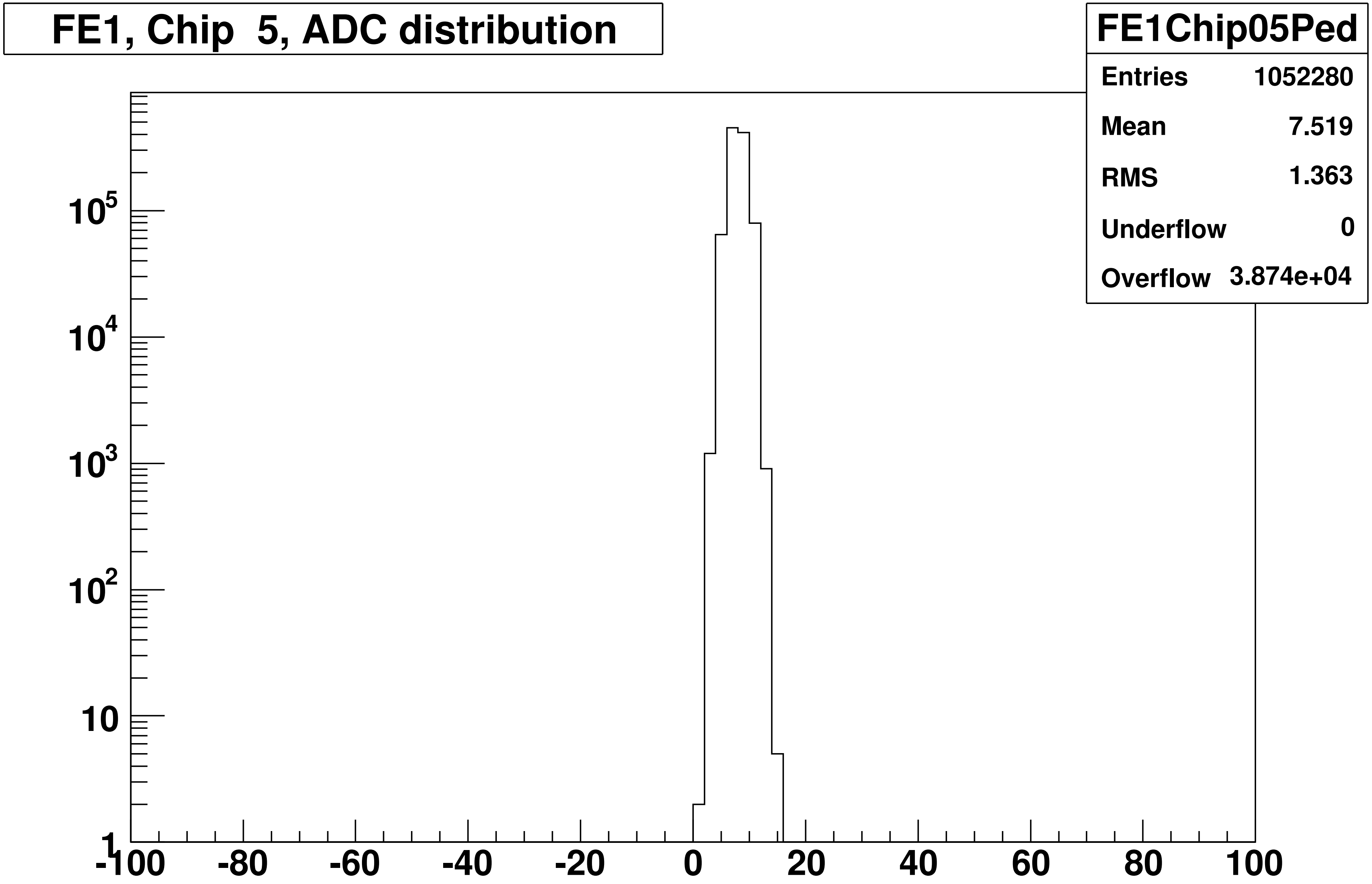
40
60
80
100

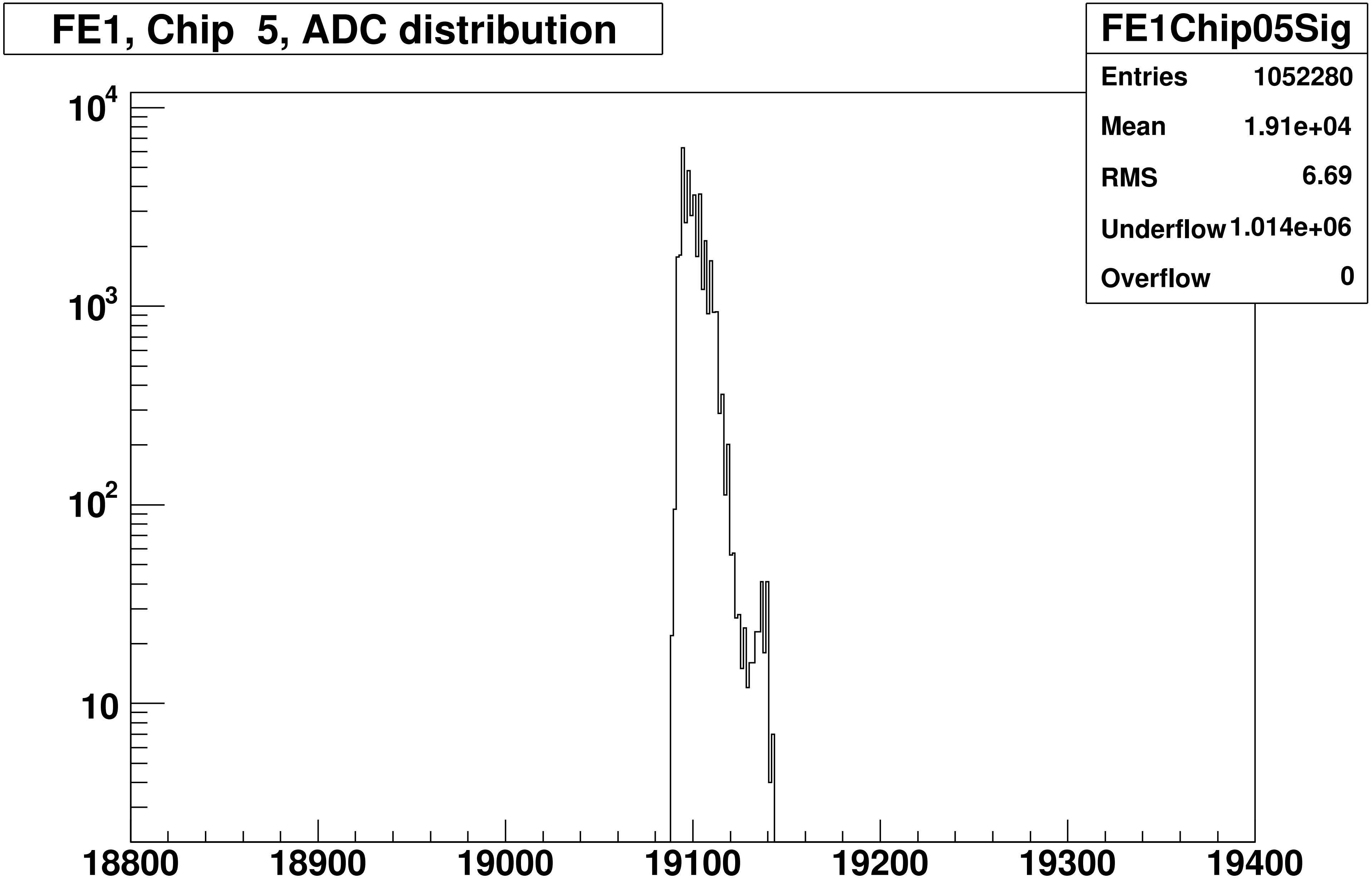


FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 1052280
Mean 1.915e+04
RMS 6.836
Underflow 1.014e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

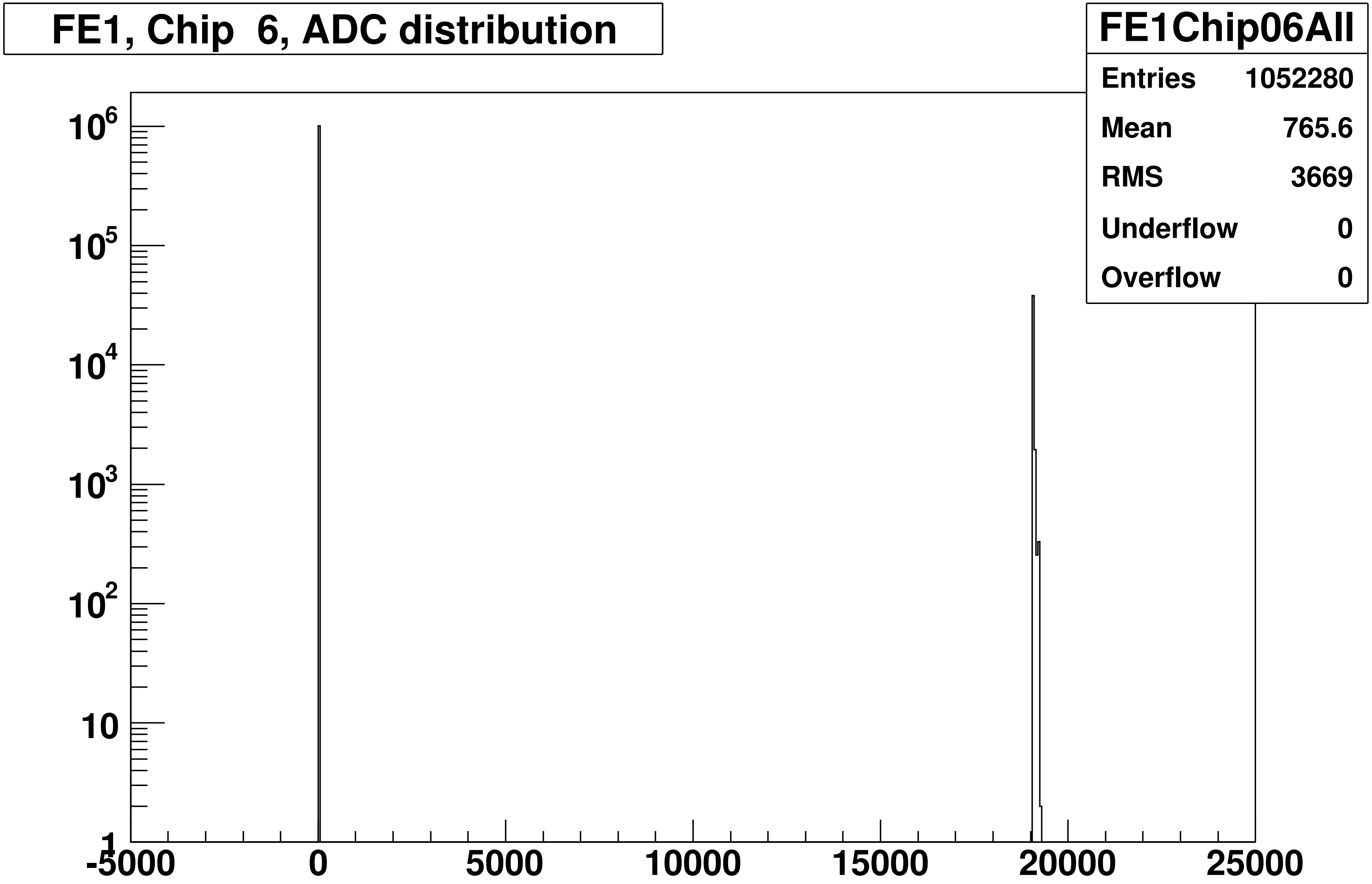


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 1052280
Mean 707.7
RMS 3589
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

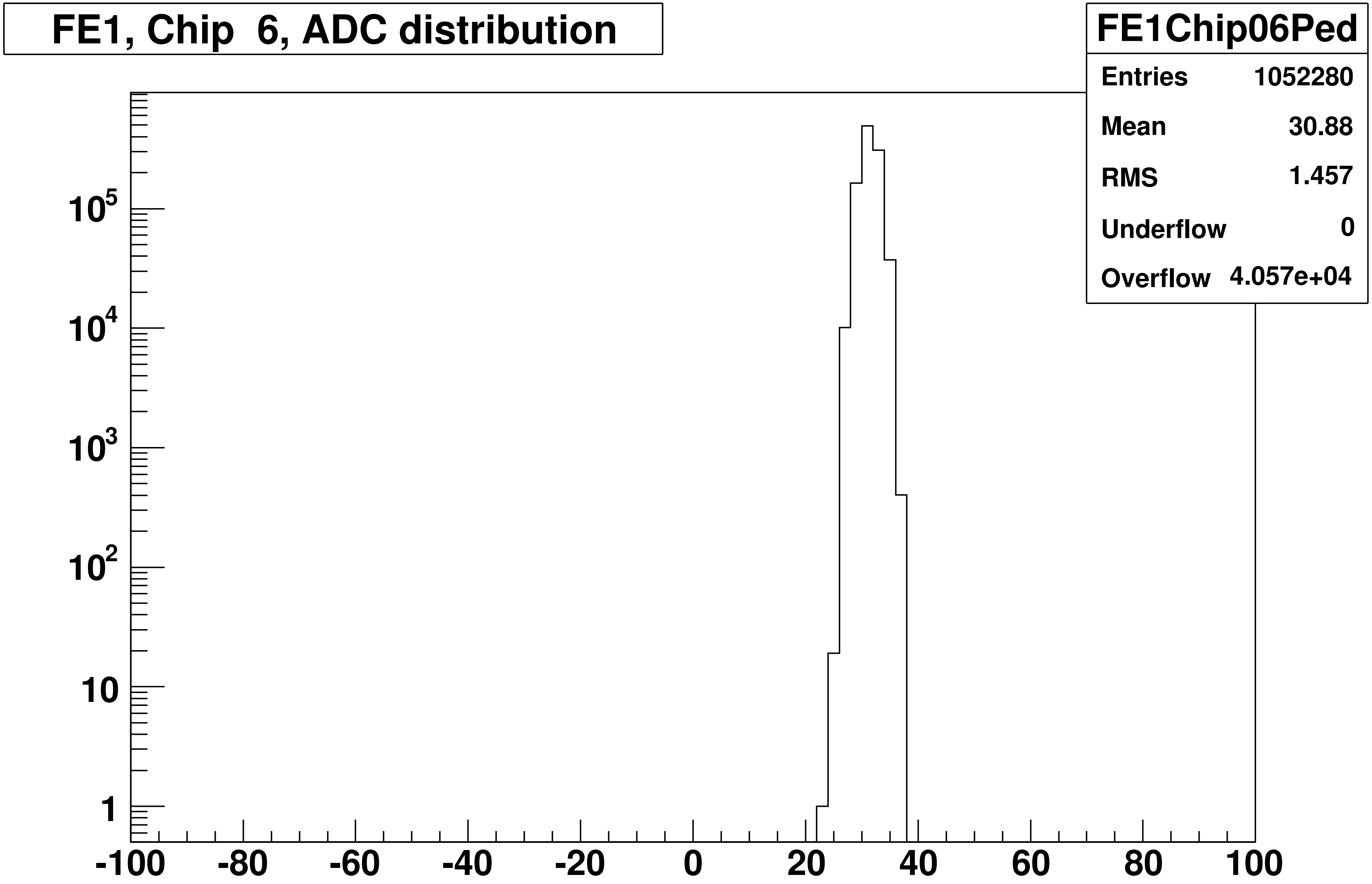

FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 1052280
Mean 7.519
RMS 1.363
Underflow 0
Overflow 3.874e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



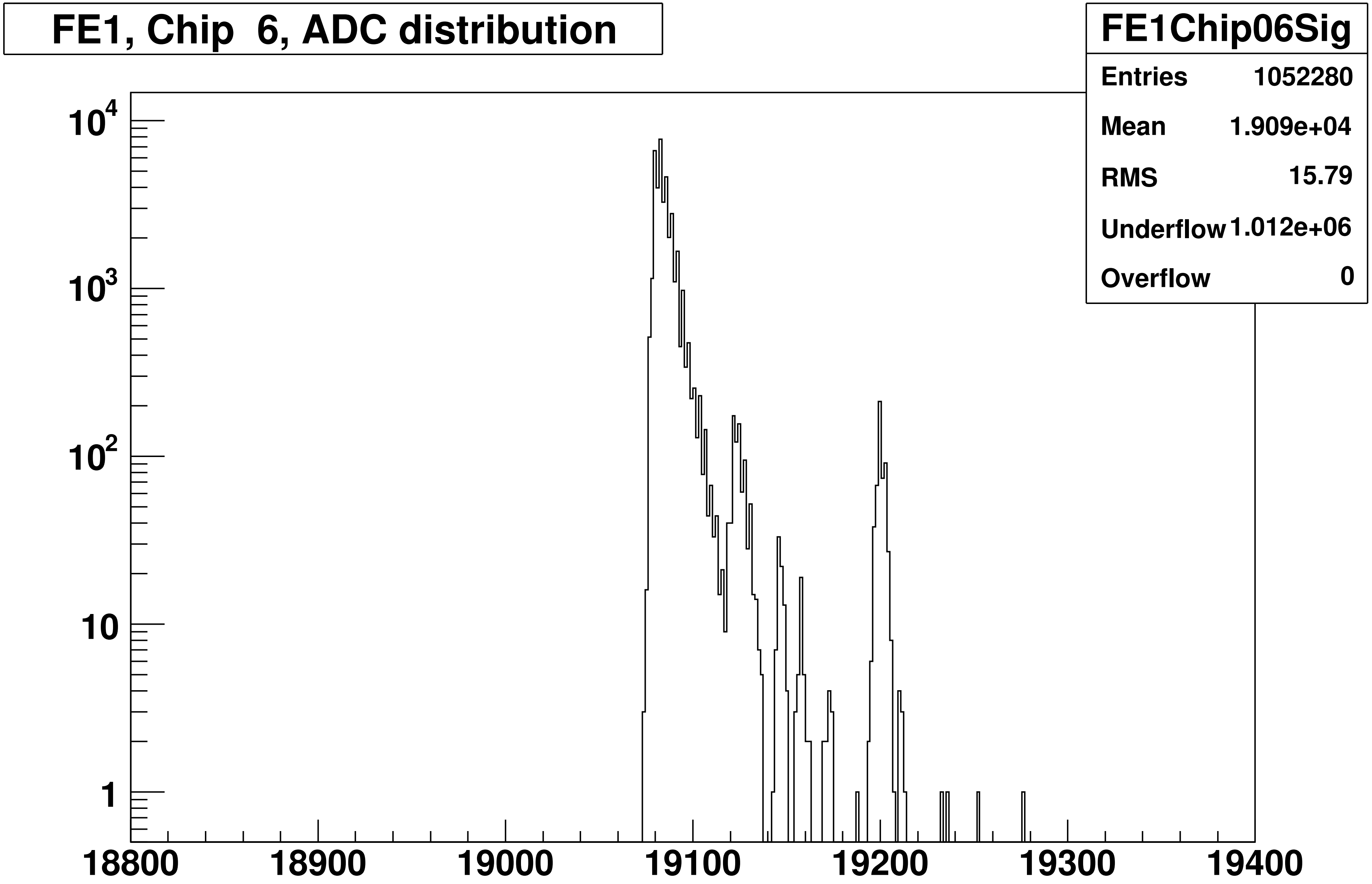
FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 1052280
Mean 1.91e+04
RMS 6.69
Underflow 1.014e+06
Overflow 0
10^4
10^3
10^2
10
18800
18900
19000
19100
19200
19300
19400



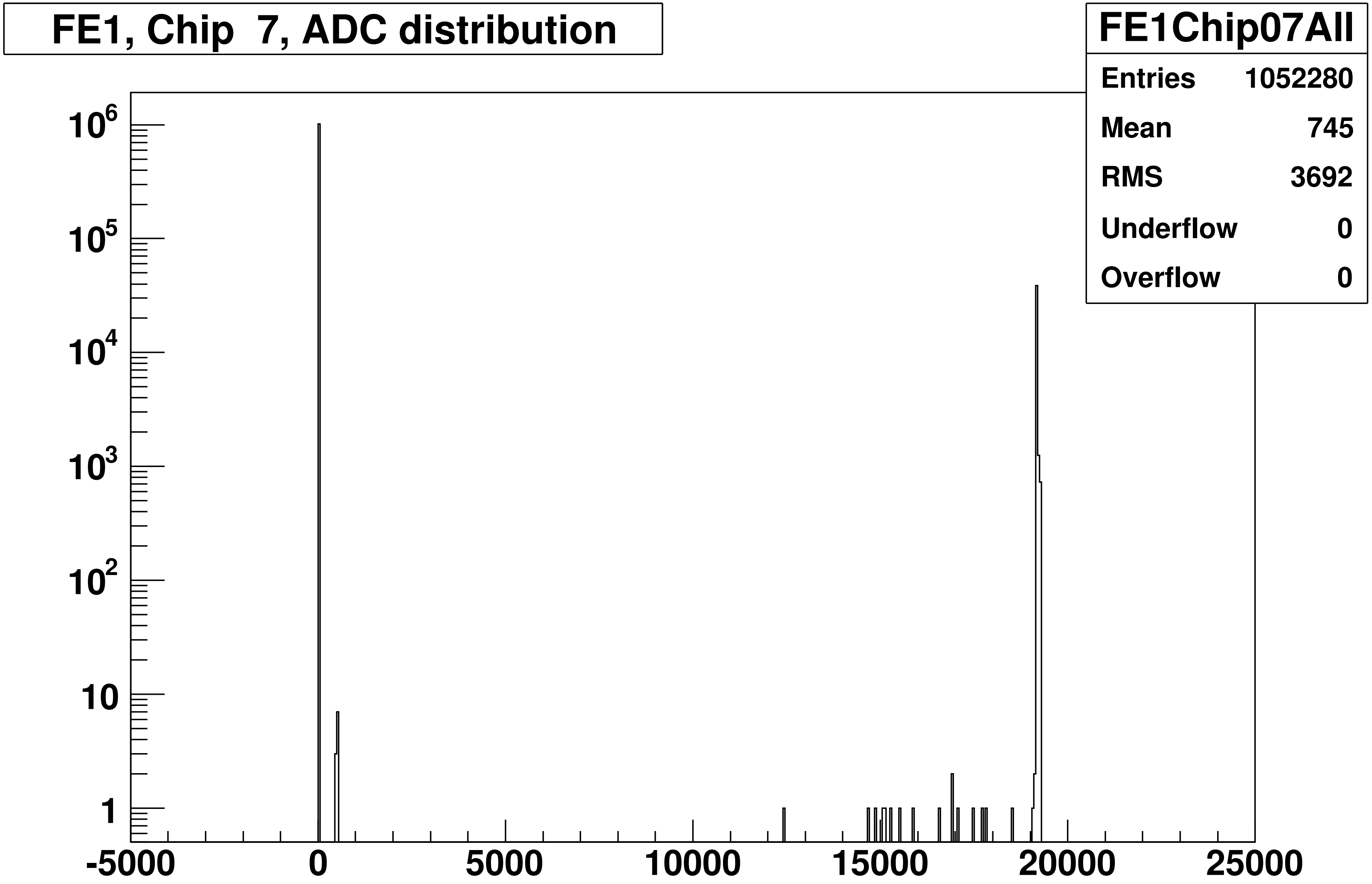
FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 1052280
Mean 765.6
RMS 3669
Underflow 0
Overflow 0
-5000
0
5000
10000
15000
20000
25000
1
10
10^2
10^3
10^4
10^5
10^6

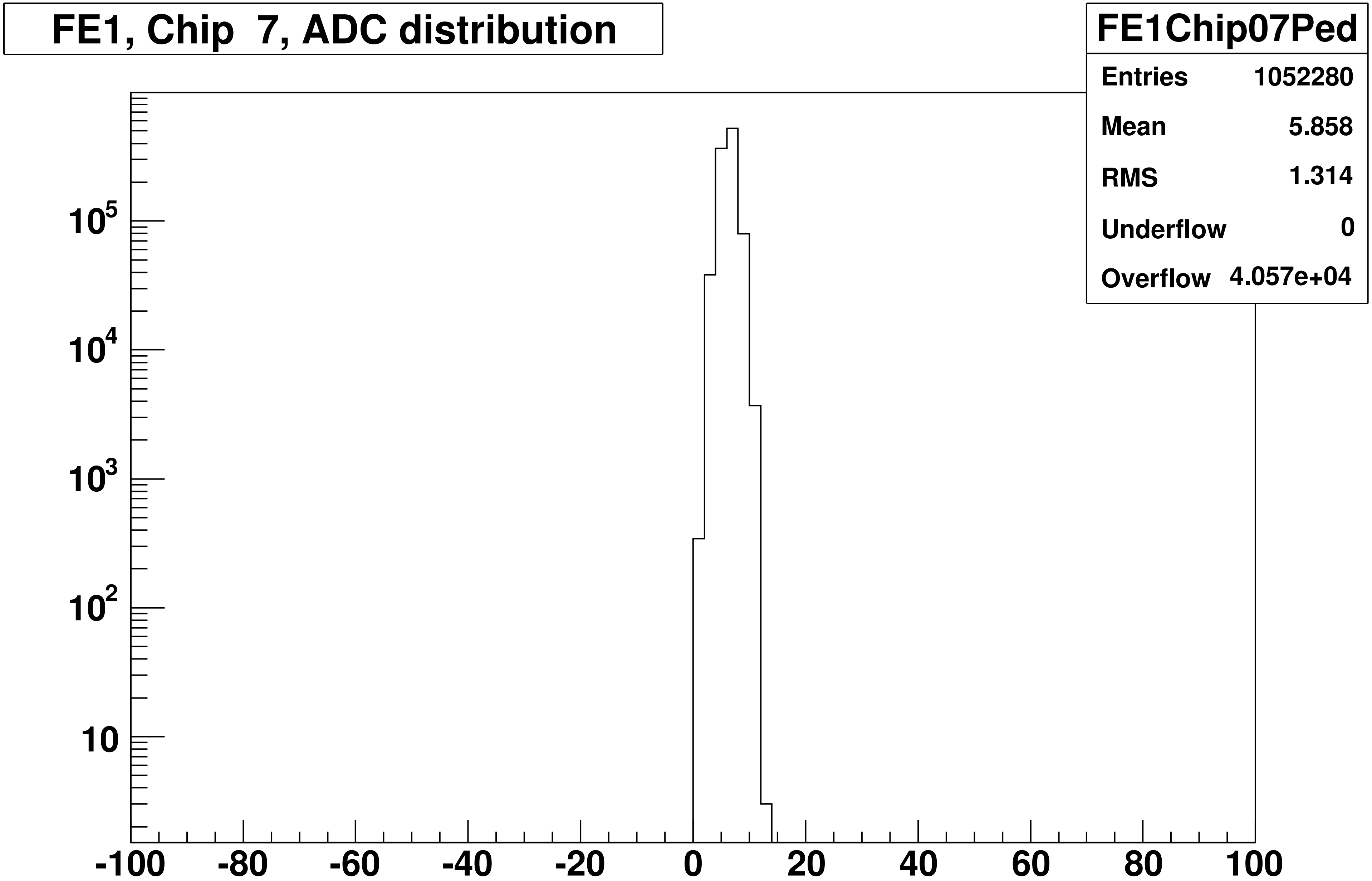


FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 1052280
Mean 30.88
RMS 1.457
Underflow 0
Overflow 4.057e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100

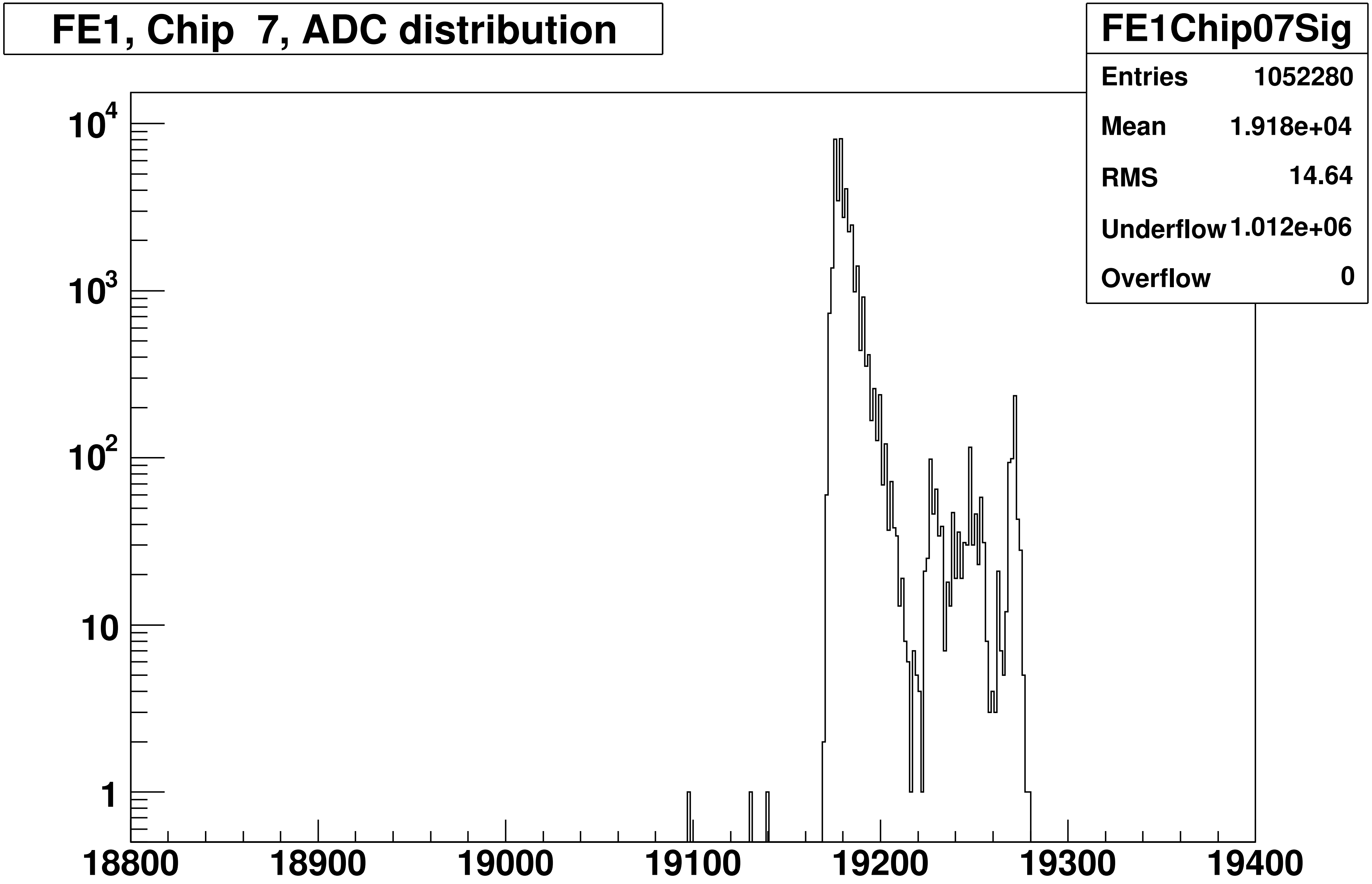


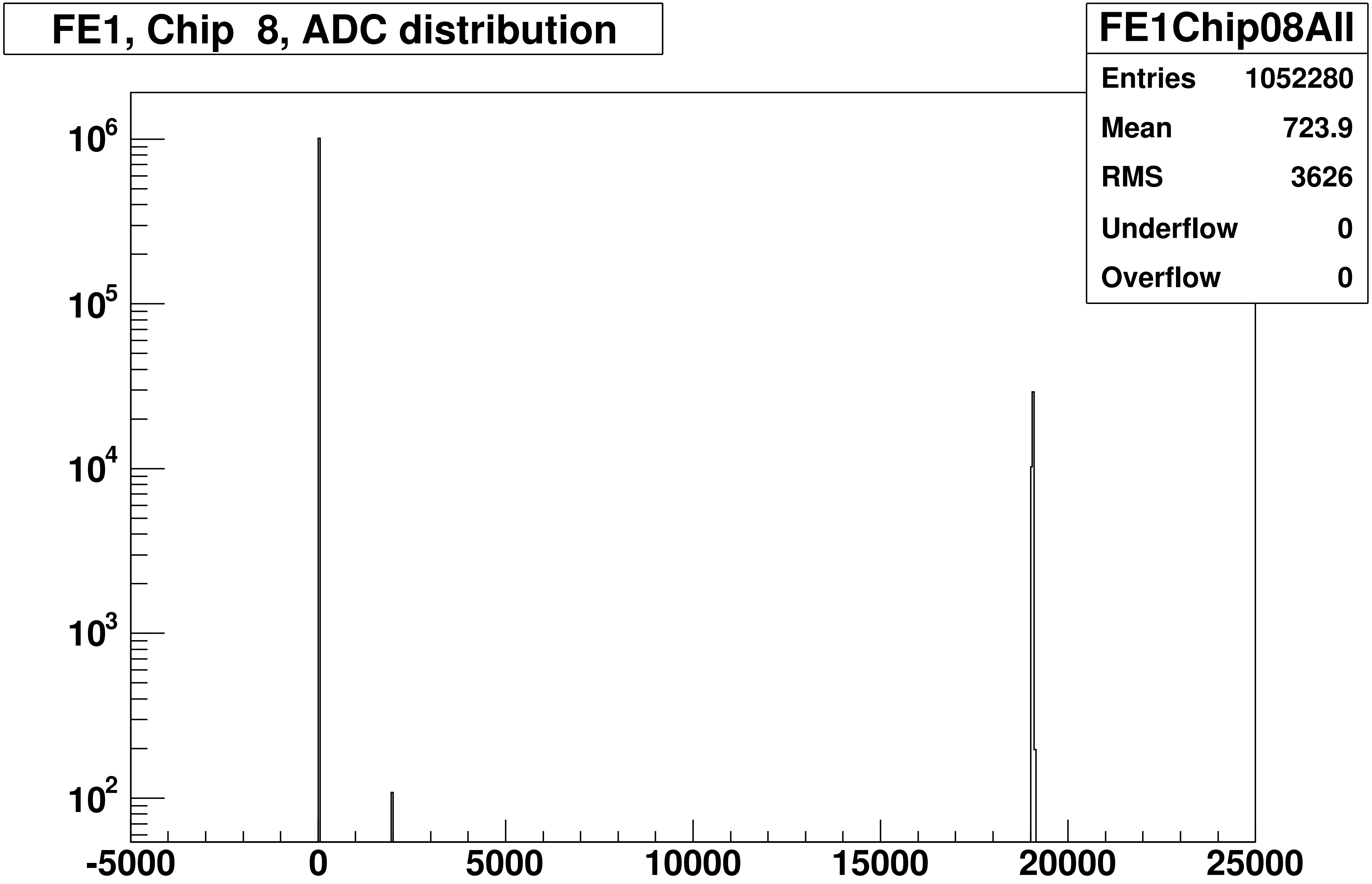
FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 1052280
Mean 1.909e+04
RMS 15.79
Underflow 1.012e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

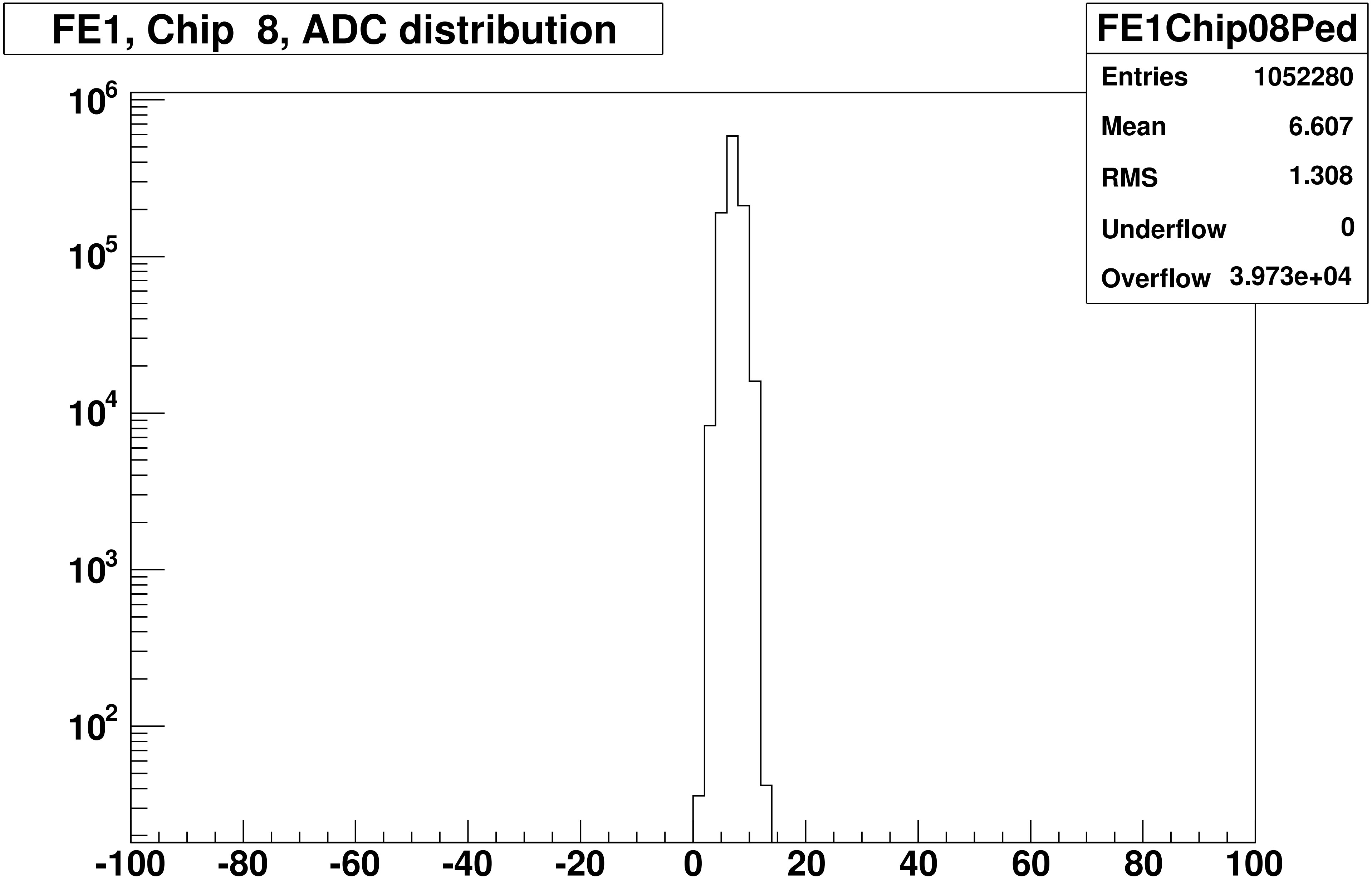

FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 1052280
Mean 745
RMS 3692
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



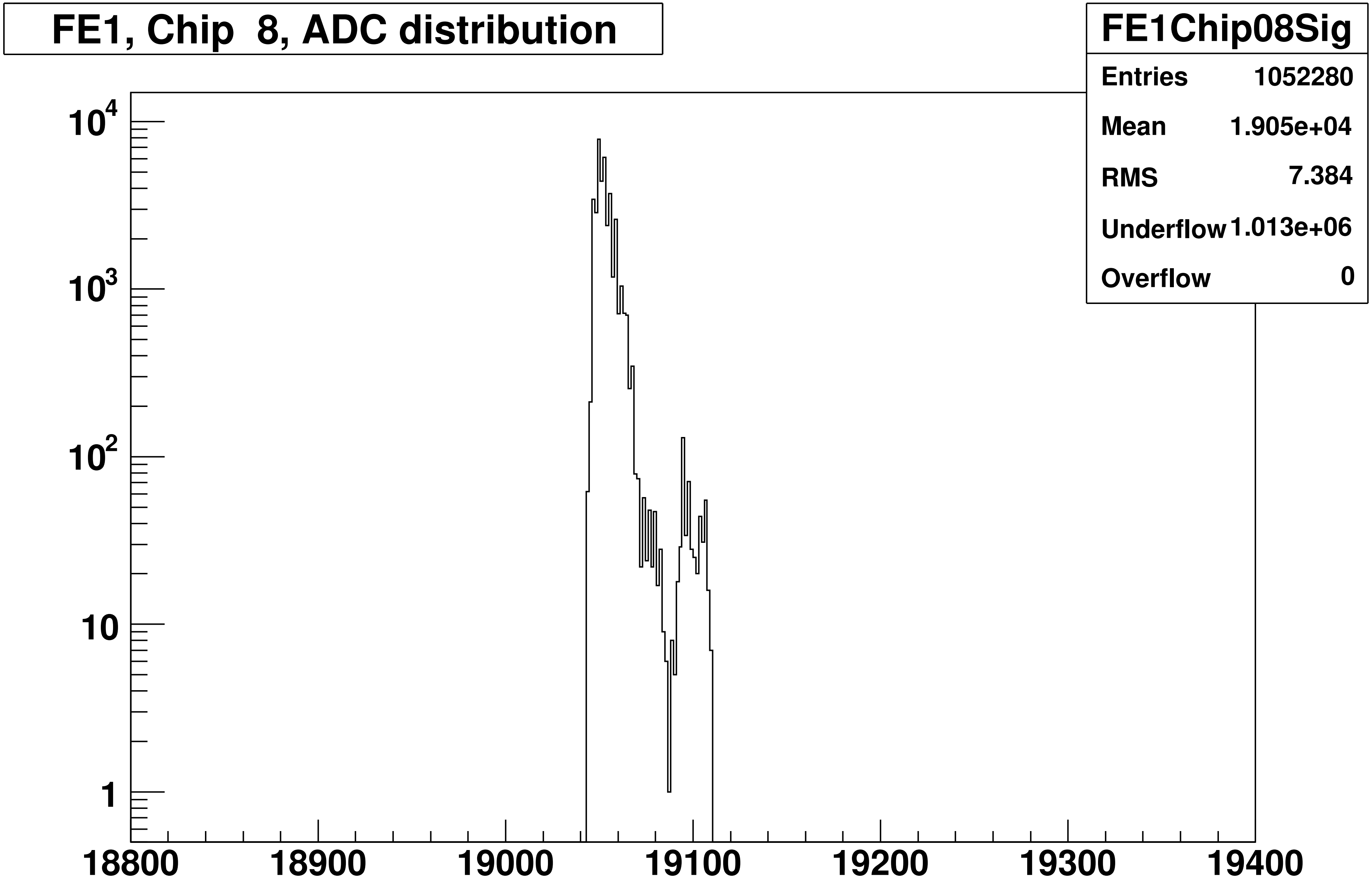
FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 1052280
Mean 5.858
RMS 1.314
Underflow 0
Overflow 4.057e+04
10^5
10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
100

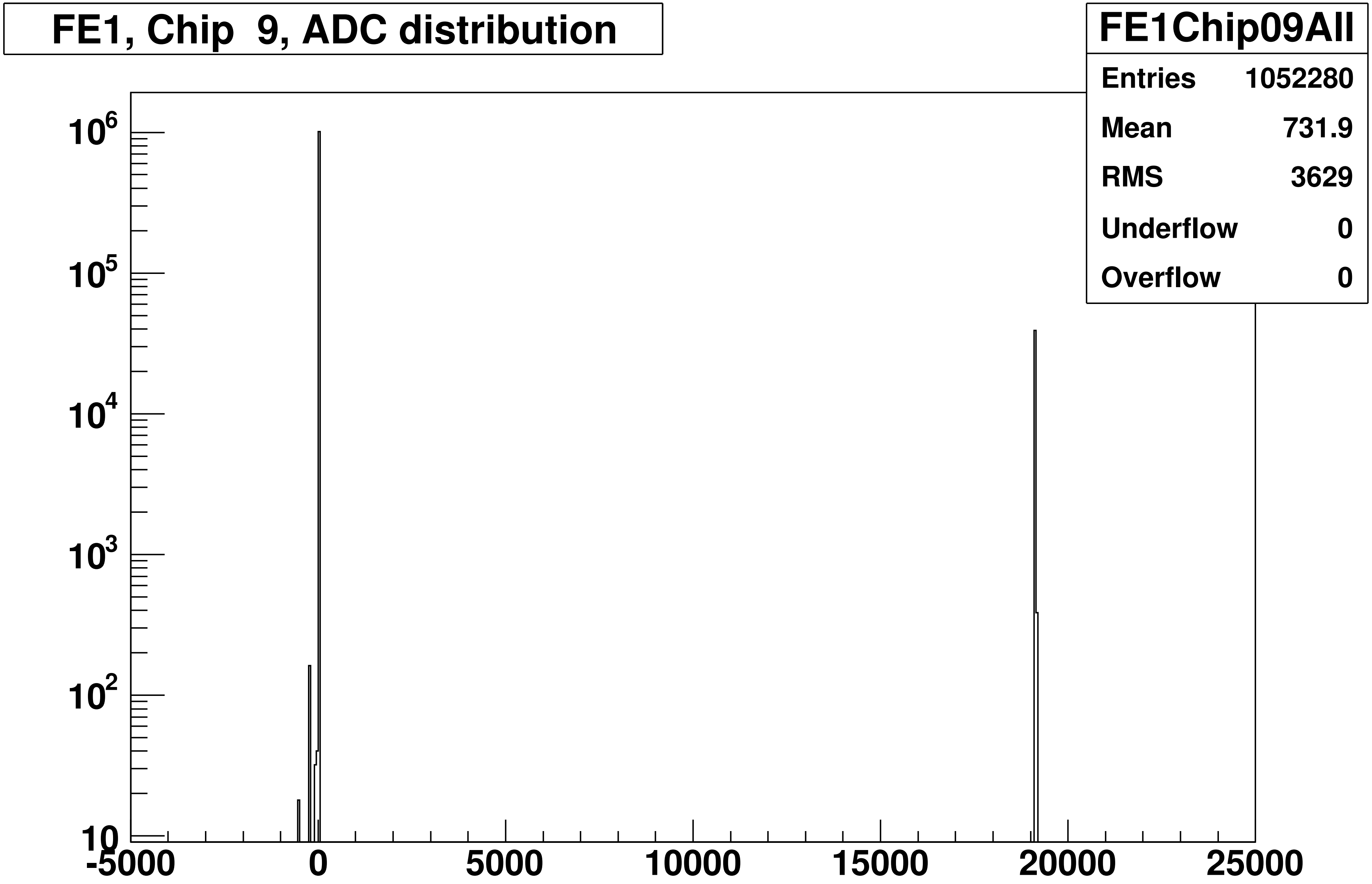

FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 1052280
Mean 1.918e+04
RMS 14.64
Underflow 1.012e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

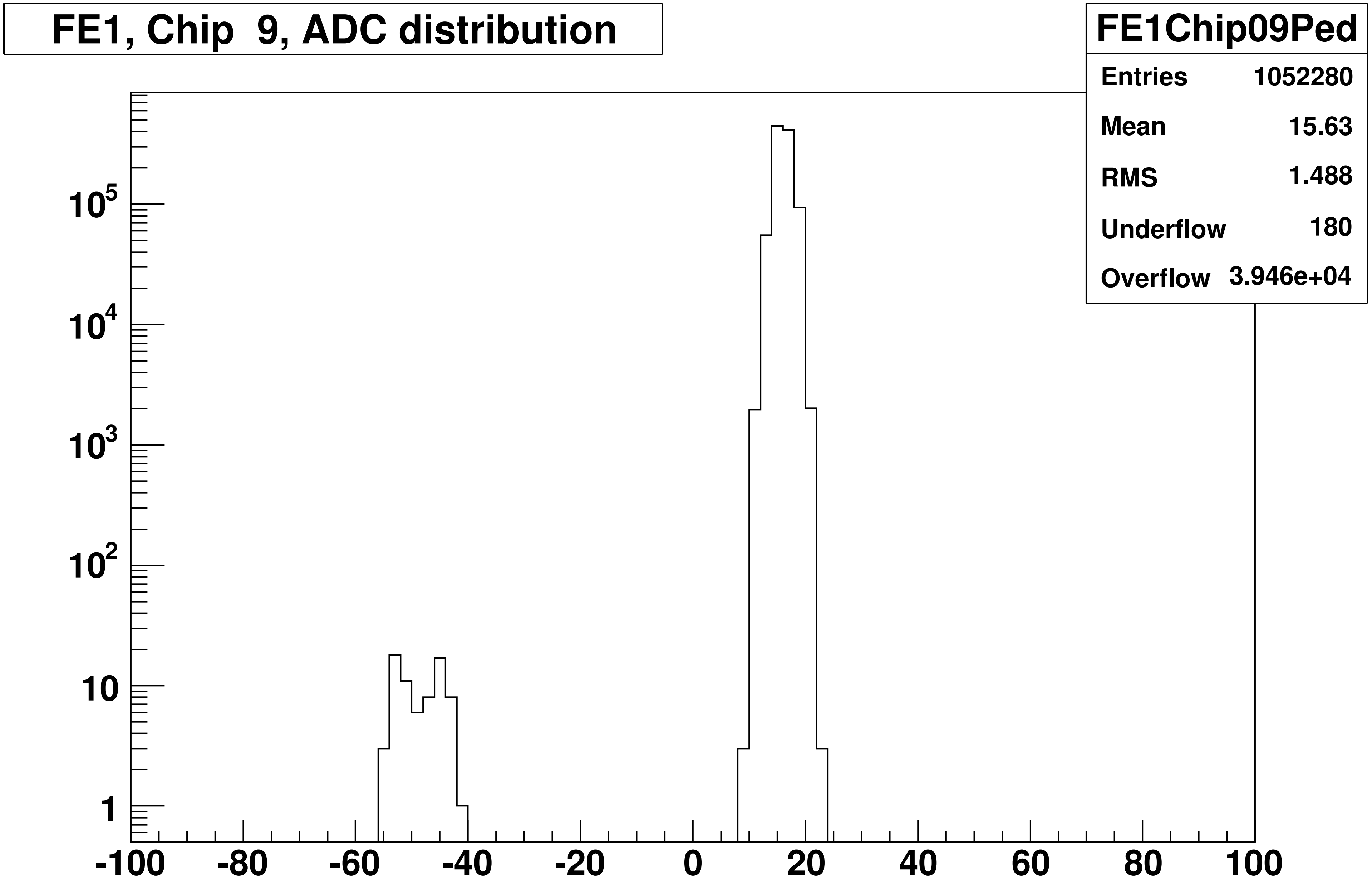

FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 1052280
Mean 723.9
RMS 3626
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



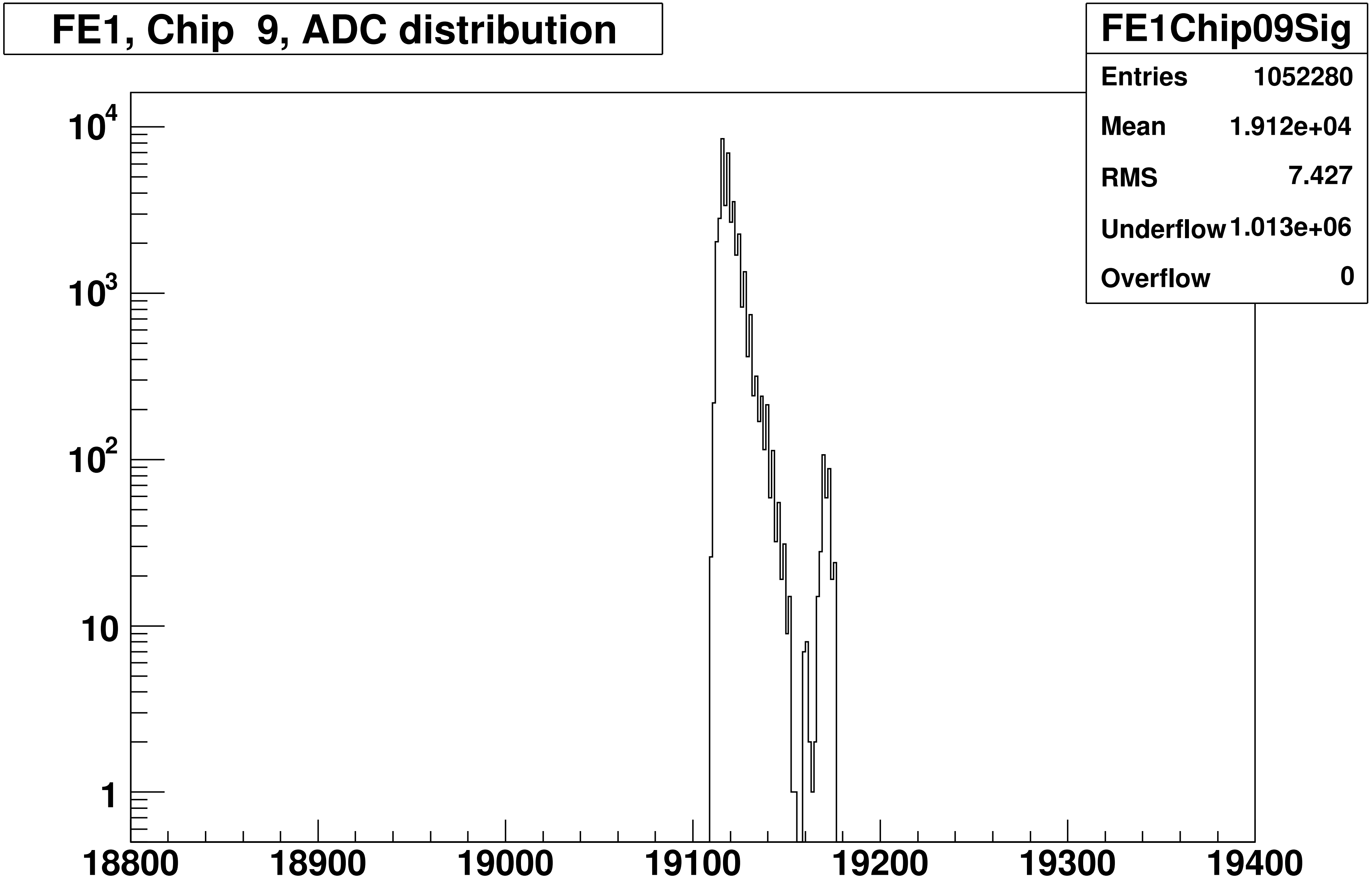
FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 1052280
Mean 6.607
RMS 1.308
Underflow 0
Overflow 3.973e+04
10^6
10^5
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 1052280
Mean 1.905e+04
RMS 7.384
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 1052280
Mean 731.9
RMS 3629
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 1052280
Mean 15.63
RMS 1.488
Underflow 180
Overflow 3.946e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 1052280
Mean 1.912e+04
RMS 7.427
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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19100
19200
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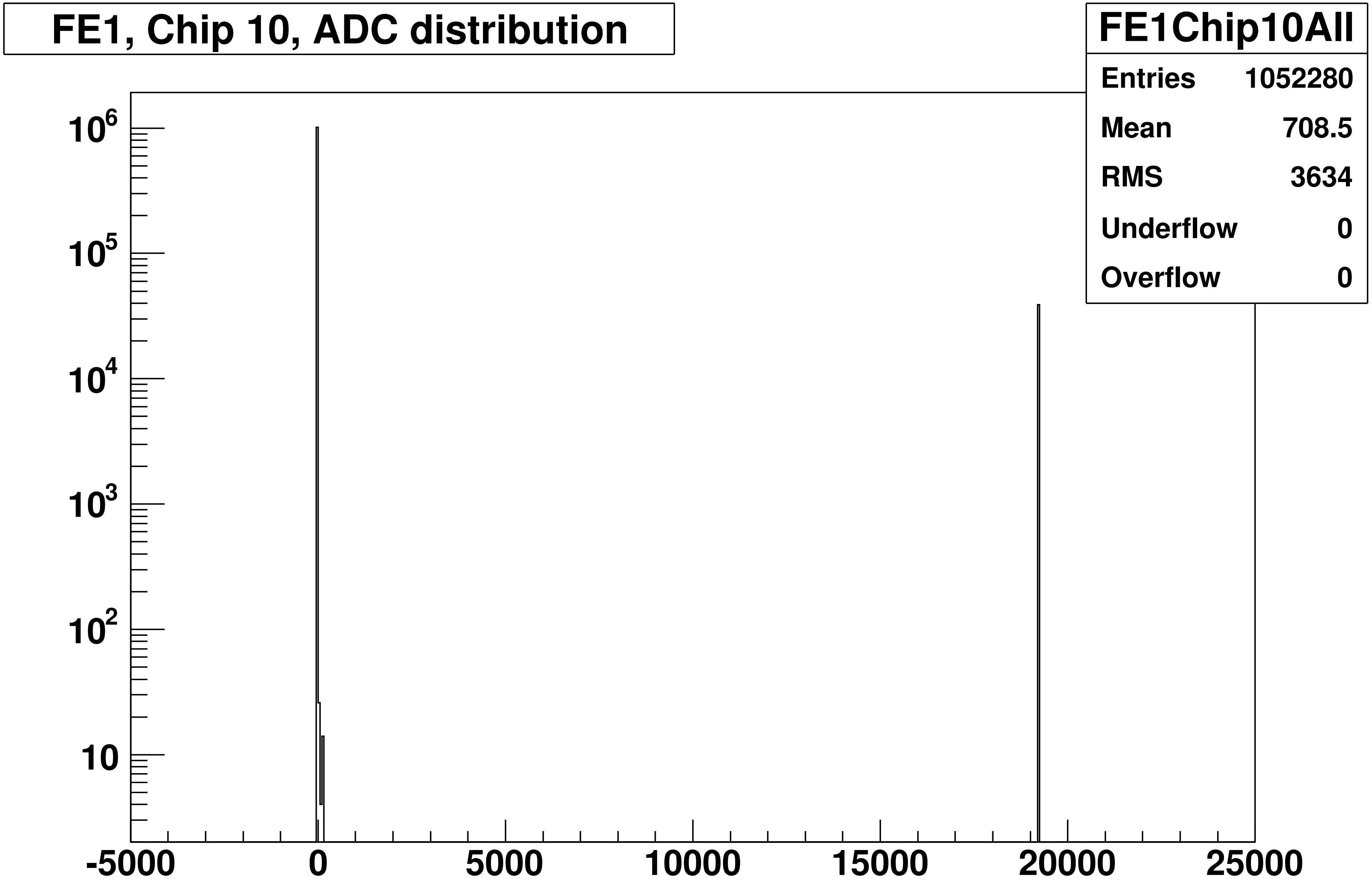
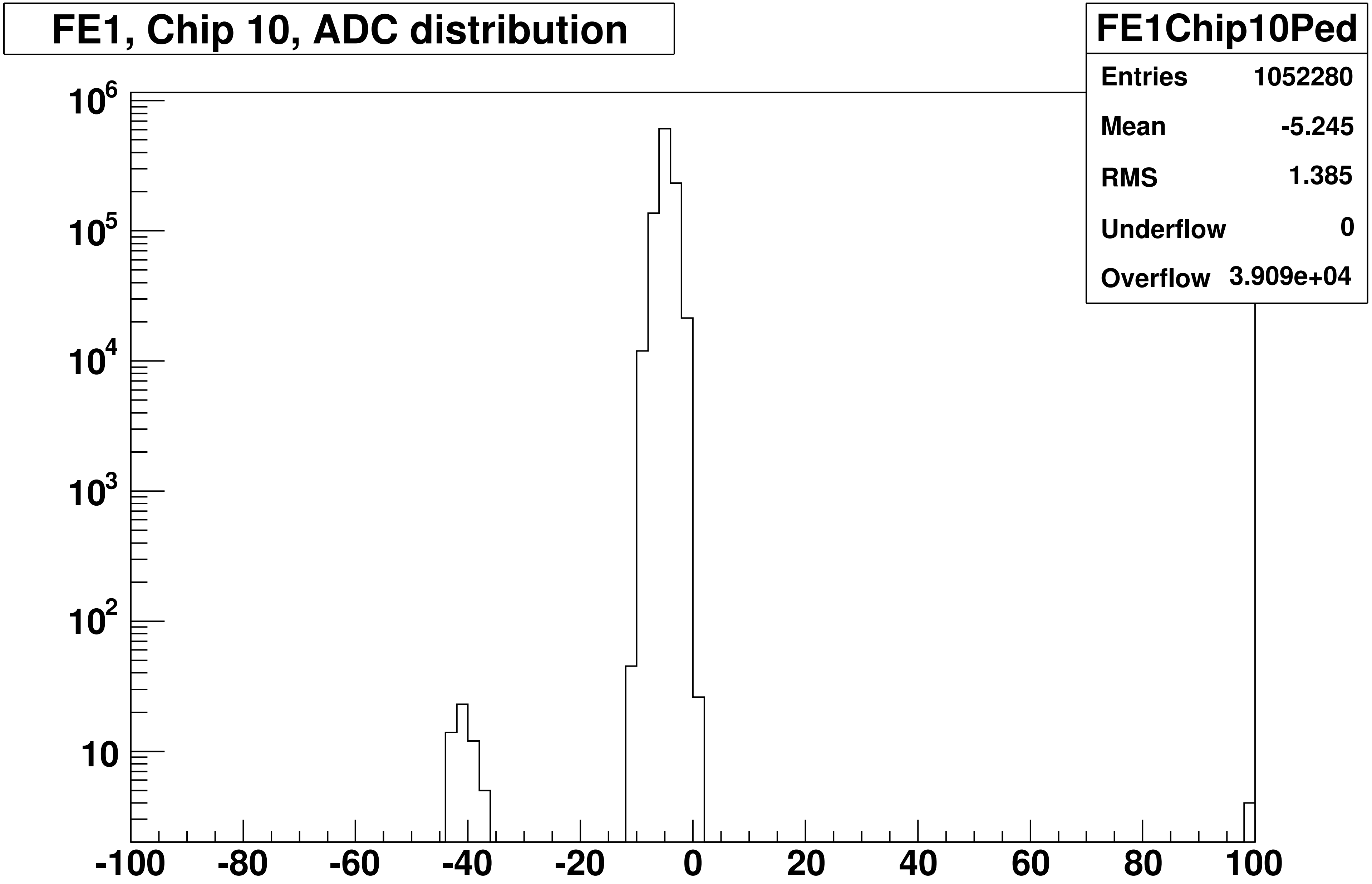
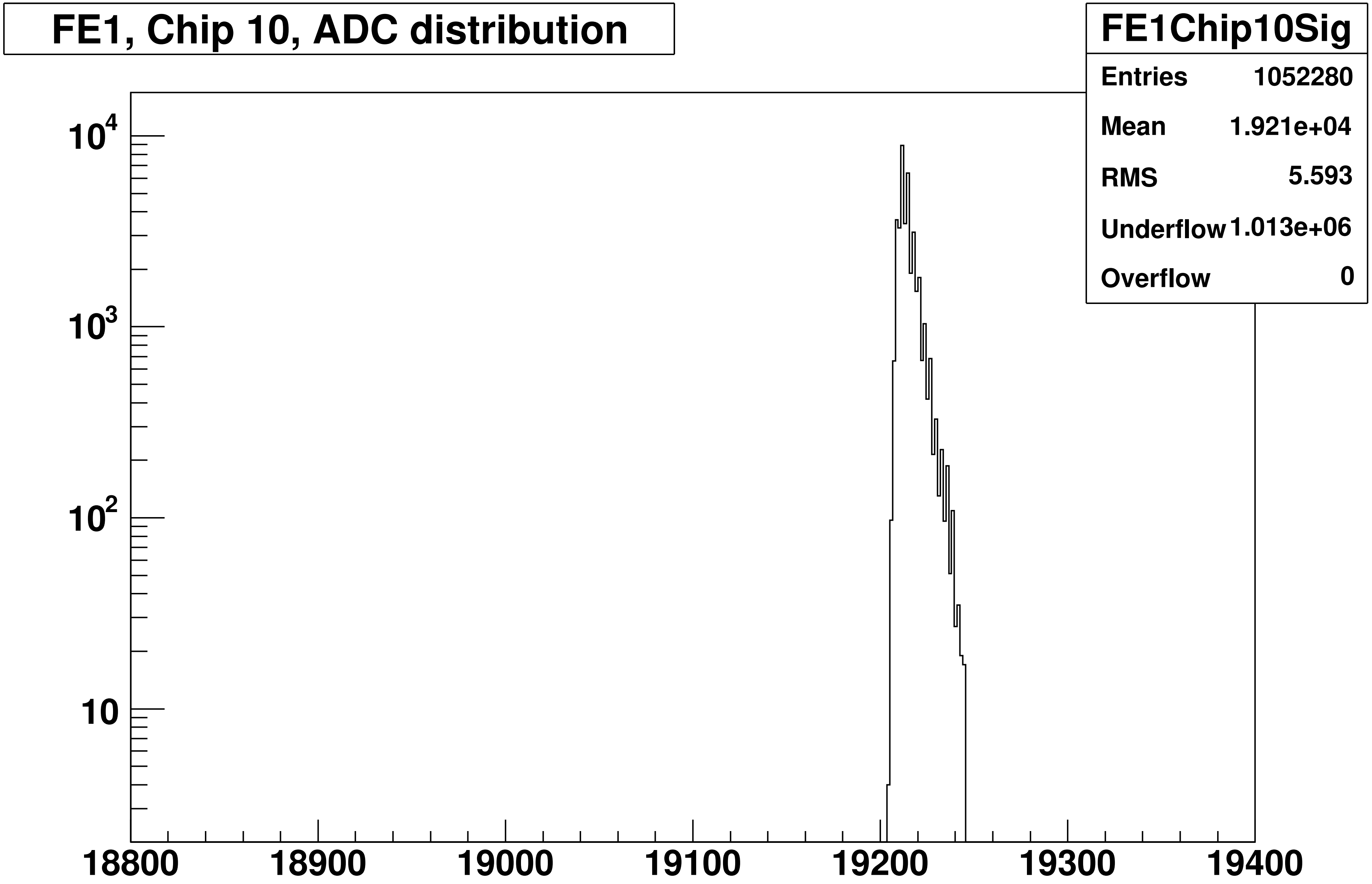
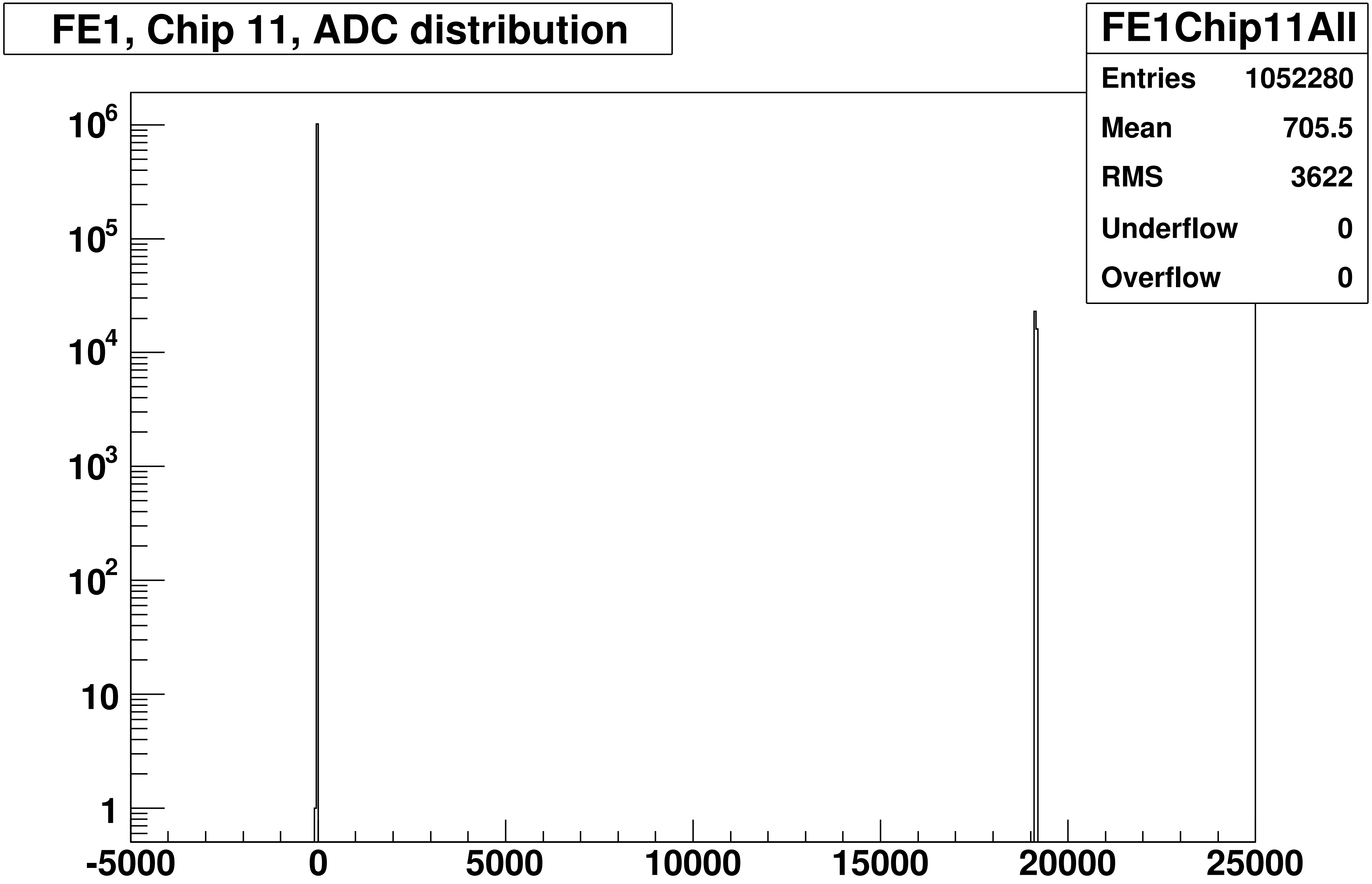
19400

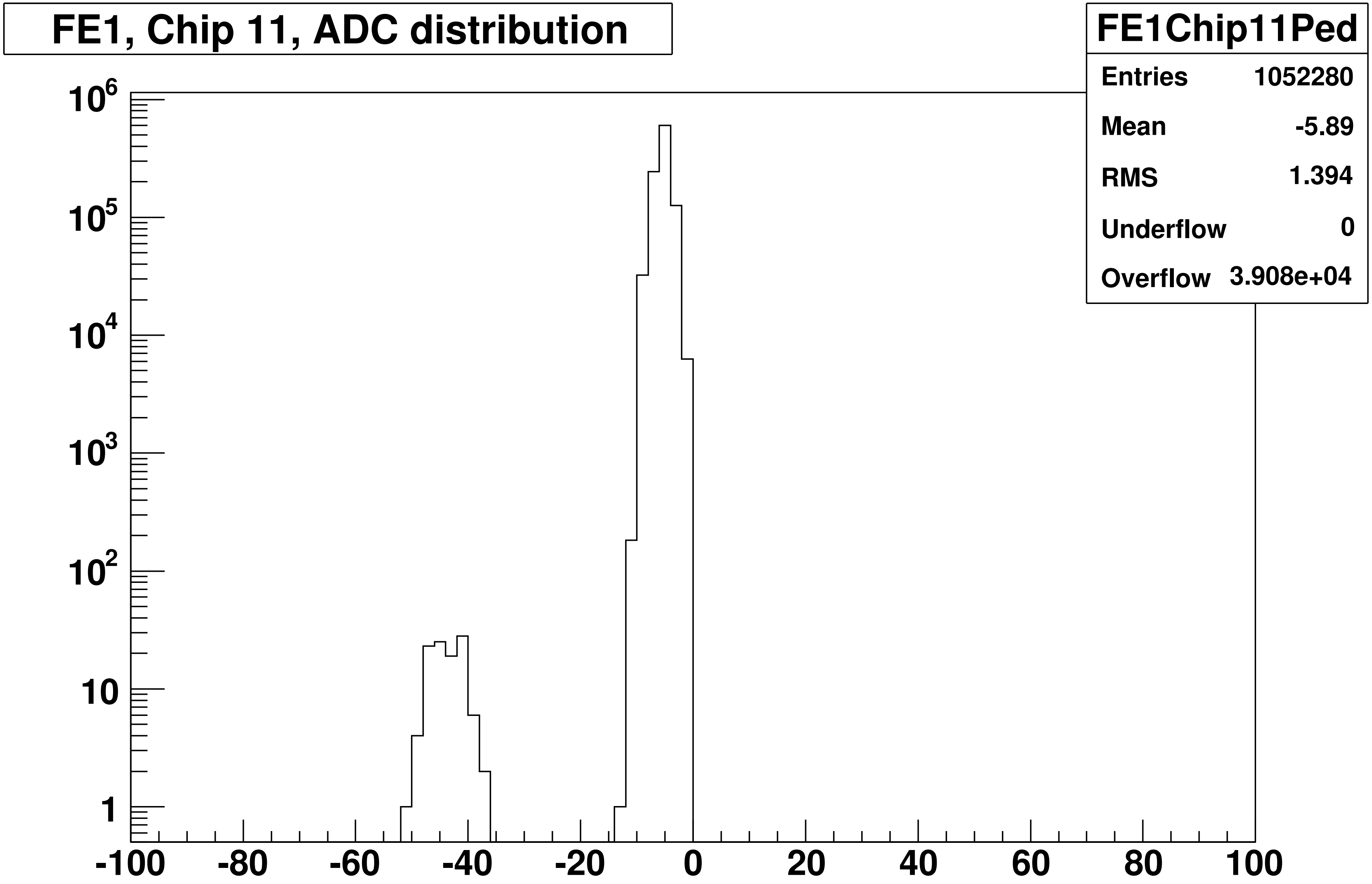


FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 1052280
Mean 708.5
RMS 3634
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 1052280
Mean -5.245
RMS 1.385
Underflow 0
Overflow 3.909e+04
10^6
10^5
10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 1052280
Mean 1.921e+04
RMS 5.593
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
18800
18900
19000
19100
19200
19300
19400


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 1052280
Mean 705.5
RMS 3622
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 1052280
Mean -5.89
RMS 1.394
Underflow 0
Overflow 3.908e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
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-20
0
20
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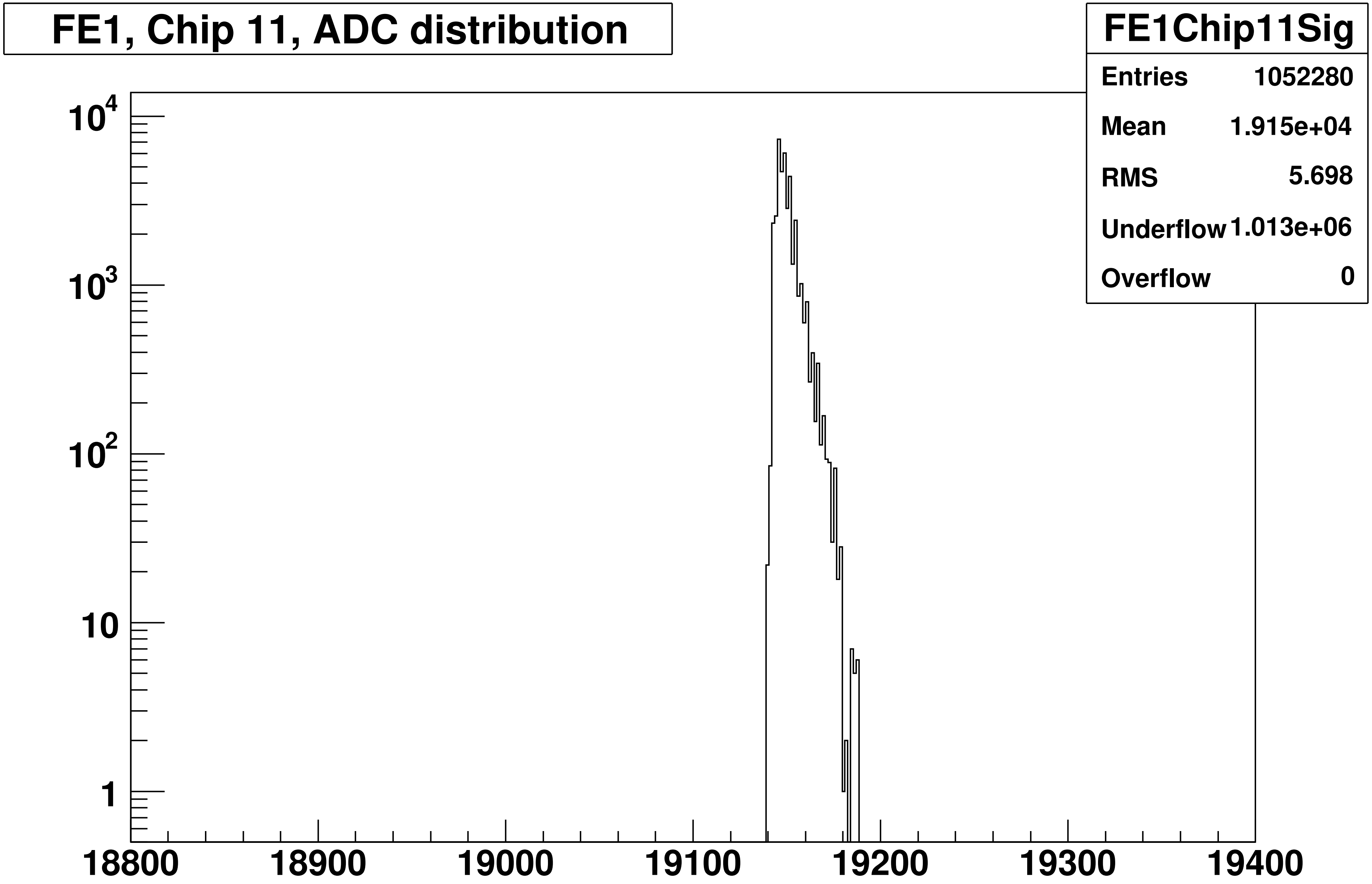
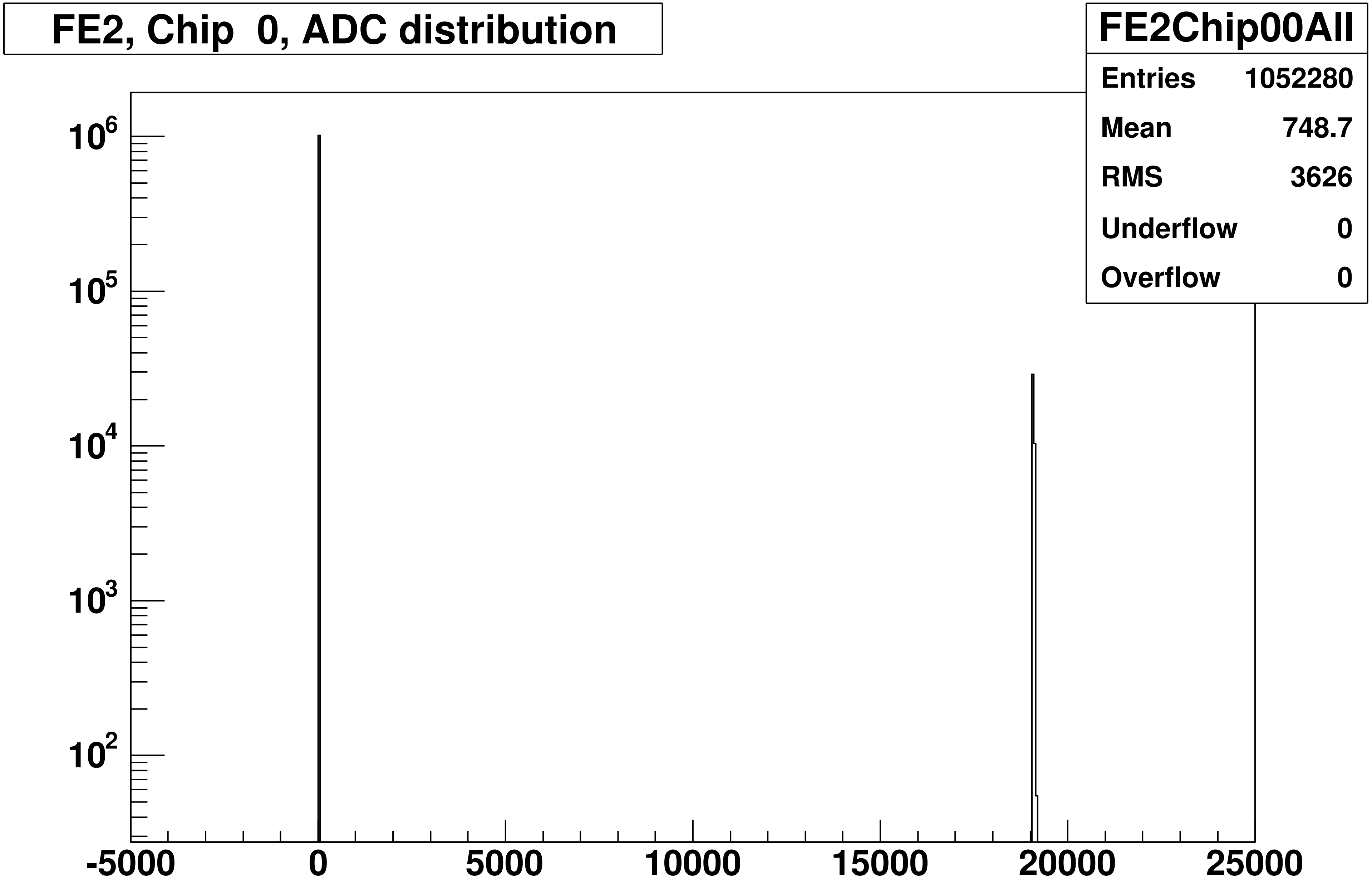
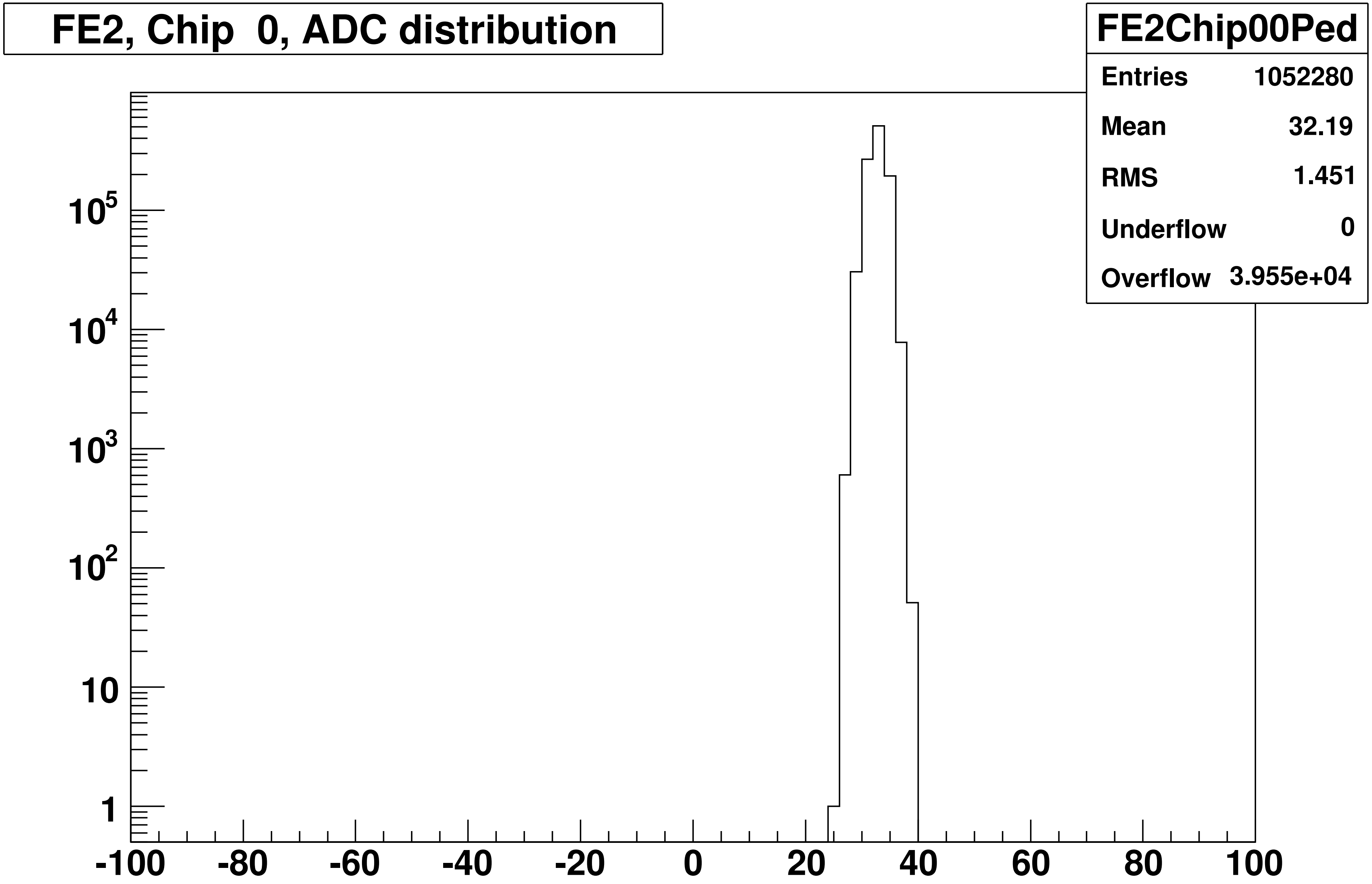
60
80
100

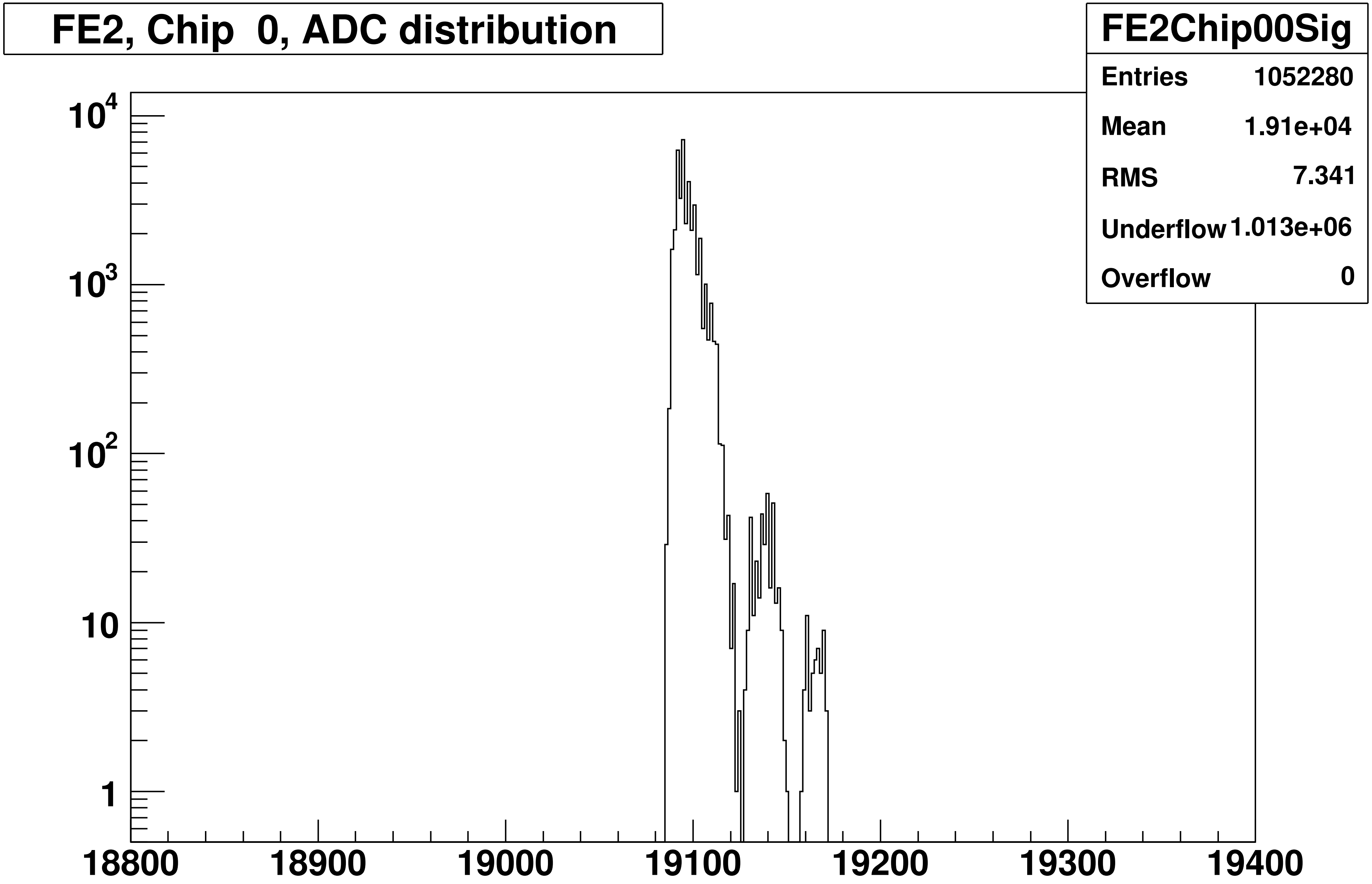

FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 1052280
Mean 1.915e+04
RMS 5.698
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



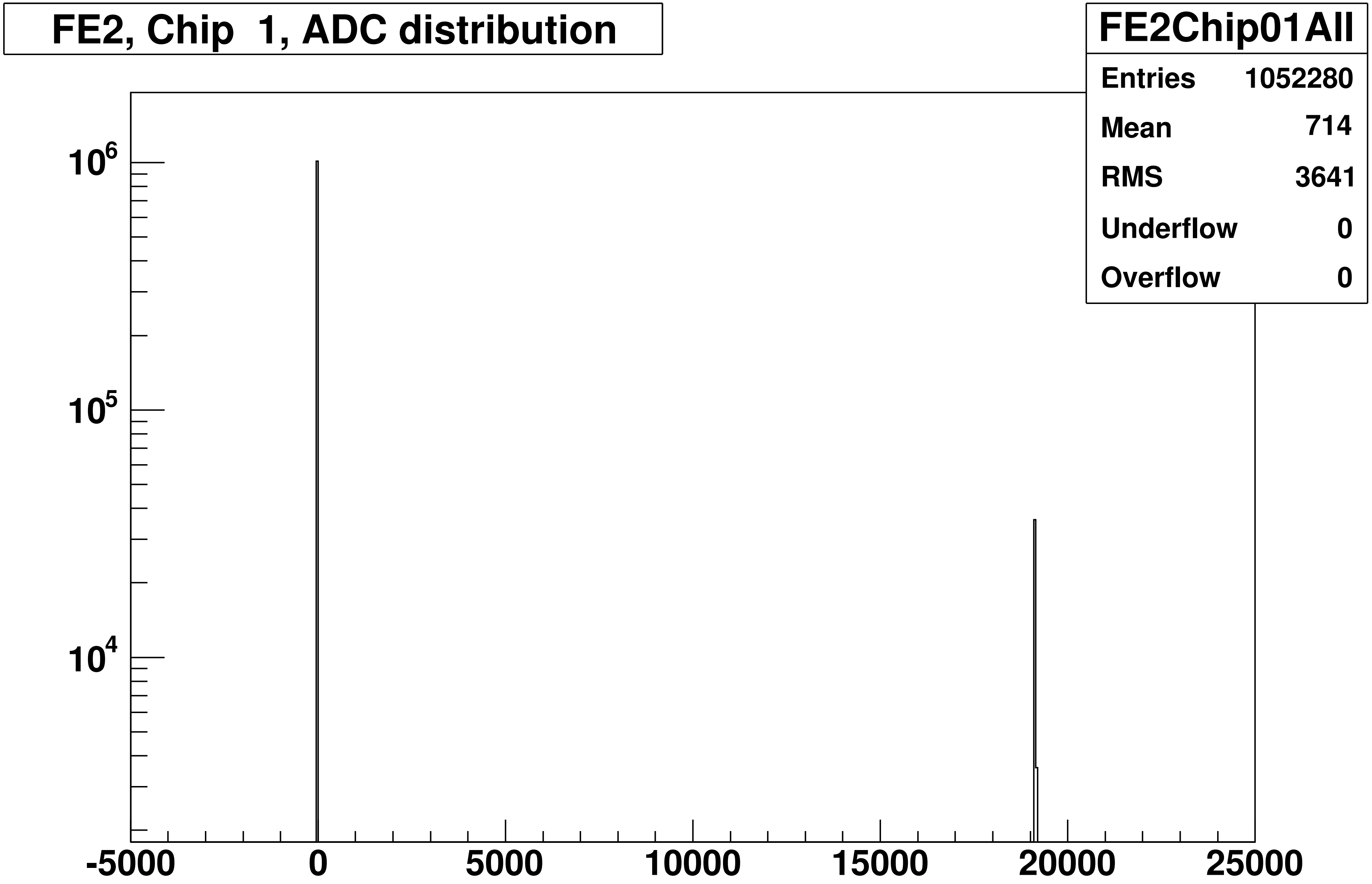
FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 1052280
Mean 748.7
RMS 3626
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



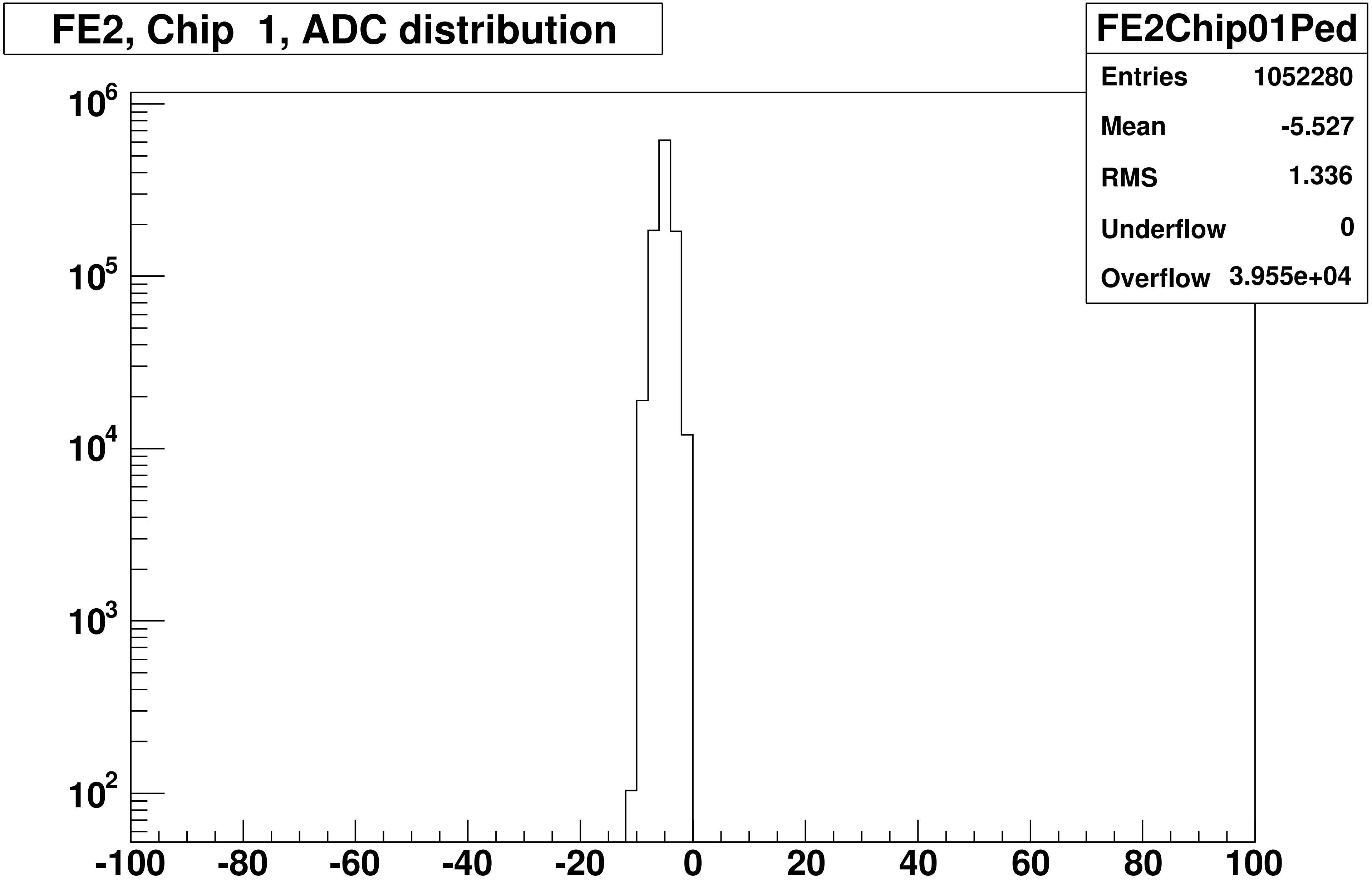
FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 1052280
Mean 32.19
RMS 1.451
Underflow 0
Overflow 3.955e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100

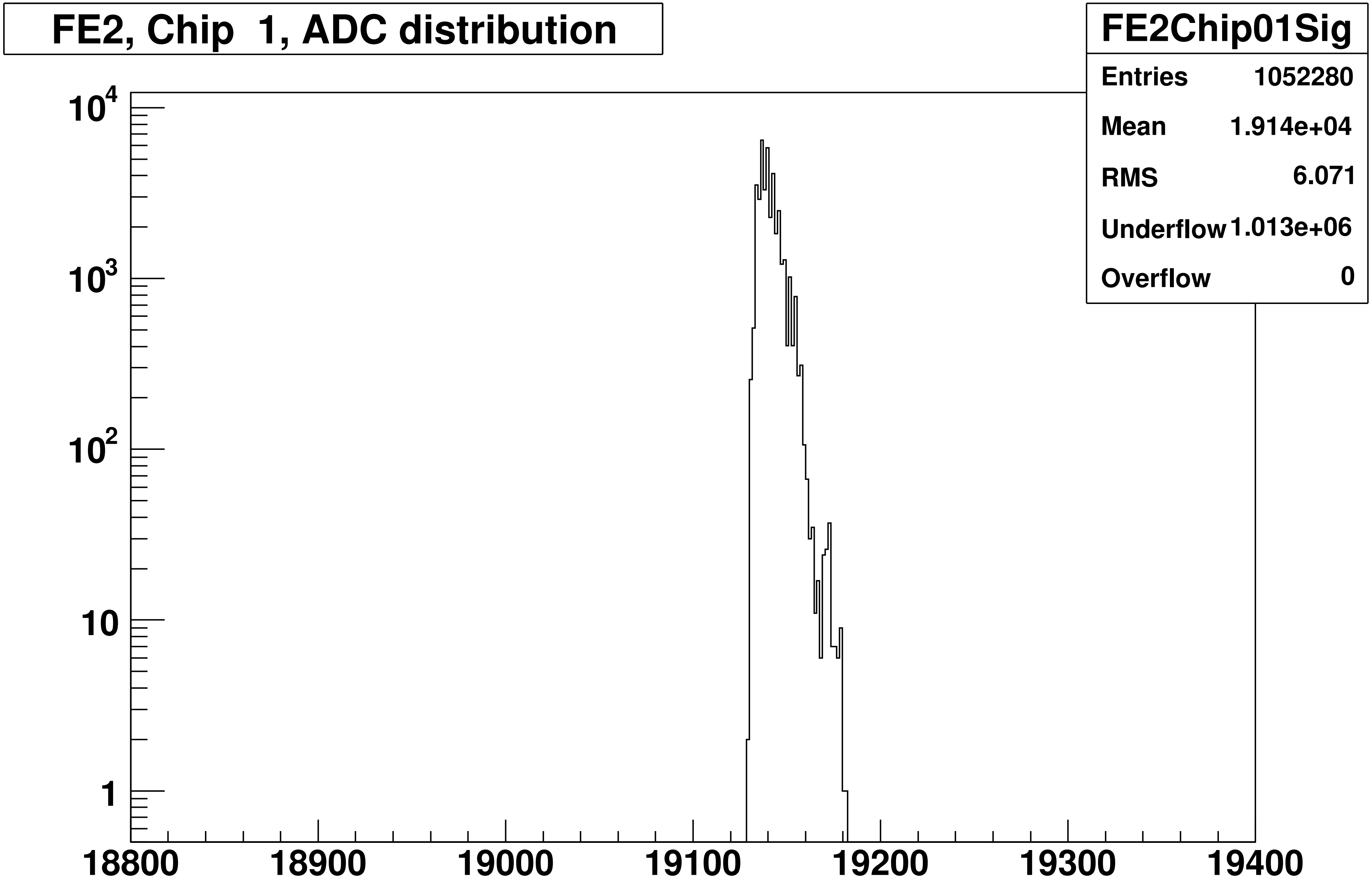


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 1052280
Mean 1.91e+04
RMS 7.341
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

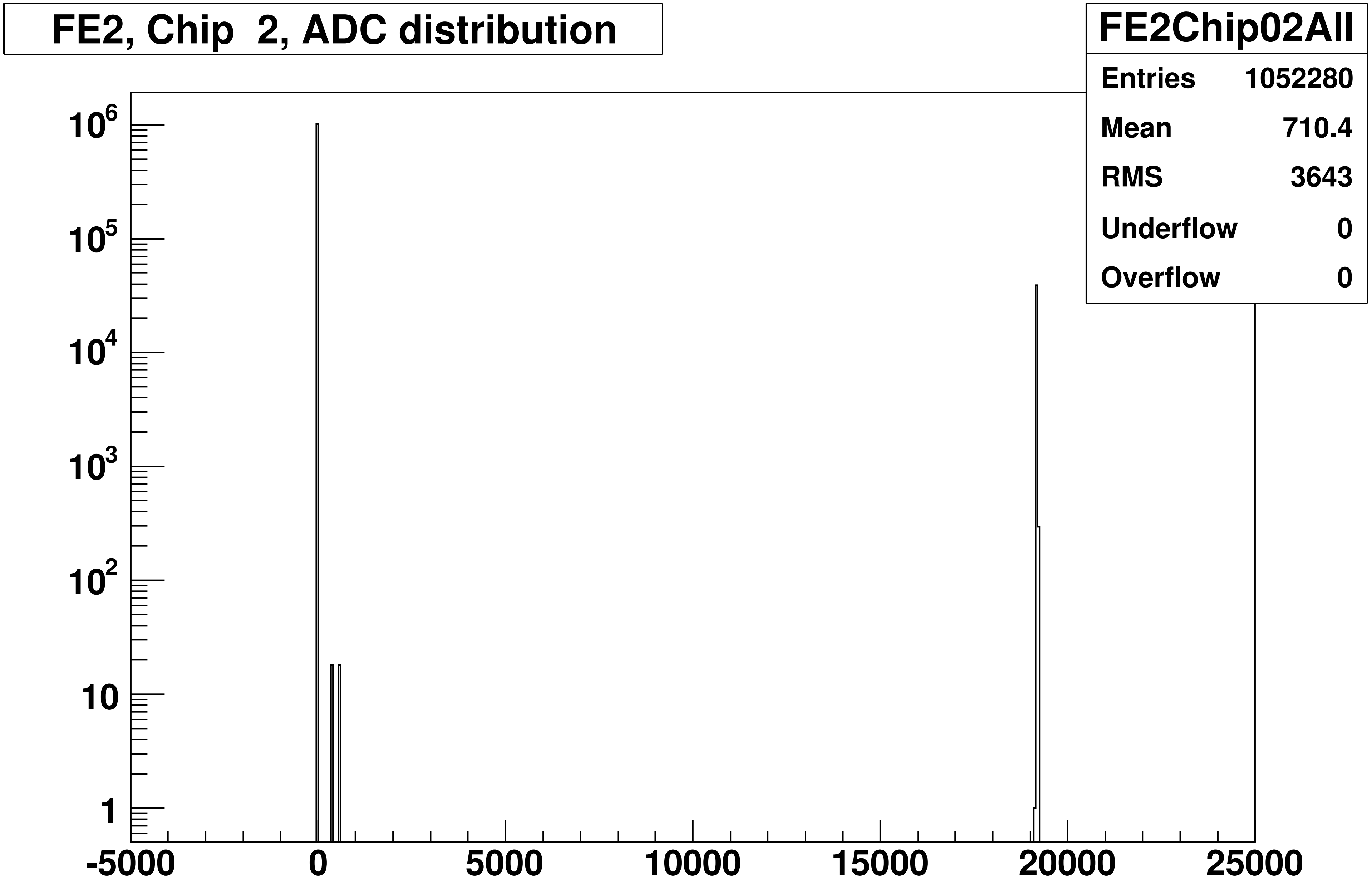


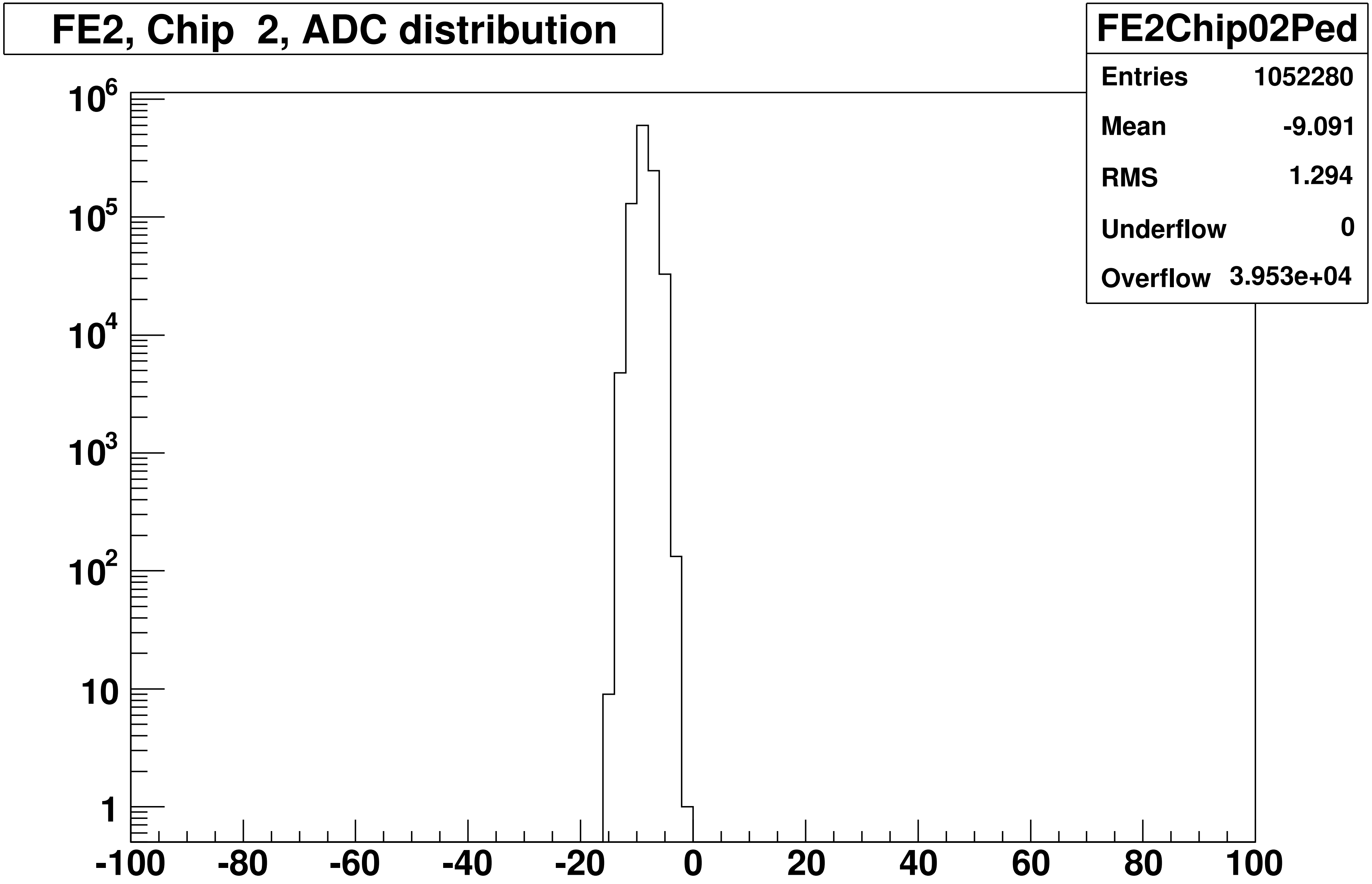
FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 1052280
Mean 714
RMS 3641
Underflow 0
Overflow 0
10^6
10^5
10^4
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 1052280
Mean -5.527
RMS 1.336
Underflow 0
Overflow 3.955e+04
10^6
10^5
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 1052280
Mean 1.914e+04
RMS 6.071
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 1052280
Mean 710.4
RMS 3643
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 1052280
Mean -9.091
RMS 1.294
Underflow 0
Overflow 3.953e+04
10^6
10^5
10^4
10^3
10^2
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1
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80
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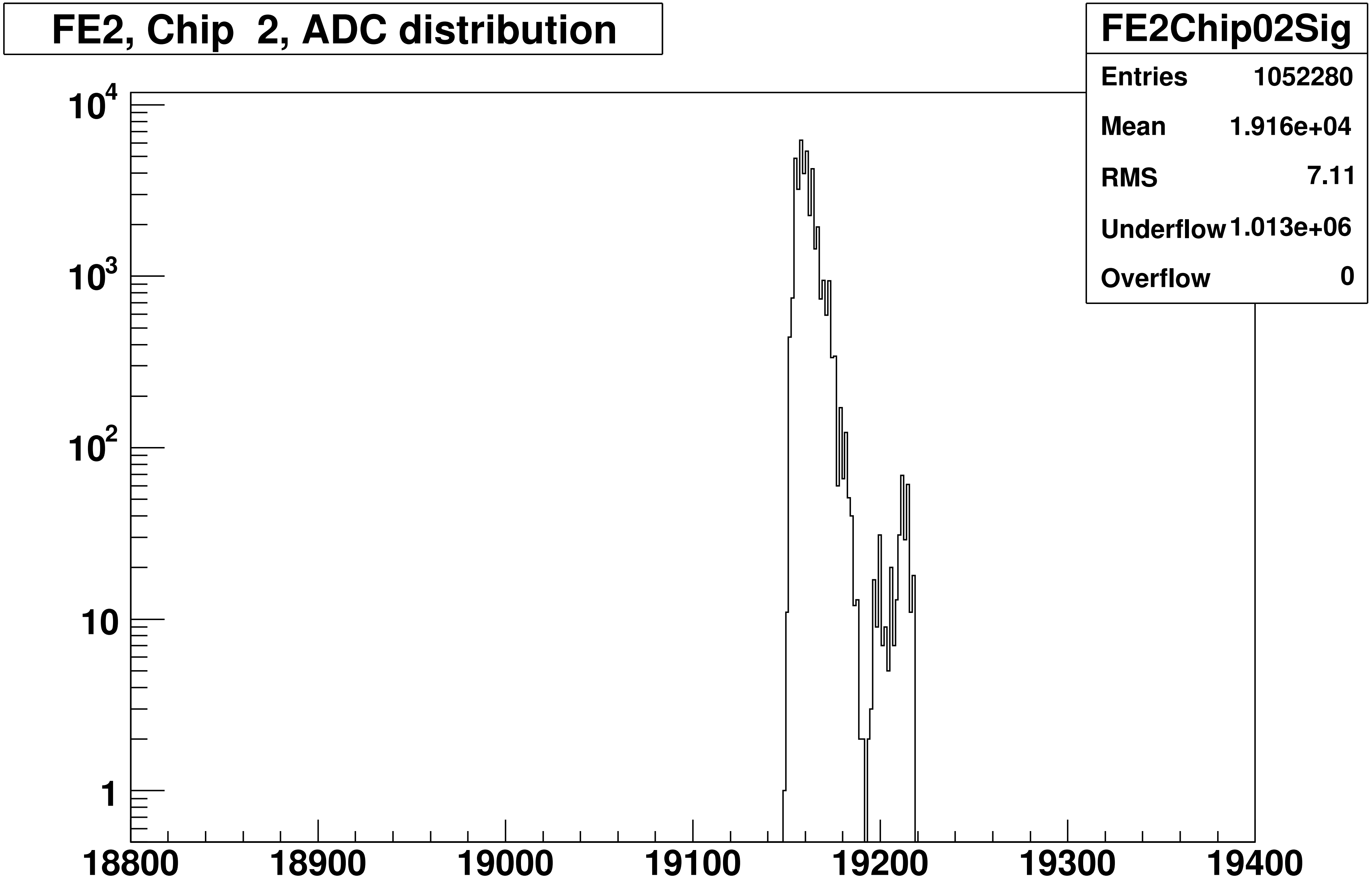

FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 1052280
Mean 1.916e+04
RMS 7.11
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
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18800
18900
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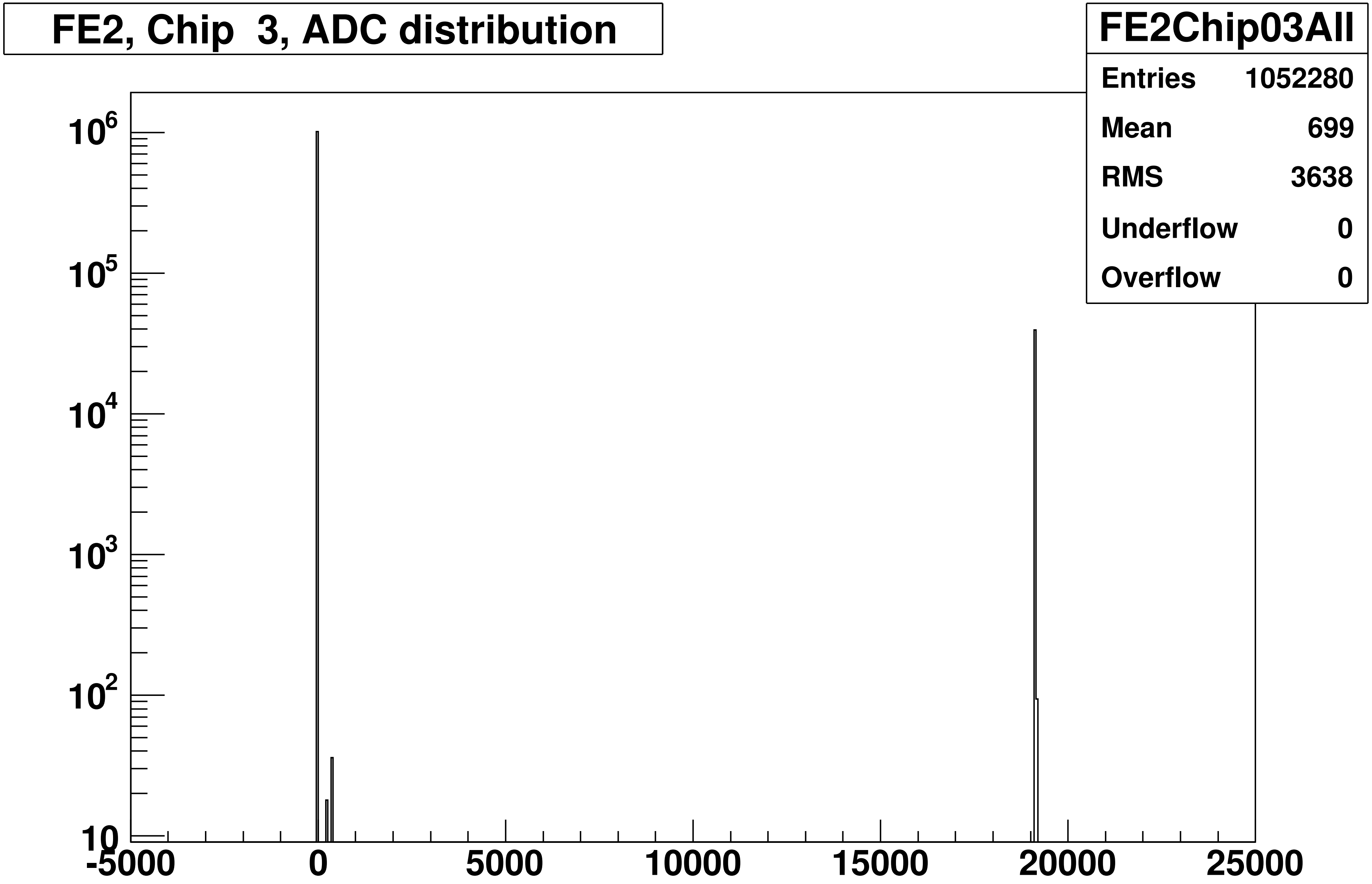

FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 1052280
Mean 699
RMS 3638
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
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5000
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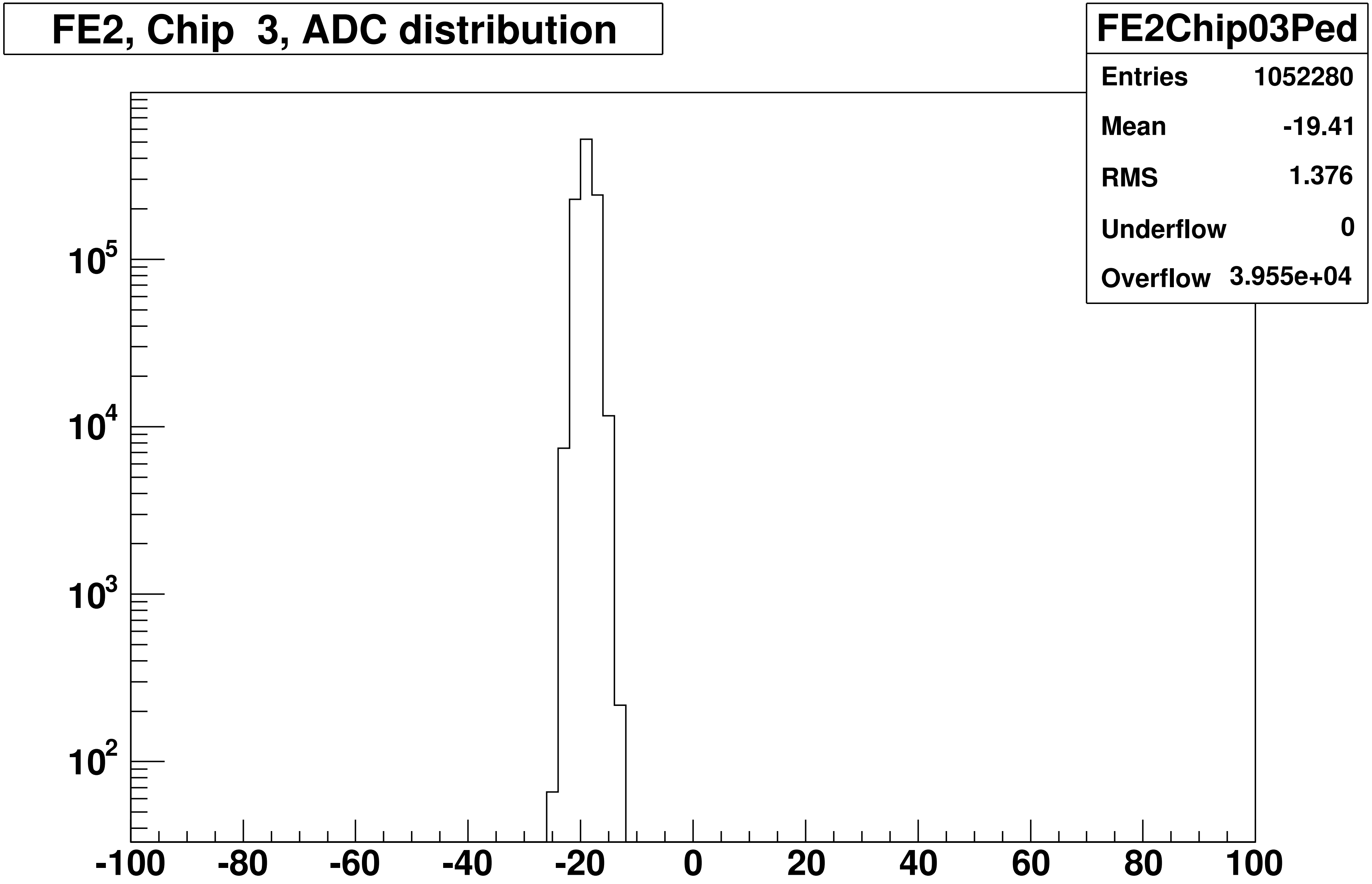
20000
25000



FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 1052280
Mean -19.41
RMS 1.376
Underflow 0
Overflow 3.955e+04
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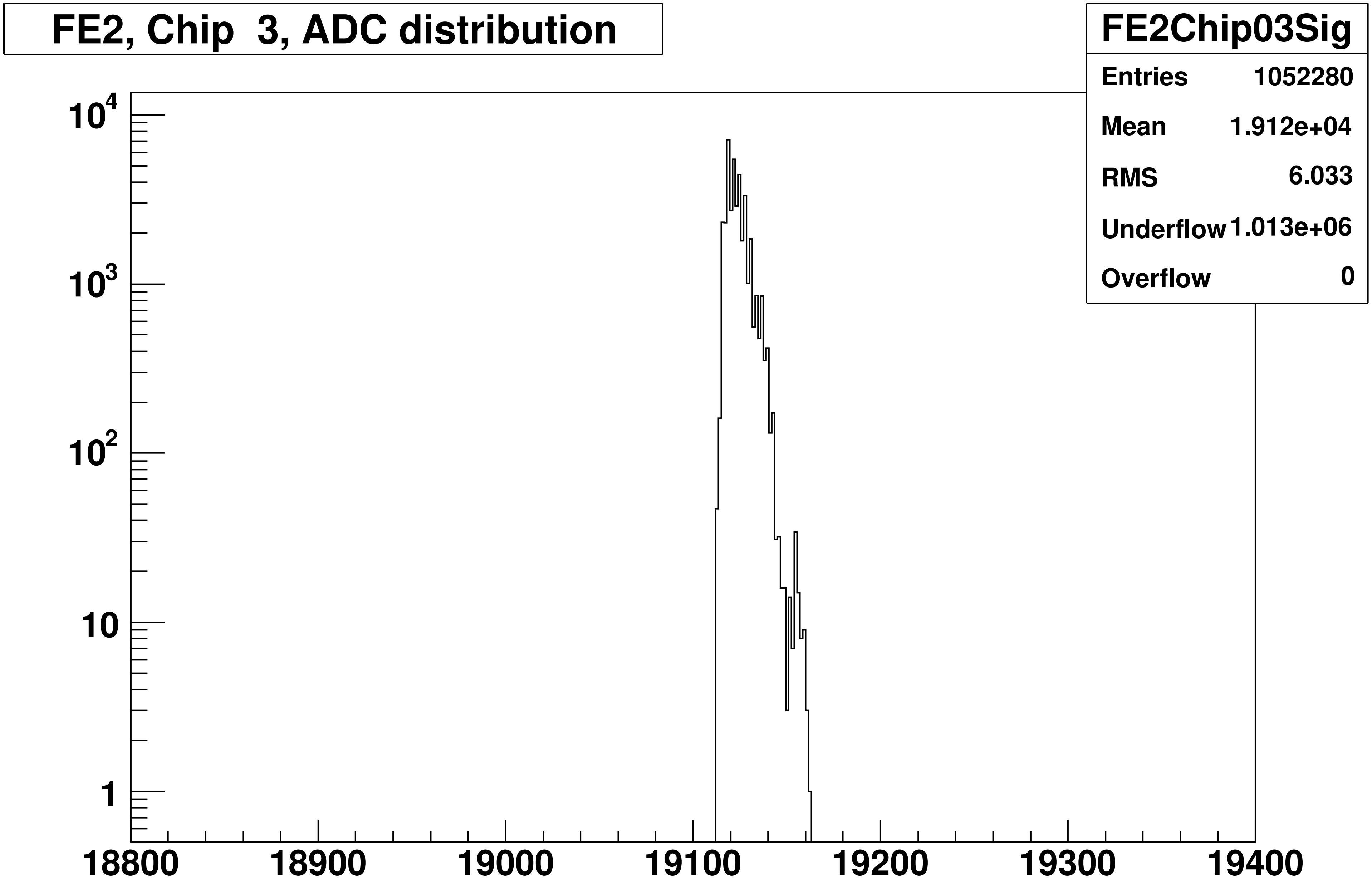
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 1052280
Mean 1.912e+04
RMS 6.033
Underflow 1.013e+06
Overflow 0
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10^3
10^2
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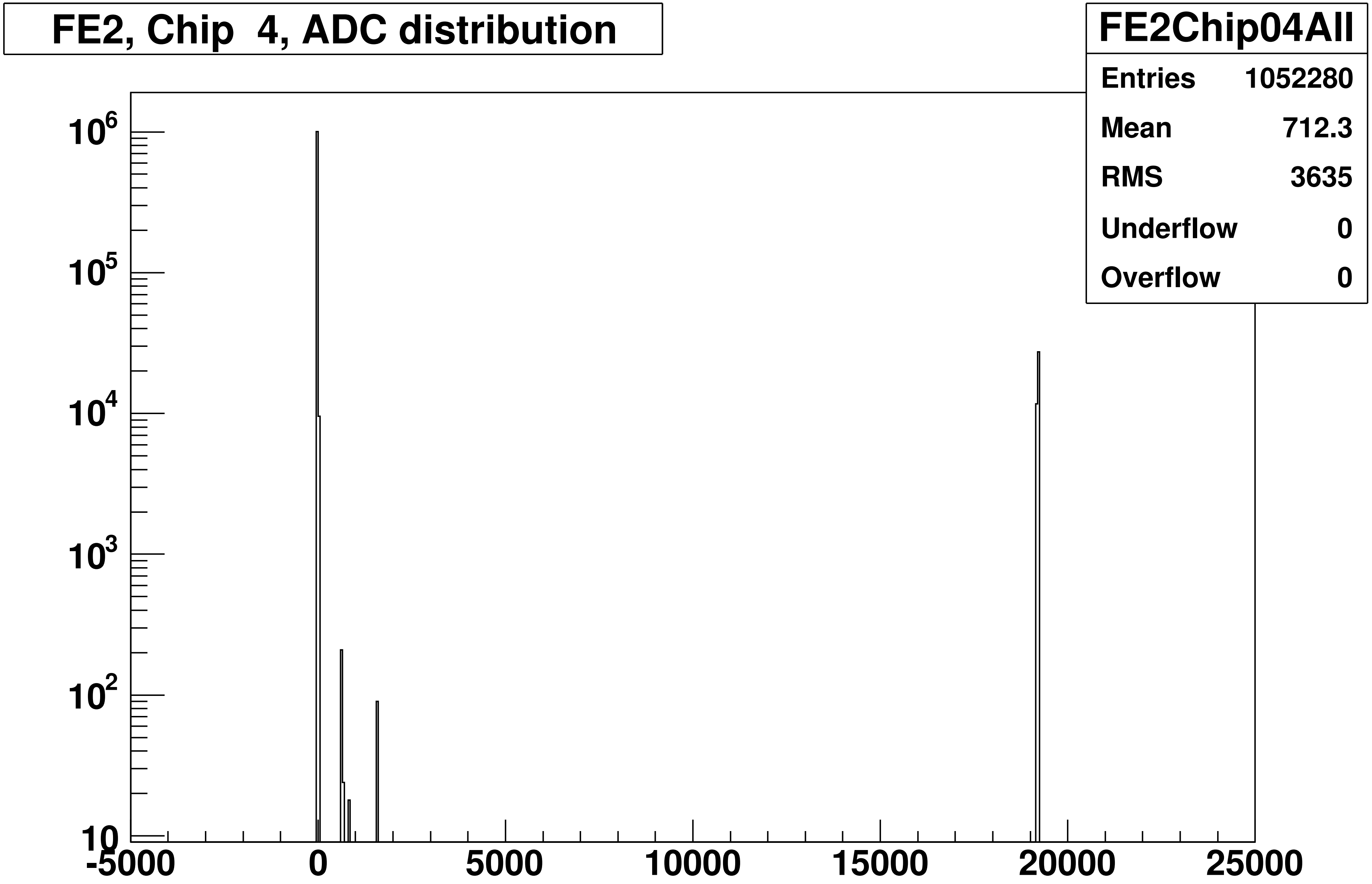

FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 1052280
Mean 712.3
RMS 3635
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
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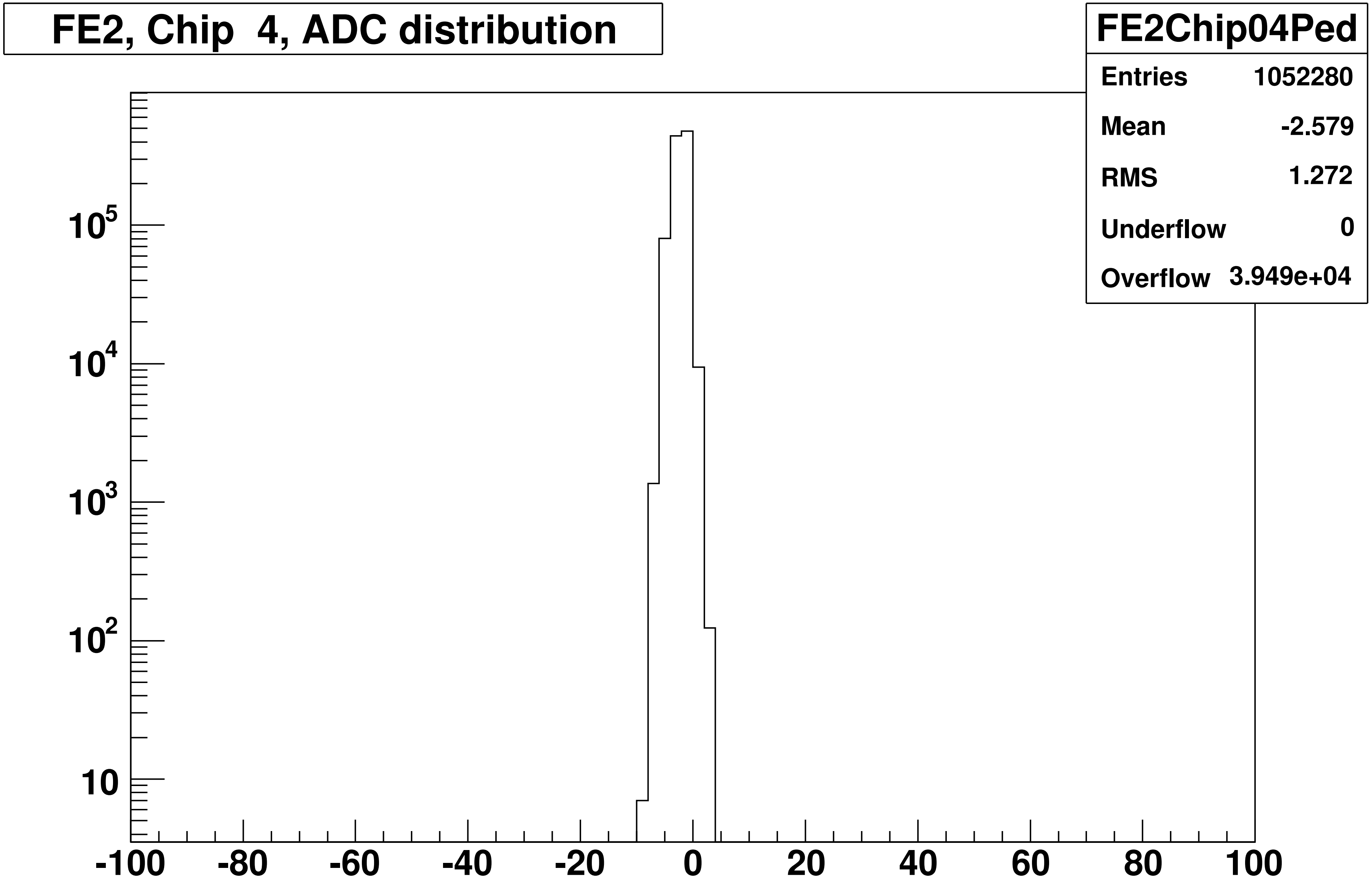
FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 1052280
Mean -2.579
RMS 1.272
Underflow 0
Overflow 3.949e+04
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10^4
10^3
10^2
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-100
-80
-60
-40
-20
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60
80
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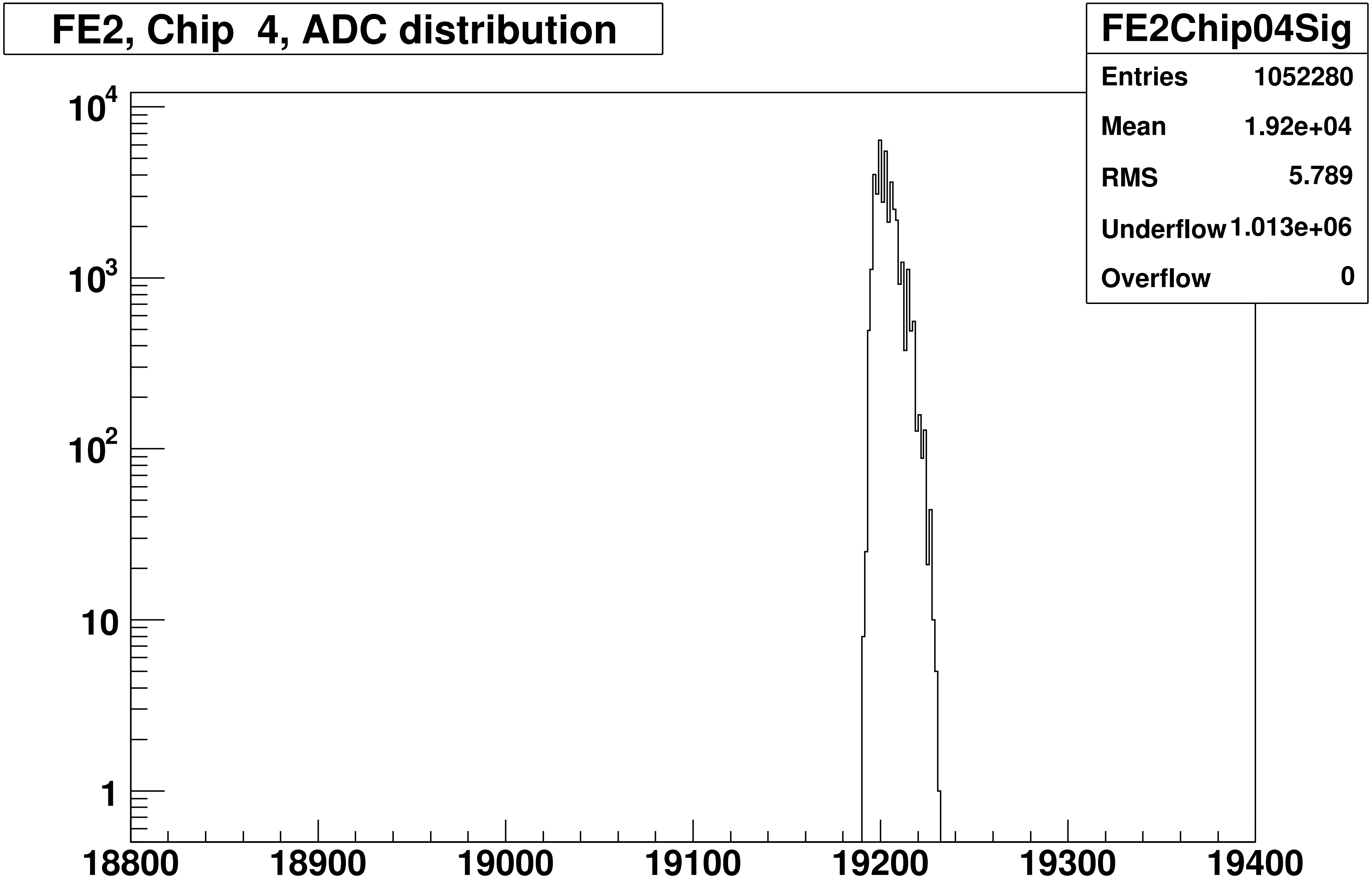
FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 1052280
Mean 1.92e+04
RMS 5.789
Underflow 1.013e+06
Overflow 0
10^4
10^3
10^2
10
1
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18900
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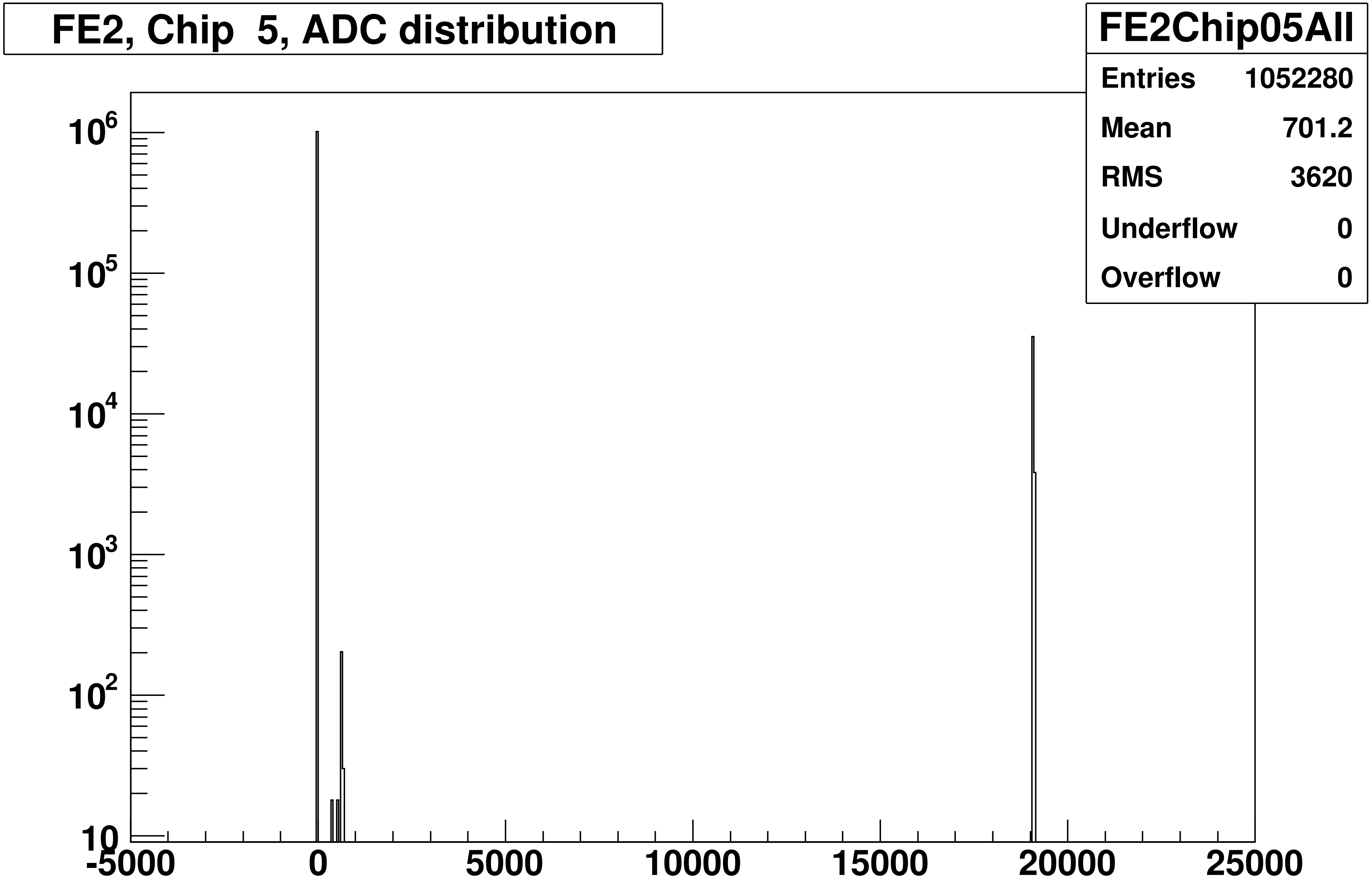

FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 1052280
Mean 701.2
RMS 3620
Underflow 0
Overflow 0
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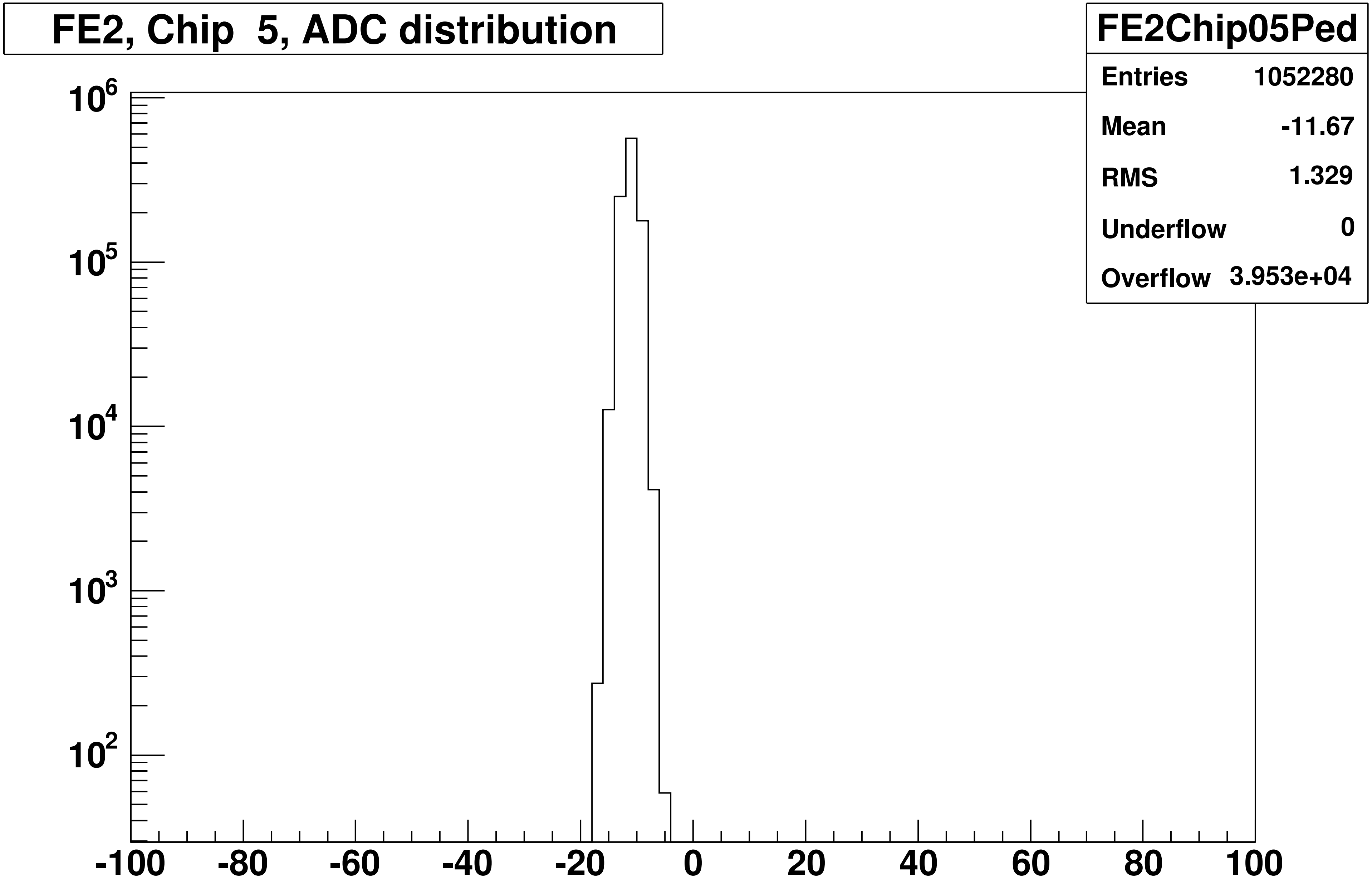
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 1052280
Mean -11.67
RMS 1.329
Underflow 0
Overflow 3.953e+04
10^6
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10^4
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10^2
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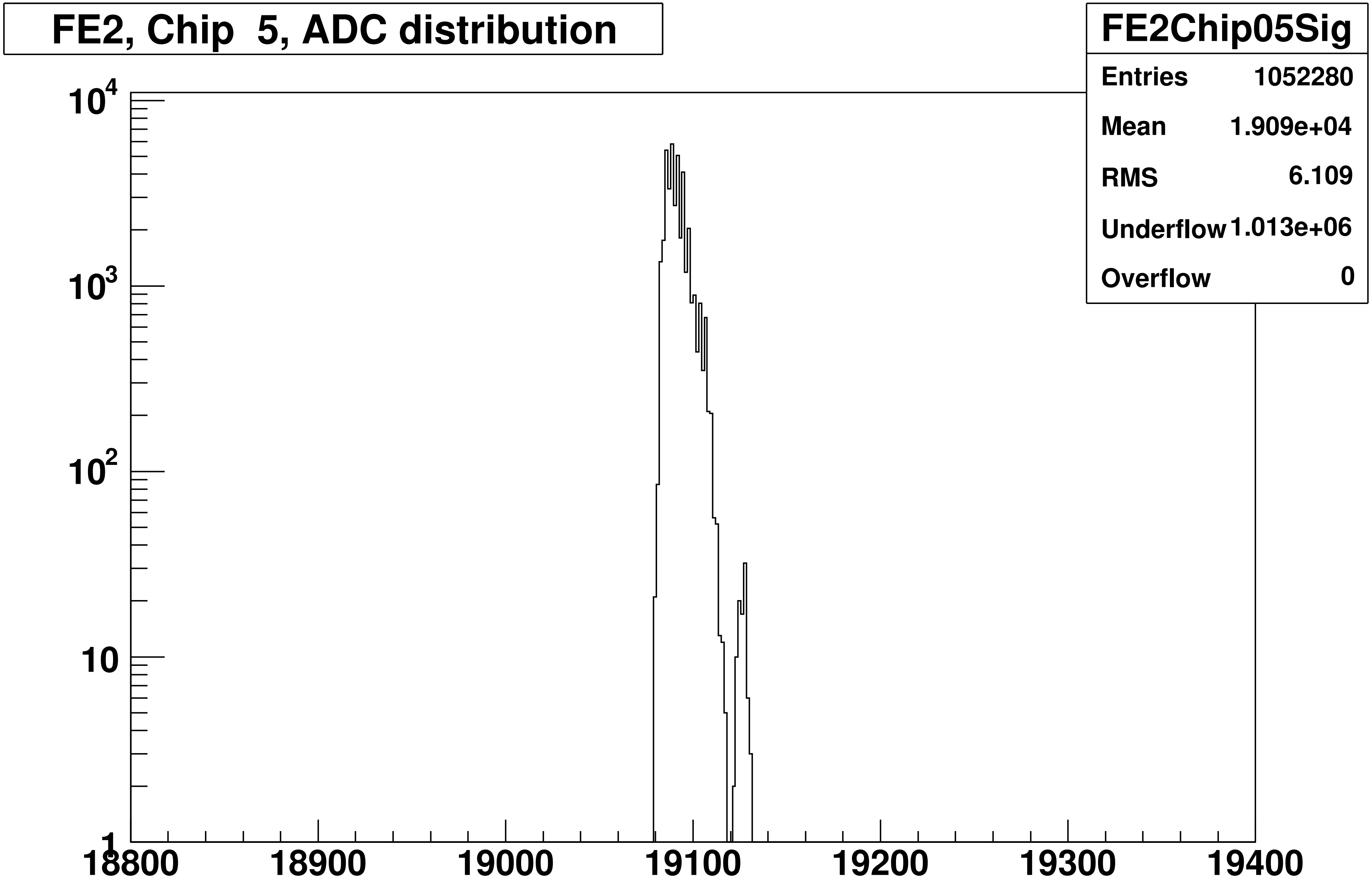
FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 1052280
Mean 1.909e+04
RMS 6.109
Underflow 1.013e+06
Overflow 0
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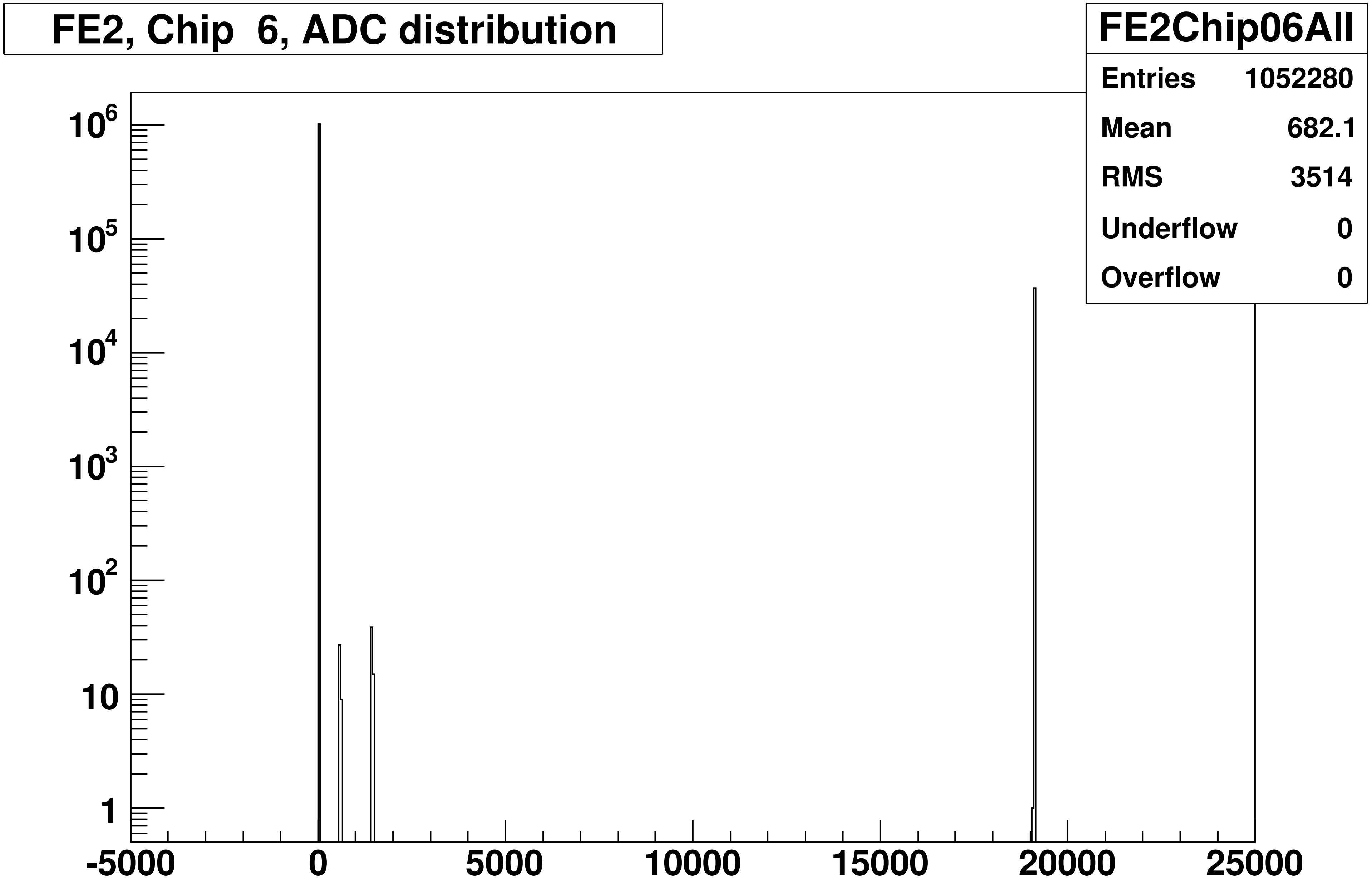
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 1052280
Mean 682.1
RMS 3514
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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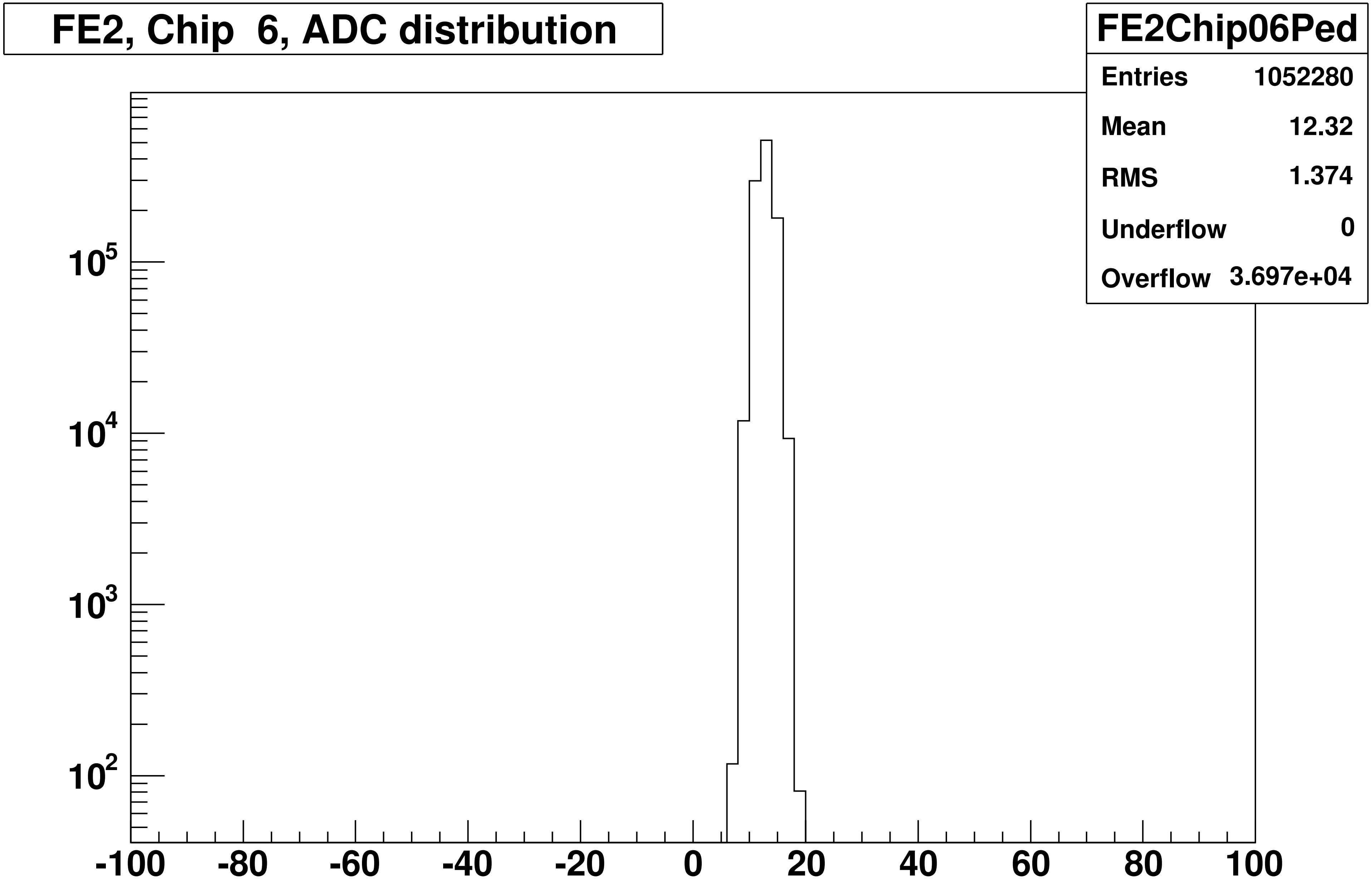
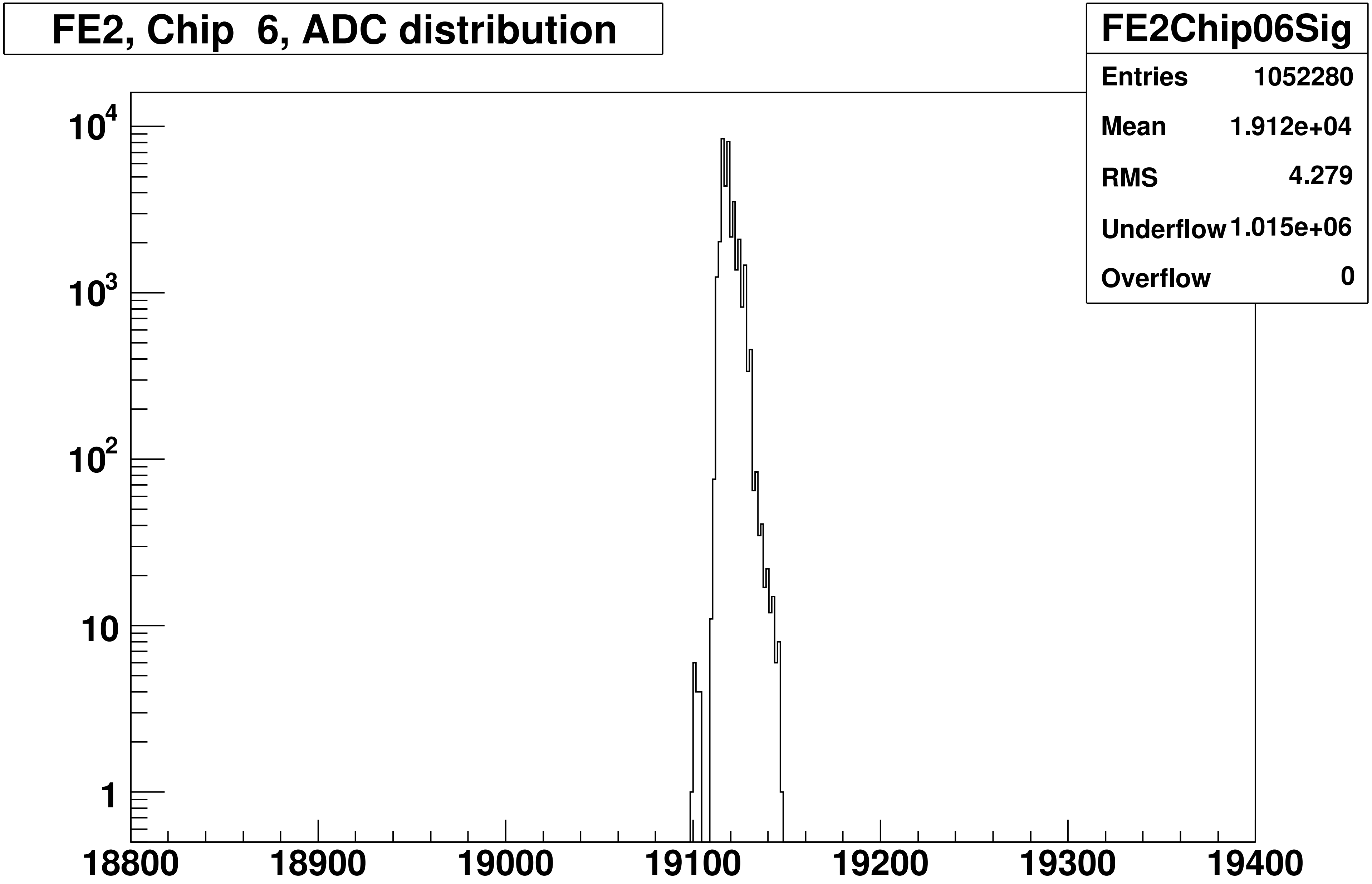
10000
15000
20000
25000



FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 1052280
Mean 12.32
RMS 1.374
Underflow 0
Overflow 3.697e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 1052280
Mean 1.912e+04
RMS 4.279
Underflow 1.015e+06
Overflow 0
10^4
10^3
10^2
10
1
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18900
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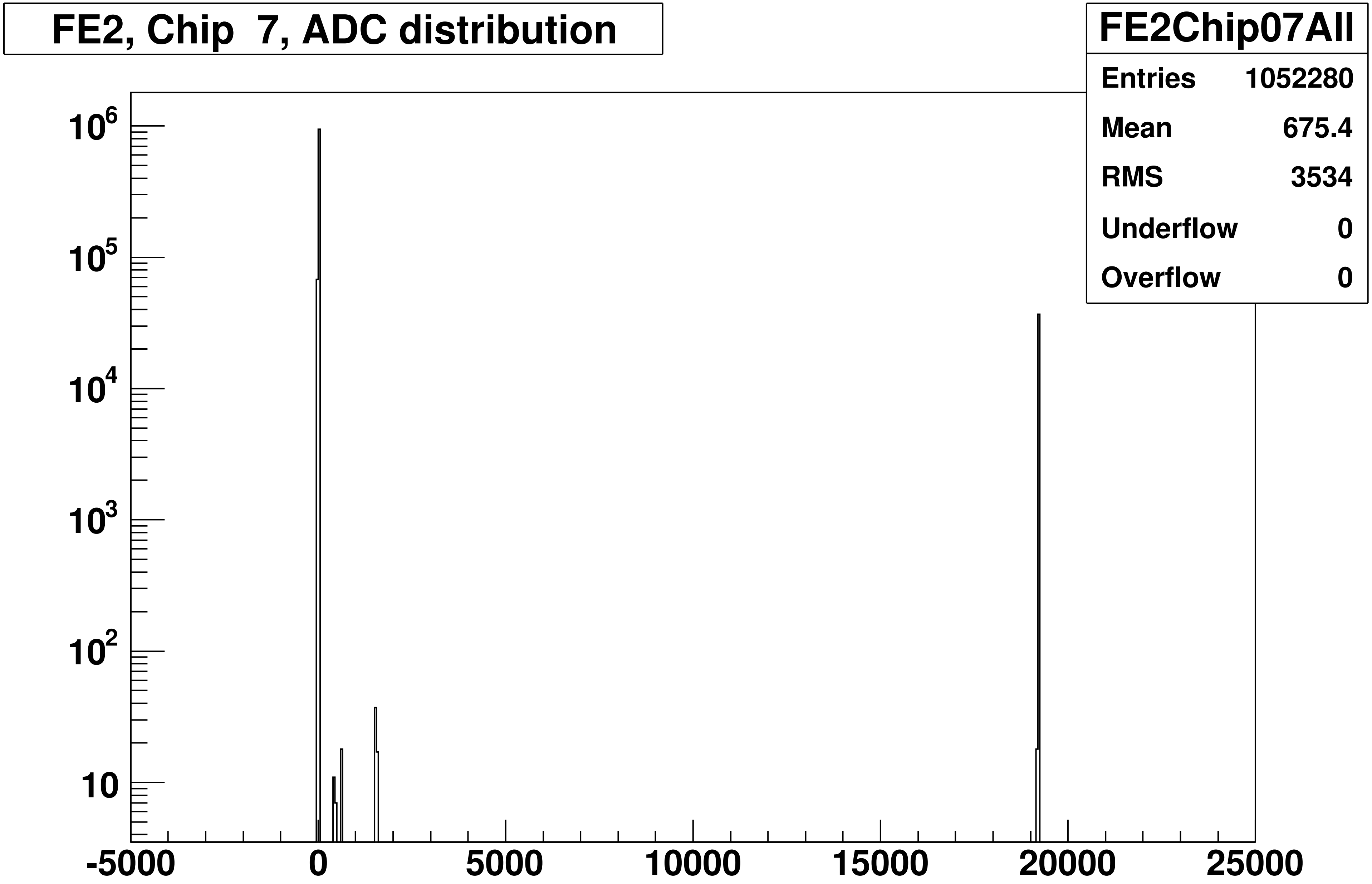
19200
19300
19400


FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 1052280
Mean 675.4
RMS 3534
Underflow 0
Overflow 0
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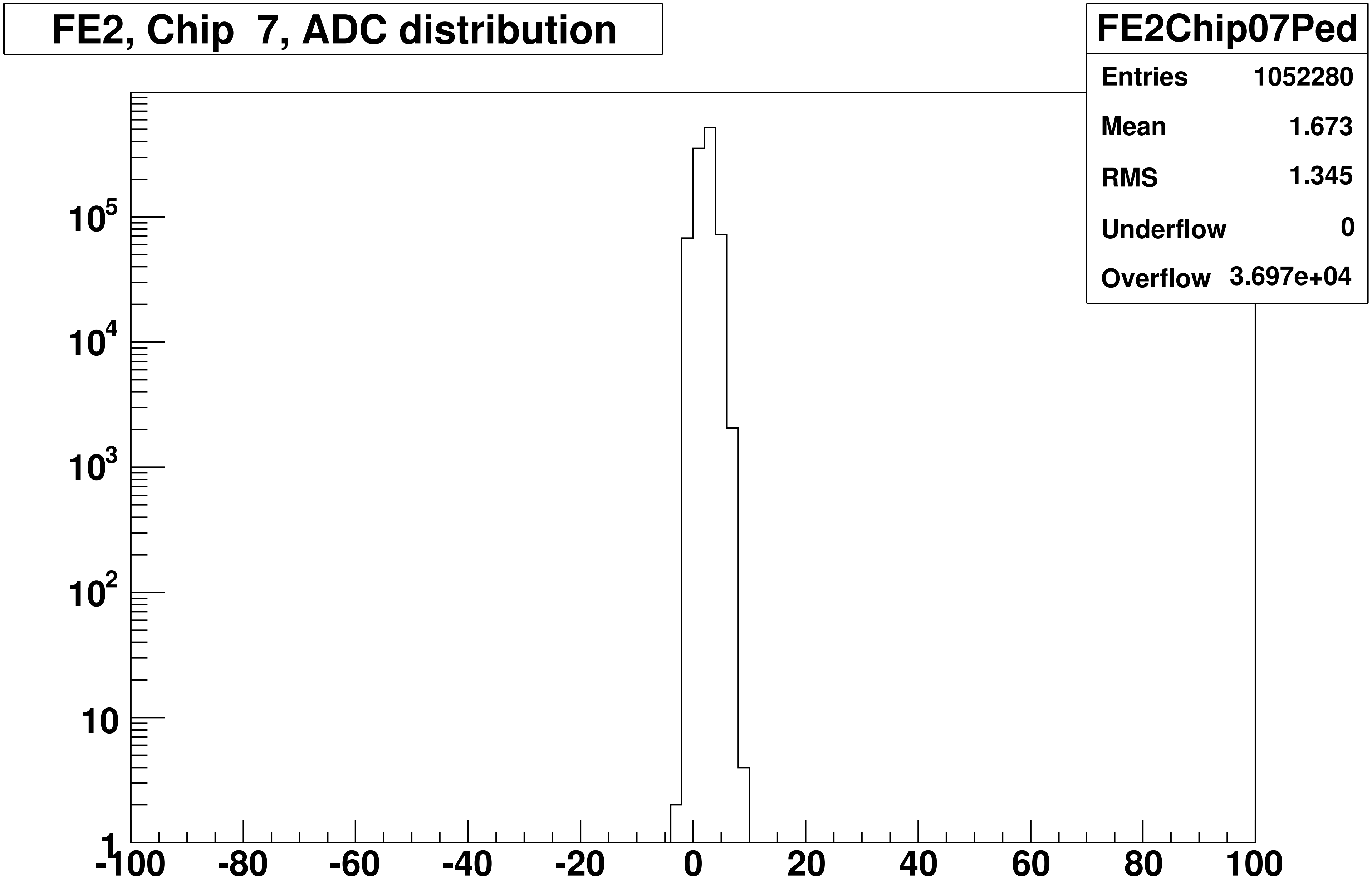
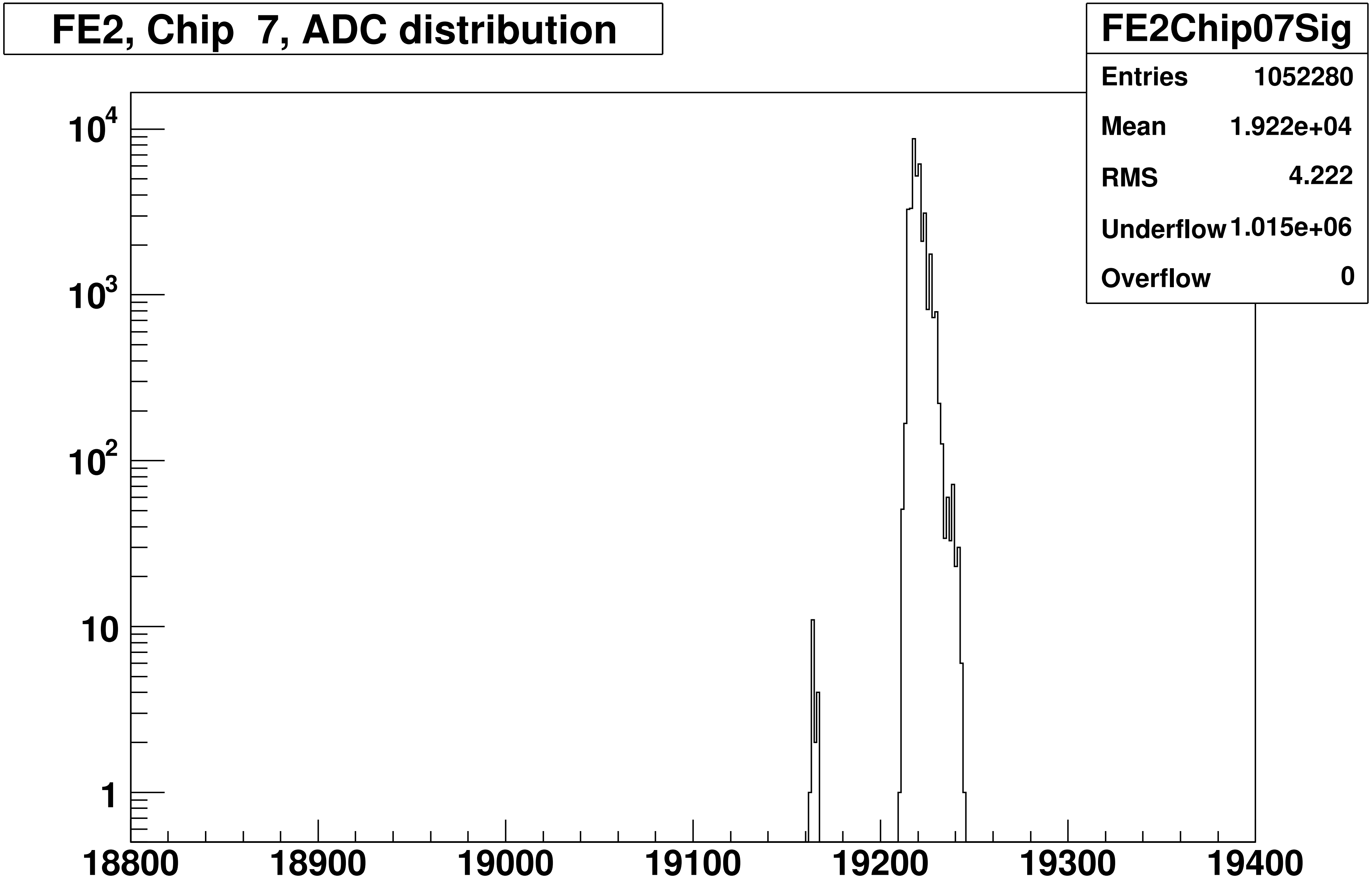
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 1052280
Mean 1.673
RMS 1.345
Underflow 0
Overflow 3.697e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 1052280
Mean 1.922e+04
RMS 4.222
Underflow 1.015e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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19100
19200
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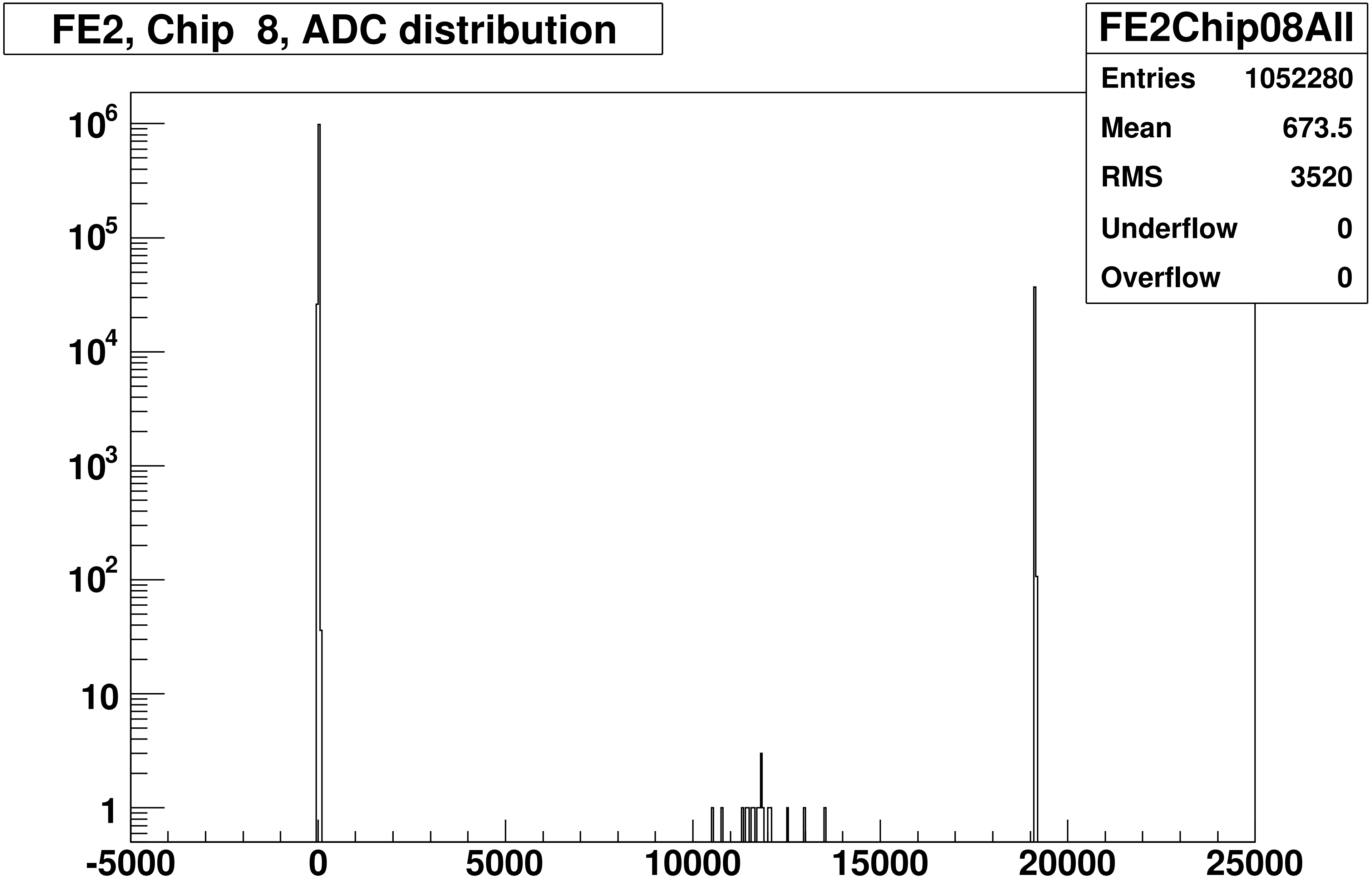
19400



FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 1052280
Mean 673.5
RMS 3520
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
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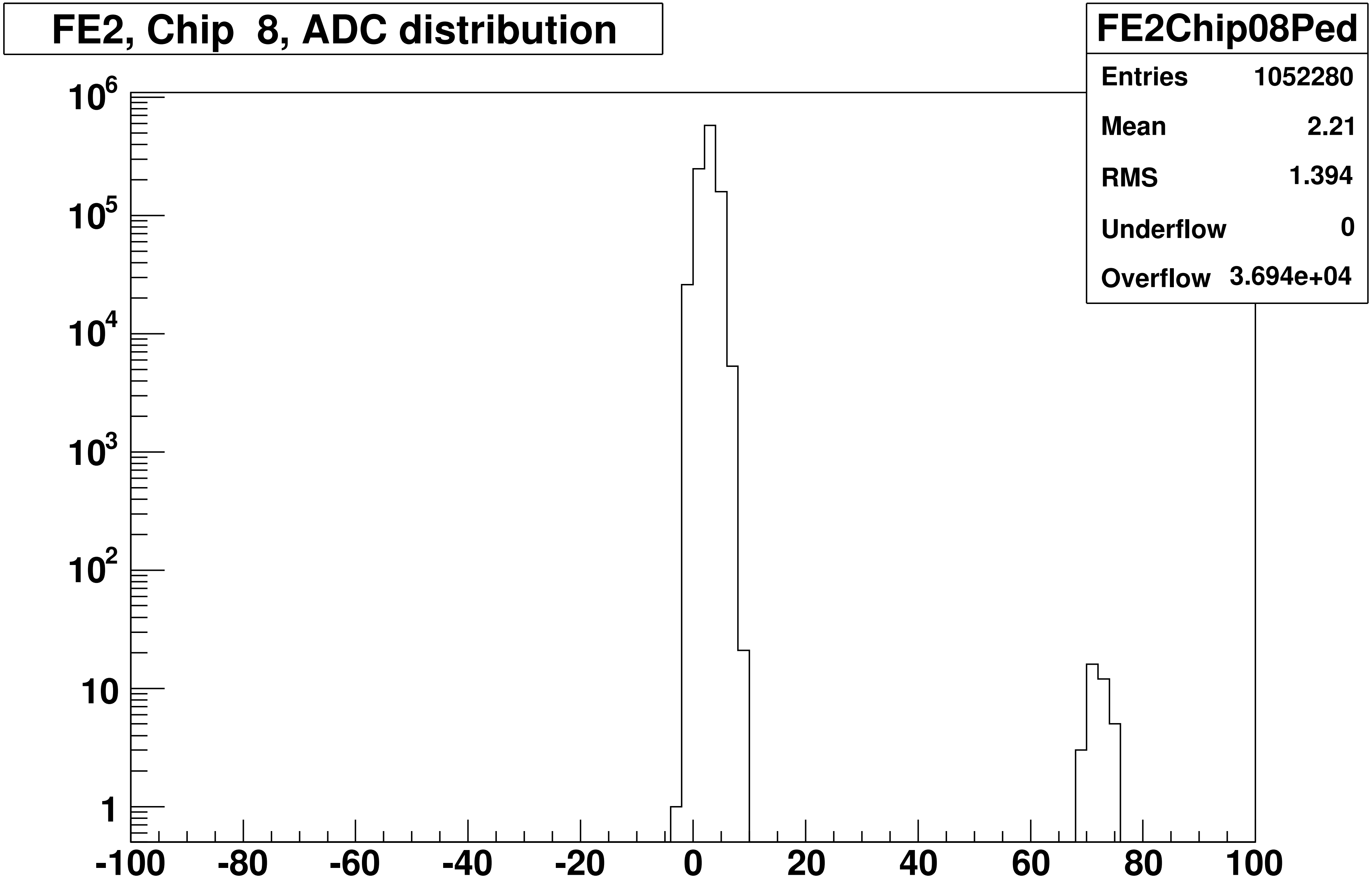
15000
20000
25000


FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 1052280
Mean 2.21
RMS 1.394
Underflow 0
Overflow 3.694e+04
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10^5
10^4
10^3
10^2
10
1
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-40
-20
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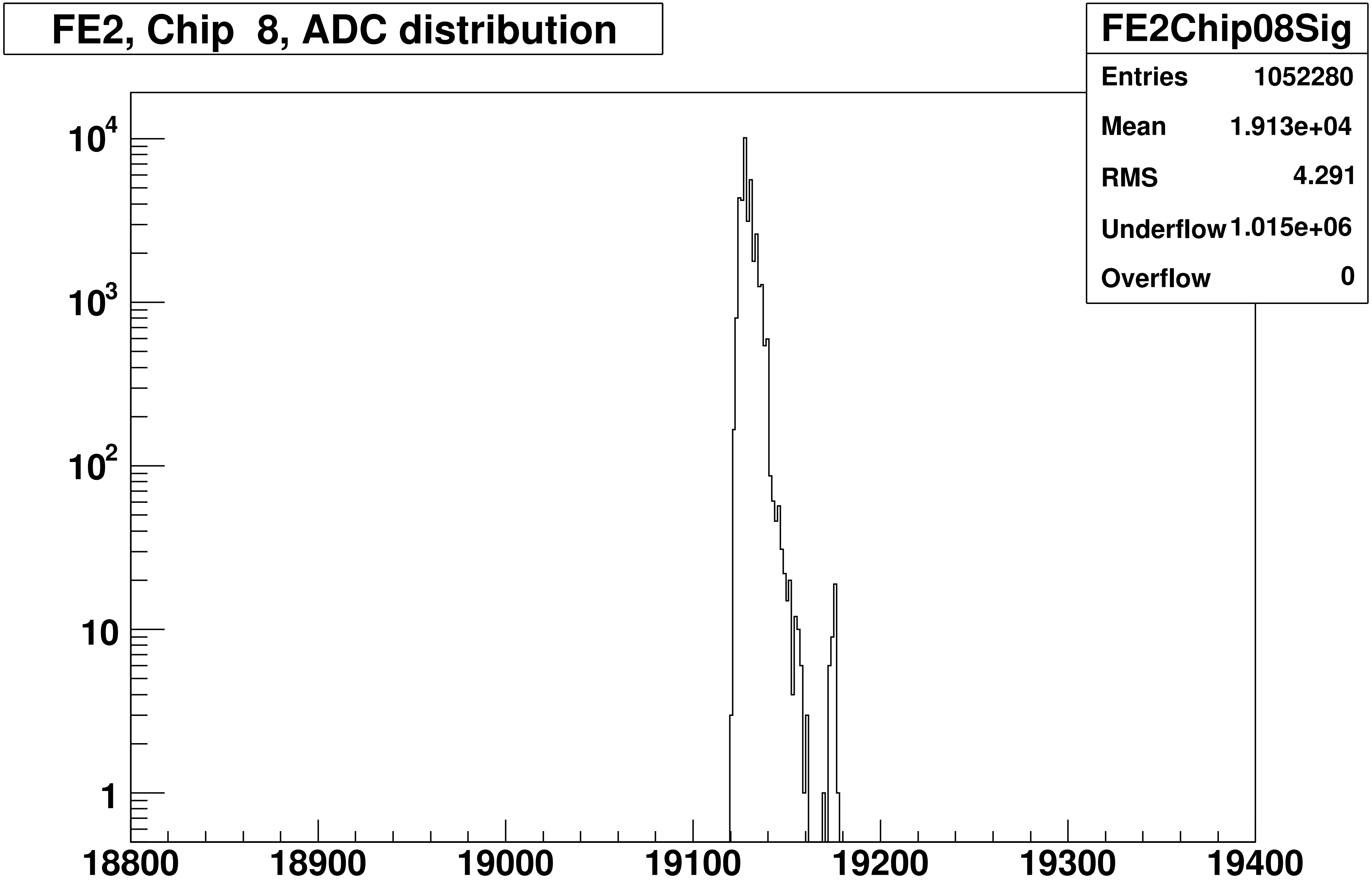
60
80
100


FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 1052280
Mean 1.913e+04
RMS 4.291
Underflow 1.015e+06
Overflow 0
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10^3
10^2
10
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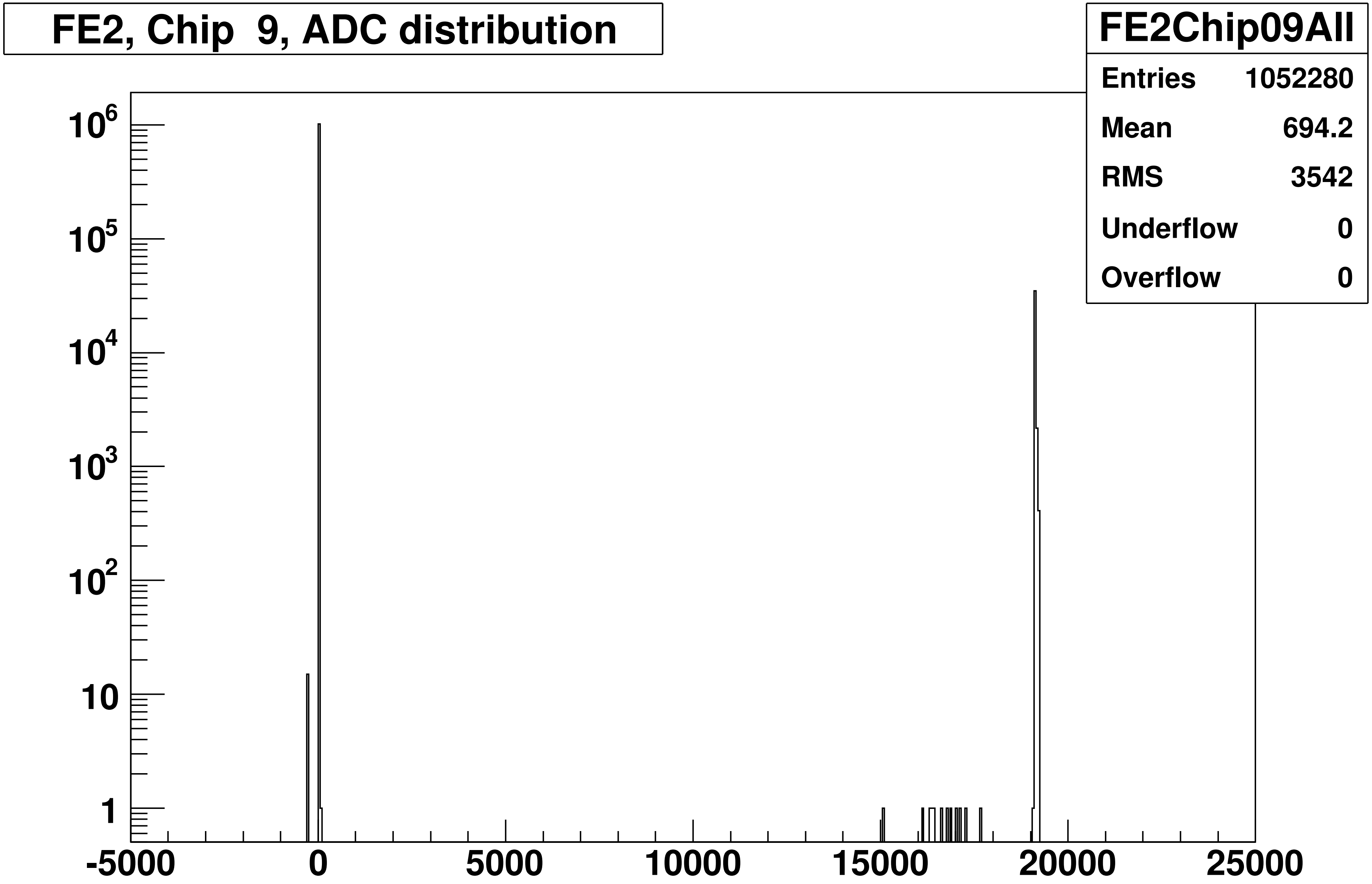
FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 1052280
Mean 694.2
RMS 3542
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
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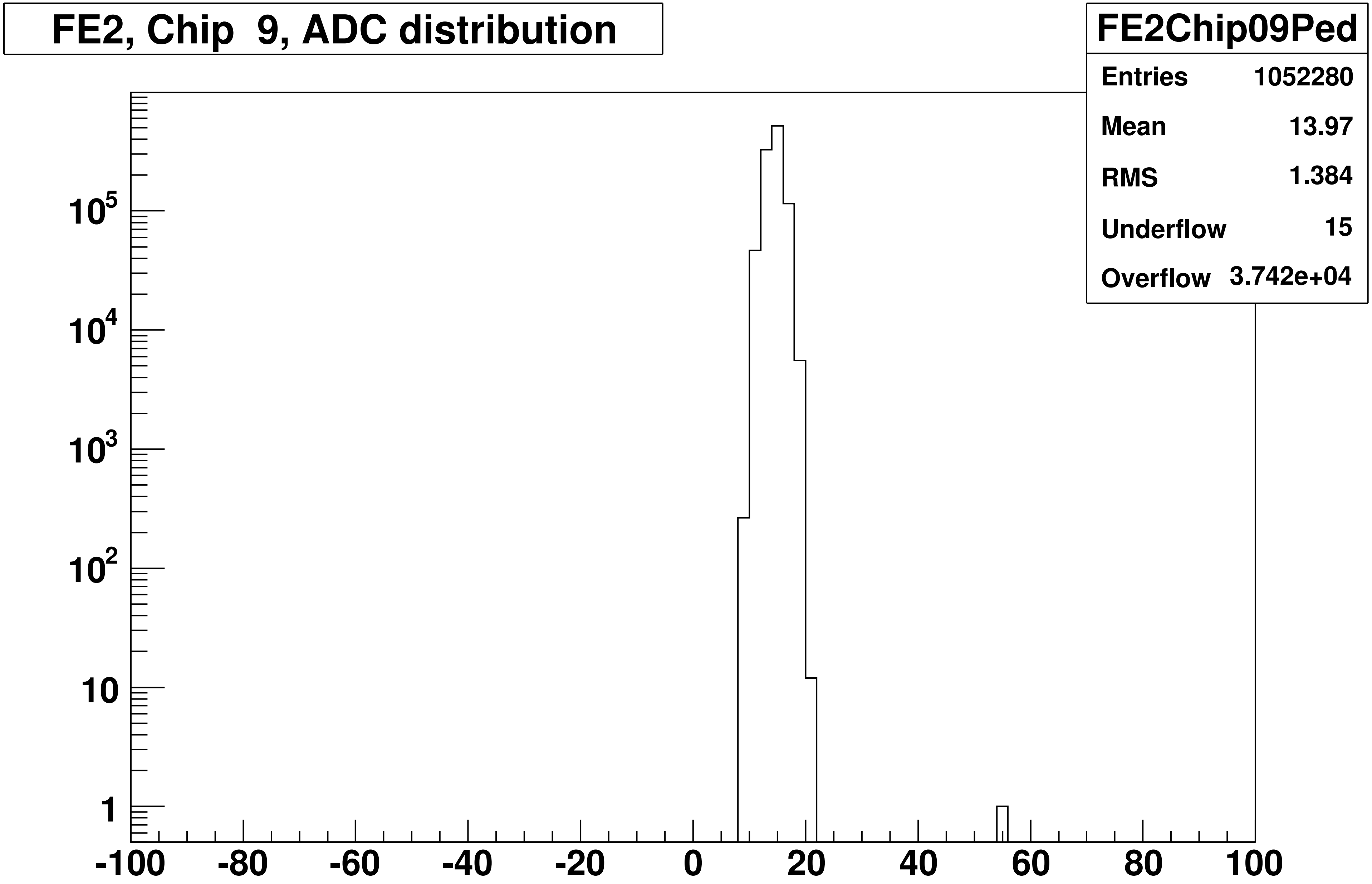
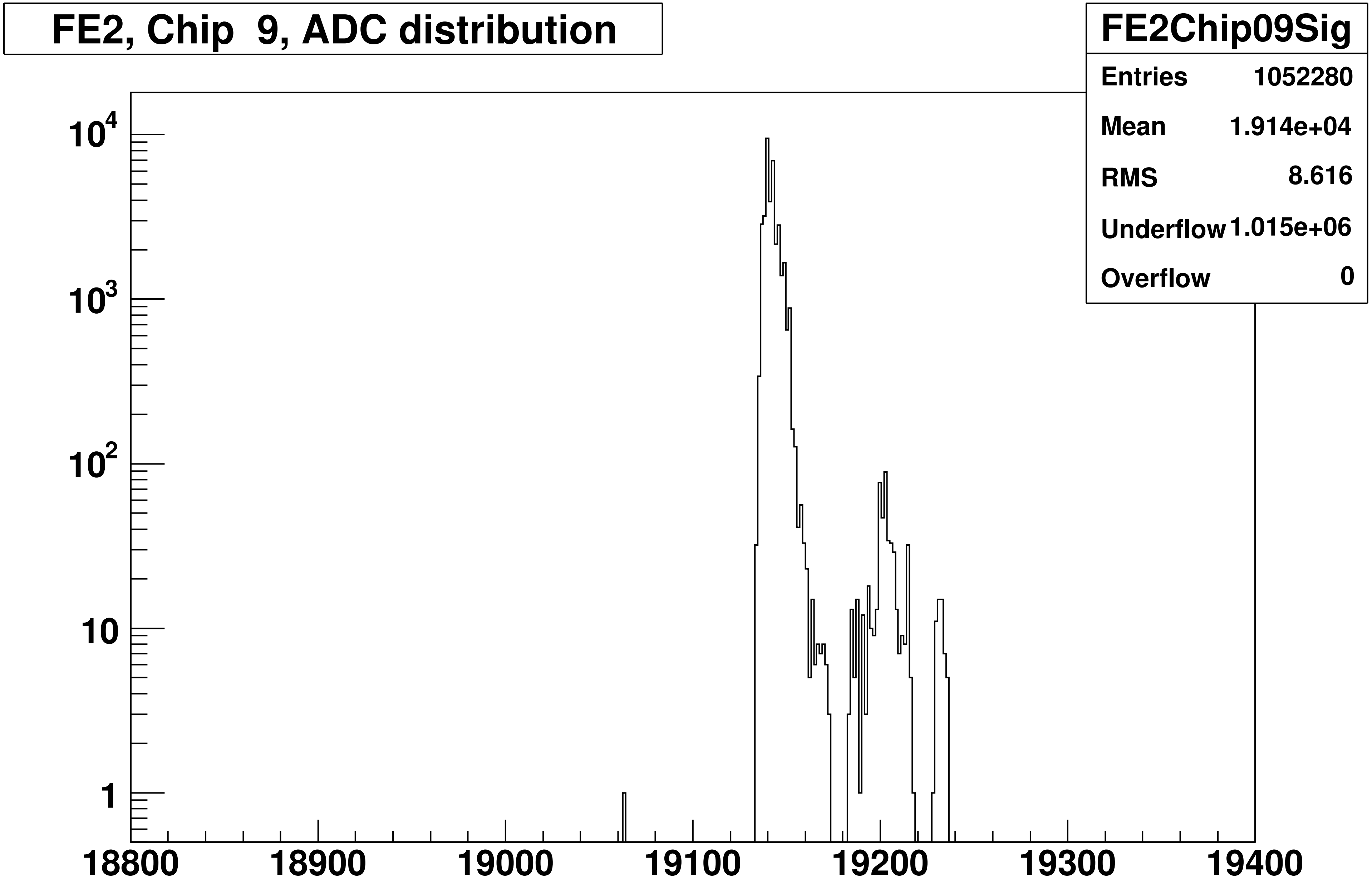
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 1052280
Mean 13.97
RMS 1.384
Underflow 15
Overflow 3.742e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 1052280
Mean 1.914e+04
RMS 8.616
Underflow 1.015e+06
Overflow 0
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10^3
10^2
10
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18900
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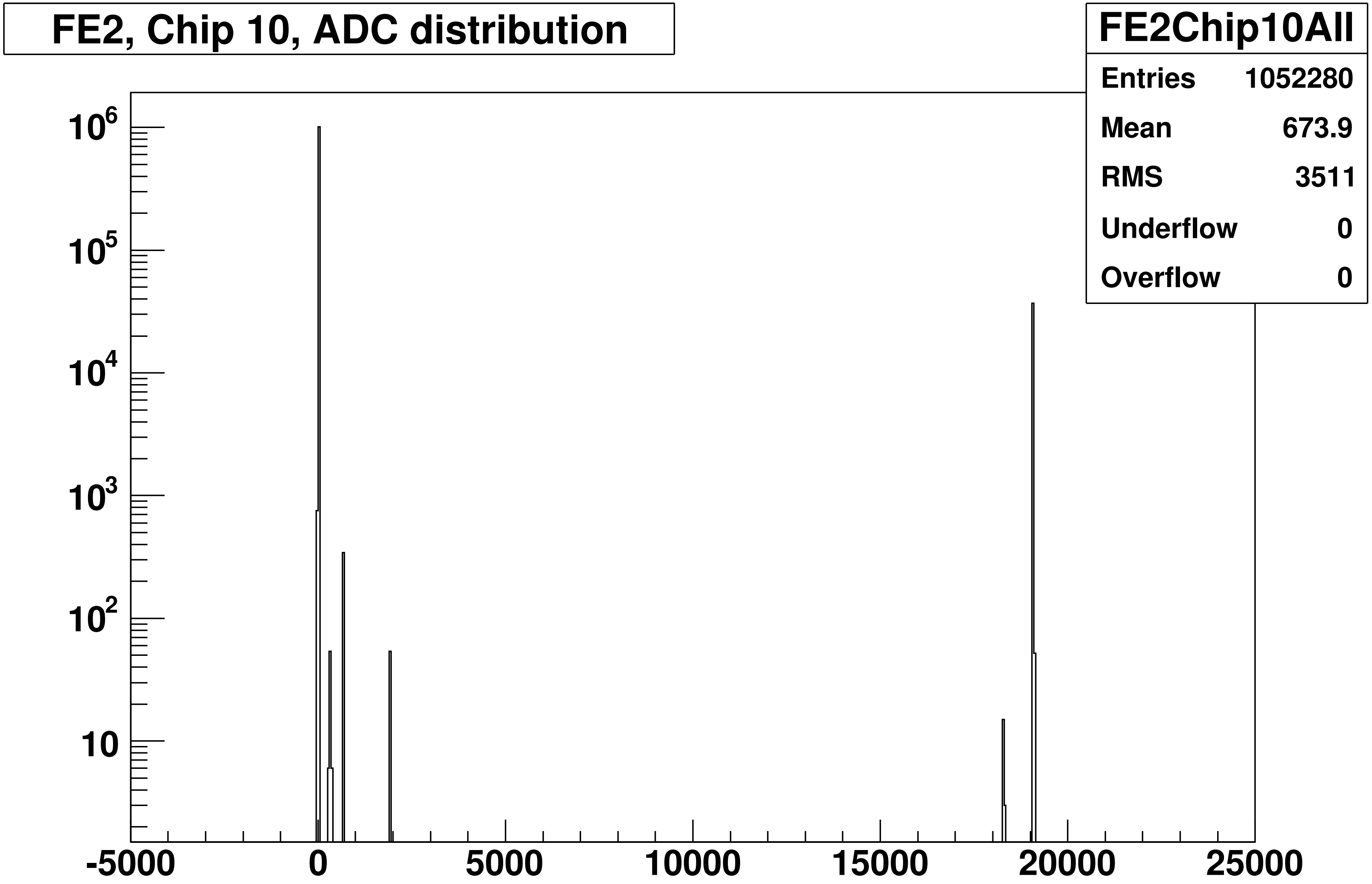

FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 1052280
Mean 673.9
RMS 3511
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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0
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10000
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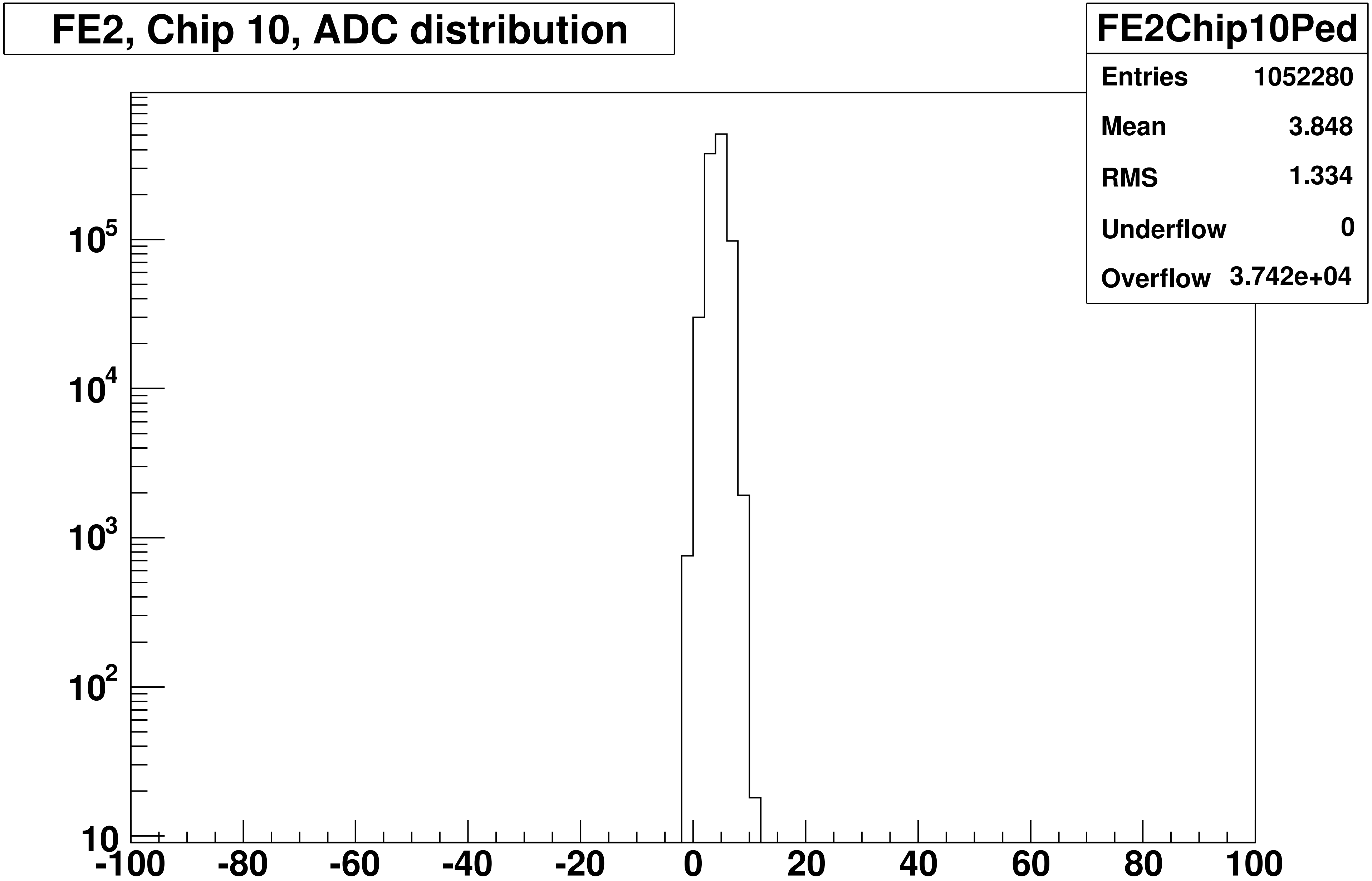
20000
25000



FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 1052280
Mean 3.848
RMS 1.334
Underflow 0
Overflow 3.742e+04
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10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
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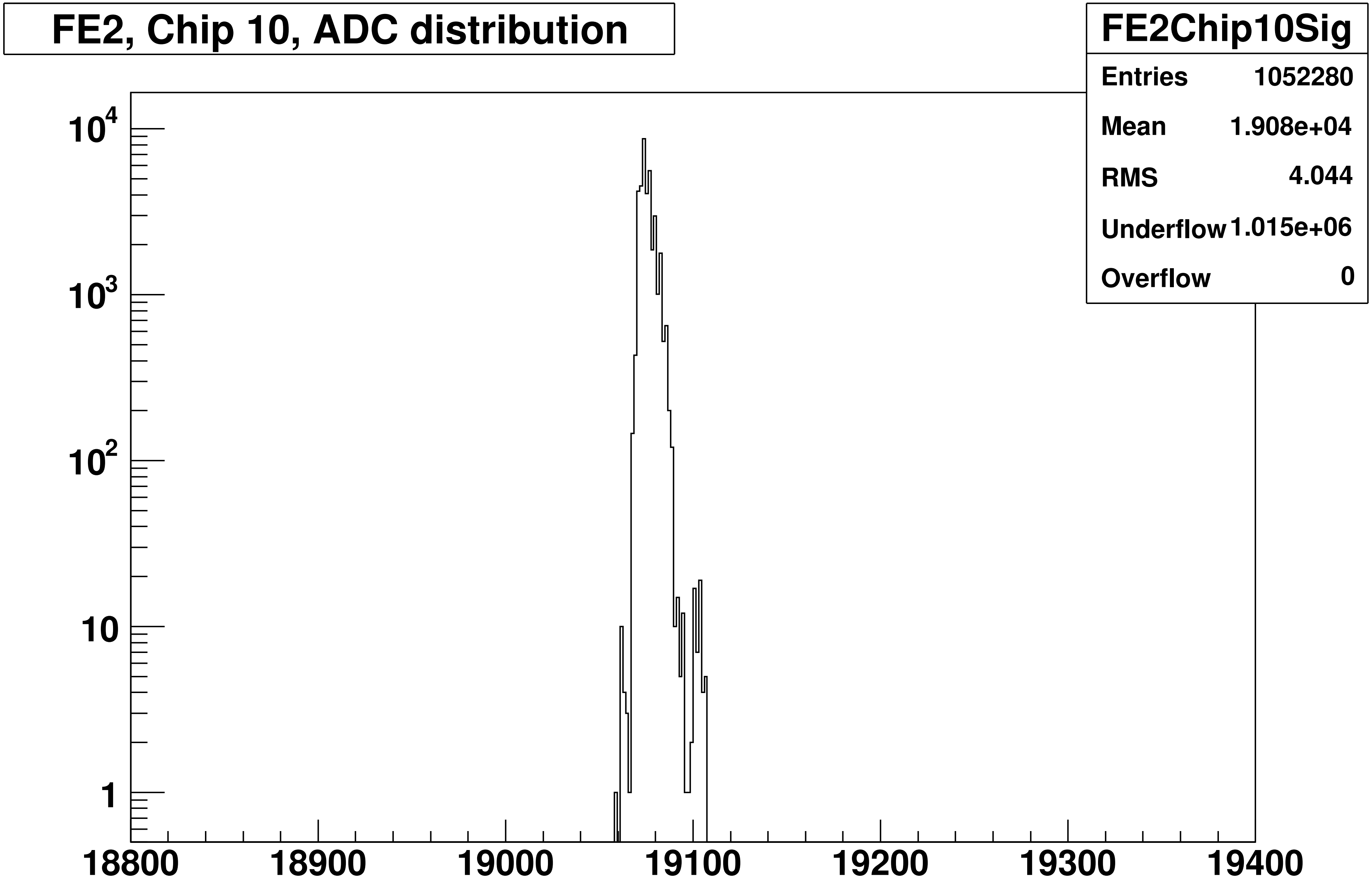
80
100


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 1052280
Mean 1.908e+04
RMS 4.044
Underflow 1.015e+06
Overflow 0
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10^3
10^2
10
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18900
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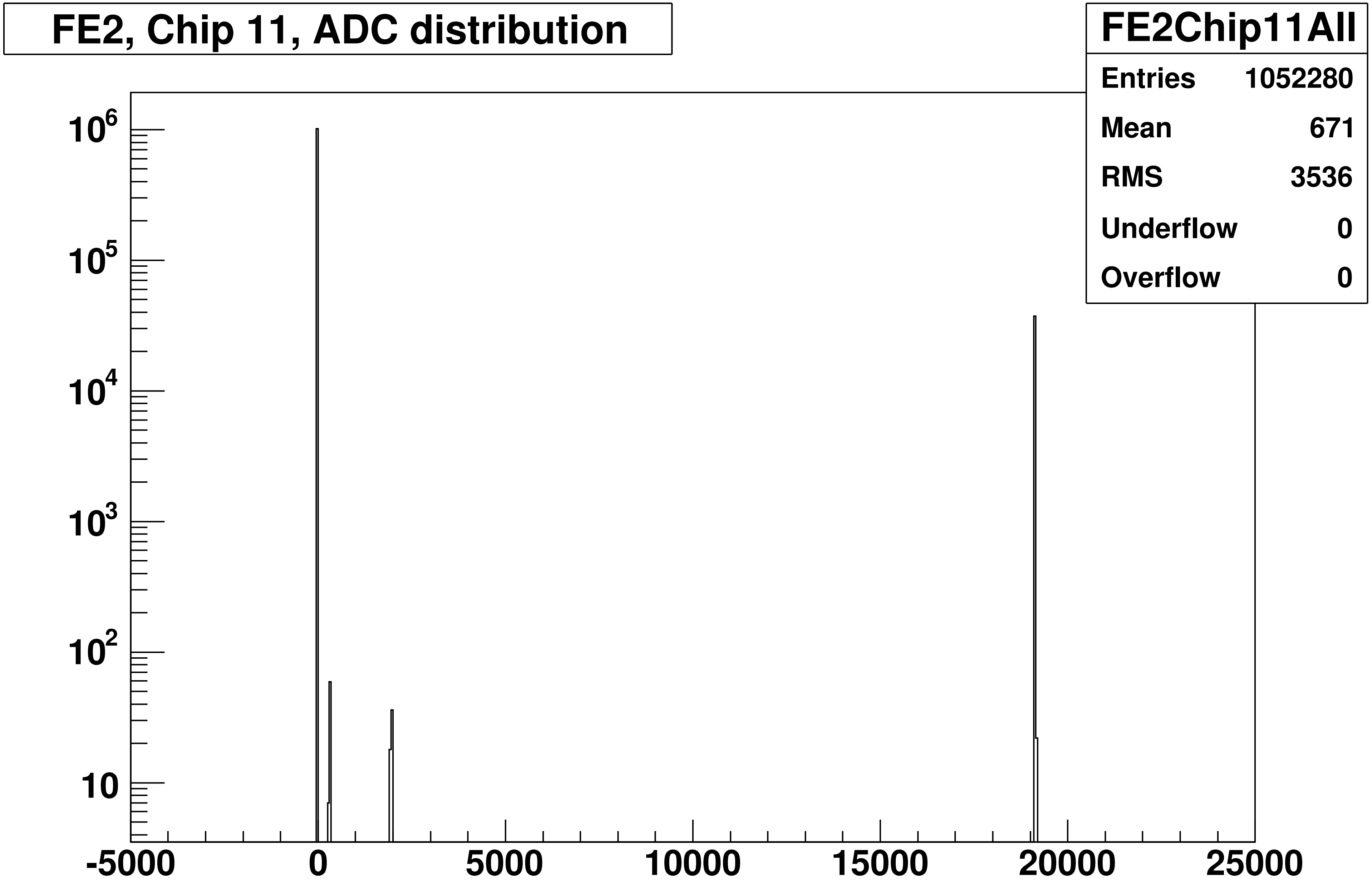

FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 1052280
Mean 671
RMS 3536
Underflow 0
Overflow 0
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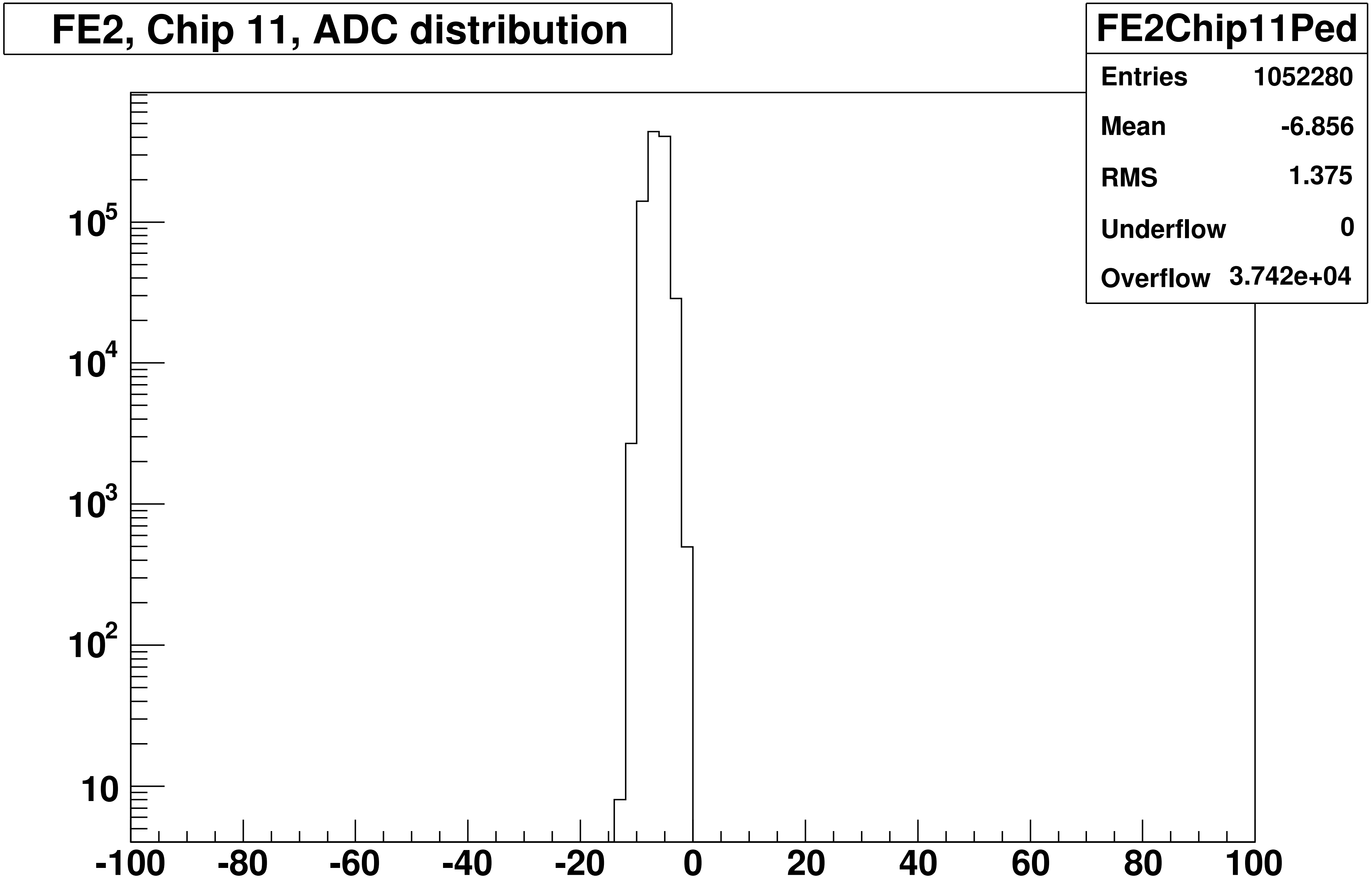
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 1052280
Mean -6.856
RMS 1.375
Underflow 0
Overflow 3.742e+04
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10^4
10^3
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-100
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-20
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80
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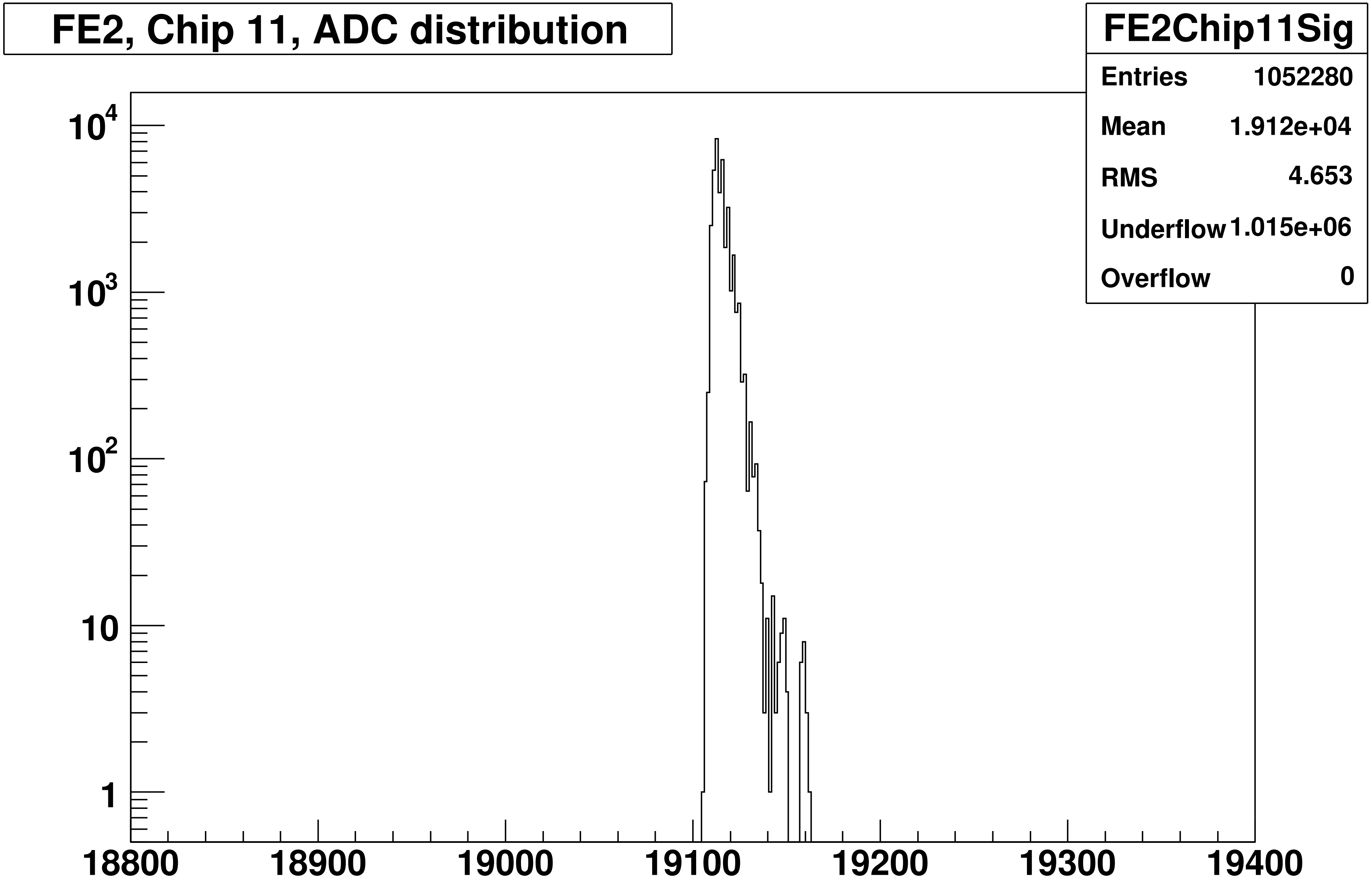
FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 1052280
Mean 1.912e+04
RMS 4.653
Underflow 1.015e+06
Overflow 0
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10^3
10^2
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18900
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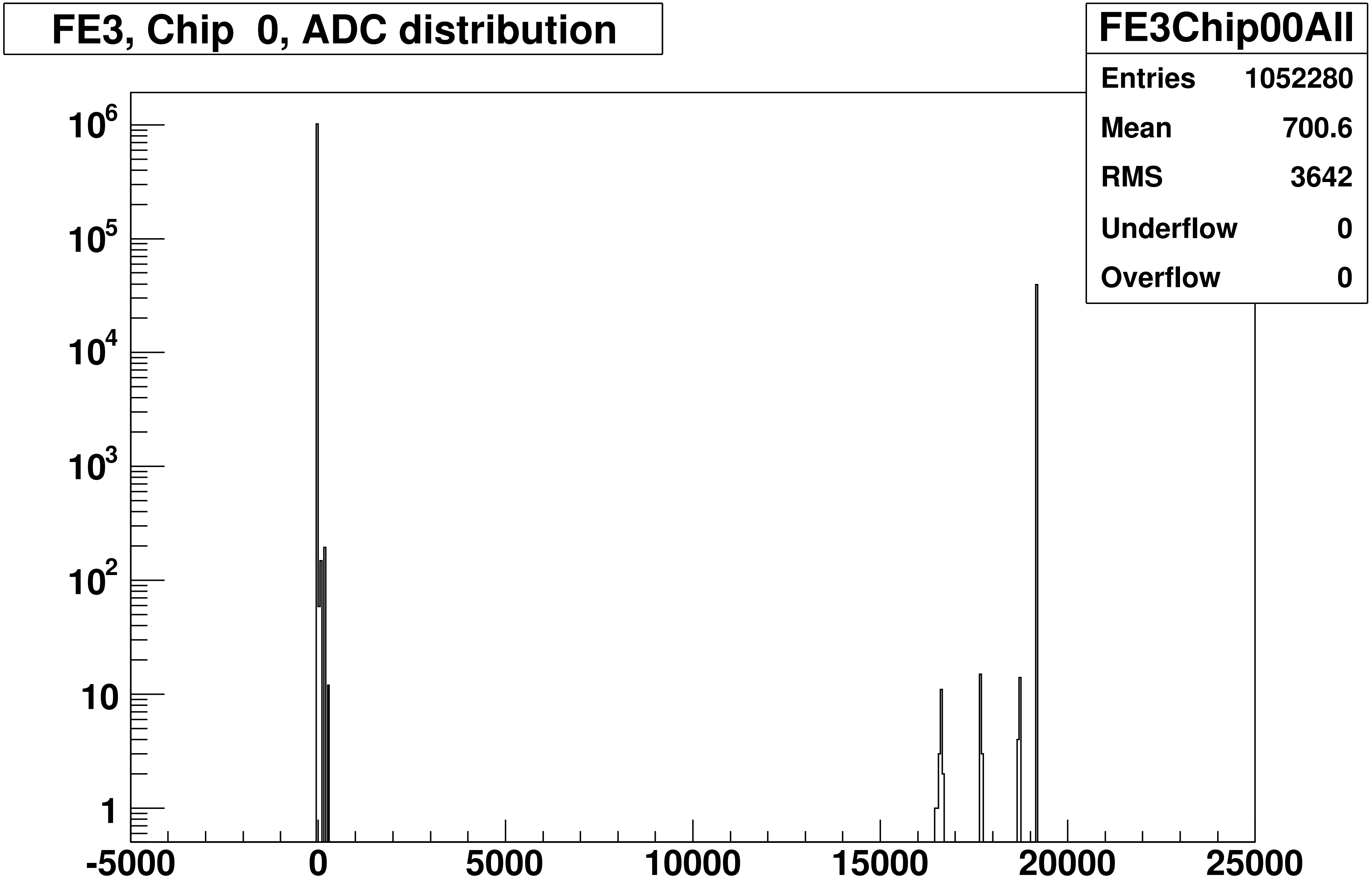

FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 1052280
Mean 700.6
RMS 3642
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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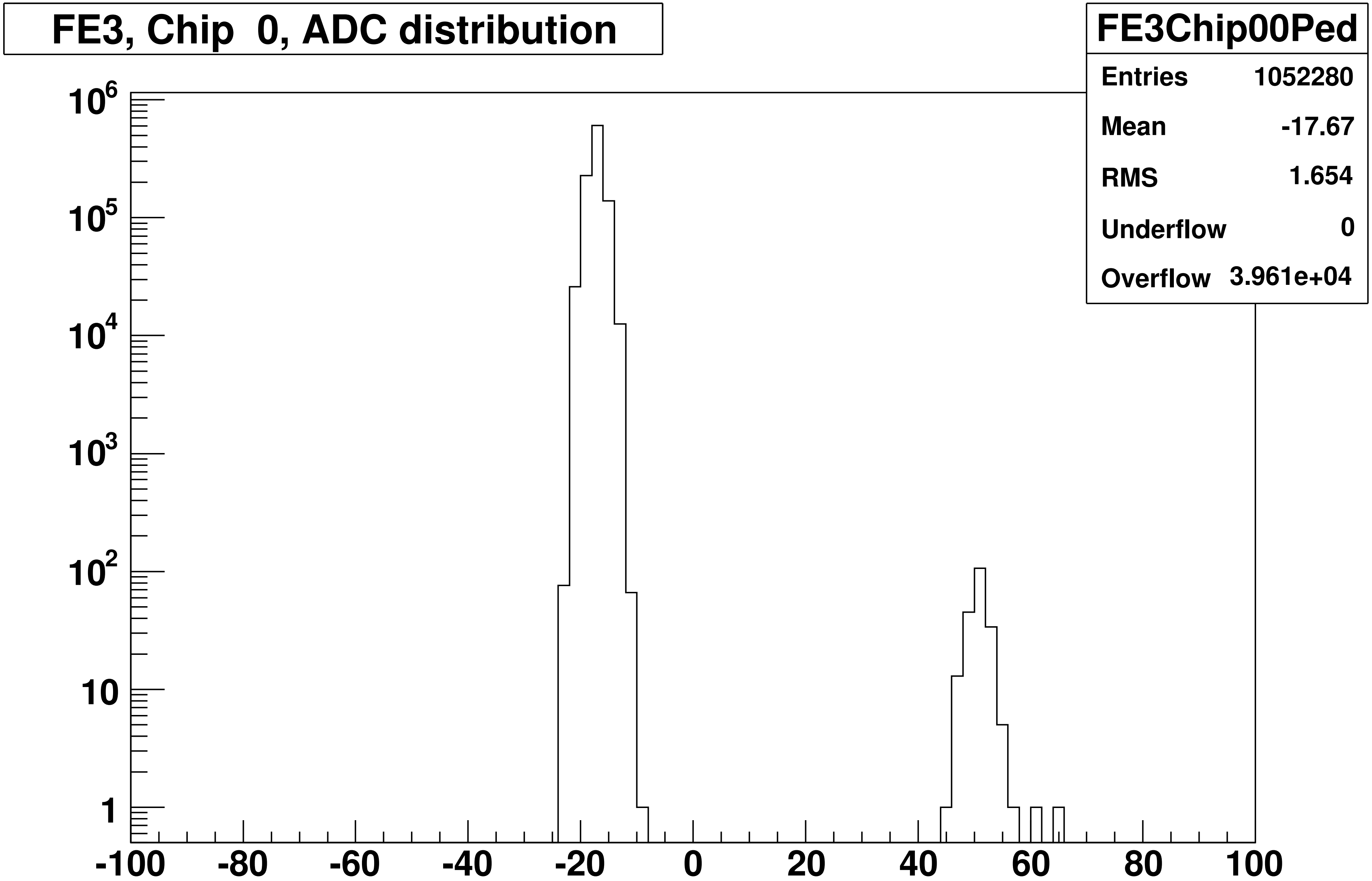
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 1052280
Mean -17.67
RMS 1.654
Underflow 0
Overflow 3.961e+04
10^6
10^5
10^4
10^3
10^2
10
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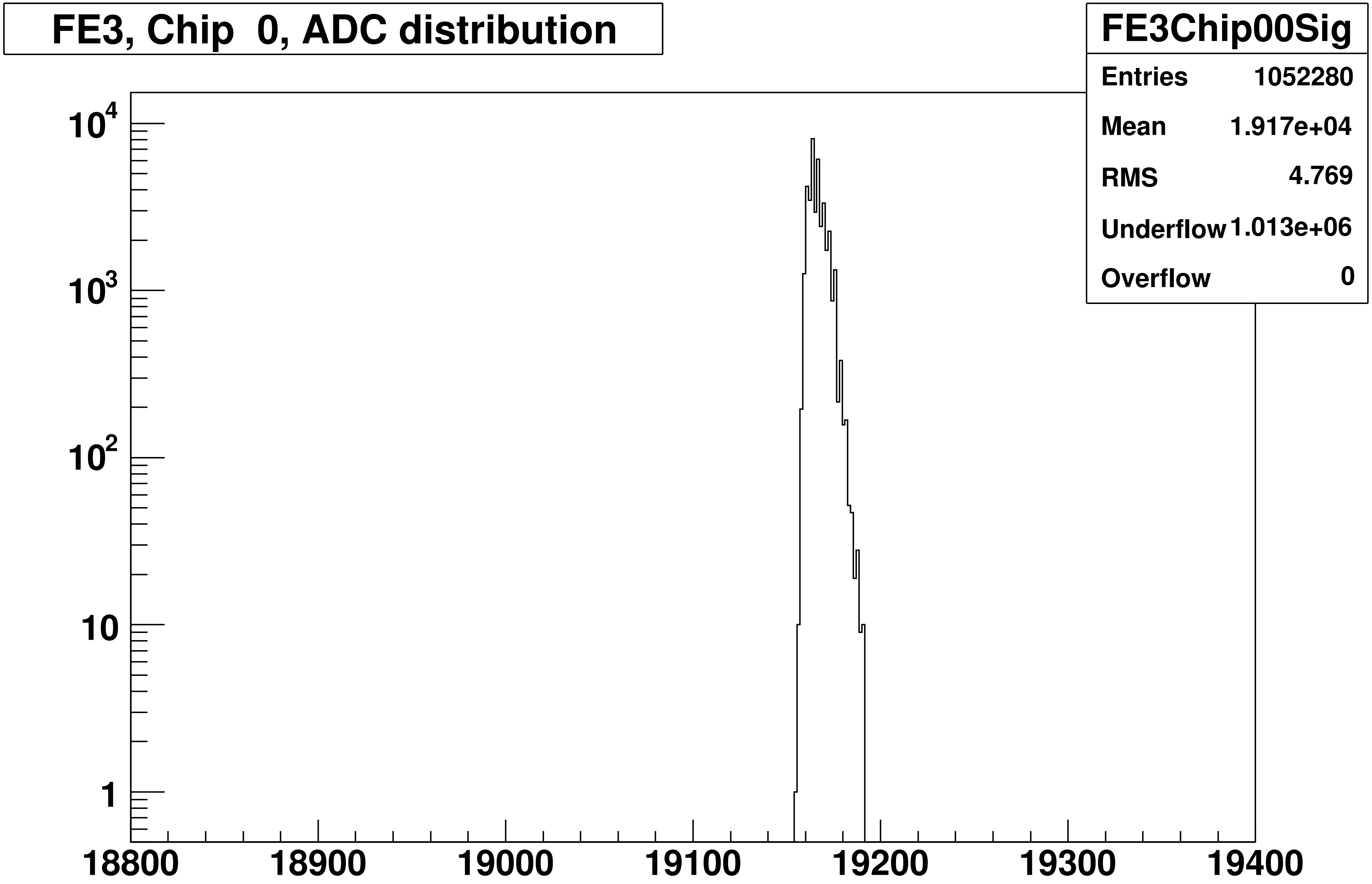
FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 1052280
Mean 1.917e+04
RMS 4.769
Underflow 1.013e+06
Overflow 0
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10^3
10^2
10
1
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18900
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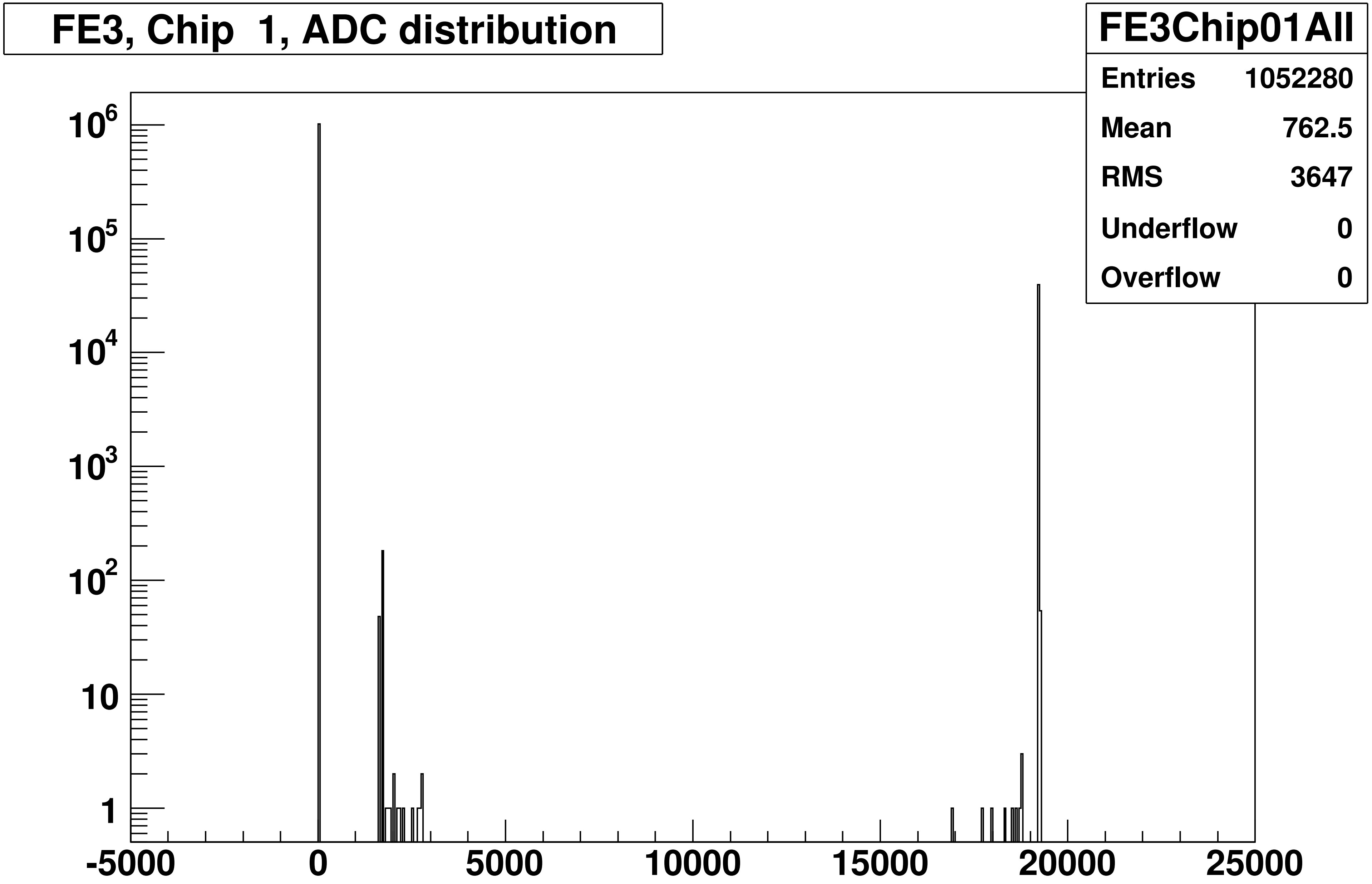
FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 1052280
Mean 762.5
RMS 3647
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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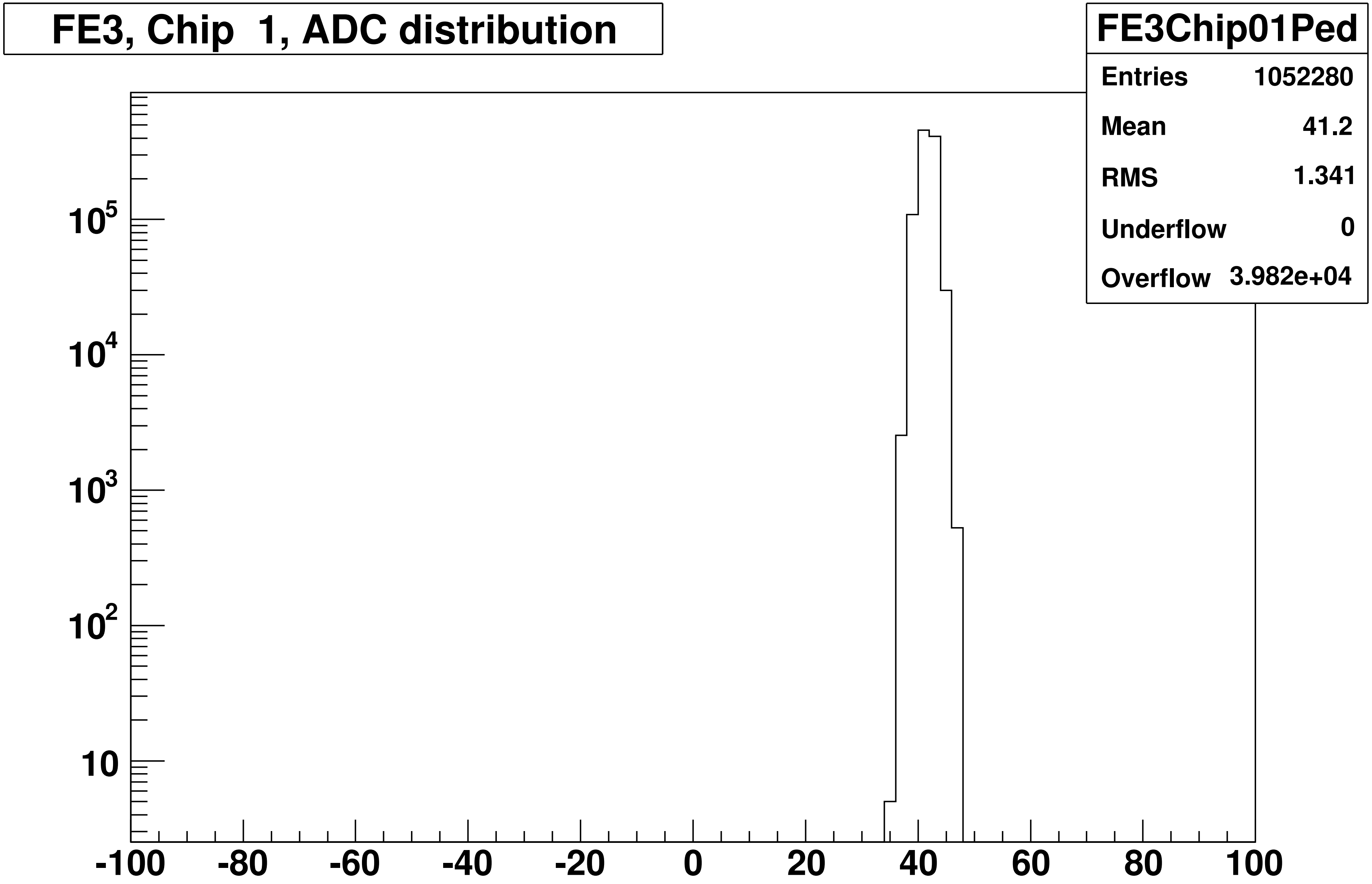
FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 1052280
Mean 41.2
RMS 1.341
Underflow 0
Overflow 3.982e+04
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10^4
10^3
10^2
10
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-60
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-20
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80
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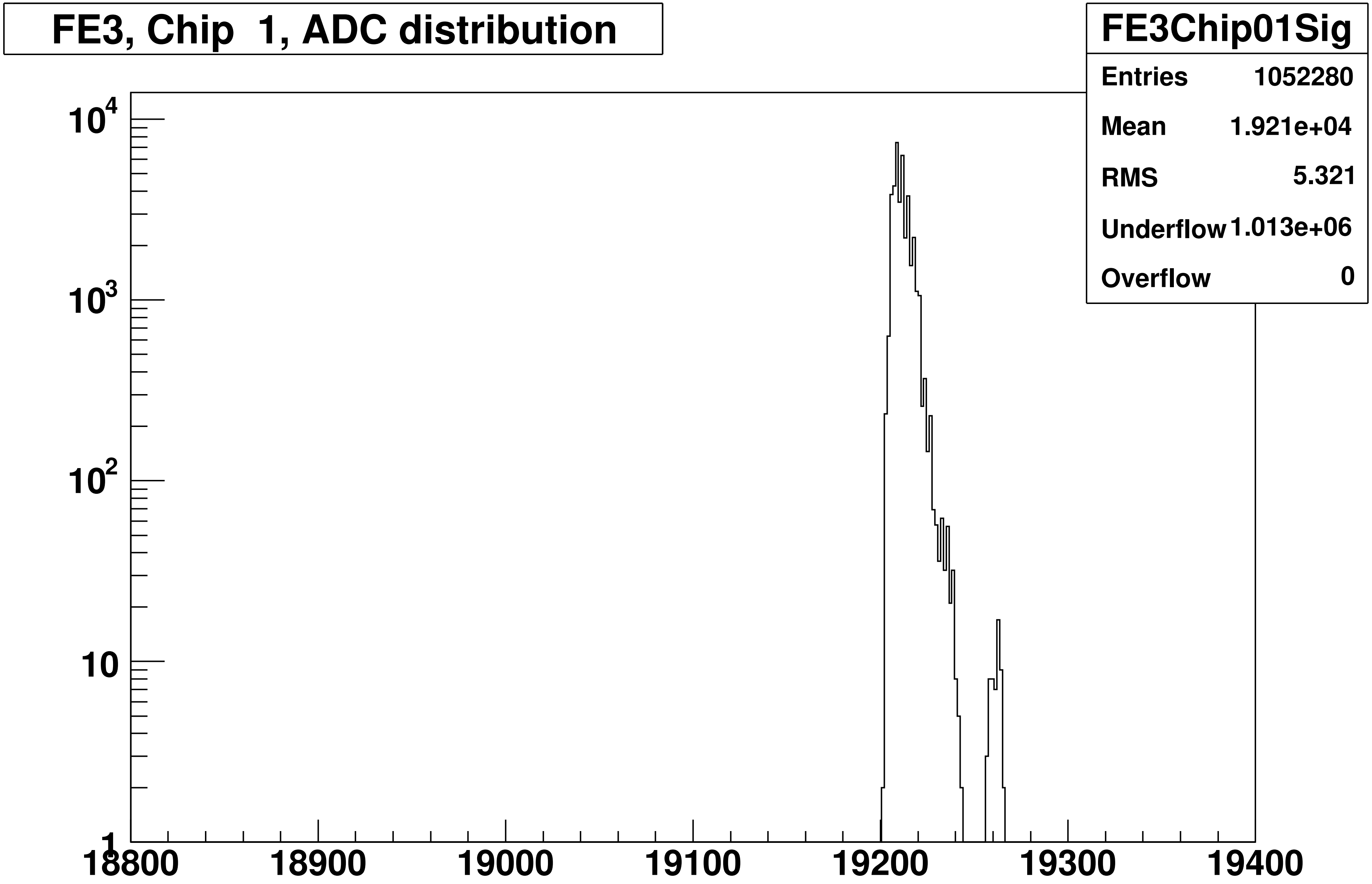

FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 1052280
Mean 1.921e+04
RMS 5.321
Underflow 1.013e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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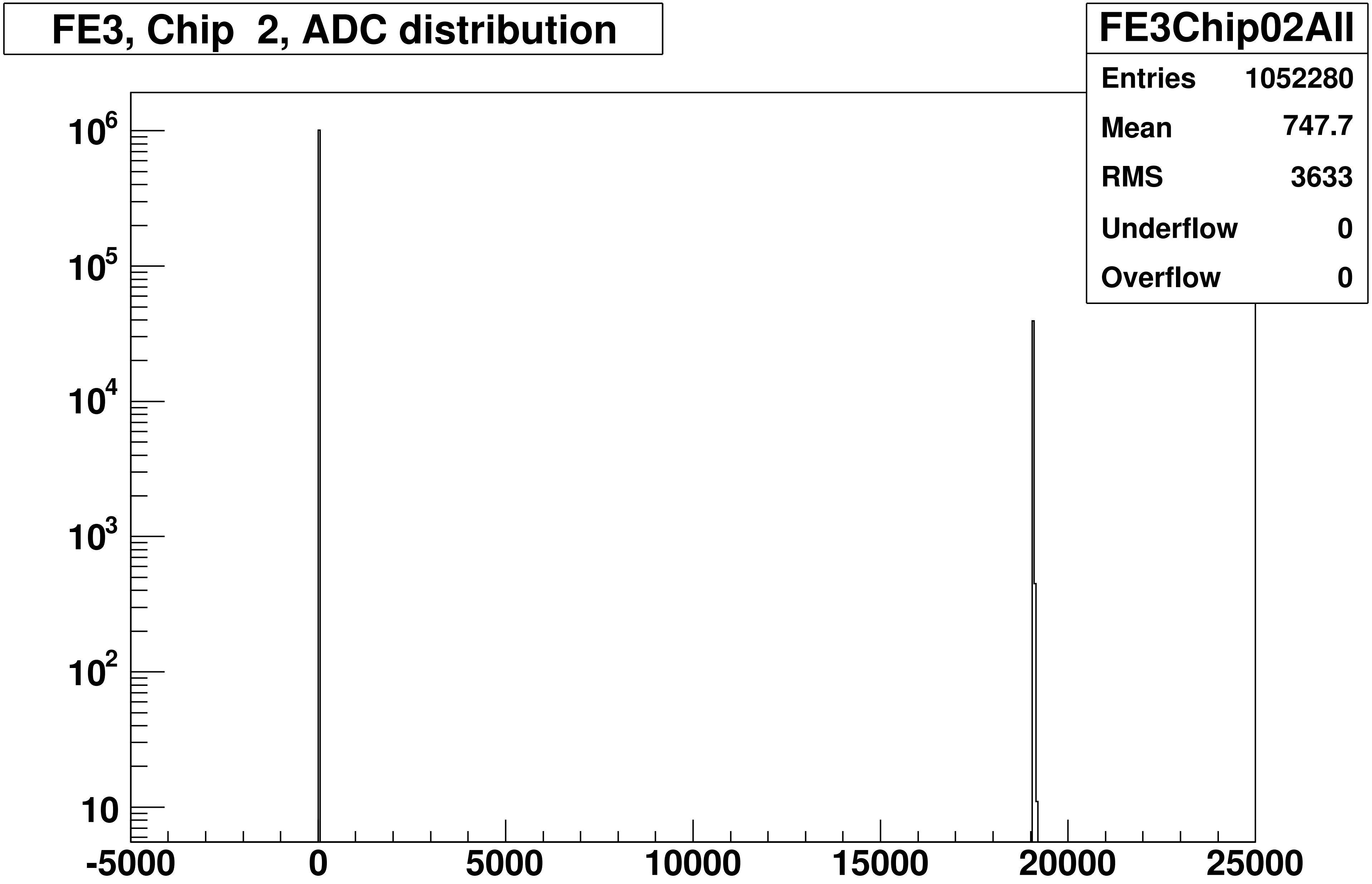
FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 1052280
Mean 747.7
RMS 3633
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
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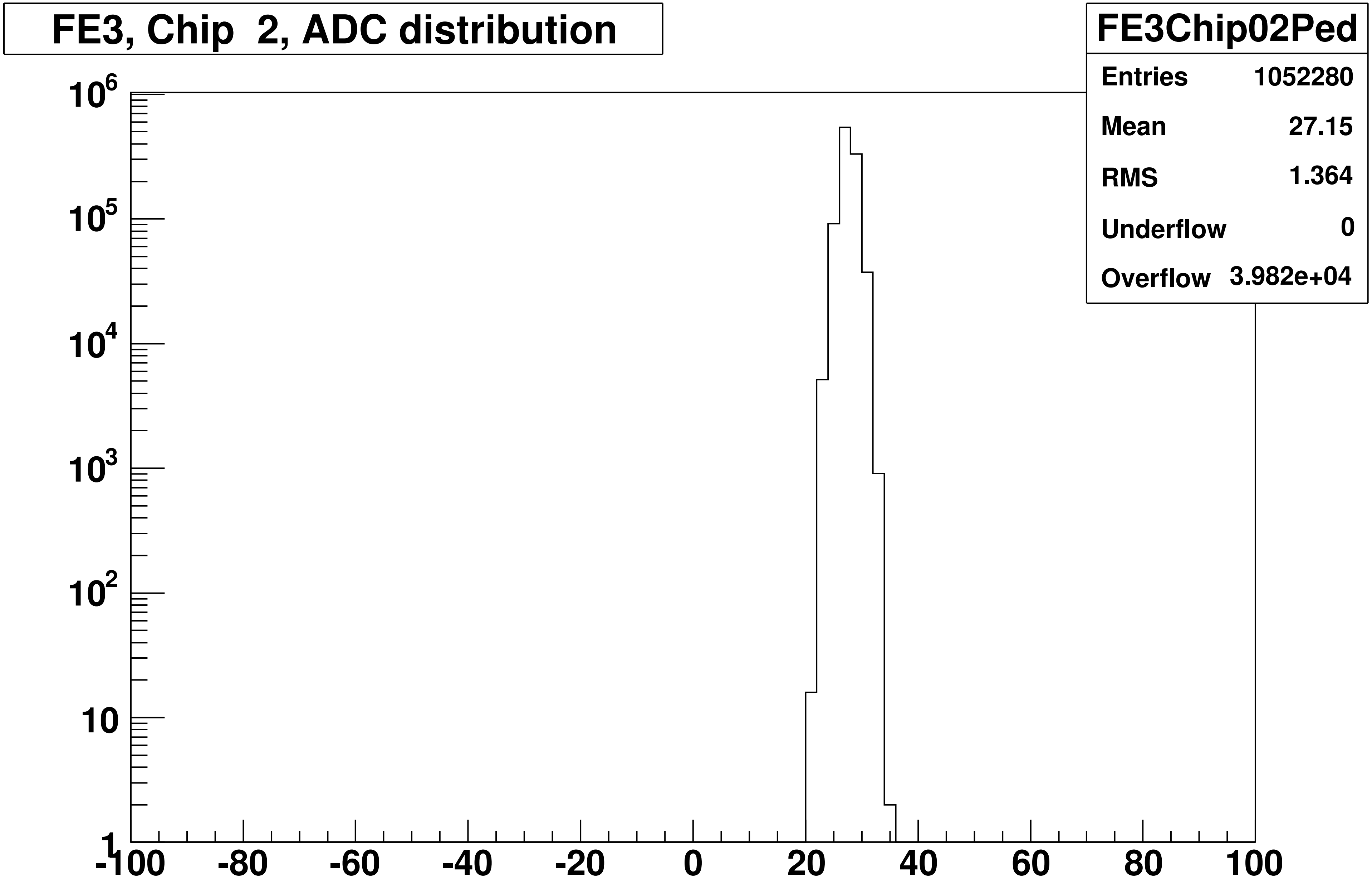

FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 1052280
Mean 27.15
RMS 1.364
Underflow 0
Overflow 3.982e+04
10^6
10^5
10^4
10^3
10^2
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1
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-20
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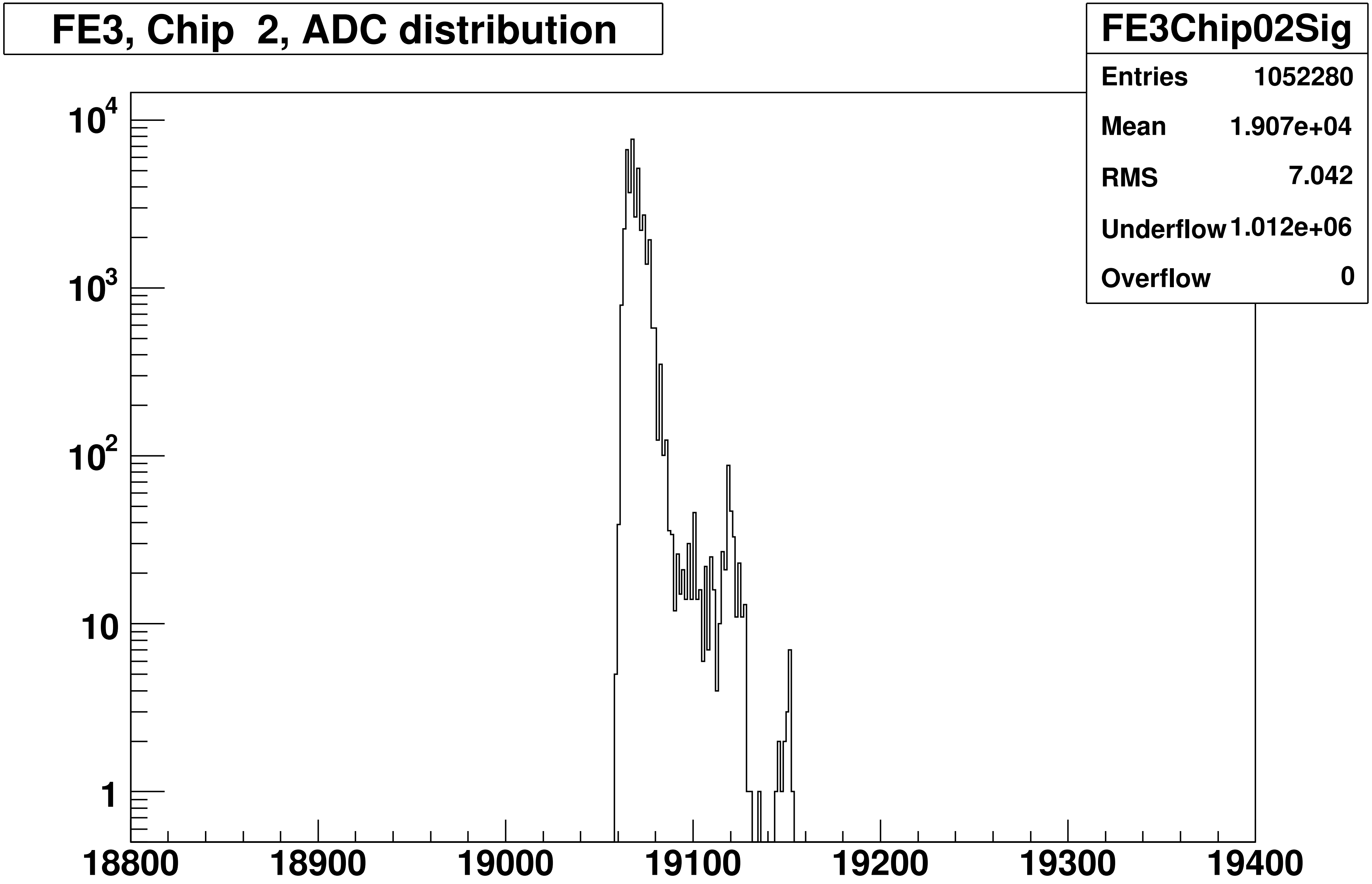
FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 1052280
Mean 1.907e+04
RMS 7.042
Underflow 1.012e+06
Overflow 0
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10^3
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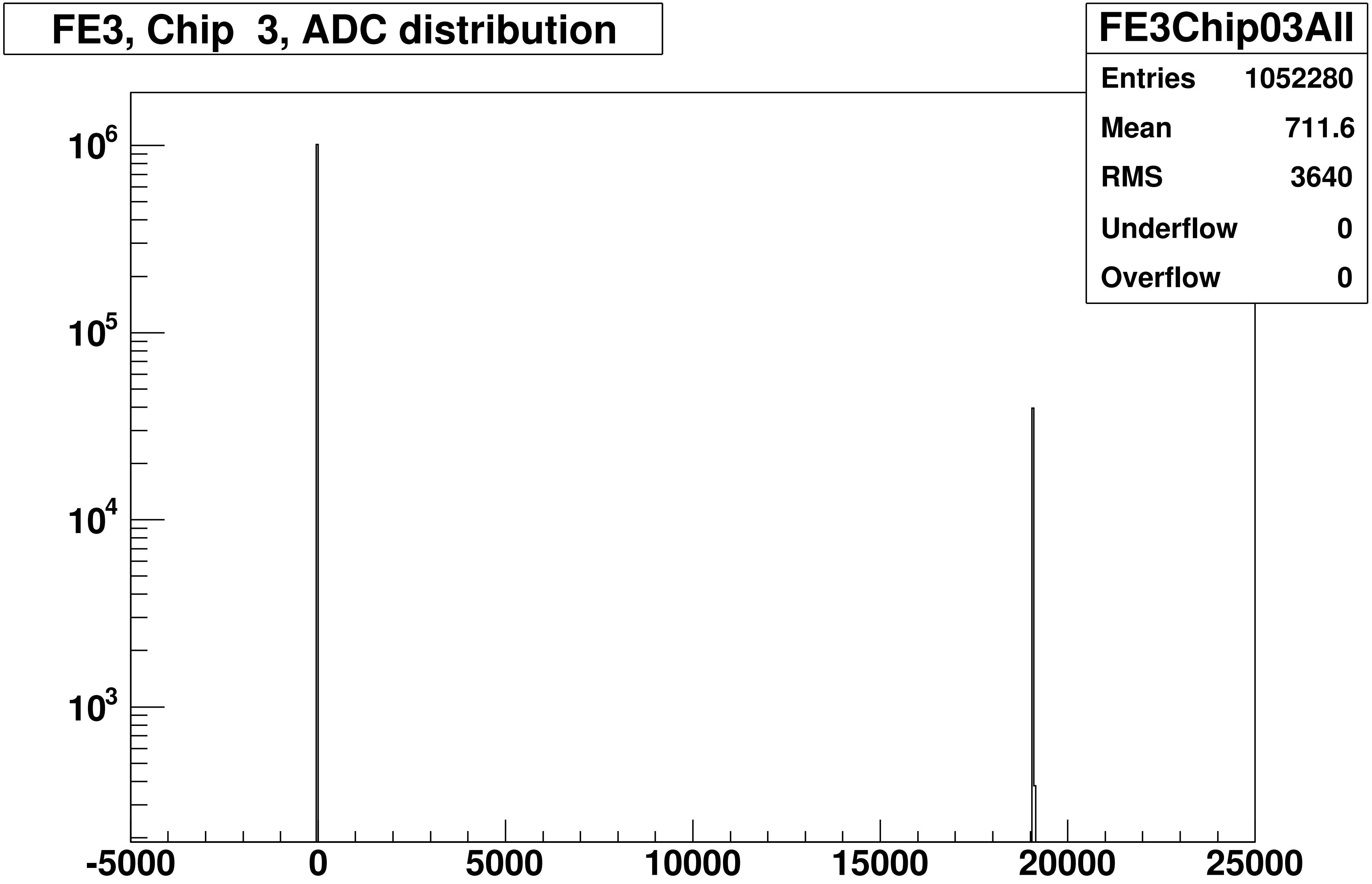
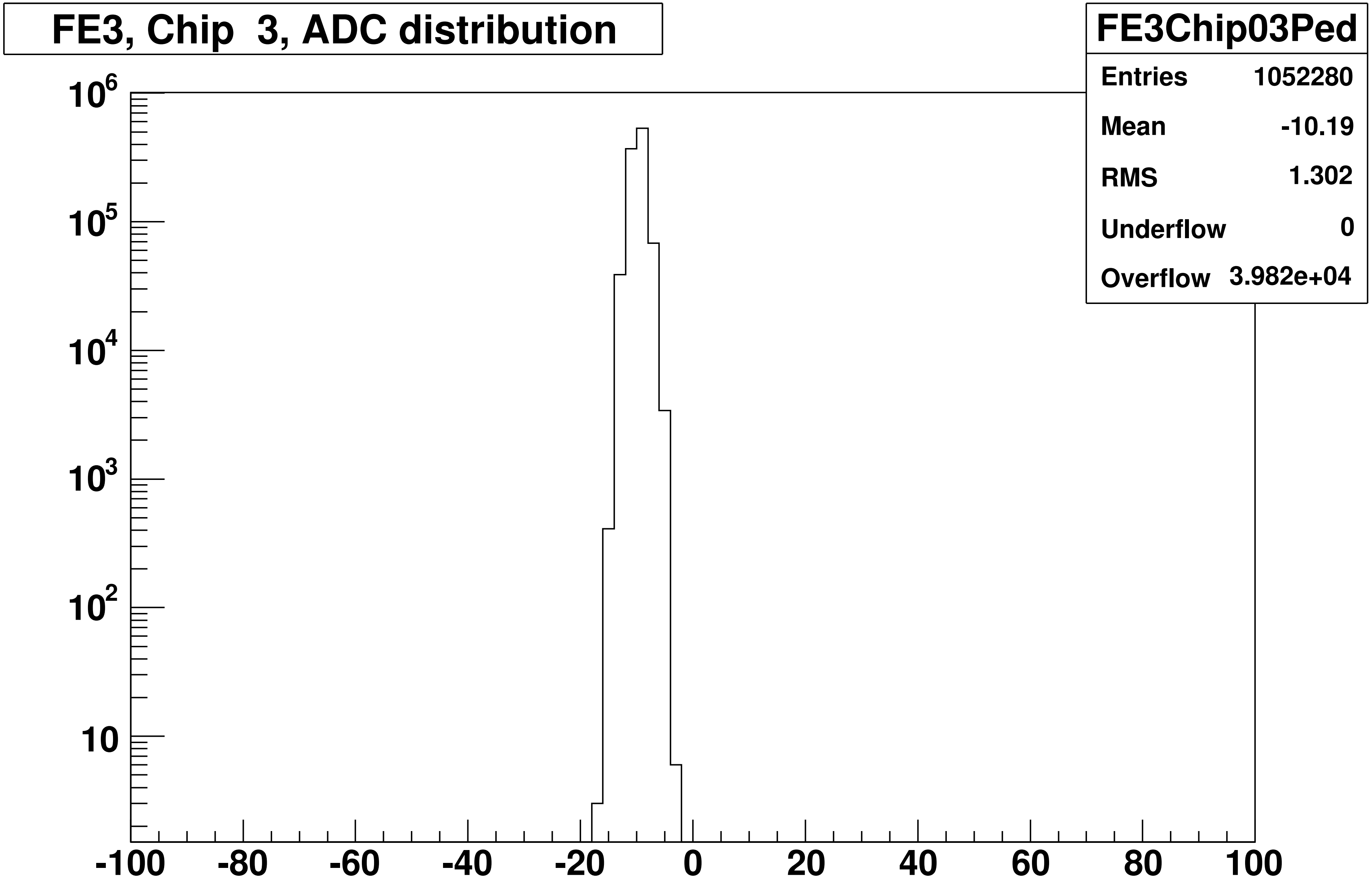
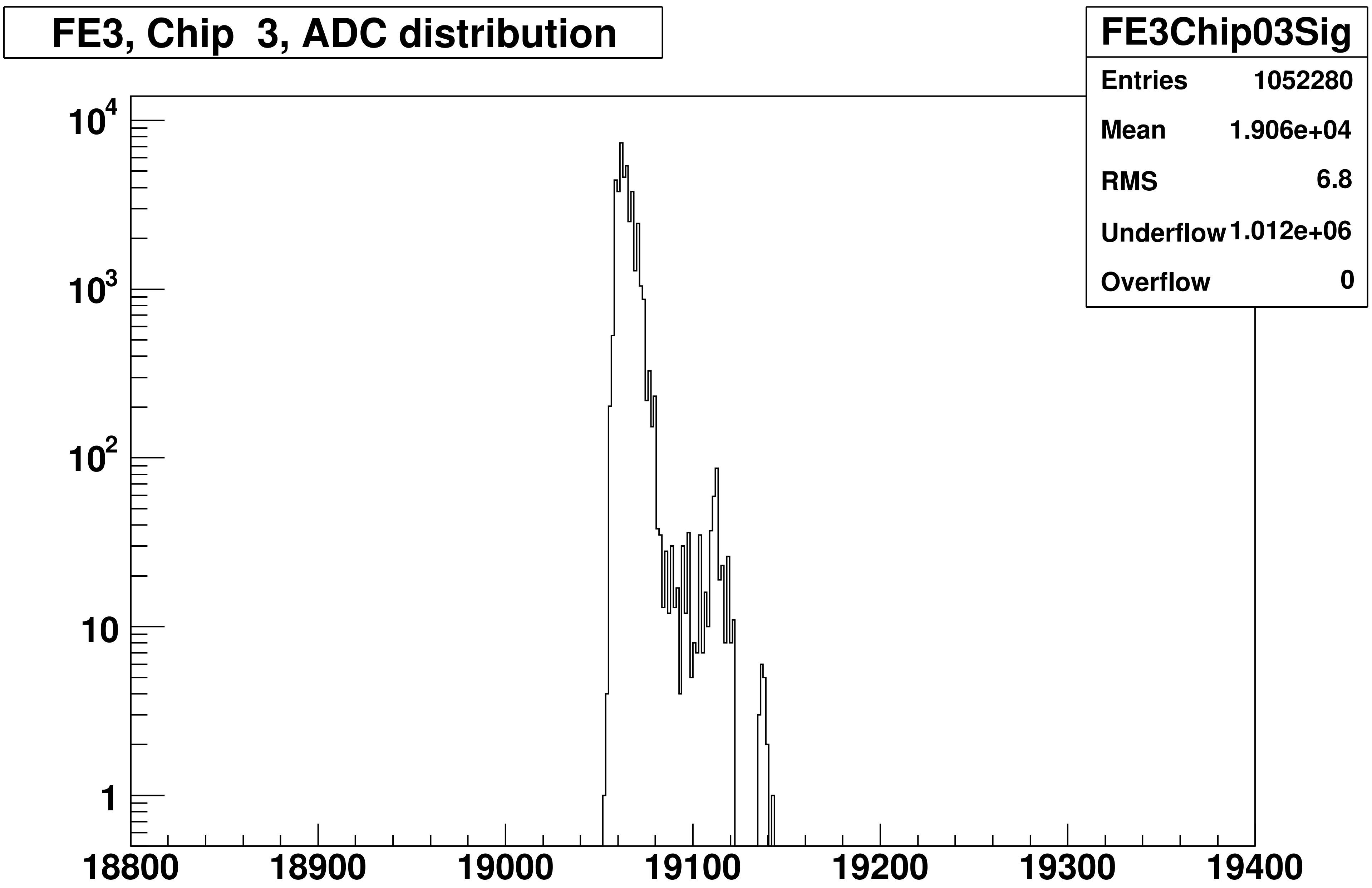

FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 1052280
Mean 711.6
RMS 3640
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 1052280
Mean -10.19
RMS 1.302
Underflow 0
Overflow 3.982e+04
10^6
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 1052280
Mean 1.906e+04
RMS 6.8
Underflow 1.012e+06
Overflow 0
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10^3
10^2
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1
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18900
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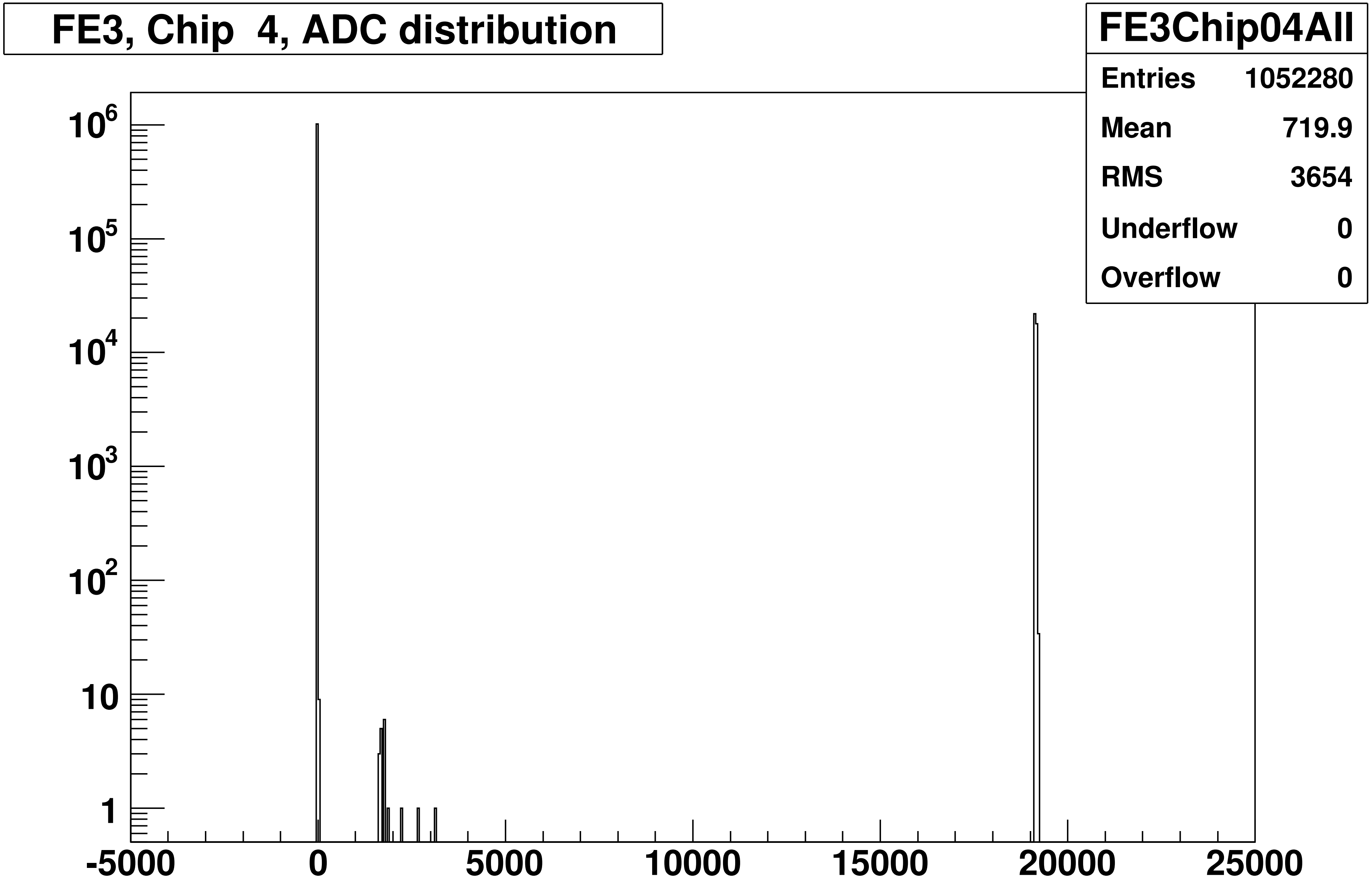

FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 1052280
Mean 719.9
RMS 3654
Underflow 0
Overflow 0
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10^4
10^3
10^2
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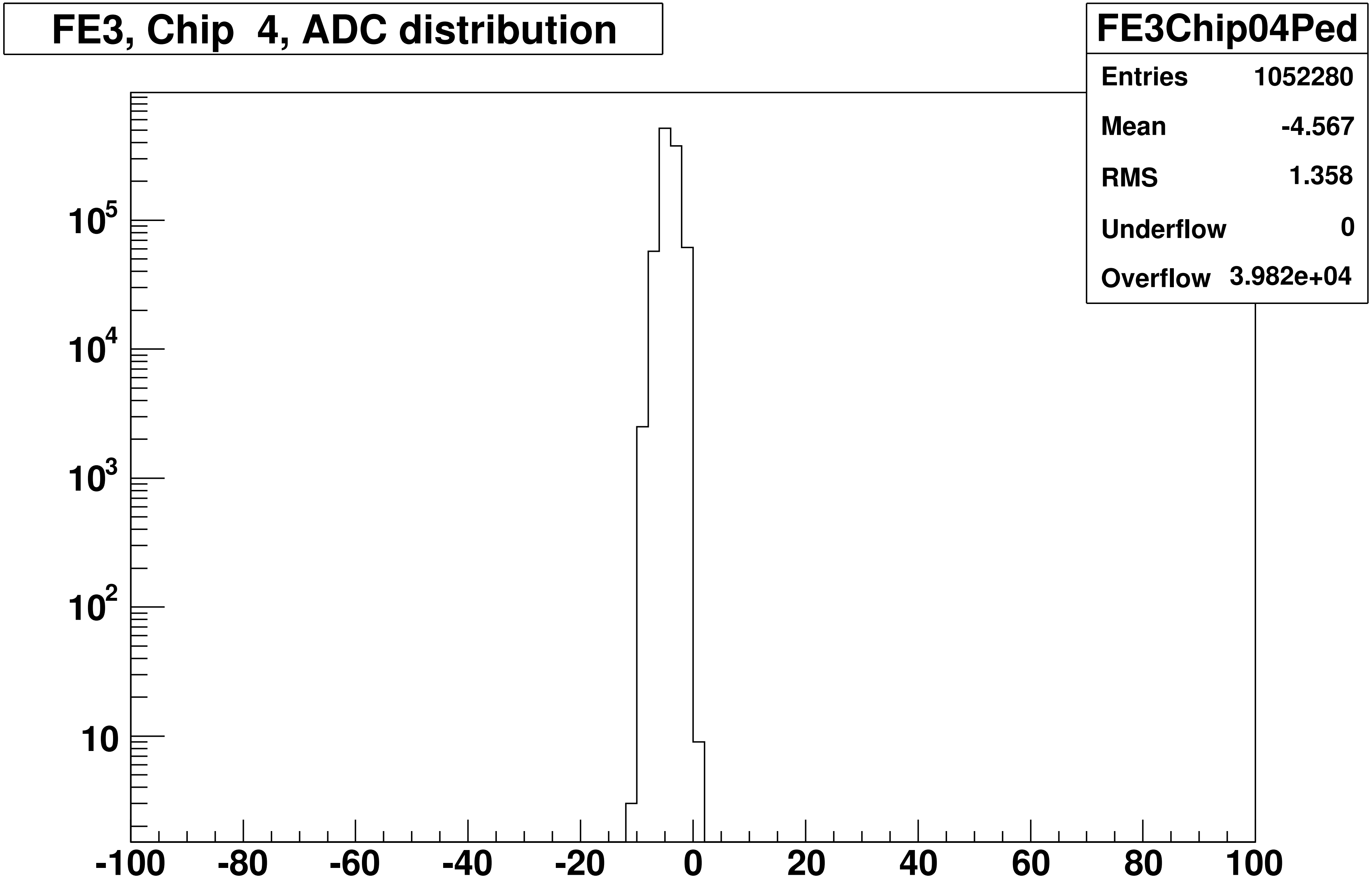

FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 1052280
Mean -4.567
RMS 1.358
Underflow 0
Overflow 3.982e+04
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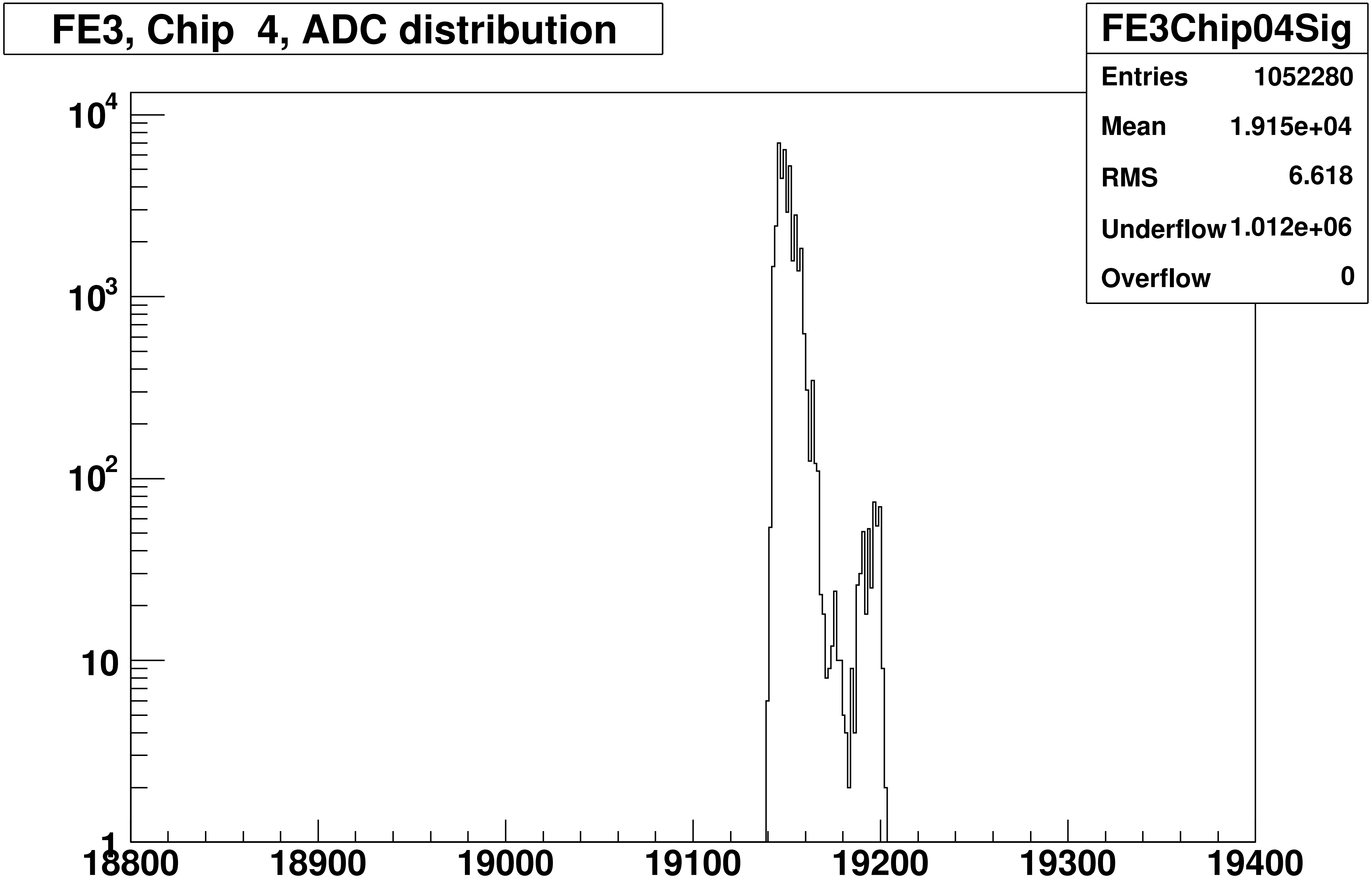
FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 1052280
Mean 1.915e+04
RMS 6.618
Underflow 1.012e+06
Overflow 0
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10^3
10^2
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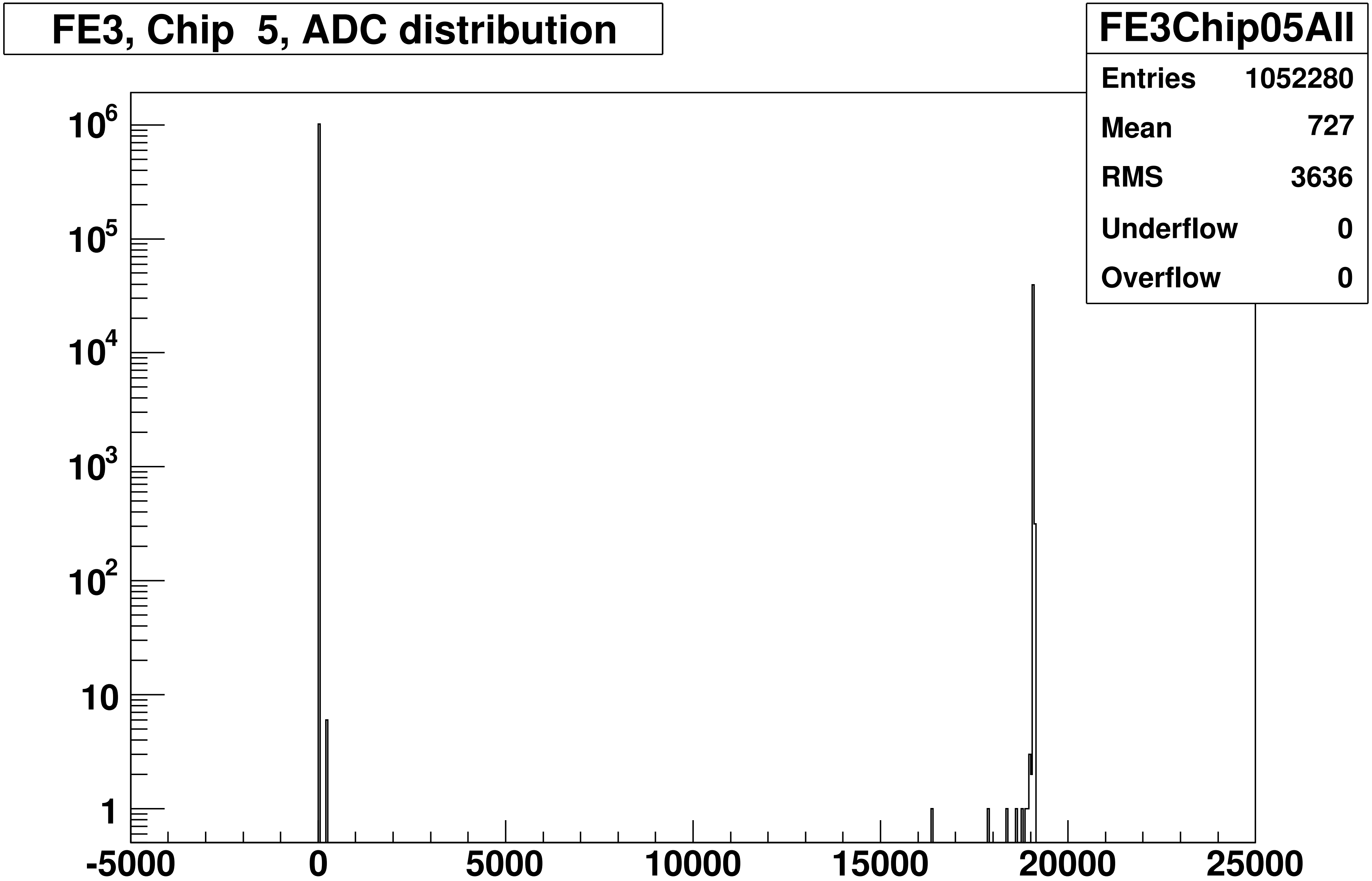
FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 1052280
Mean 727
RMS 3636
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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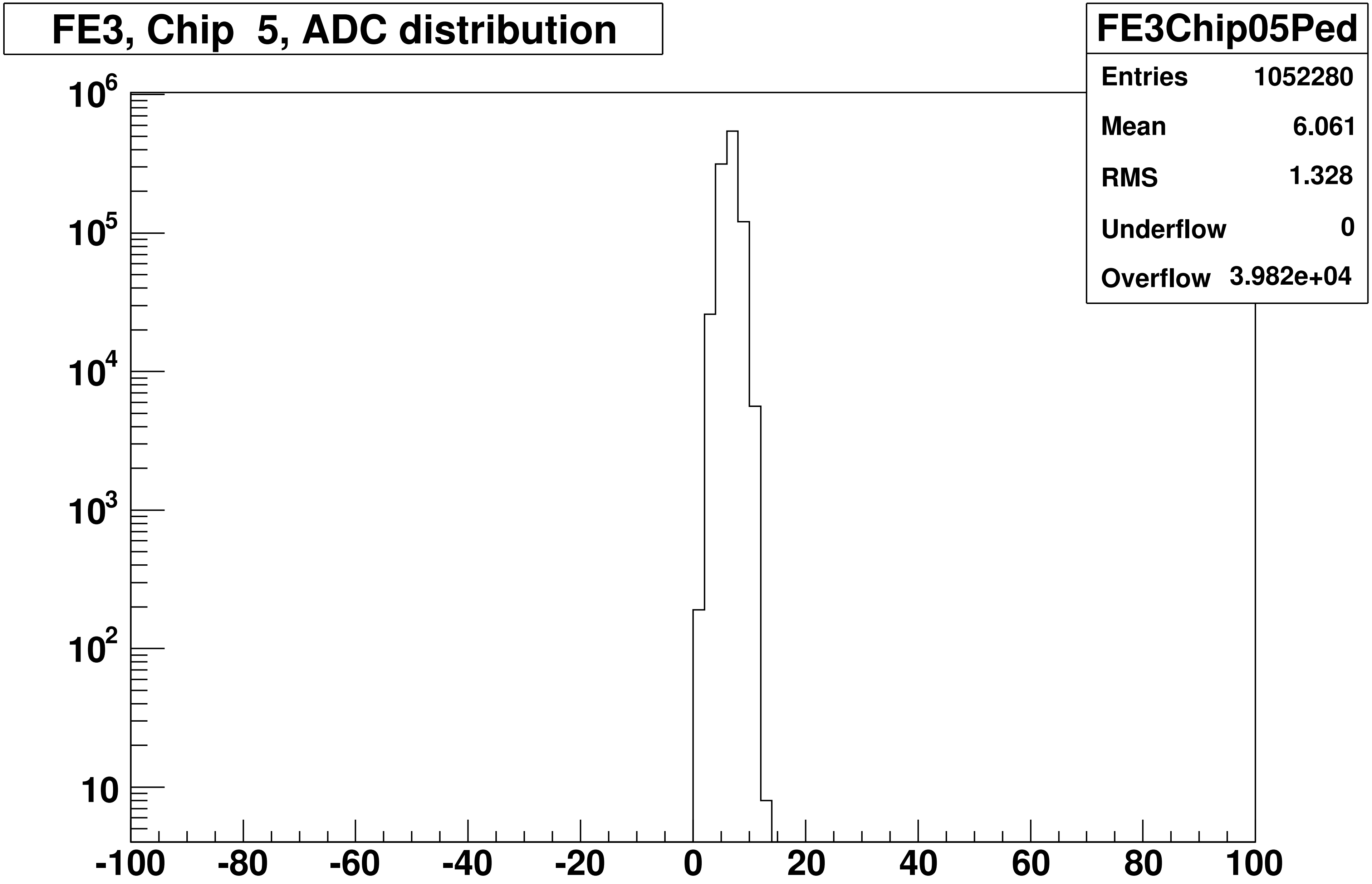
FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 1052280
Mean 6.061
RMS 1.328
Underflow 0
Overflow 3.982e+04
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10^5
10^4
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10^2
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-100
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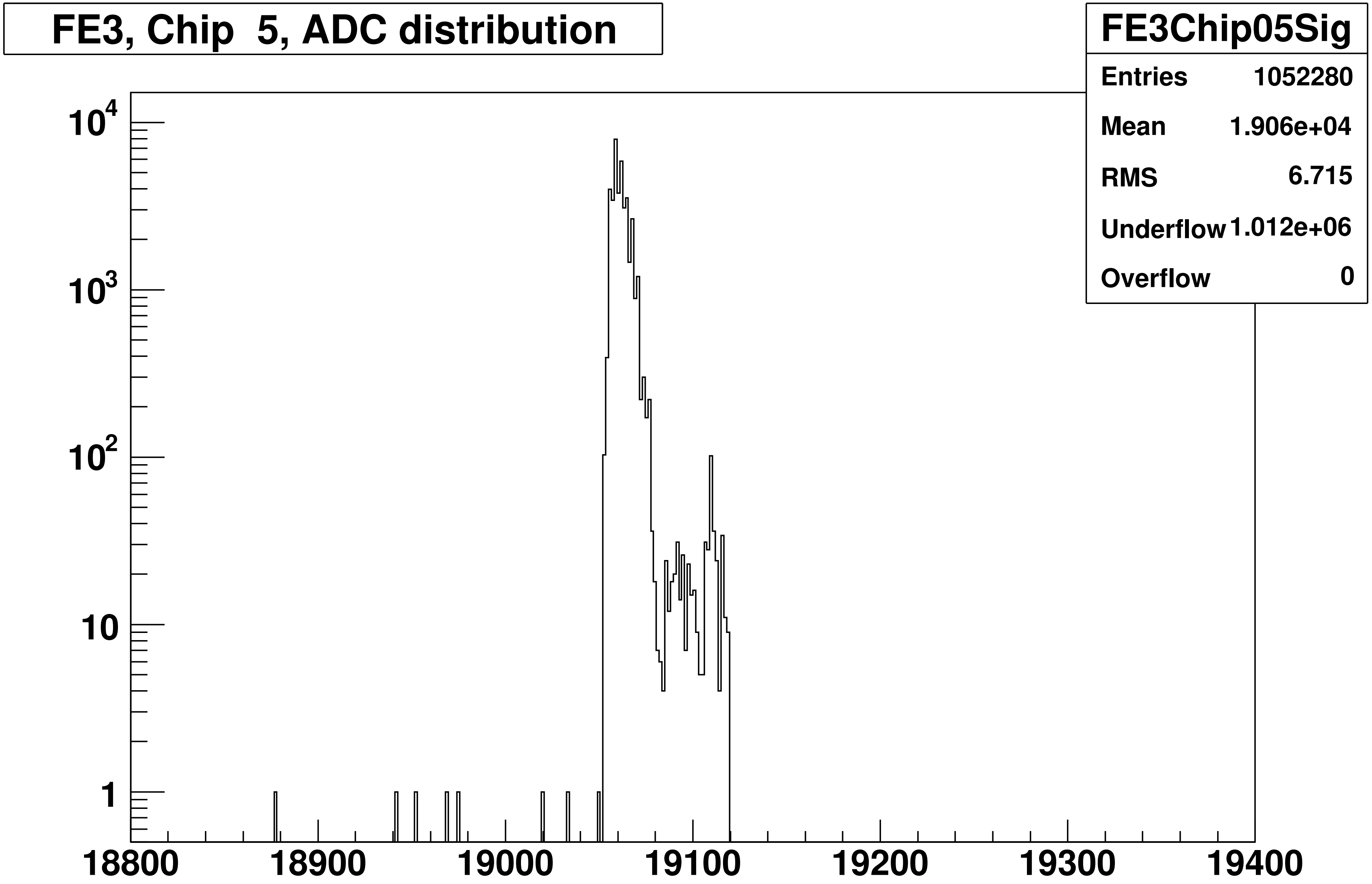
FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 1052280
Mean 1.906e+04
RMS 6.715
Underflow 1.012e+06
Overflow 0
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10^3
10^2
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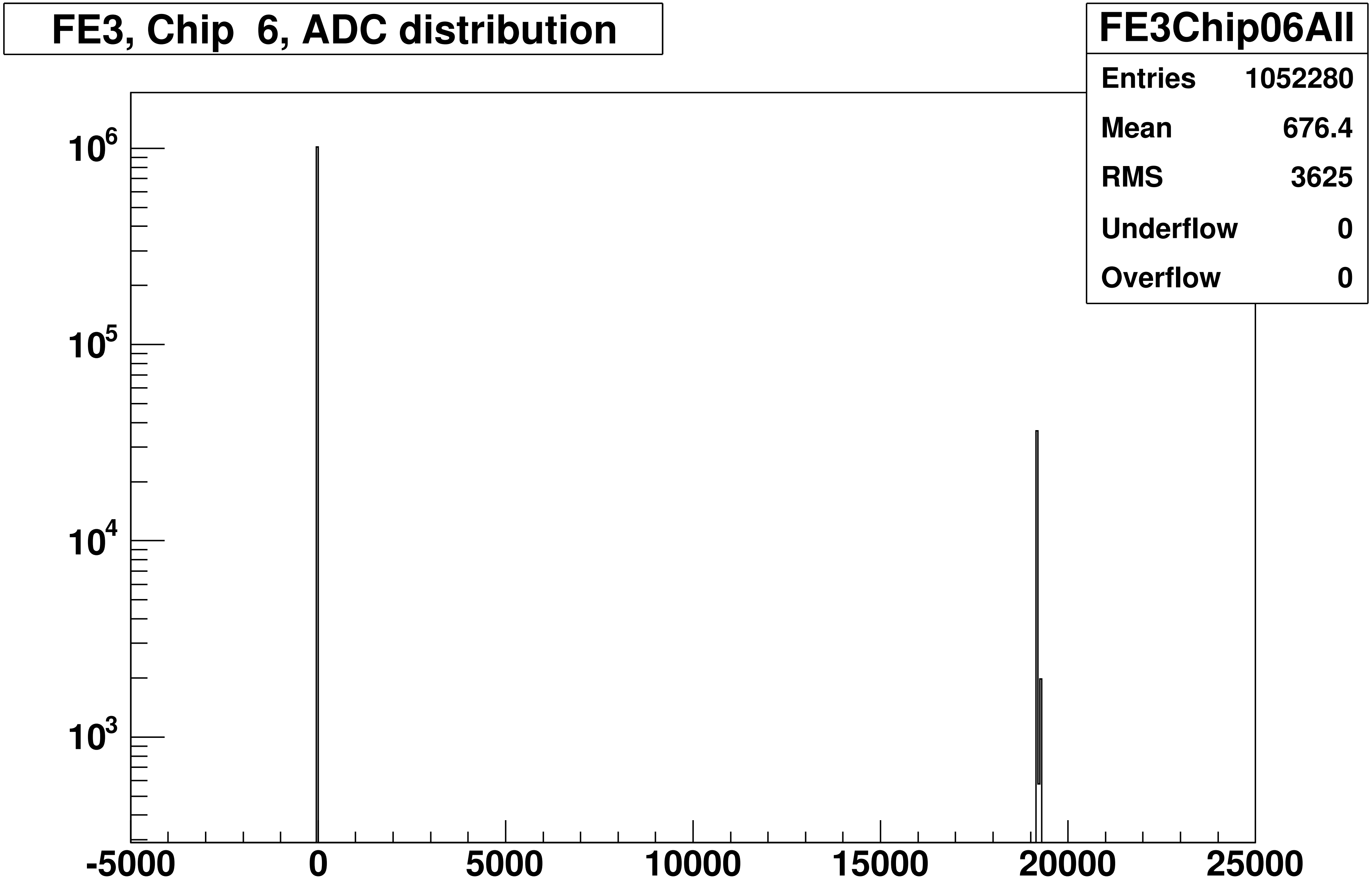
FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 1052280
Mean 676.4
RMS 3625
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
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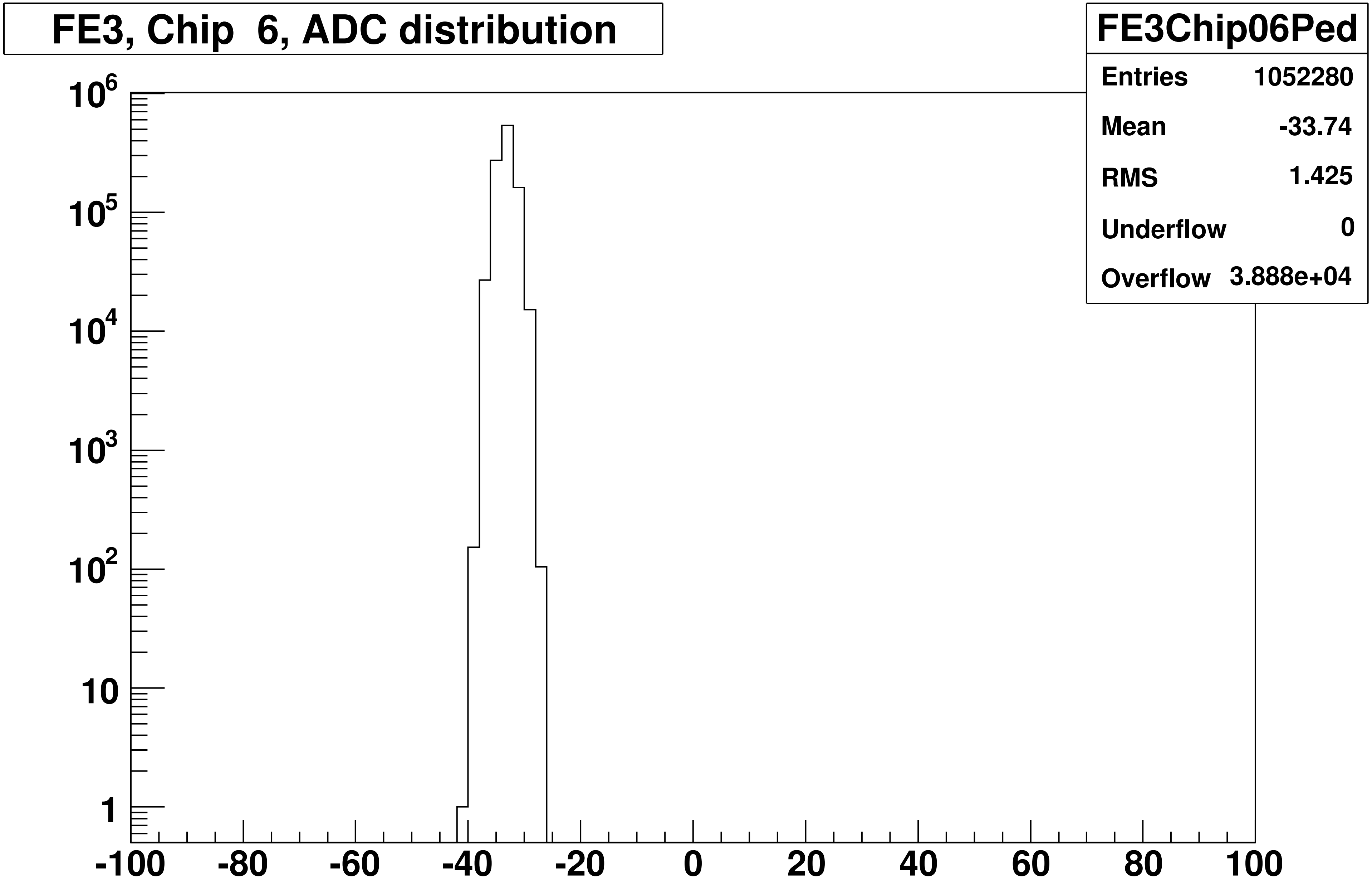
20000
25000


FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 1052280
Mean -33.74
RMS 1.425
Underflow 0
Overflow 3.888e+04
10^6
10^5
10^4
10^3
10^2
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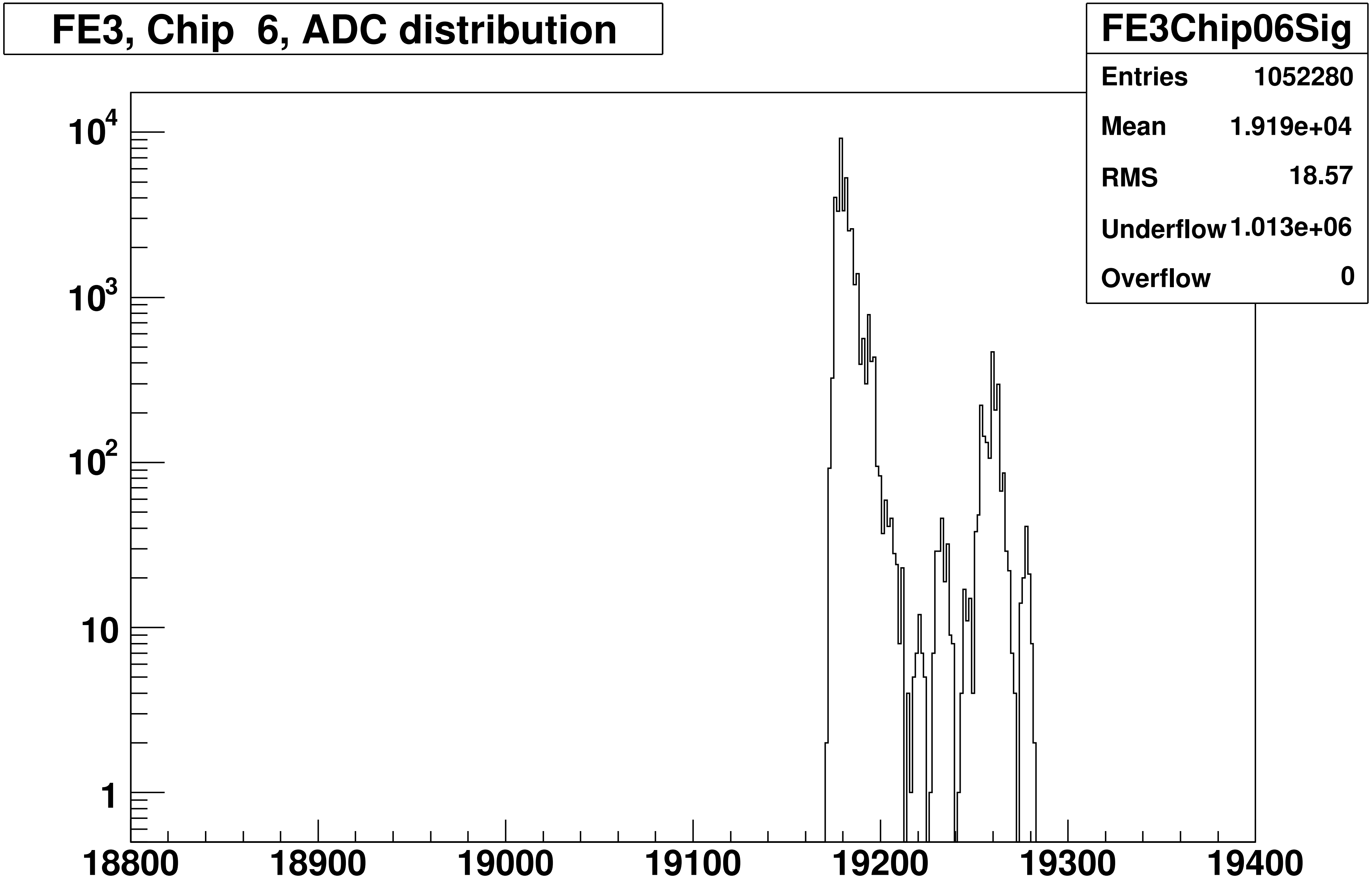
FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 1052280
Mean 1.919e+04
RMS 18.57
Underflow 1.013e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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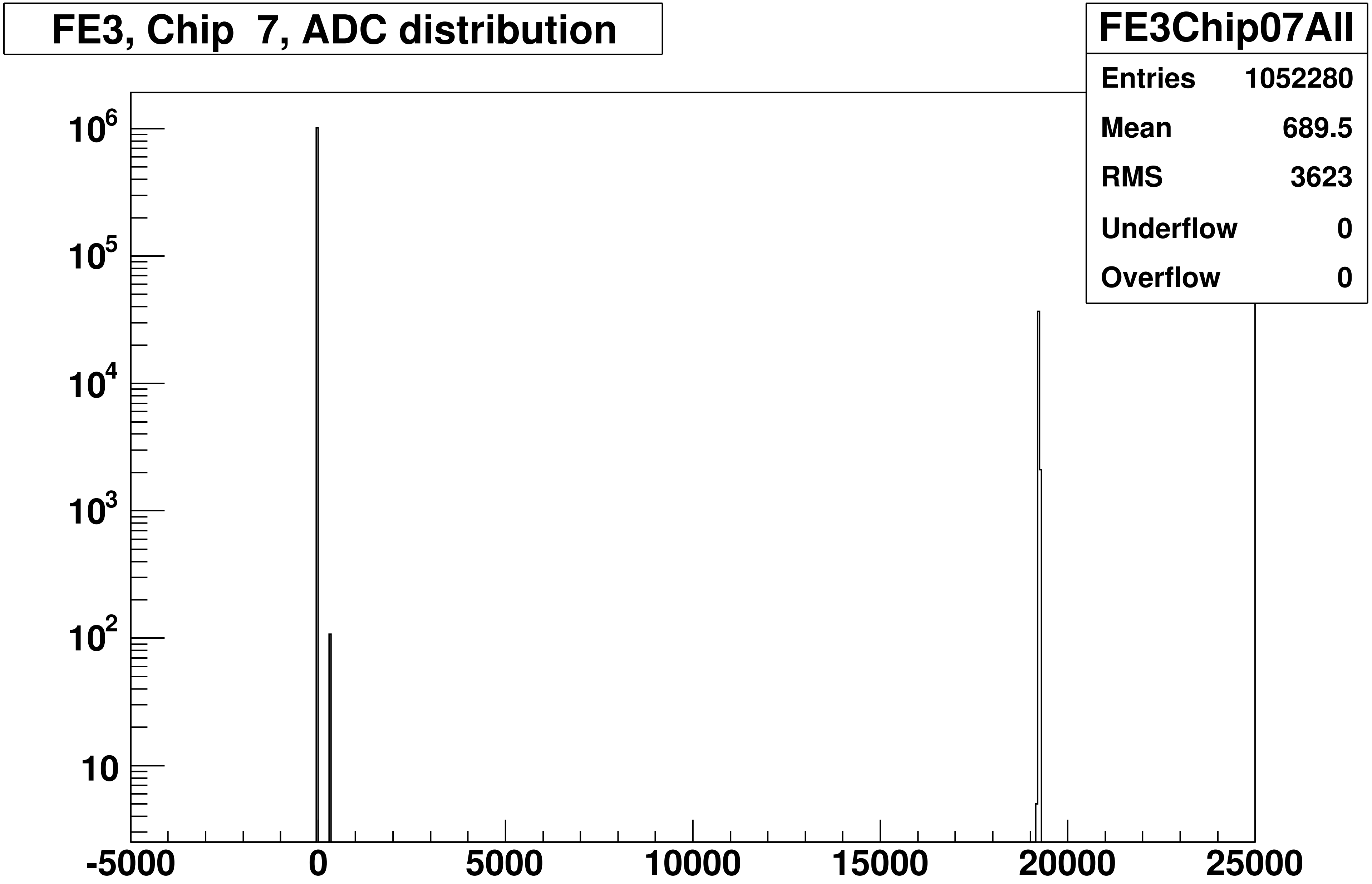
FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 1052280
Mean 689.5
RMS 3623
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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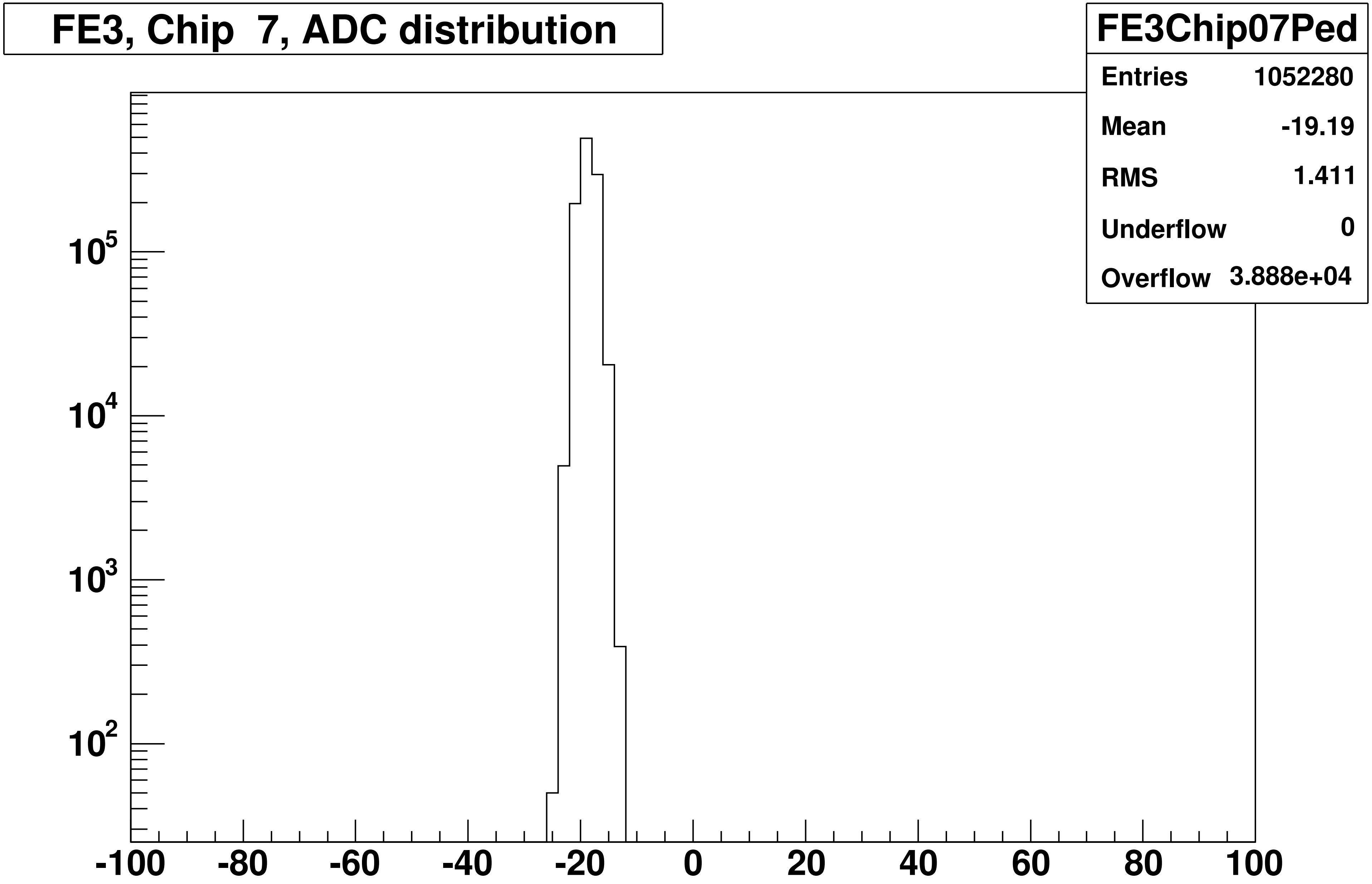
FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 1052280
Mean -19.19
RMS 1.411
Underflow 0
Overflow 3.888e+04
10^5
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10^3
10^2
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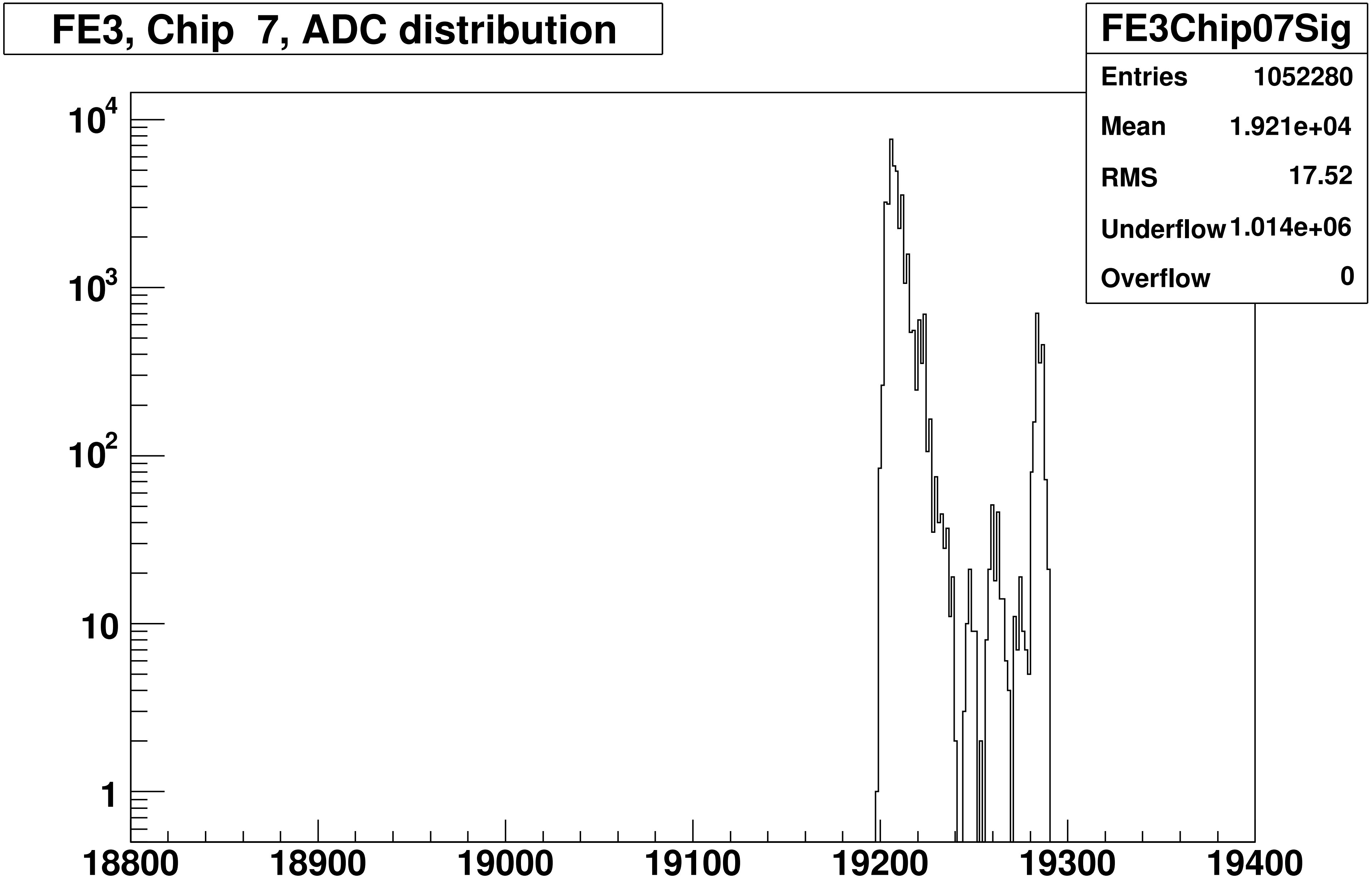
FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 1052280
Mean 1.921e+04
RMS 17.52
Underflow 1.014e+06
Overflow 0
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10^3
10^2
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18900
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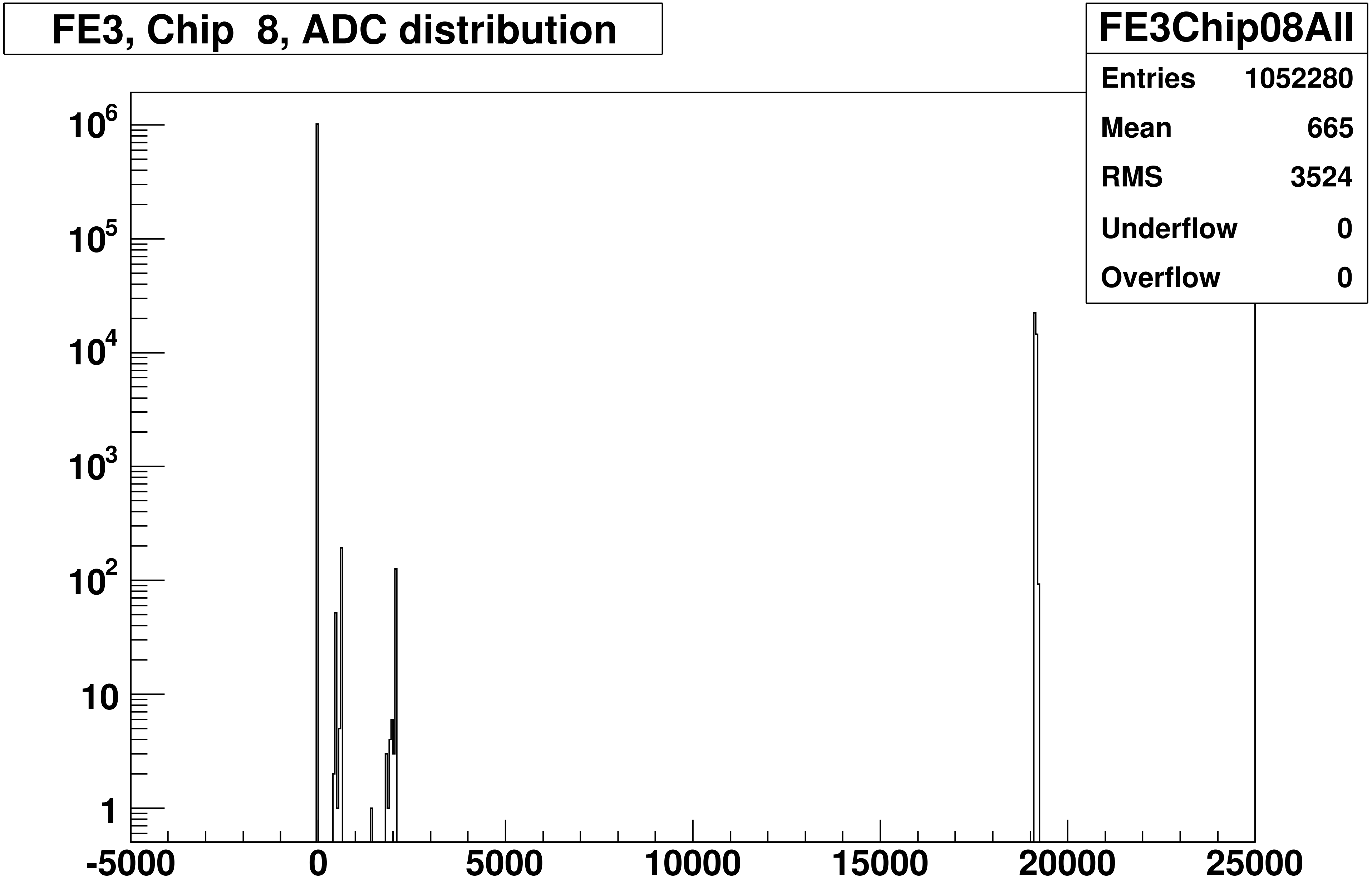
FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 1052280
Mean 665
RMS 3524
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
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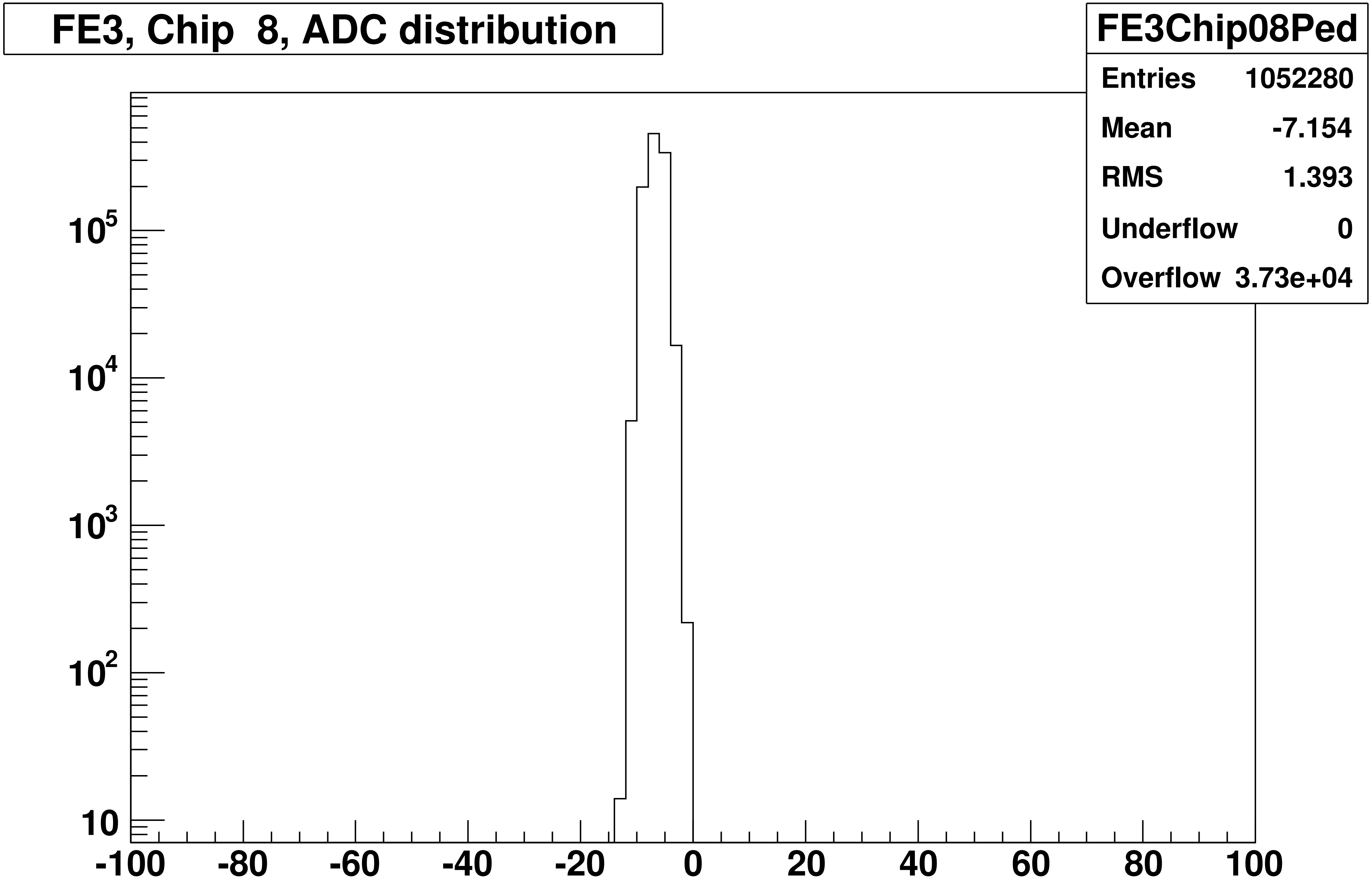
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 1052280
Mean -7.154
RMS 1.393
Underflow 0
Overflow 3.73e+04
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10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
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40
60
80
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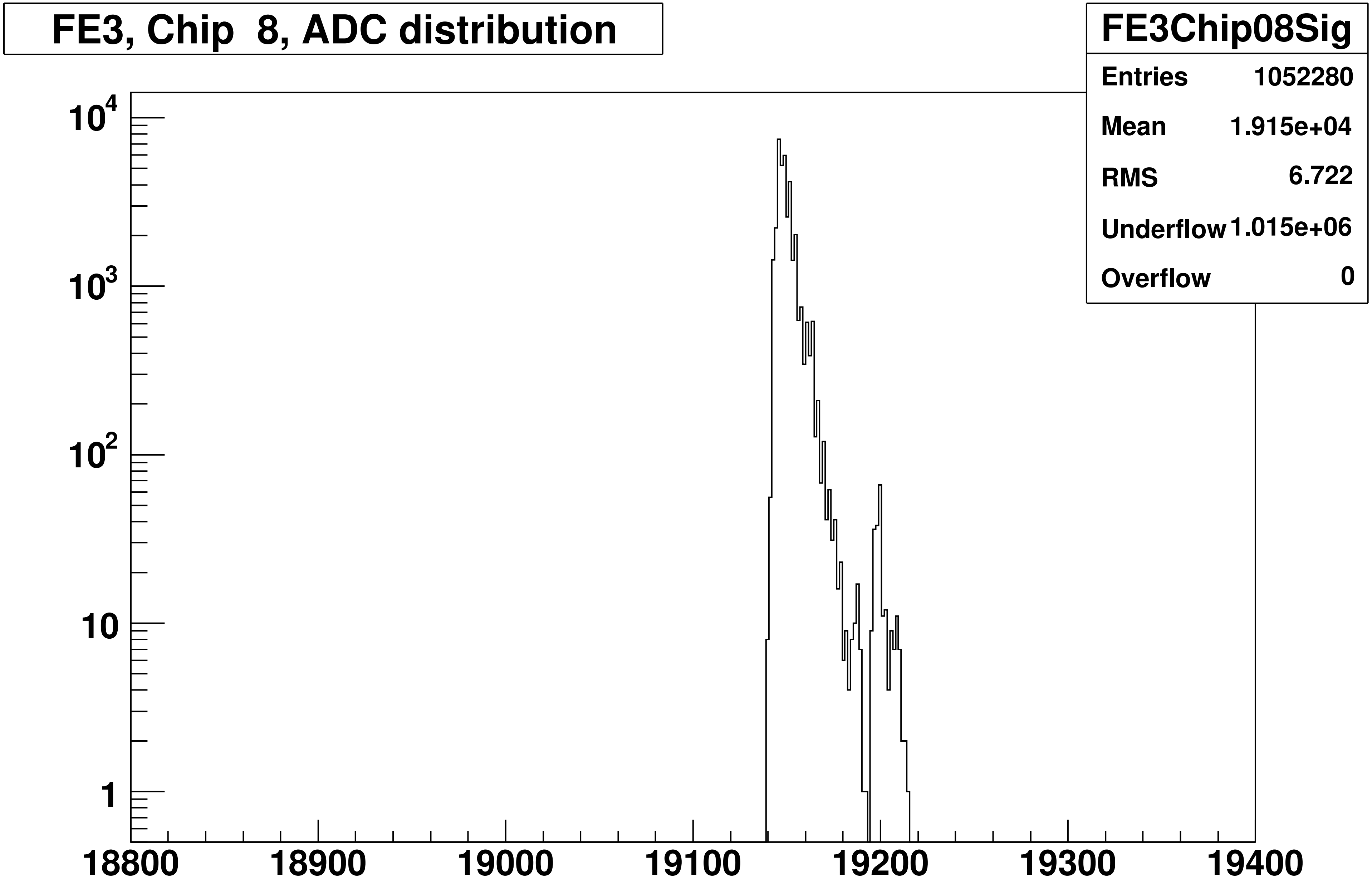
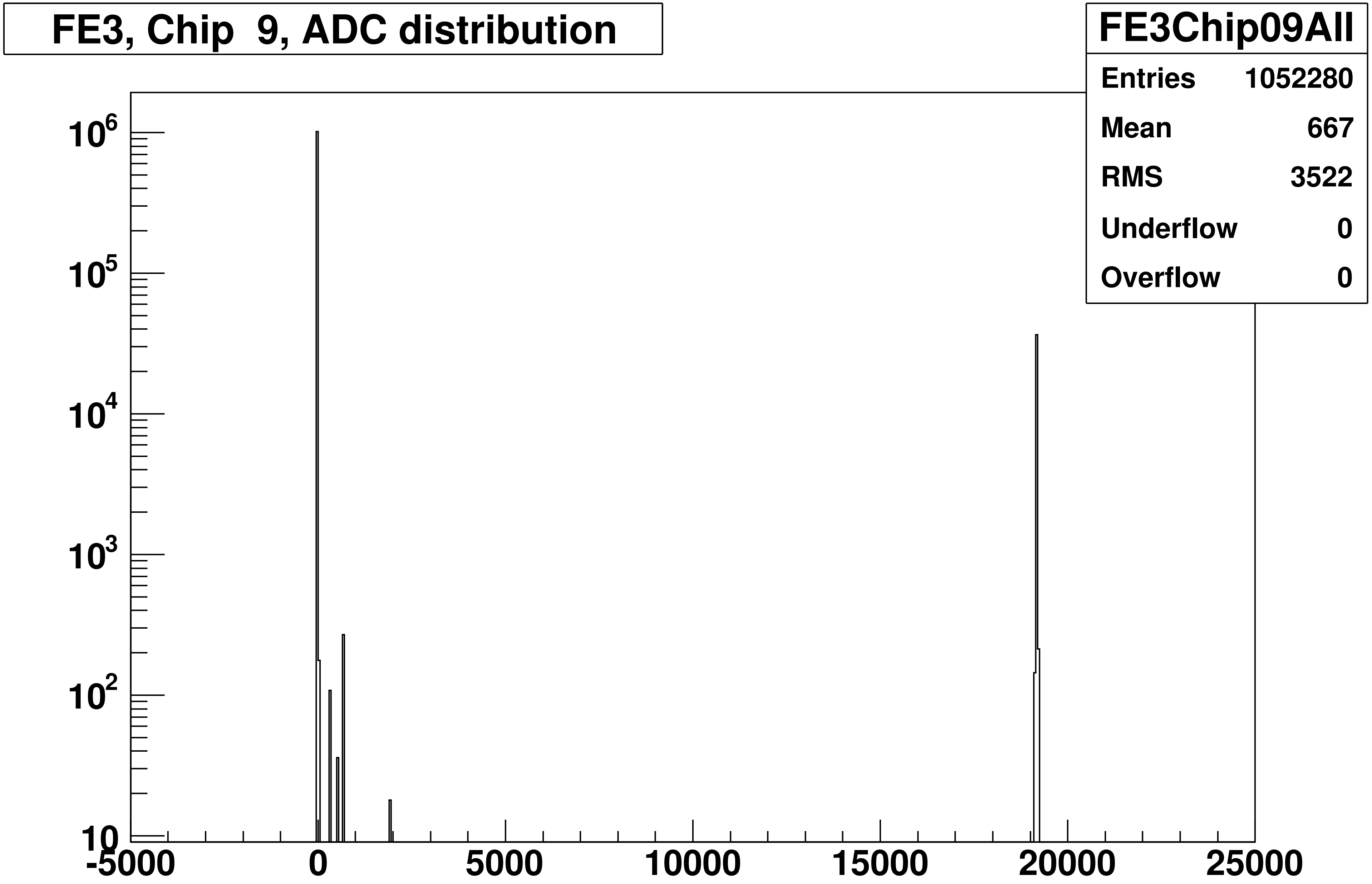
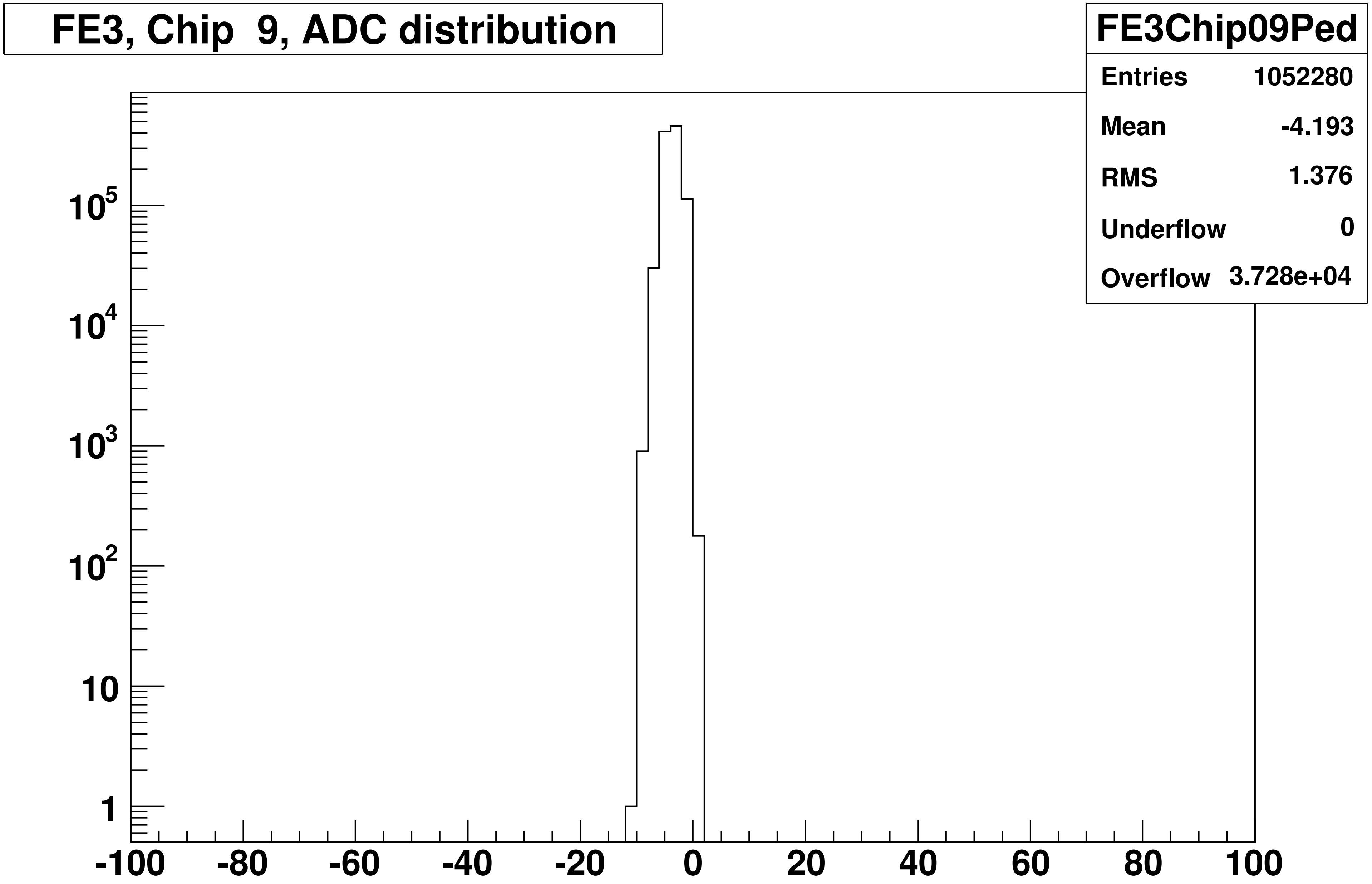
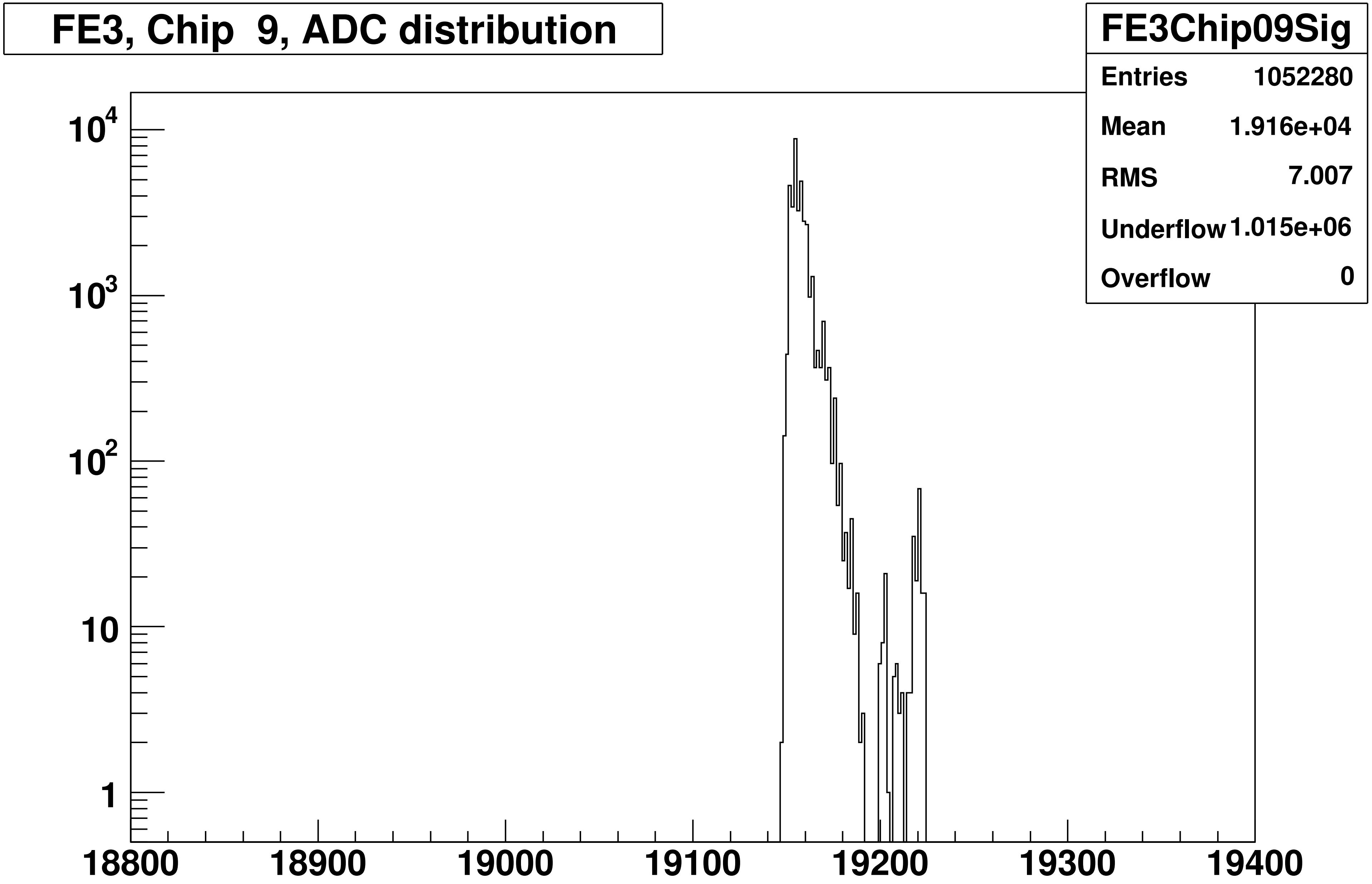


FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 1052280
Mean 1.915e+04
RMS 6.722
Underflow 1.015e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 1052280
Mean 667
RMS 3522
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 1052280
Mean -4.193
RMS 1.376
Underflow 0
Overflow 3.728e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 1052280
Mean 1.916e+04
RMS 7.007
Underflow 1.015e+06
Overflow 0
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10^3
10^2
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18900
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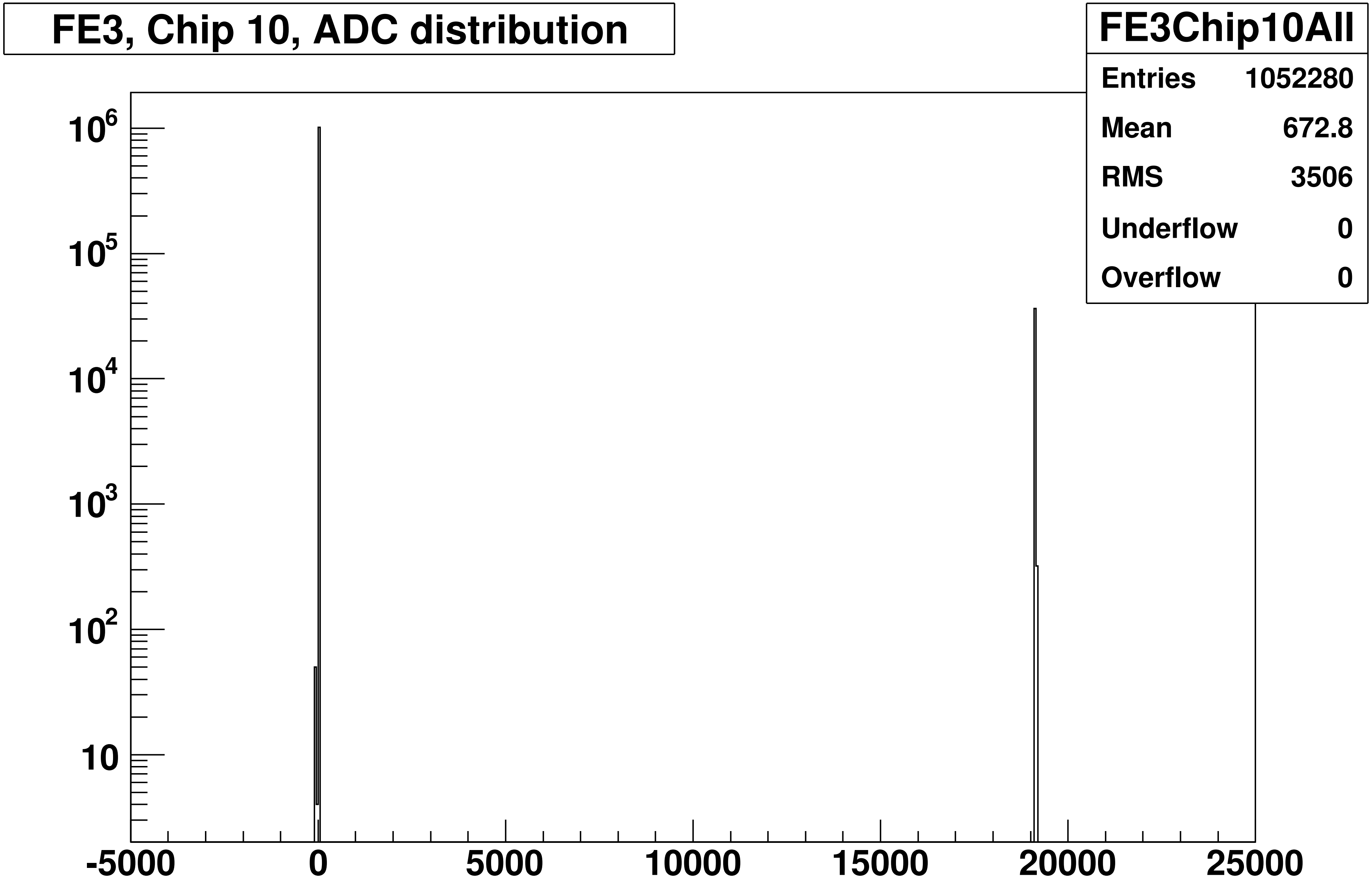
19300
19400


FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 1052280
Mean 672.8
RMS 3506
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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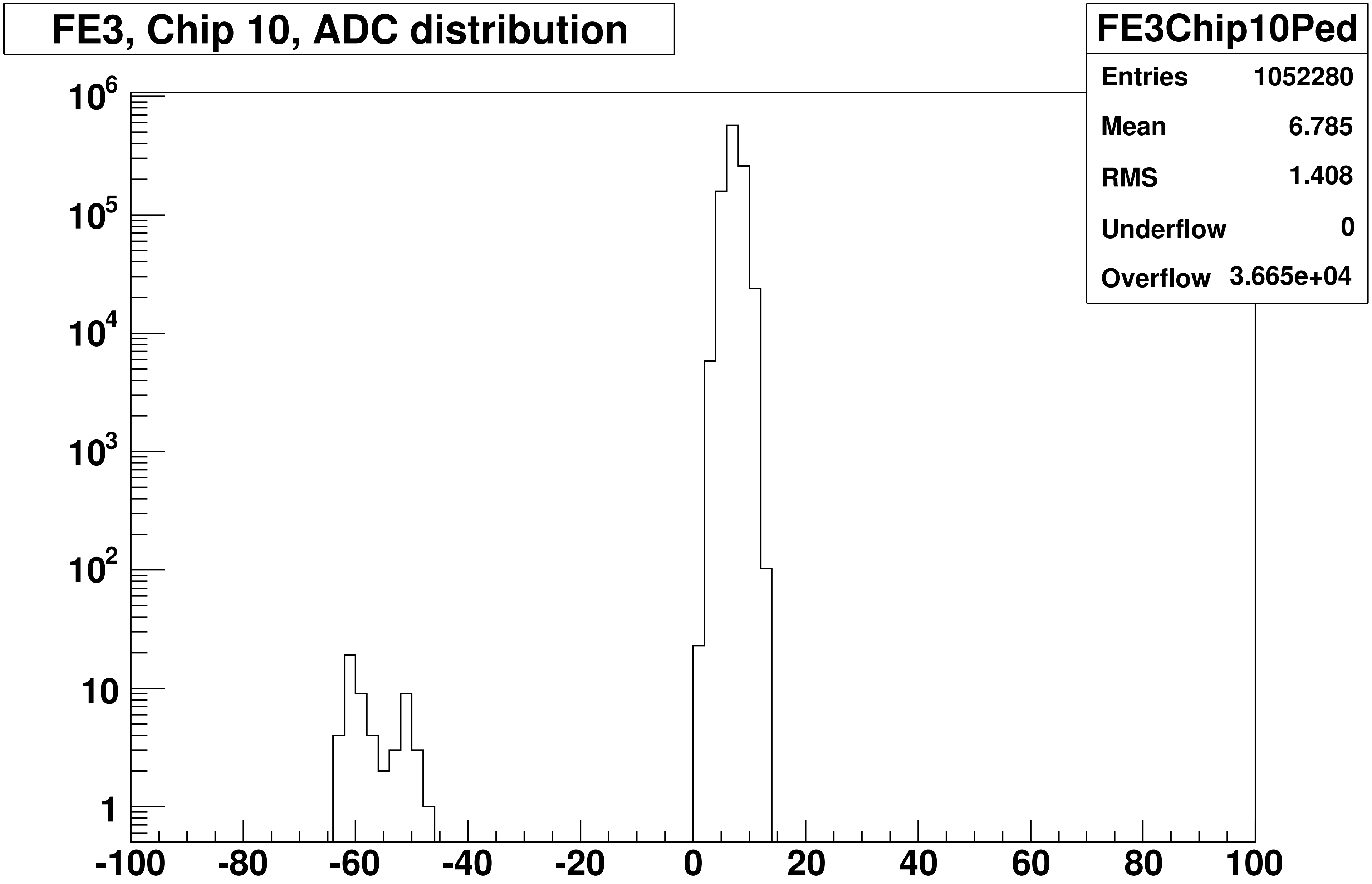
10000
15000
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 1052280
Mean 6.785
RMS 1.408
Underflow 0
Overflow 3.665e+04
10^6
10^5
10^4
10^3
10^2
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-20
0
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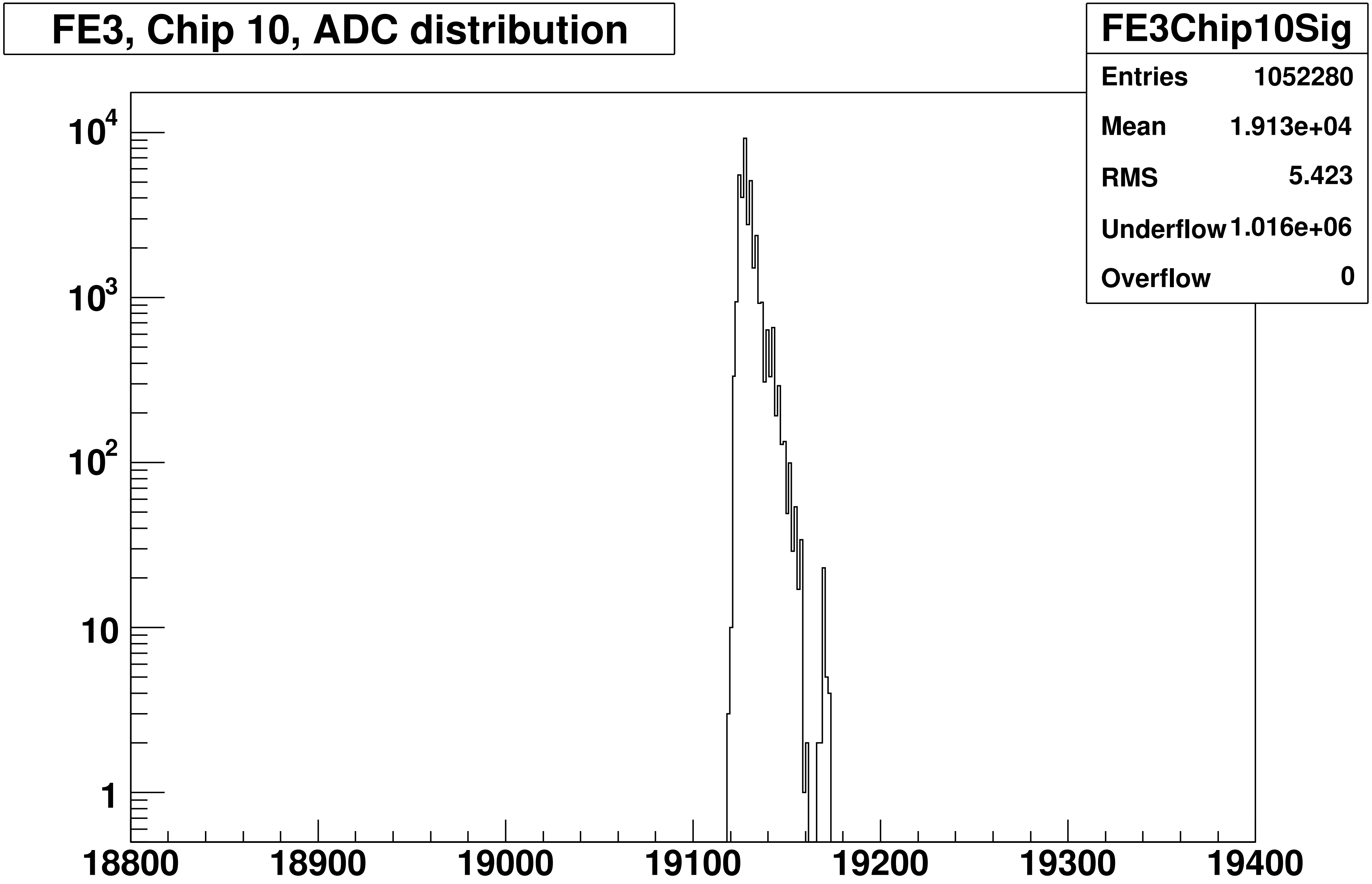
60
80
100



FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 1052280
Mean 1.913e+04
RMS 5.423
Underflow 1.016e+06
Overflow 0
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10^3
10^2
10
1
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18900
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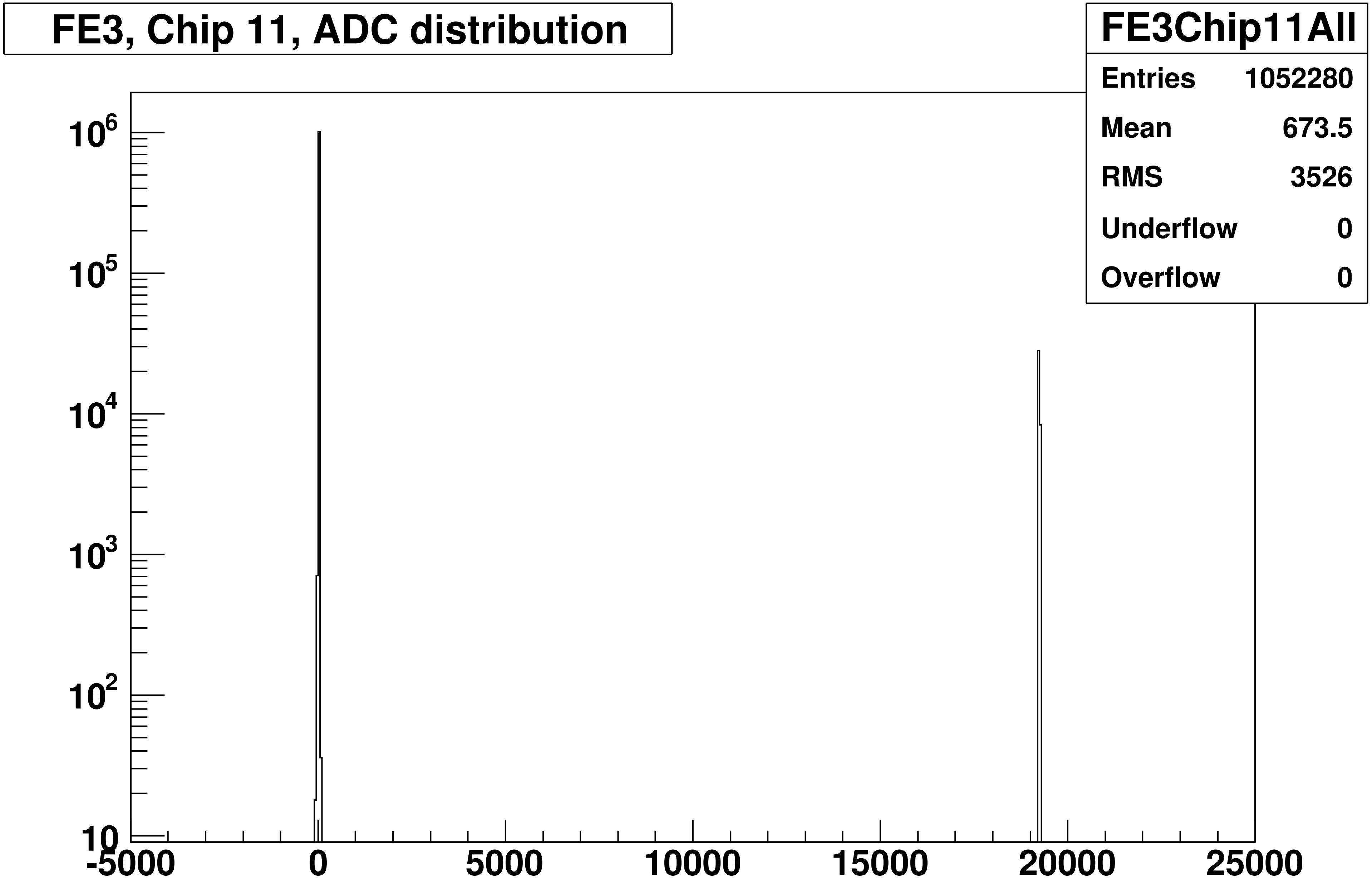

FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 1052280
Mean 673.5
RMS 3526
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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-5000
0
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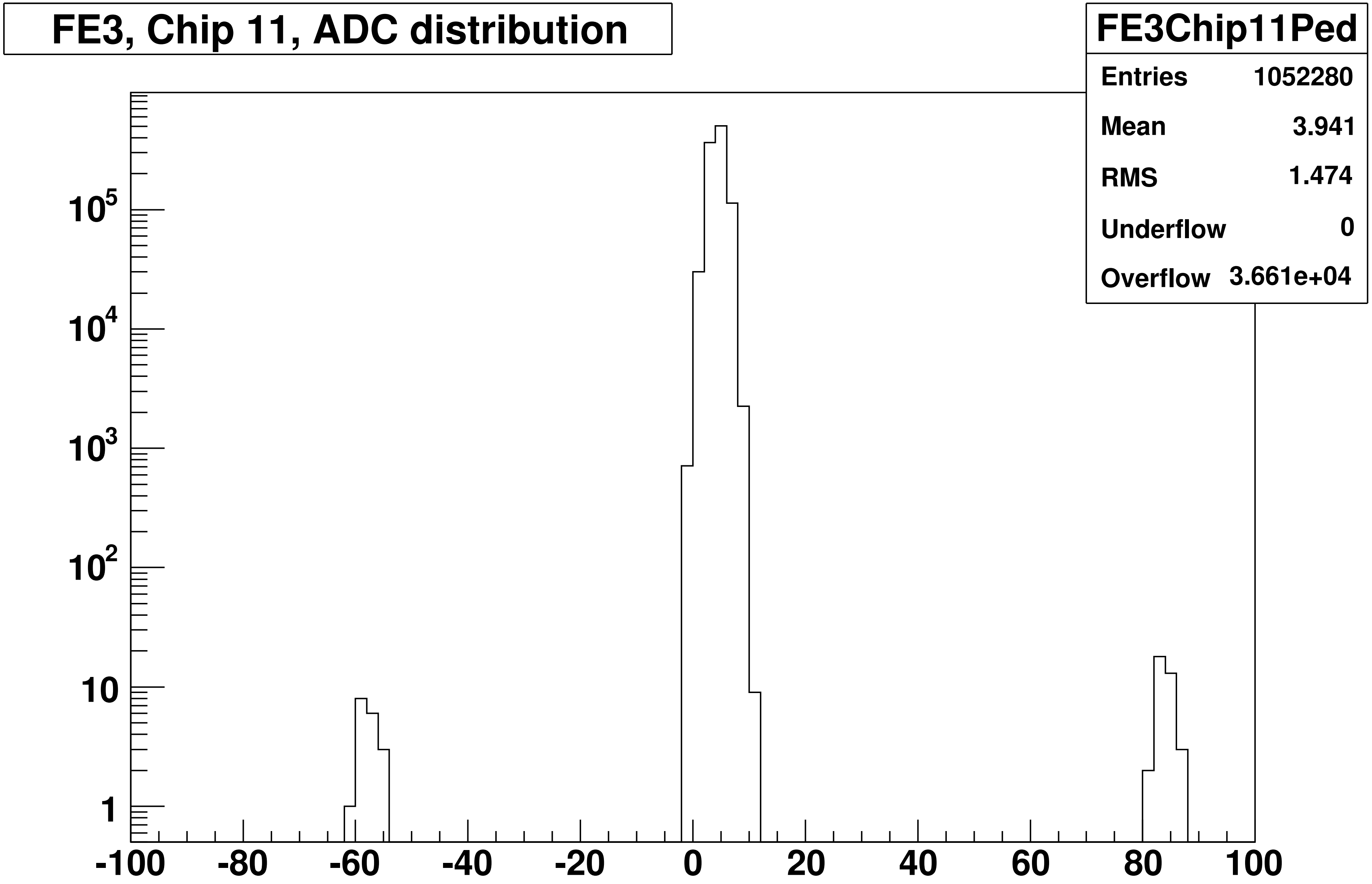
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 1052280
Mean 3.941
RMS 1.474
Underflow 0
Overflow 3.661e+04
10^5
10^4
10^3
10^2
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1
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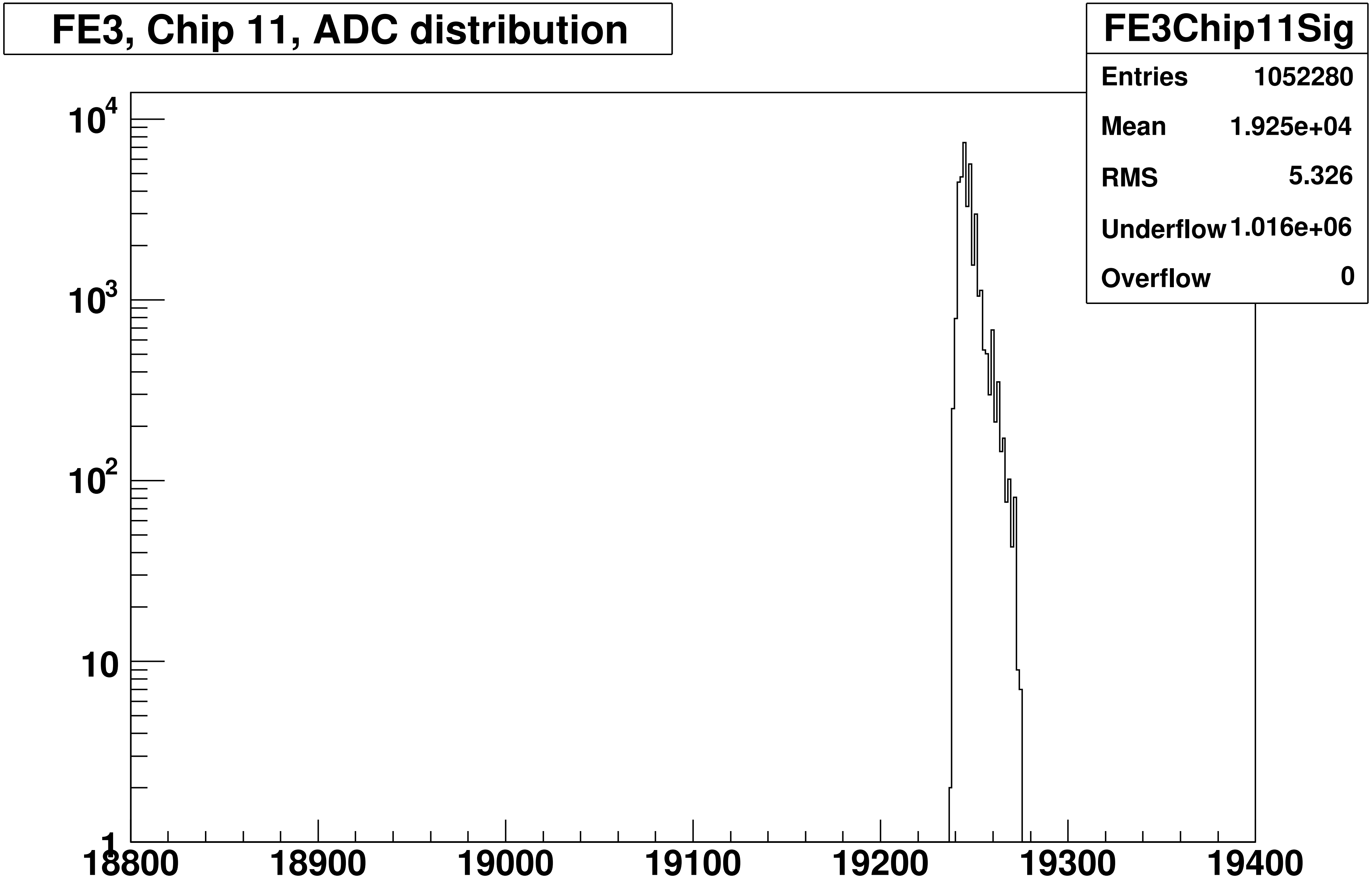

FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 1052280
Mean 1.925e+04
RMS 5.326
Underflow 1.016e+06
Overflow 0
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10^3
10^2
10
1
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18900
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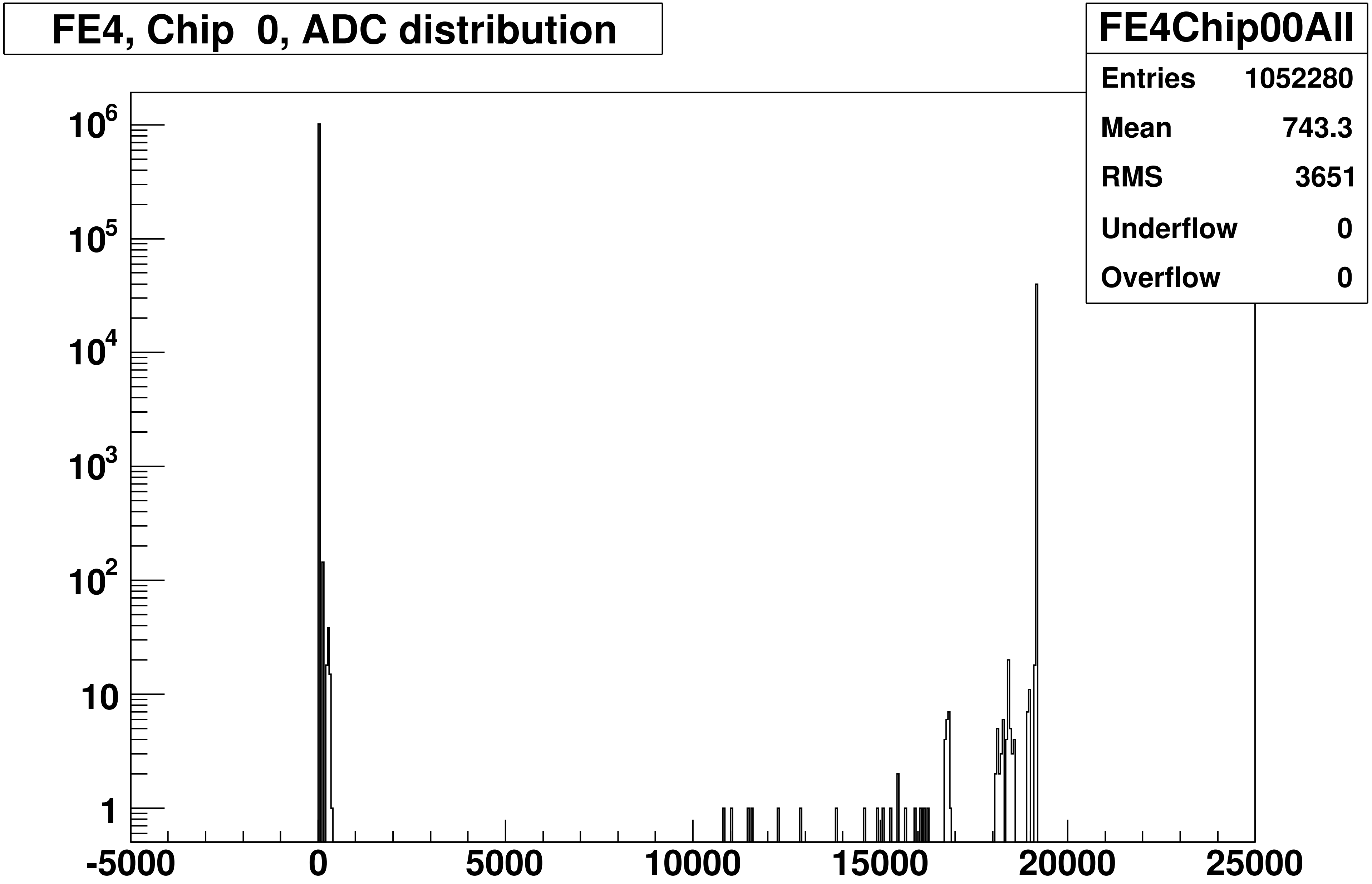

FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 1052280
Mean 743.3
RMS 3651
Underflow 0
Overflow 0
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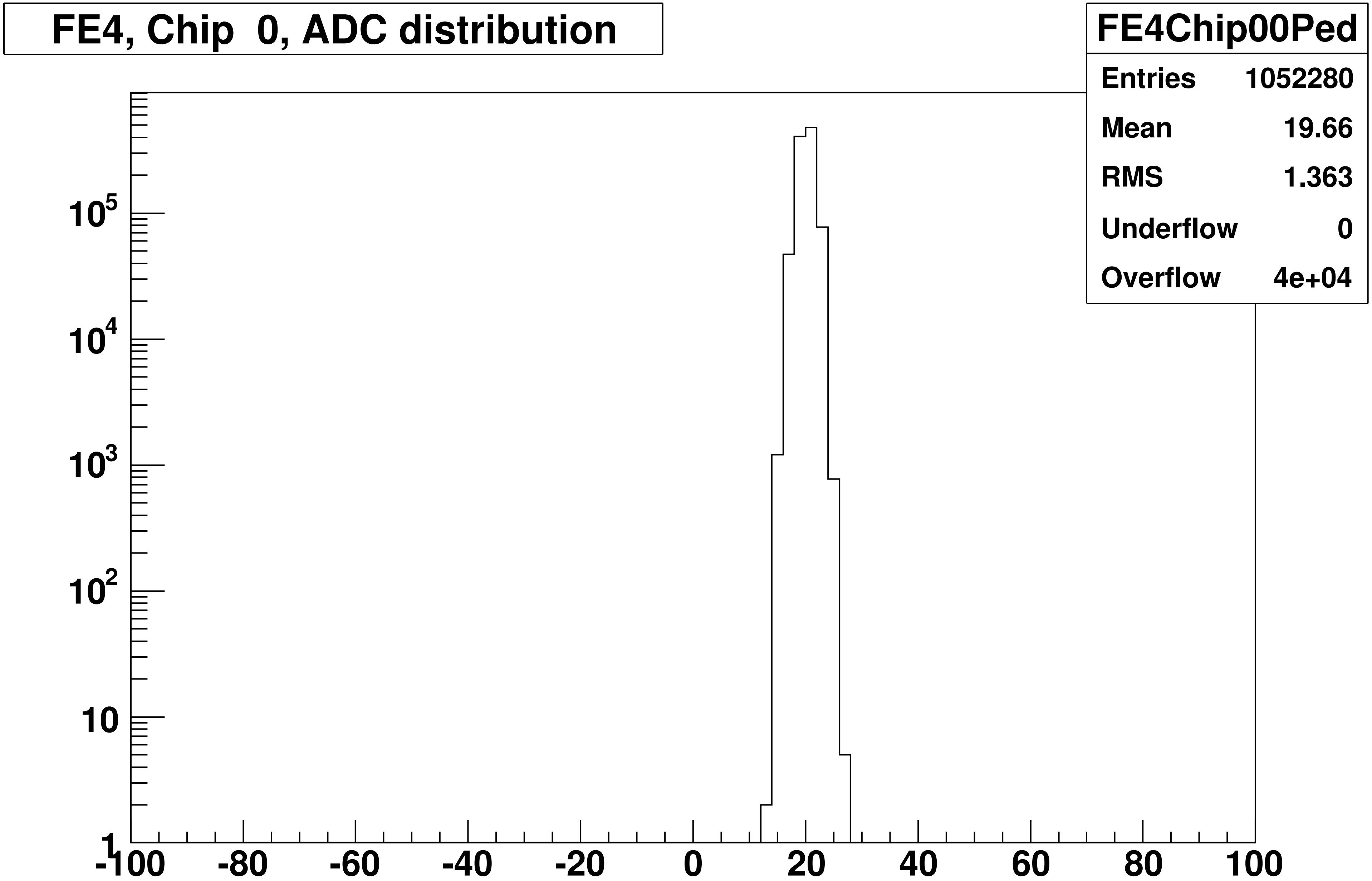
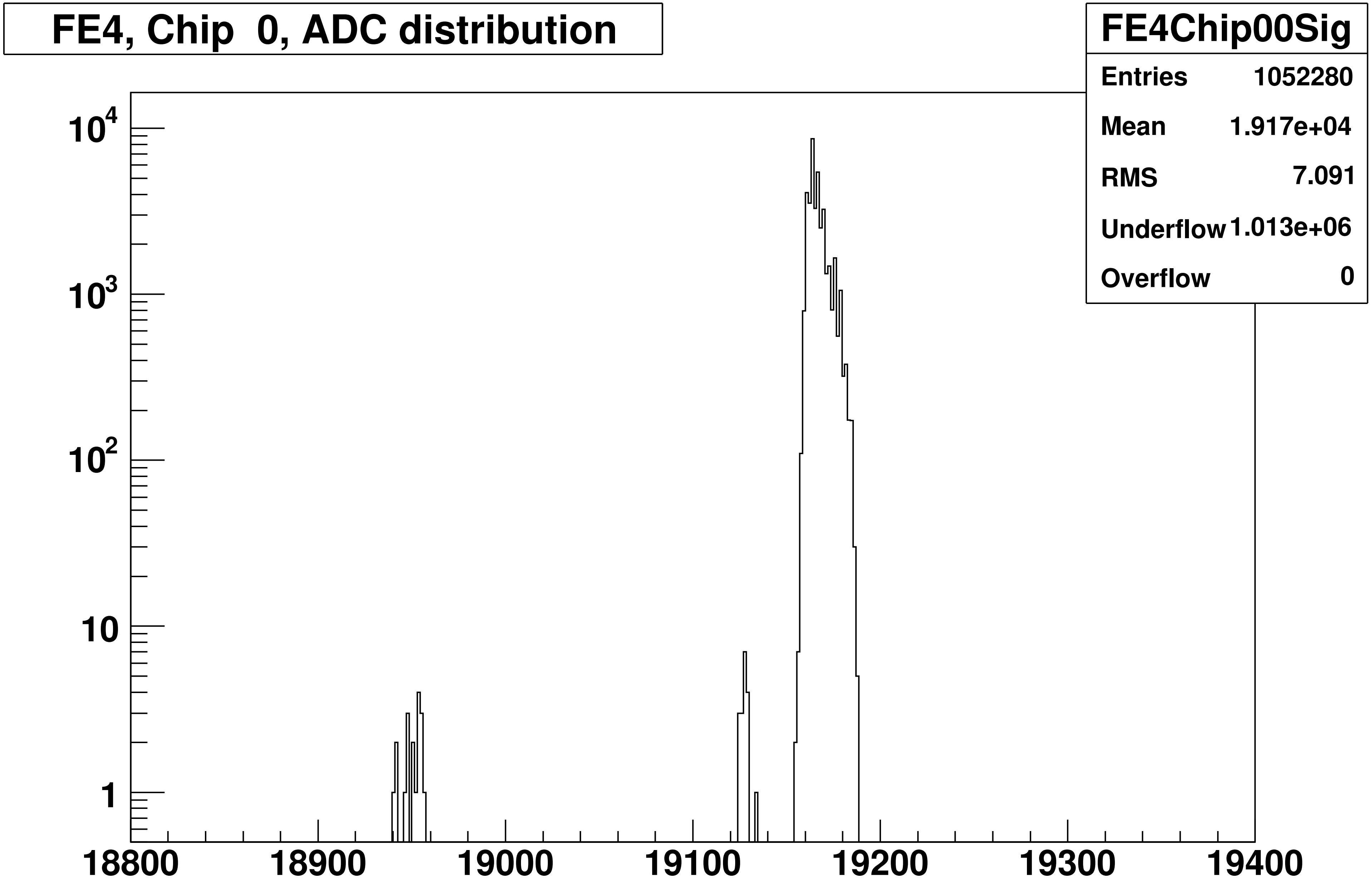
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 1052280
Mean 19.66
RMS 1.363
Underflow 0
Overflow 4e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 1052280
Mean 1.917e+04
RMS 7.091
Underflow 1.013e+06
Overflow 0
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10^3
10^2
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1
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18900
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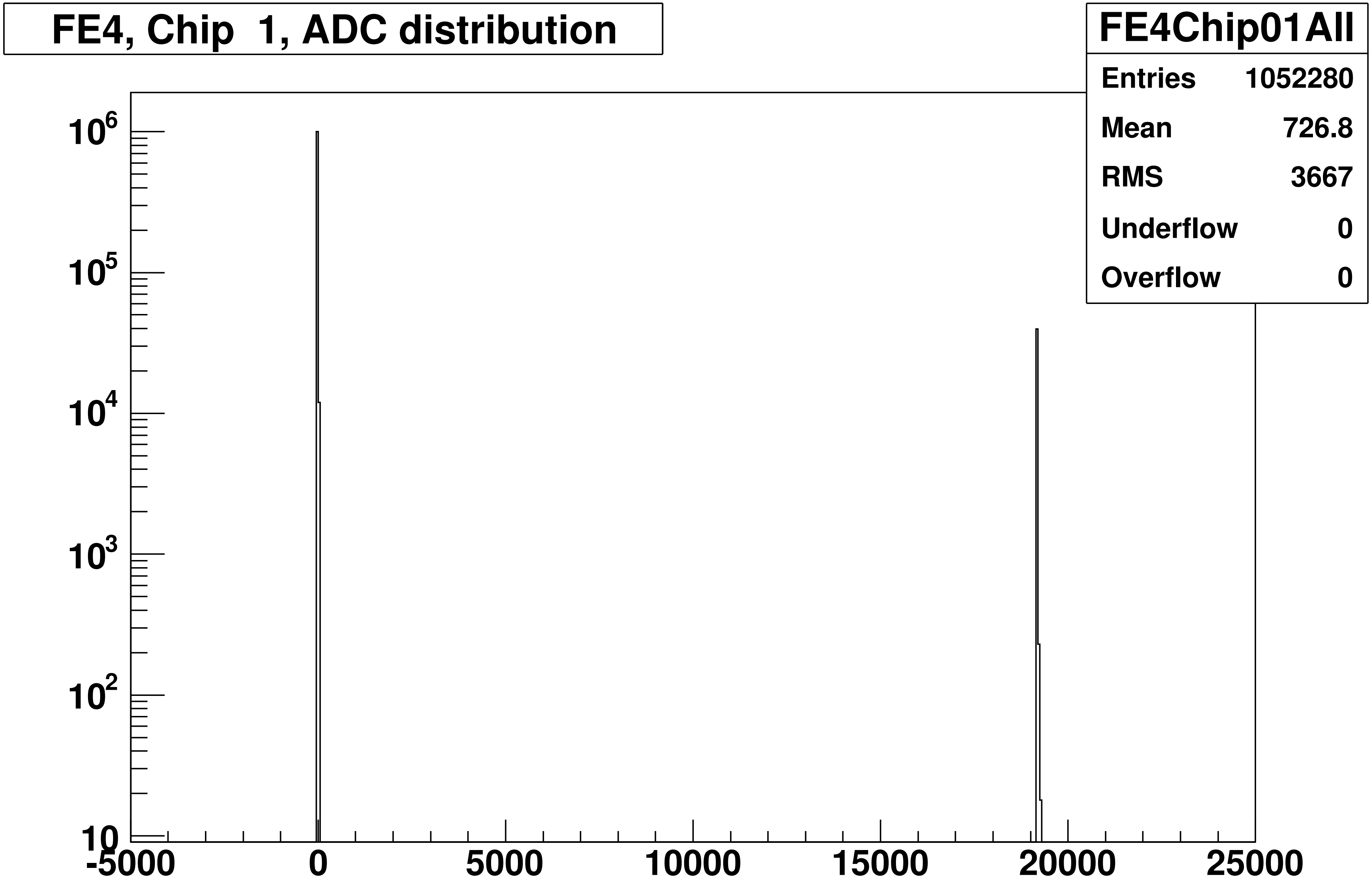
FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 1052280
Mean 726.8
RMS 3667
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
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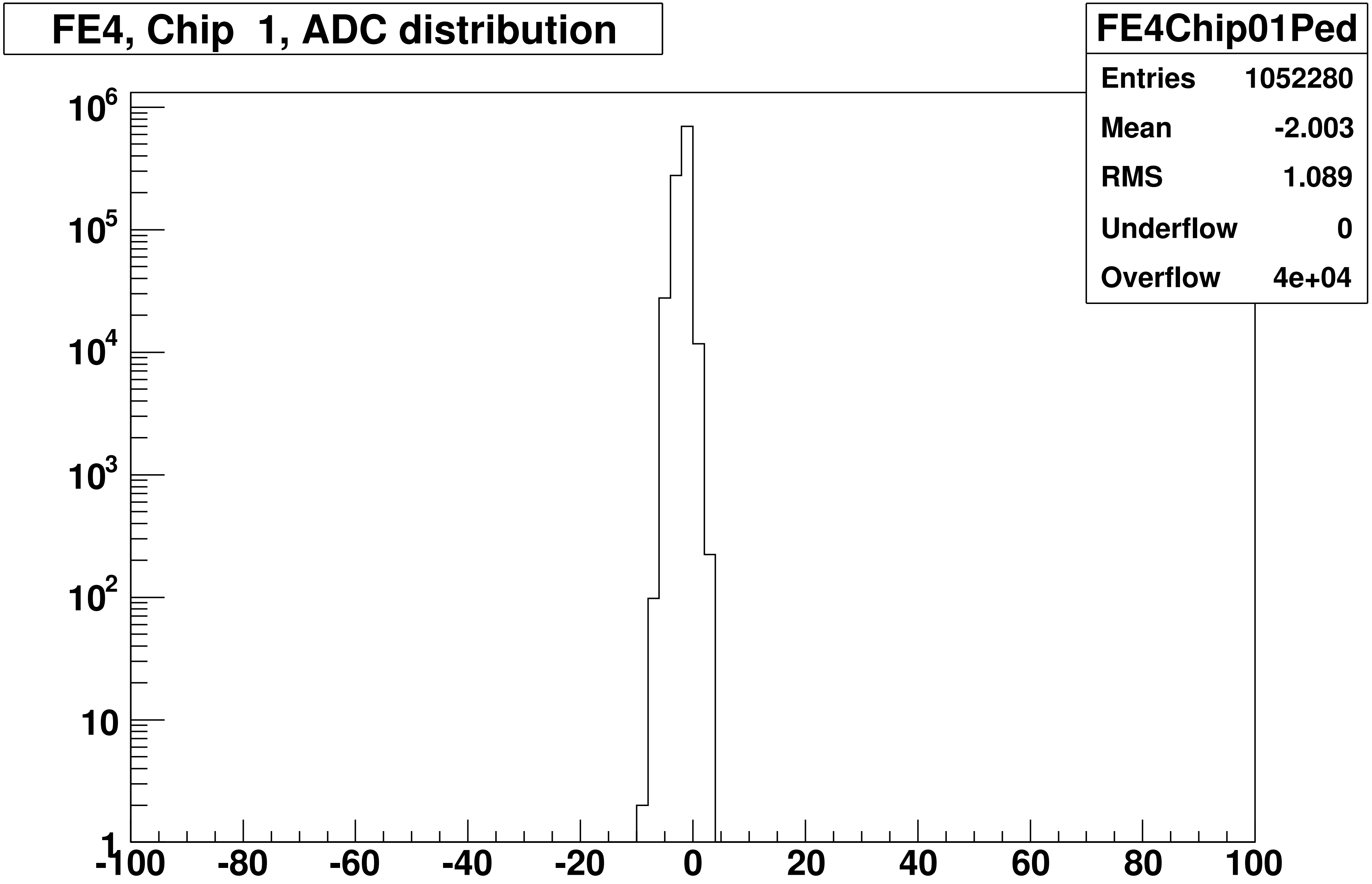
20000
25000


FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 1052280
Mean -2.003
RMS 1.089
Underflow 0
Overflow 4e+04
10^6
10^5
10^4
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10^2
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-20
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80
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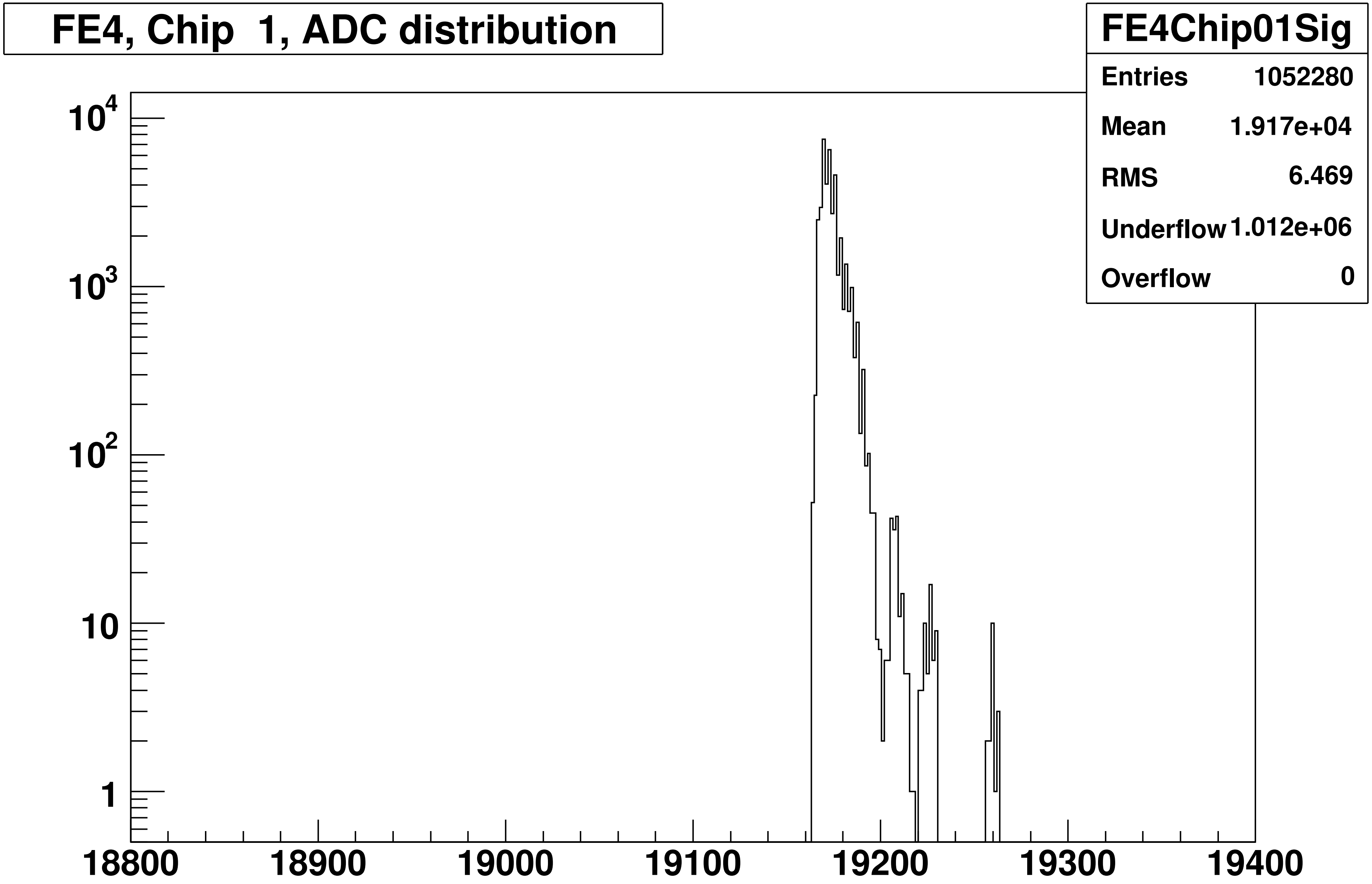
FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 1052280
Mean 1.917e+04
RMS 6.469
Underflow 1.012e+06
Overflow 0
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10^3
10^2
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18900
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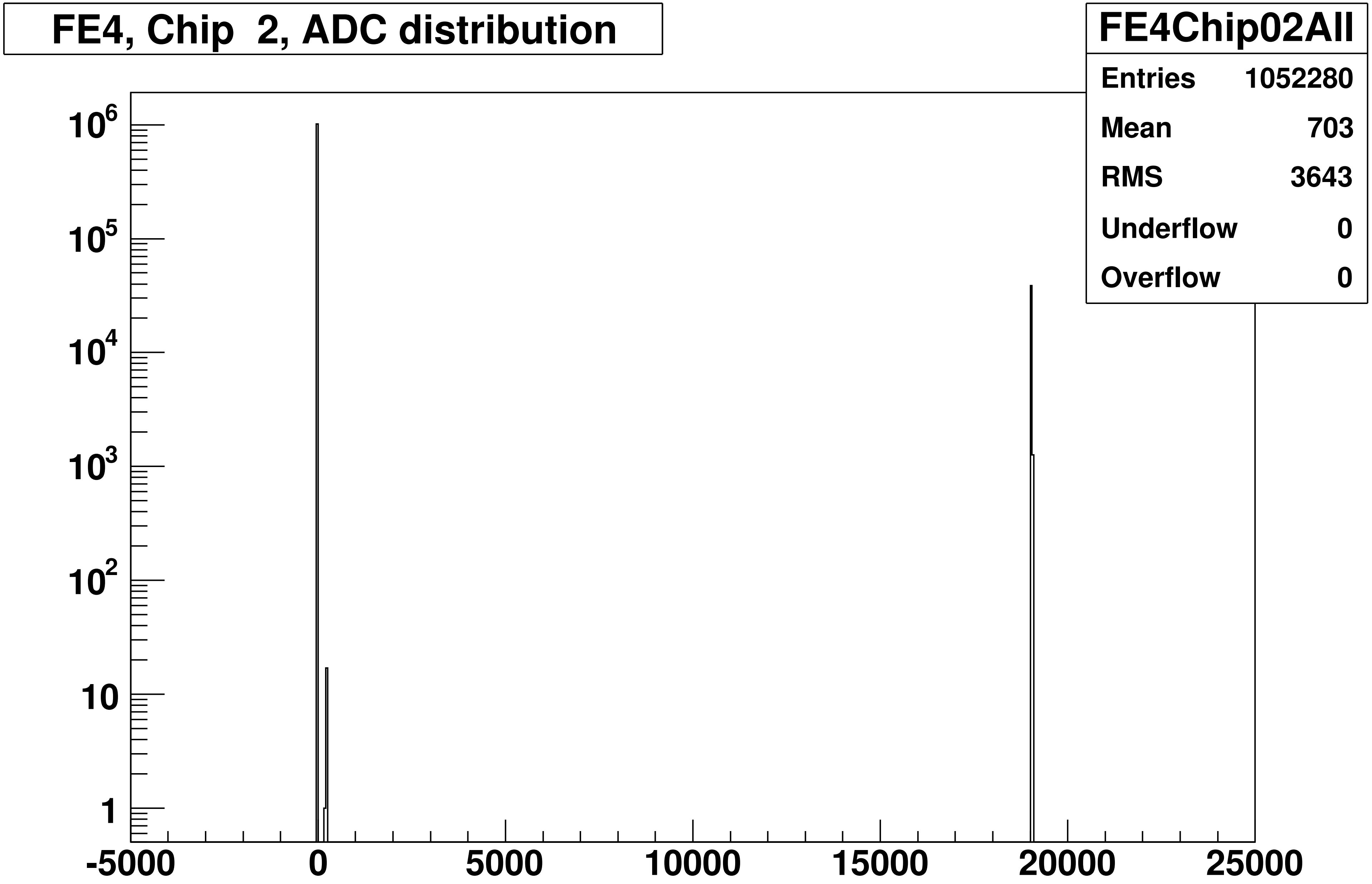
FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 1052280
Mean 703
RMS 3643
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
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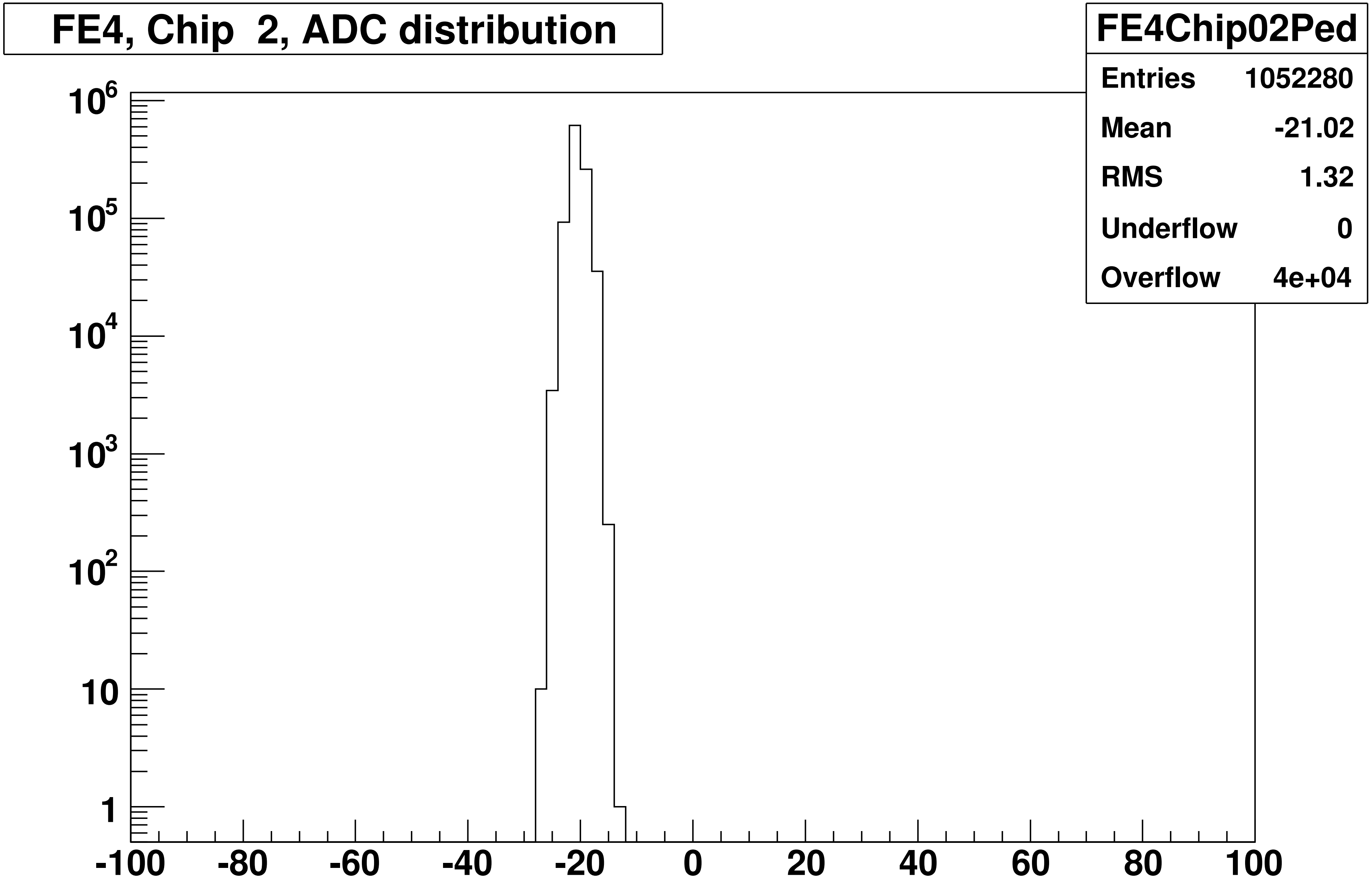

FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 1052280
Mean -21.02
RMS 1.32
Underflow 0
Overflow 4e+04
10^6
10^5
10^4
10^3
10^2
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1
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-20
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60
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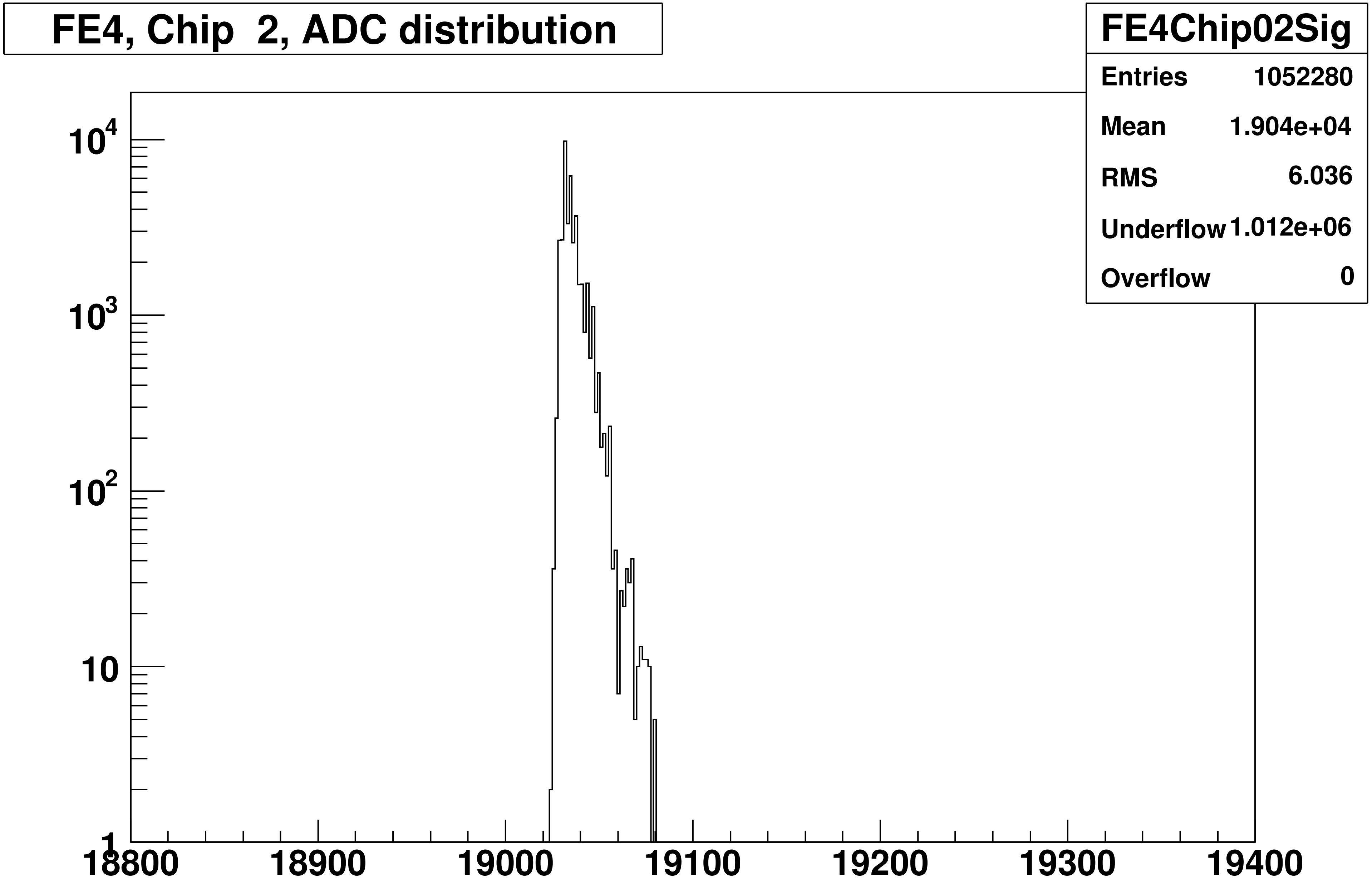
100


FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 1052280
Mean 1.904e+04
RMS 6.036
Underflow 1.012e+06
Overflow 0
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10^3
10^2
10
1
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18900
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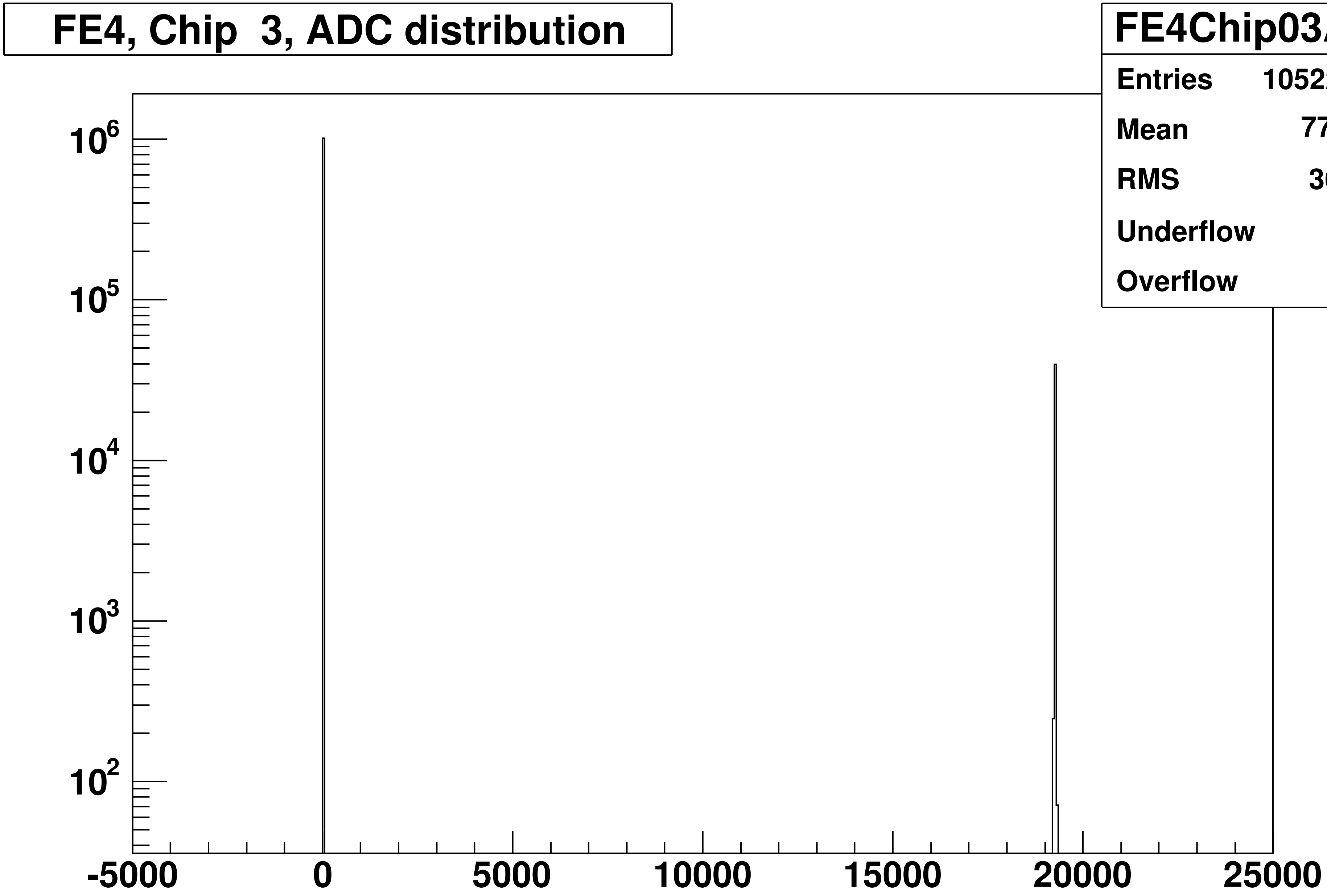

FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 1052280
Mean 772.7
RMS 3674
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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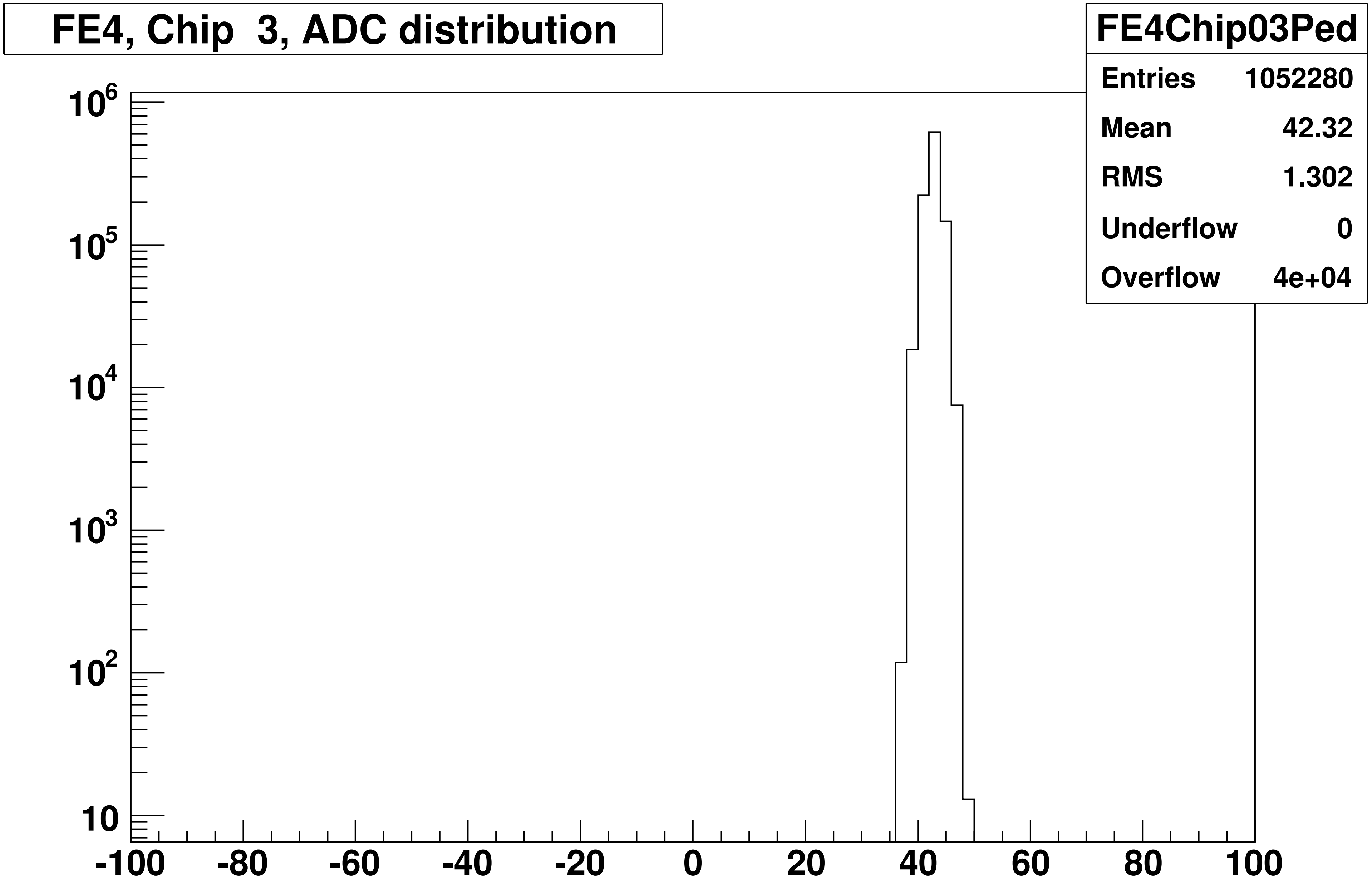

FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 1052280
Mean 42.32
RMS 1.302
Underflow 0
Overflow 4e+04
10^6
10^5
10^4
10^3
10^2
10
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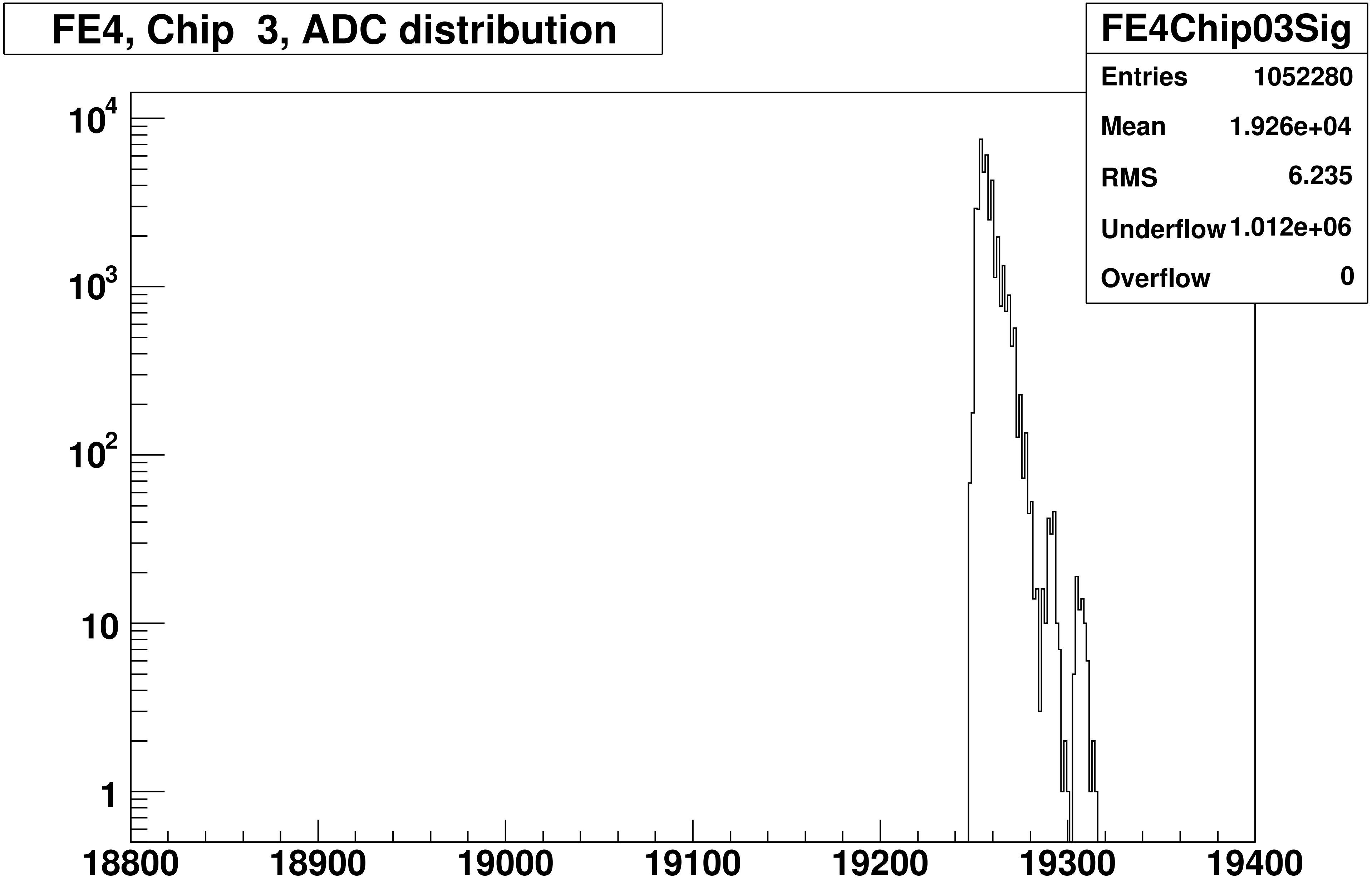

FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 1052280
Mean 1.926e+04
RMS 6.235
Underflow 1.012e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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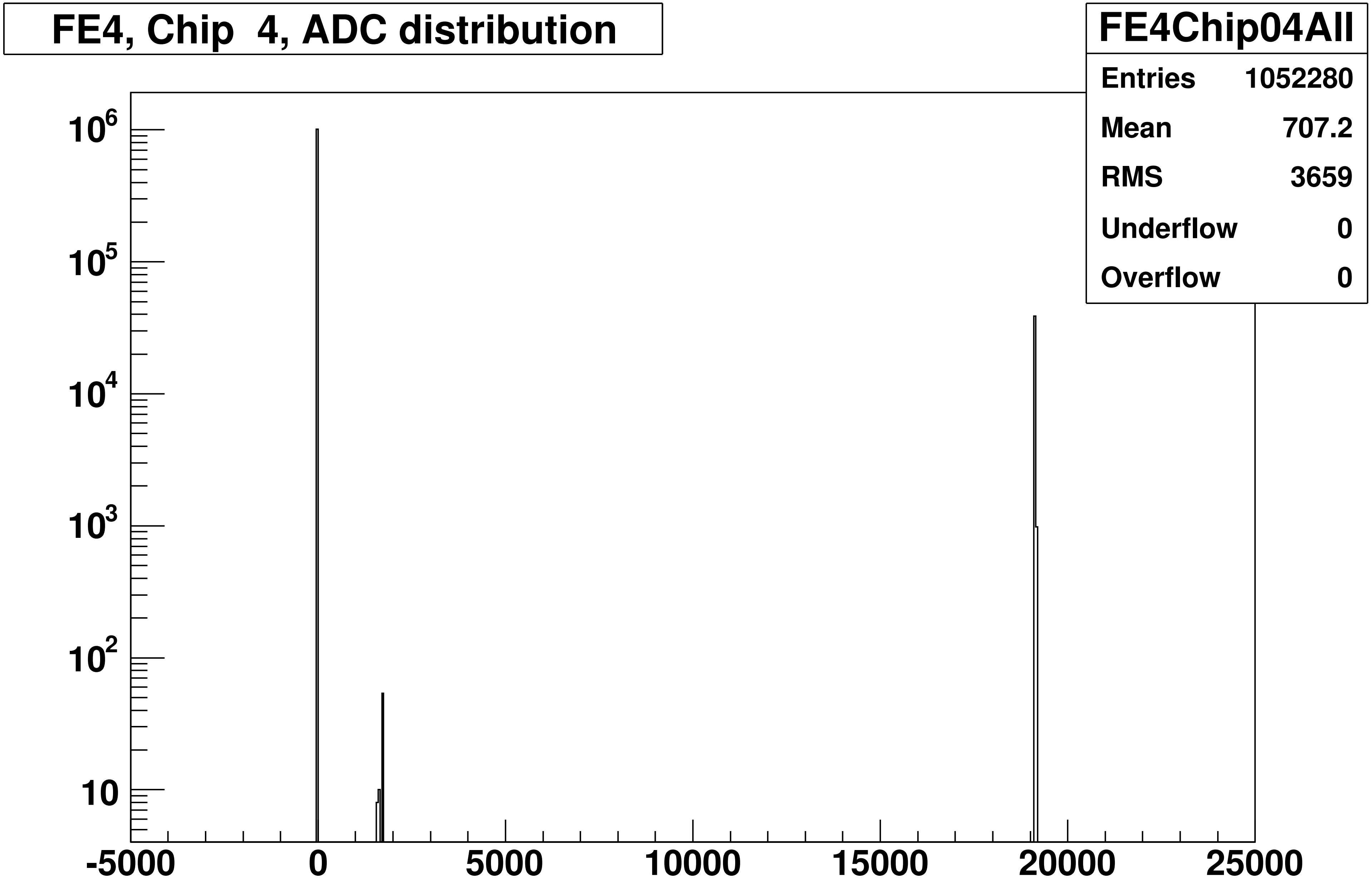
19400



FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 1052280
Mean 707.2
RMS 3659
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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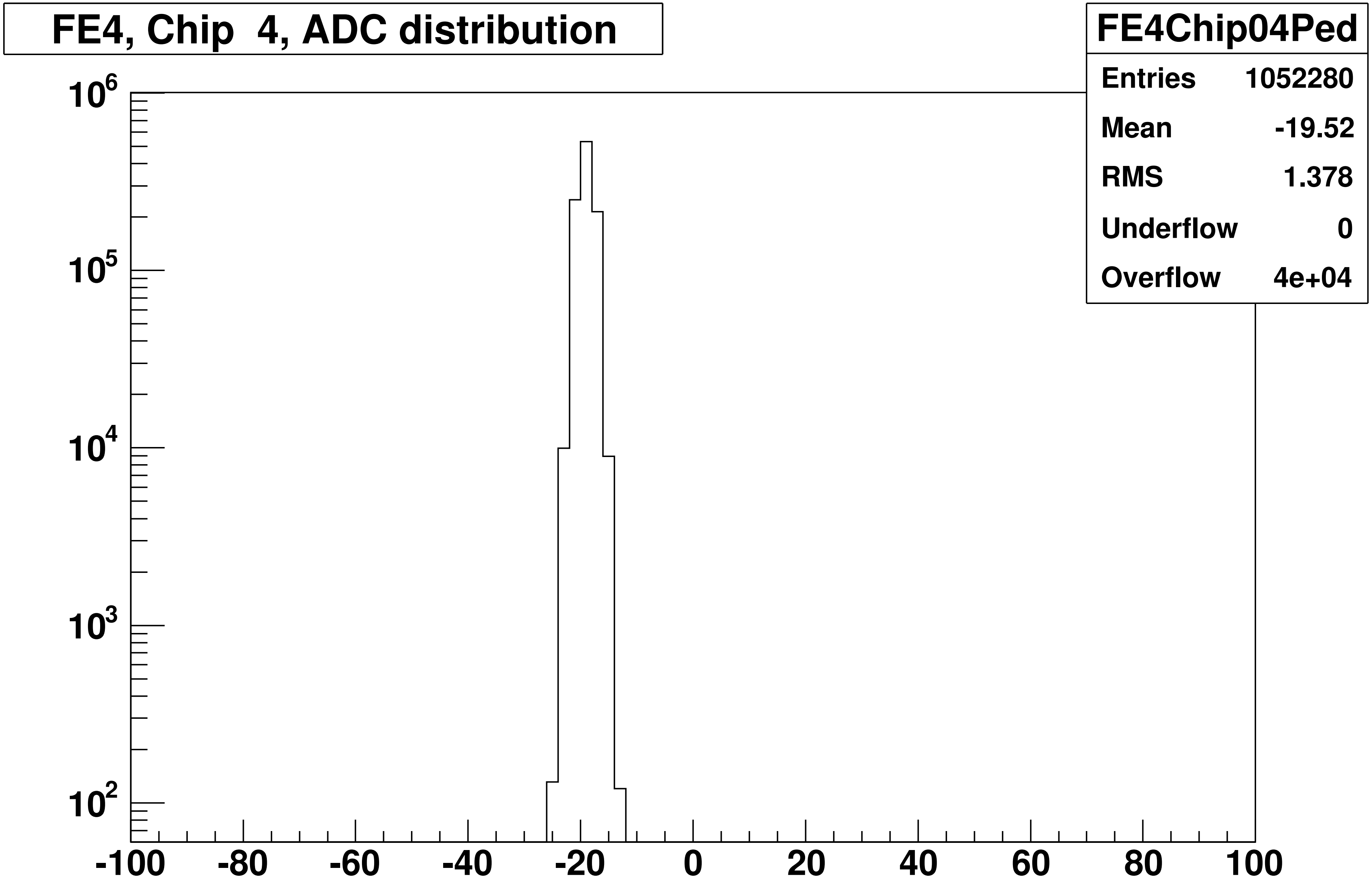
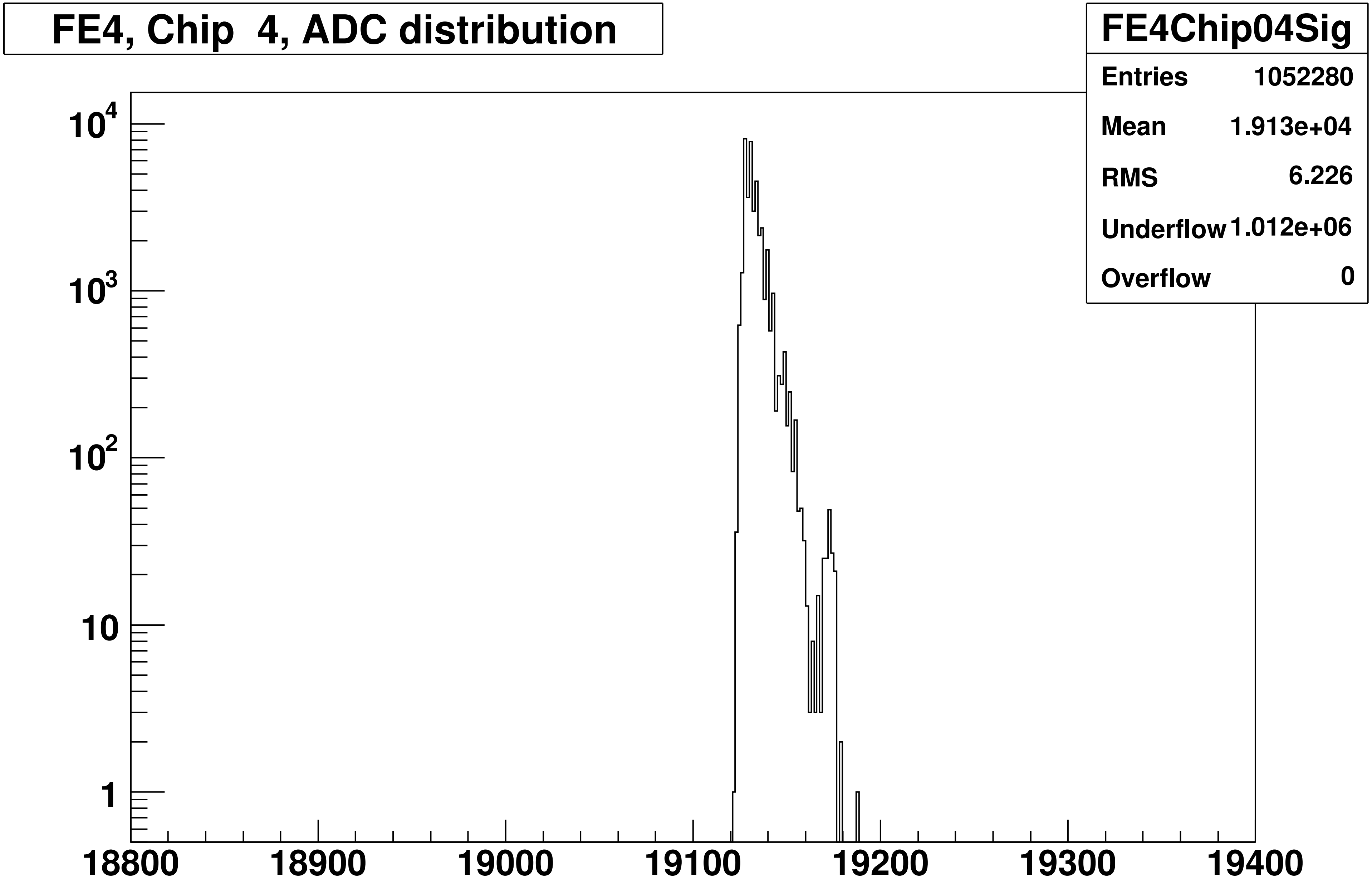

FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 1052280
Mean -19.52
RMS 1.378
Underflow 0
Overflow 4e+04
10^6
10^5
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 1052280
Mean 1.913e+04
RMS 6.226
Underflow 1.012e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
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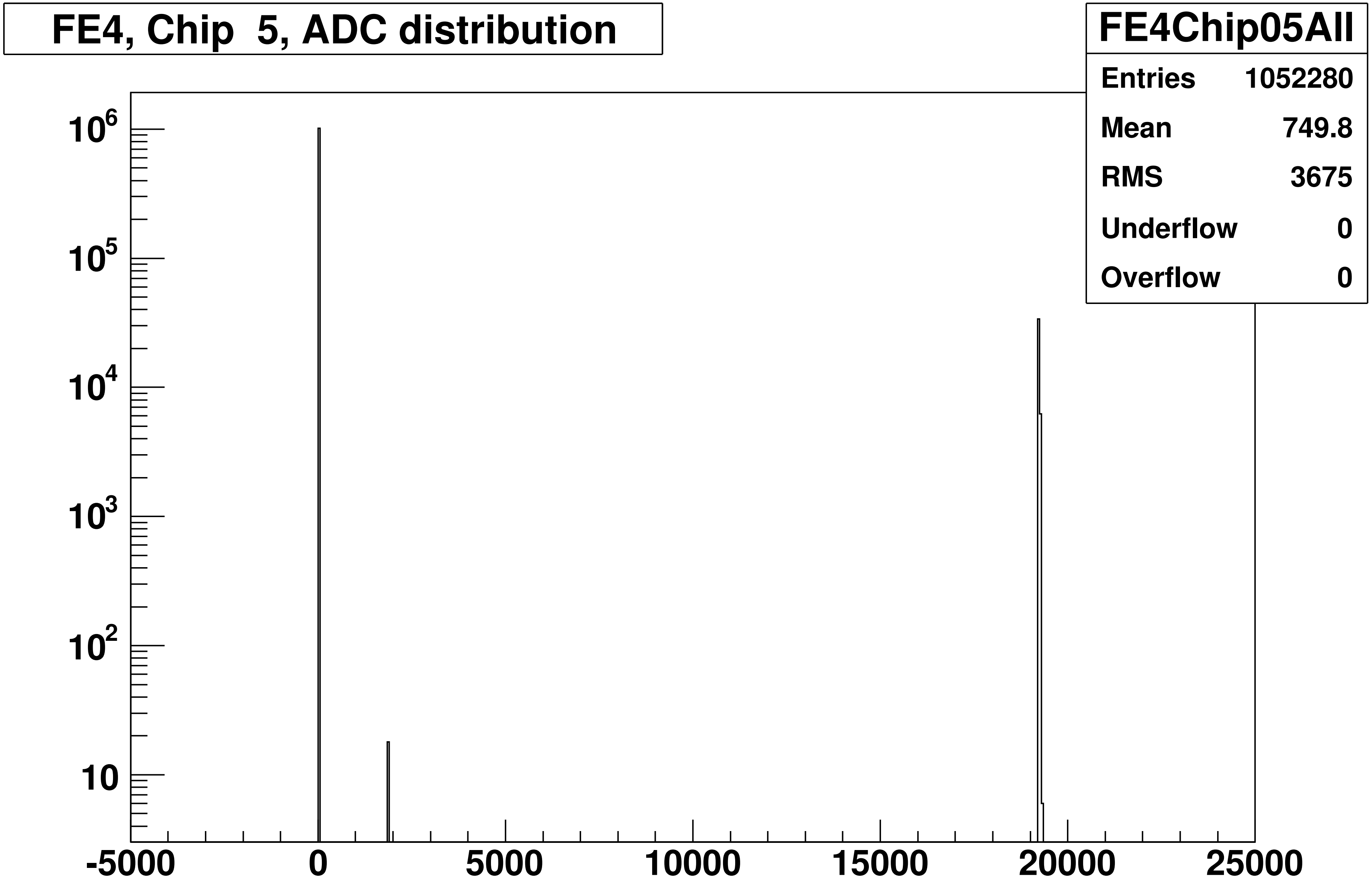
19400



FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 1052280
Mean 749.8
RMS 3675
Underflow 0
Overflow 0
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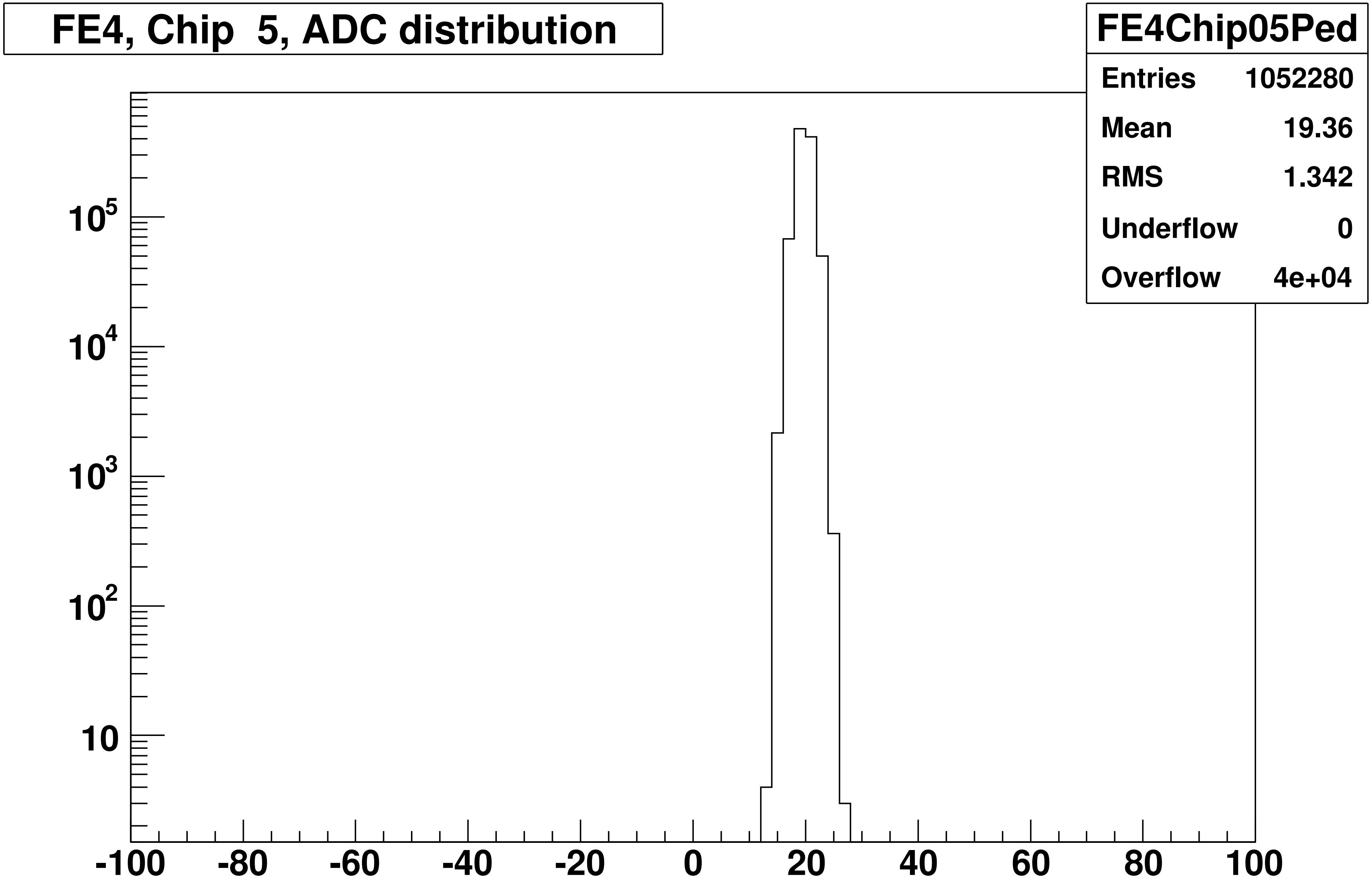
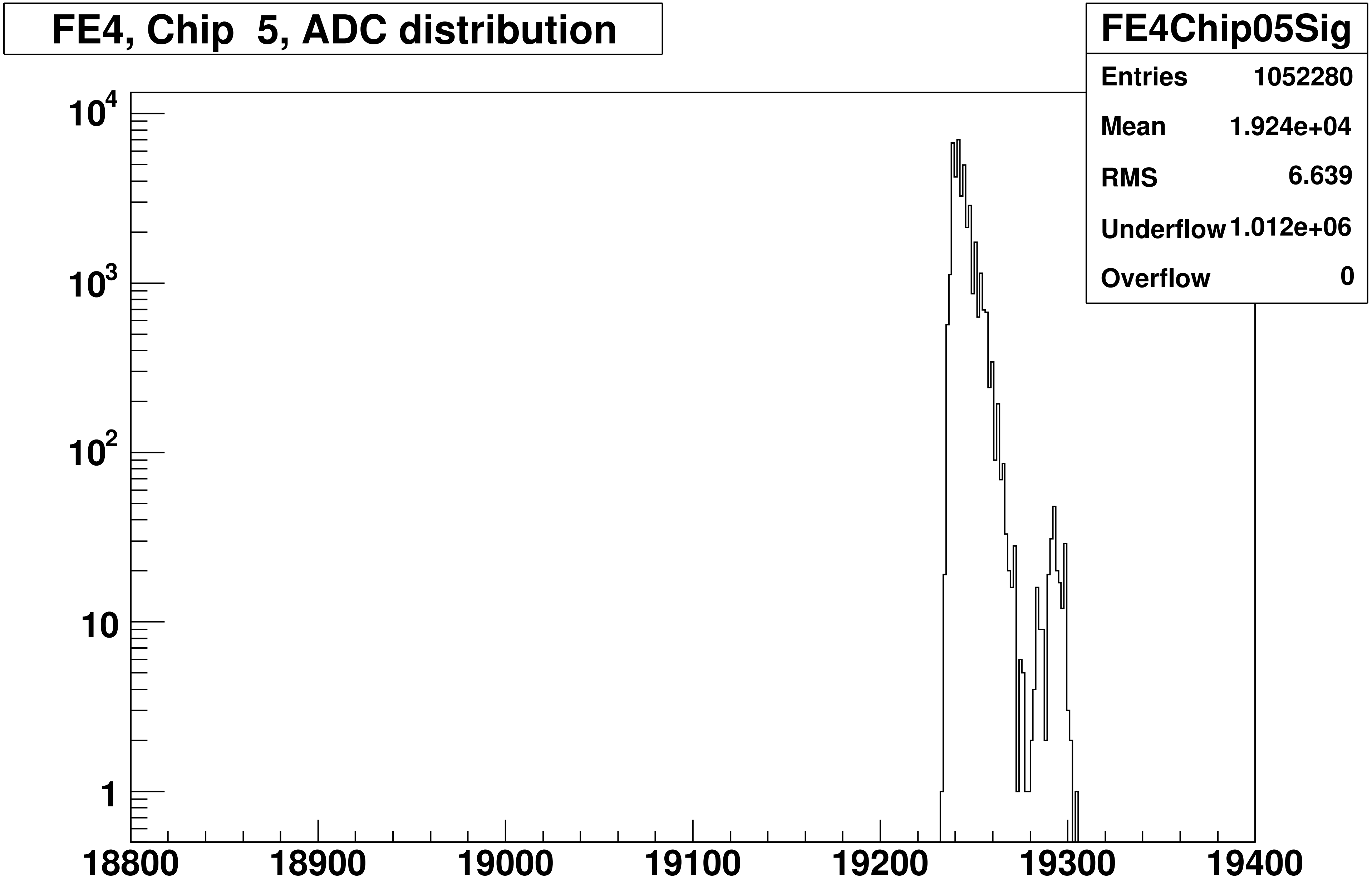
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 1052280
Mean 19.36
RMS 1.342
Underflow 0
Overflow 4e+04
10^5
10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 1052280
Mean 1.924e+04
RMS 6.639
Underflow 1.012e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
19000
19100
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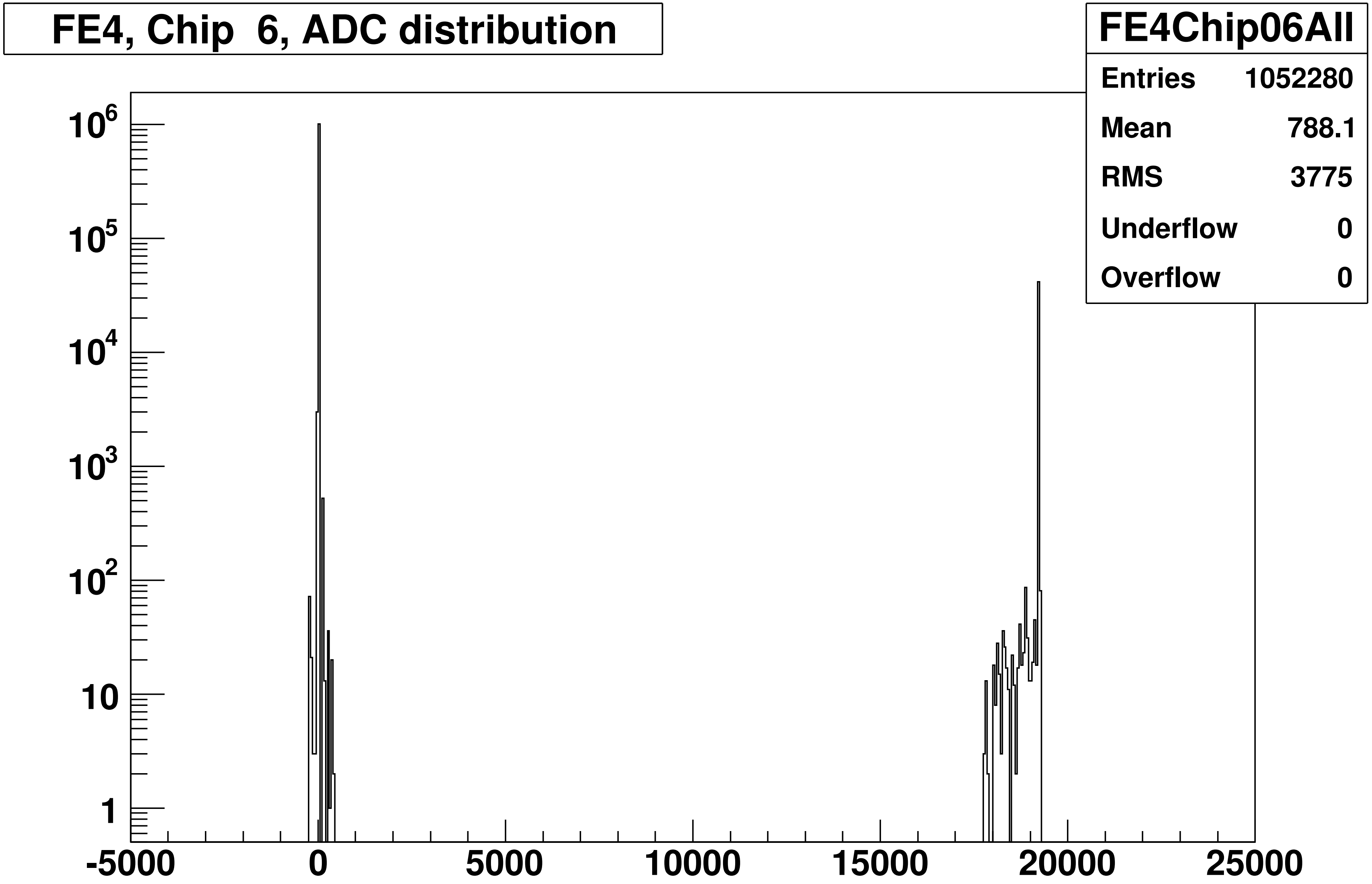
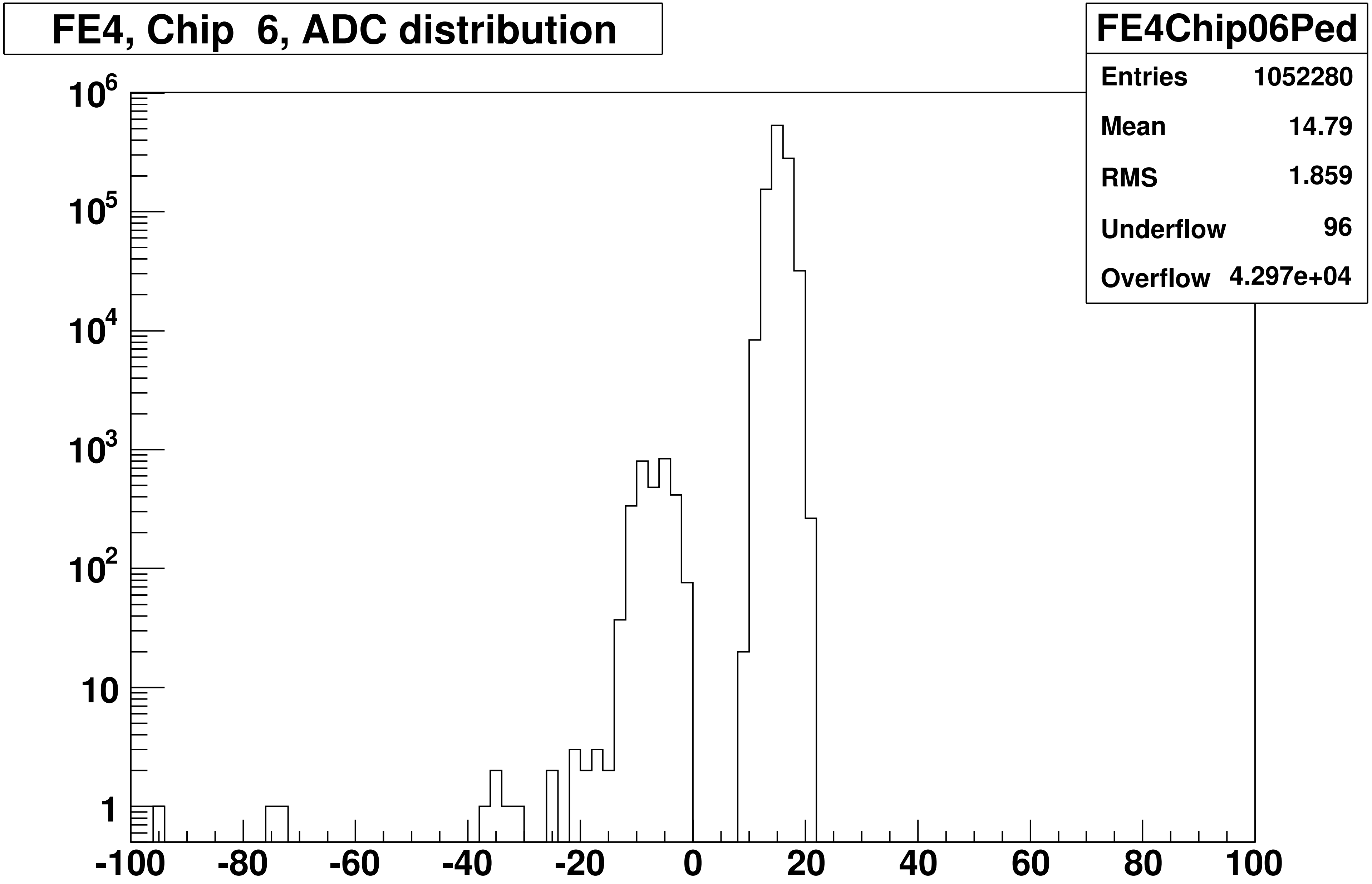
19300
19400


FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 1052280
Mean 788.1
RMS 3775
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 1052280
Mean 14.79
RMS 1.859
Underflow 96
Overflow 4.297e+04
10^6
10^5
10^4
10^3
10^2
10
1
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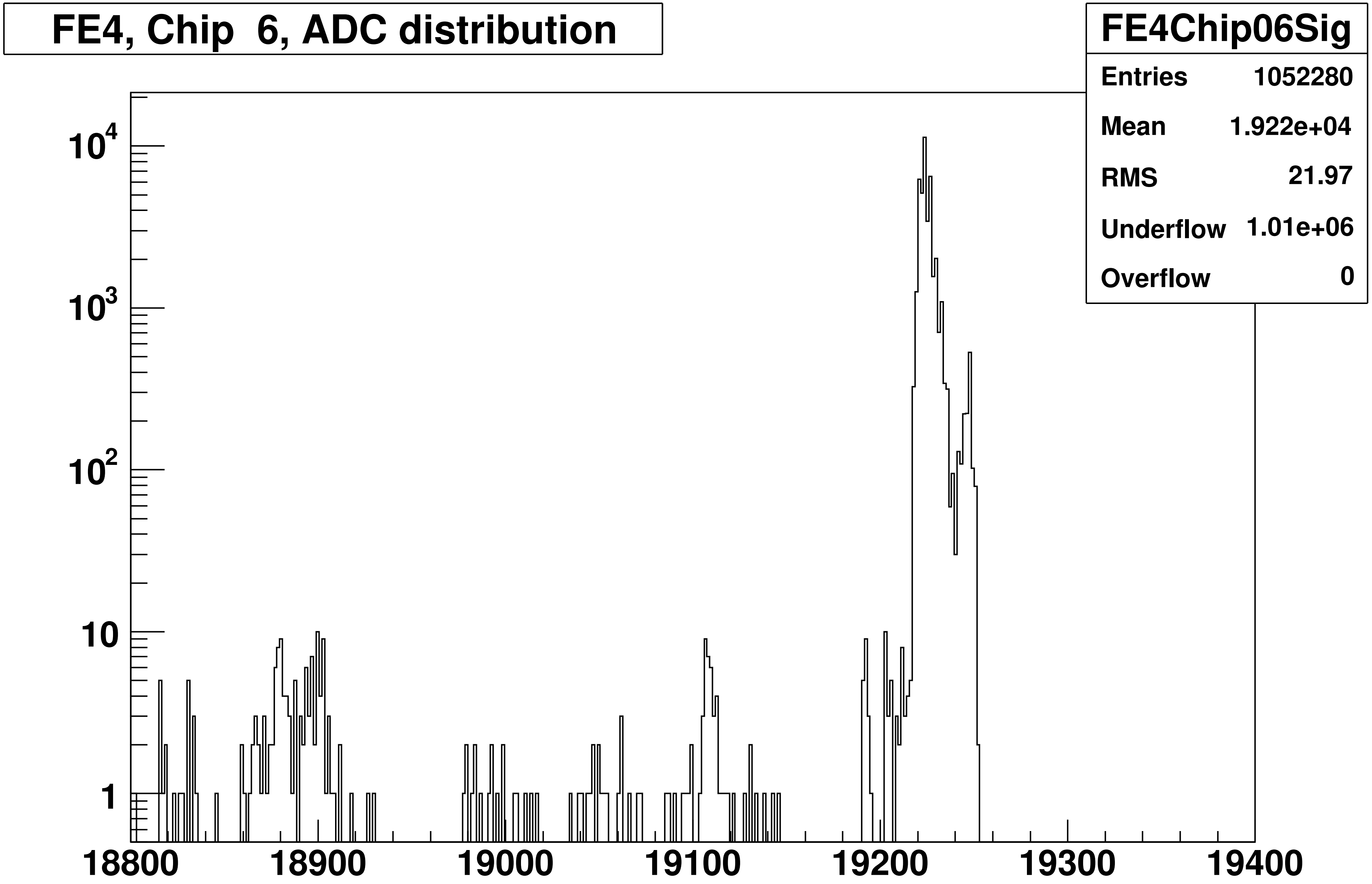
-40
-20
0
20
40
60
80
100



FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 1052280
Mean 1.922e+04
RMS 21.97
Underflow 1.01e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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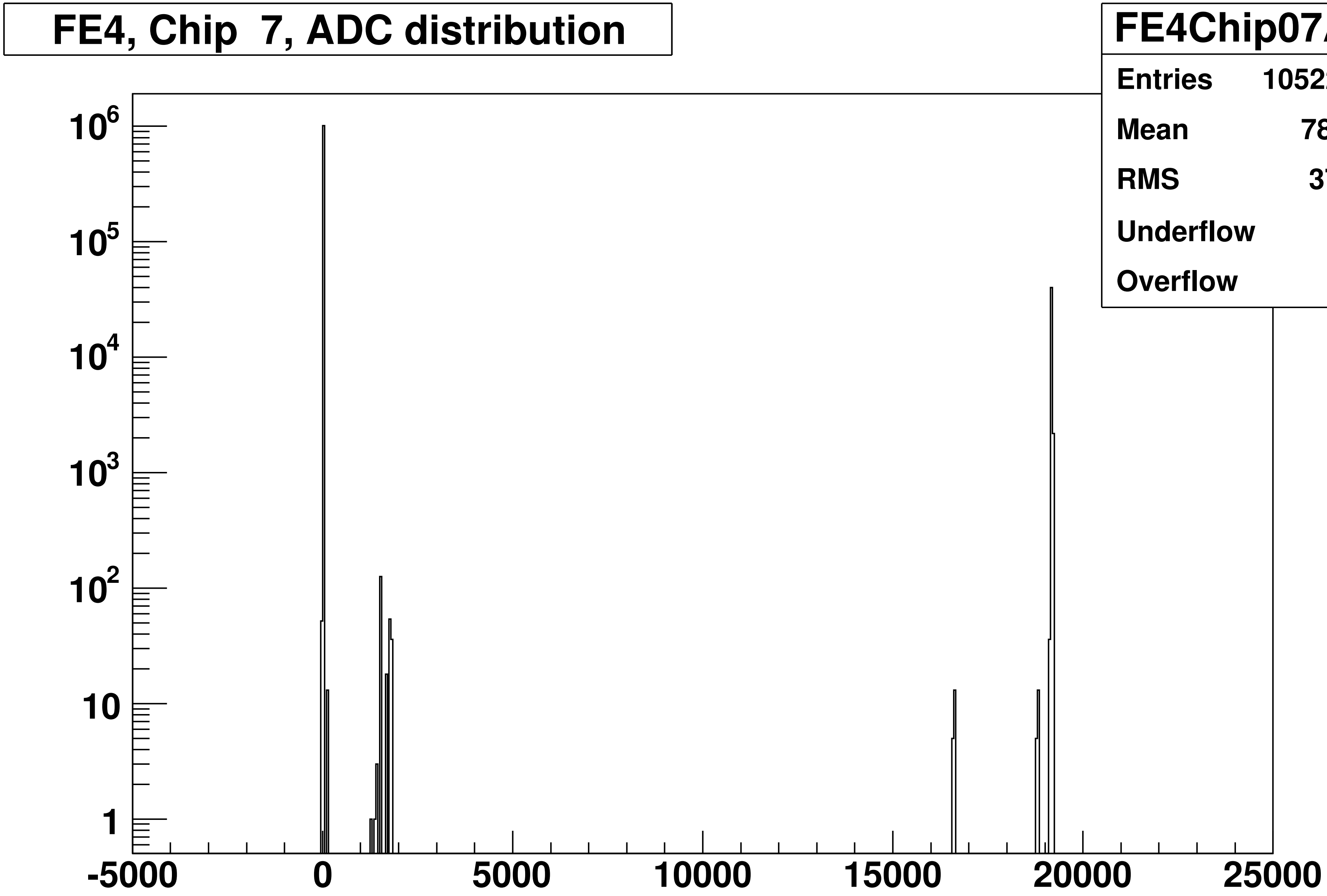
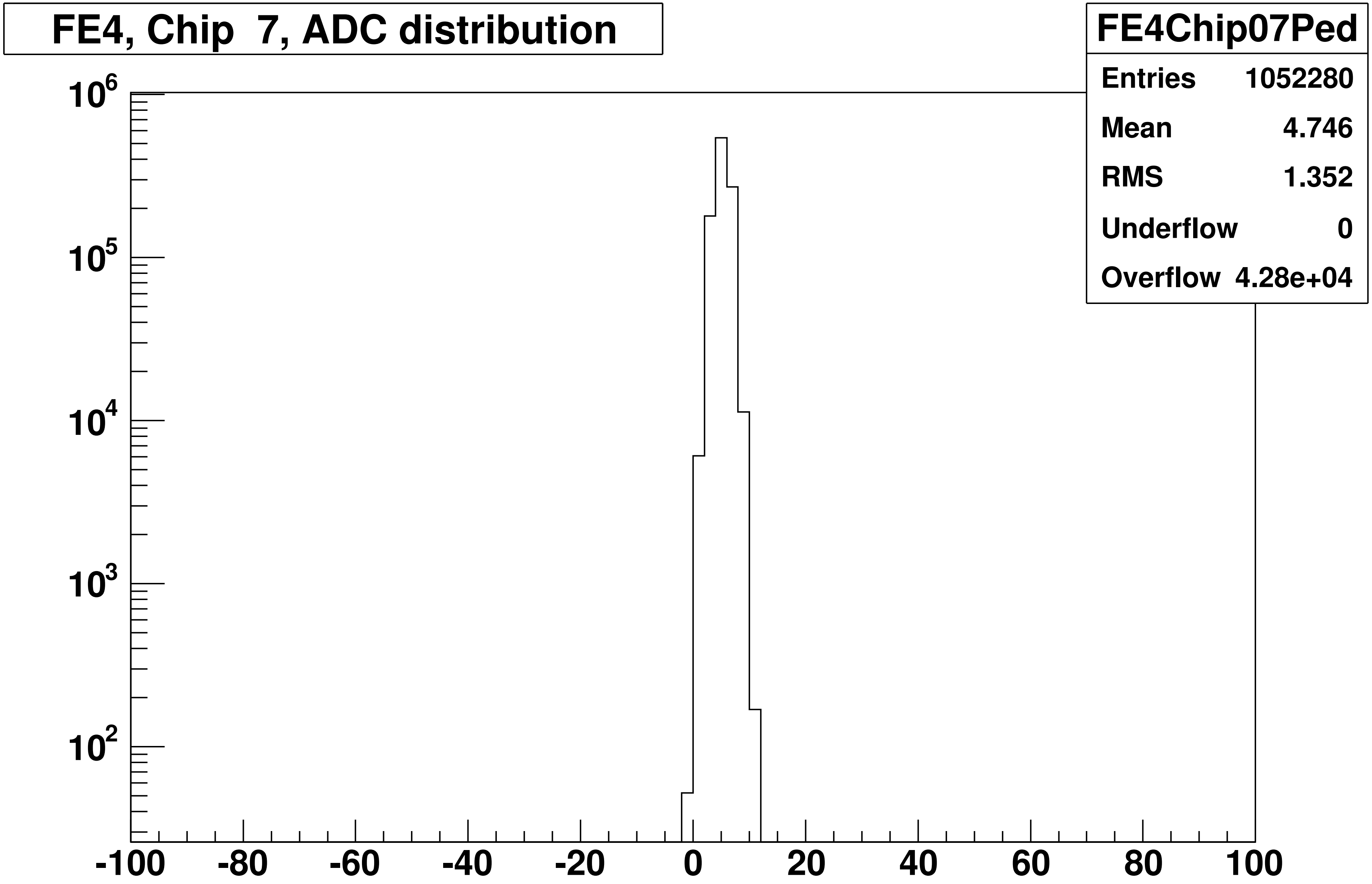

FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 1052280
Mean 780.8
RMS 3779
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 1052280
Mean 4.746
RMS 1.352
Underflow 0
Overflow 4.28e+04
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10^5
10^4
10^3
10^2
-100
-80
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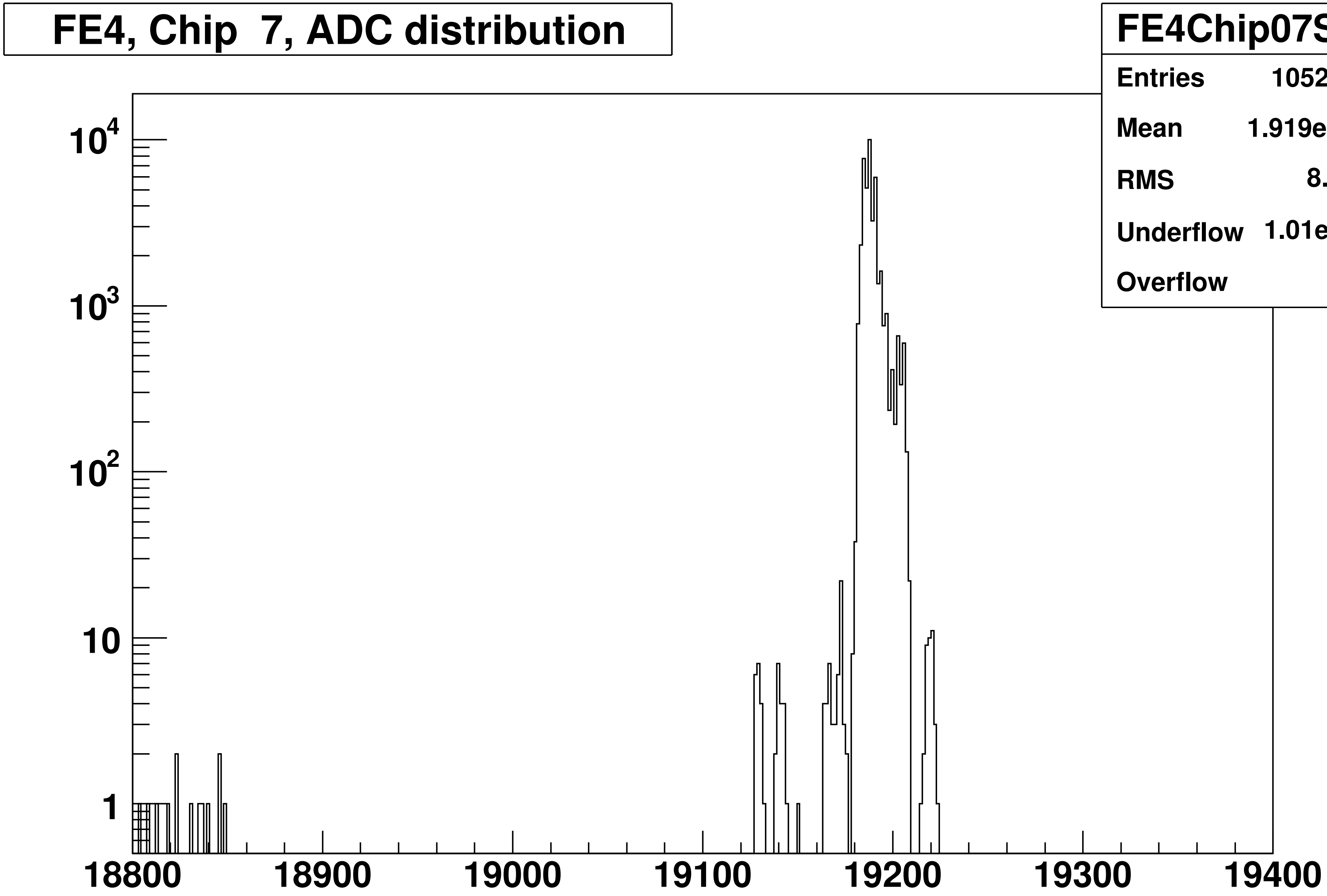
-40
-20
0
20
40
60
80
100



FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 1052280
Mean 1.919e+04
RMS 8.162
Underflow 1.01e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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19100
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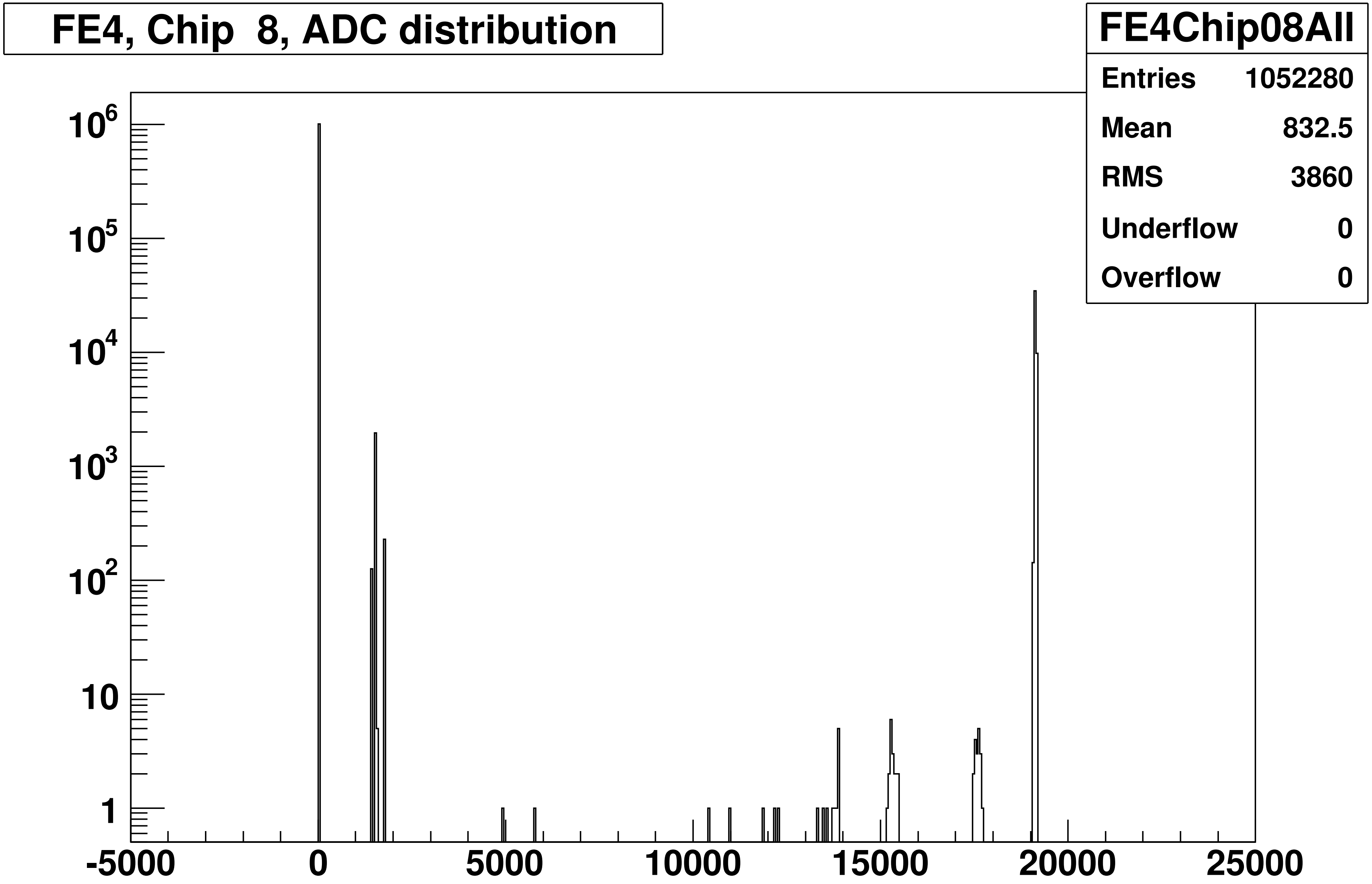
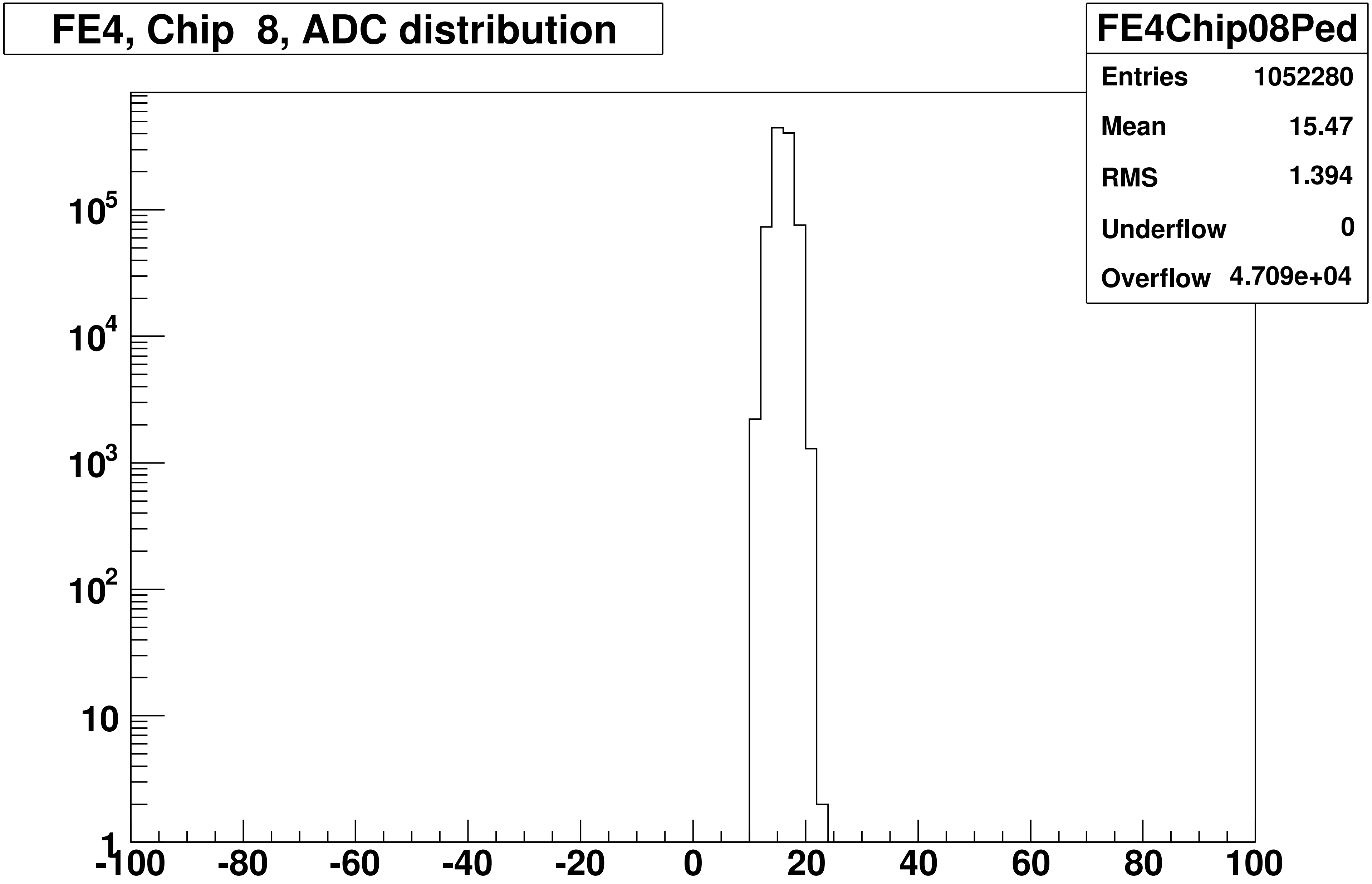
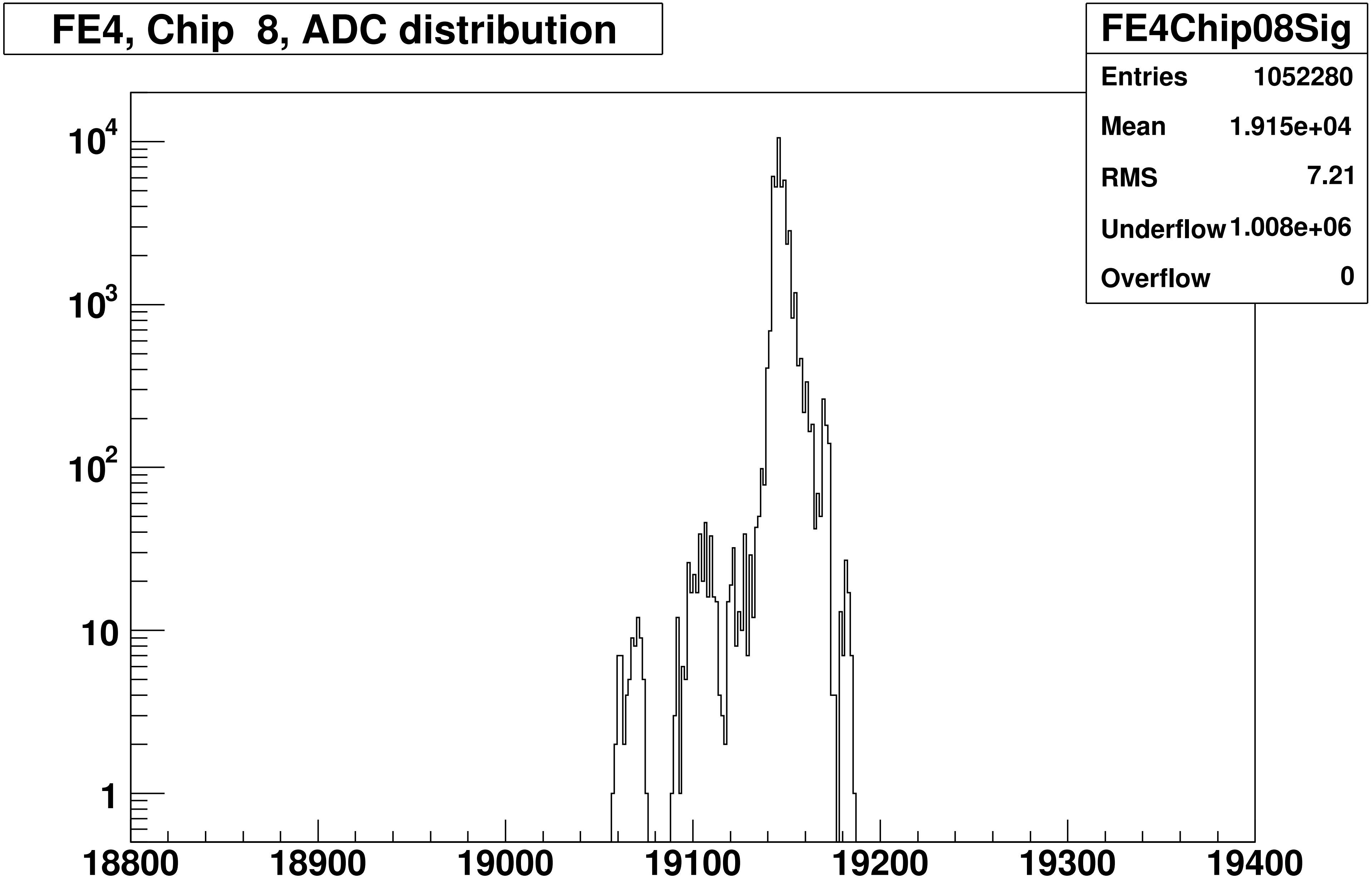


FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 1052280
Mean 832.5
RMS 3860
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 1052280
Mean 15.47
RMS 1.394
Underflow 0
Overflow 4.709e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 1052280
Mean 1.915e+04
RMS 7.21
Underflow 1.008e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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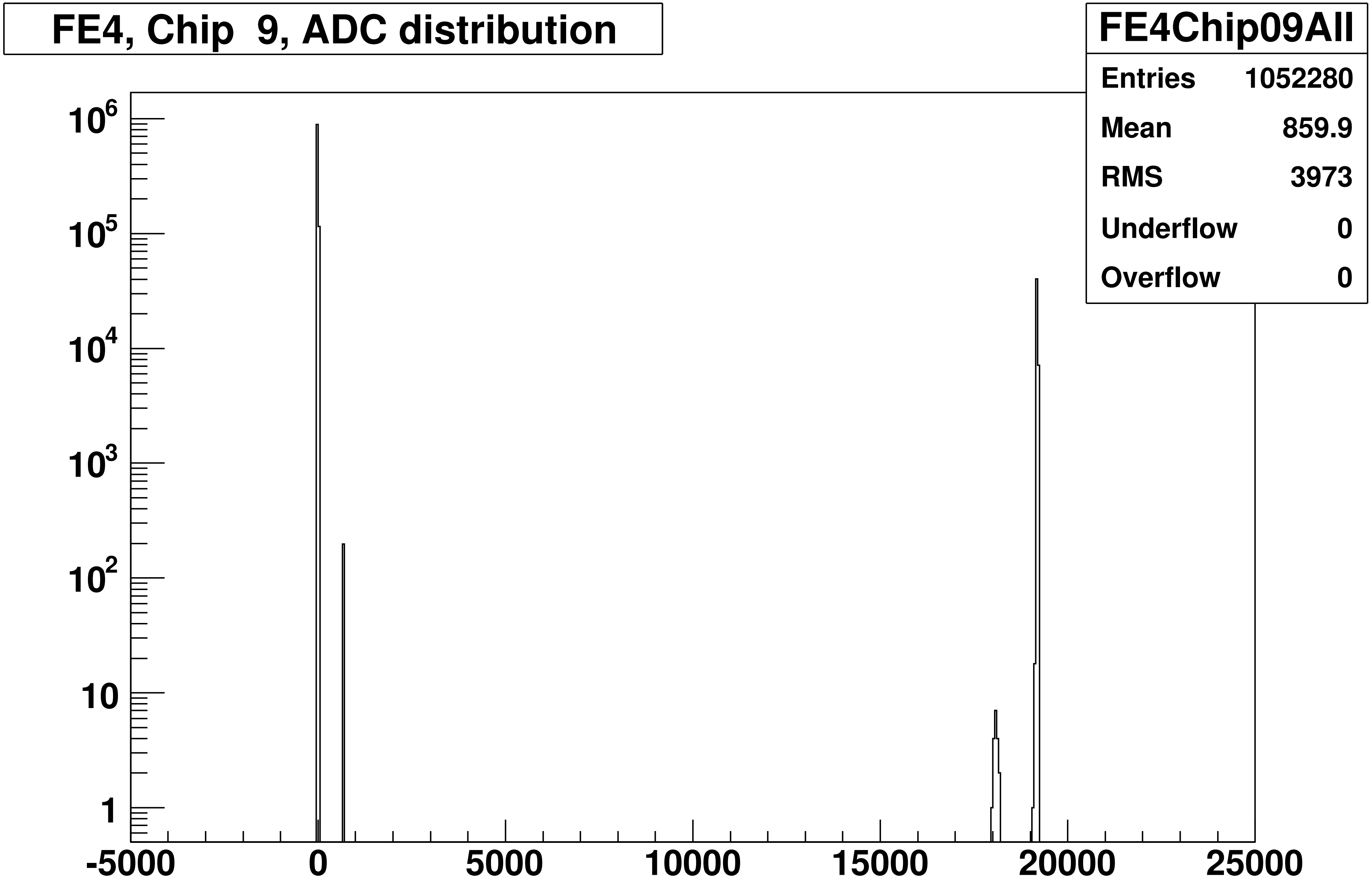
19100
19200
19300
19400



FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 1052280
Mean 859.9
RMS 3973
Underflow 0
Overflow 0
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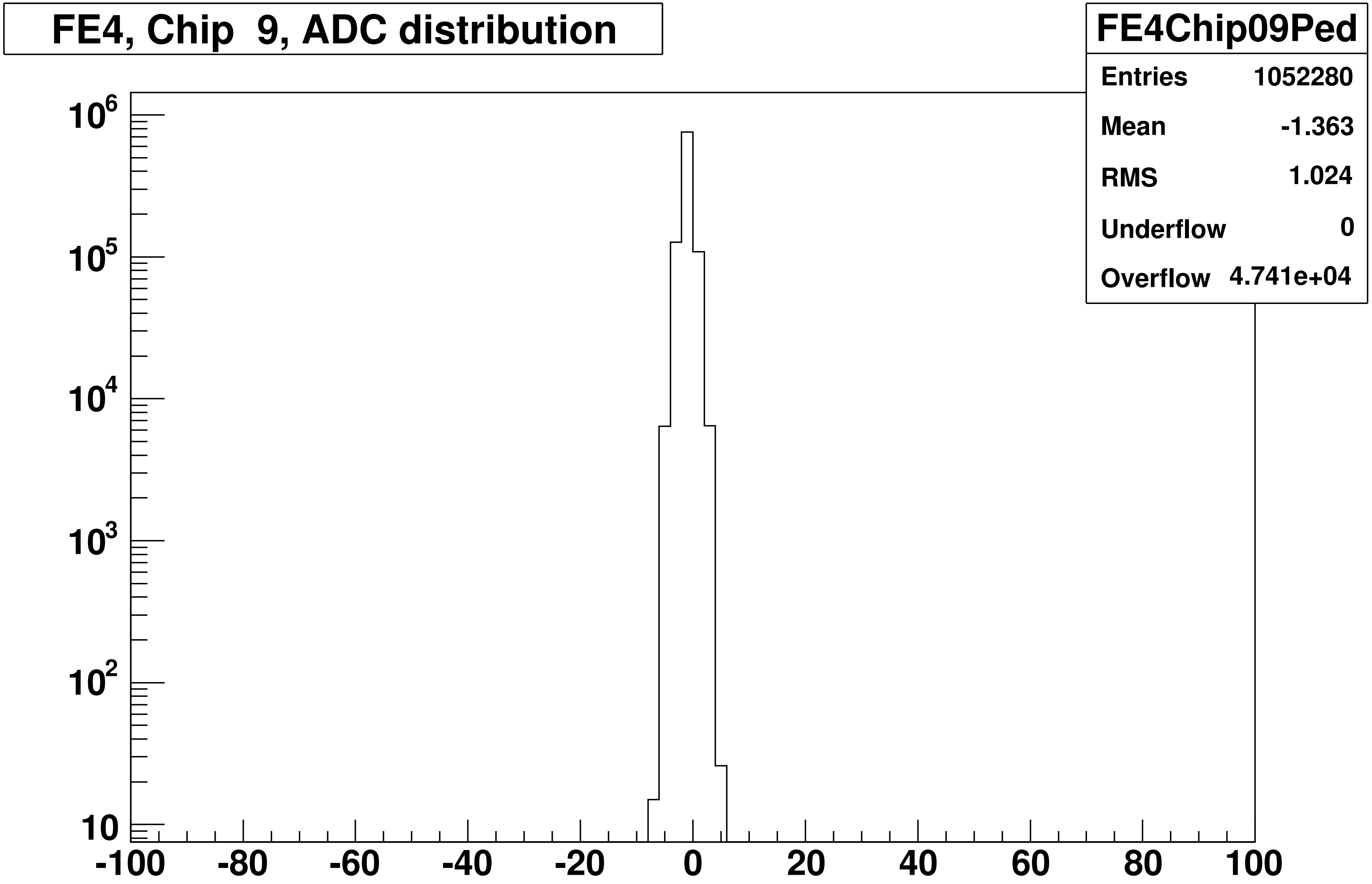
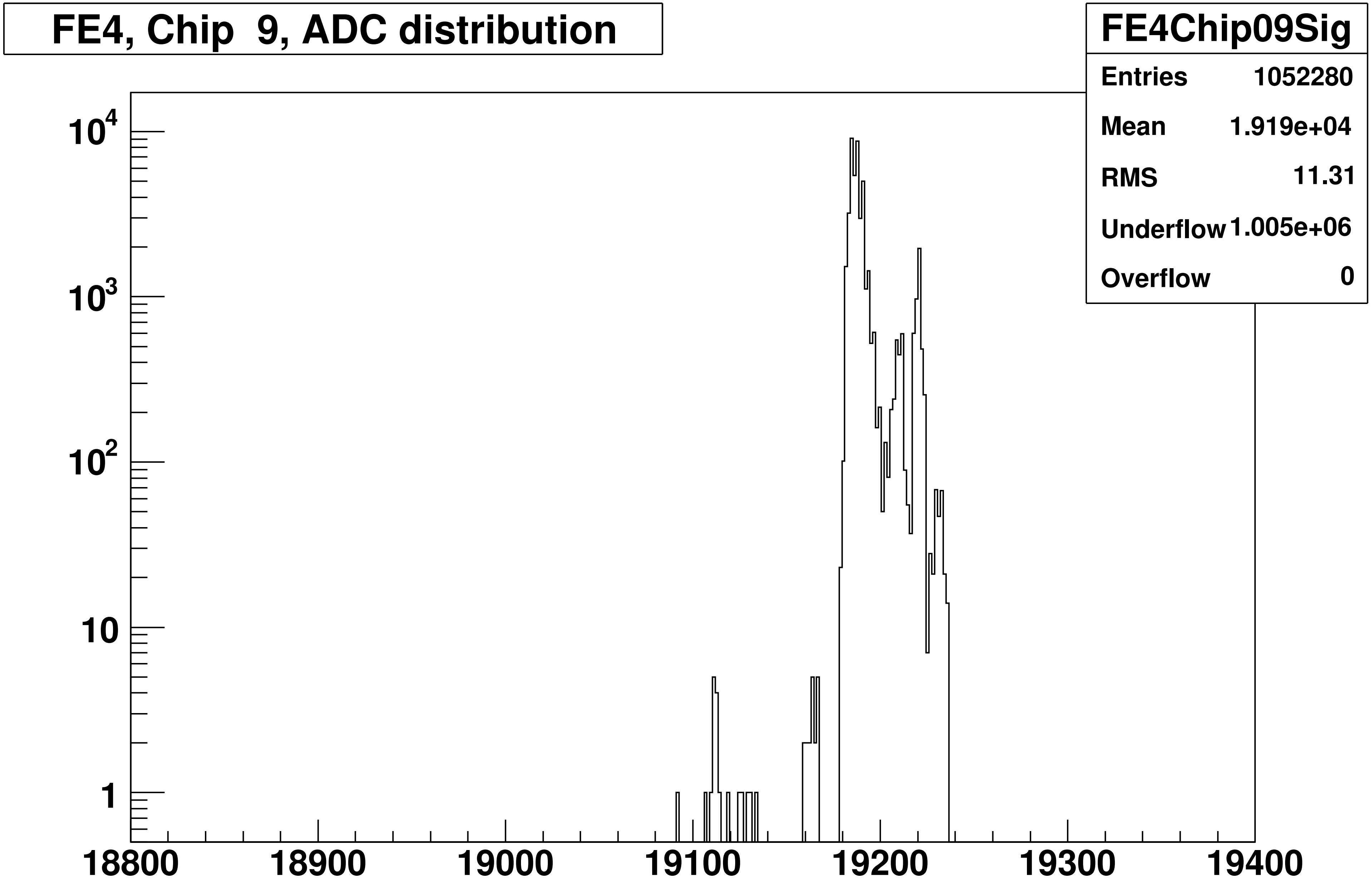
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 1052280
Mean -1.363
RMS 1.024
Underflow 0
Overflow 4.741e+04
10^6
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 1052280
Mean 1.919e+04
RMS 11.31
Underflow 1.005e+06
Overflow 0
10^4
10^3
10^2
10
1
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18900
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19200
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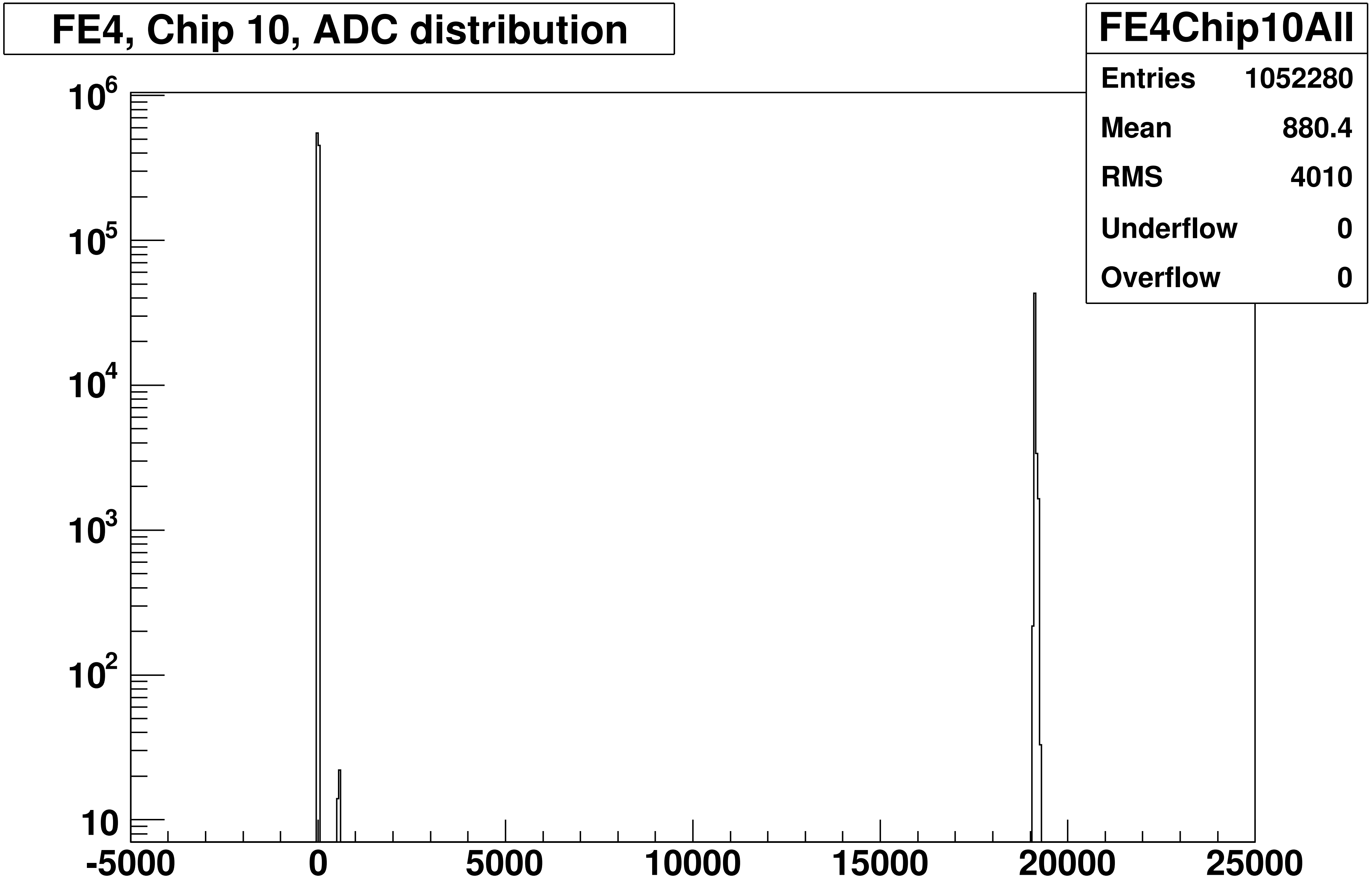
19400


FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 1052280
Mean 880.4
RMS 4010
Underflow 0
Overflow 0
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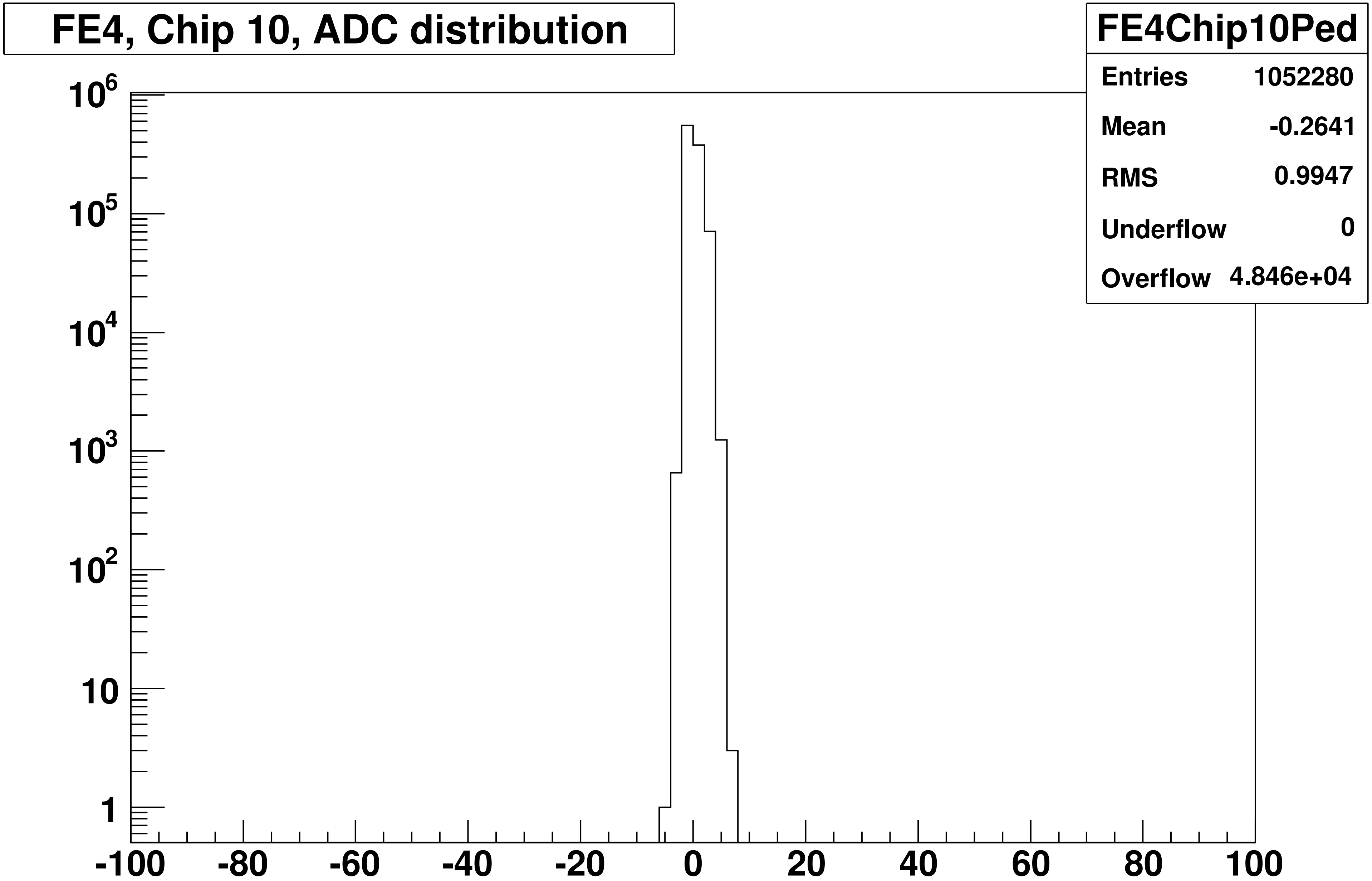
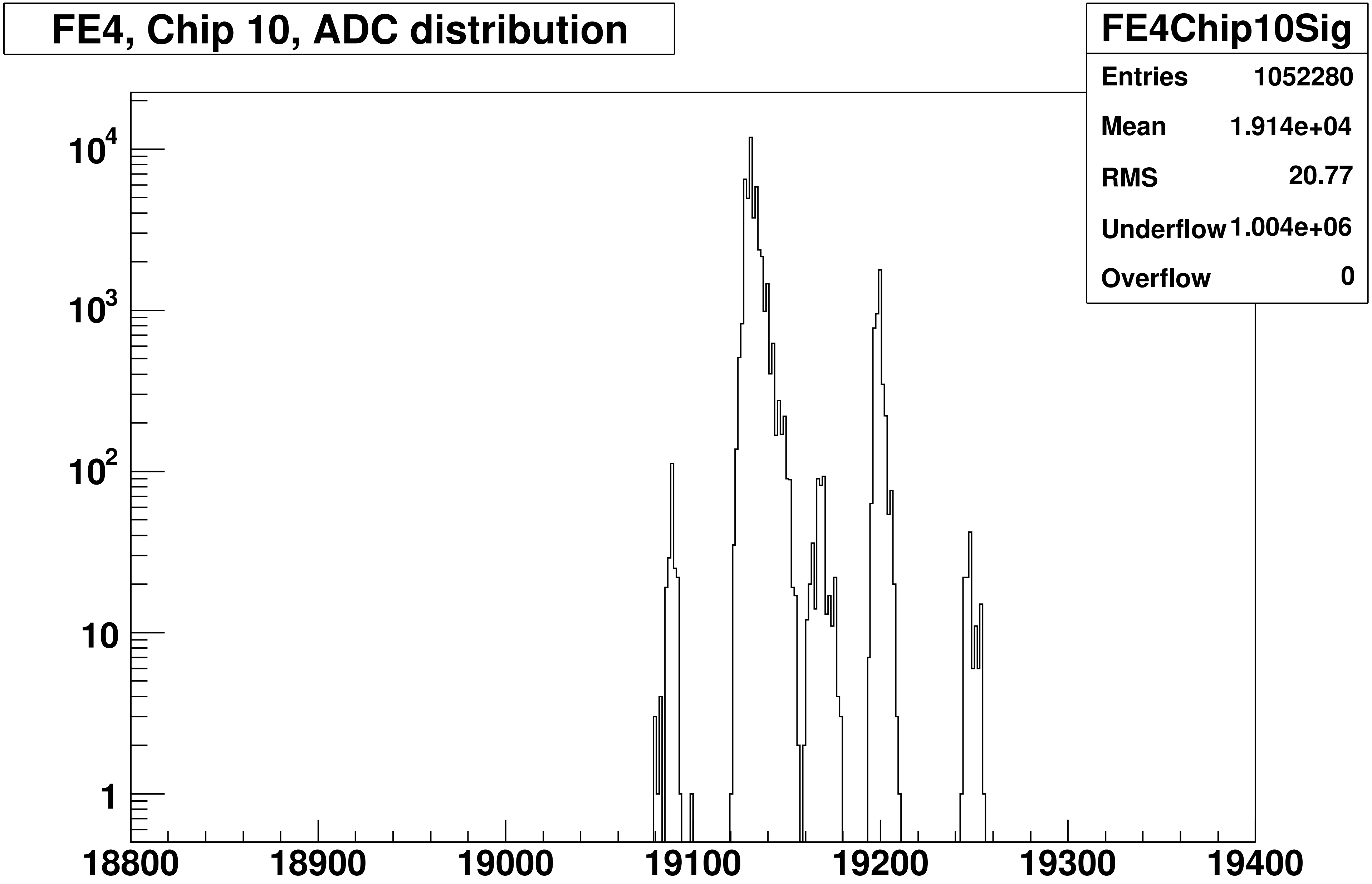
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 1052280
Mean -0.2641
RMS 0.9947
Underflow 0
Overflow 4.846e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 1052280
Mean 1.914e+04
RMS 20.77
Underflow 1.004e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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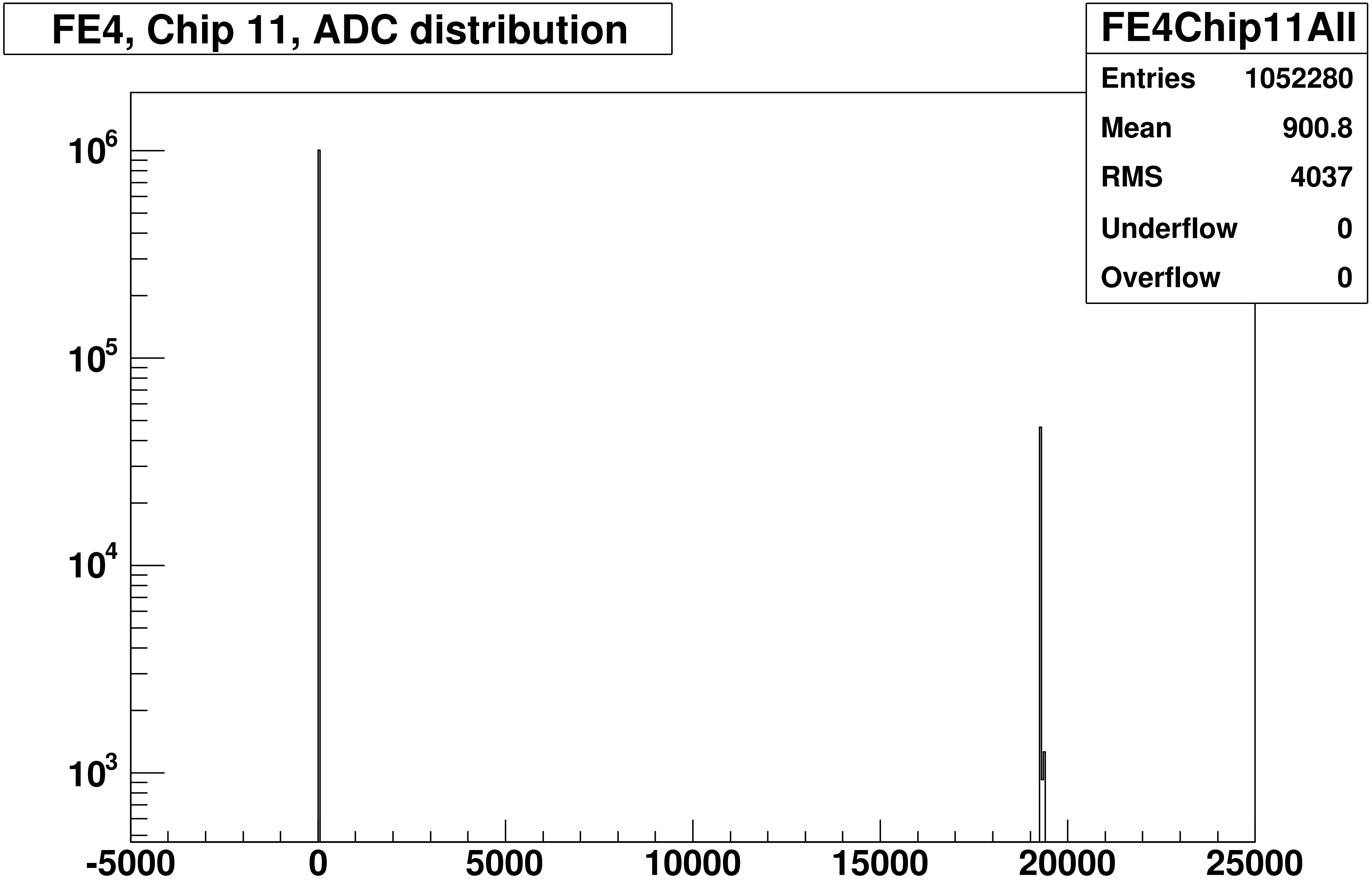
19200
19300
19400


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 1052280
Mean 900.8
RMS 4037
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
-5000
0
5000
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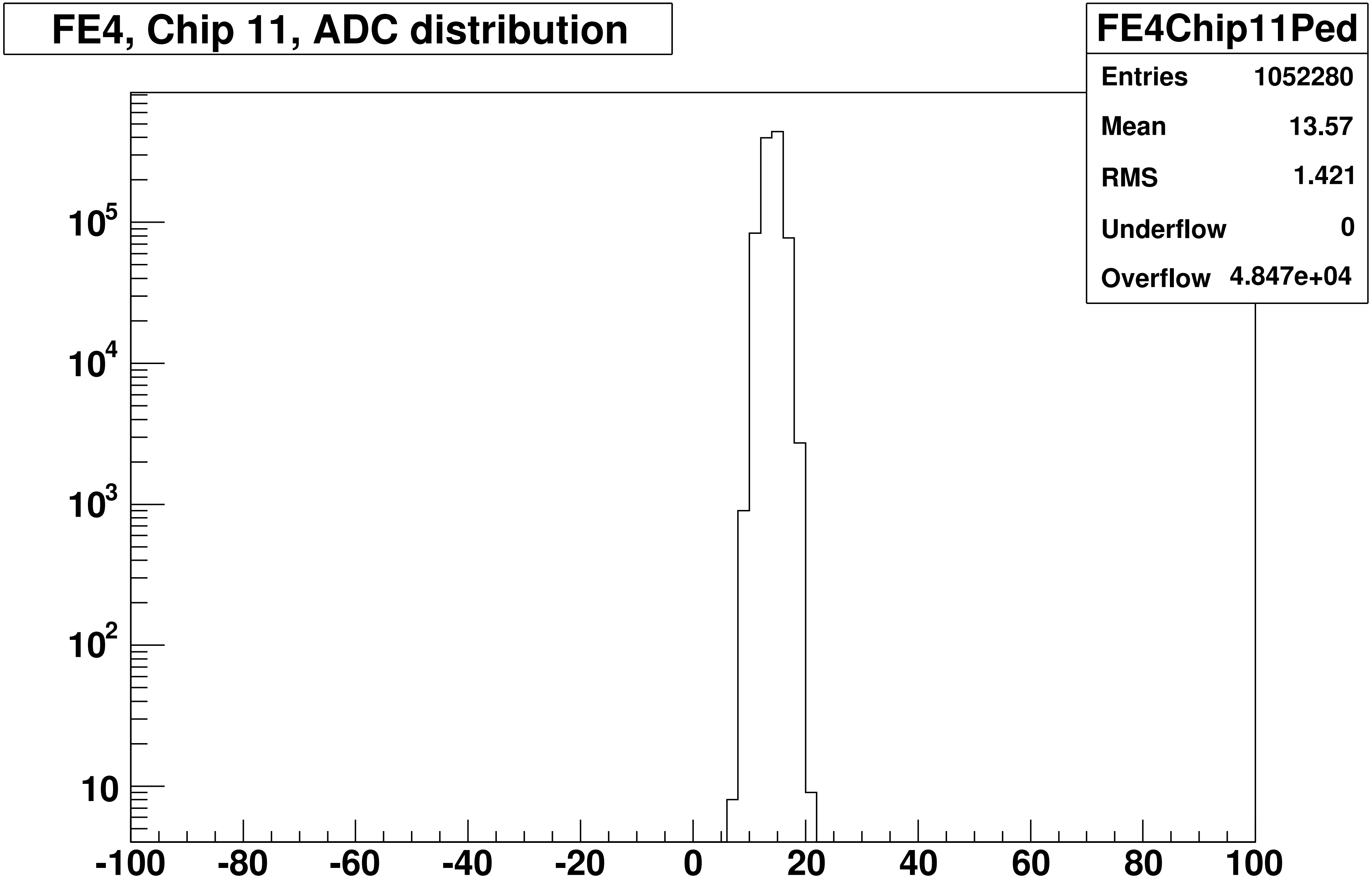
15000
20000
25000



FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 1052280
Mean 13.57
RMS 1.421
Underflow 0
Overflow 4.847e+04
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10^4
10^3
10^2
10
-100
-80
-60
-40
-20
0
20
40
60
80
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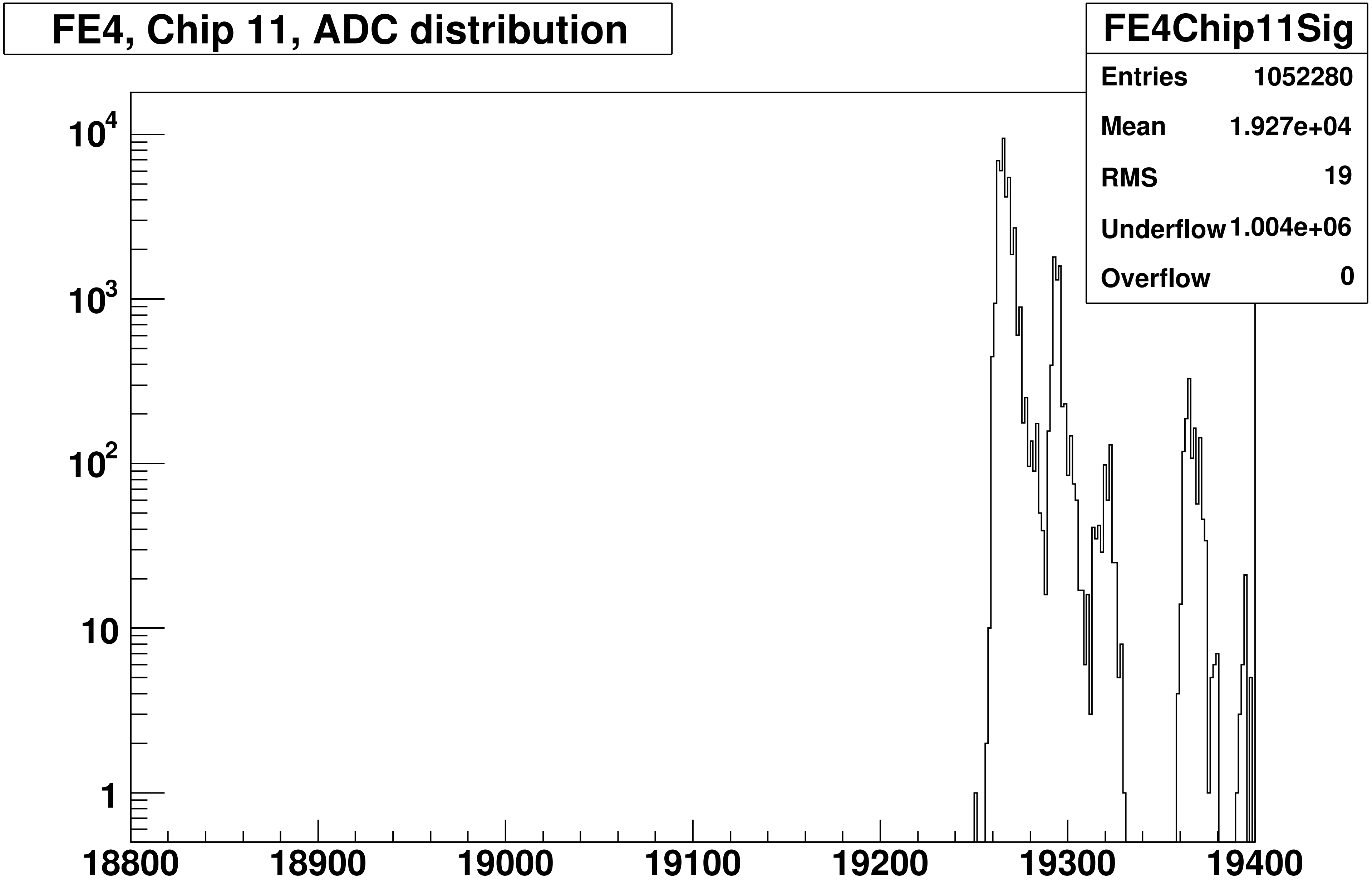

FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 1052280
Mean 1.927e+04
RMS 19
Underflow 1.004e+06
Overflow 0
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10^3
10^2
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18800
18900
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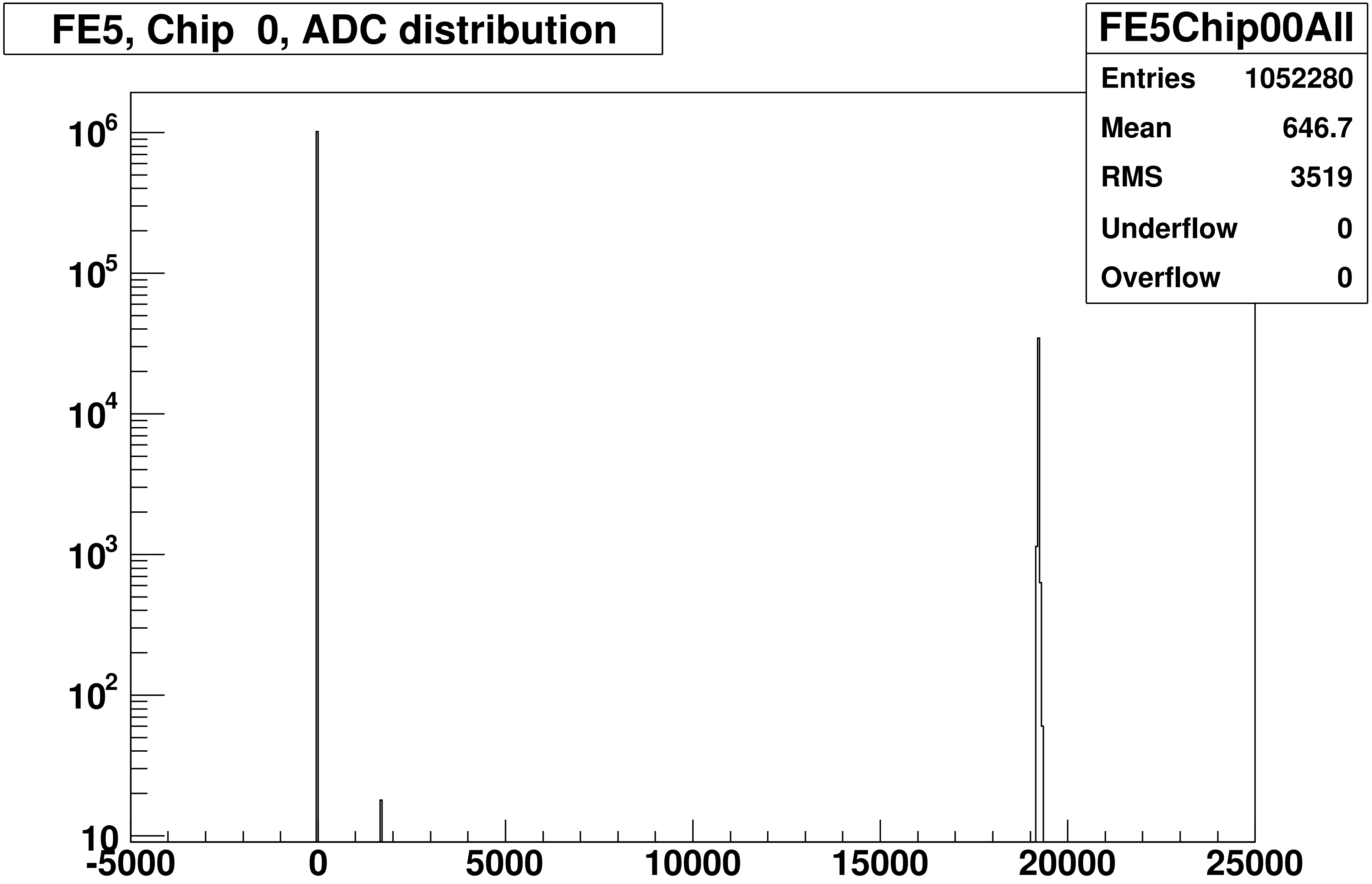
19400


FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 1052280
Mean 646.7
RMS 3519
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
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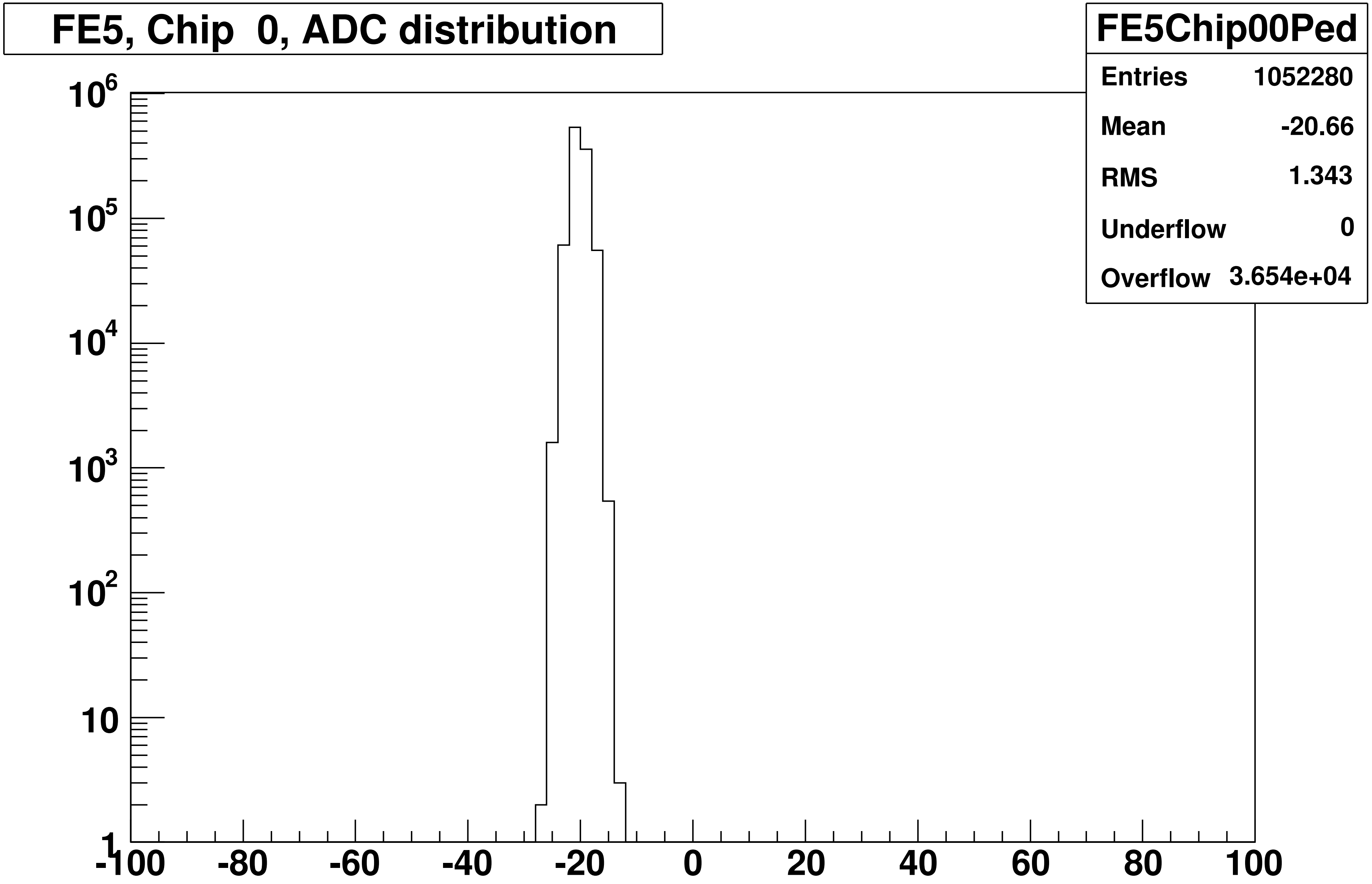
25000



FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 1052280
Mean -20.66
RMS 1.343
Underflow 0
Overflow 3.654e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
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-40
-20
0
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40
60
80
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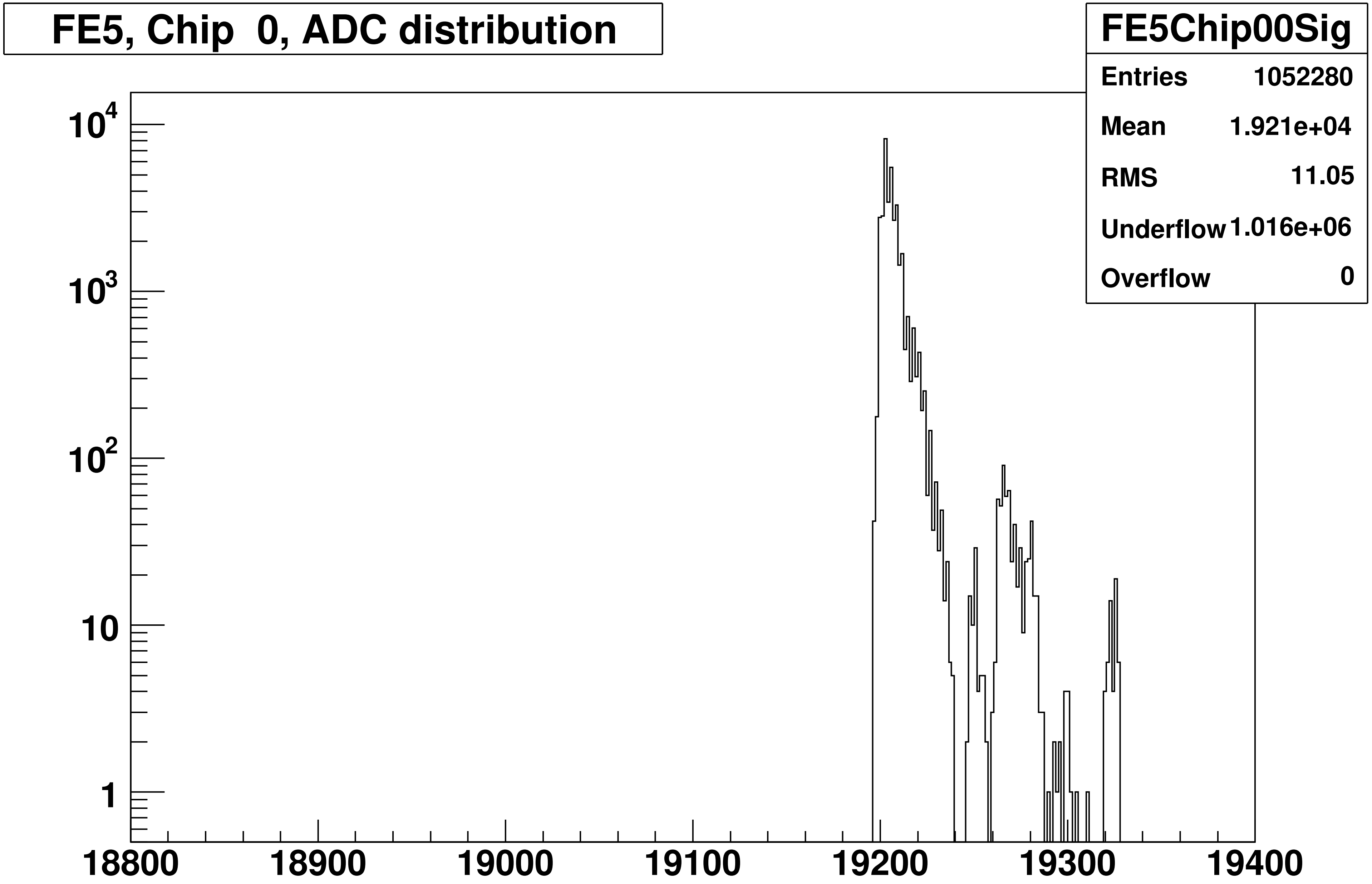
FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 1052280
Mean 1.921e+04
RMS 11.05
Underflow 1.016e+06
Overflow 0
10^4
10^3
10^2
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1
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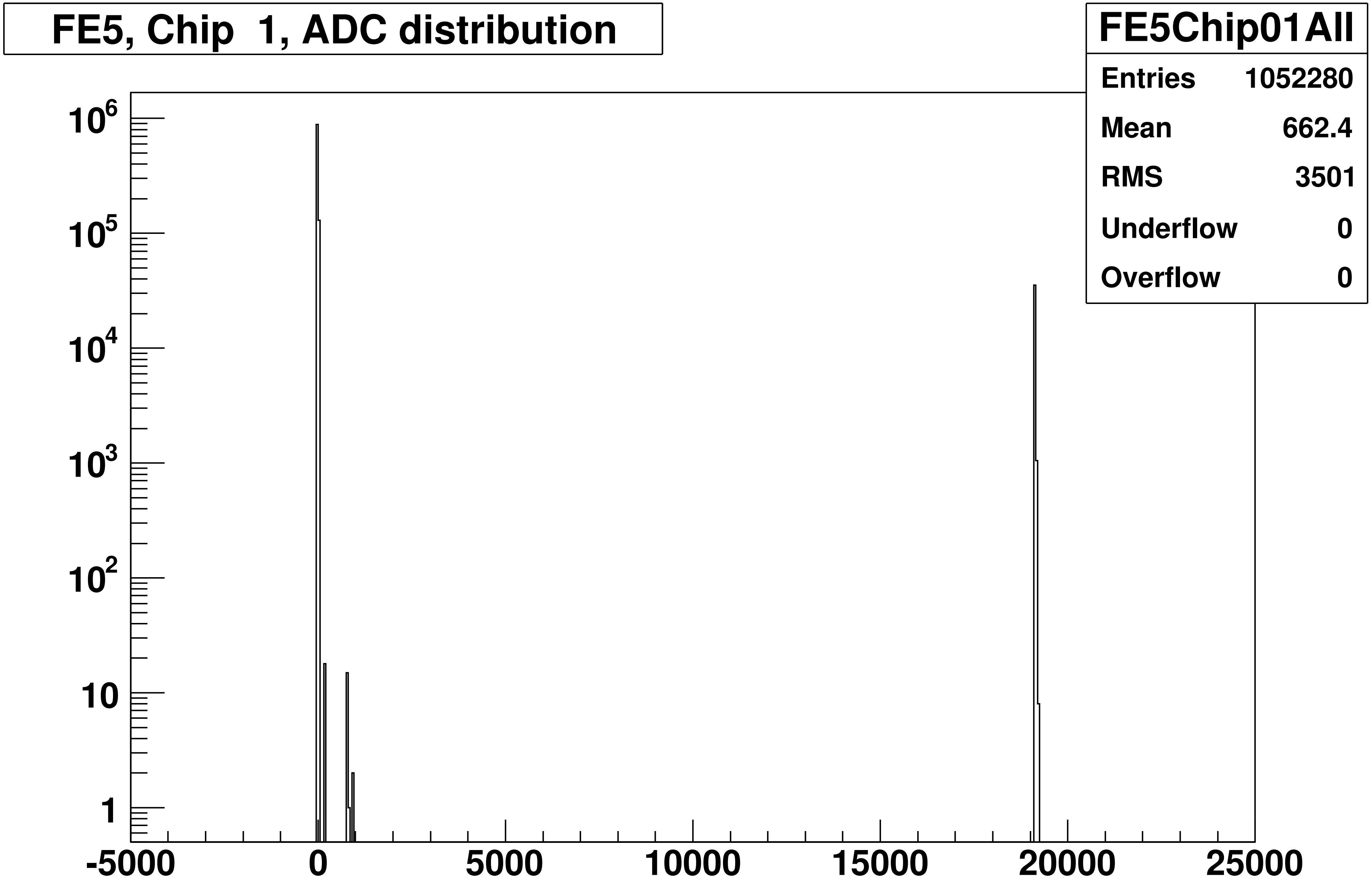

FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 1052280
Mean 662.4
RMS 3501
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
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0
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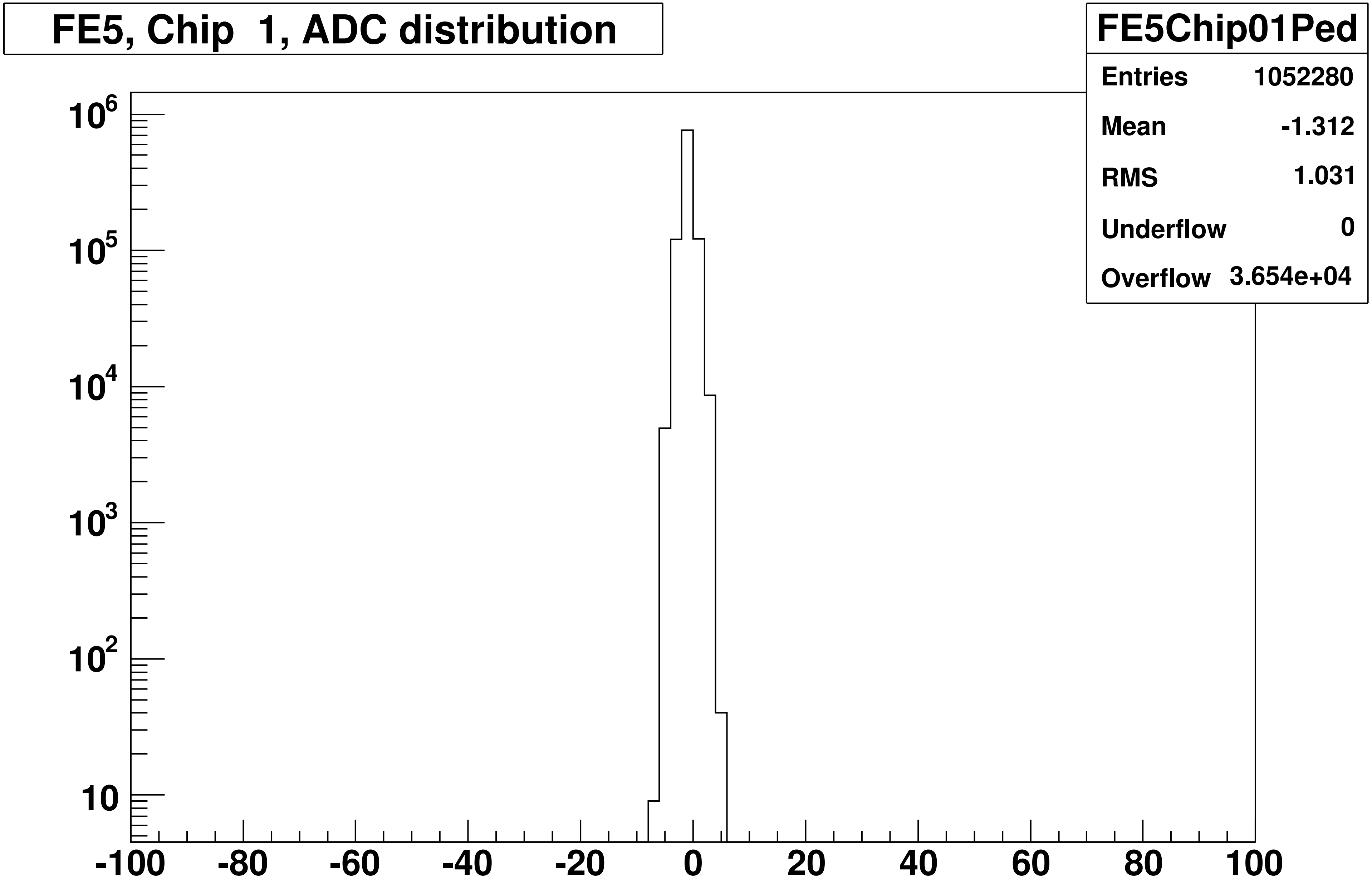
25000


FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 1052280
Mean -1.312
RMS 1.031
Underflow 0
Overflow 3.654e+04
10^6
10^5
10^4
10^3
10^2
10
-100
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-40
-20
0
20
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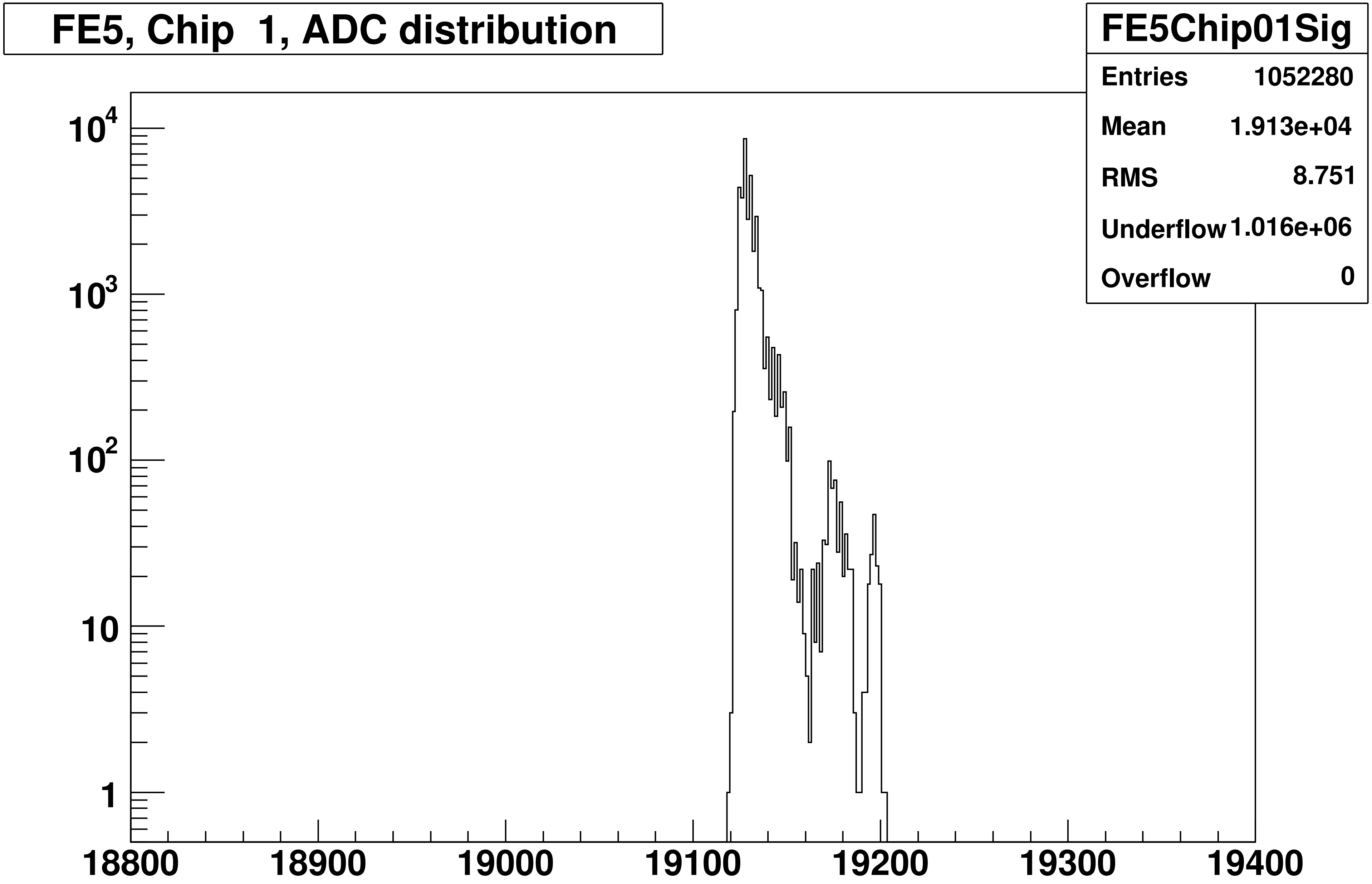

FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 1052280
Mean 1.913e+04
RMS 8.751
Underflow 1.016e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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19100
19200
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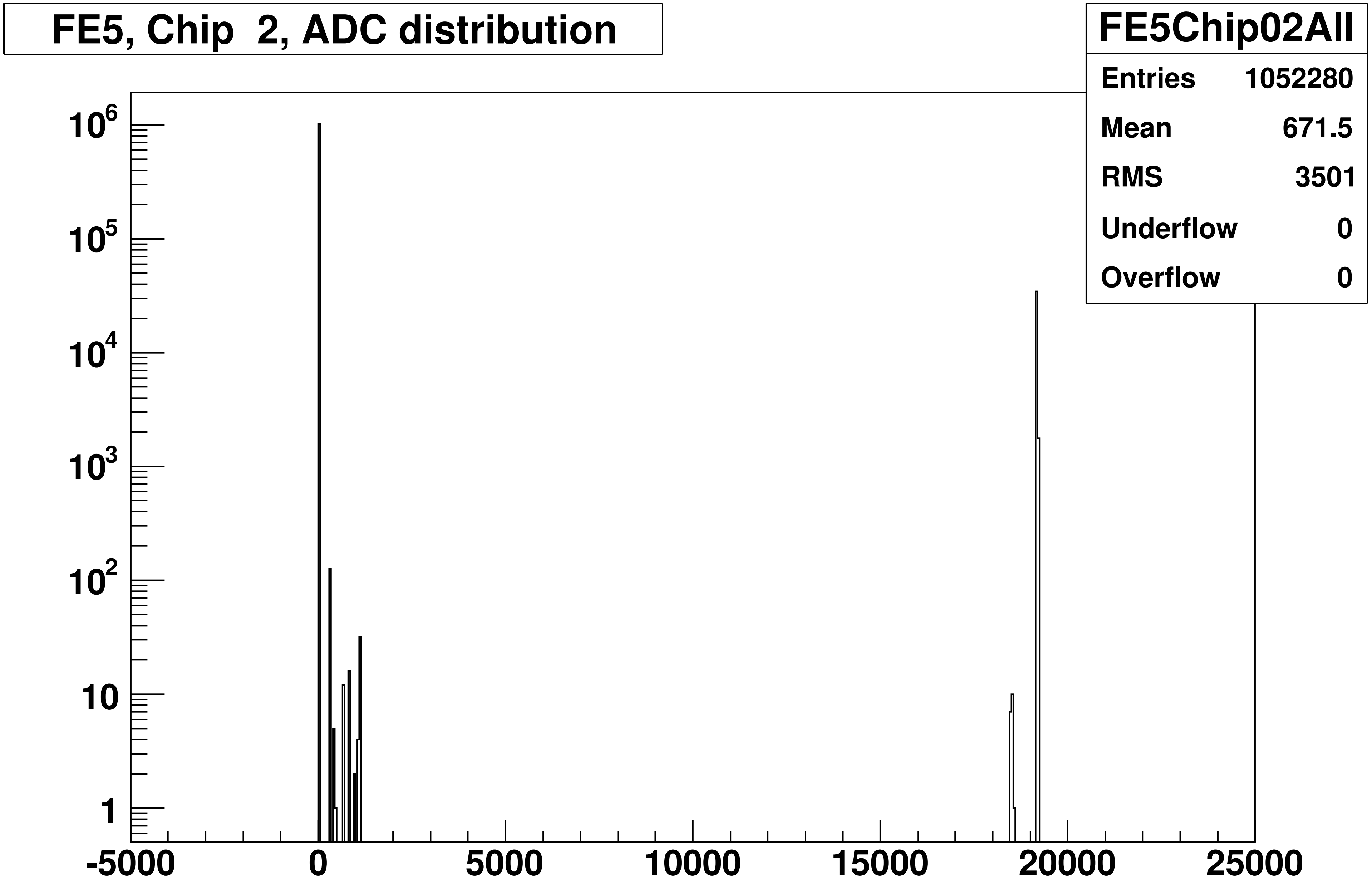
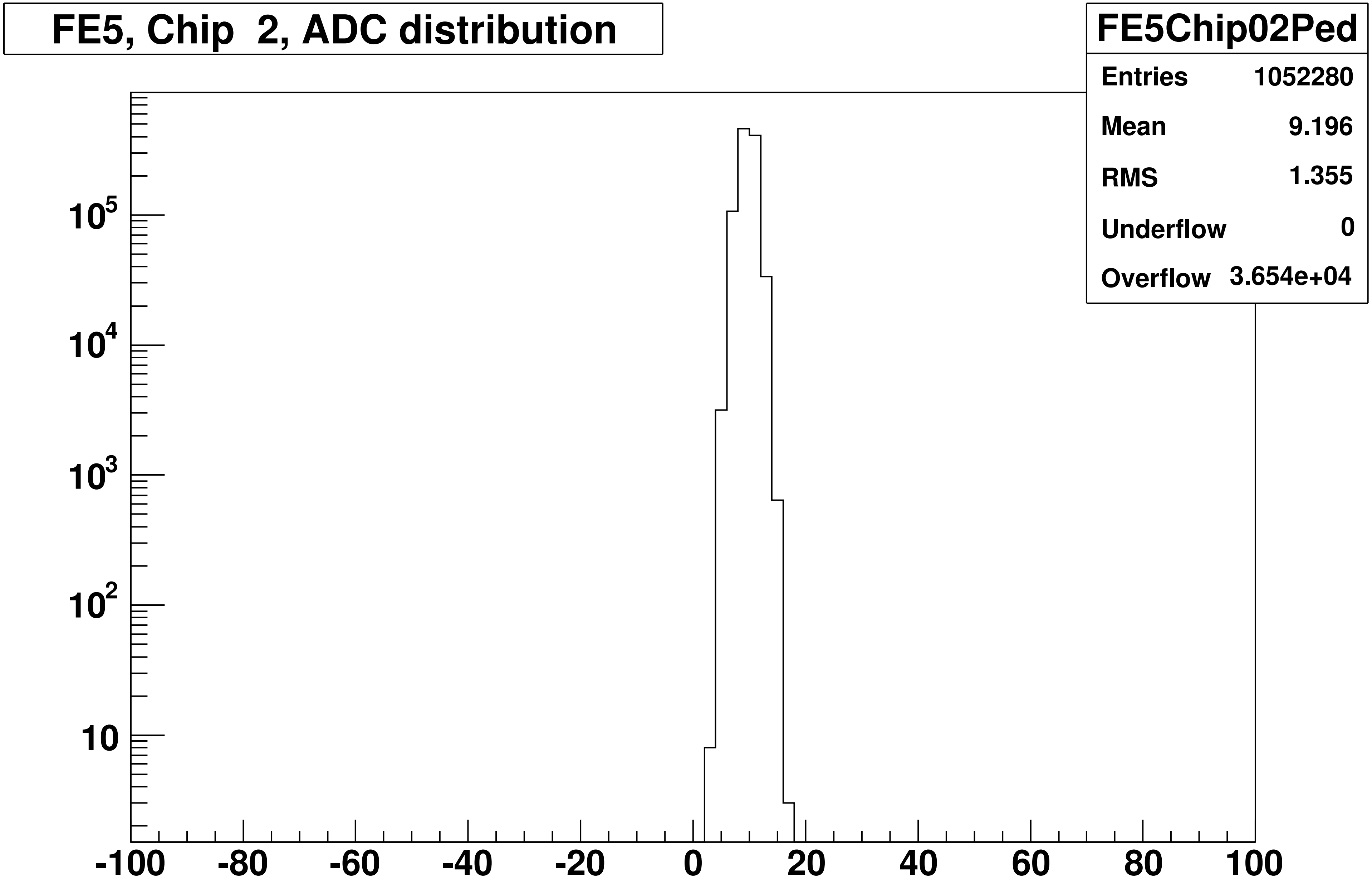
19400



FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 1052280
Mean 671.5
RMS 3501
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 1052280
Mean 9.196
RMS 1.355
Underflow 0
Overflow 3.654e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
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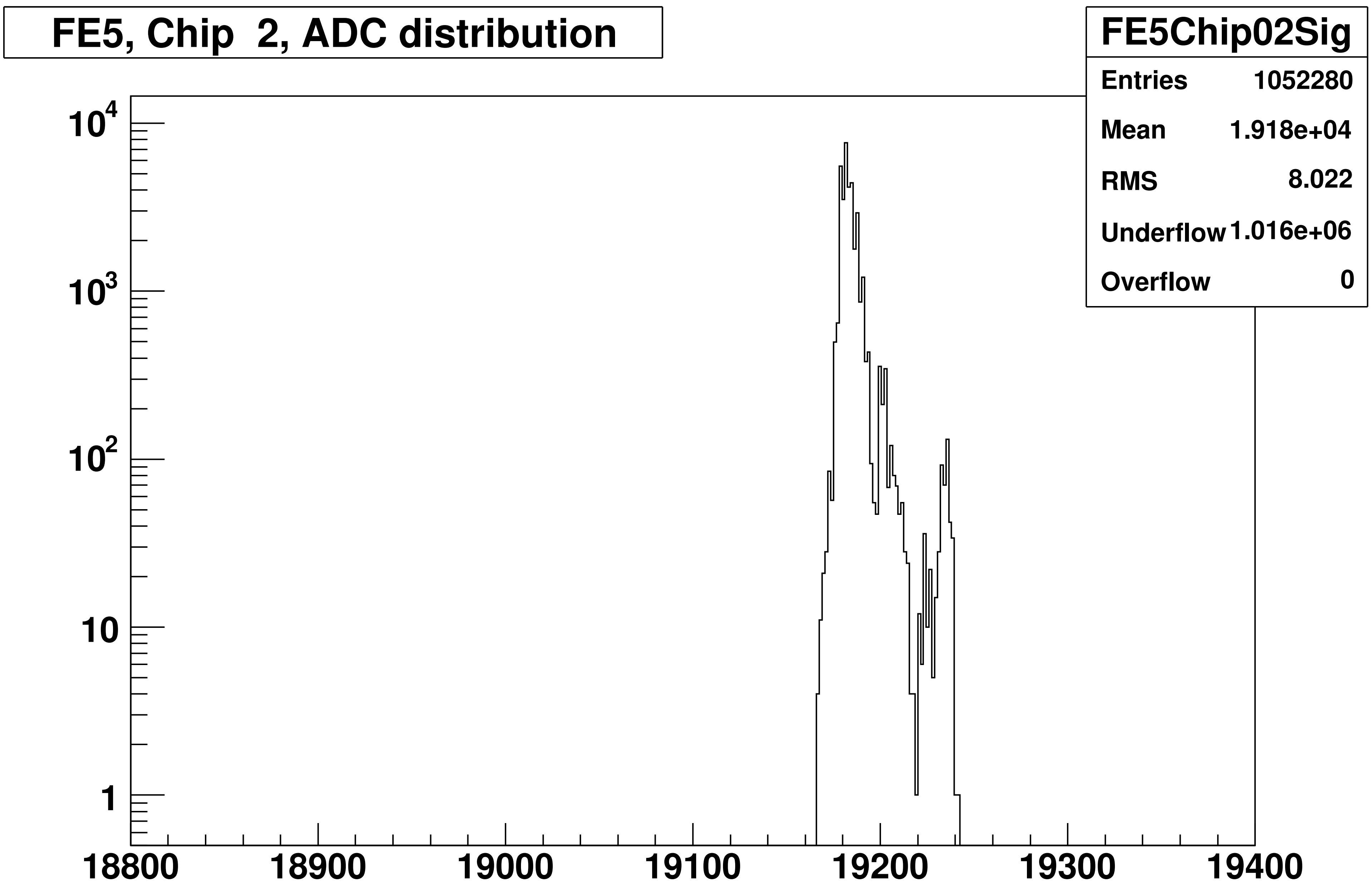
80
100


FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 1052280
Mean 1.918e+04
RMS 8.022
Underflow 1.016e+06
Overflow 0
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10^3
10^2
10
1
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18900
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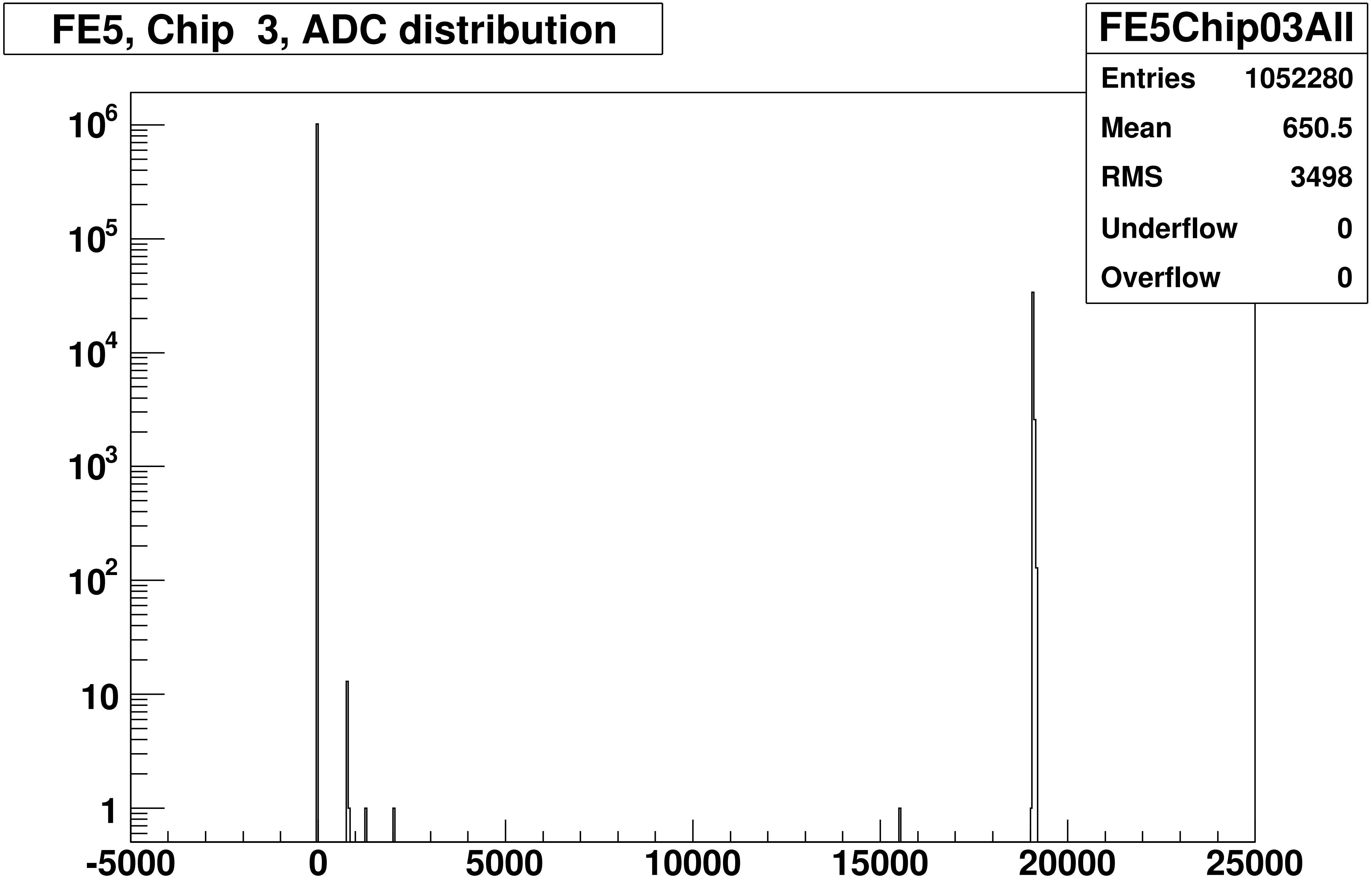
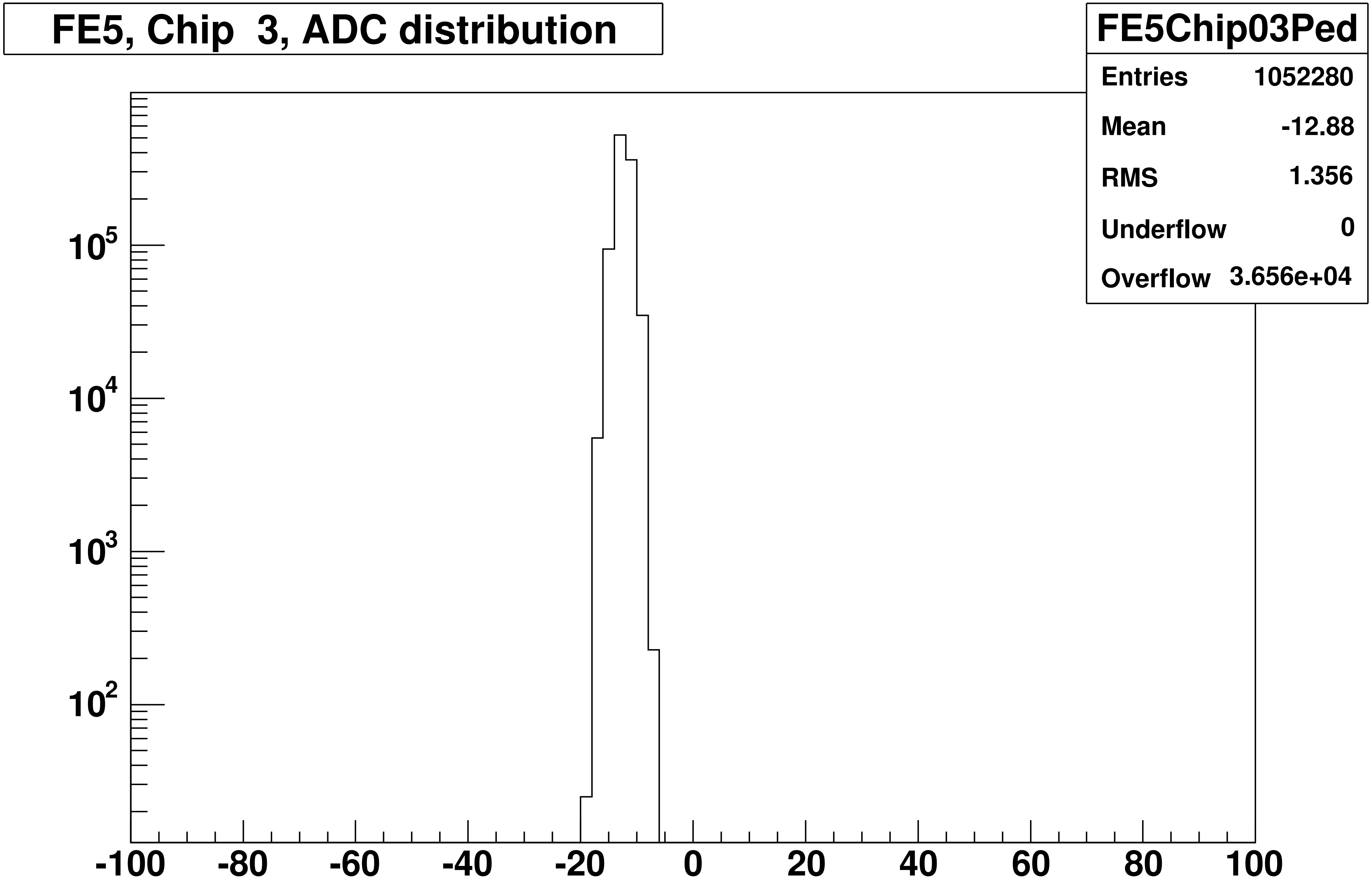

FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 1052280
Mean 650.5
RMS 3498
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 1052280
Mean -12.88
RMS 1.356
Underflow 0
Overflow 3.656e+04
10^5
10^4
10^3
10^2
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-80
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-20
0
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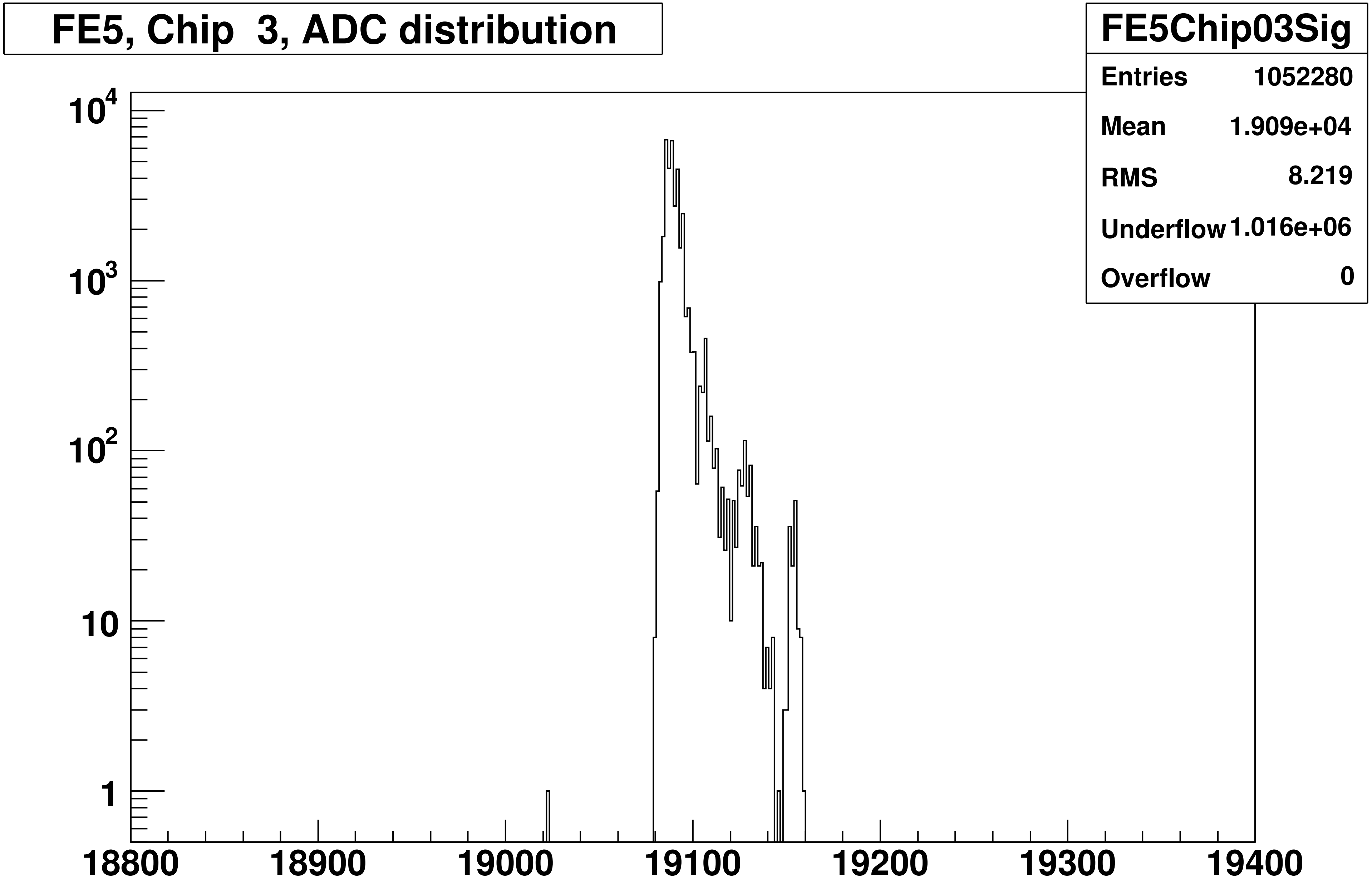
40
60
80
100



FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 1052280
Mean 1.909e+04
RMS 8.219
Underflow 1.016e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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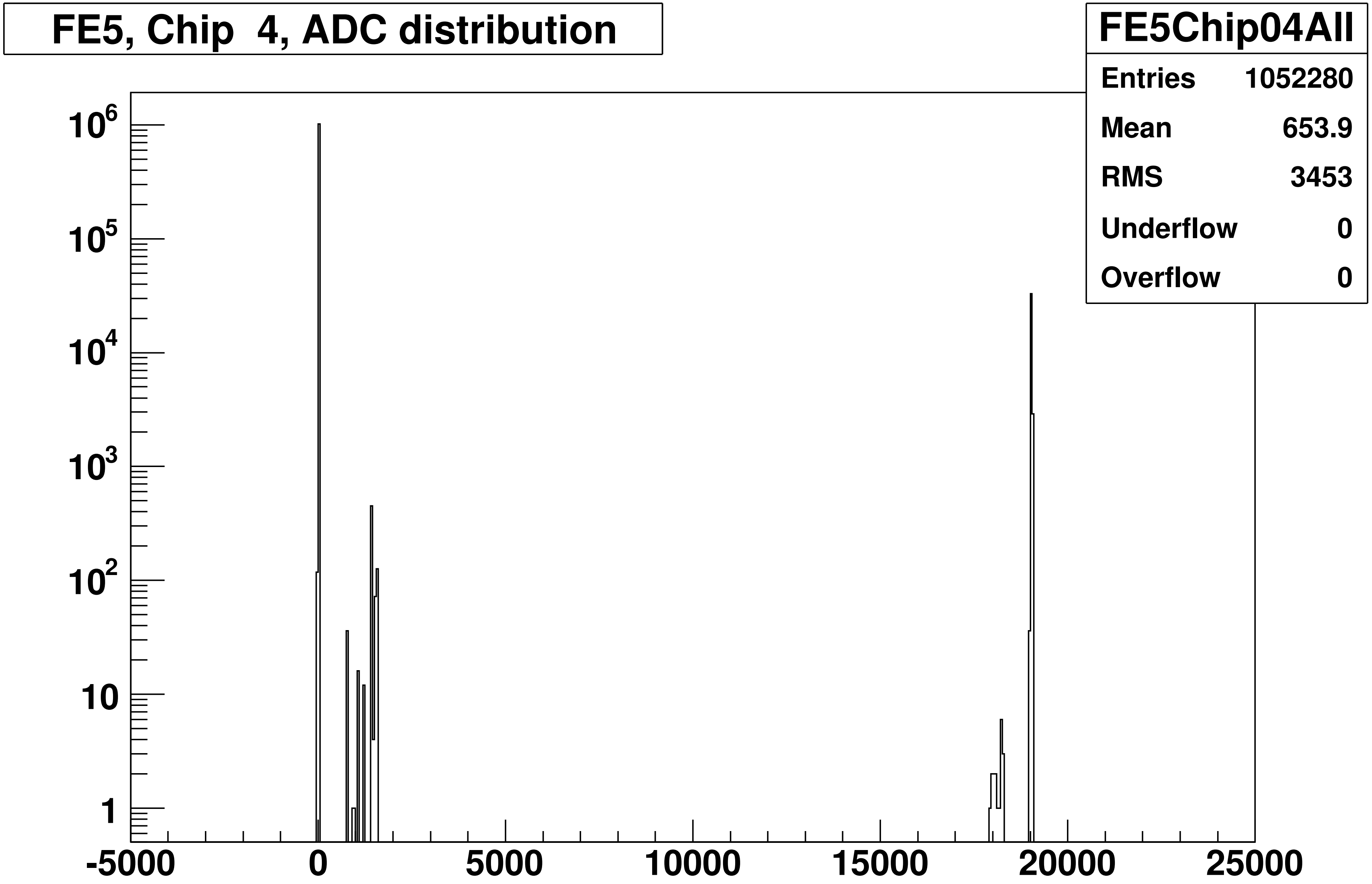
19100
19200
19300
19400


FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 1052280
Mean 653.9
RMS 3453
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
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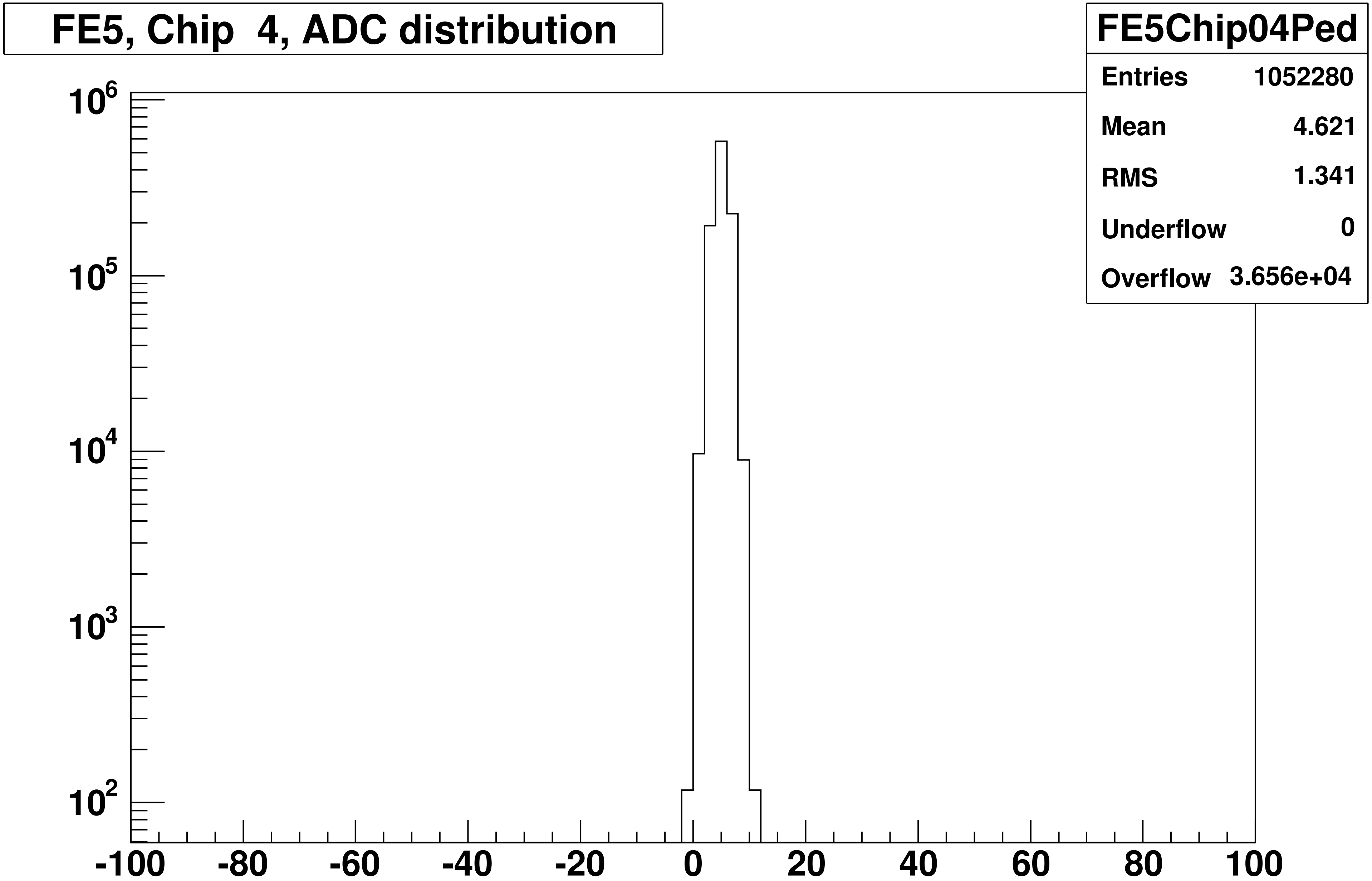
20000
25000



FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 1052280
Mean 4.621
RMS 1.341
Underflow 0
Overflow 3.656e+04
10^6
10^5
10^4
10^3
10^2
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-80
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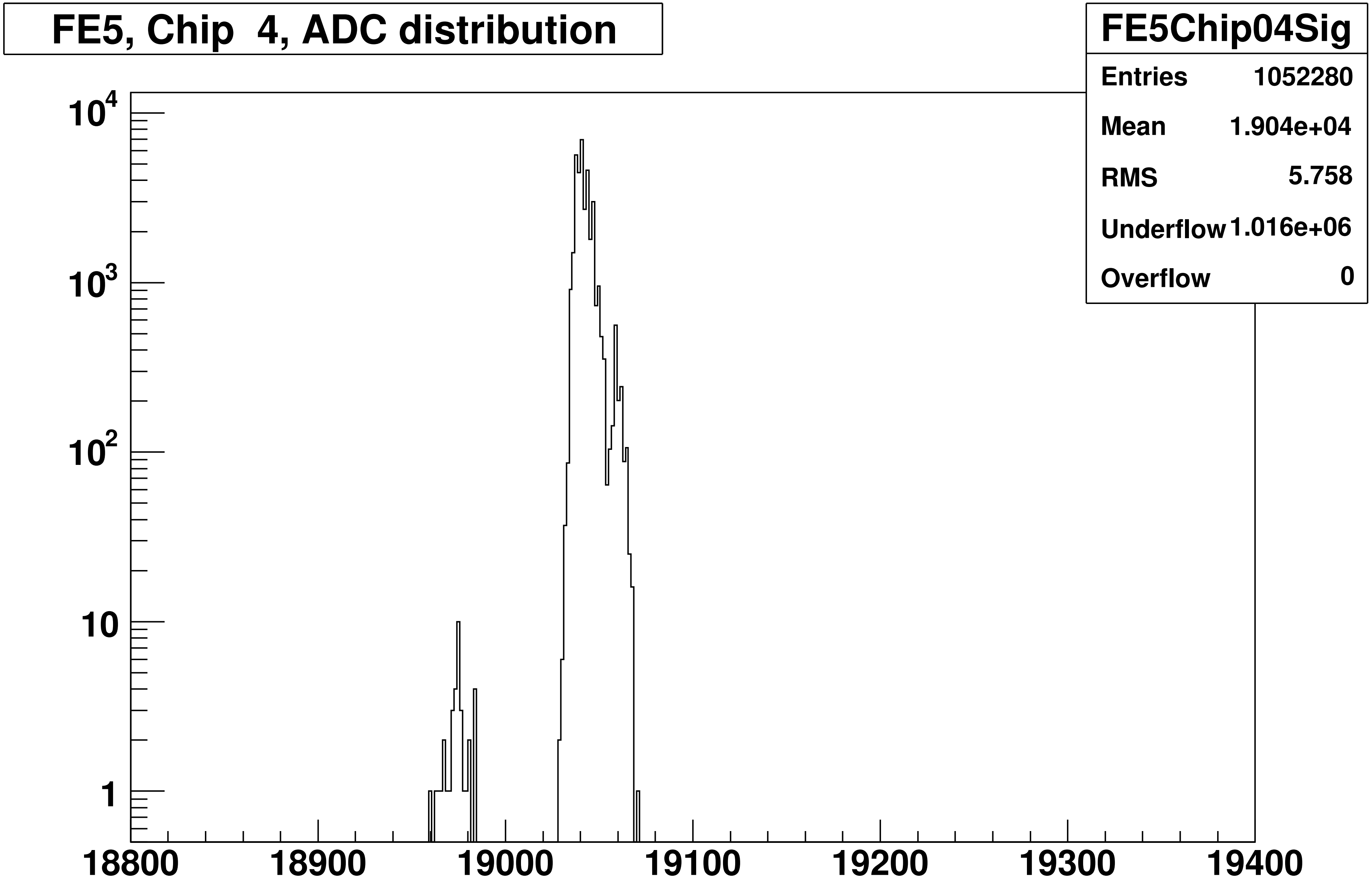

FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 1052280
Mean 1.904e+04
RMS 5.758
Underflow 1.016e+06
Overflow 0
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10^3
10^2
10
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18800
18900
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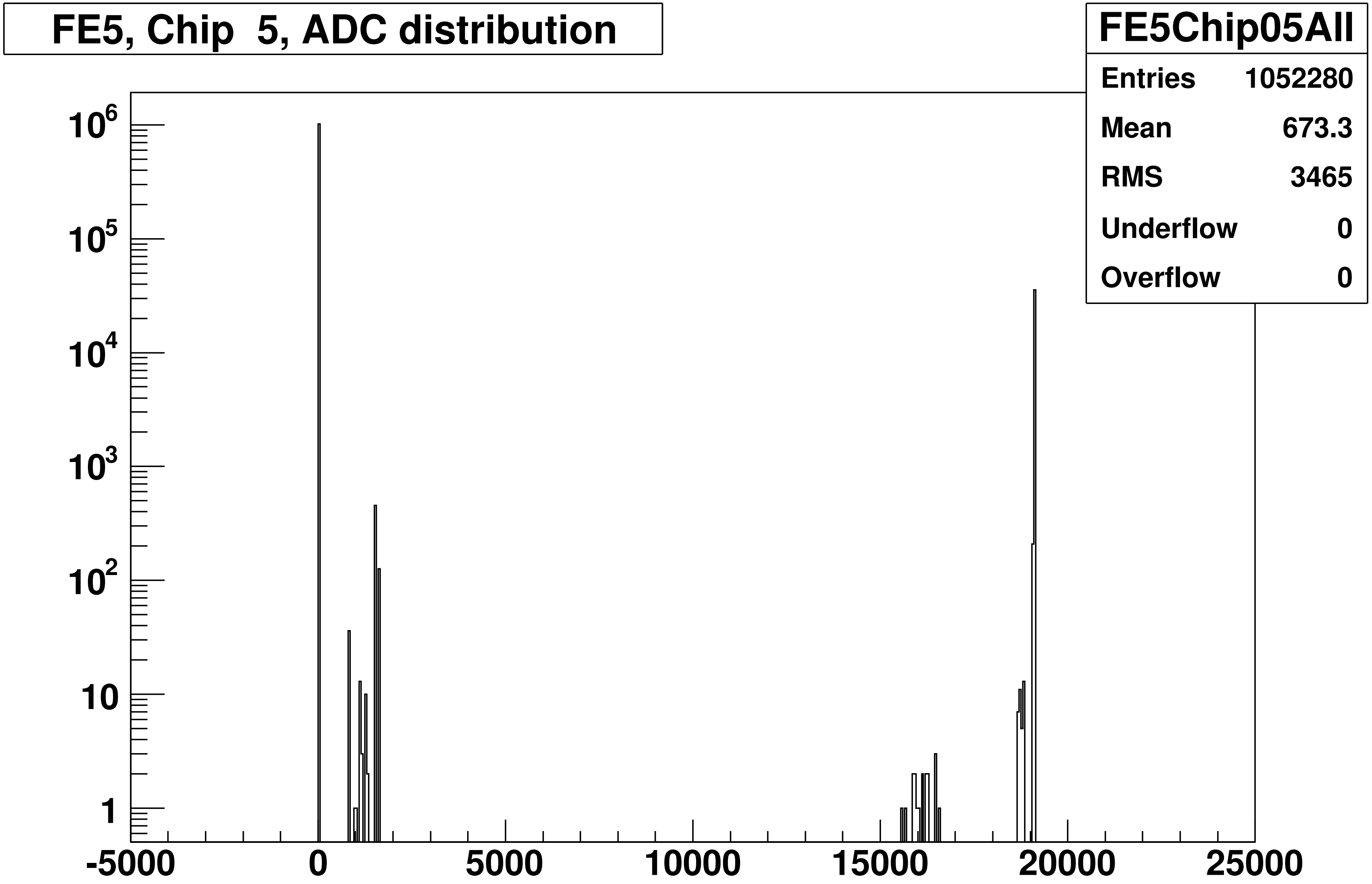
19300
19400



FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 1052280
Mean 673.3
RMS 3465
Underflow 0
Overflow 0
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5000
10000
15000
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25000
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10^2
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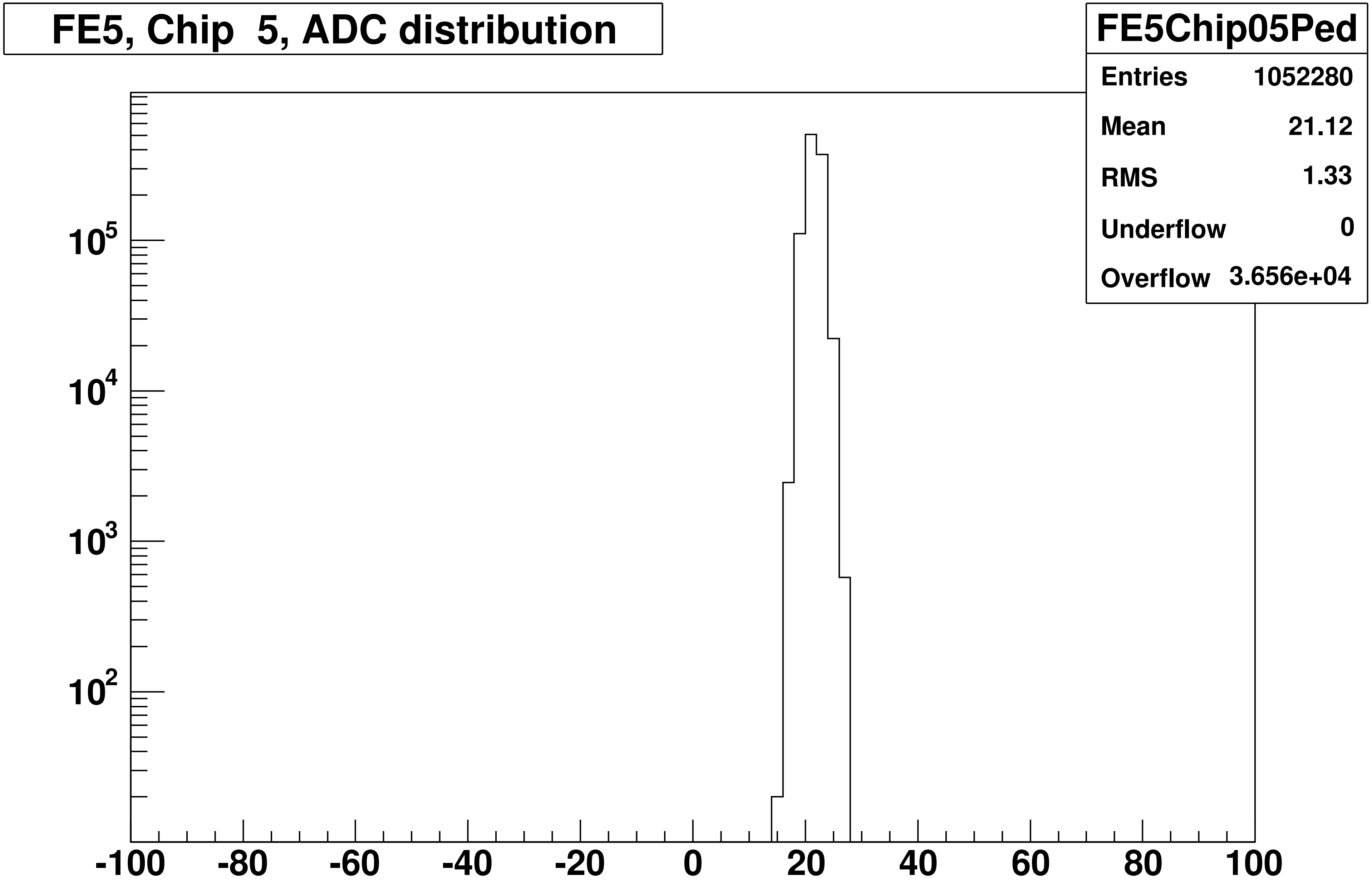
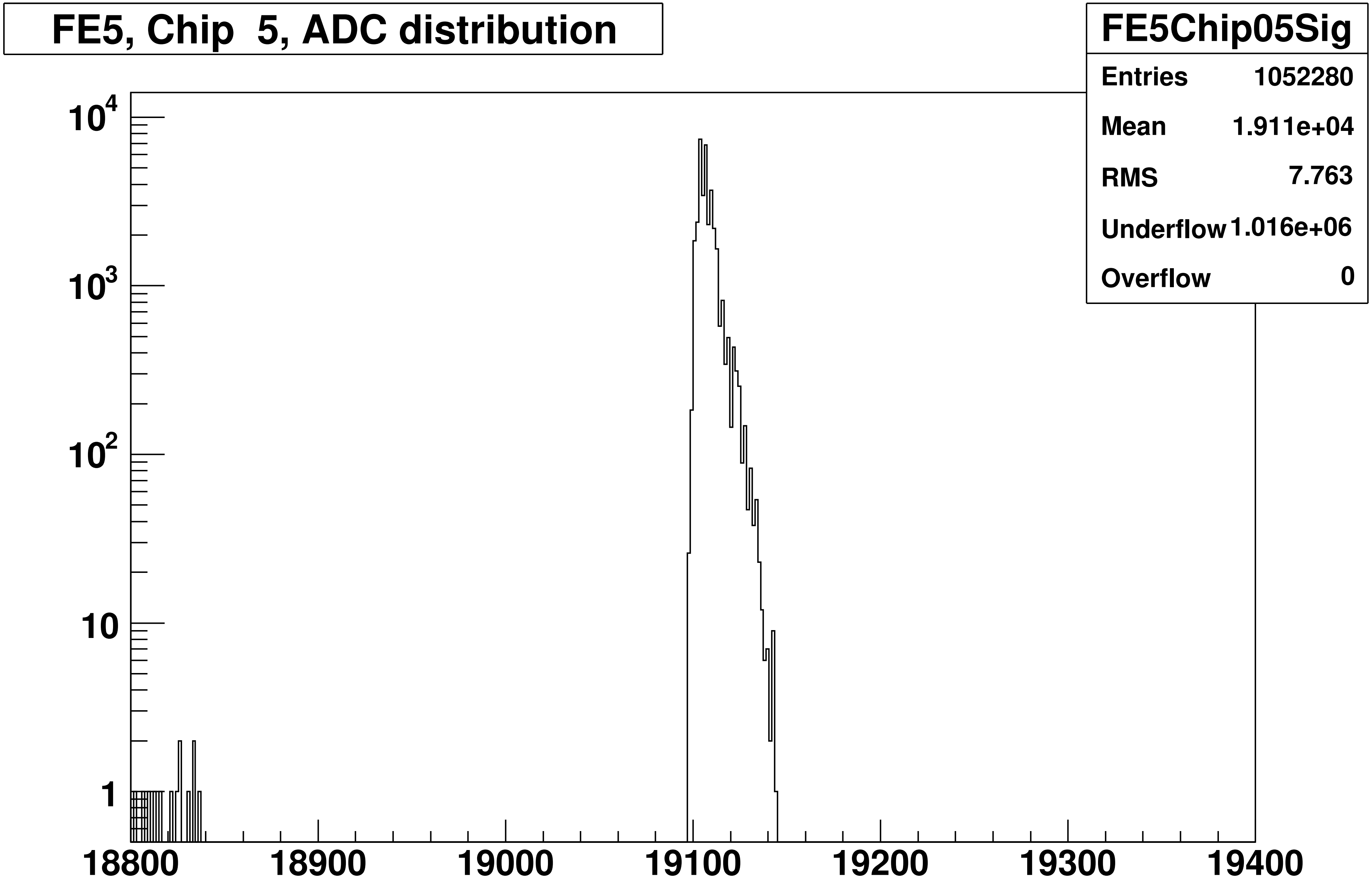
10^4
10^5
10^6



FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 1052280
Mean 21.12
RMS 1.33
Underflow 0
Overflow 3.656e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 1052280
Mean 1.911e+04
RMS 7.763
Underflow 1.016e+06
Overflow 0
10^4
10^3
10^2
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1
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18900
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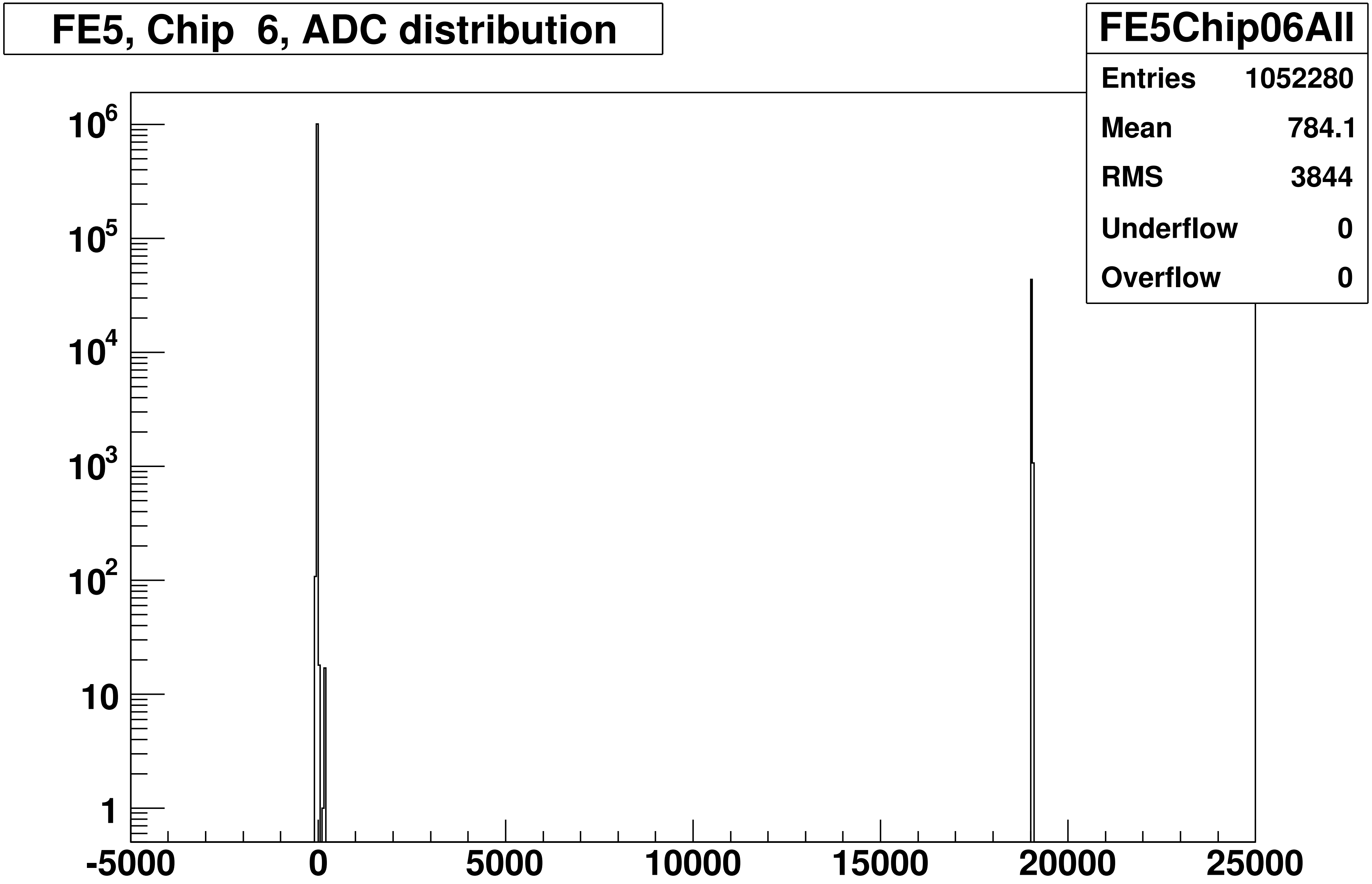

FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 1052280
Mean 784.1
RMS 3844
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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1
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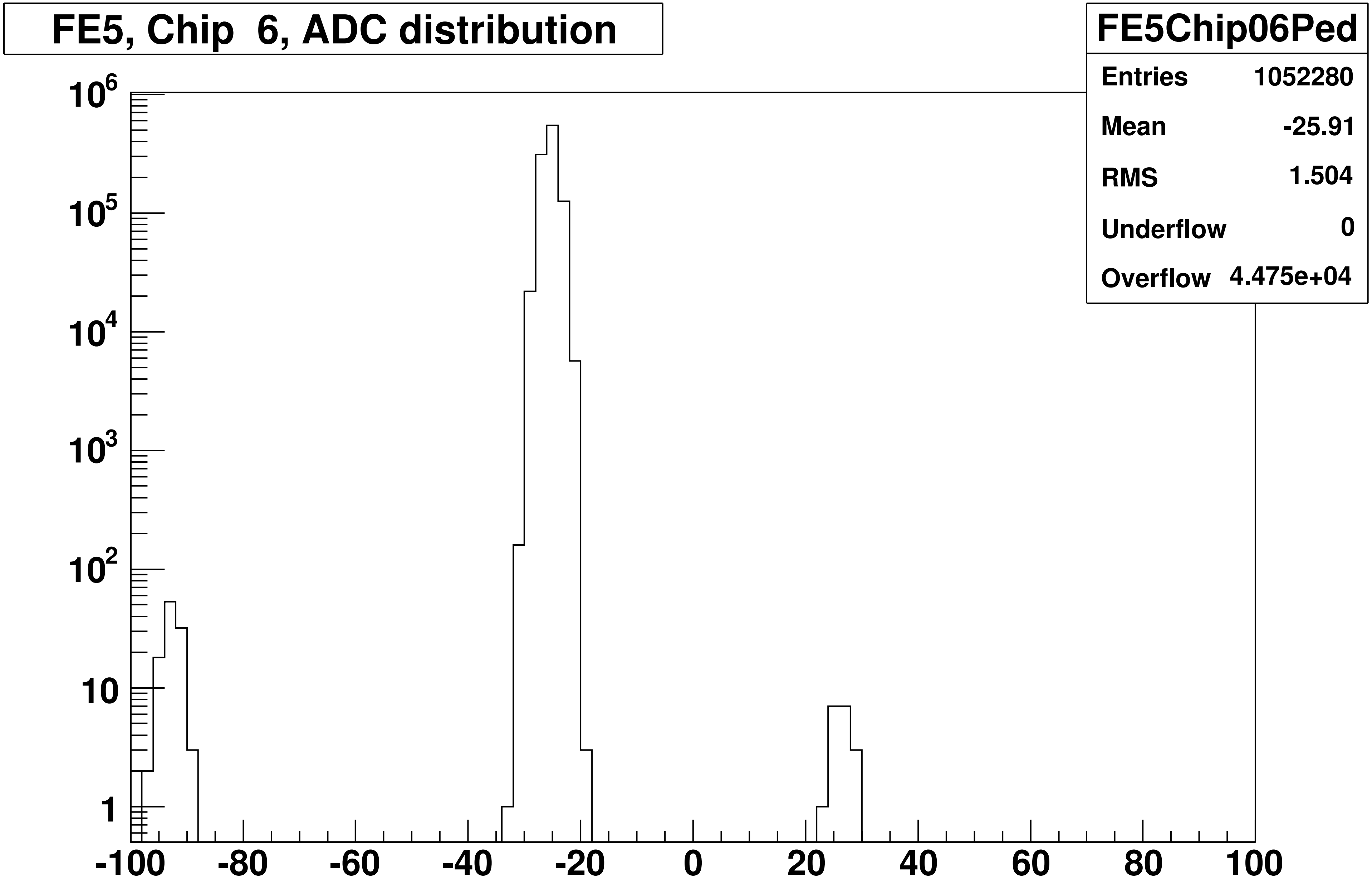
FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 1052280
Mean -25.91
RMS 1.504
Underflow 0
Overflow 4.475e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
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-60
-40
-20
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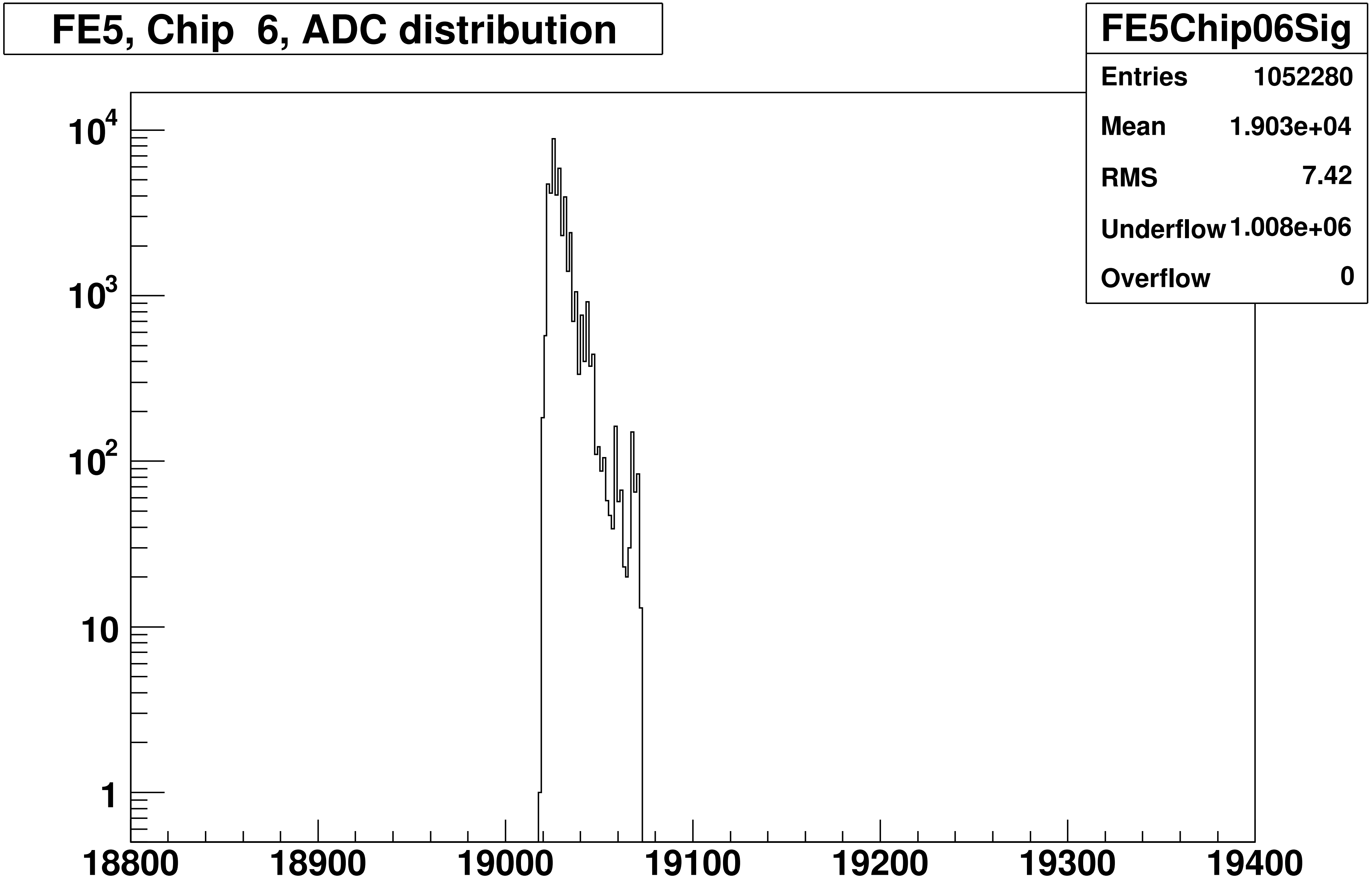
60
80
100



FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 1052280
Mean 1.903e+04
RMS 7.42
Underflow 1.008e+06
Overflow 0
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10^3
10^2
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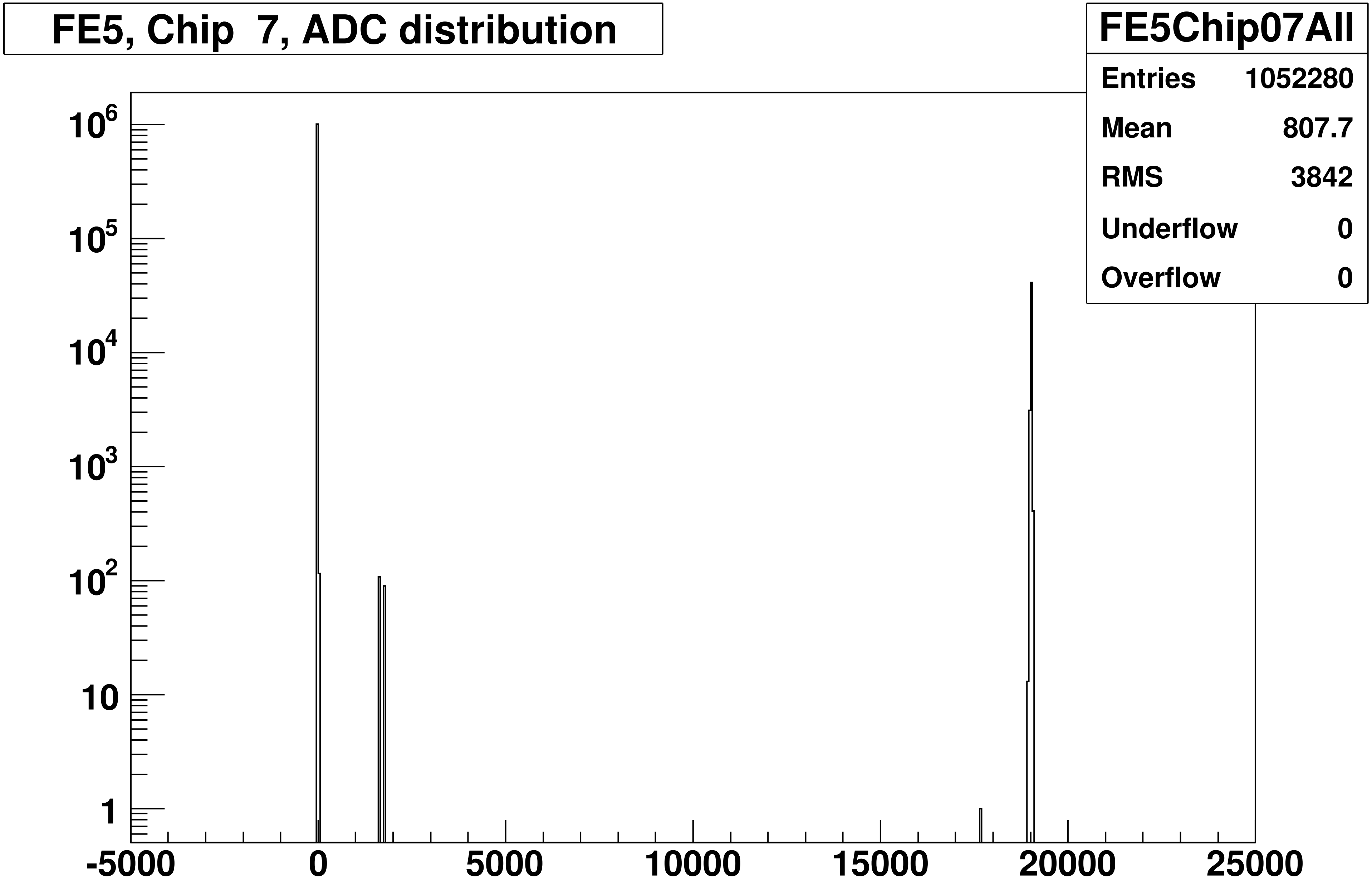
FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 1052280
Mean 807.7
RMS 3842
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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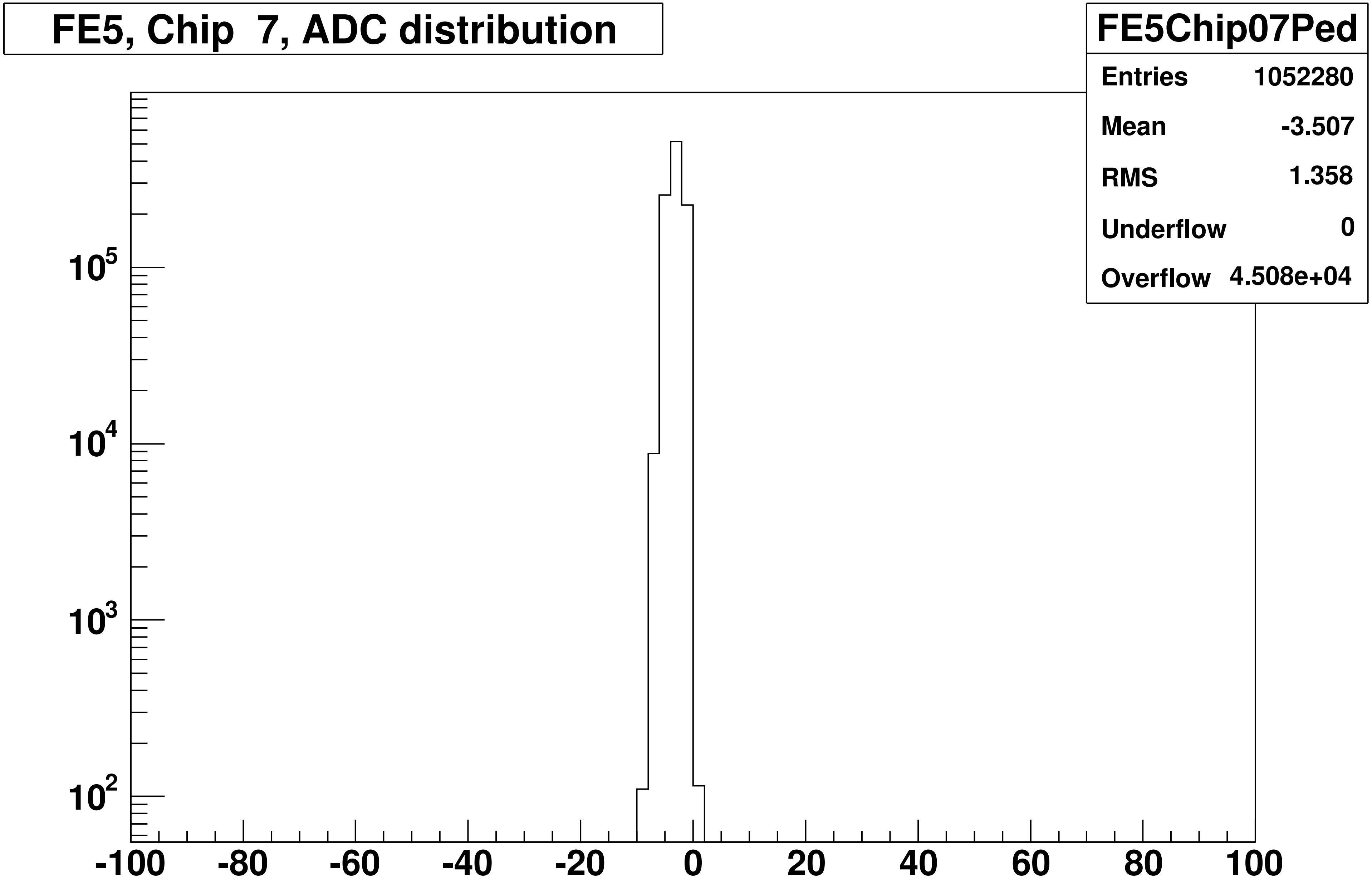
FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 1052280
Mean -3.507
RMS 1.358
Underflow 0
Overflow 4.508e+04
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10^3
10^2
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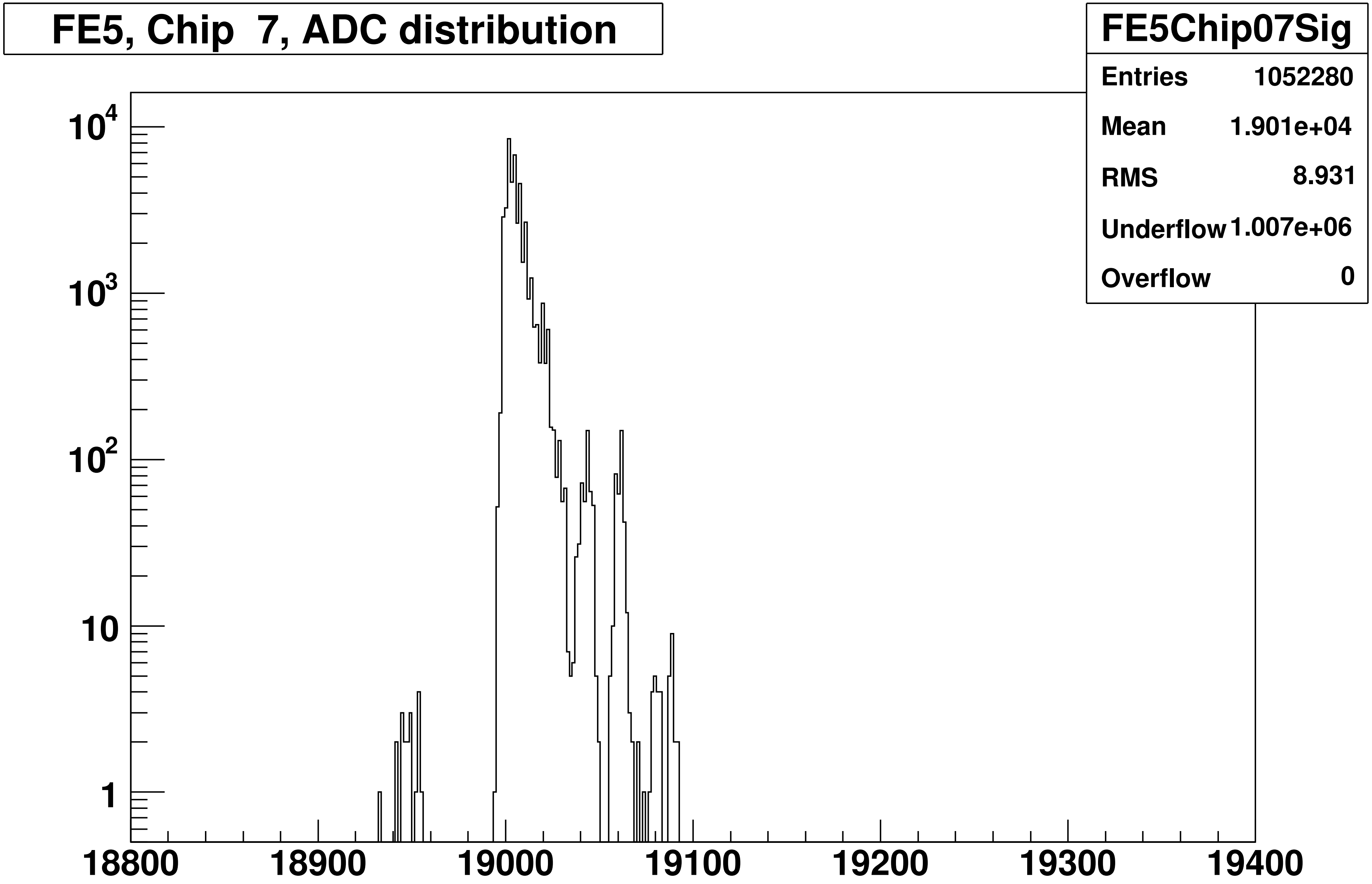
FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 1052280
Mean 1.901e+04
RMS 8.931
Underflow 1.007e+06
Overflow 0
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10^3
10^2
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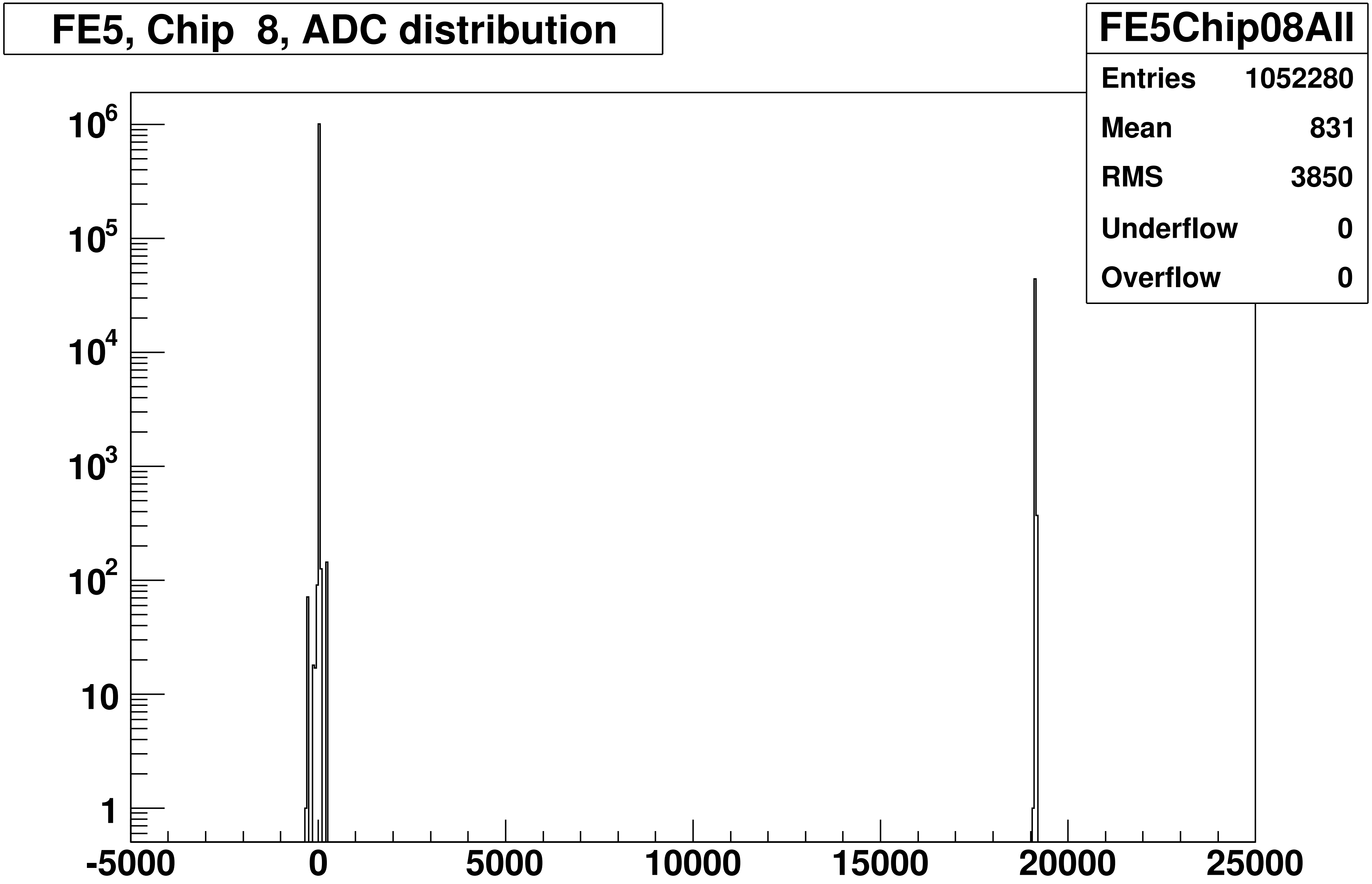
FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 1052280
Mean 831
RMS 3850
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
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0
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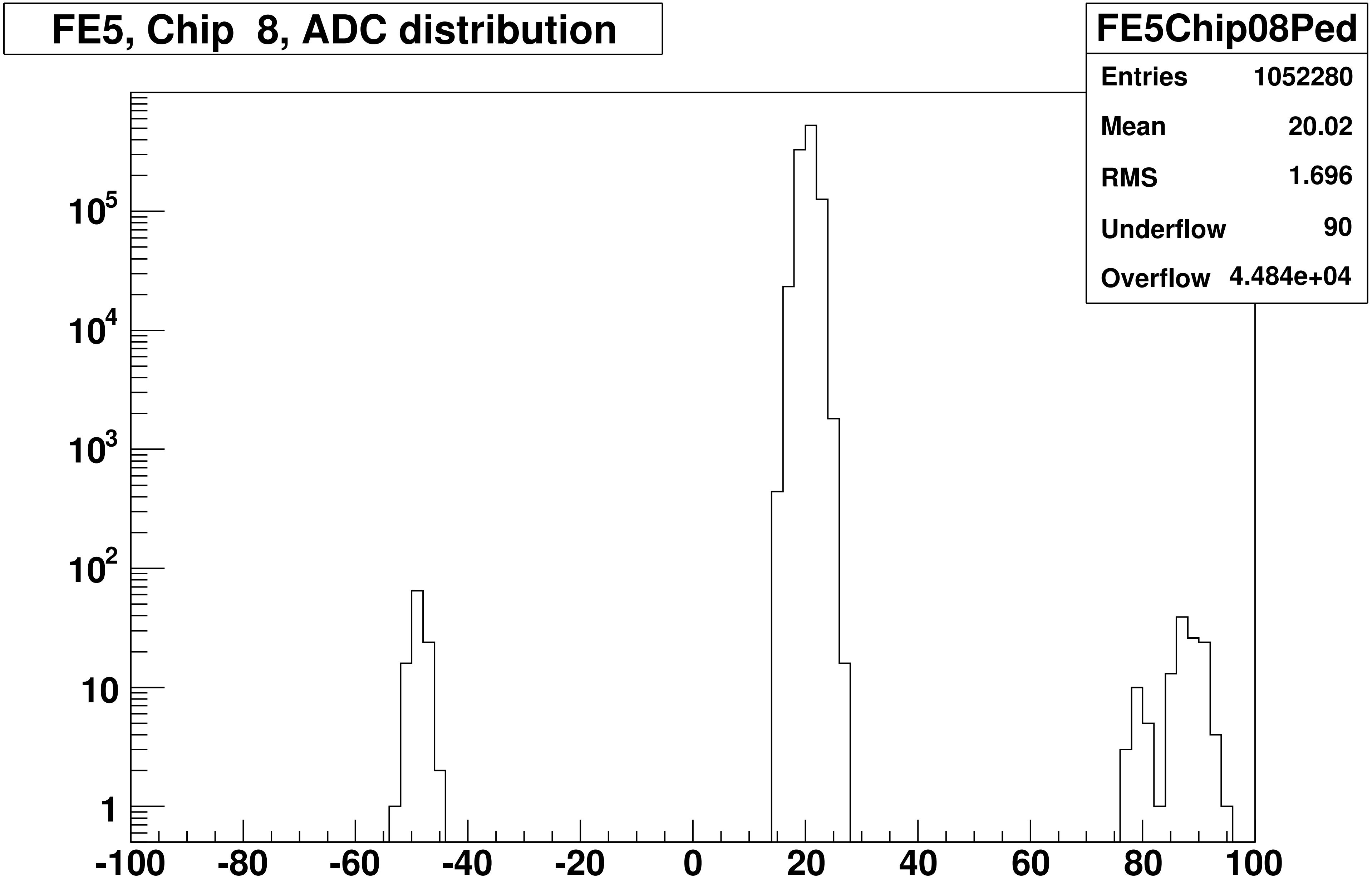

FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 1052280
Mean 20.02
RMS 1.696
Underflow 90
Overflow 4.484e+04
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10^4
10^3
10^2
10
1
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-20
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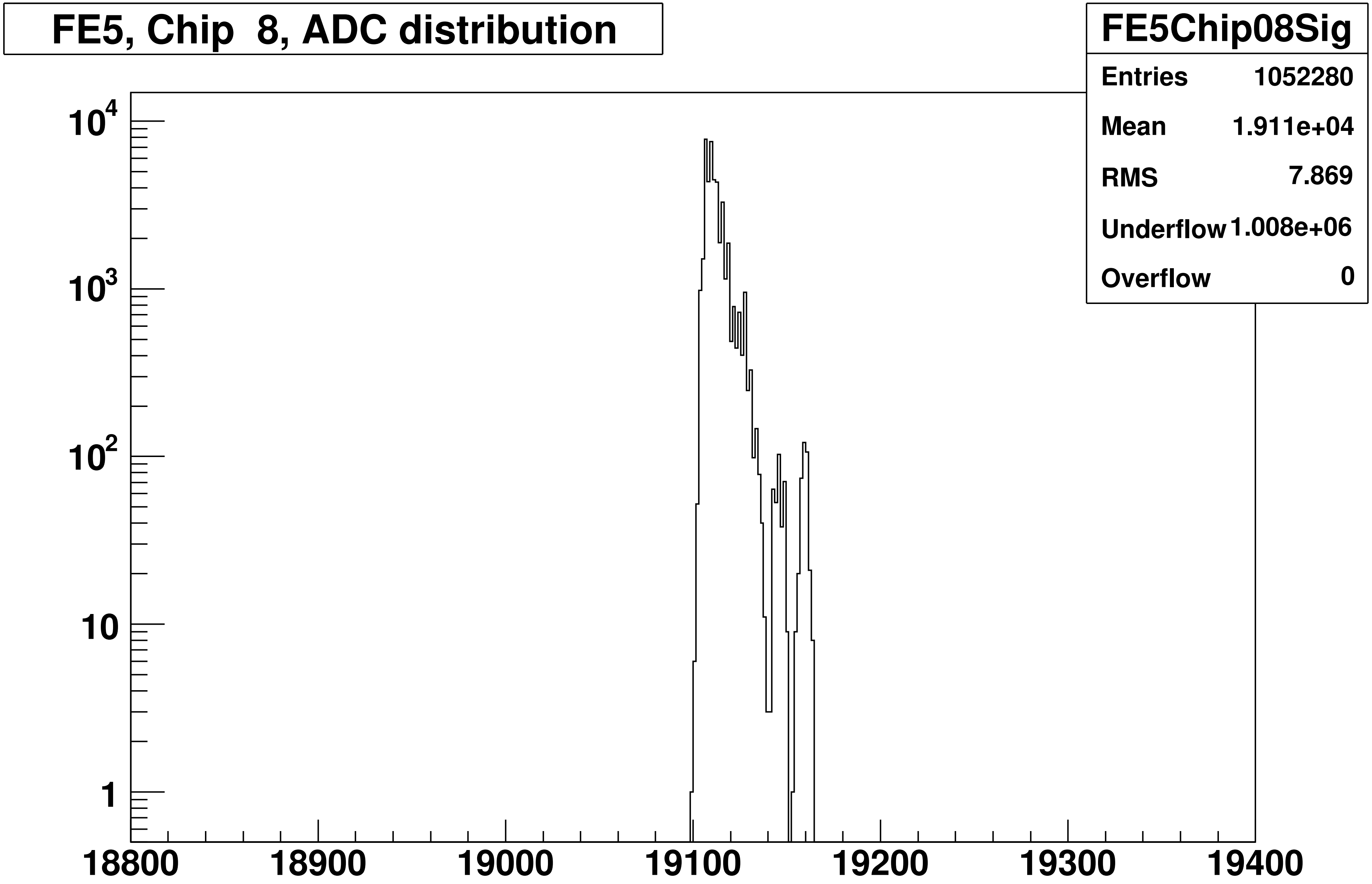

FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 1052280
Mean 1.911e+04
RMS 7.869
Underflow 1.008e+06
Overflow 0
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10^3
10^2
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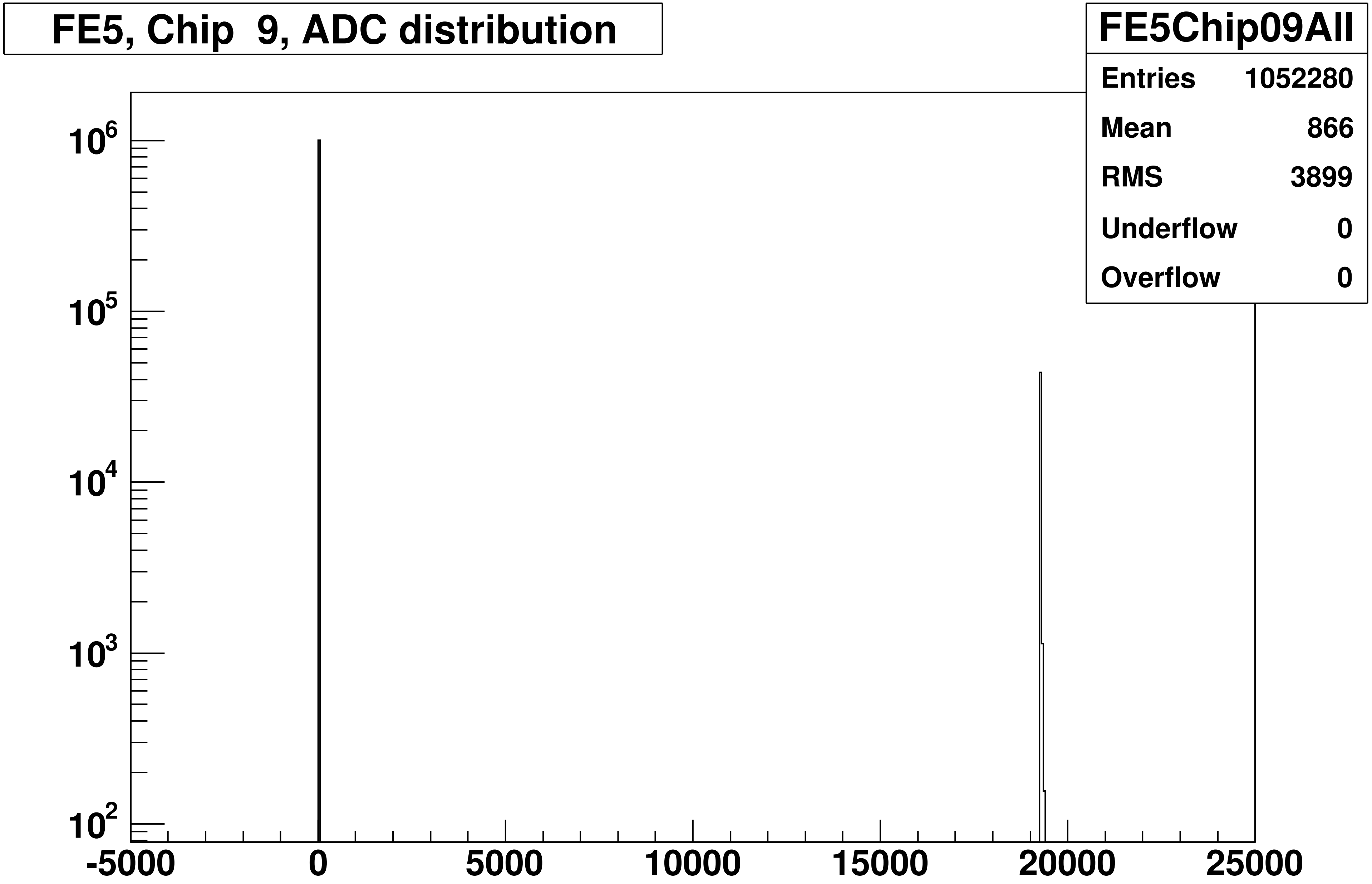
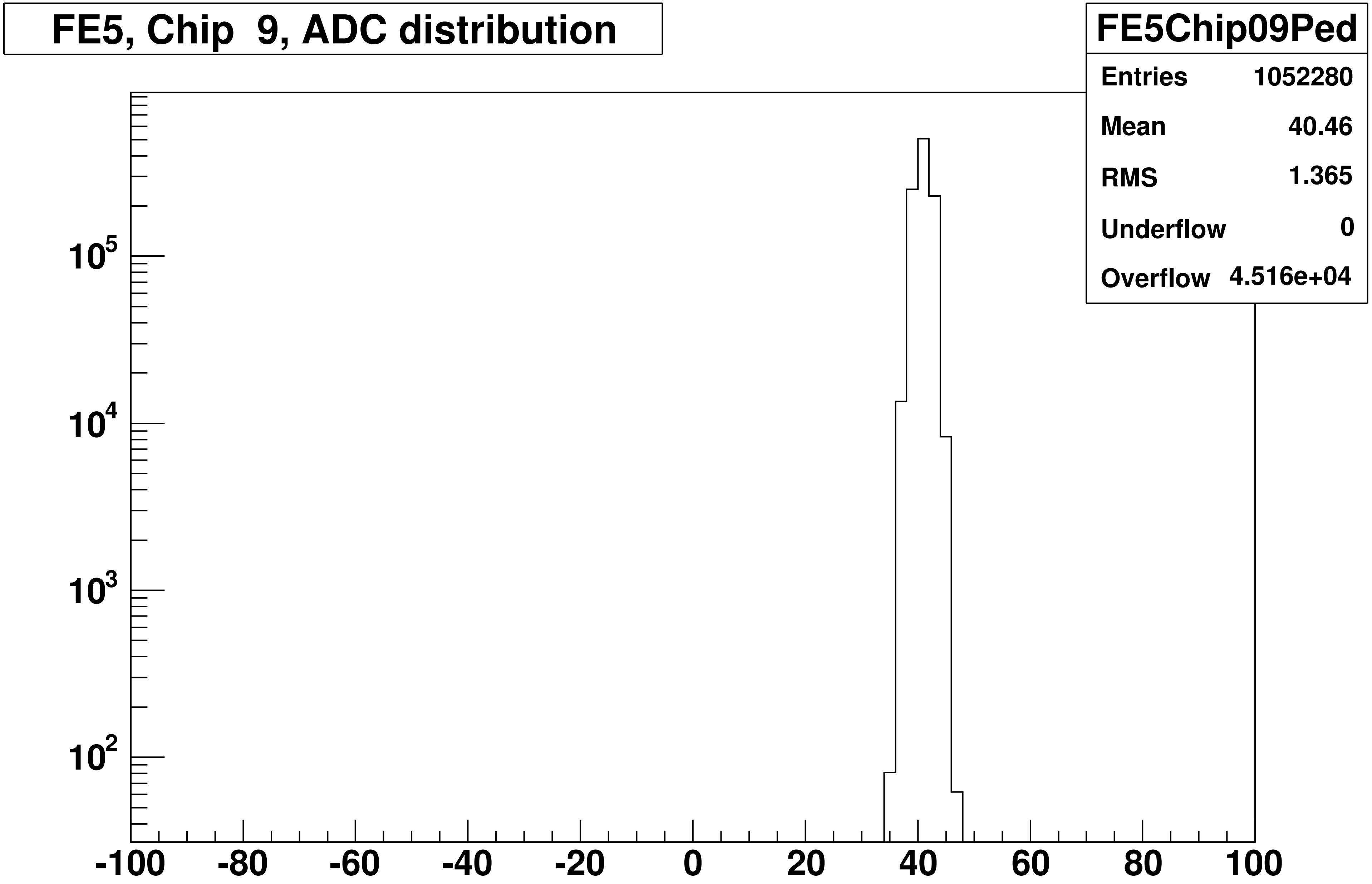


FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 1052280
Mean 866
RMS 3899
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 1052280
Mean 40.46
RMS 1.365
Underflow 0
Overflow 4.516e+04
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10^4
10^3
10^2
-100
-80
-60
-40
-20
0
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40
60
80
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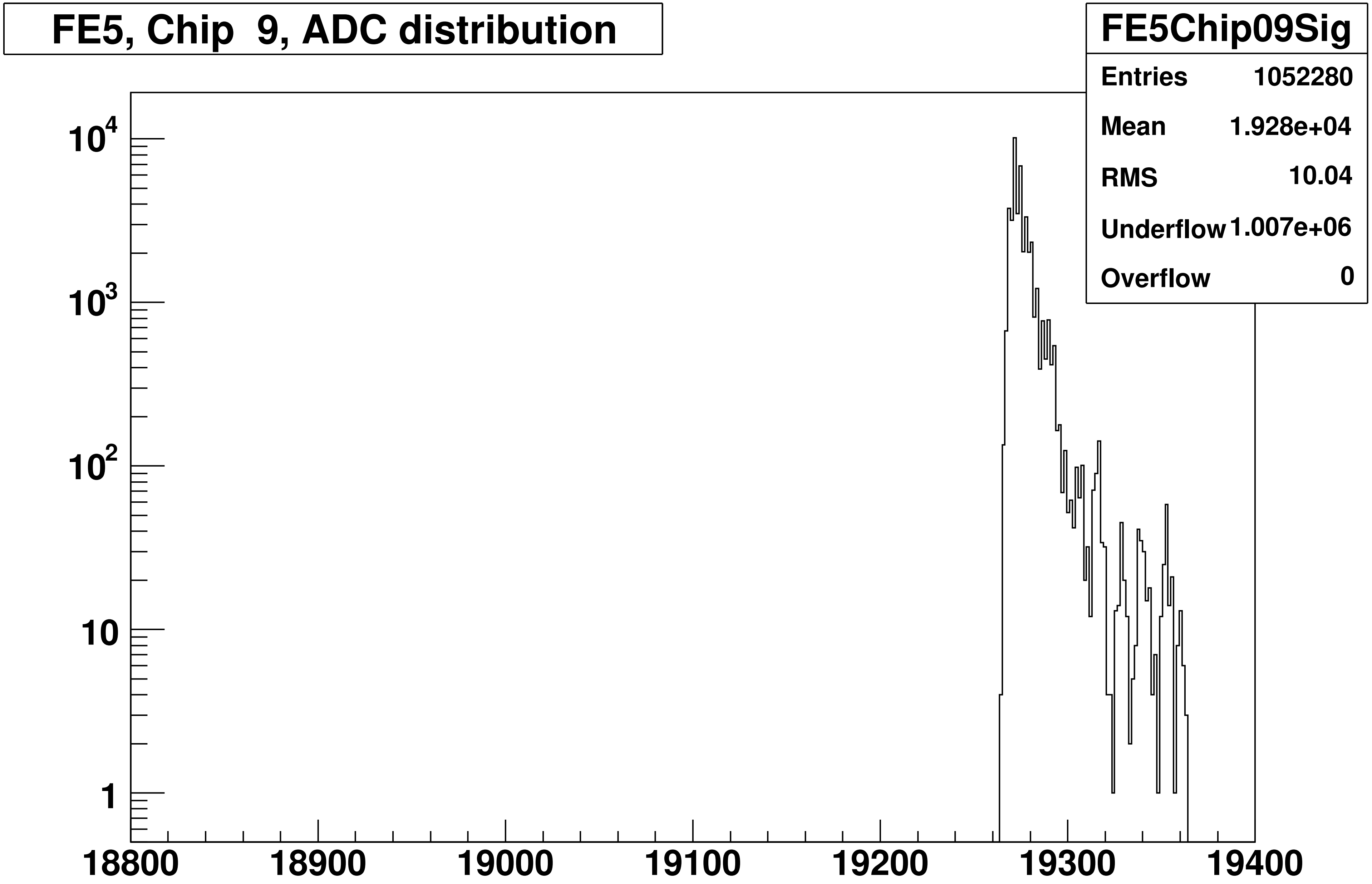

FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 1052280
Mean 1.928e+04
RMS 10.04
Underflow 1.007e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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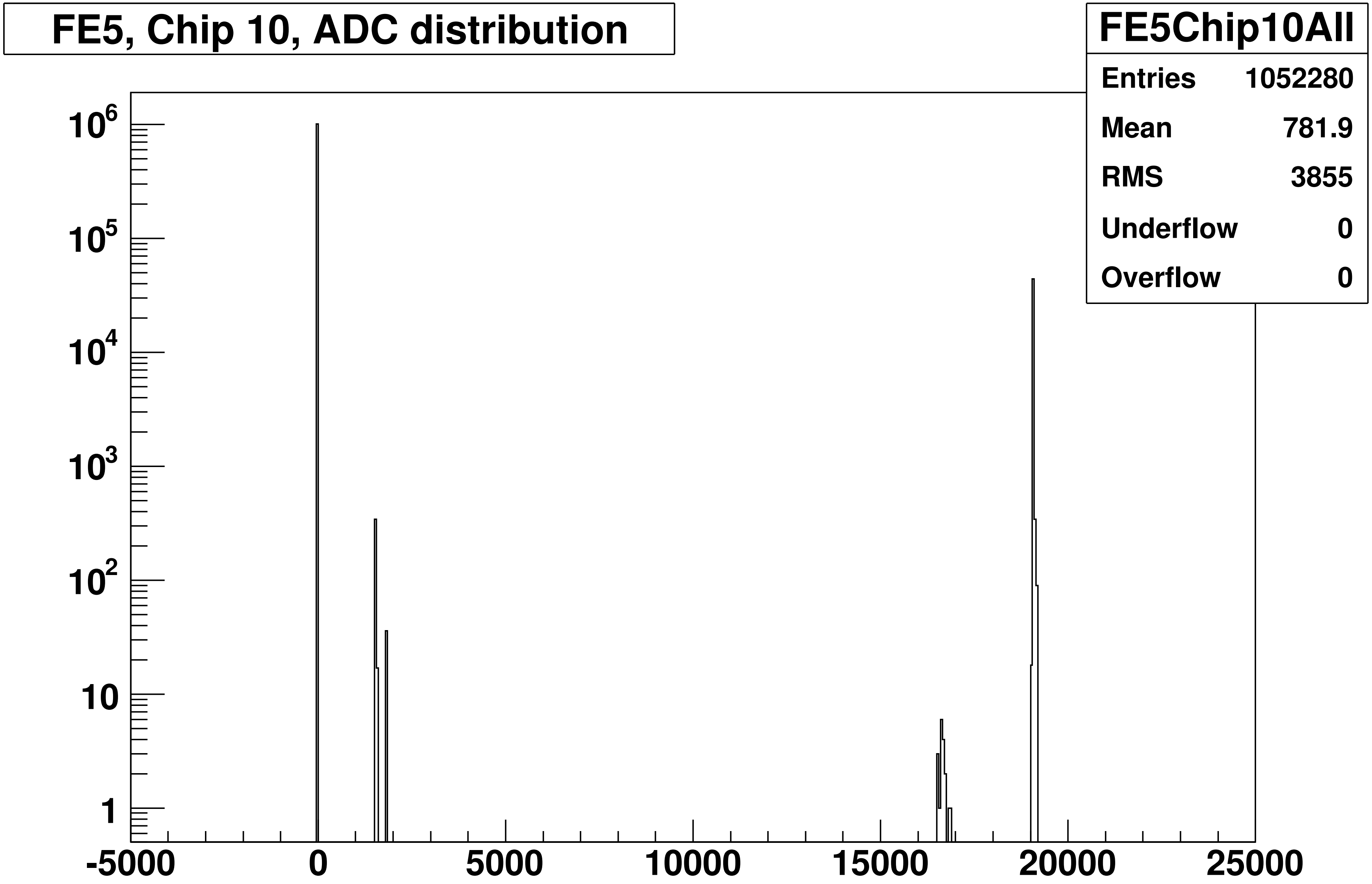

FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 1052280
Mean 781.9
RMS 3855
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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-5000
0
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10000
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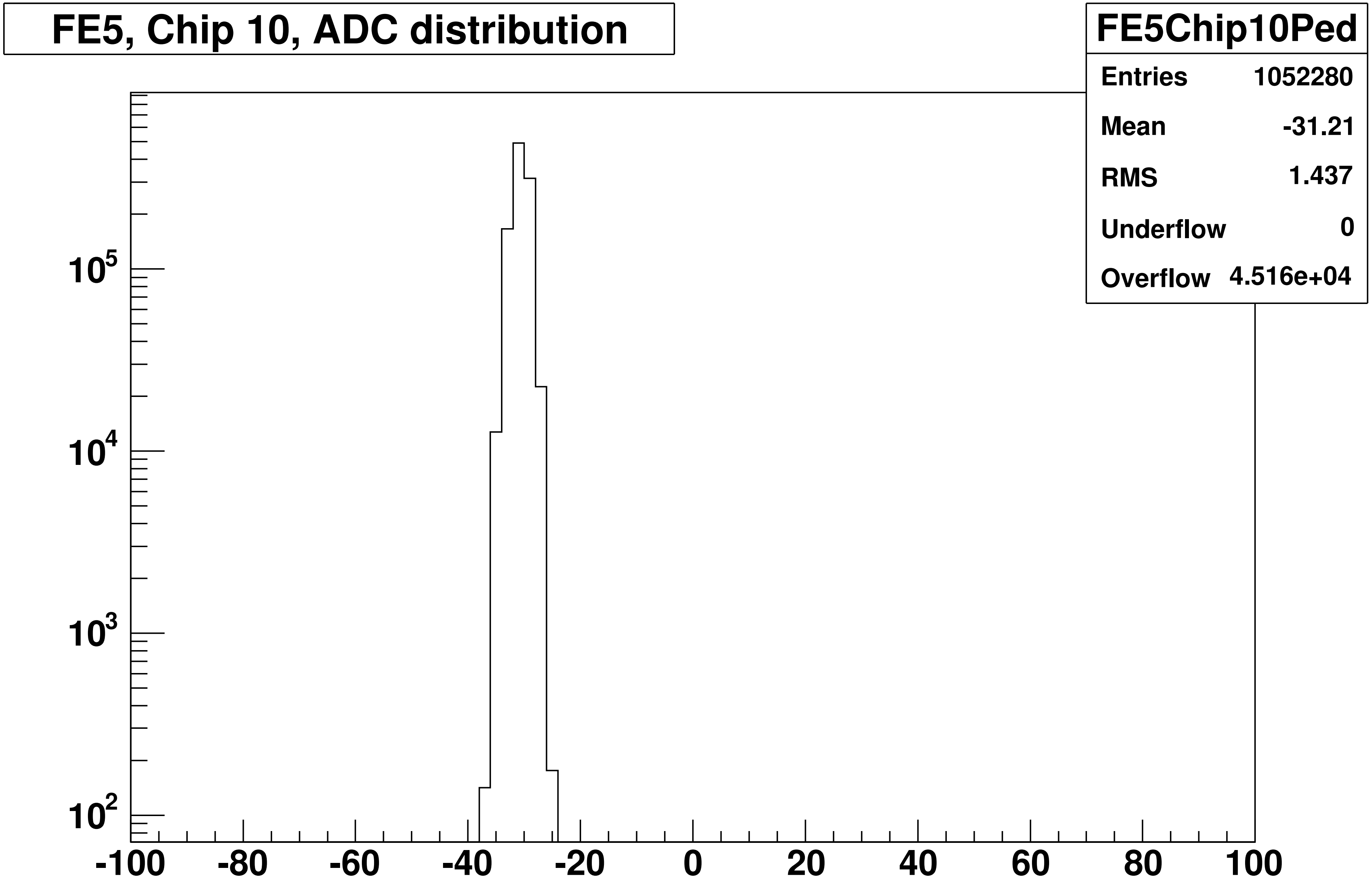
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 1052280
Mean -31.21
RMS 1.437
Underflow 0
Overflow 4.516e+04
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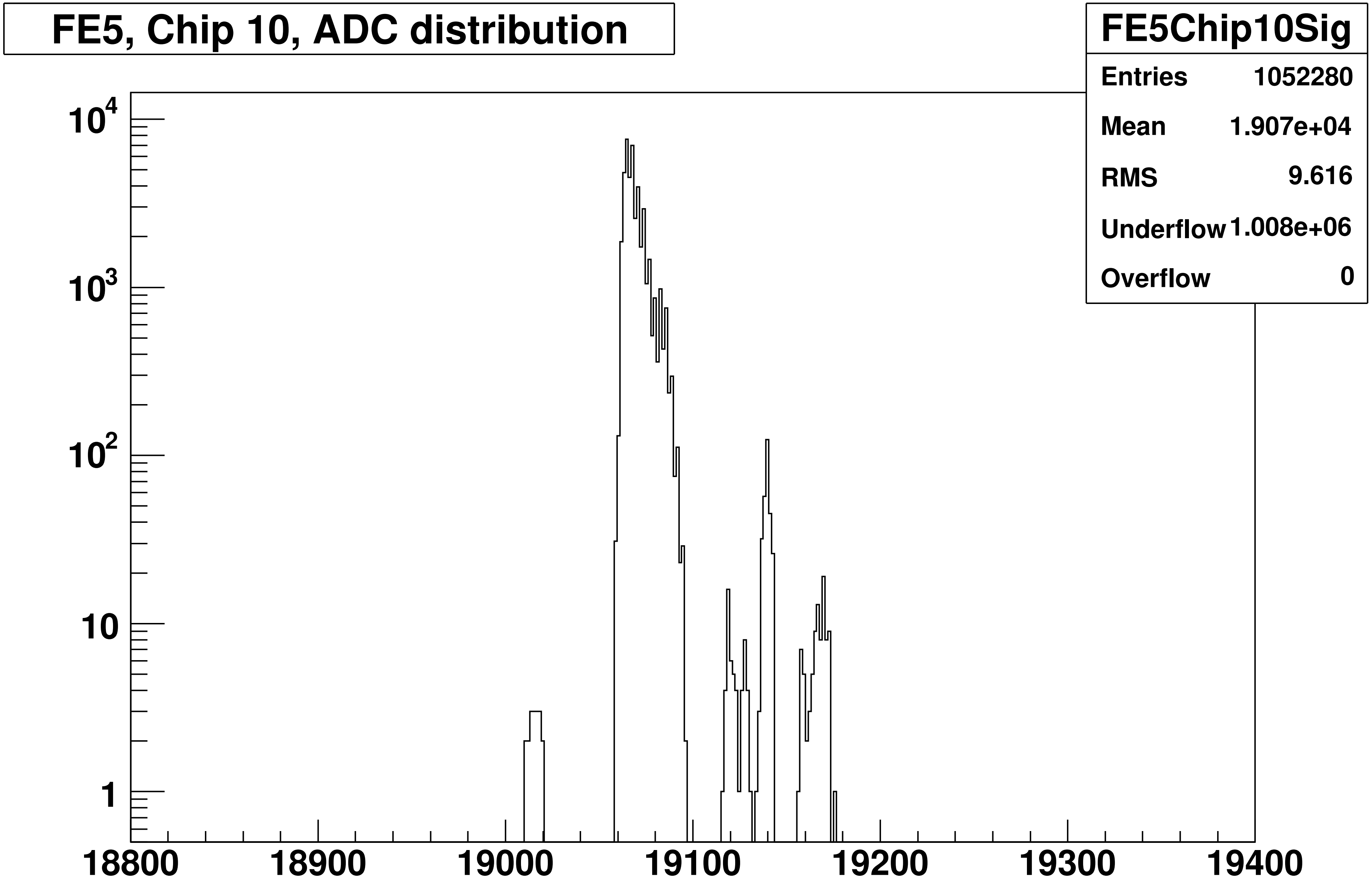
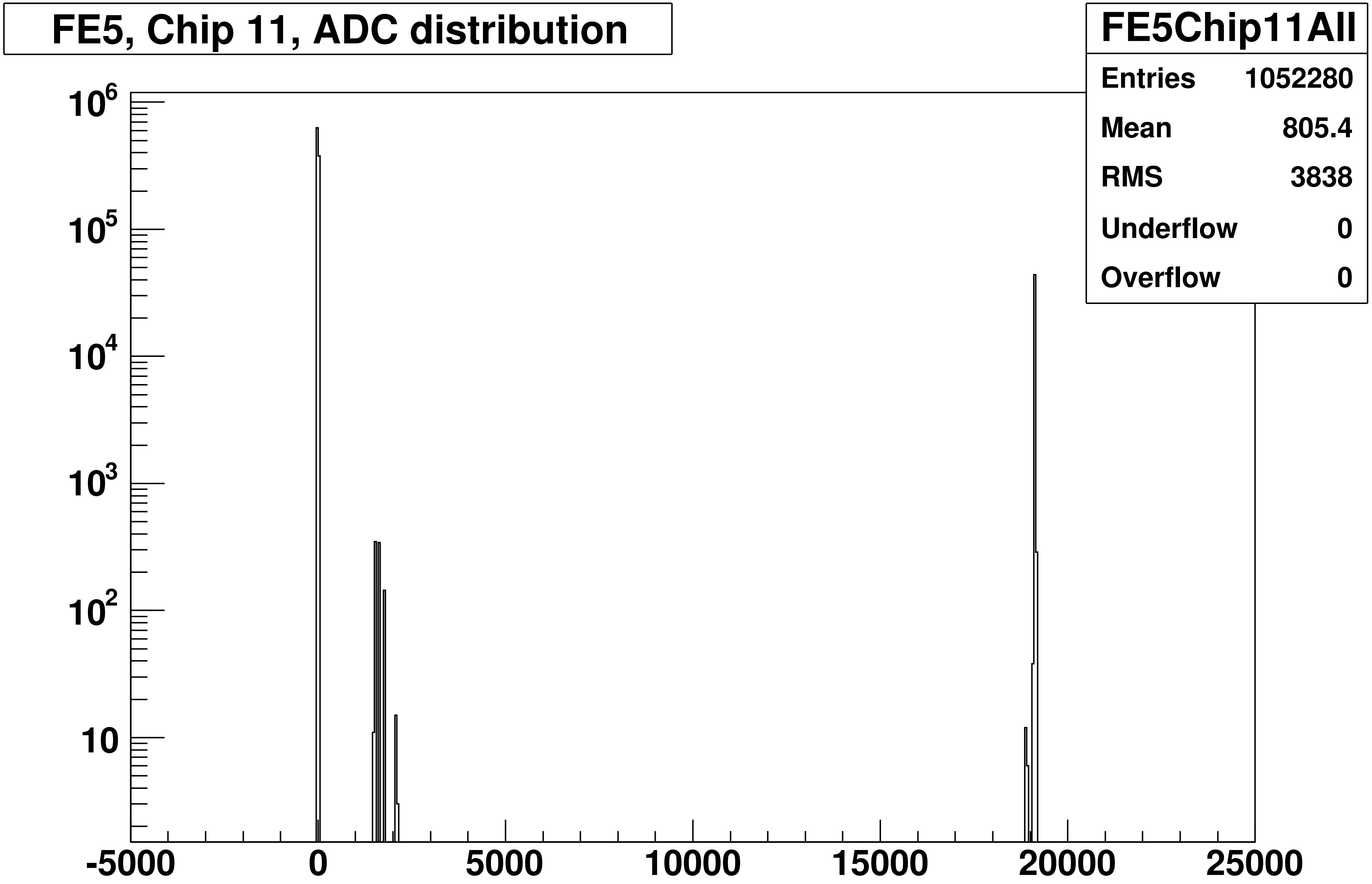
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 1052280
Mean 1.907e+04
RMS 9.616
Underflow 1.008e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 1052280
Mean 805.4
RMS 3838
Underflow 0
Overflow 0
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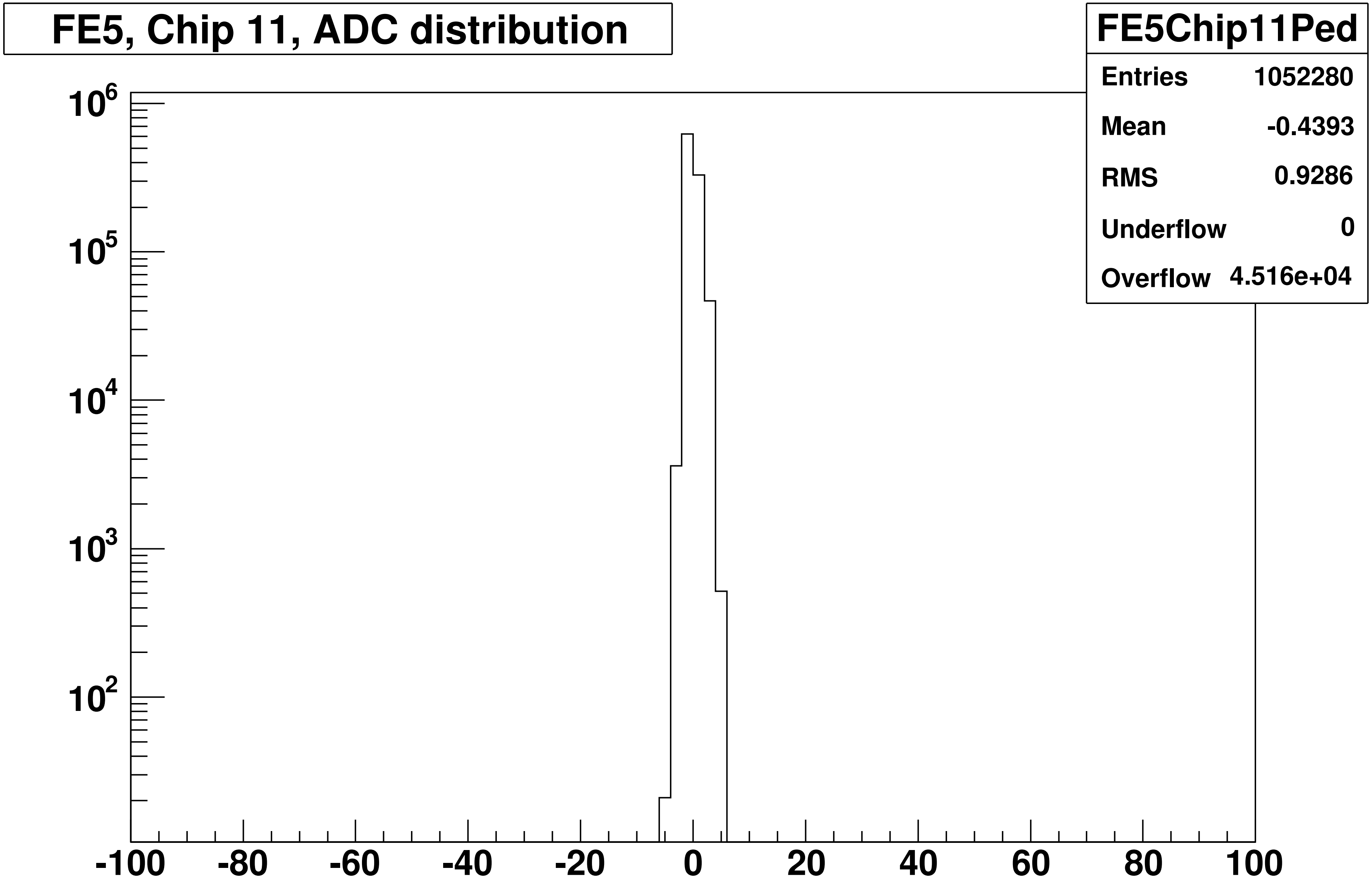
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 1052280
Mean -0.4393
RMS 0.9286
Underflow 0
Overflow 4.516e+04
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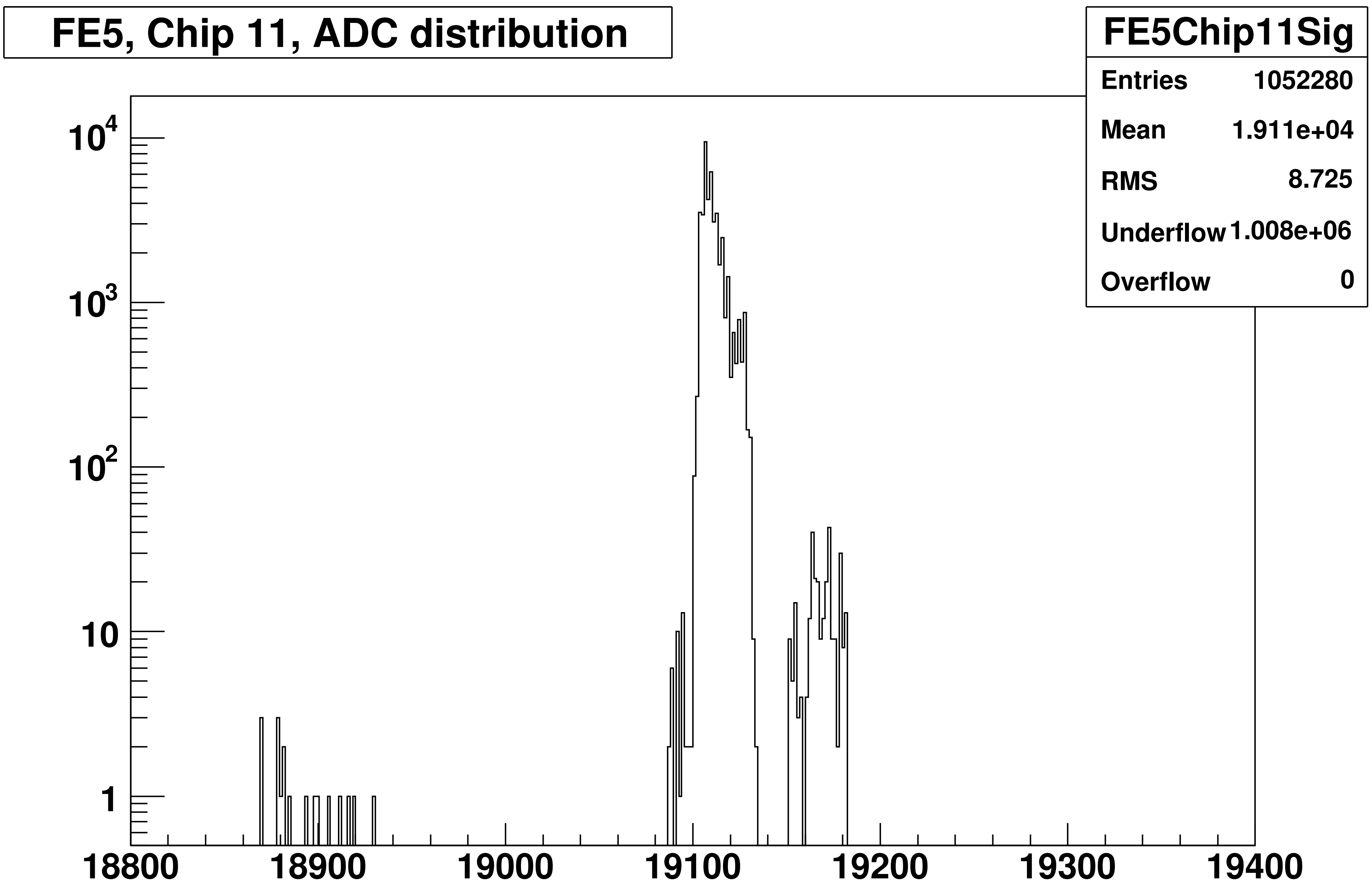
FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 1052280
Mean 1.911e+04
RMS 8.725
Underflow 1.008e+06
Overflow 0
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10^3
10^2
10
1
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18900
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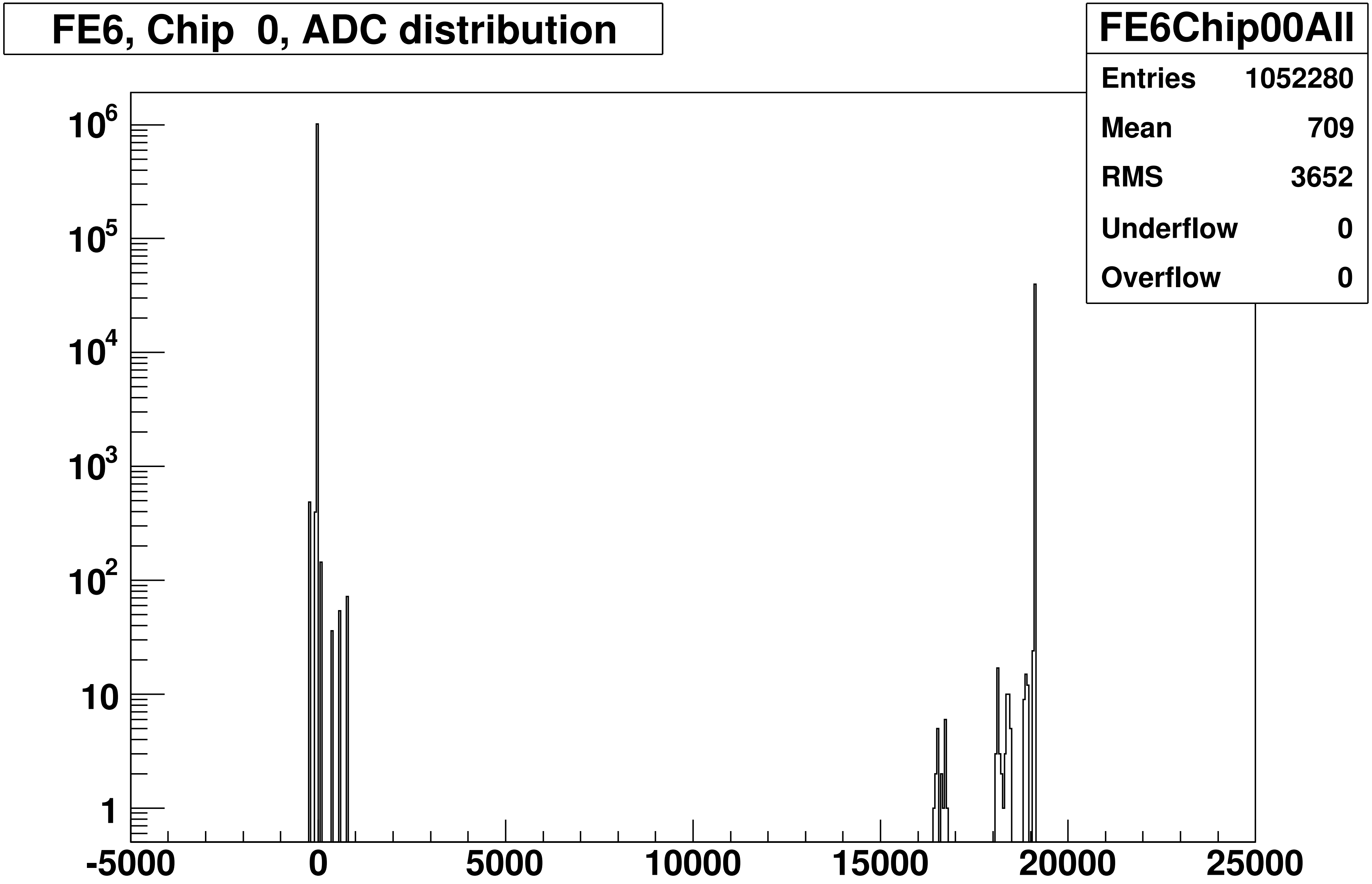
19200
19300
19400


FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 1052280
Mean 709
RMS 3652
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
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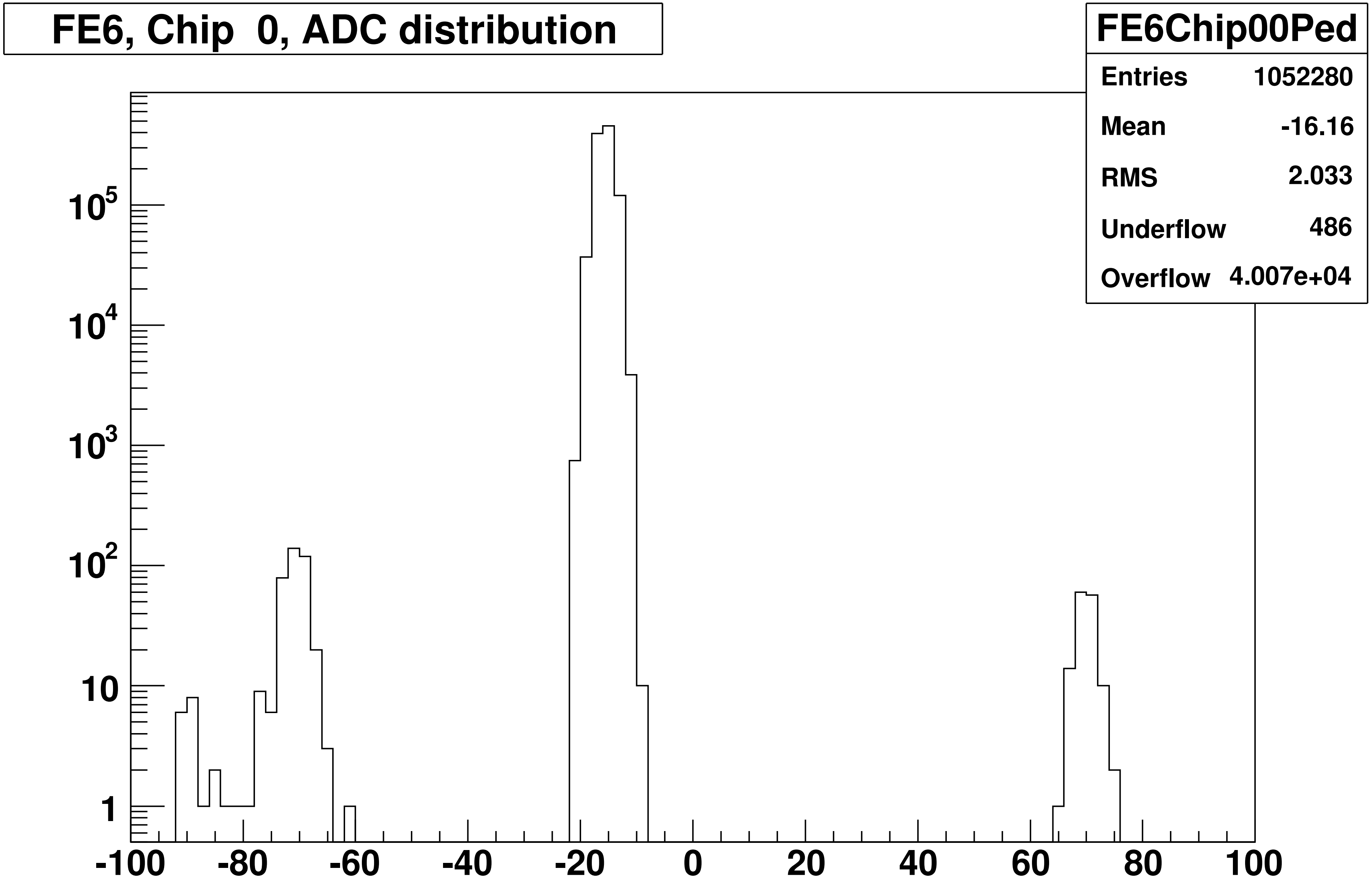
10000
15000
20000
25000



FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 1052280
Mean -16.16
RMS 2.033
Underflow 486
Overflow 4.007e+04
10^5
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10^3
10^2
10
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80
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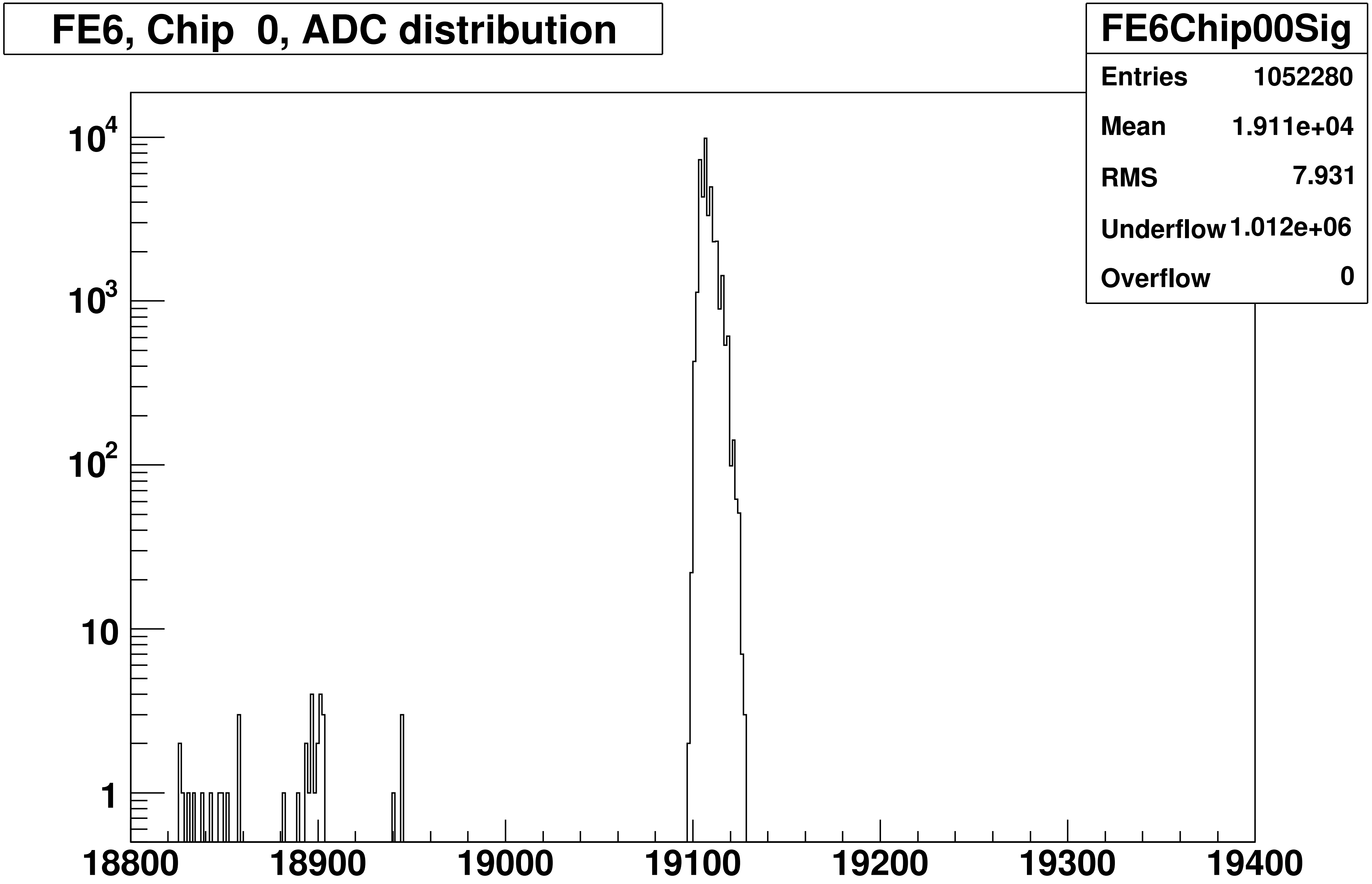
FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 1052280
Mean 1.911e+04
RMS 7.931
Underflow 1.012e+06
Overflow 0
10^4
10^3
10^2
10
1
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18900
19000
19100
19200
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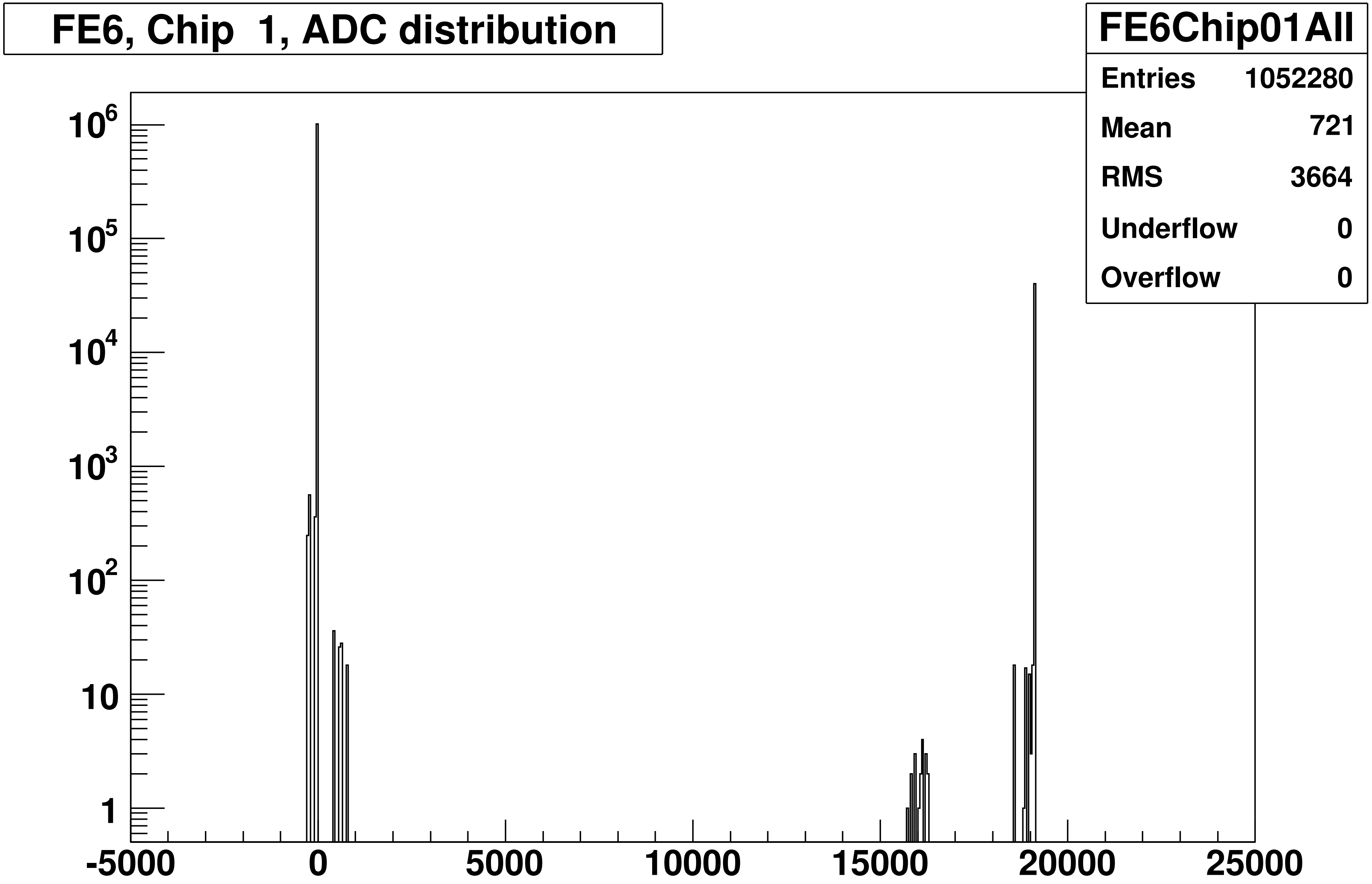
19400


FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 1052280
Mean 721
RMS 3664
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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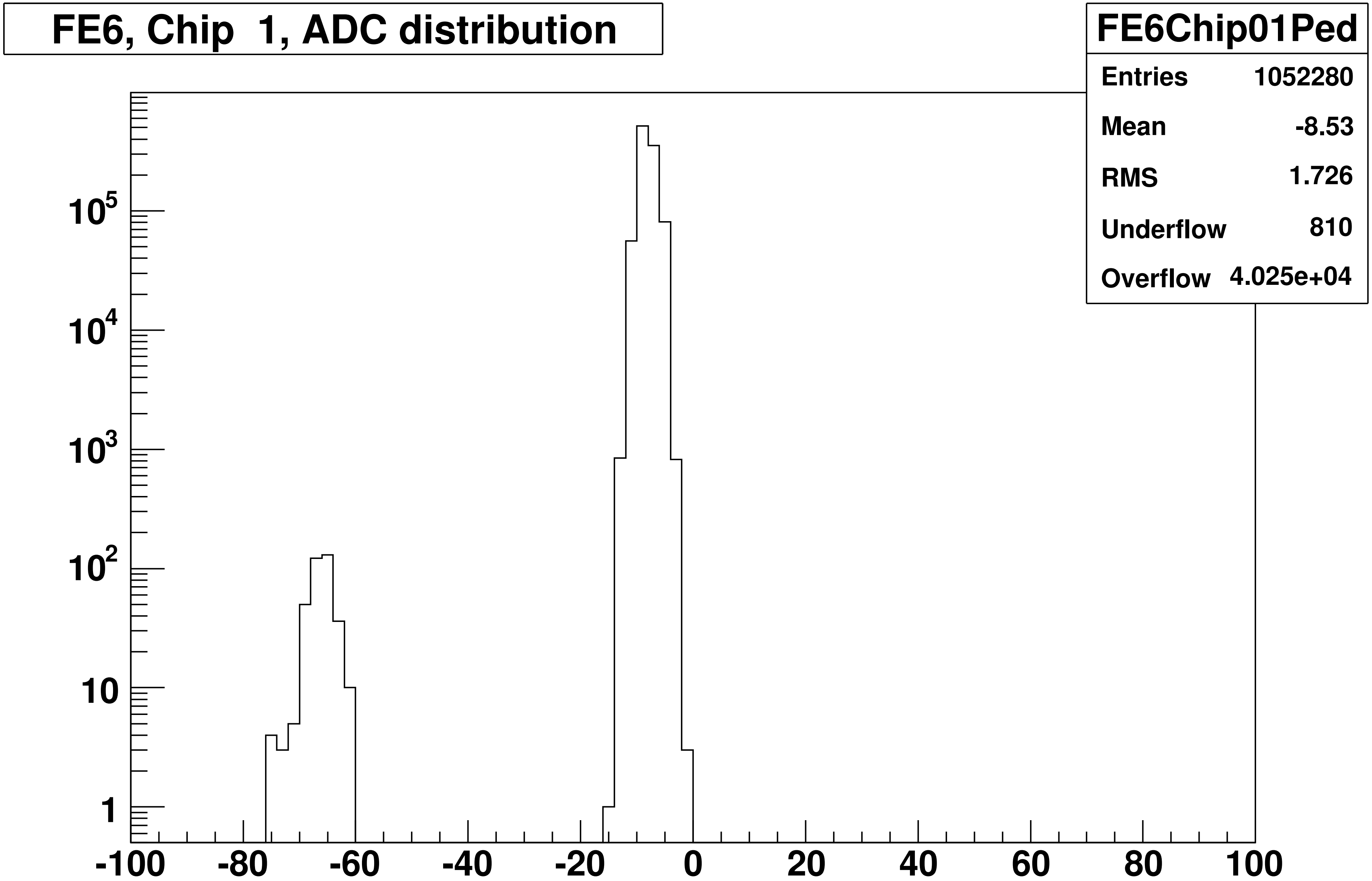
25000



FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 1052280
Mean -8.53
RMS 1.726
Underflow 810
Overflow 4.025e+04
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10^4
10^3
10^2
10
1
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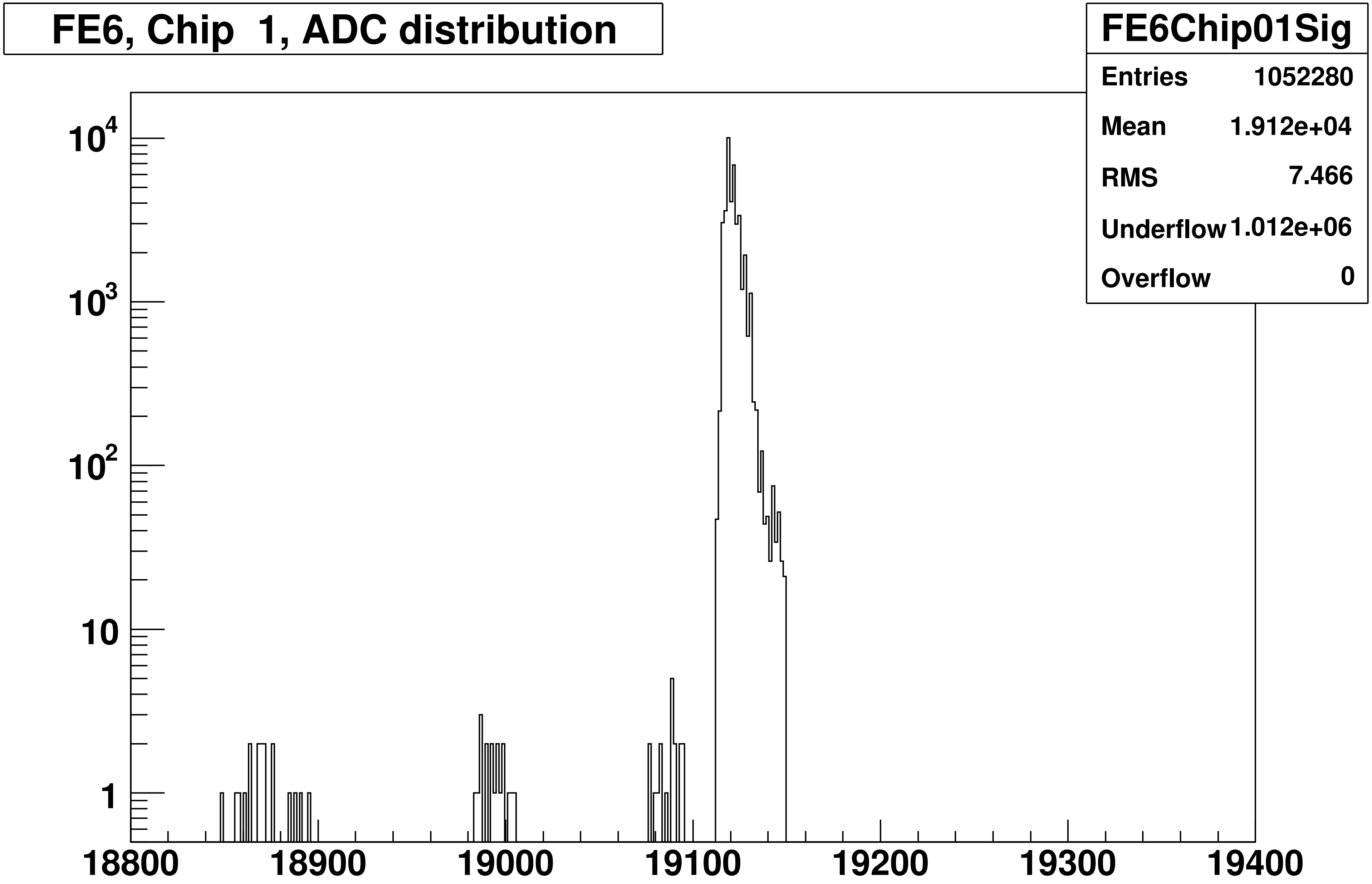

FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 1052280
Mean 1.912e+04
RMS 7.466
Underflow 1.012e+06
Overflow 0
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10^3
10^2
10
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18900
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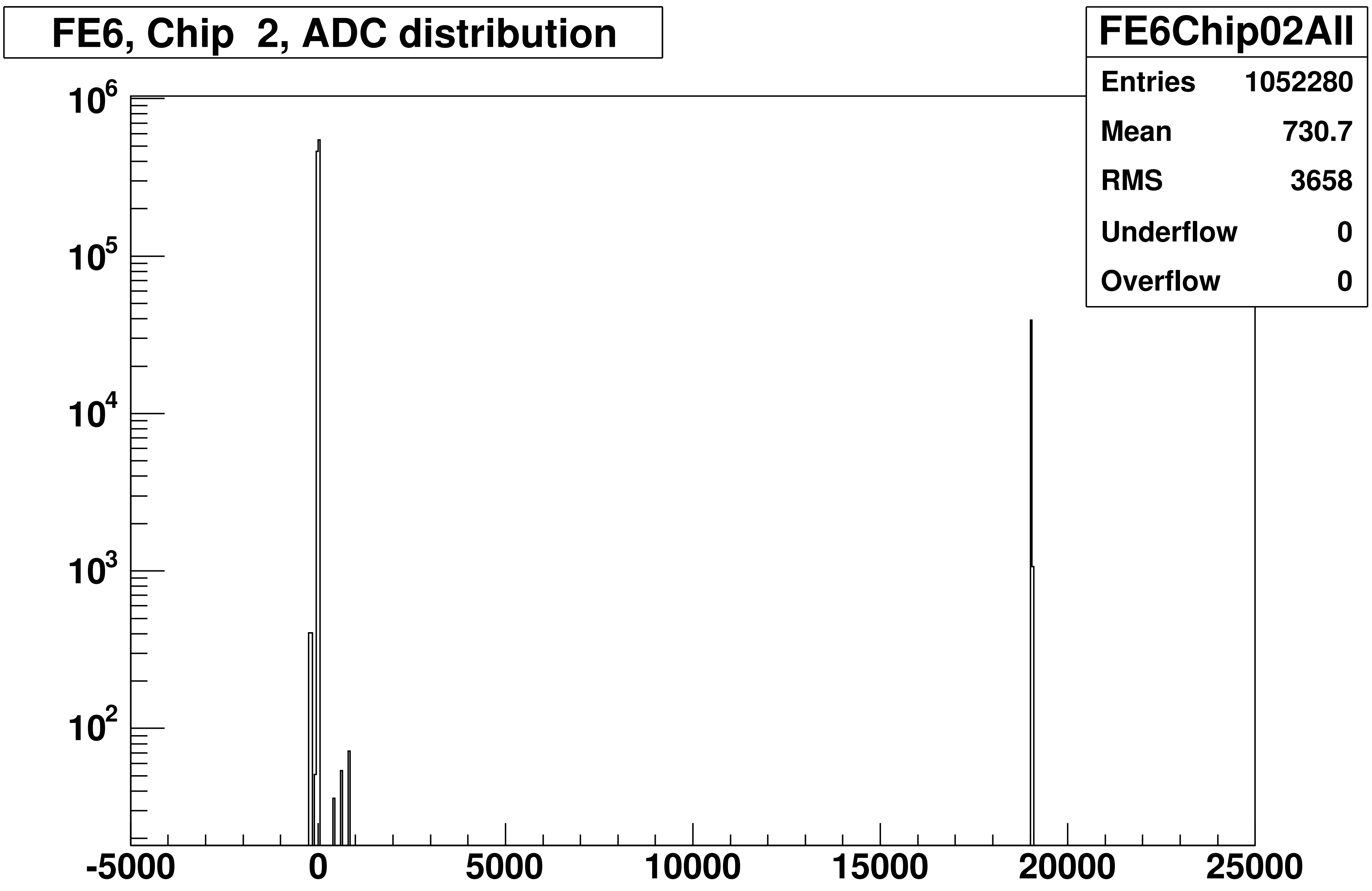

FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 1052280
Mean 730.7
RMS 3658
Underflow 0
Overflow 0
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10^5
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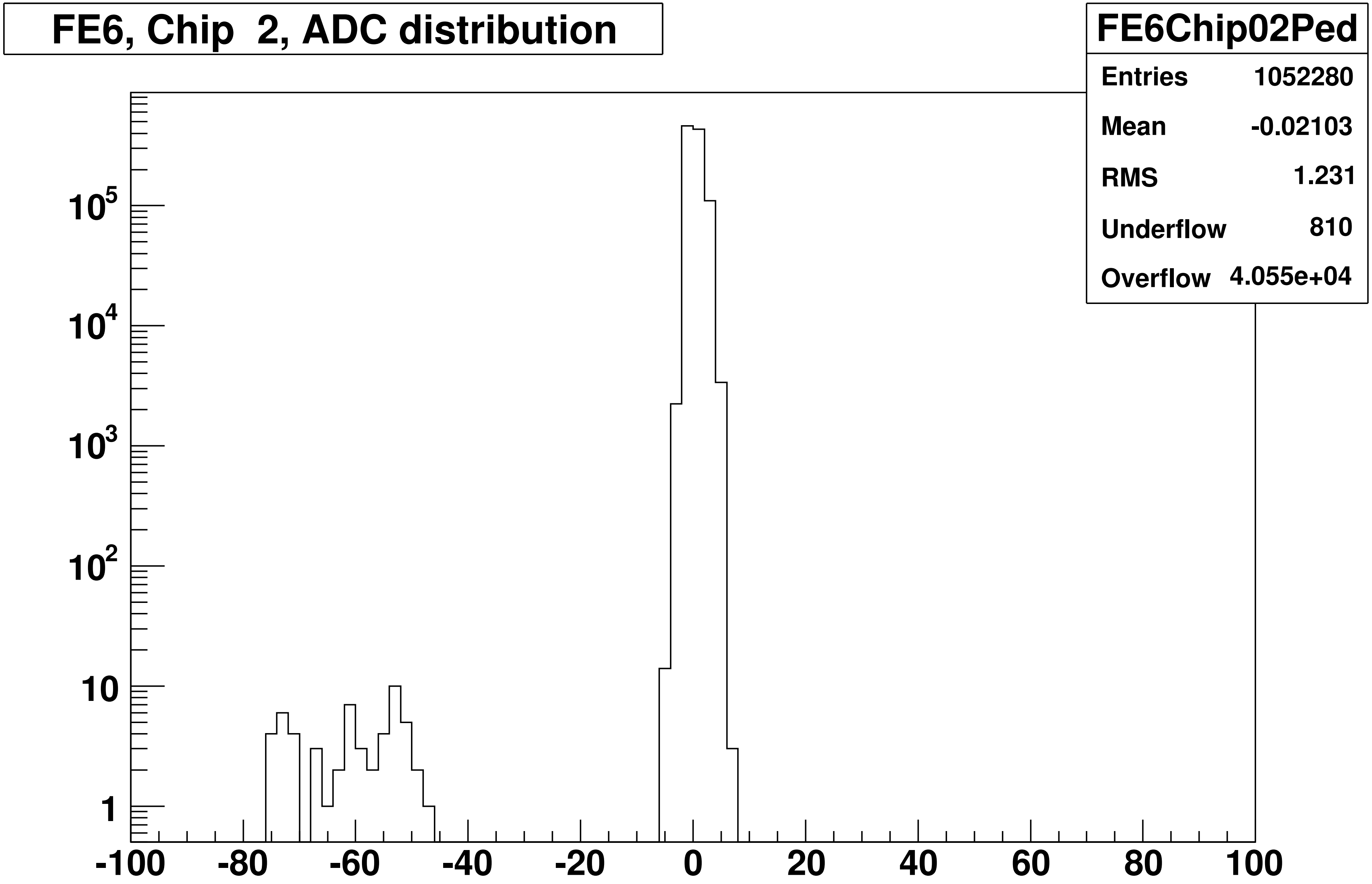
FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 1052280
Mean -0.02103
RMS 1.231
Underflow 810
Overflow 4.055e+04
10^5
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10^3
10^2
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1
-100
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80
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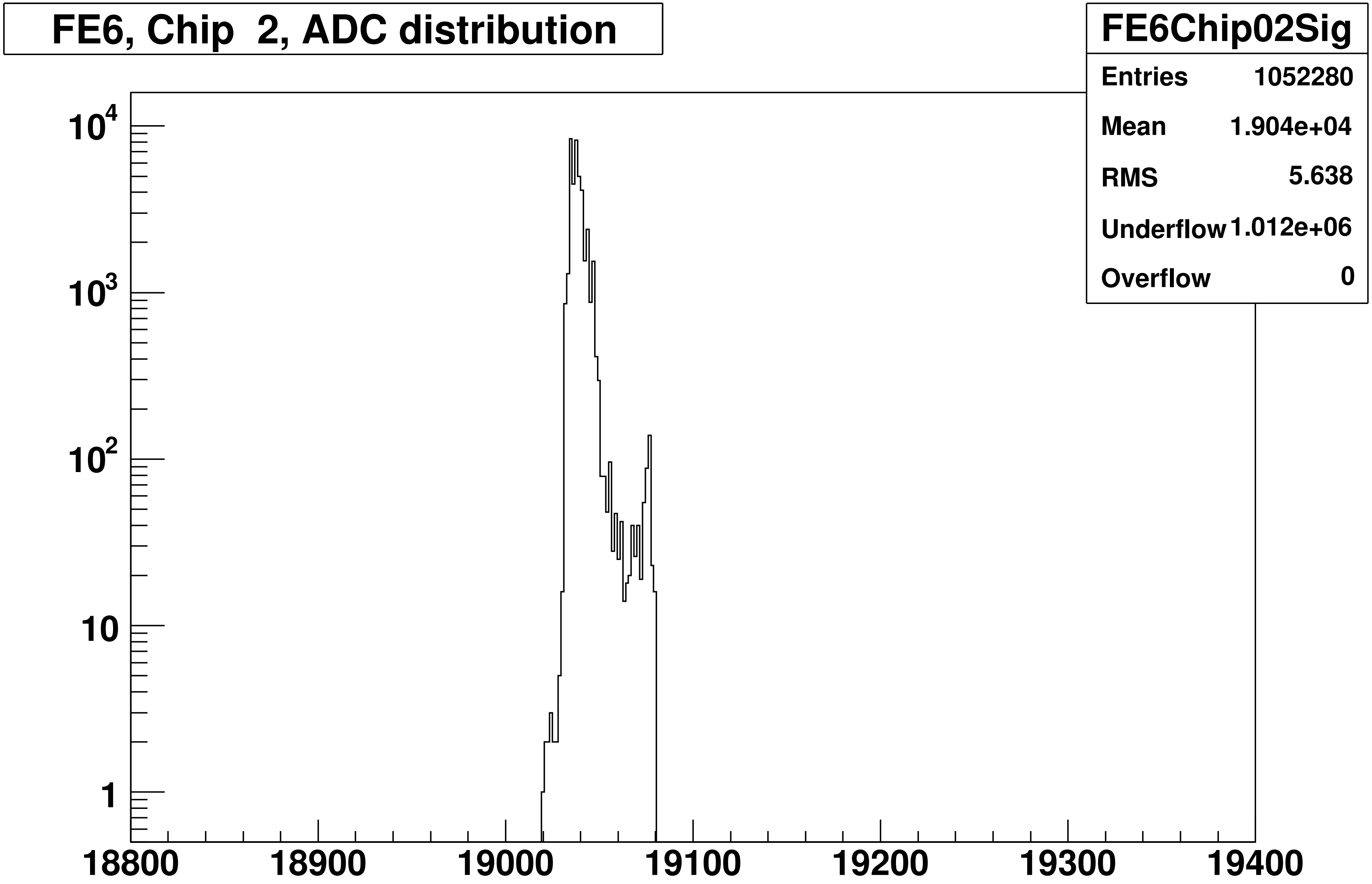

FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 1052280
Mean 1.904e+04
RMS 5.638
Underflow 1.012e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
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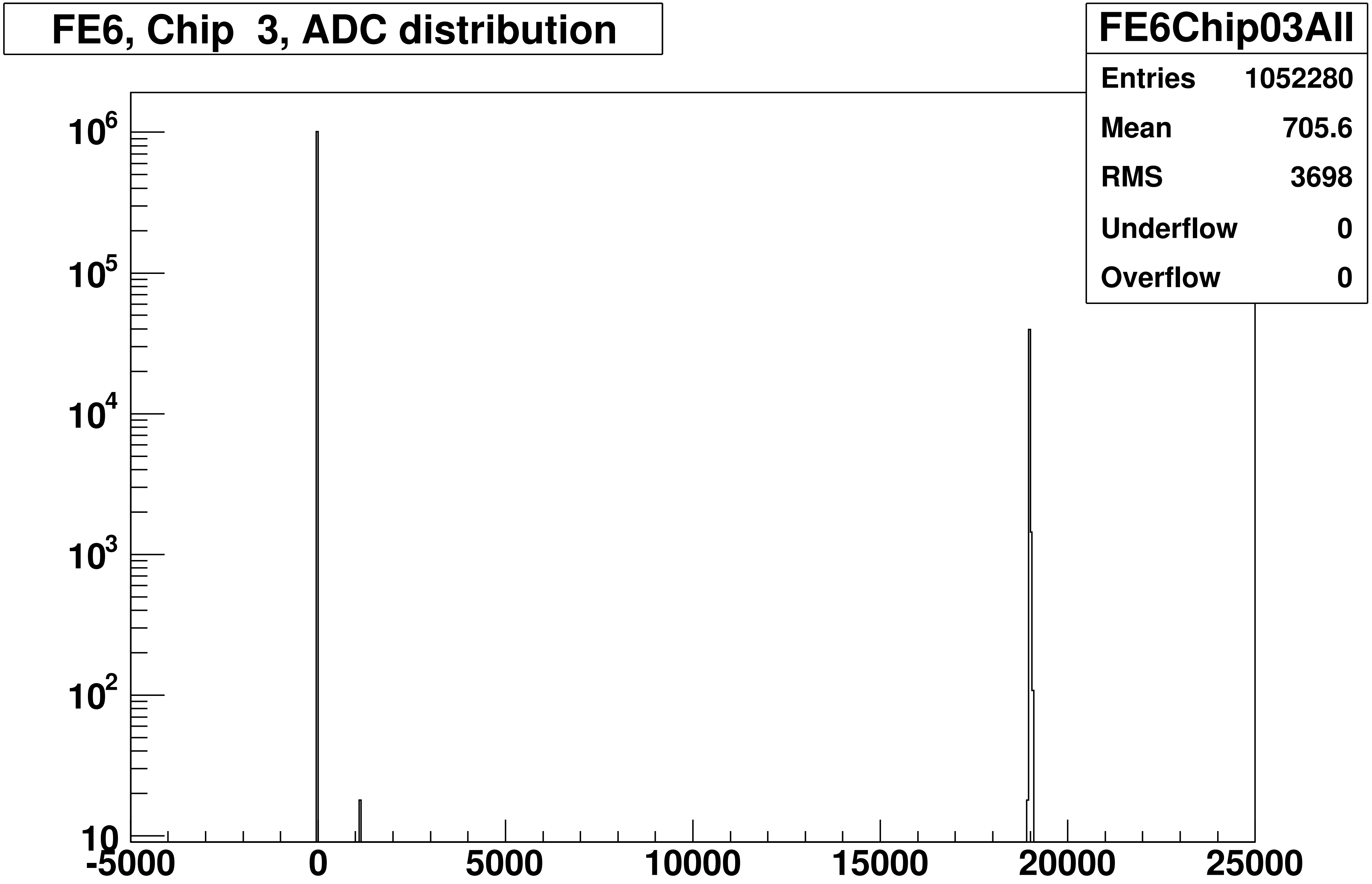

FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 1052280
Mean 705.6
RMS 3698
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
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5000
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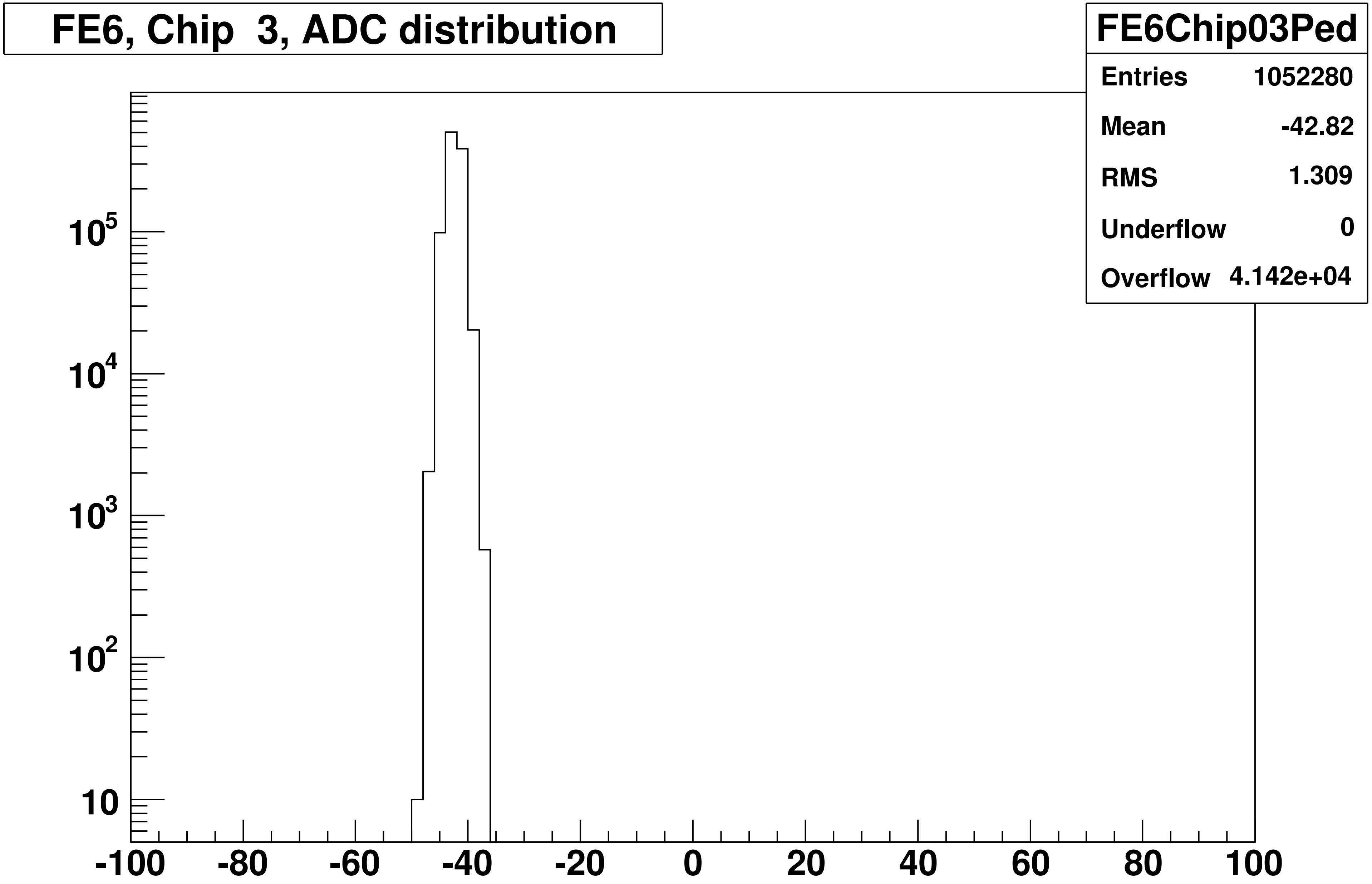
20000
25000


FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 1052280
Mean -42.82
RMS 1.309
Underflow 0
Overflow 4.142e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
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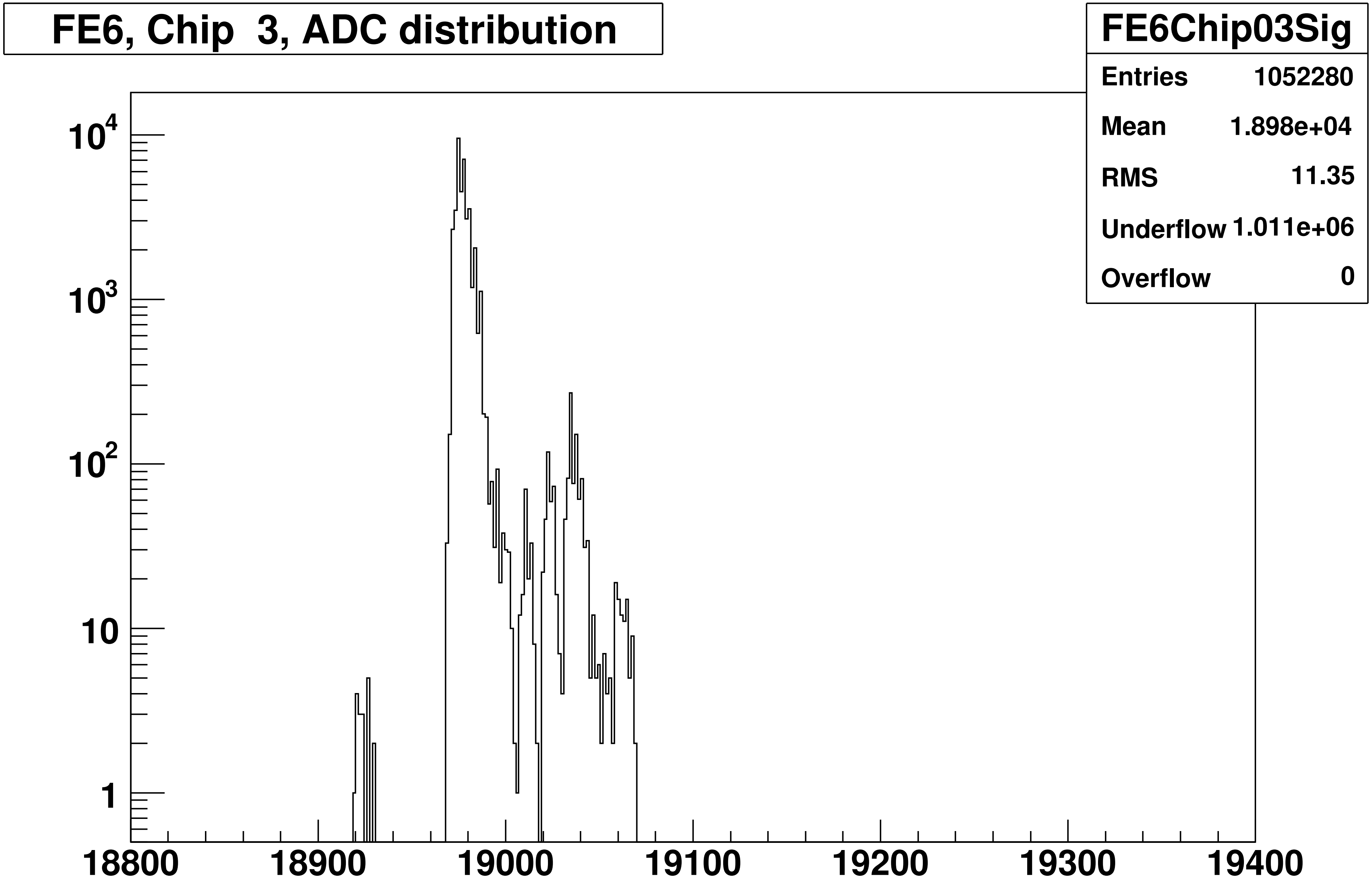
40
60
80
100



FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 1052280
Mean 1.898e+04
RMS 11.35
Underflow 1.011e+06
Overflow 0
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10^3
10^2
10
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18900
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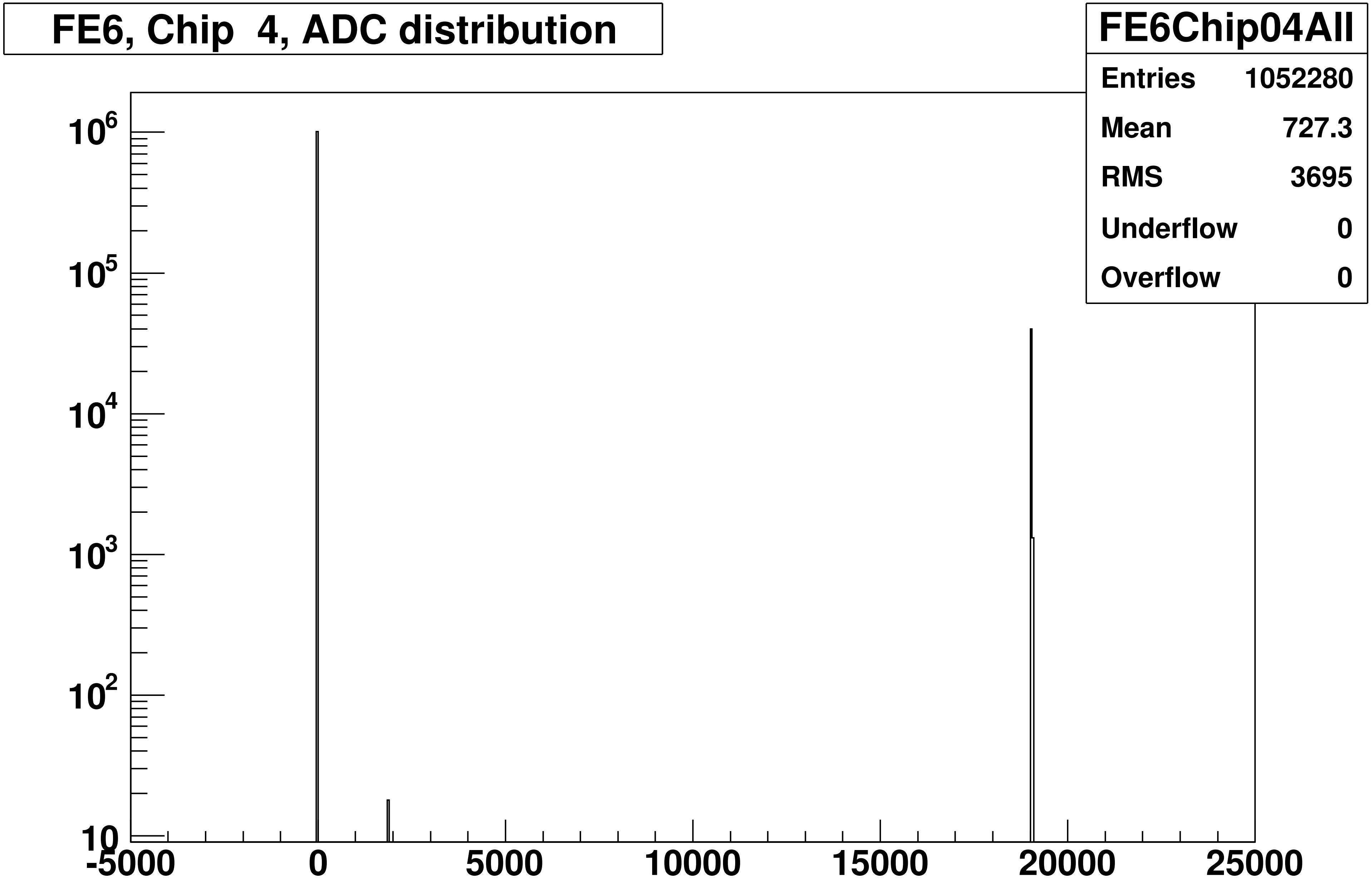

FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 1052280
Mean 727.3
RMS 3695
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
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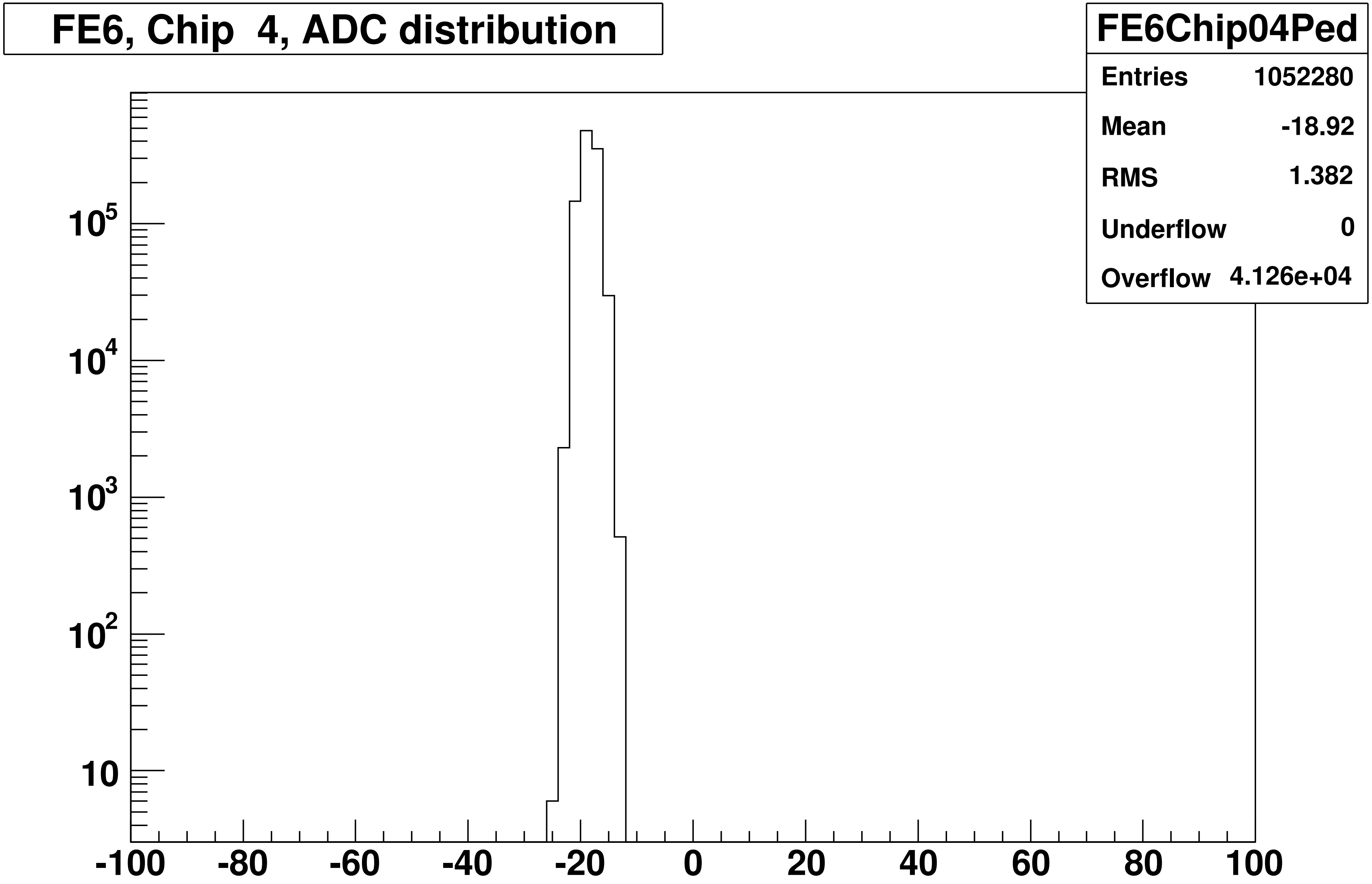
20000
25000



FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 1052280
Mean -18.92
RMS 1.382
Underflow 0
Overflow 4.126e+04
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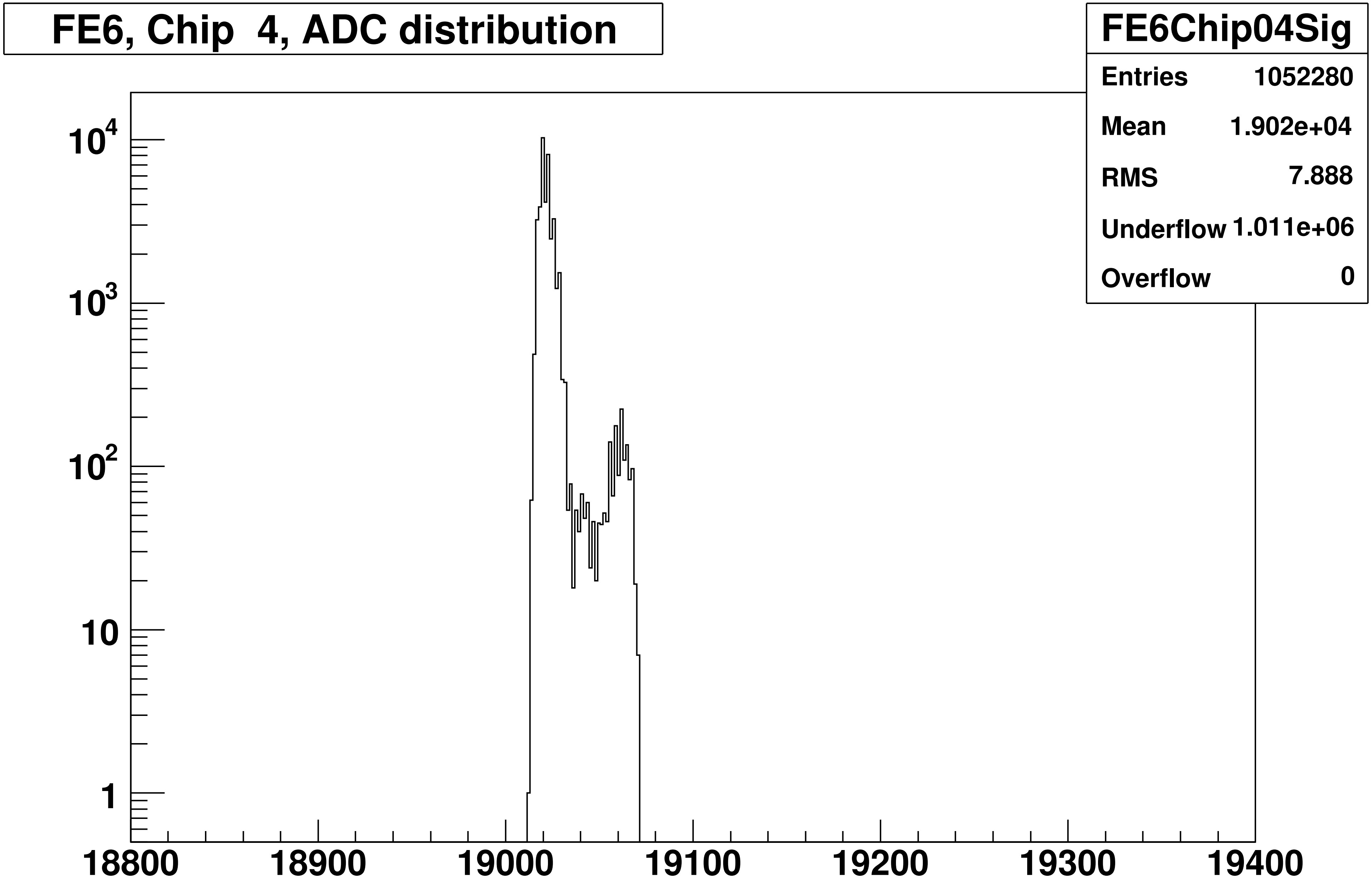

FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 1052280
Mean 1.902e+04
RMS 7.888
Underflow 1.011e+06
Overflow 0
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10^3
10^2
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18900
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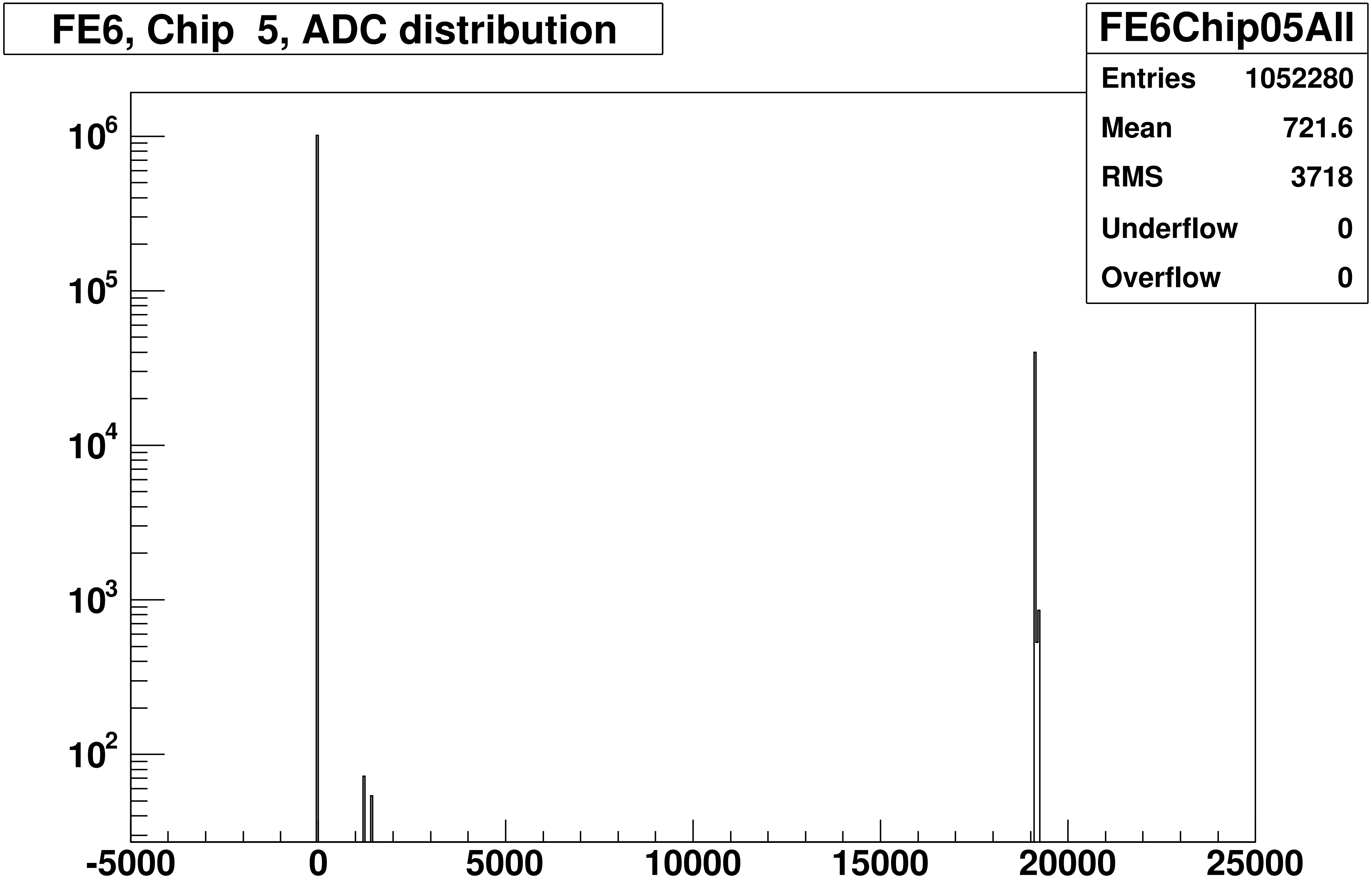

FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 1052280
Mean 721.6
RMS 3718
Underflow 0
Overflow 0
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10^5
10^4
10^3
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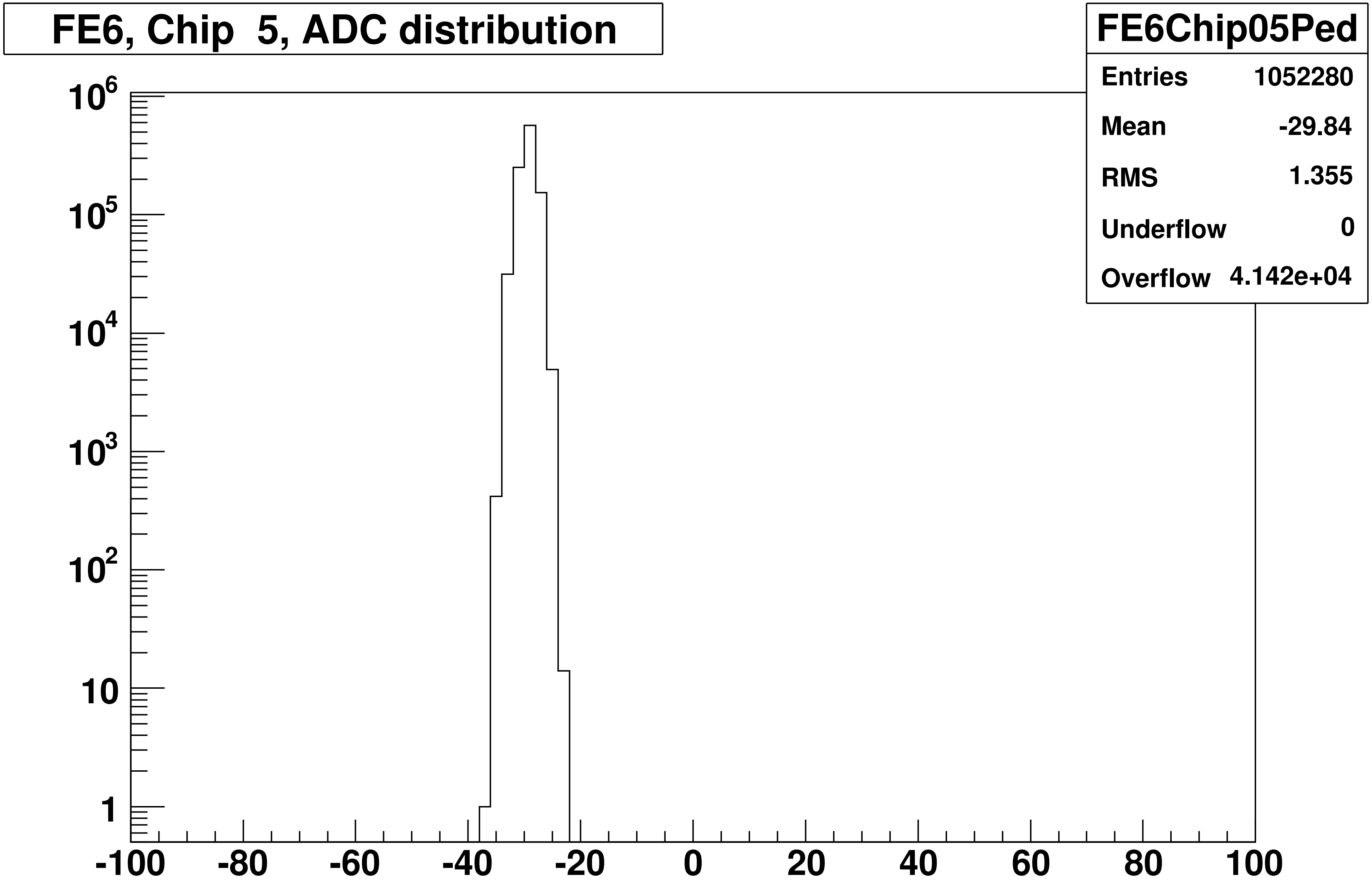
FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 1052280
Mean -29.84
RMS 1.355
Underflow 0
Overflow 4.142e+04
10^6
10^5
10^4
10^3
10^2
10
1
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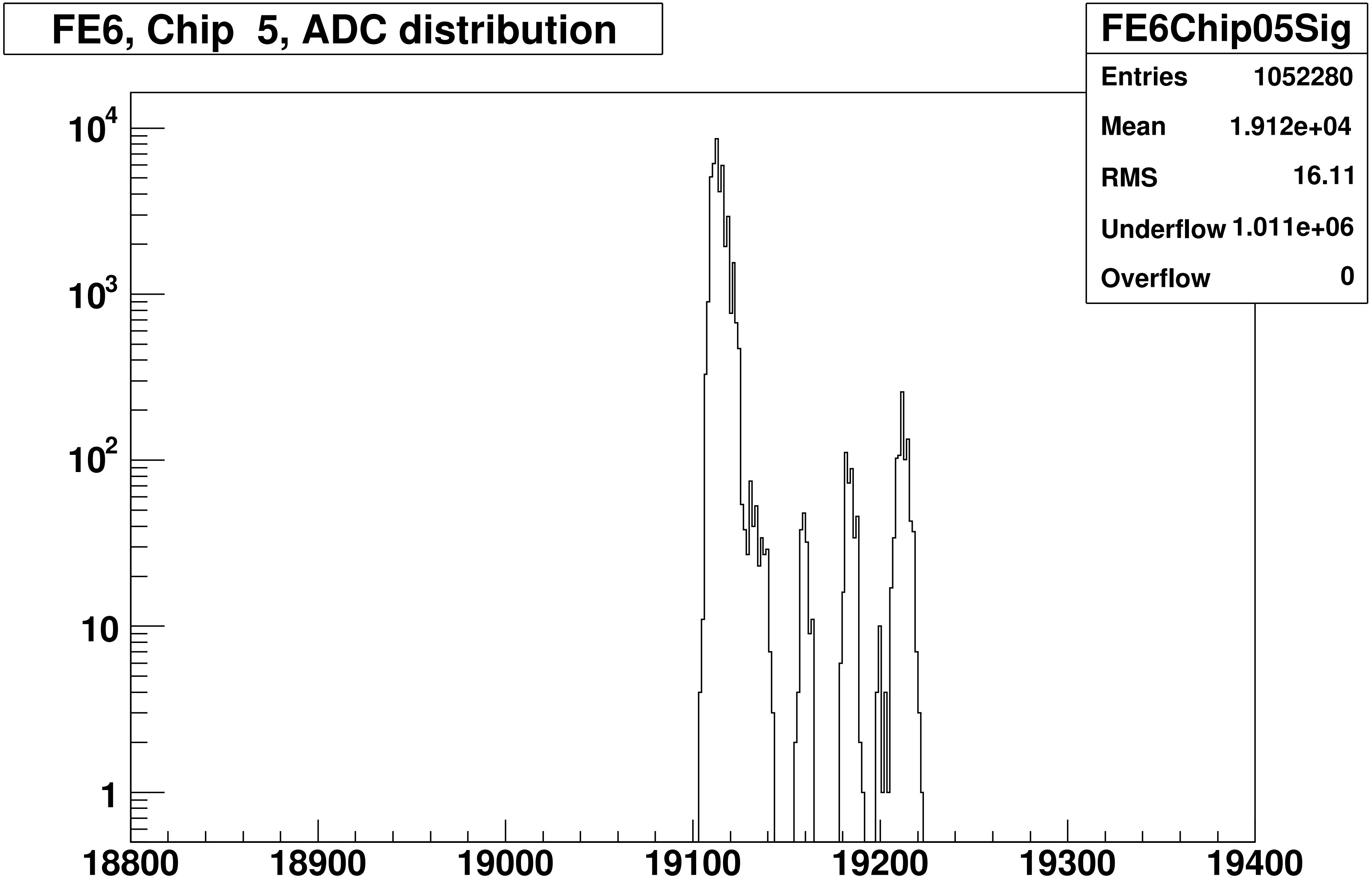

FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 1052280
Mean 1.912e+04
RMS 16.11
Underflow 1.011e+06
Overflow 0
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10^3
10^2
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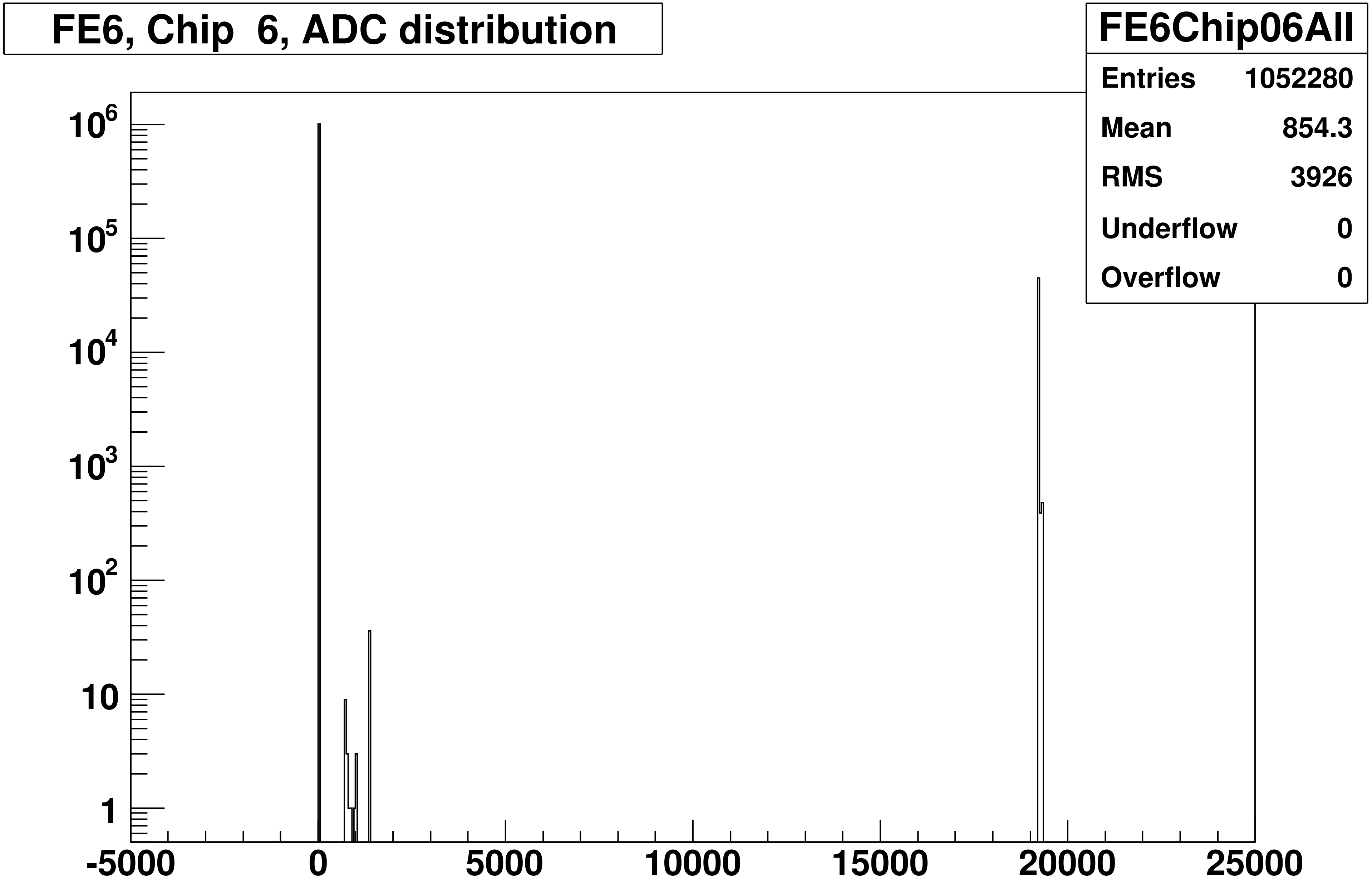
FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 1052280
Mean 854.3
RMS 3926
Underflow 0
Overflow 0
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10^4
10^3
10^2
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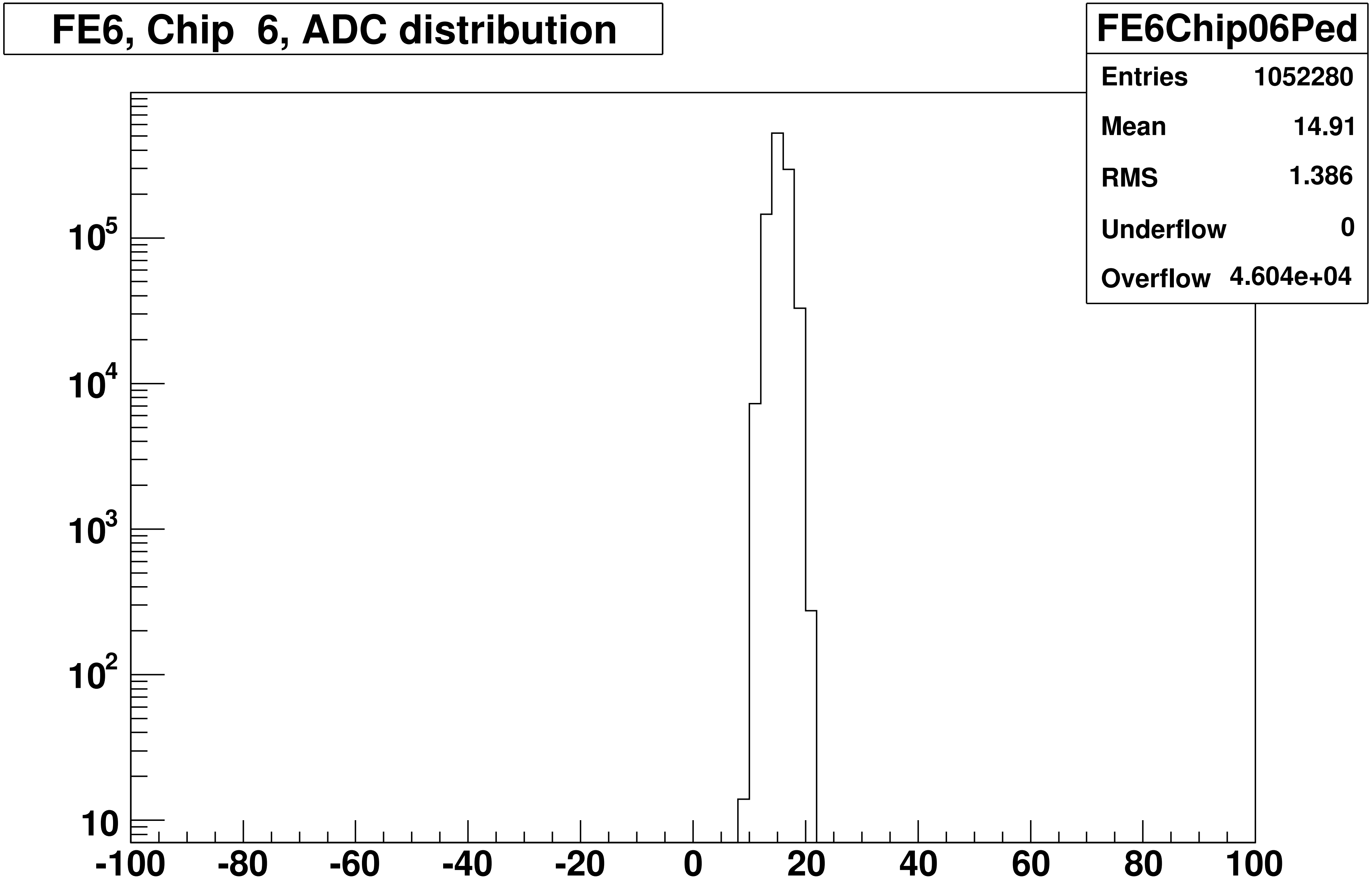
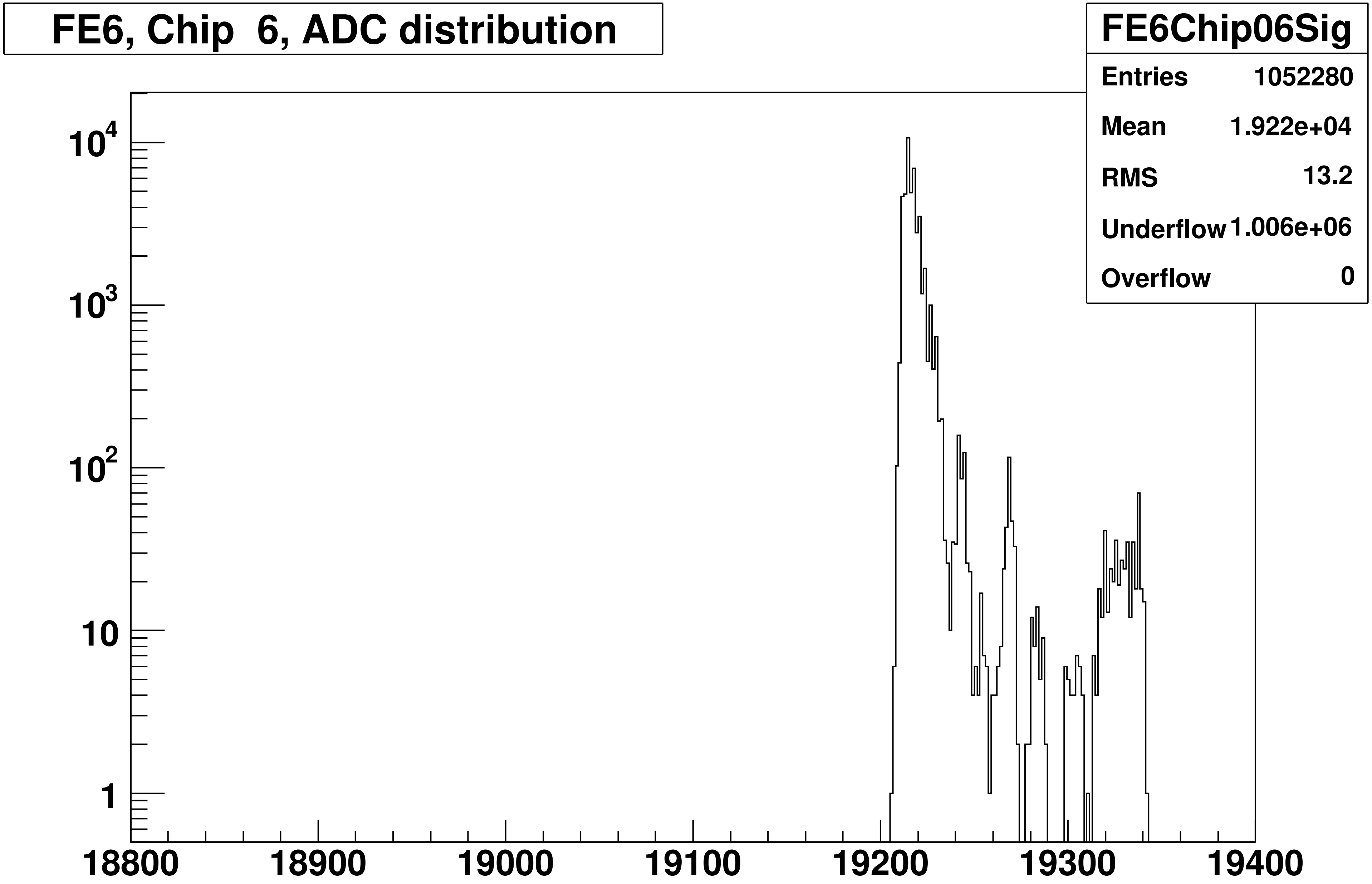

FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 1052280
Mean 14.91
RMS 1.386
Underflow 0
Overflow 4.604e+04
10
10^2
10^3
10^4
10^5
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 1052280
Mean 1.922e+04
RMS 13.2
Underflow 1.006e+06
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
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19100
19200
19300
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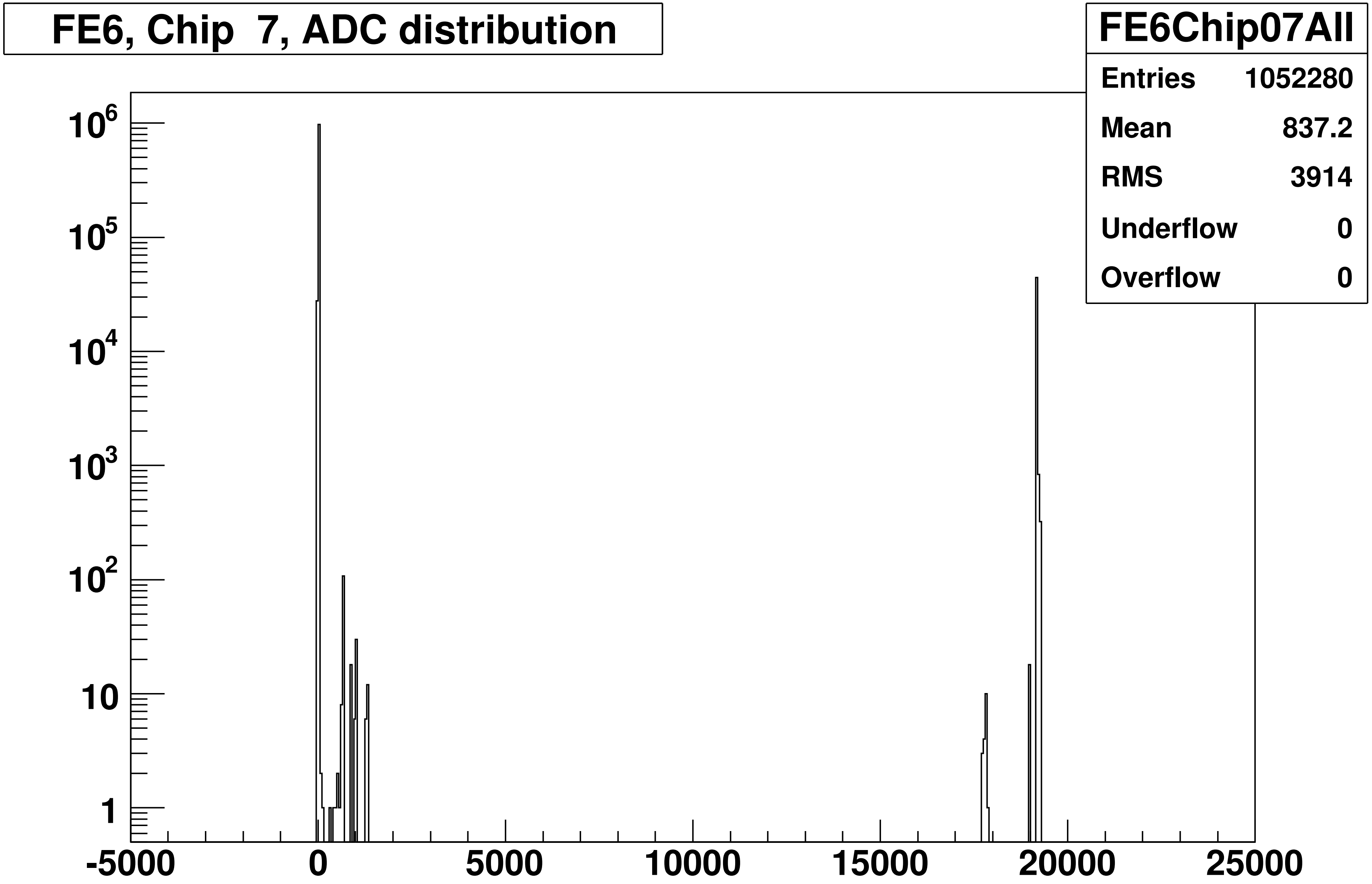

FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 1052280
Mean 837.2
RMS 3914
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
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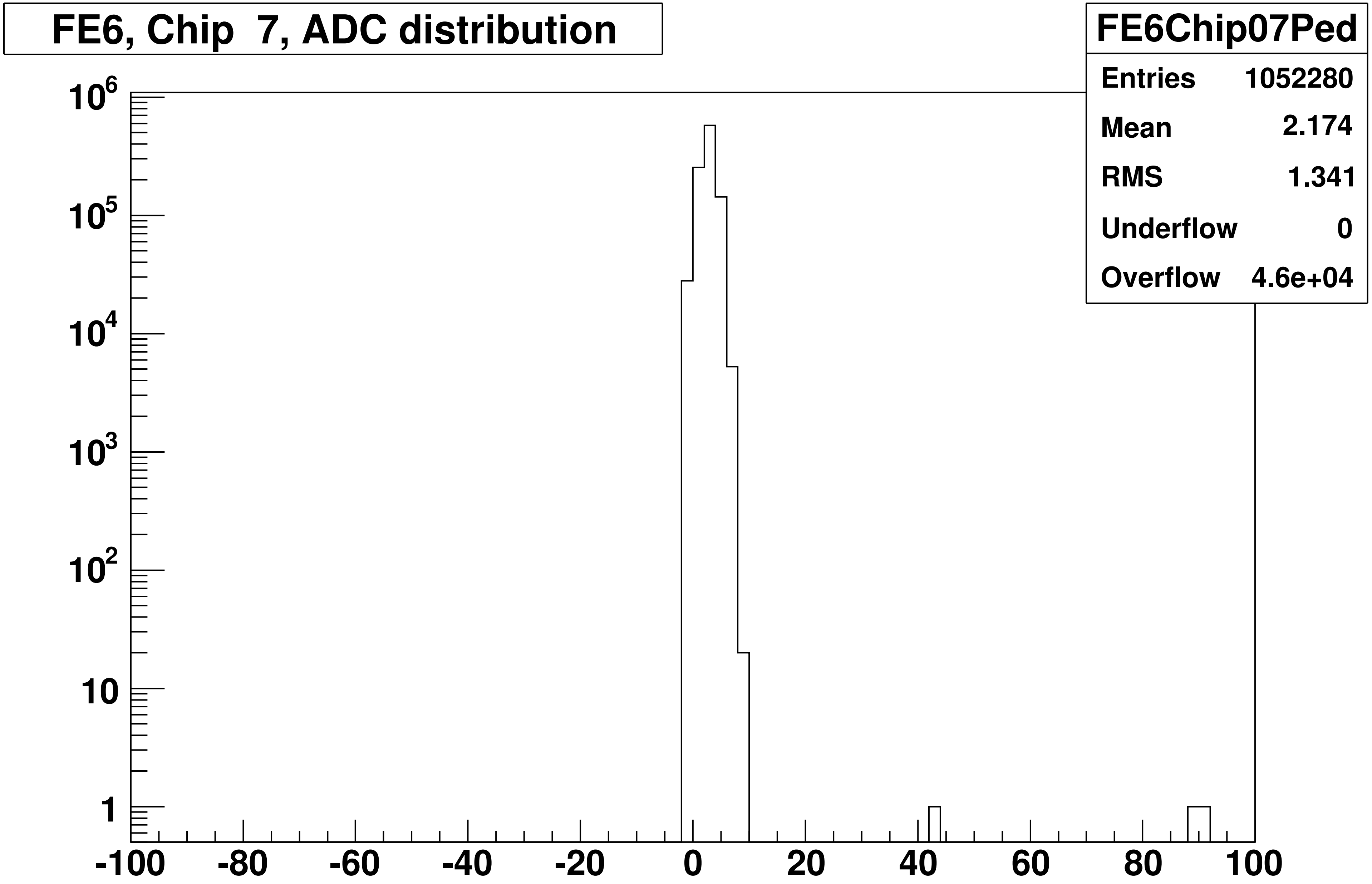
FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 1052280
Mean 2.174
RMS 1.341
Underflow 0
Overflow 4.6e+04
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10^5
10^4
10^3
10^2
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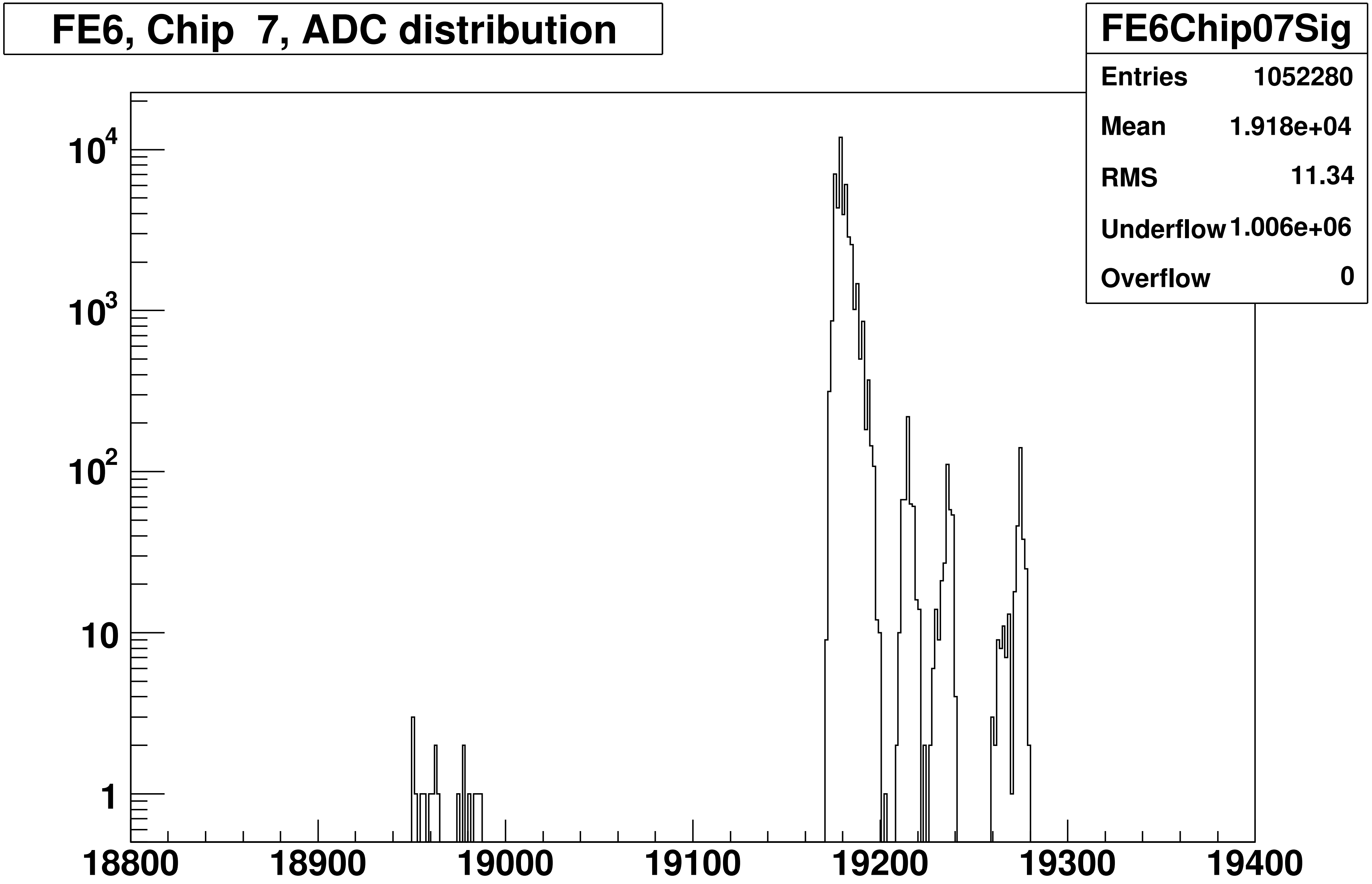
FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 1052280
Mean 1.918e+04
RMS 11.34
Underflow 1.006e+06
Overflow 0
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10^3
10^2
10
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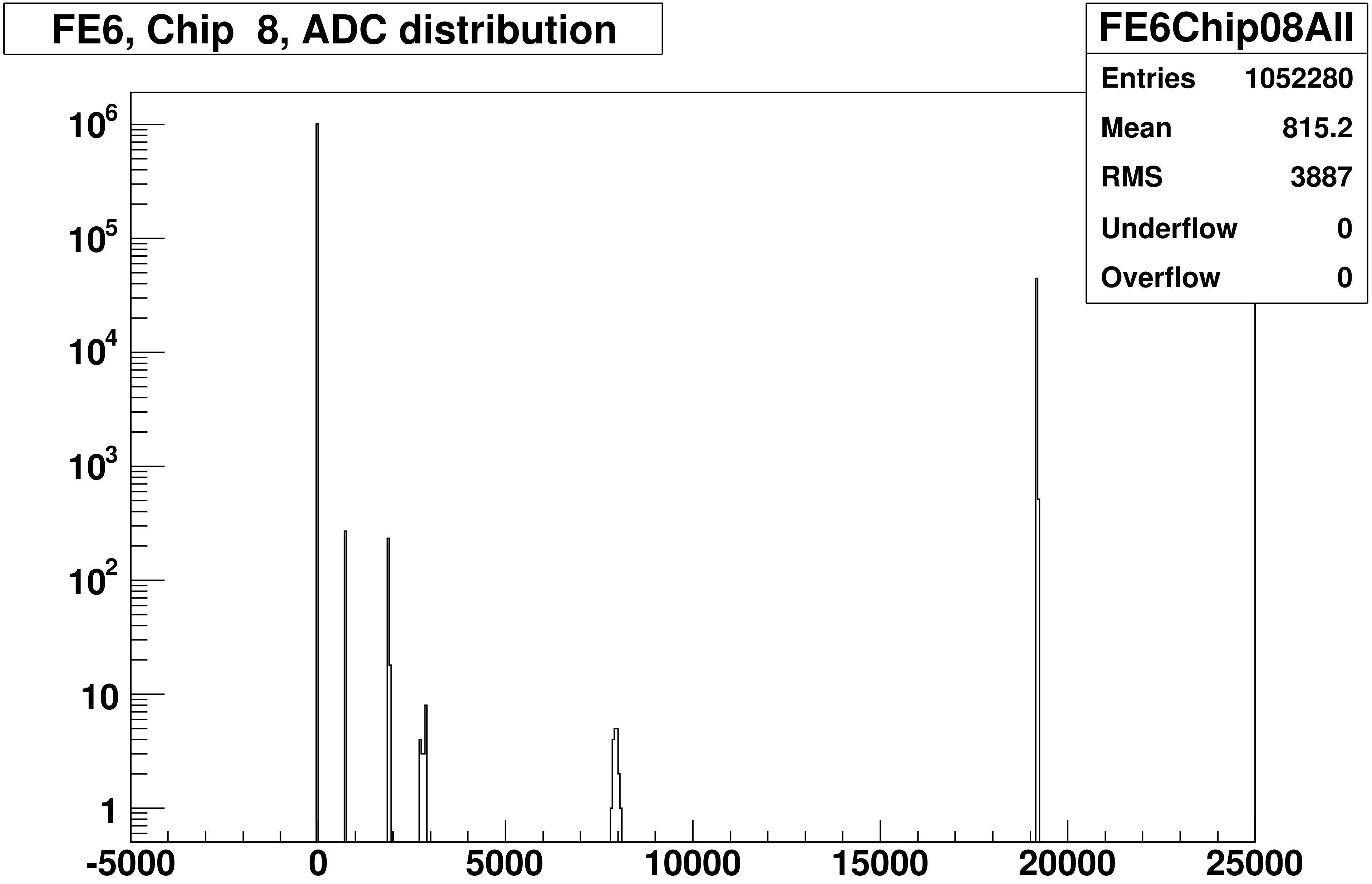

FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 1052280
Mean 815.2
RMS 3887
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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0
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10000
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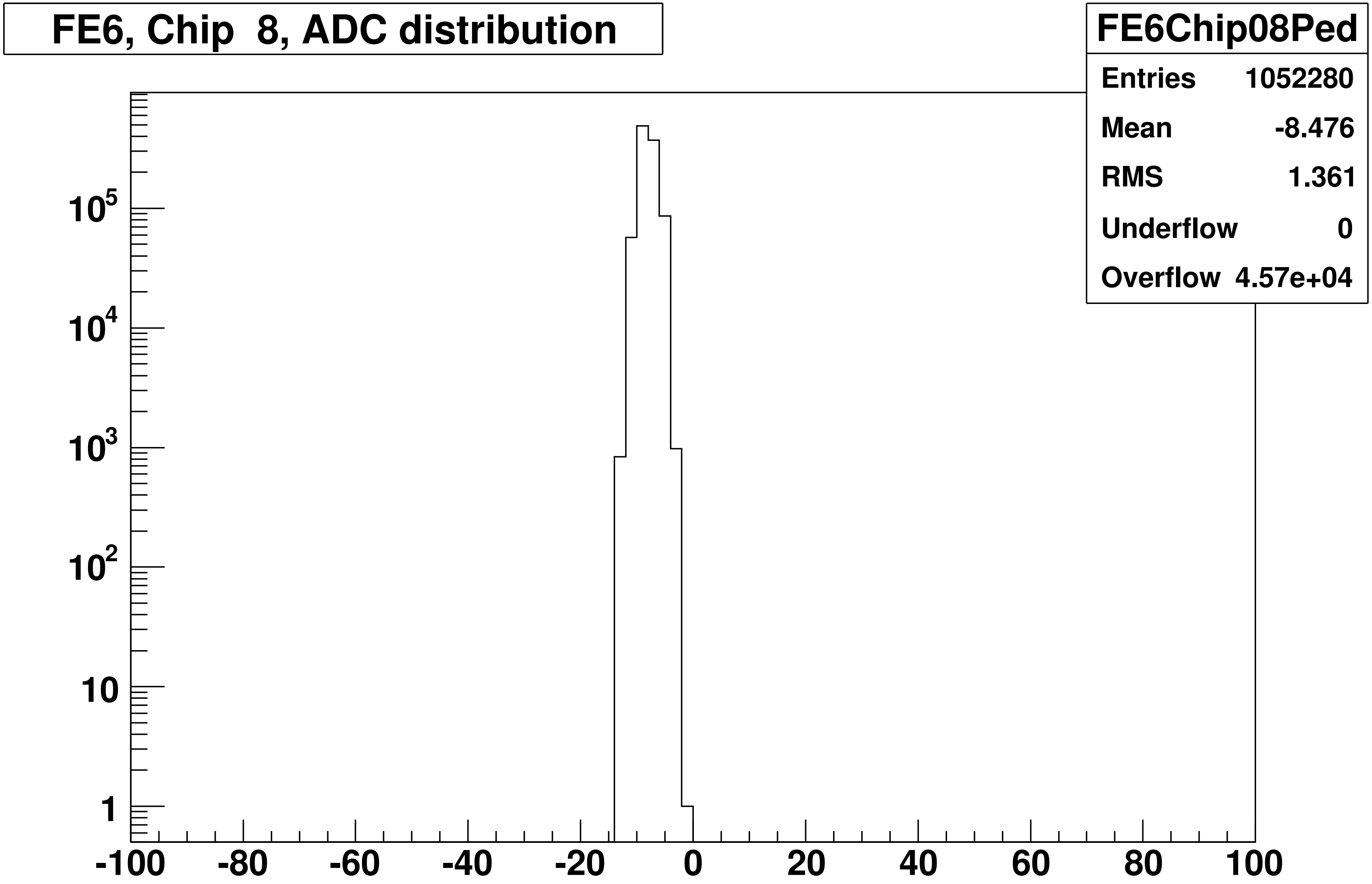

FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 1052280
Mean -8.476
RMS 1.361
Underflow 0
Overflow 4.57e+04
10^5
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10^2
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-40
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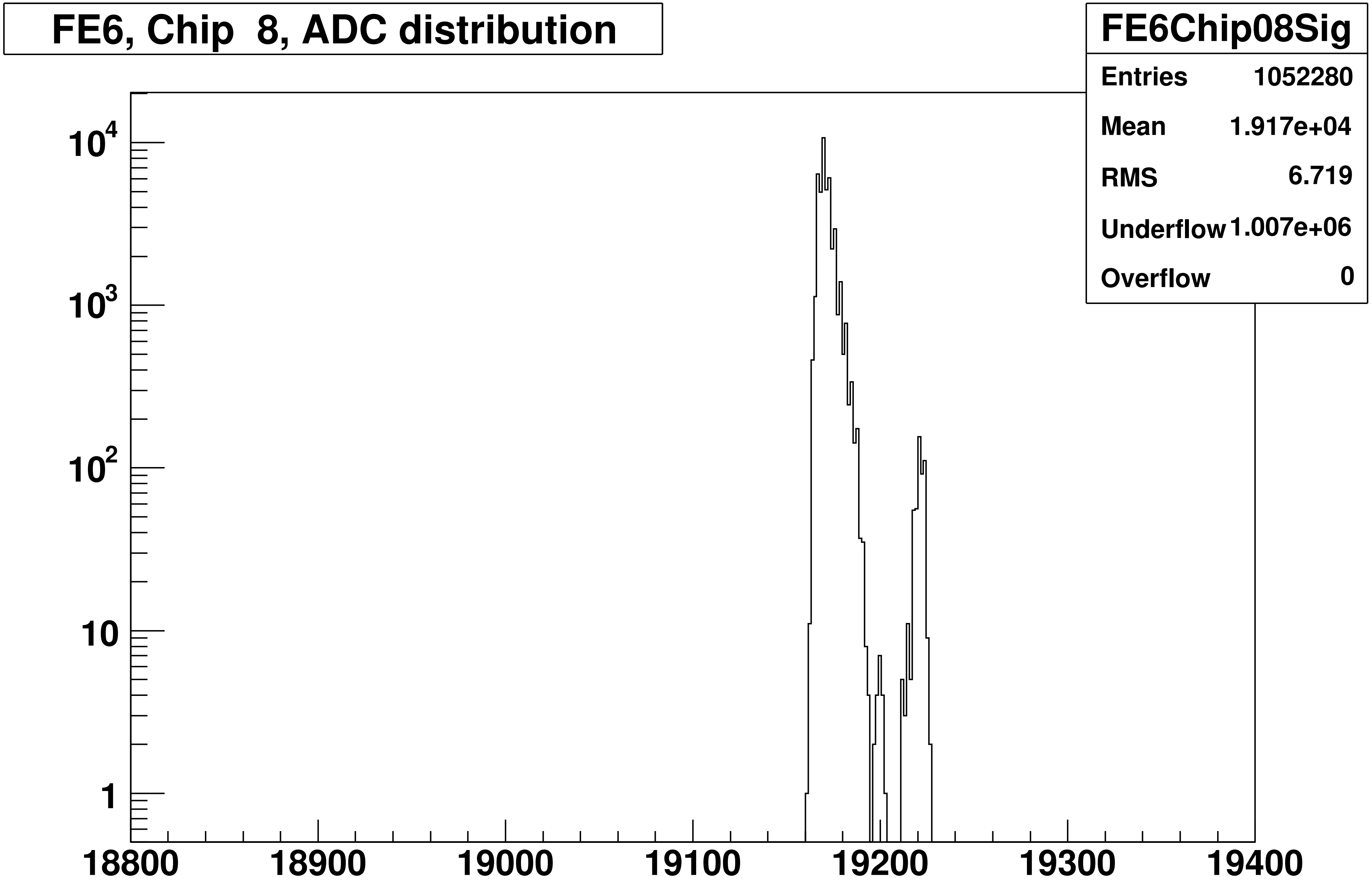

FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 1052280
Mean 1.917e+04
RMS 6.719
Underflow 1.007e+06
Overflow 0
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10^3
10^2
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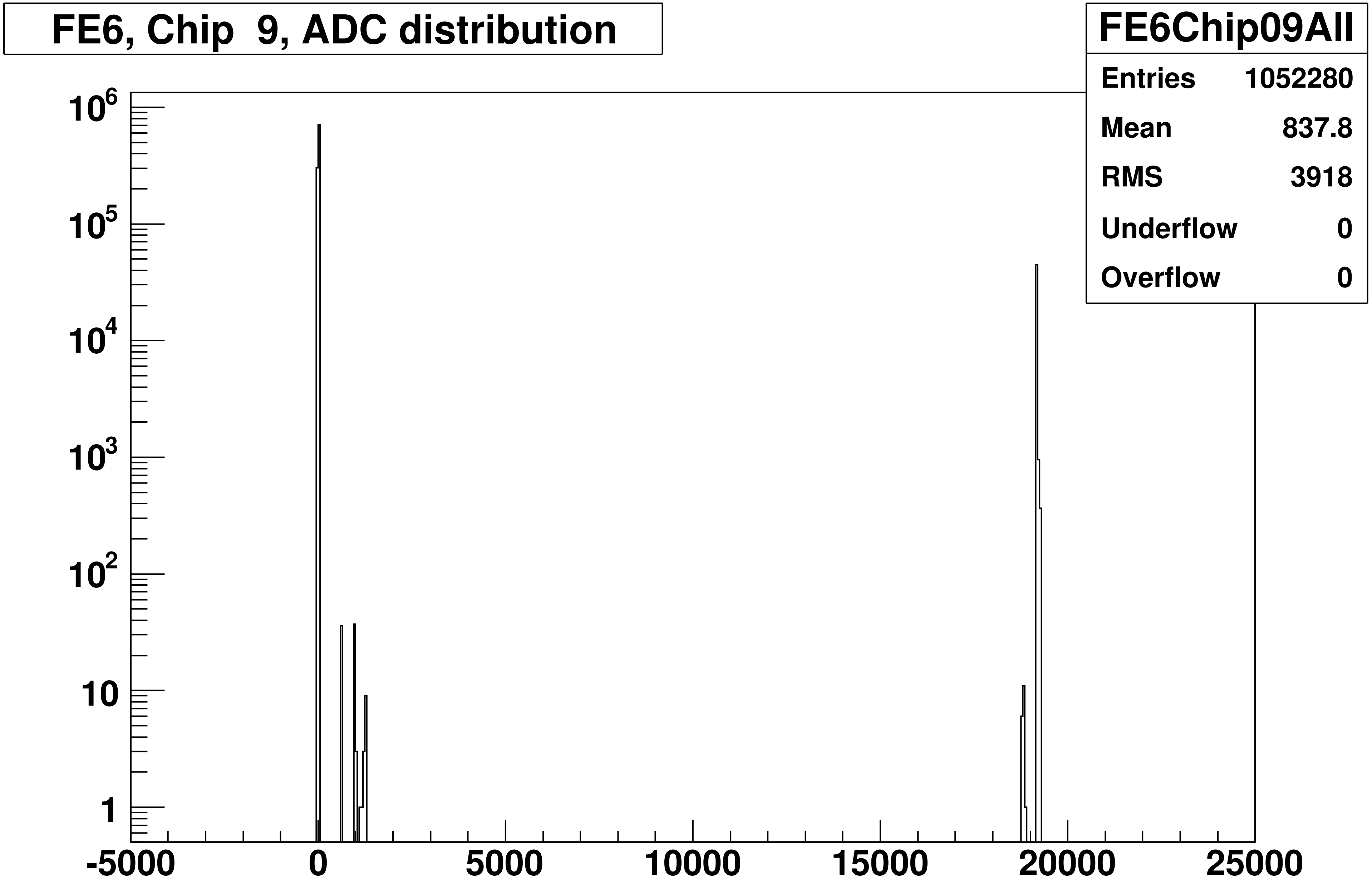

FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 1052280
Mean 837.8
RMS 3918
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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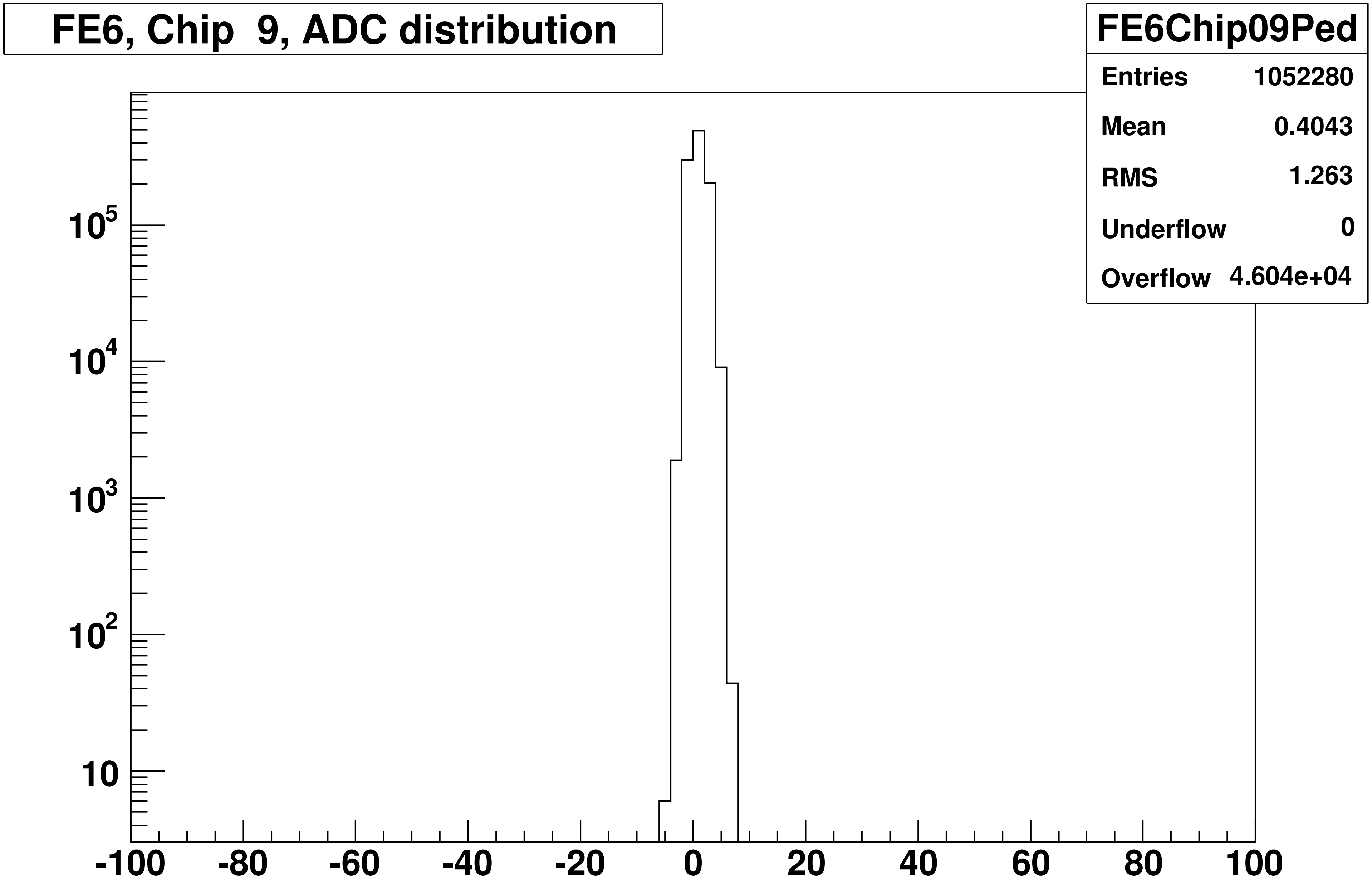

FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 1052280
Mean 0.4043
RMS 1.263
Underflow 0
Overflow 4.604e+04
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10^4
10^3
10^2
10
-100
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-40
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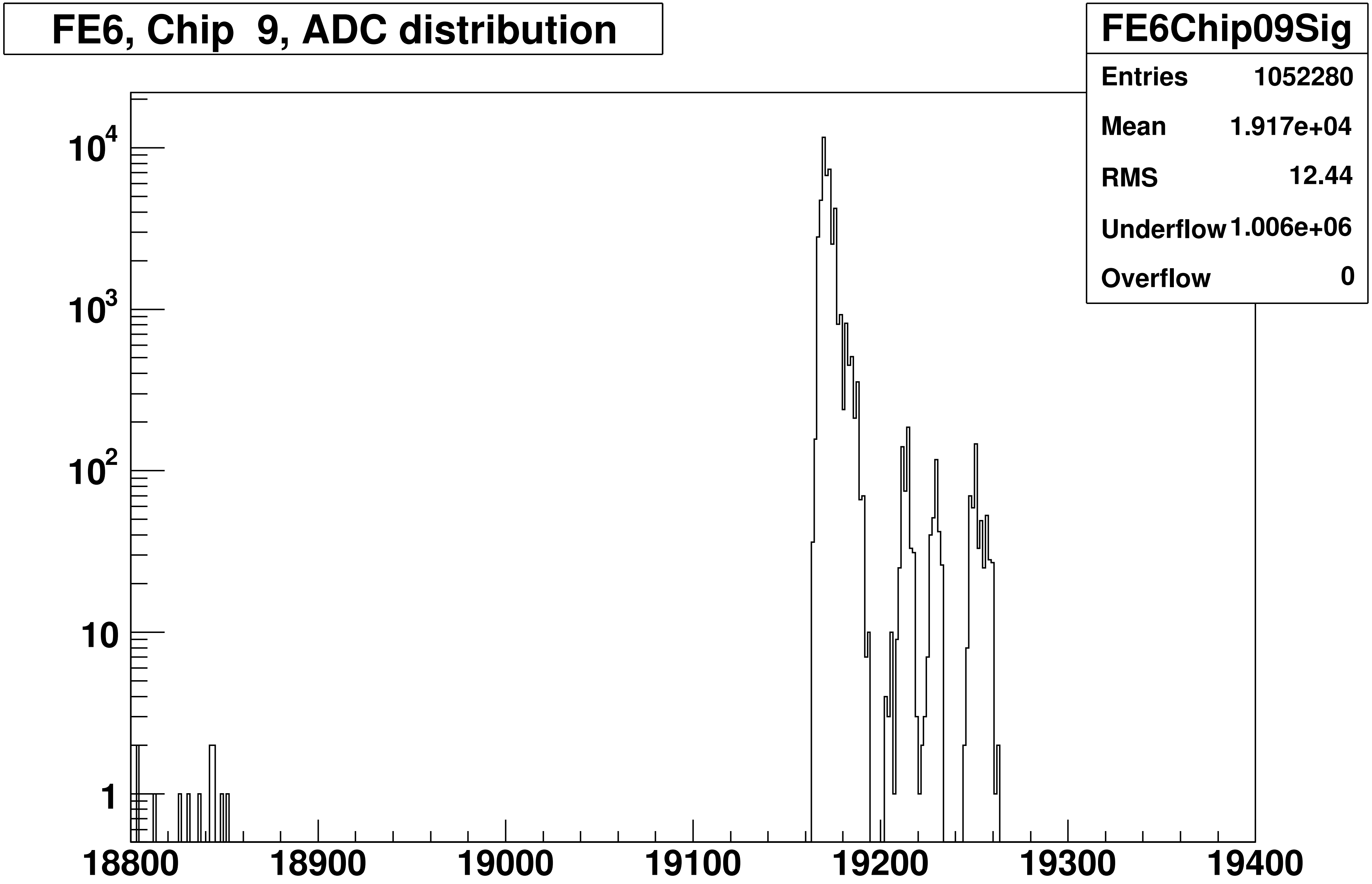
FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 1052280
Mean 1.917e+04
RMS 12.44
Underflow 1.006e+06
Overflow 0
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10^3
10^2
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1
18800
18900
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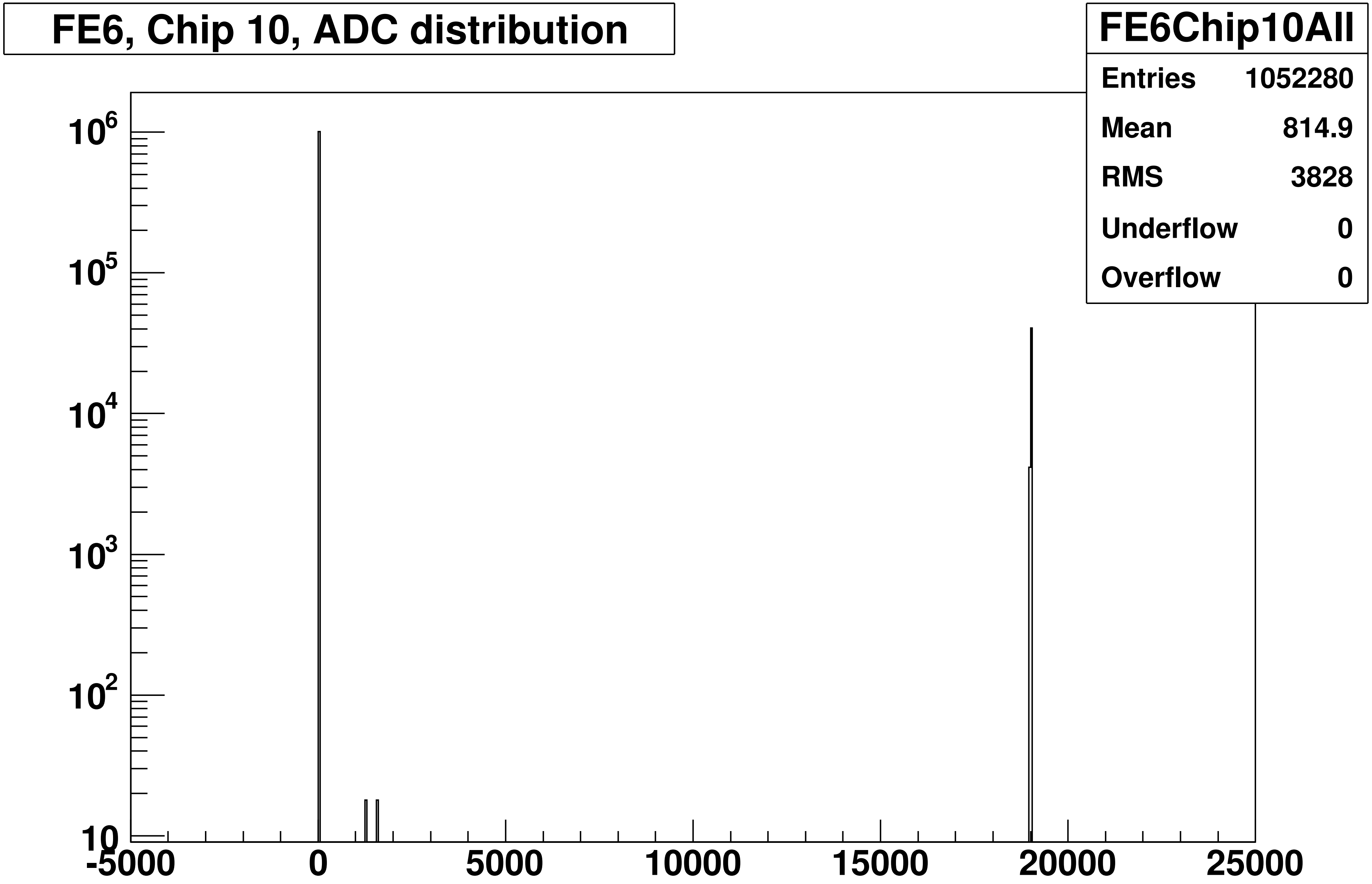

FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 1052280
Mean 814.9
RMS 3828
Underflow 0
Overflow 0
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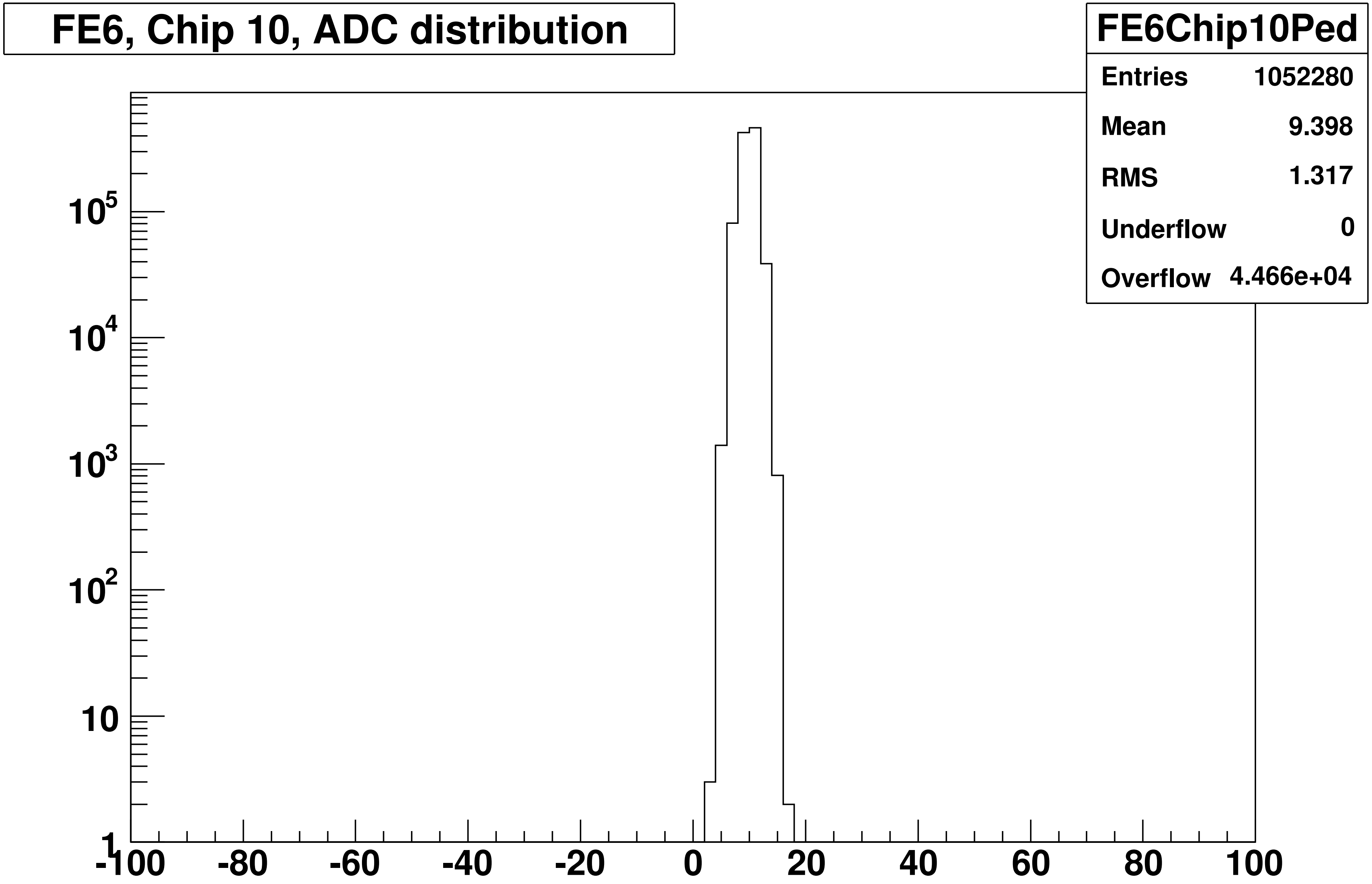
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000



FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 1052280
Mean 9.398
RMS 1.317
Underflow 0
Overflow 4.466e+04
10^5
10^4
10^3
10^2
10
1
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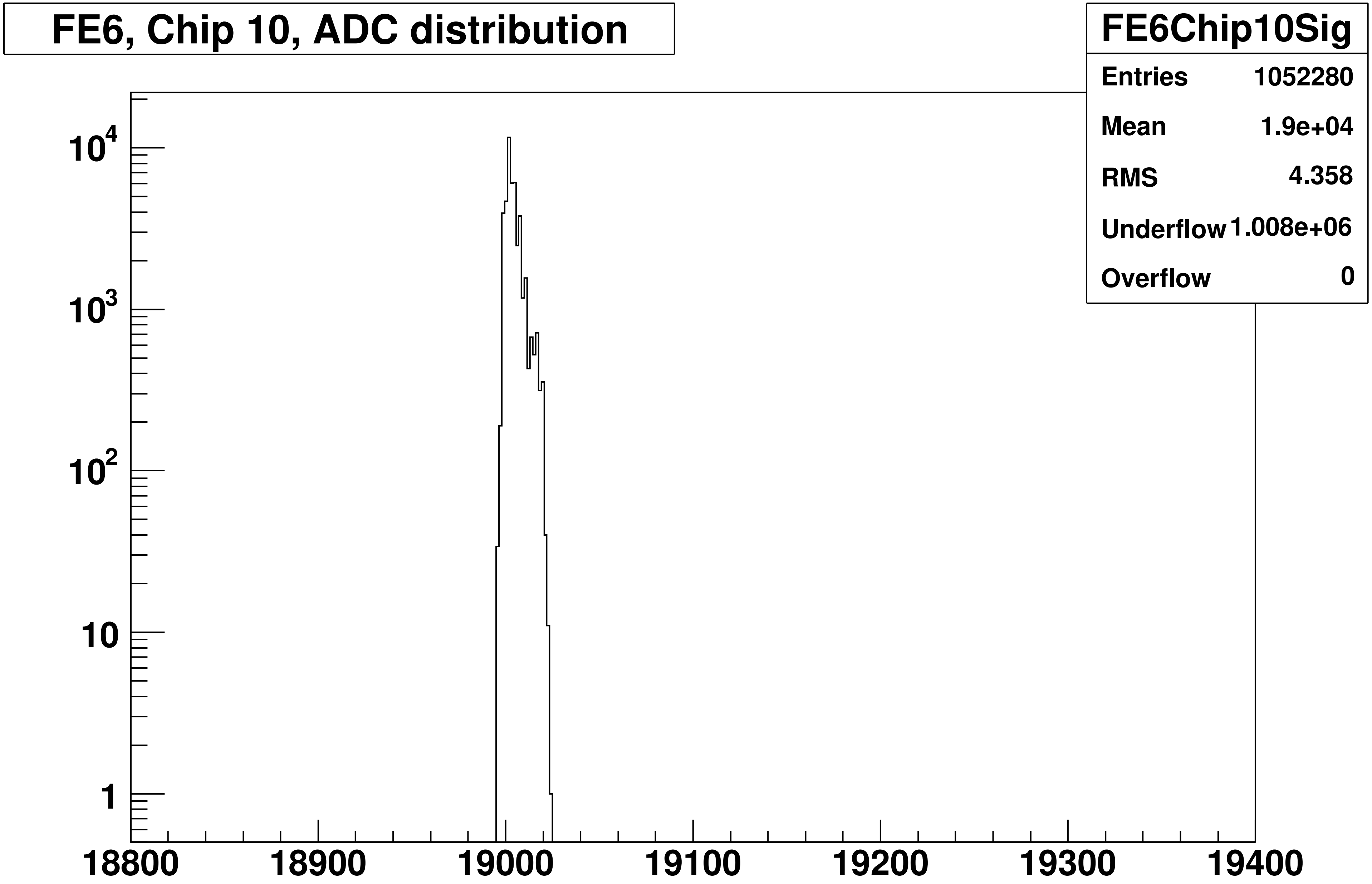
-60
-40
-20
0
20
40
60
80
100


FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 1052280
Mean 1.9e+04
RMS 4.358
Underflow 1.008e+06
Overflow 0
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10^3
10^2
10
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18900
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19100
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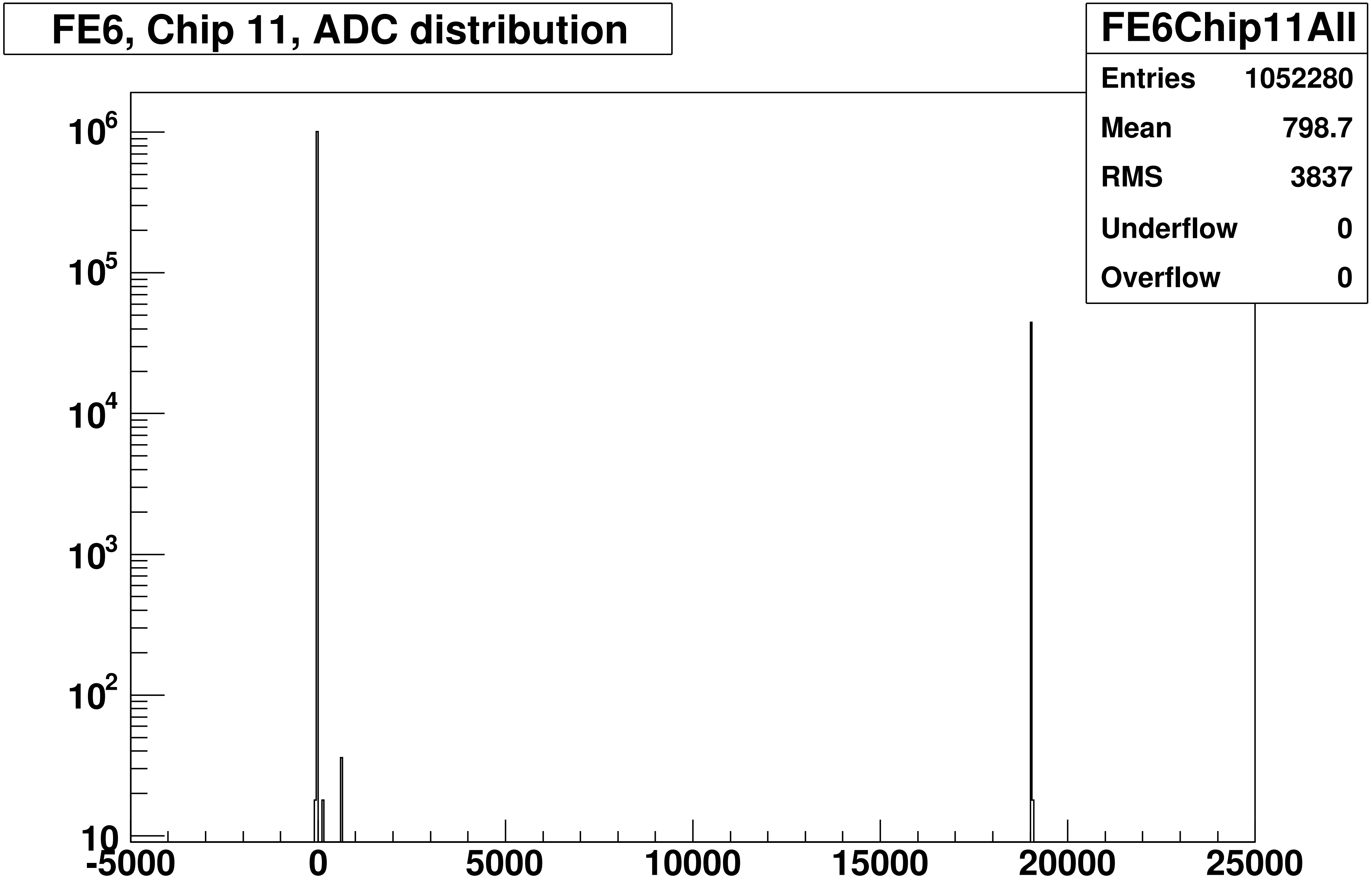
19300
19400



FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 1052280
Mean 798.7
RMS 3837
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
10^6
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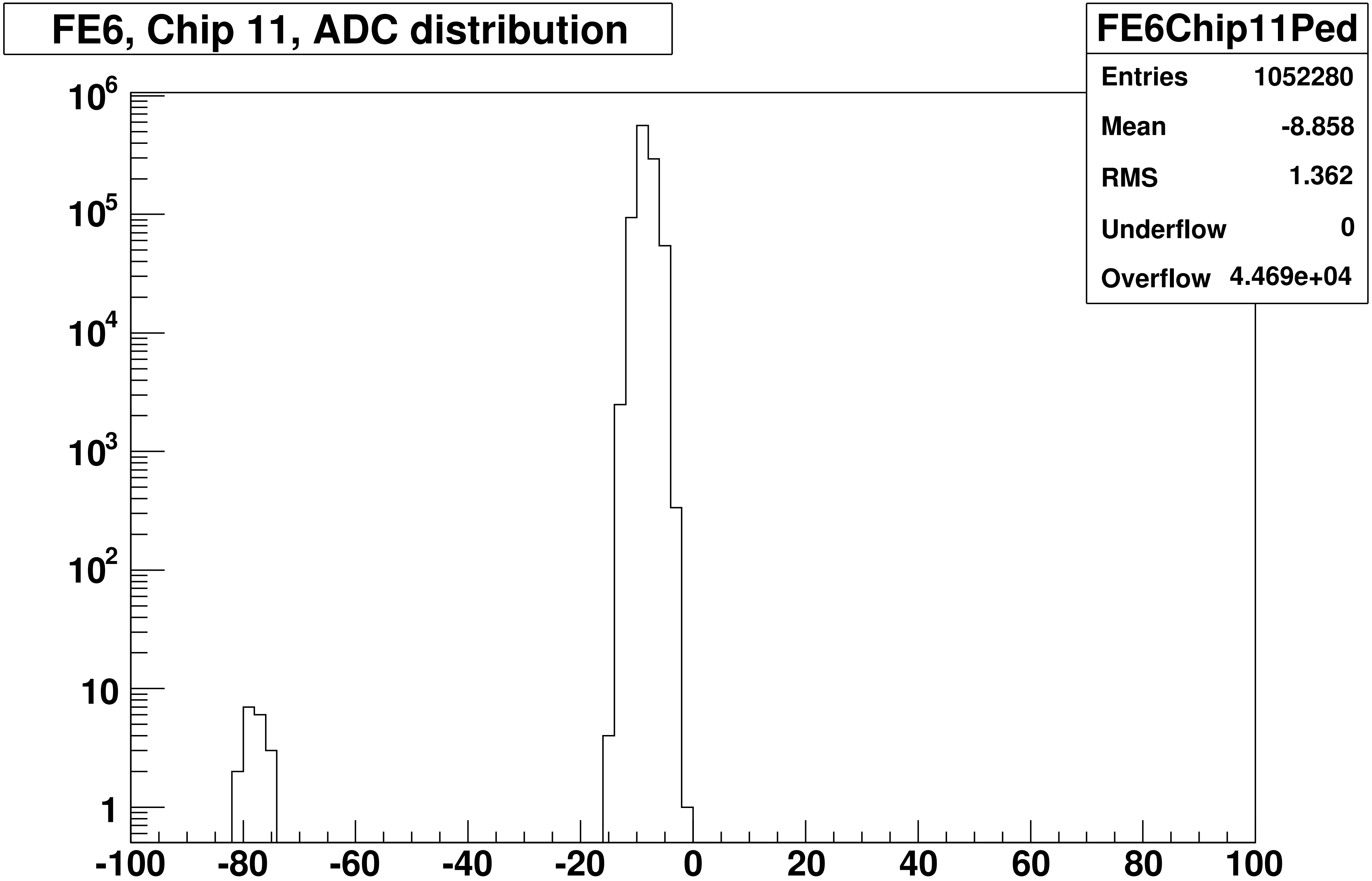
10000
15000
20000
25000



FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 1052280
Mean -8.858
RMS 1.362
Underflow 0
Overflow 4.469e+04
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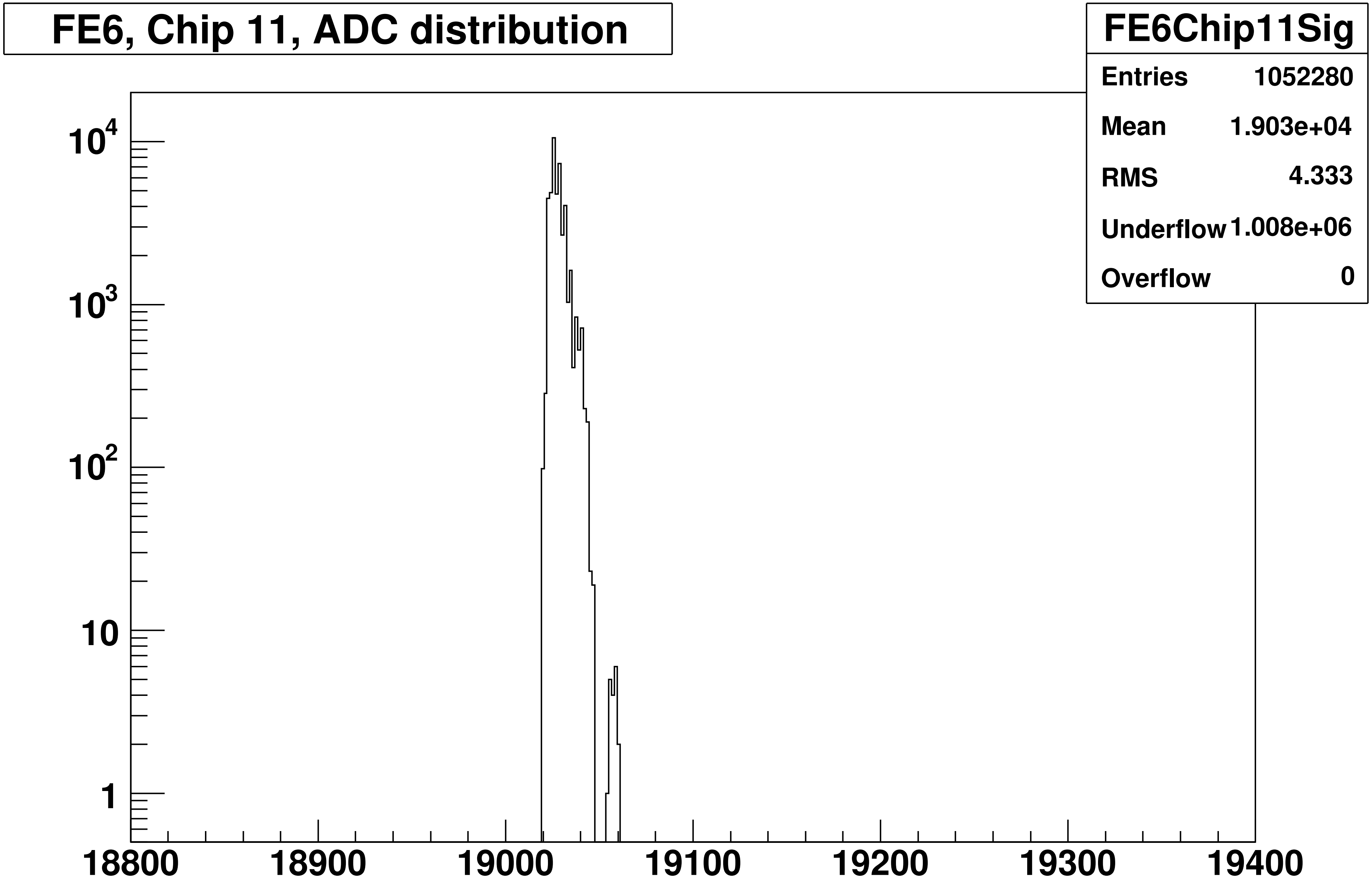
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 1052280
Mean 1.903e+04
RMS 4.333
Underflow 1.008e+06
Overflow 0
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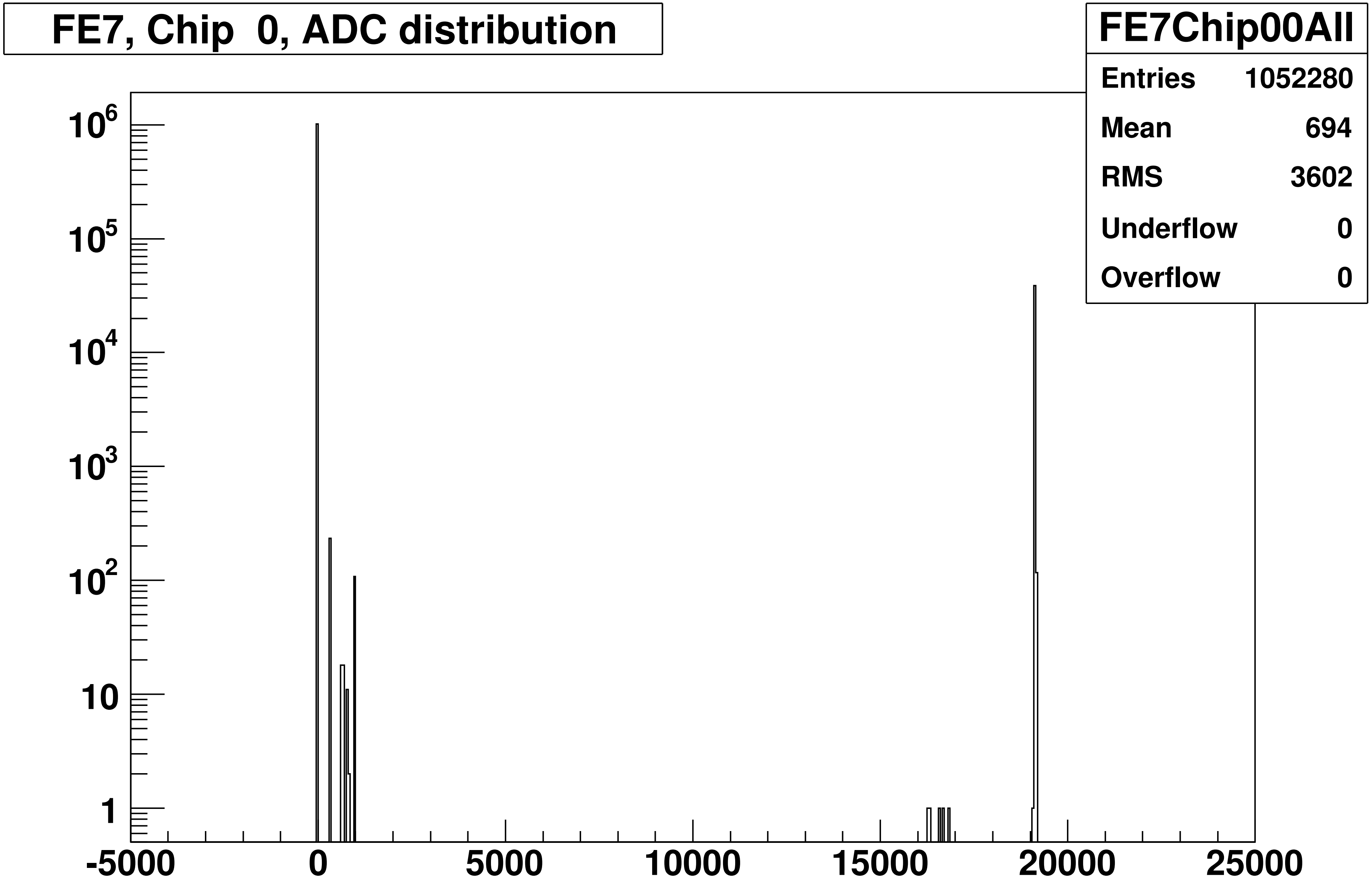
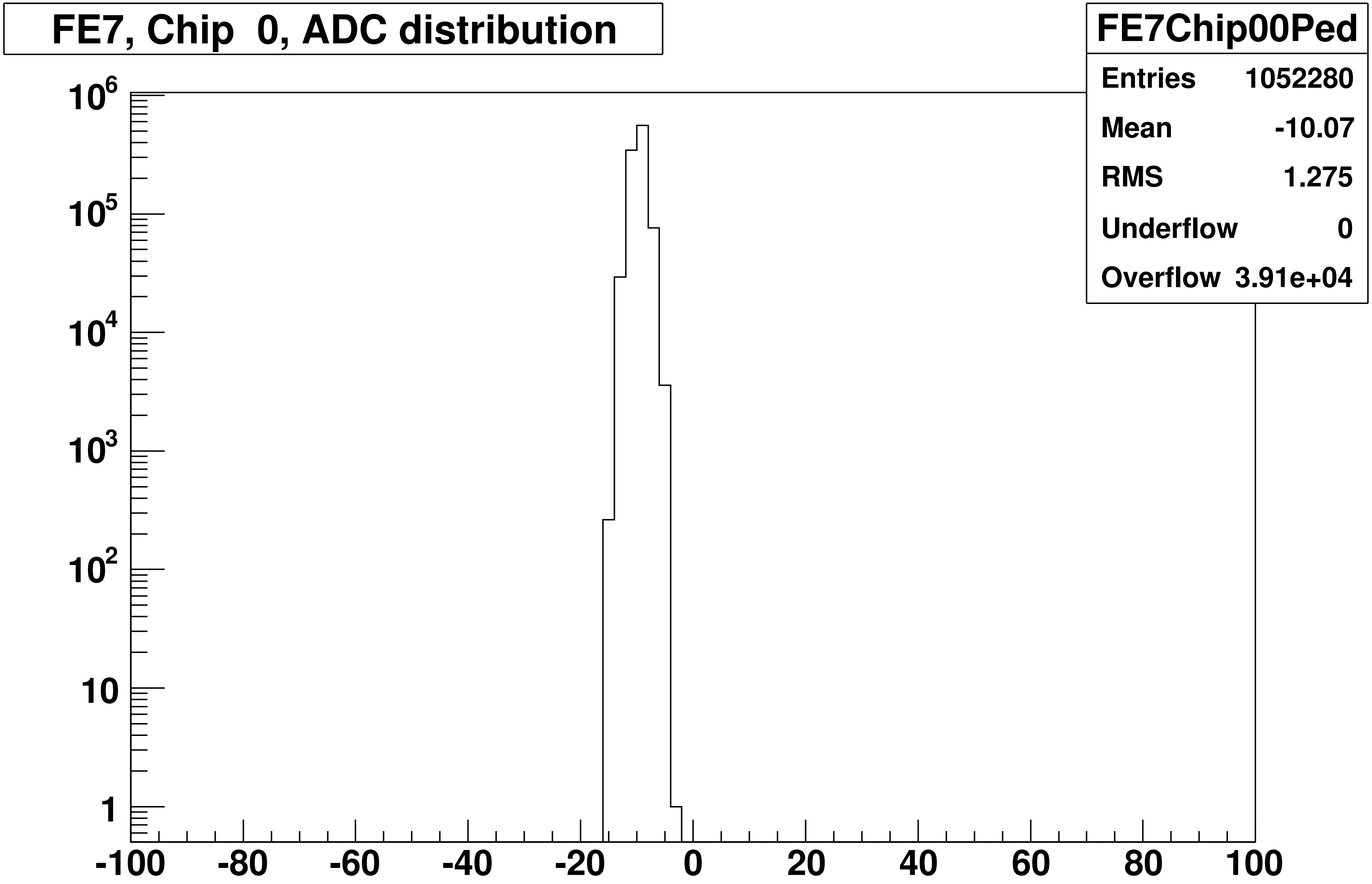
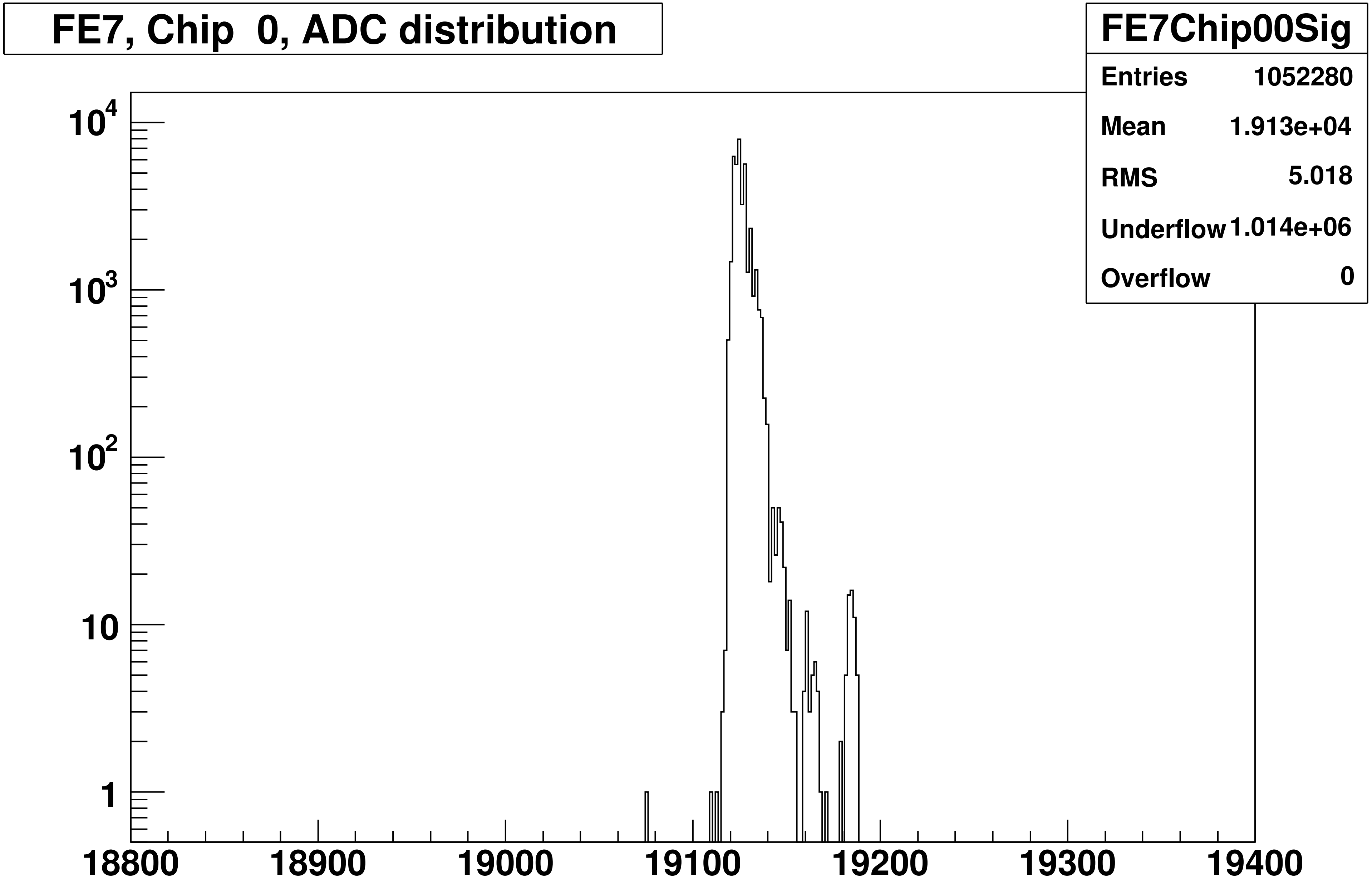
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 1052280
Mean 694
RMS 3602
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 1052280
Mean -10.07
RMS 1.275
Underflow 0
Overflow 3.91e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100



FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 1052280
Mean 1.913e+04
RMS 5.018
Underflow 1.014e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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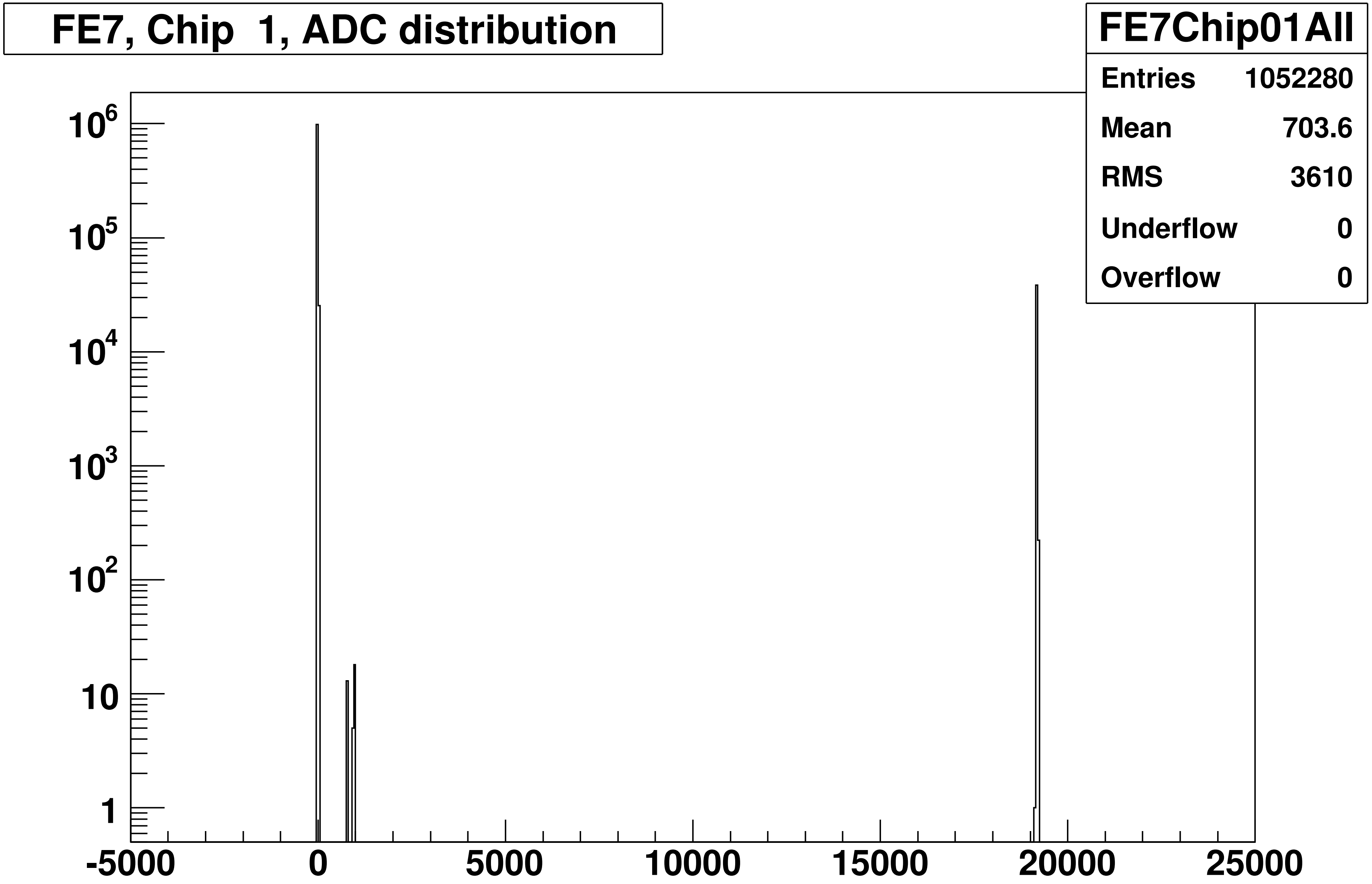
FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 1052280
Mean 703.6
RMS 3610
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
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0
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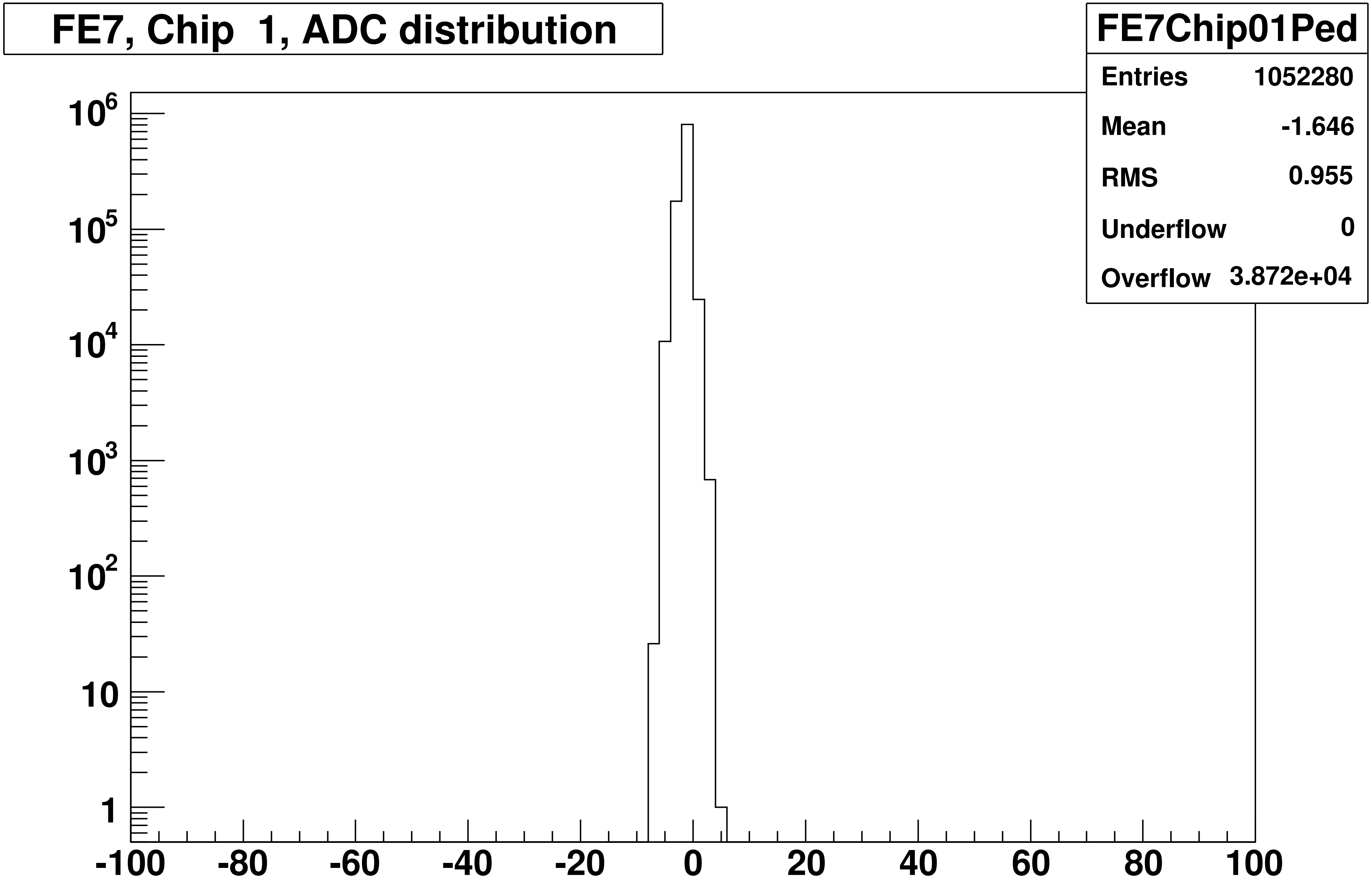
10000
15000
20000
25000



FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 1052280
Mean -1.646
RMS 0.955
Underflow 0
Overflow 3.872e+04
10^6
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
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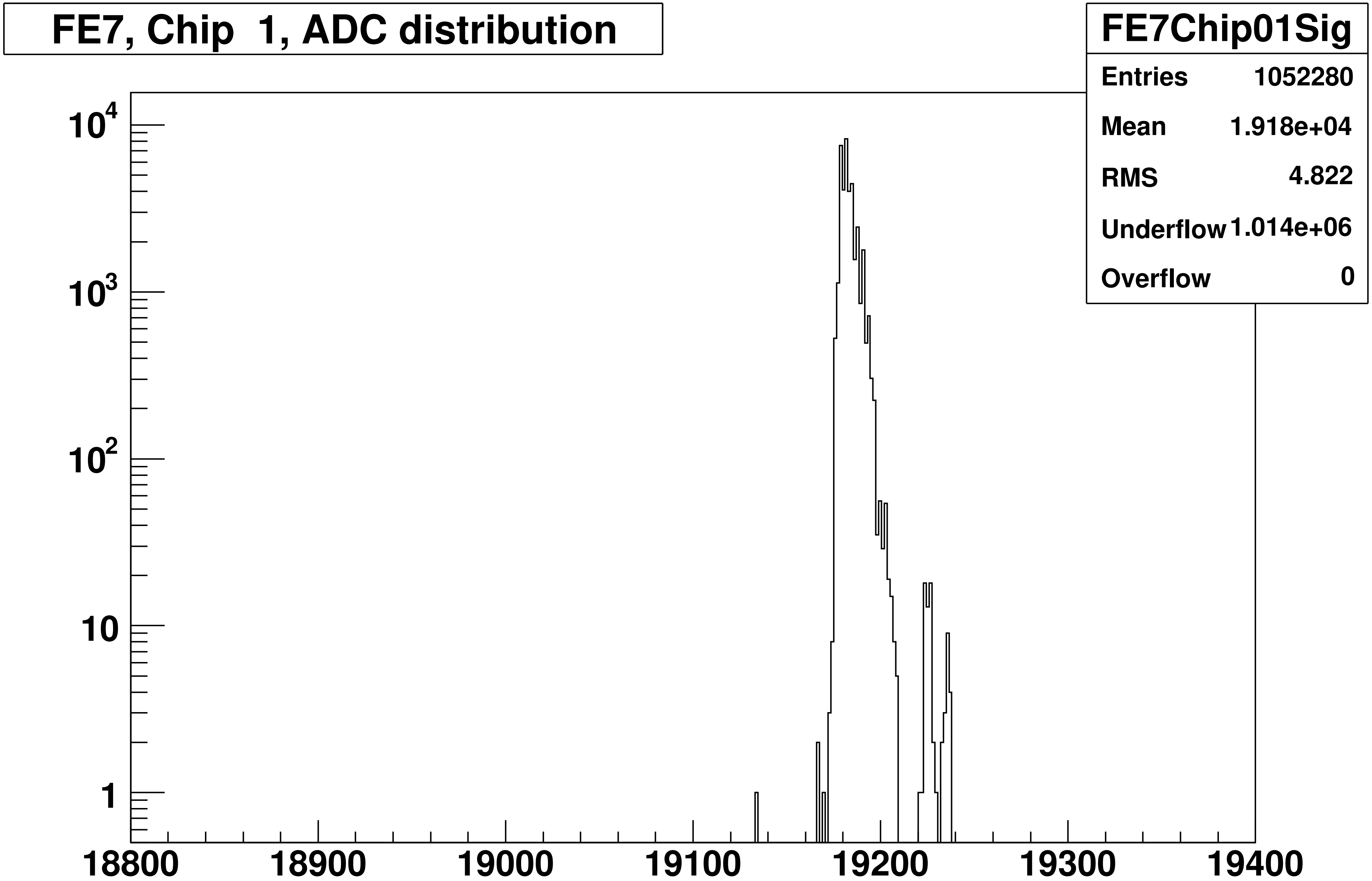
60
80
100


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 1052280
Mean 1.918e+04
RMS 4.822
Underflow 1.014e+06
Overflow 0
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10^3
10^2
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1
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18900
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19200
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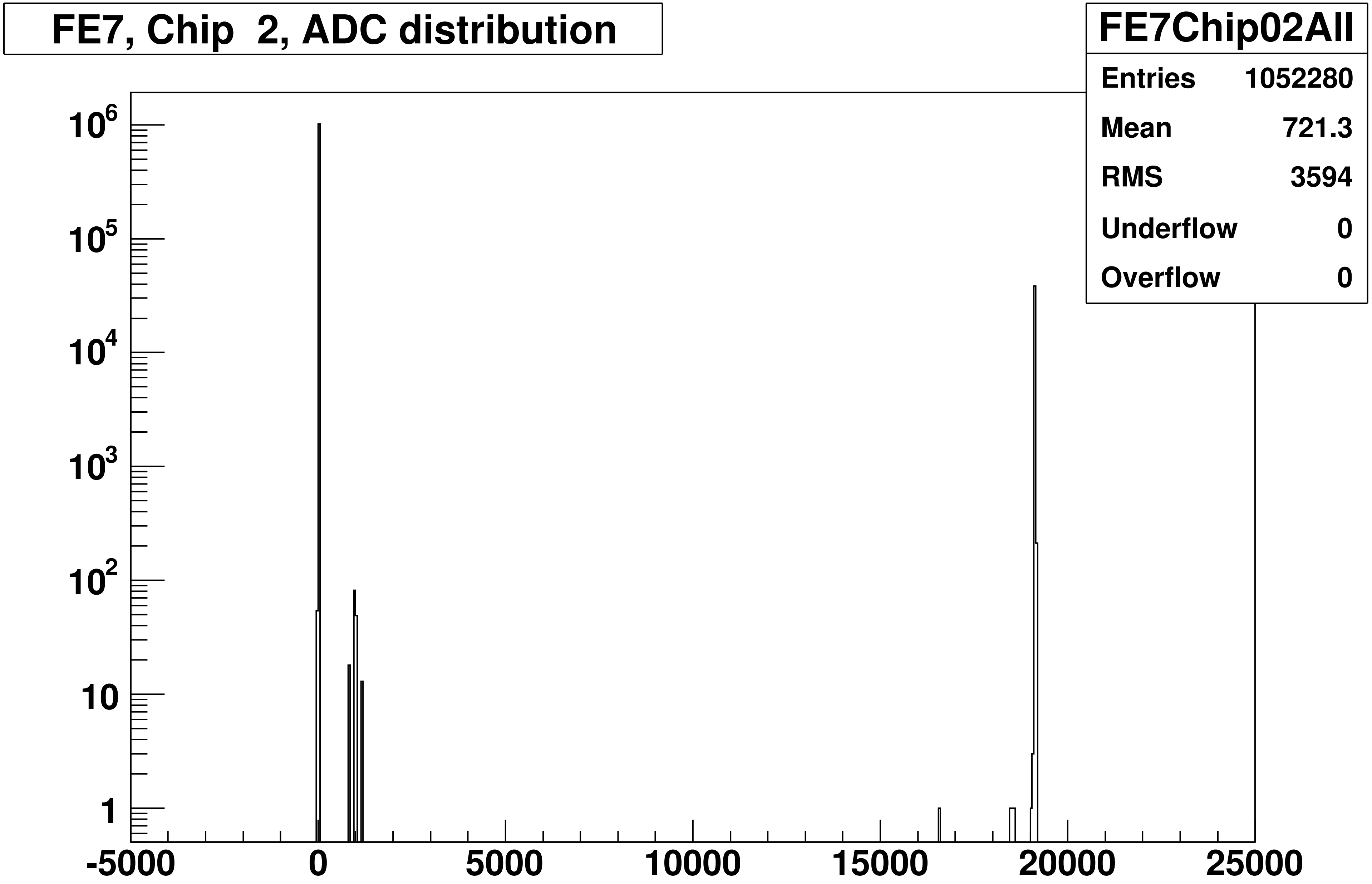
FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 1052280
Mean 721.3
RMS 3594
Underflow 0
Overflow 0
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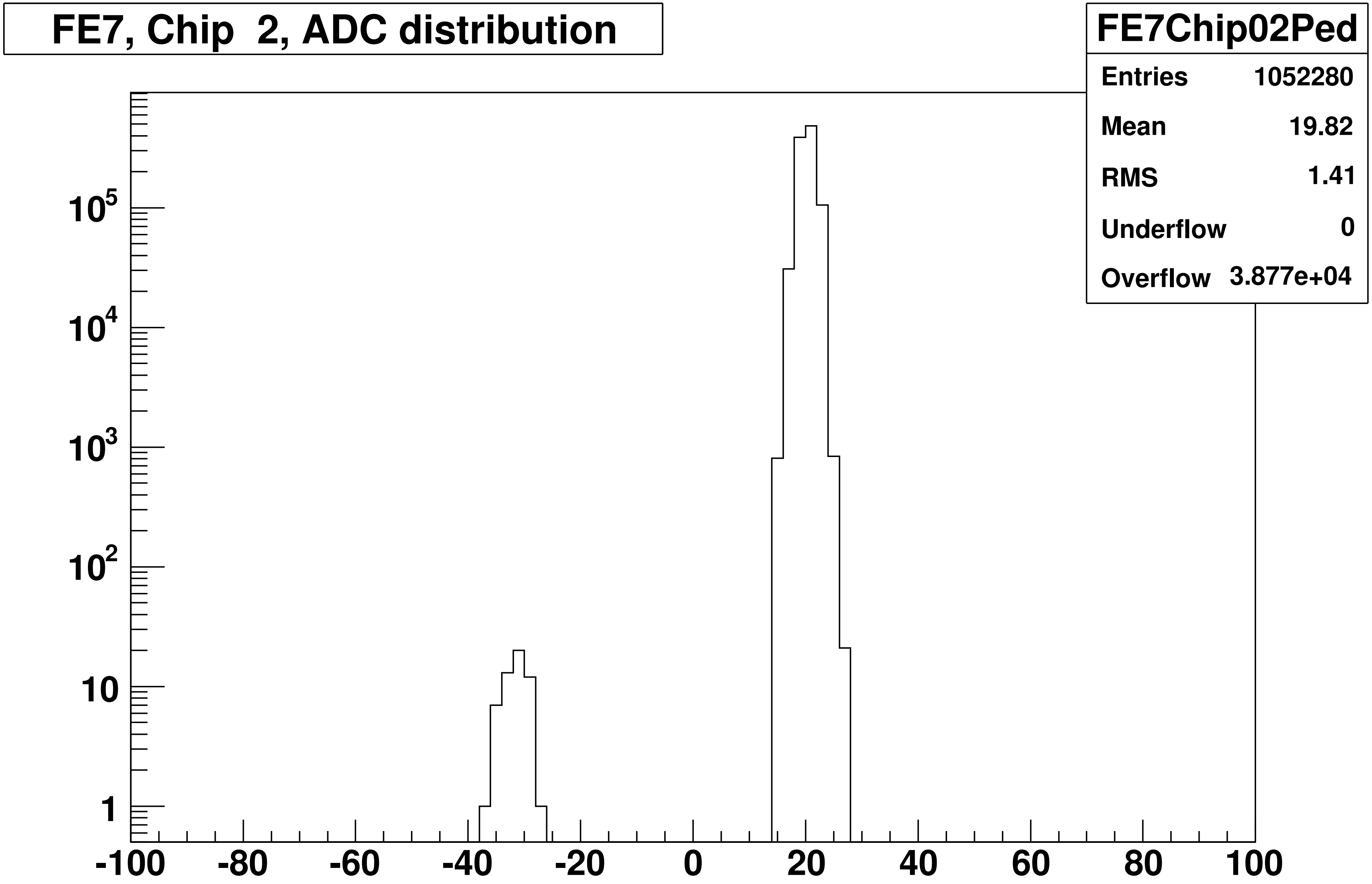
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 1052280
Mean 19.82
RMS 1.41
Underflow 0
Overflow 3.877e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
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40
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80
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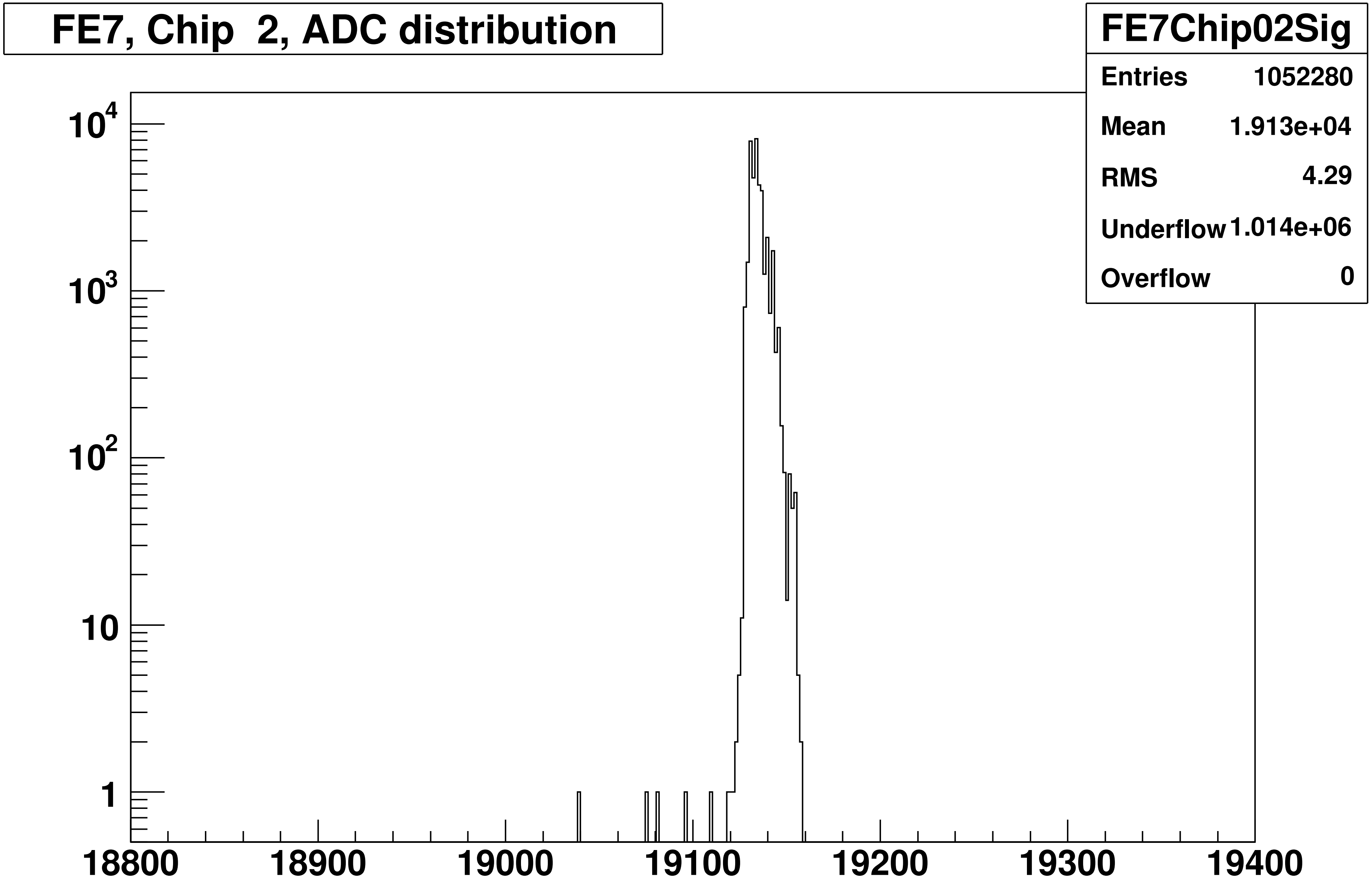
FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 1052280
Mean 1.913e+04
RMS 4.29
Underflow 1.014e+06
Overflow 0
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10^3
10^2
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1
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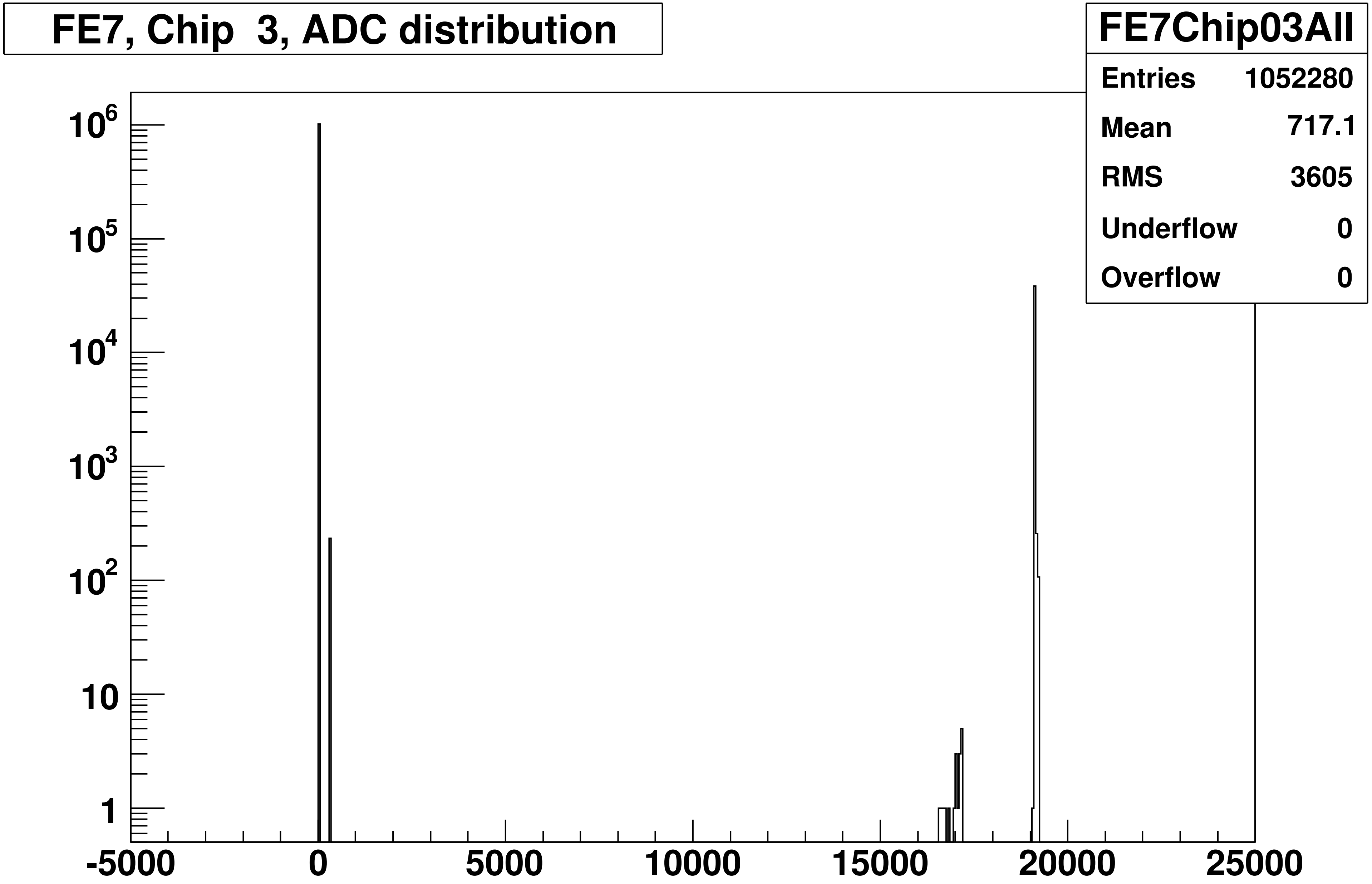

FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 1052280
Mean 717.1
RMS 3605
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
1
-5000
0
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10000
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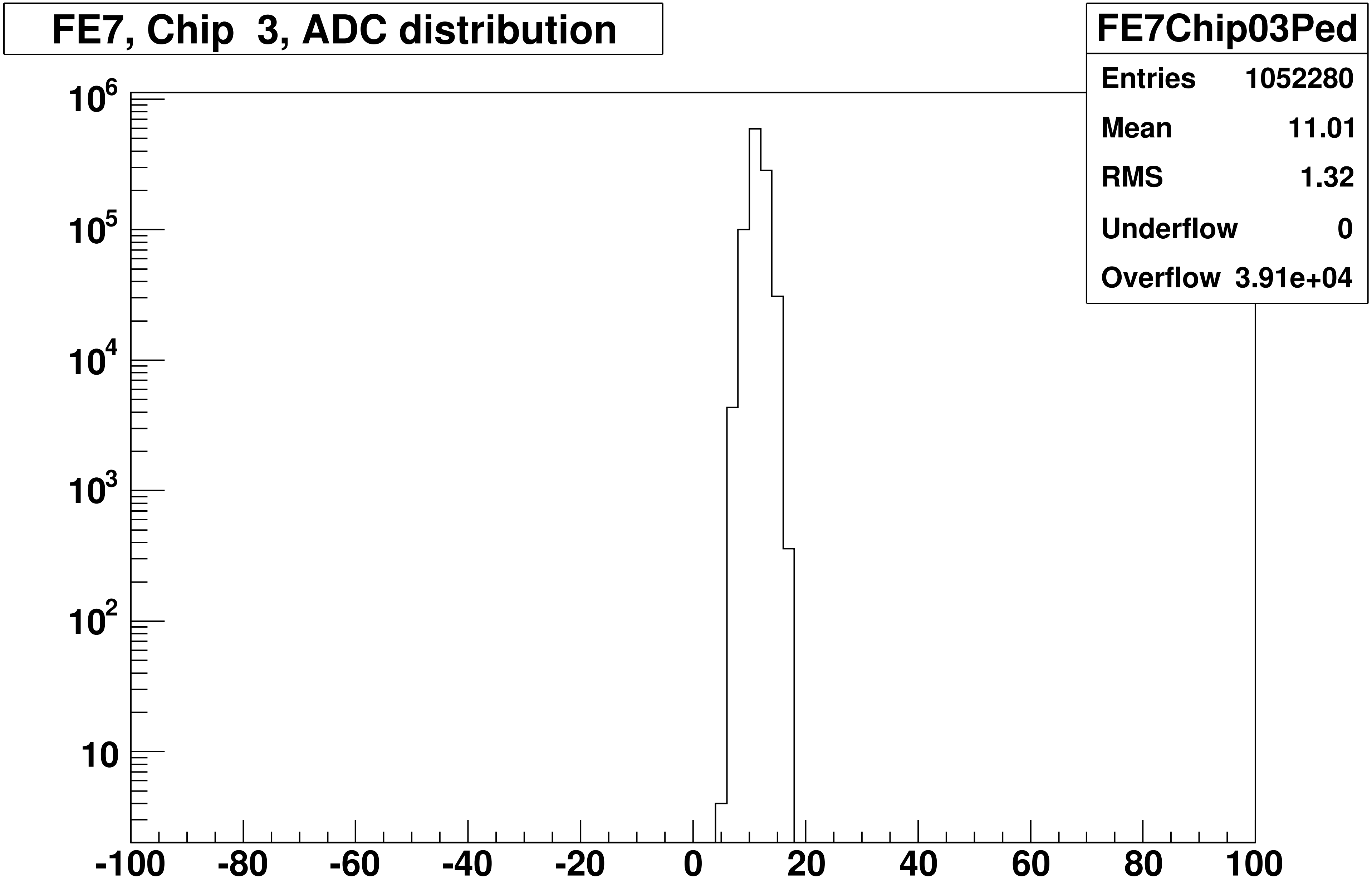
20000
25000



FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 1052280
Mean 11.01
RMS 1.32
Underflow 0
Overflow 3.91e+04
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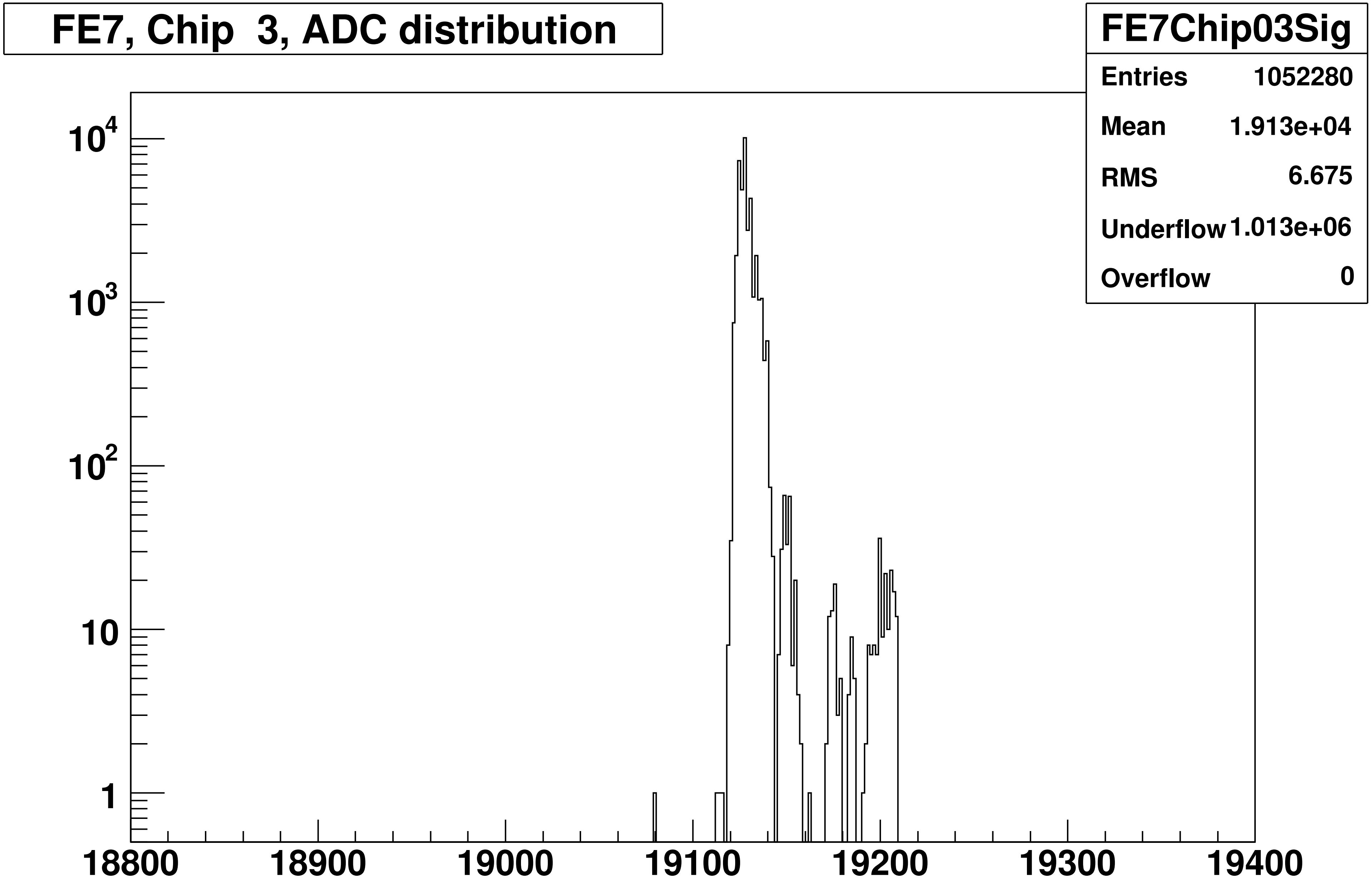
10^5
10^4
10^3
10^2
10
-100 -80 -60 -40 -20 0 20 40 60 80 100


FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 1052280
Mean 1.913e+04
RMS 6.675
Underflow 1.013e+06
Overflow 0
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10^3
10^2
10
1
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18900
19000
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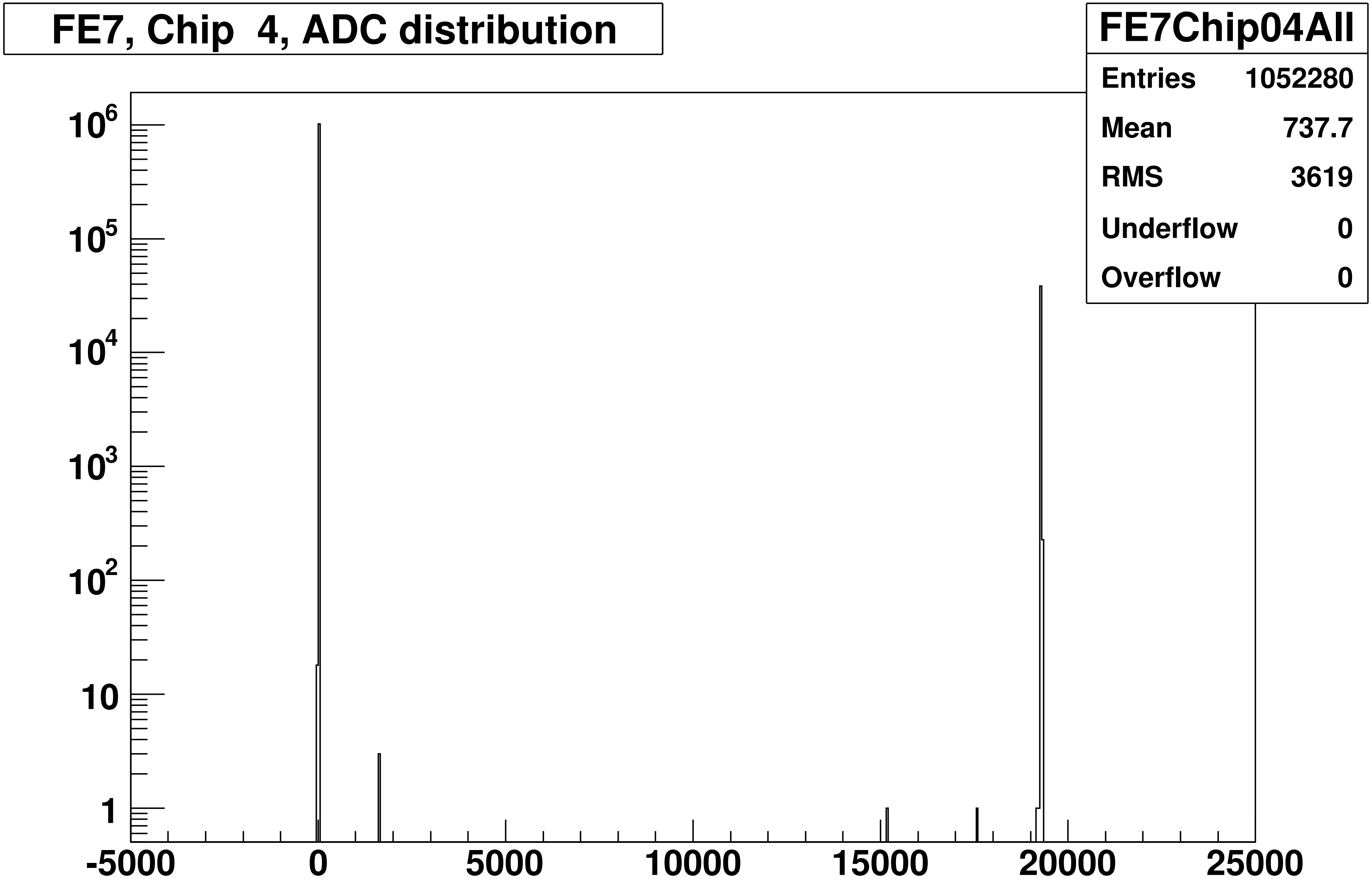
19200
19300
19400



FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 1052280
Mean 737.7
RMS 3619
Underflow 0
Overflow 0
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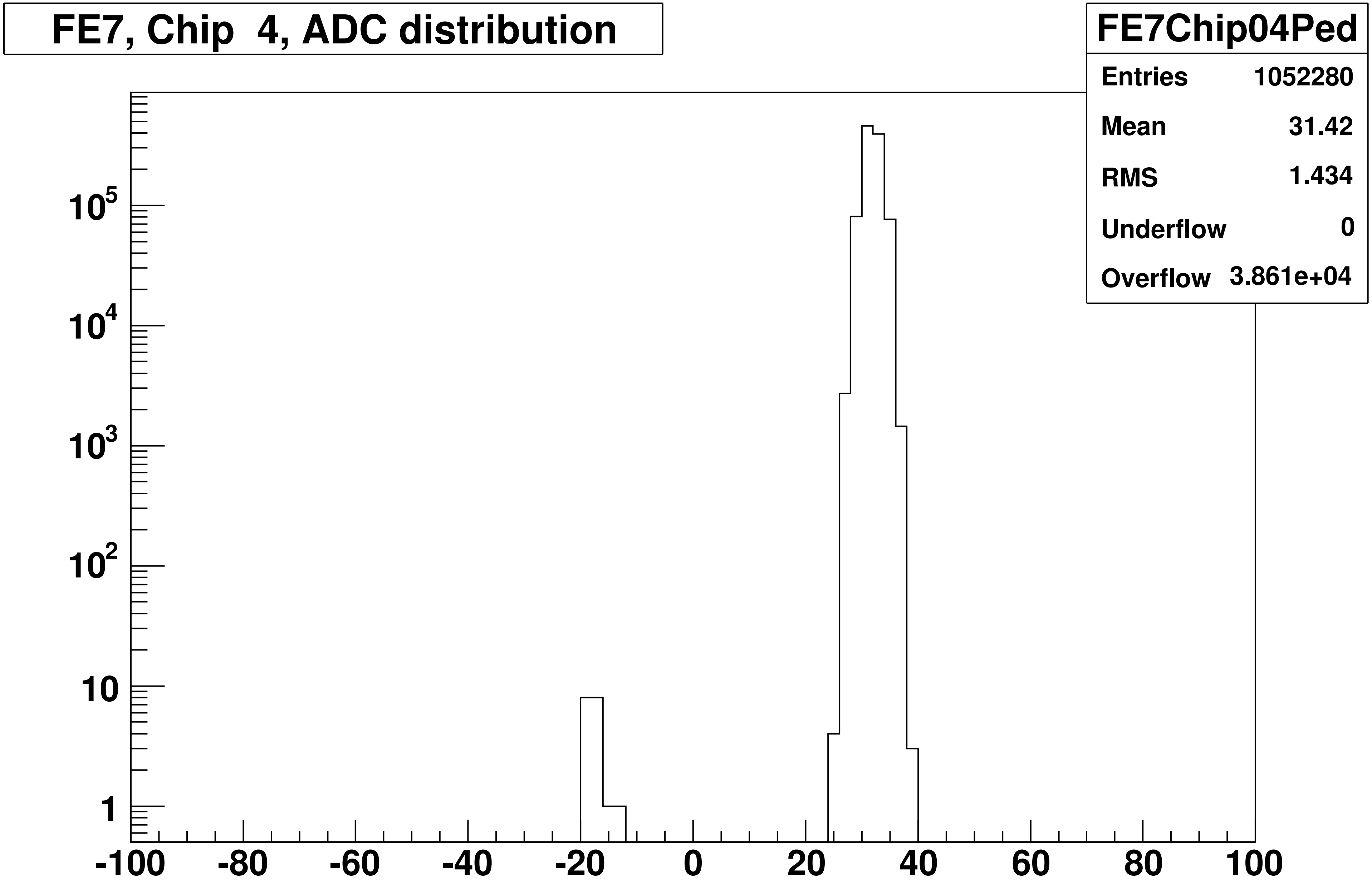
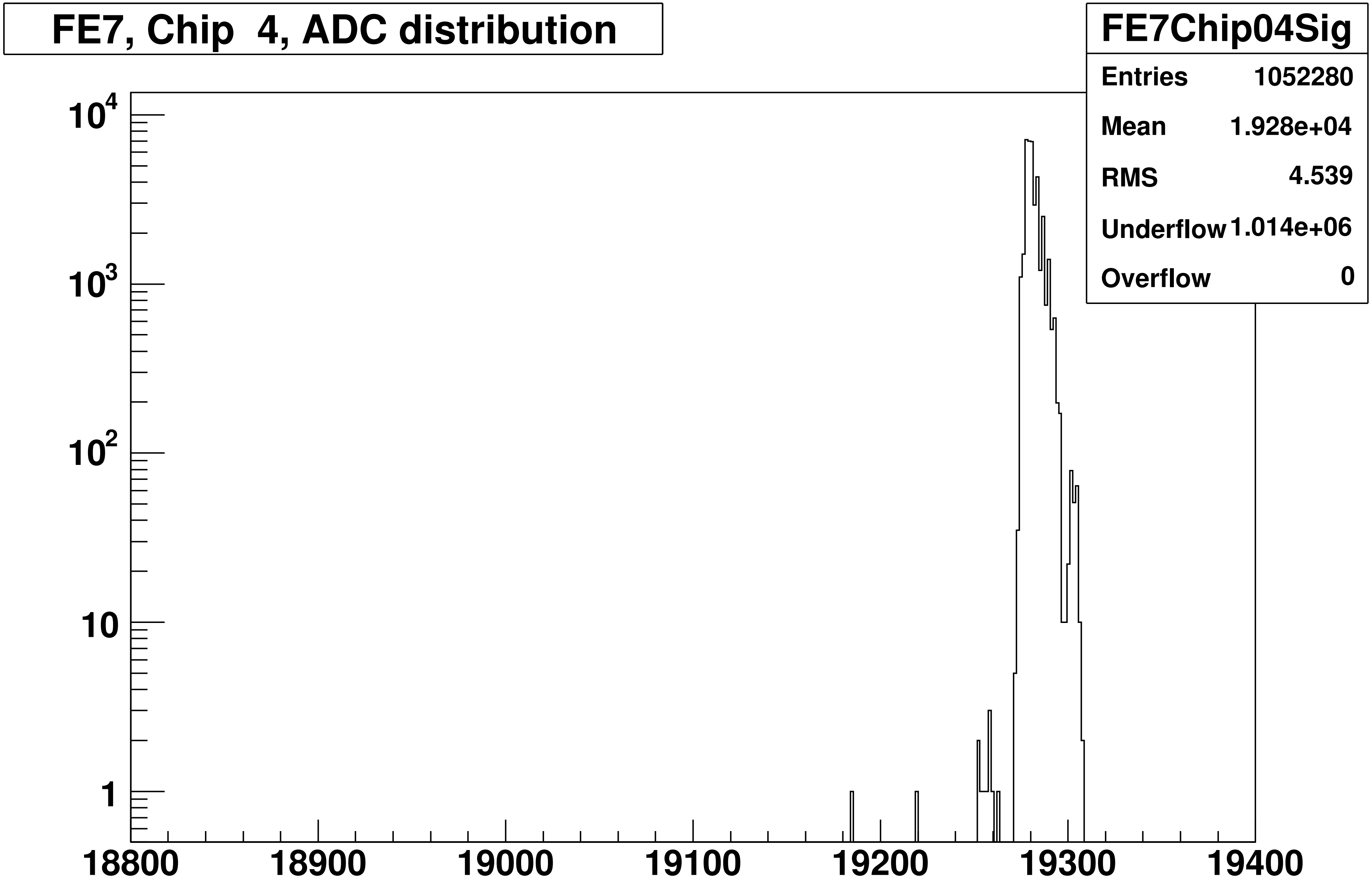
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 1052280
Mean 31.42
RMS 1.434
Underflow 0
Overflow 3.861e+04
10^5
10^4
10^3
10^2
10
1
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 1052280
Mean 1.928e+04
RMS 4.539
Underflow 1.014e+06
Overflow 0
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10^3
10^2
10
1
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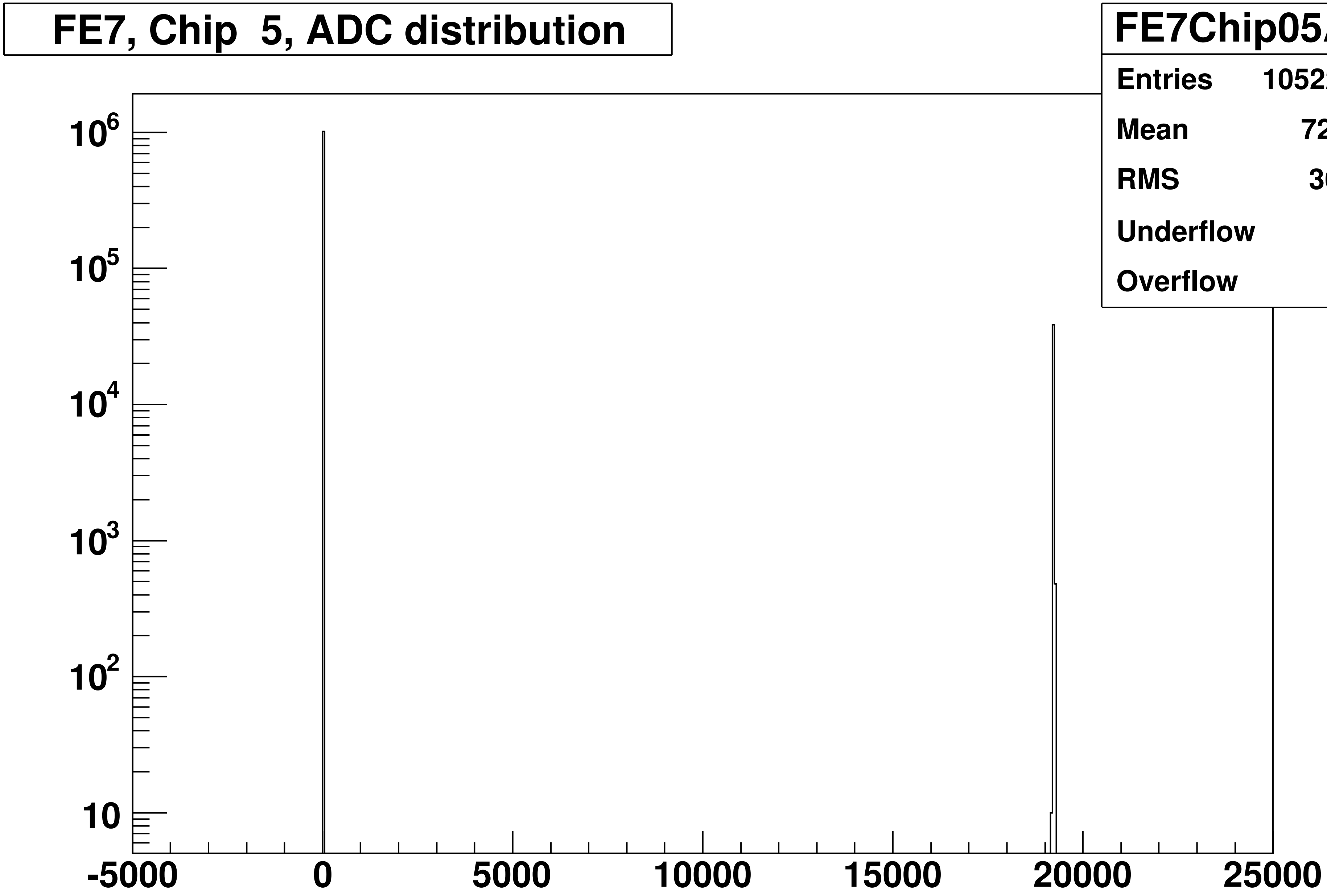
19400



FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 1052280
Mean 729.3
RMS 3630
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
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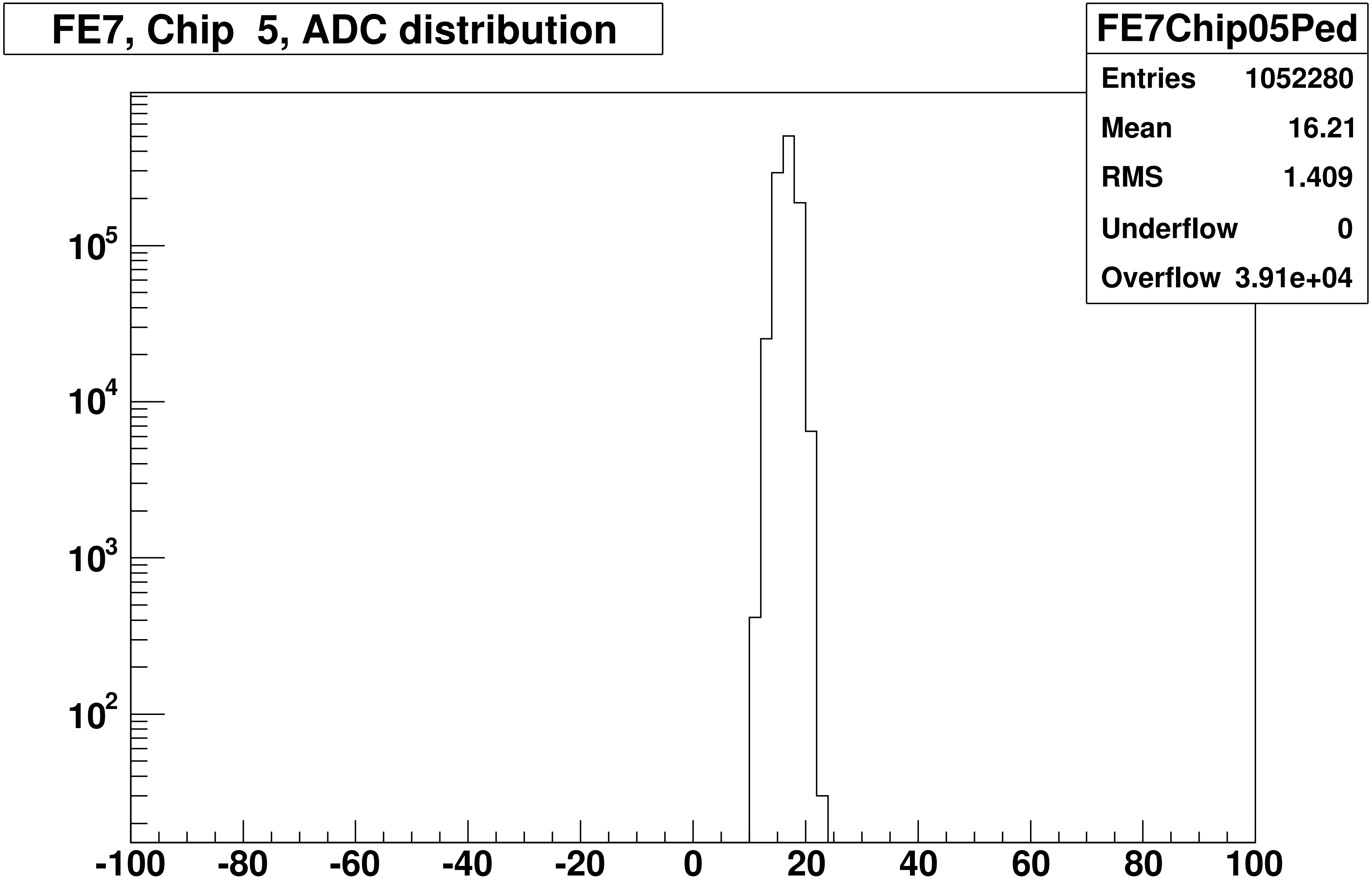
20000
25000


FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 1052280
Mean 16.21
RMS 1.409
Underflow 0
Overflow 3.91e+04
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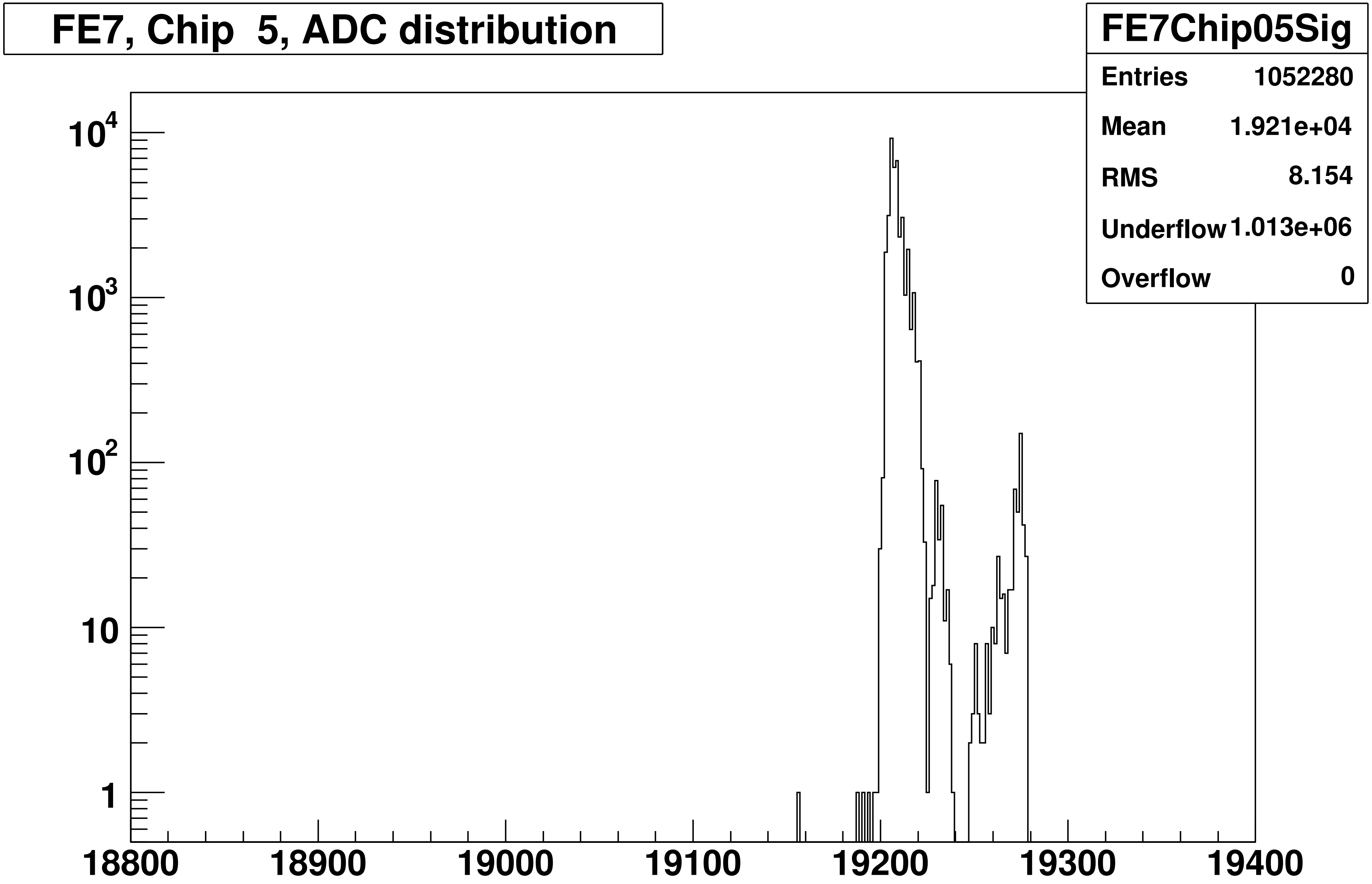
10^4
10^3
10^2
-100 -80 -60 -40 -20 0 20 40 60 80 100



FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 1052280
Mean 1.921e+04
RMS 8.154
Underflow 1.013e+06
Overflow 0
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10^3
10^2
10
1
18800
18900
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19200
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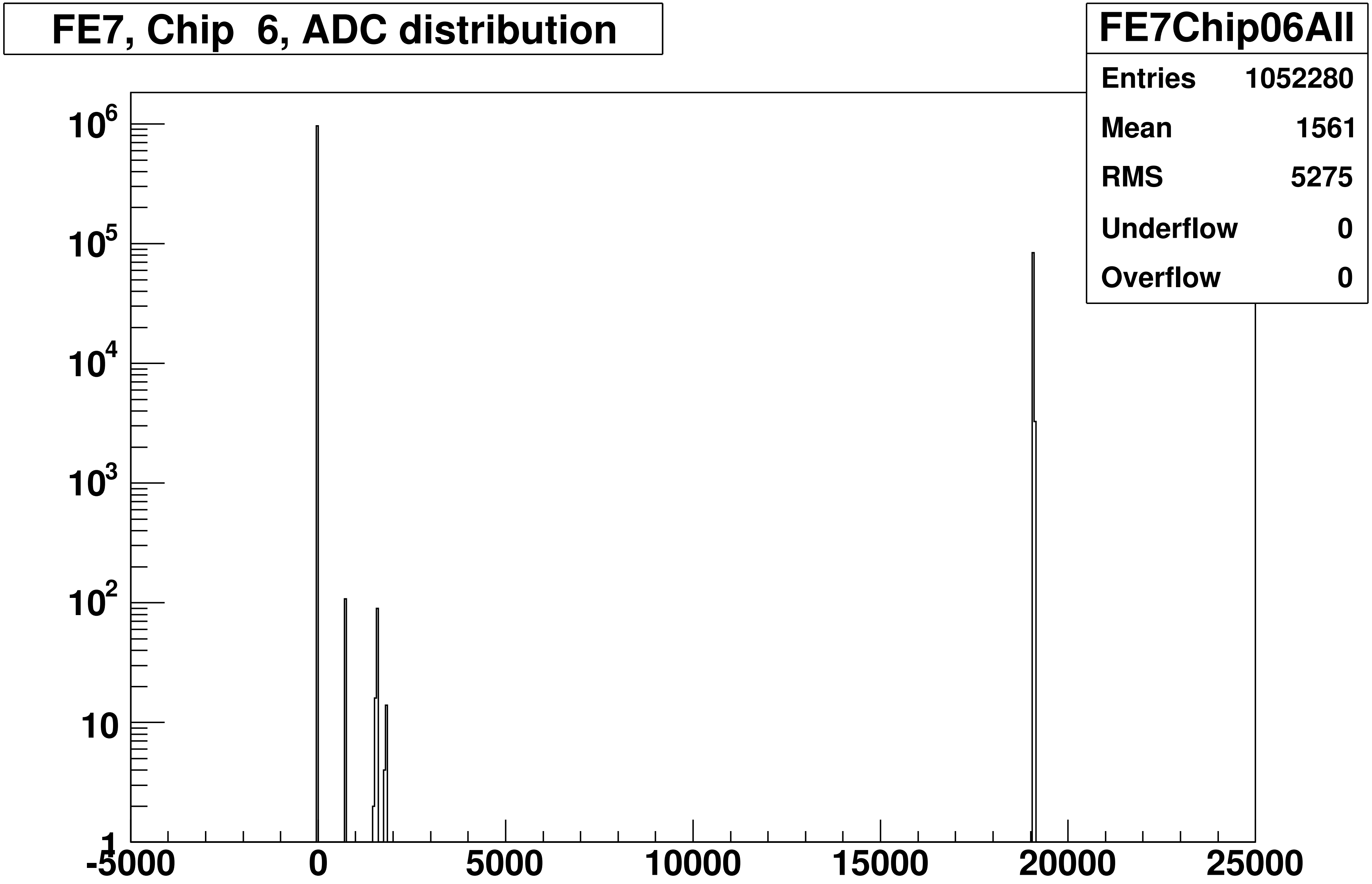
19400



FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 1052280
Mean 1561
RMS 5275
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
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1
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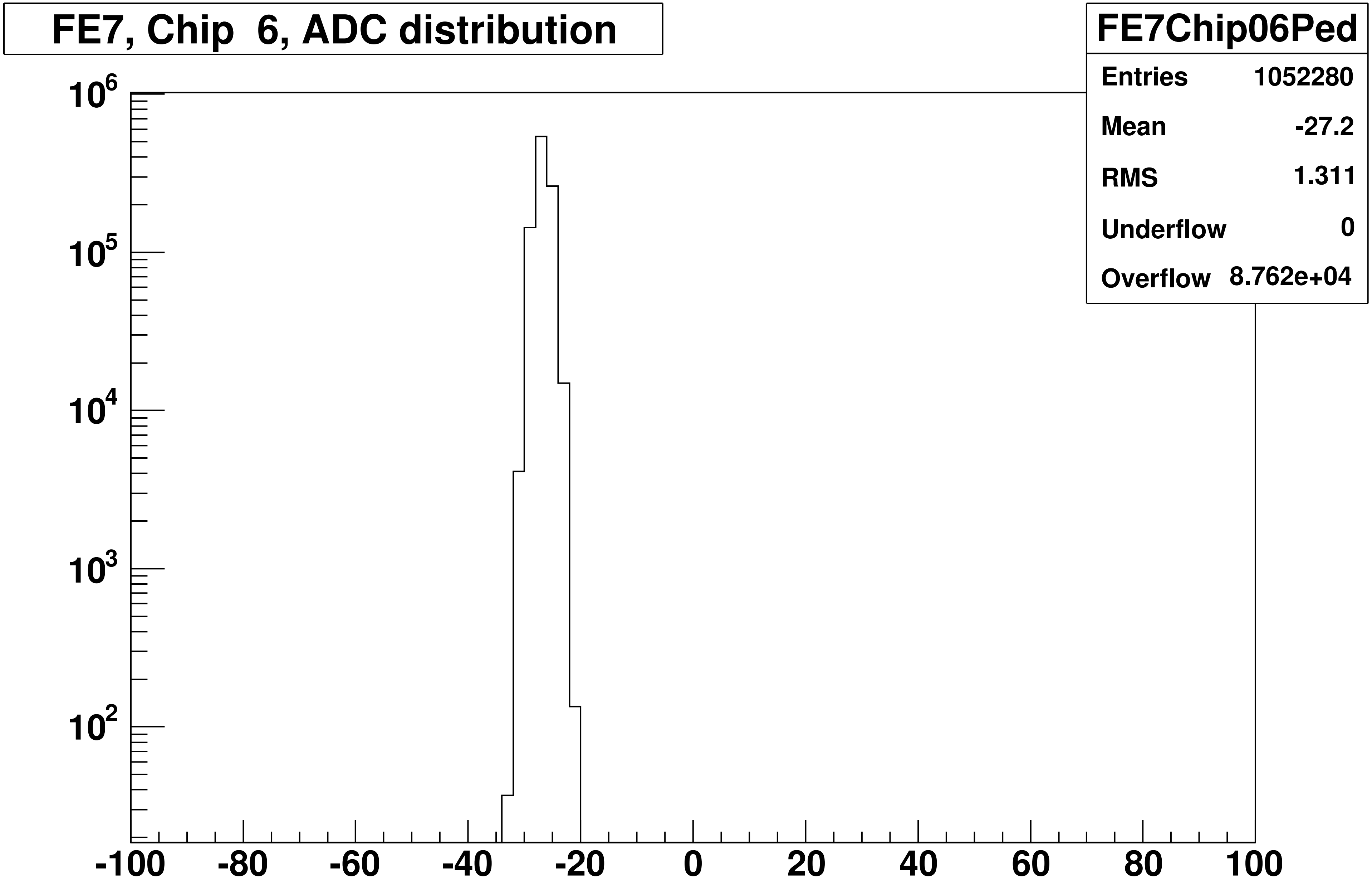
25000



FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 1052280
Mean -27.2
RMS 1.311
Underflow 0
Overflow 8.762e+04
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10^5
10^4
10^3
10^2
-100
-80
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-20
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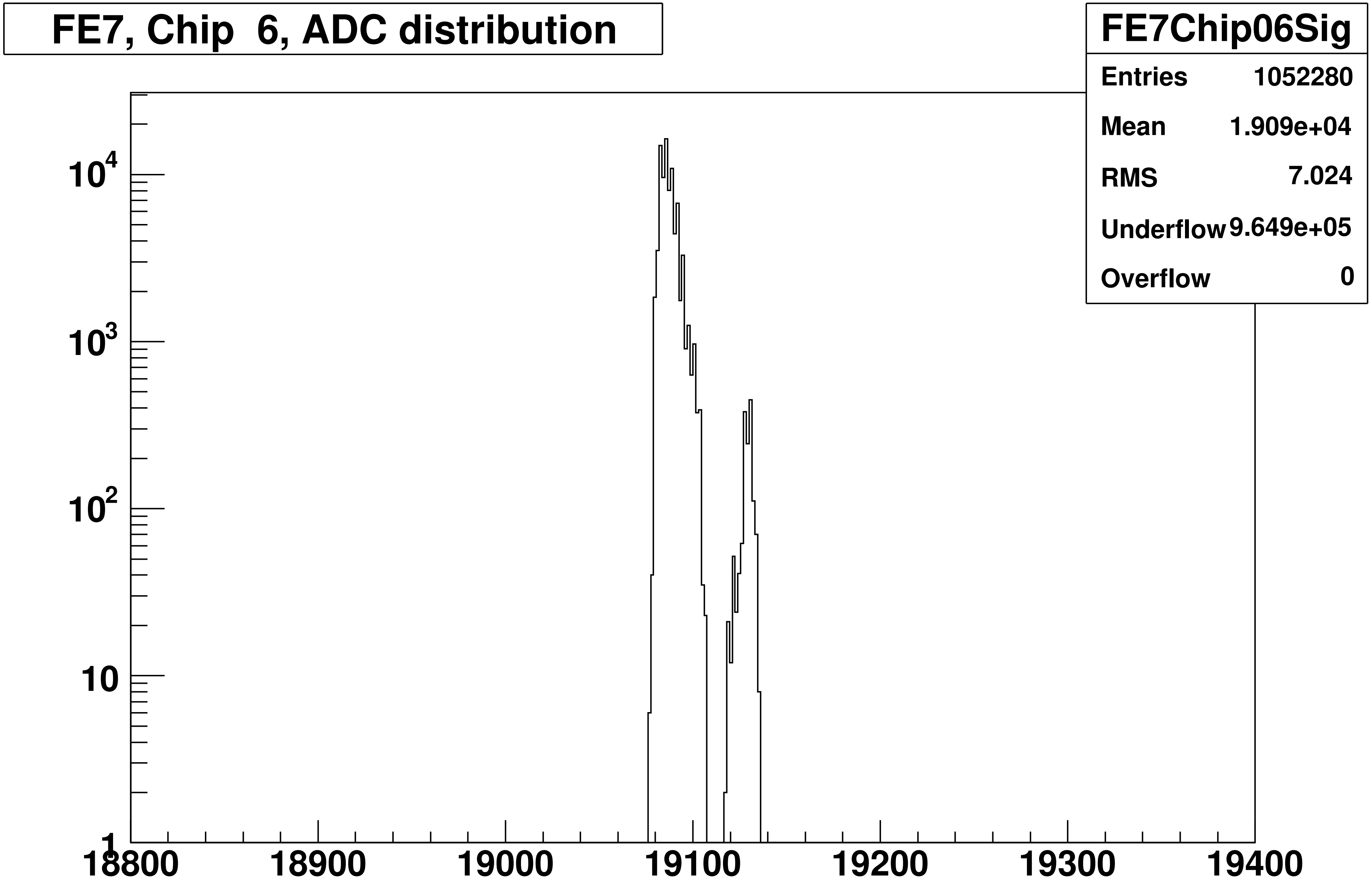
FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 1052280
Mean 1.909e+04
RMS 7.024
Underflow 9.649e+05
Overflow 0
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10^3
10^2
10
1
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18900
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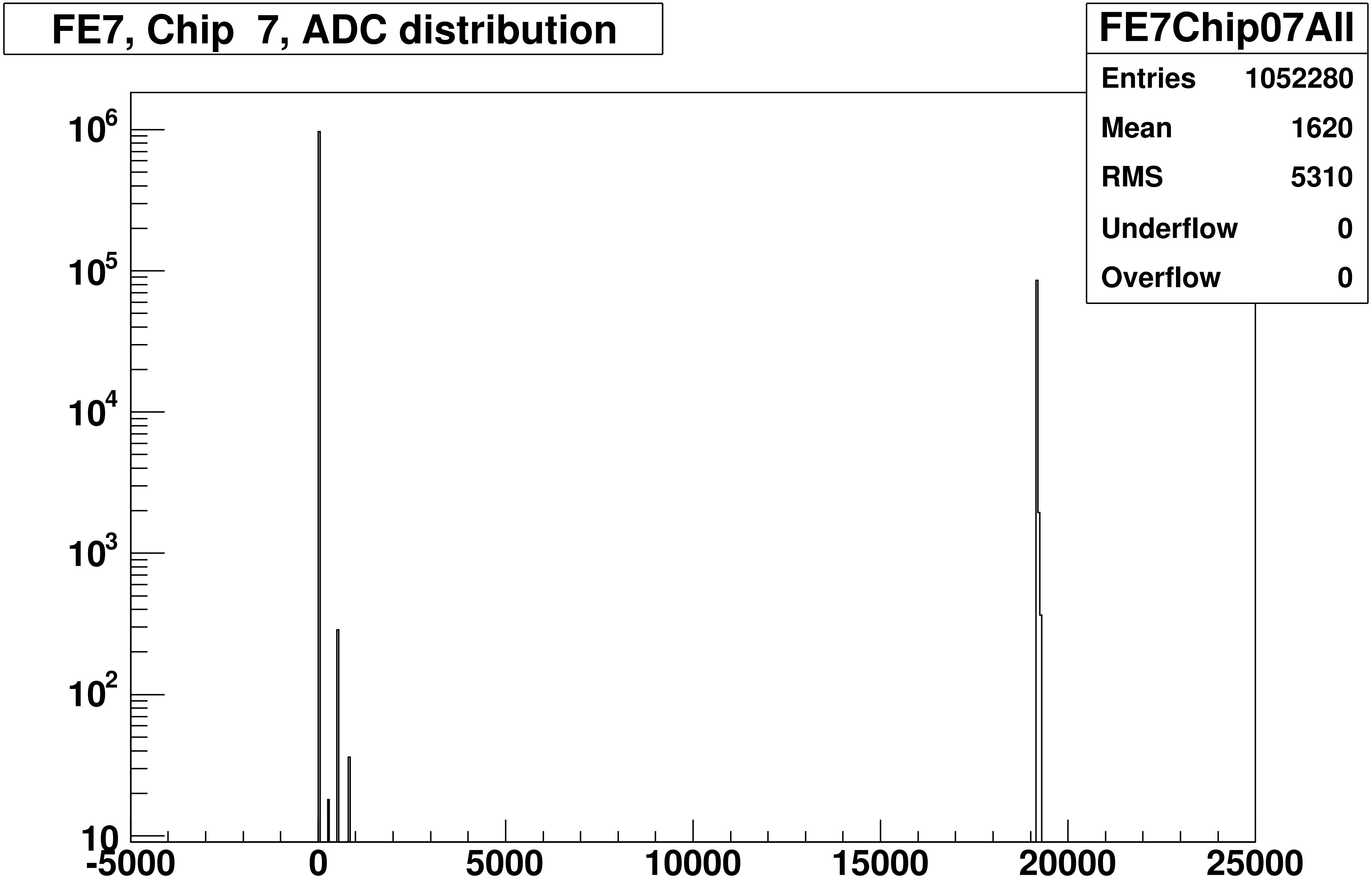

FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 1052280
Mean 1620
RMS 5310
Underflow 0
Overflow 0
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10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
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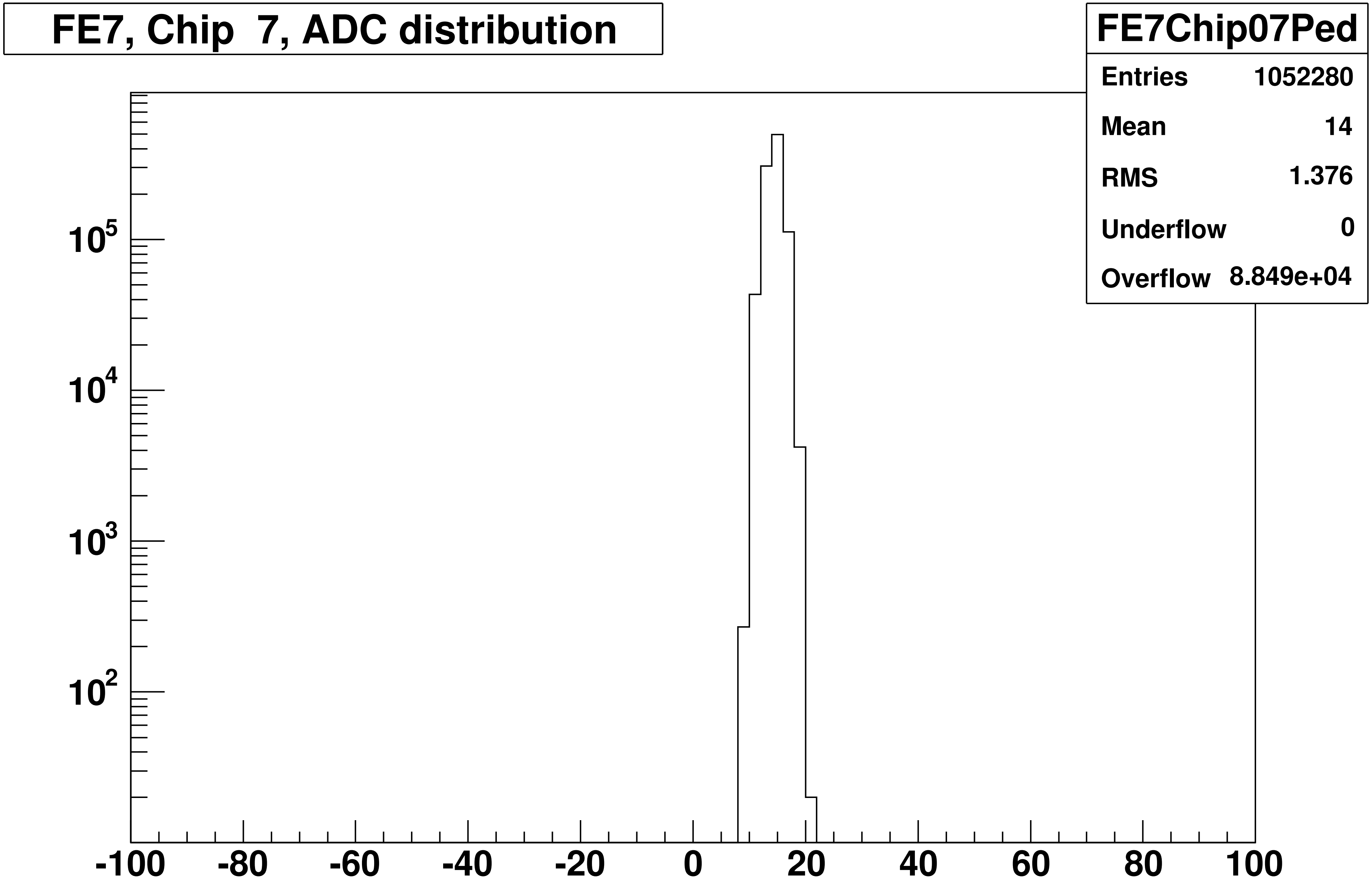
25000


FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 1052280
Mean 14
RMS 1.376
Underflow 0
Overflow 8.849e+04
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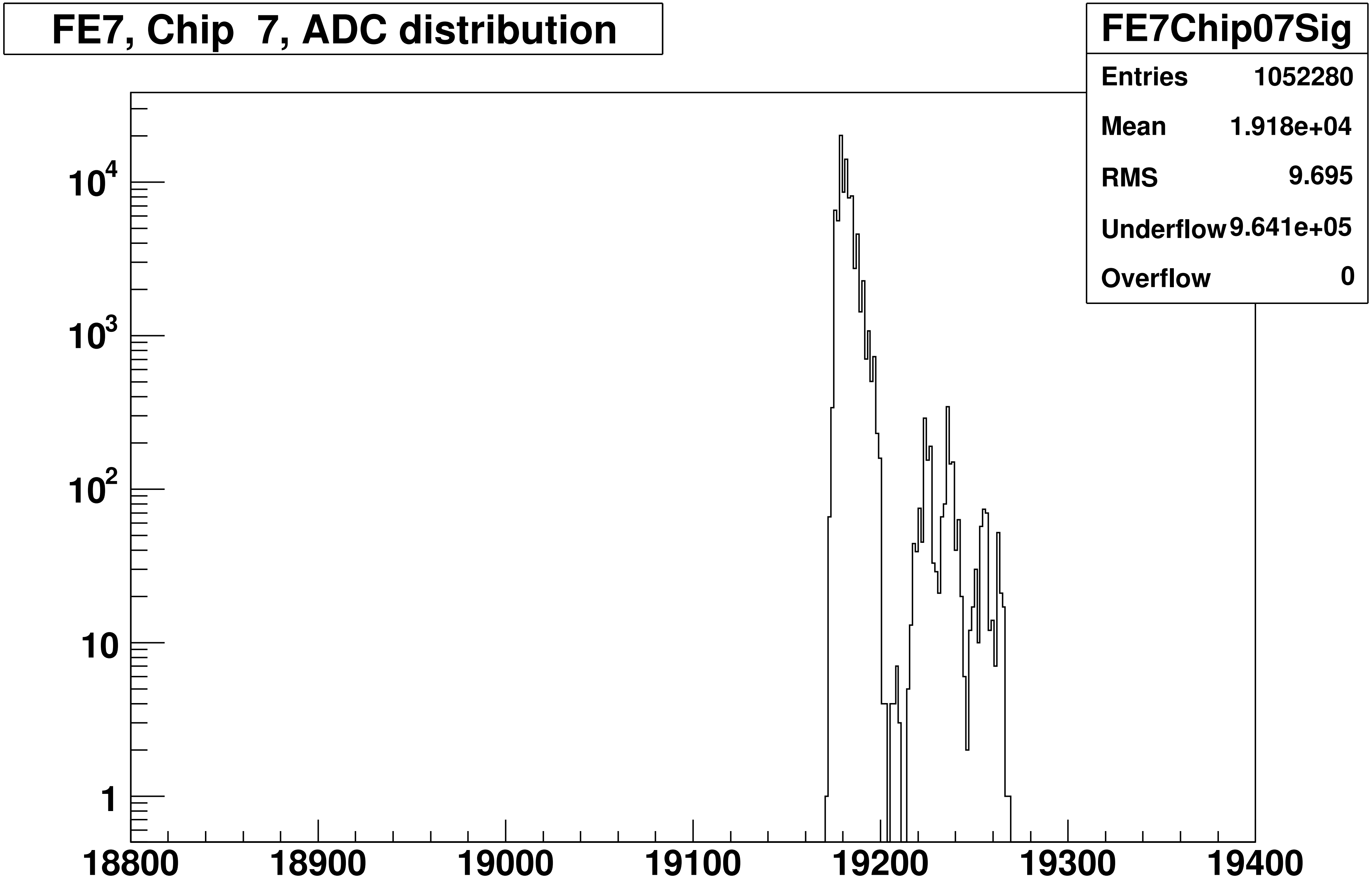
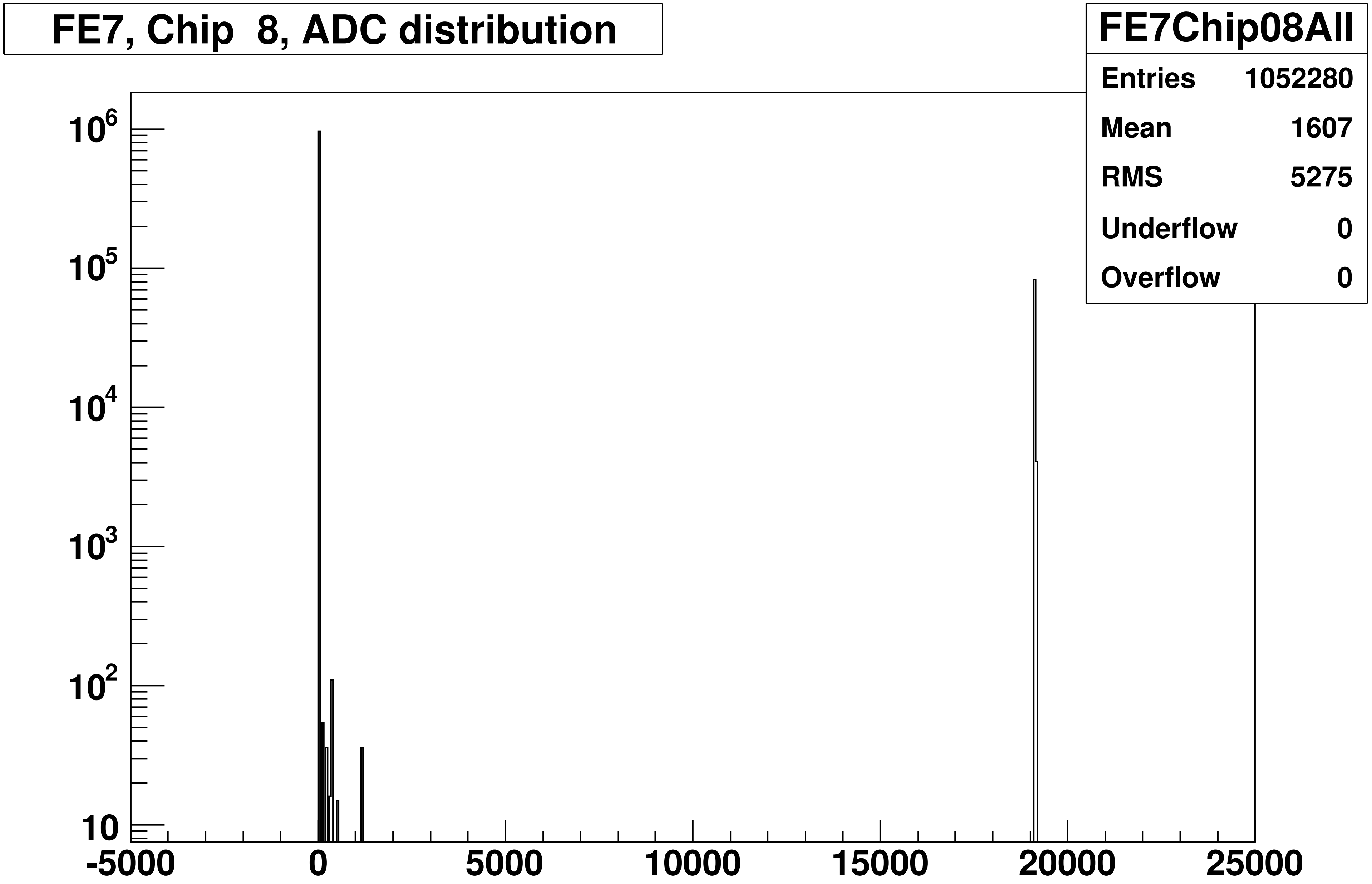
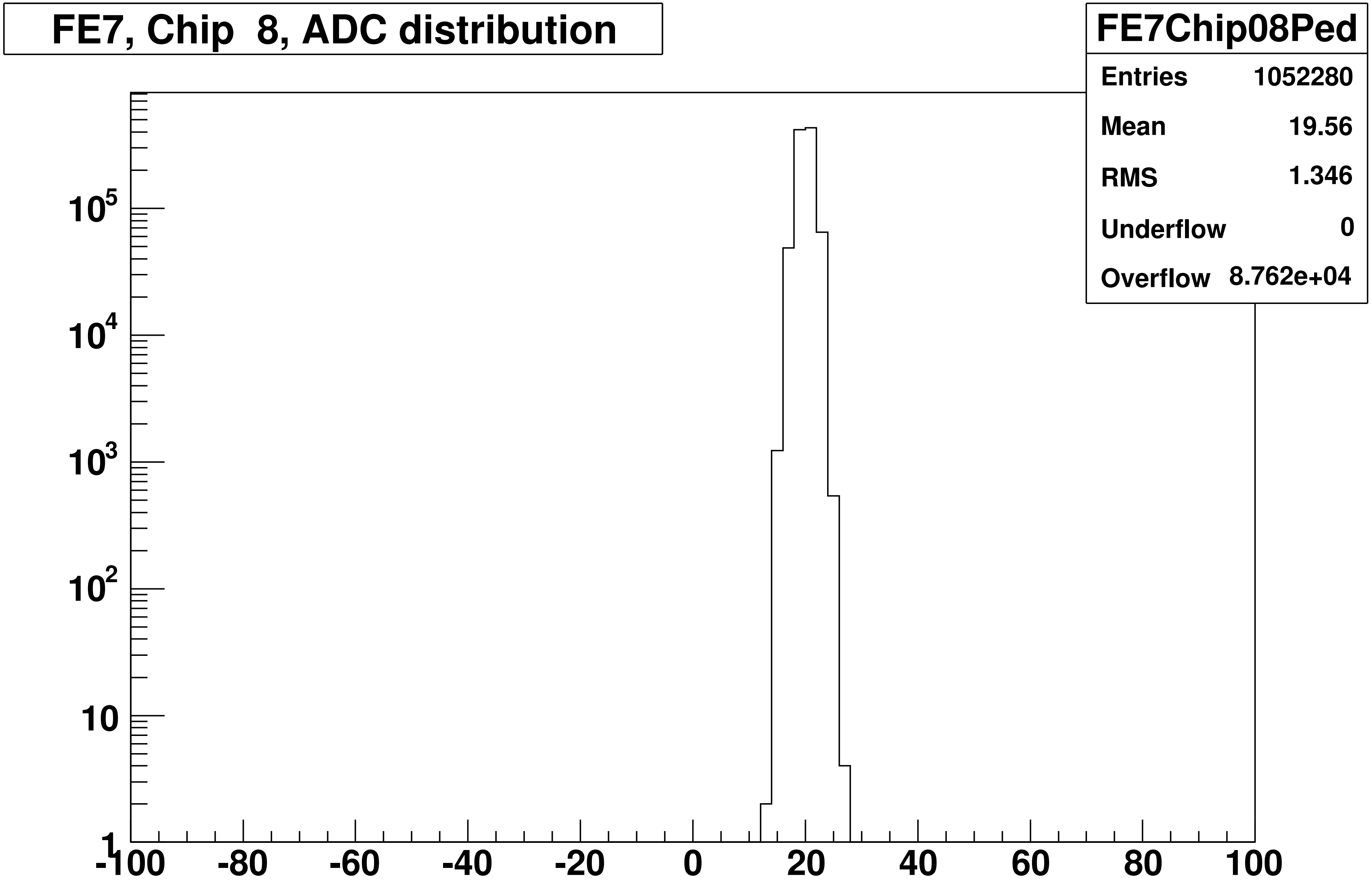
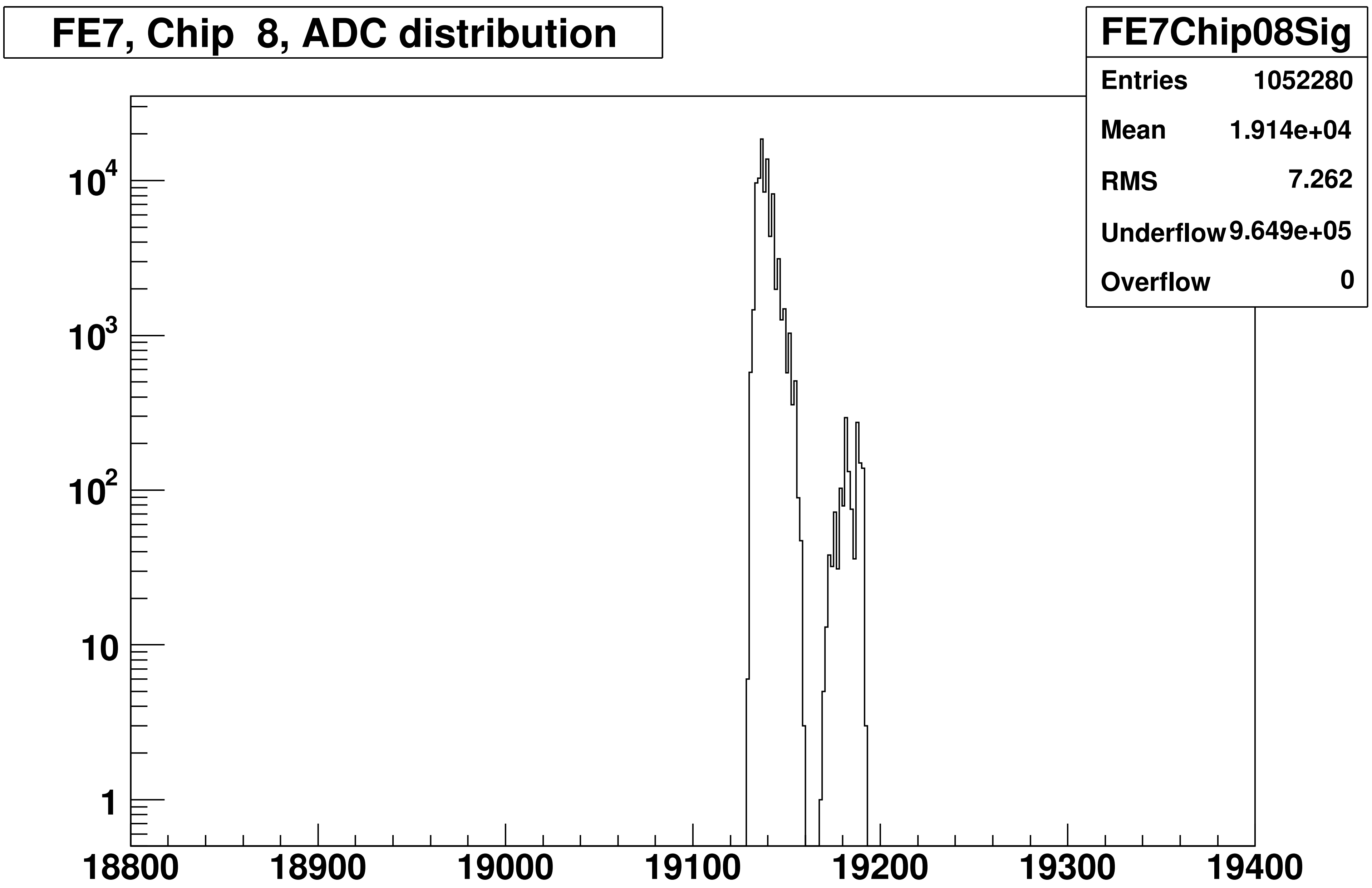
80
100

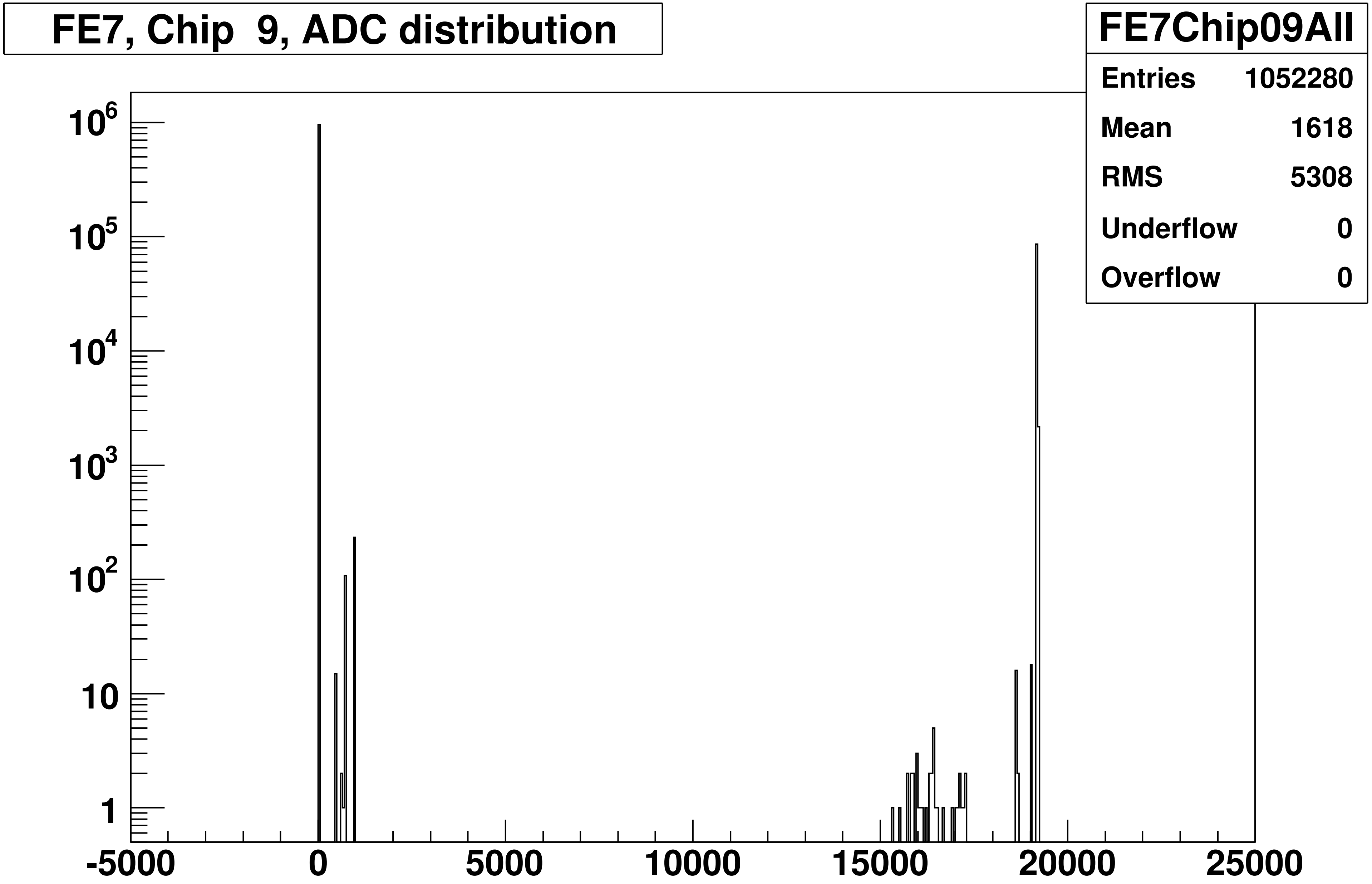

FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 1052280
Mean 1.918e+04
RMS 9.695
Underflow 9.641e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400



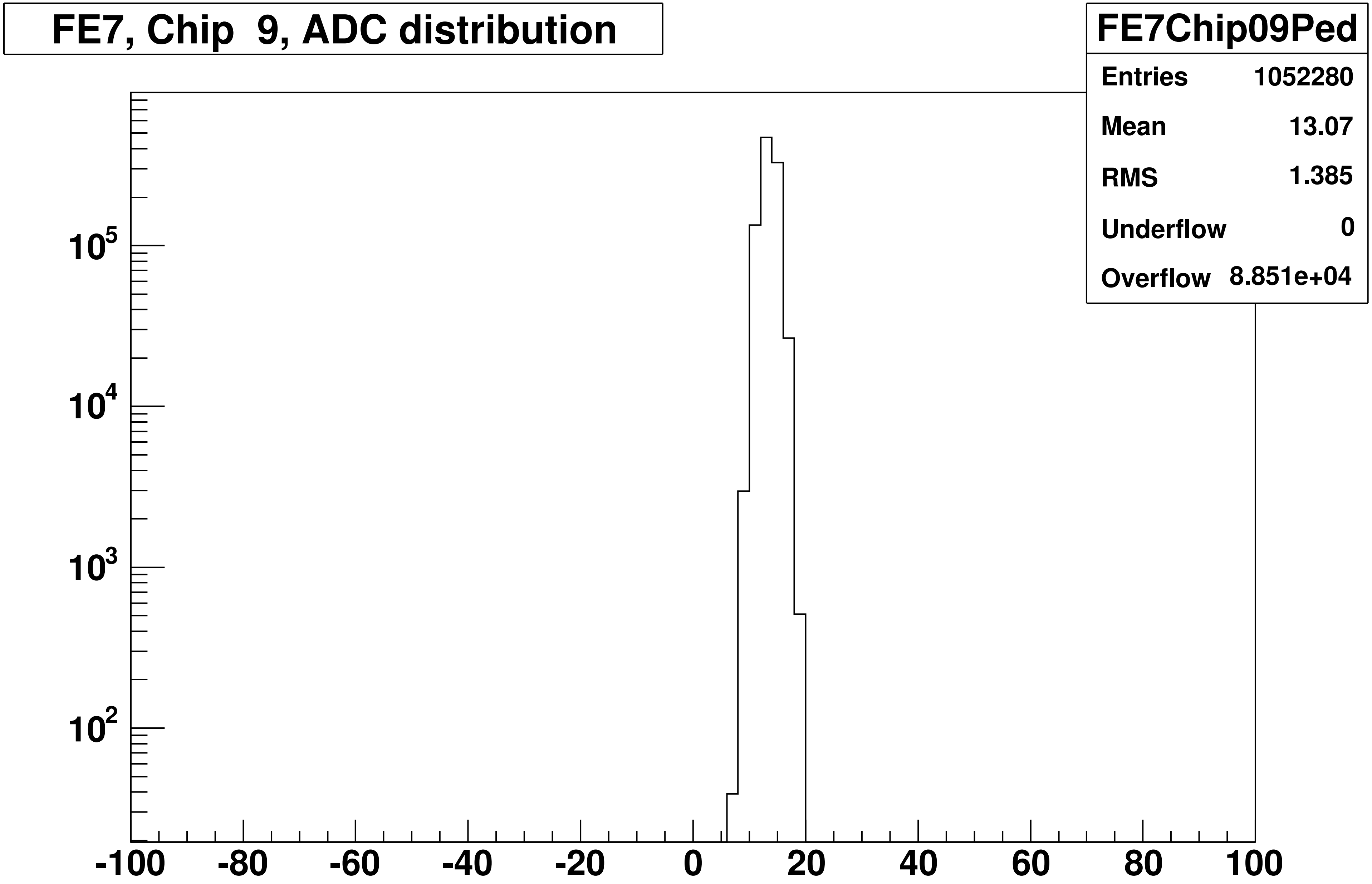
FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 1052280
Mean 1607
RMS 5275
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
10^6
-5000
0
5000
10000
15000
20000
25000

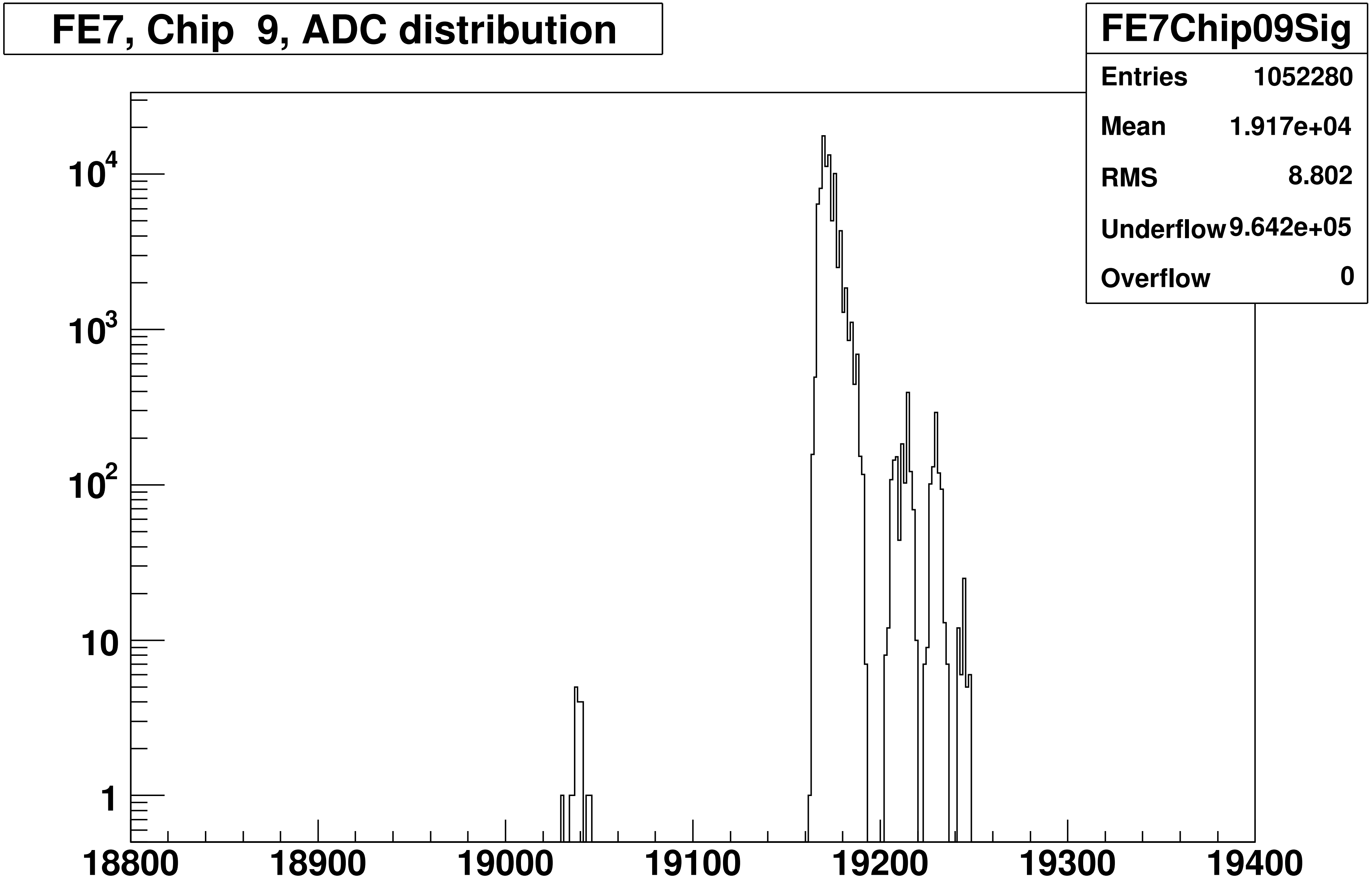

FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 1052280
Mean 19.56
RMS 1.346
Underflow 0
Overflow 8.762e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 1052280
Mean 1.914e+04
RMS 7.262
Underflow 9.649e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

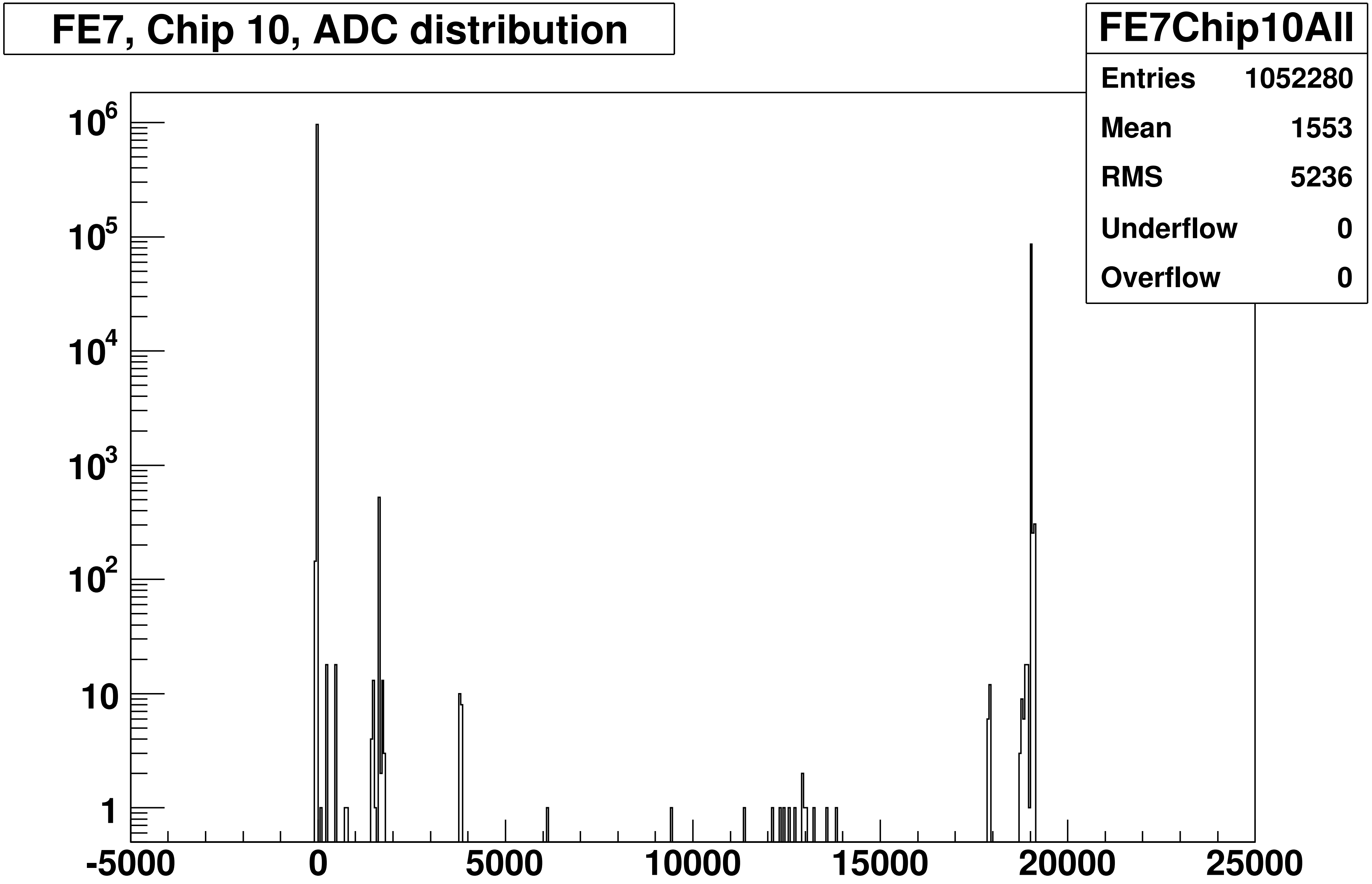


FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 1052280
Mean 1618
RMS 5308
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

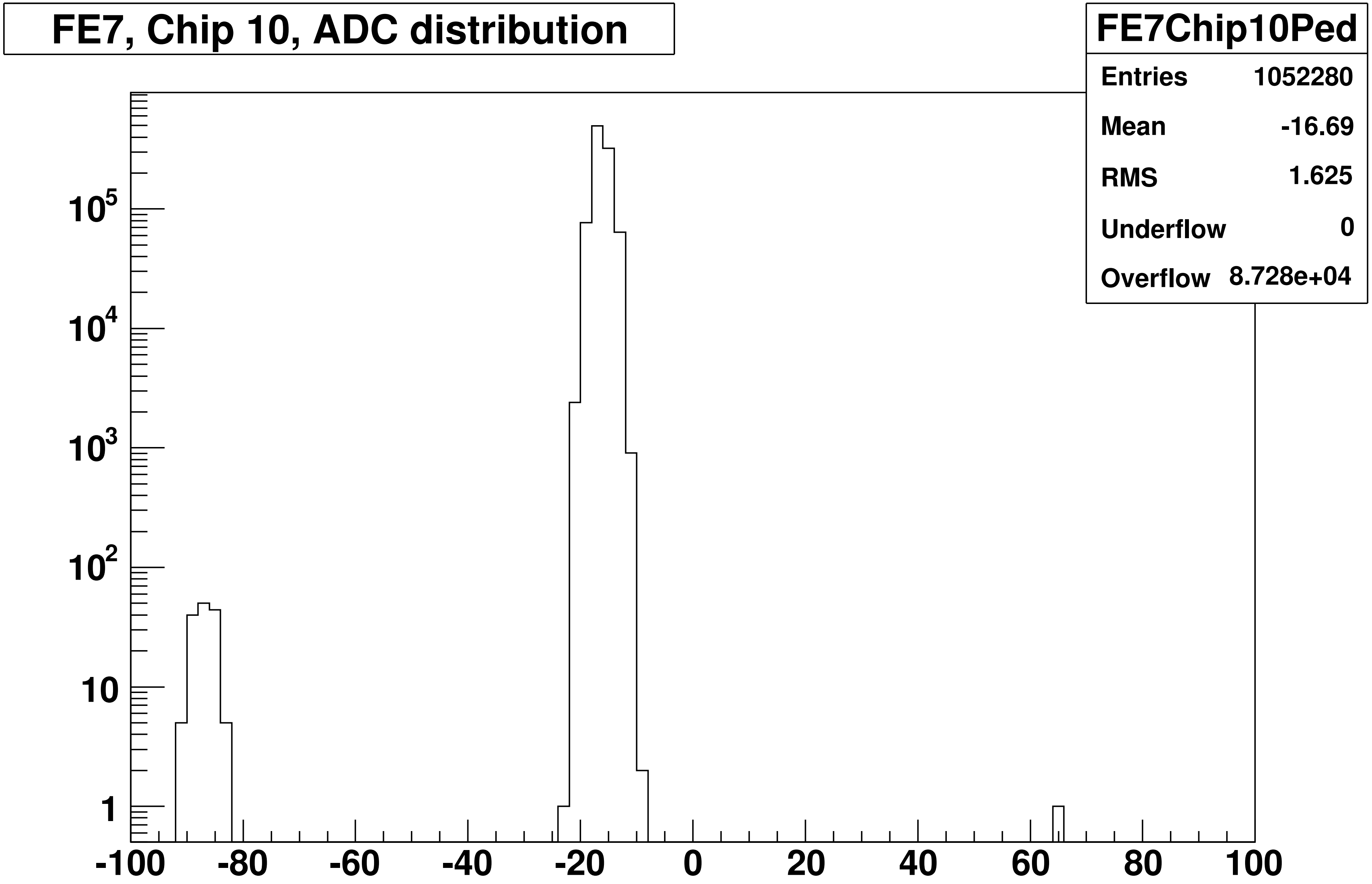

FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 1052280
Mean 13.07
RMS 1.385
Underflow 0
Overflow 8.851e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
0
20
40
60
80
100



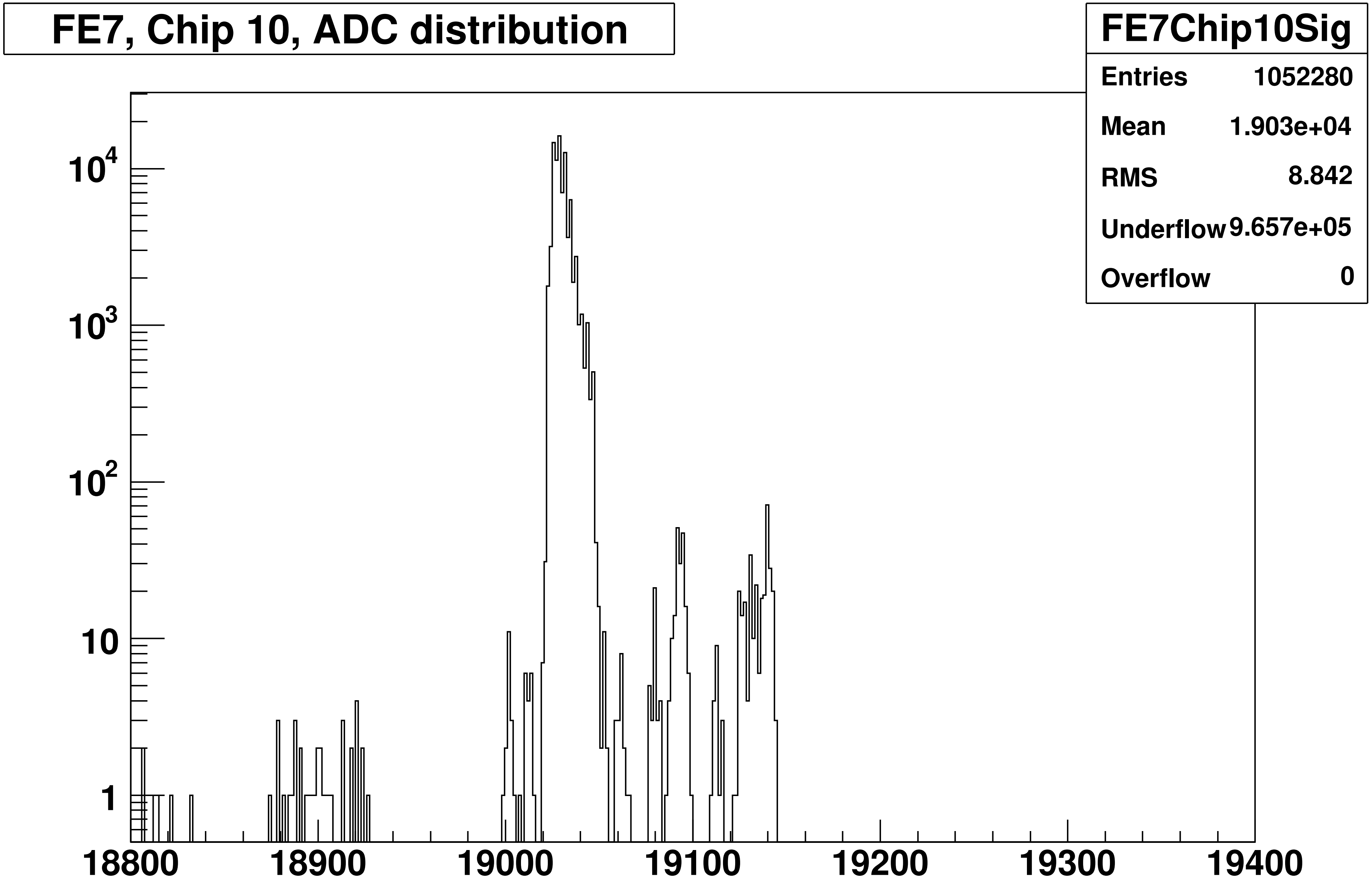
FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 1052280
Mean 1.917e+04
RMS 8.802
Underflow 9.642e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

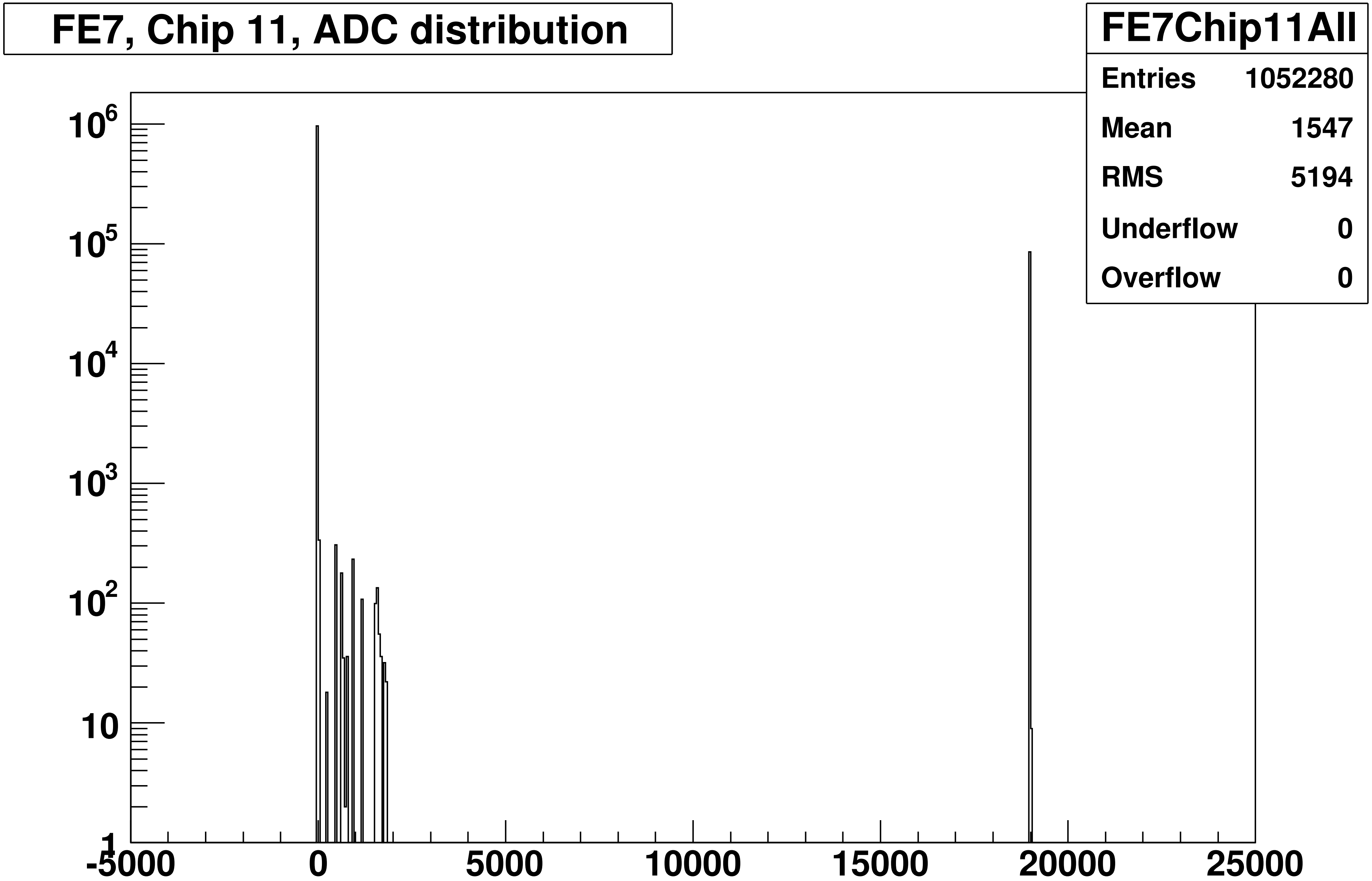


FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 1052280
Mean 1553
RMS 5236
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

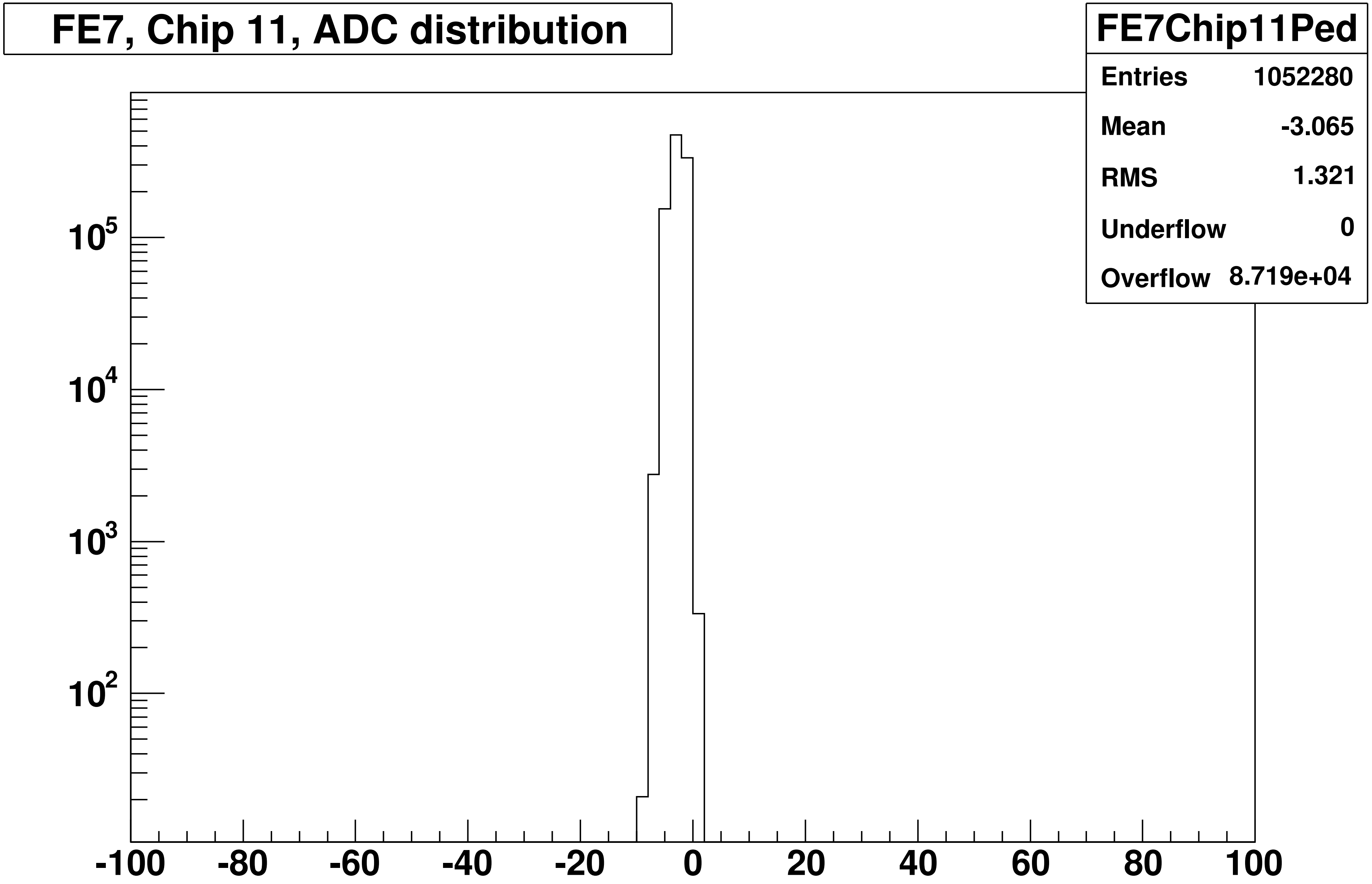


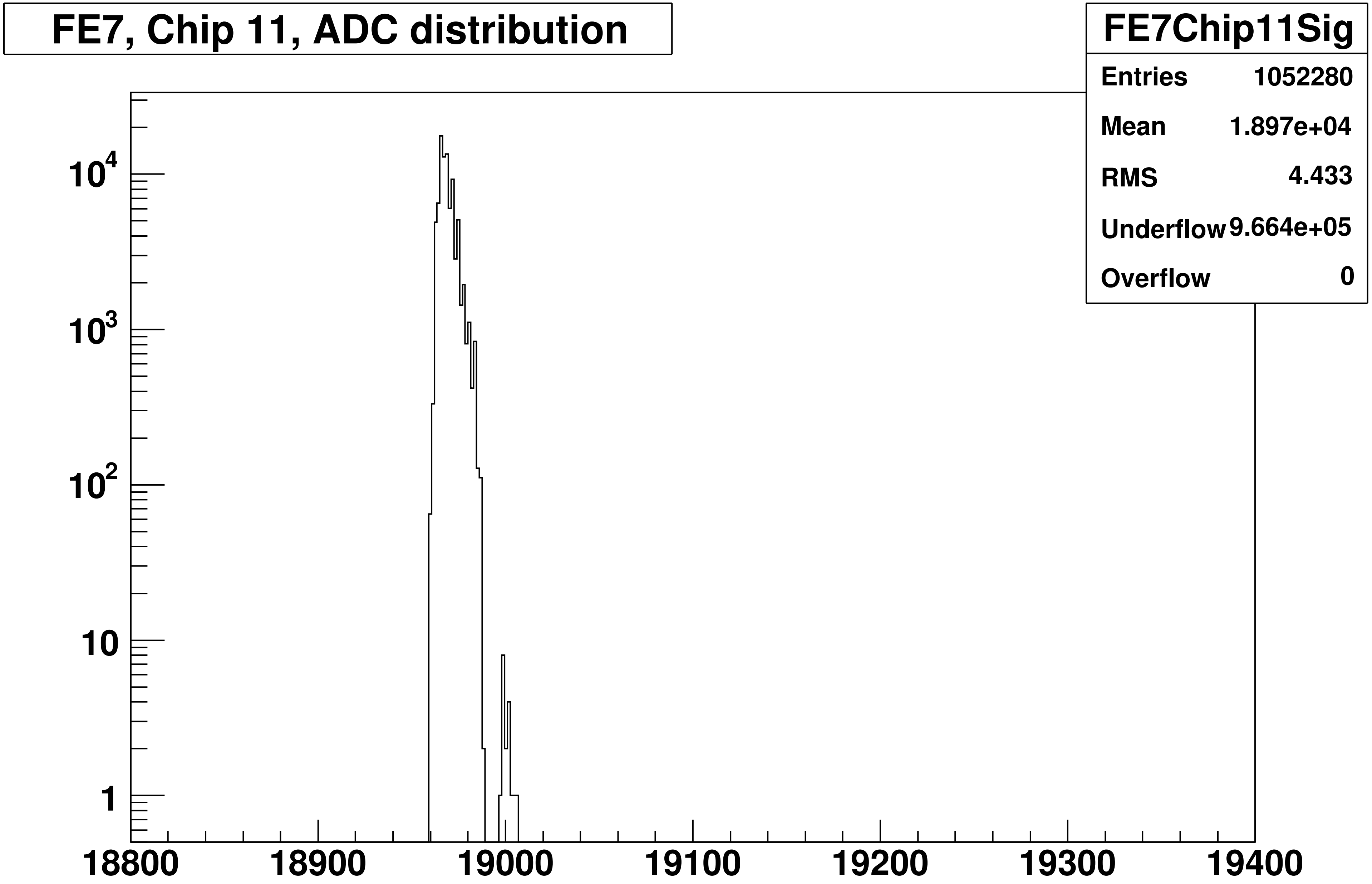
FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 1052280
Mean -16.69
RMS 1.625
Underflow 0
Overflow 8.728e+04
10^5
10^4
10^3
10^2
10
1
-100
-80
-60
-40
-20
0
20
40
60
80
100


FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 1052280
Mean 1.903e+04
RMS 8.842
Underflow 9.657e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400

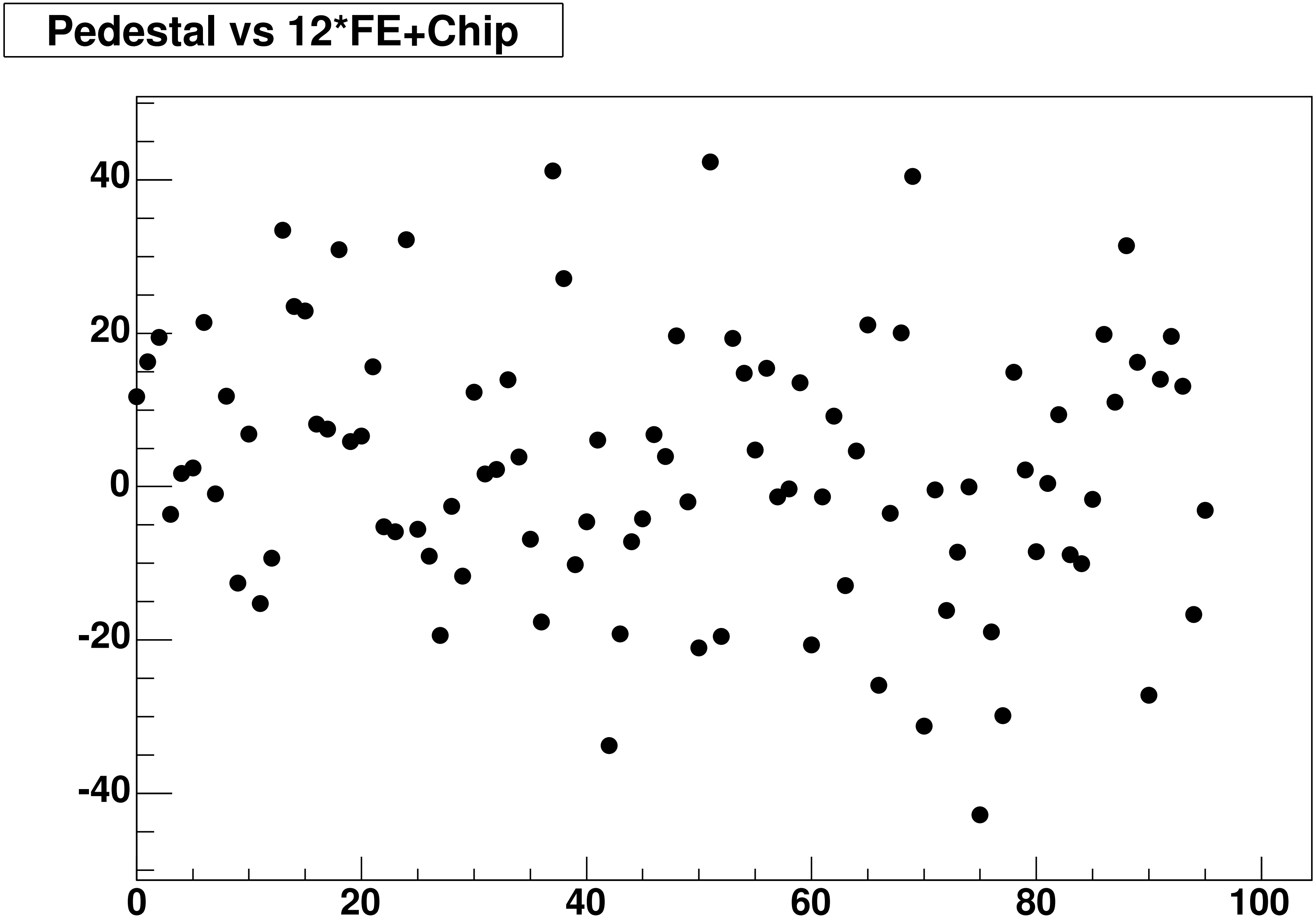


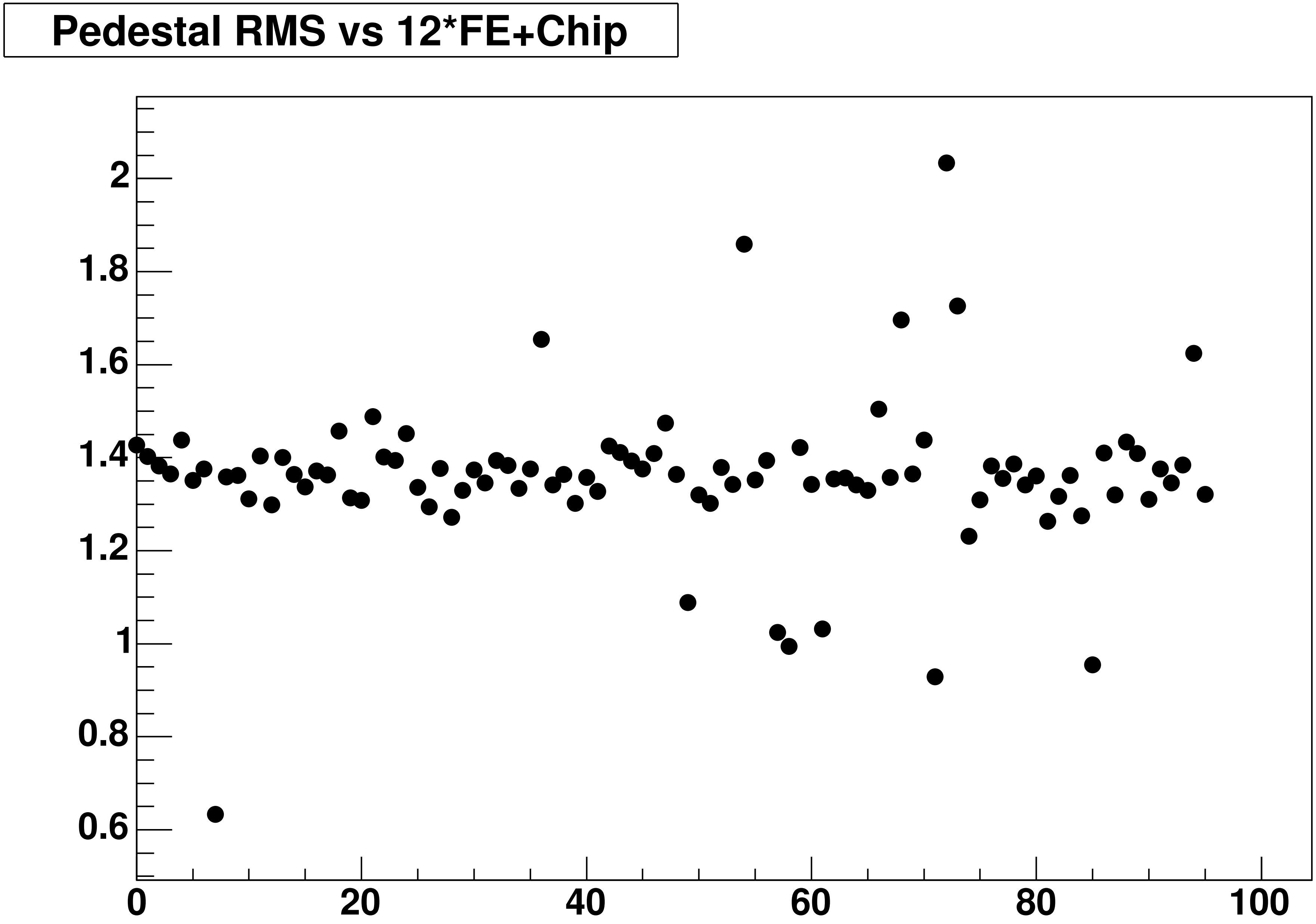
FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 1052280
Mean 1547
RMS 5194
Underflow 0
Overflow 0
10^6
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000

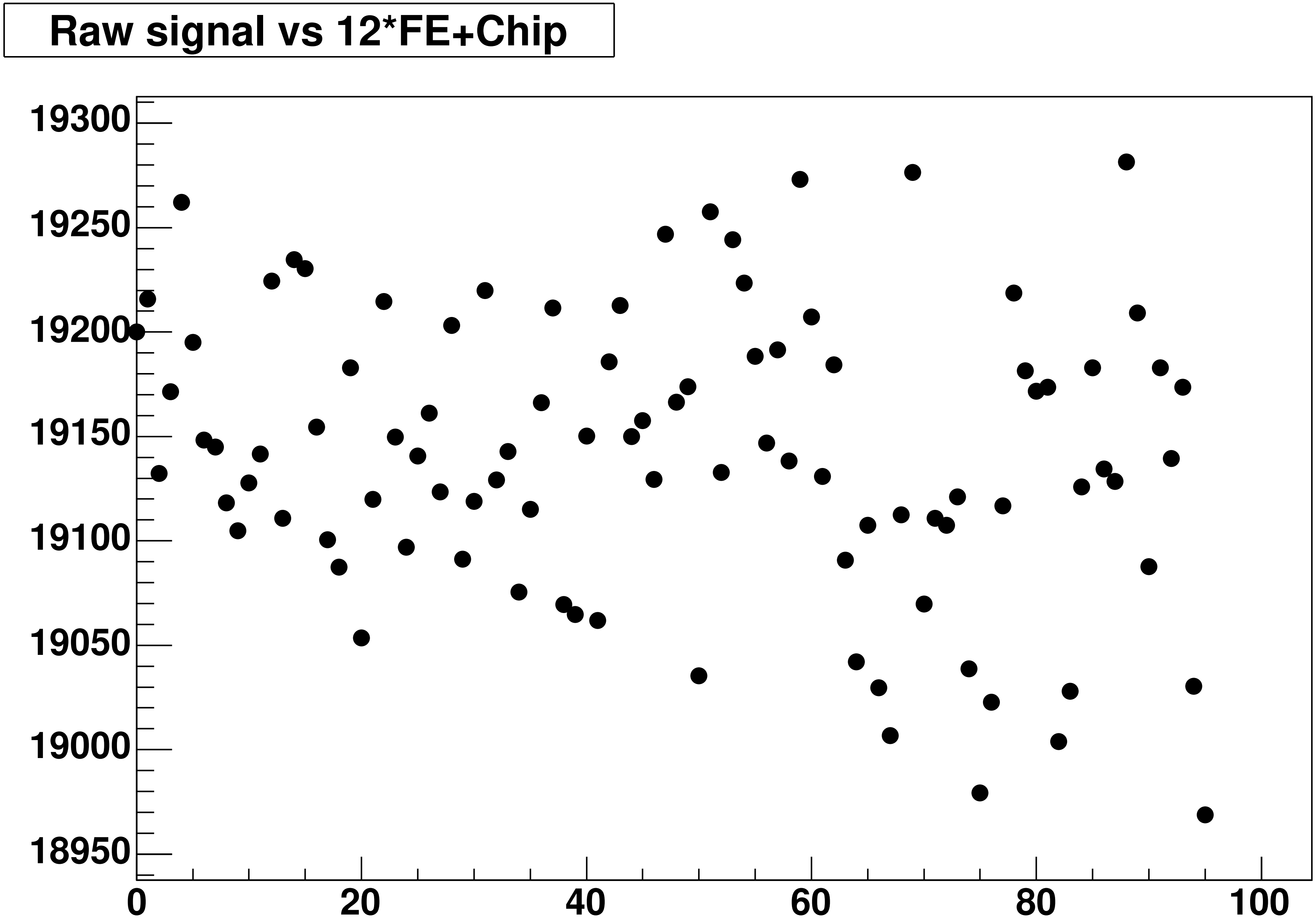

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 1052280
Mean -3.065
RMS 1.321
Underflow 0
Overflow 8.719e+04
10^5
10^4
10^3
10^2
-100
-80
-60
-40
-20
0
20
40
60
80
100

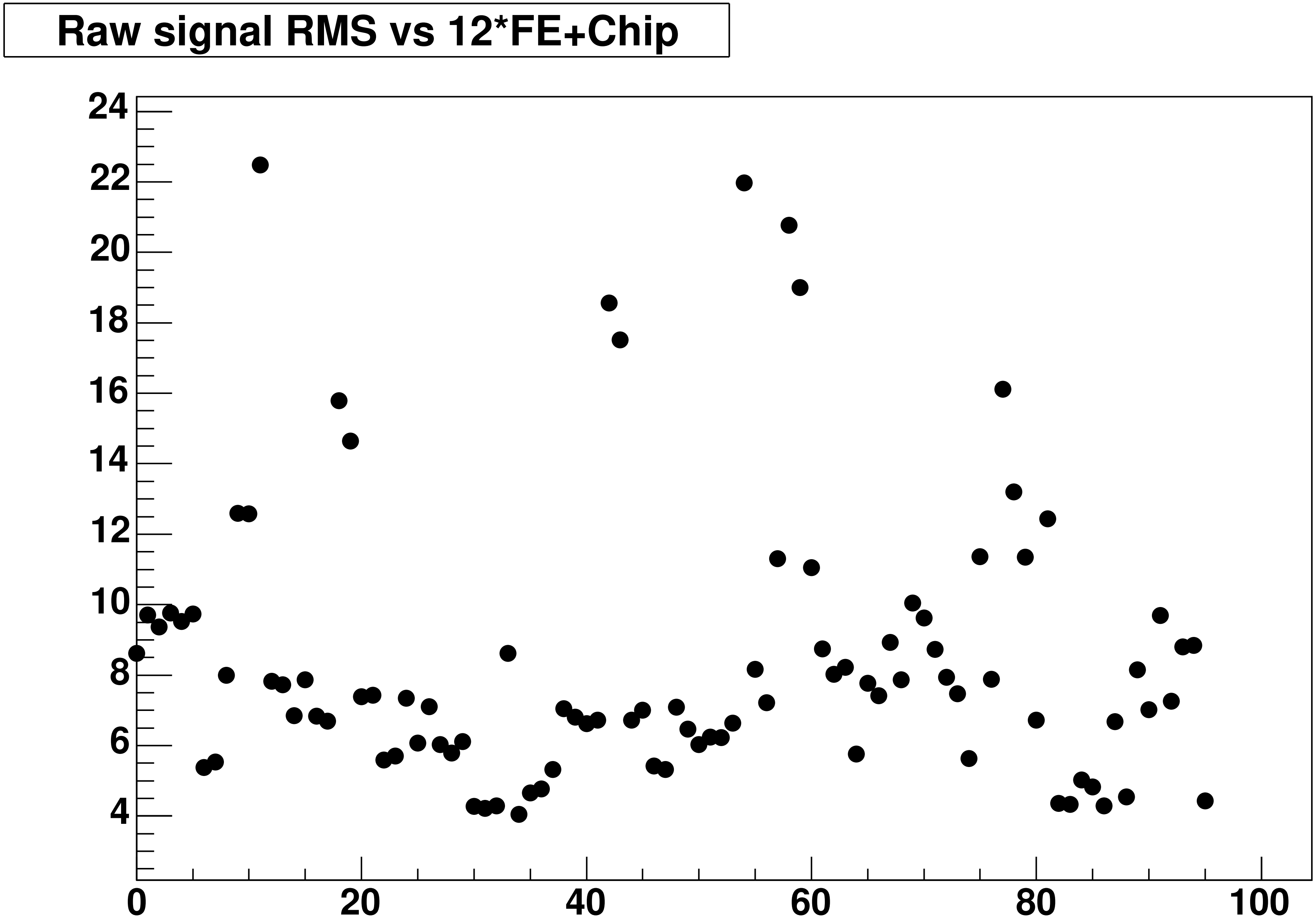


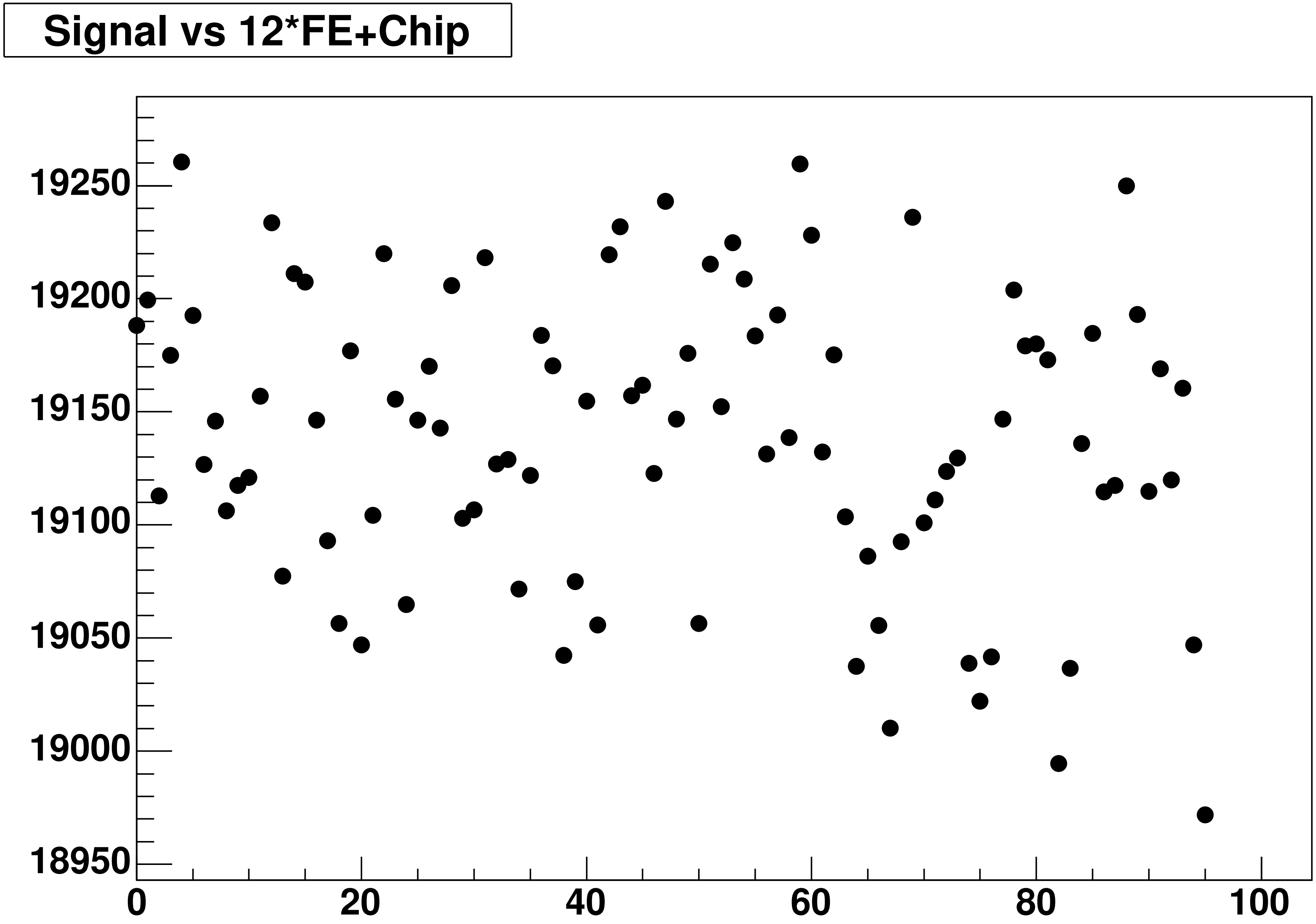
FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 1052280
Mean 1.897e+04
RMS 4.433
Underflow 9.664e+05
Overflow 0
10^4
10^3
10^2
10
1
18800
18900
19000
19100
19200
19300
19400


Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100

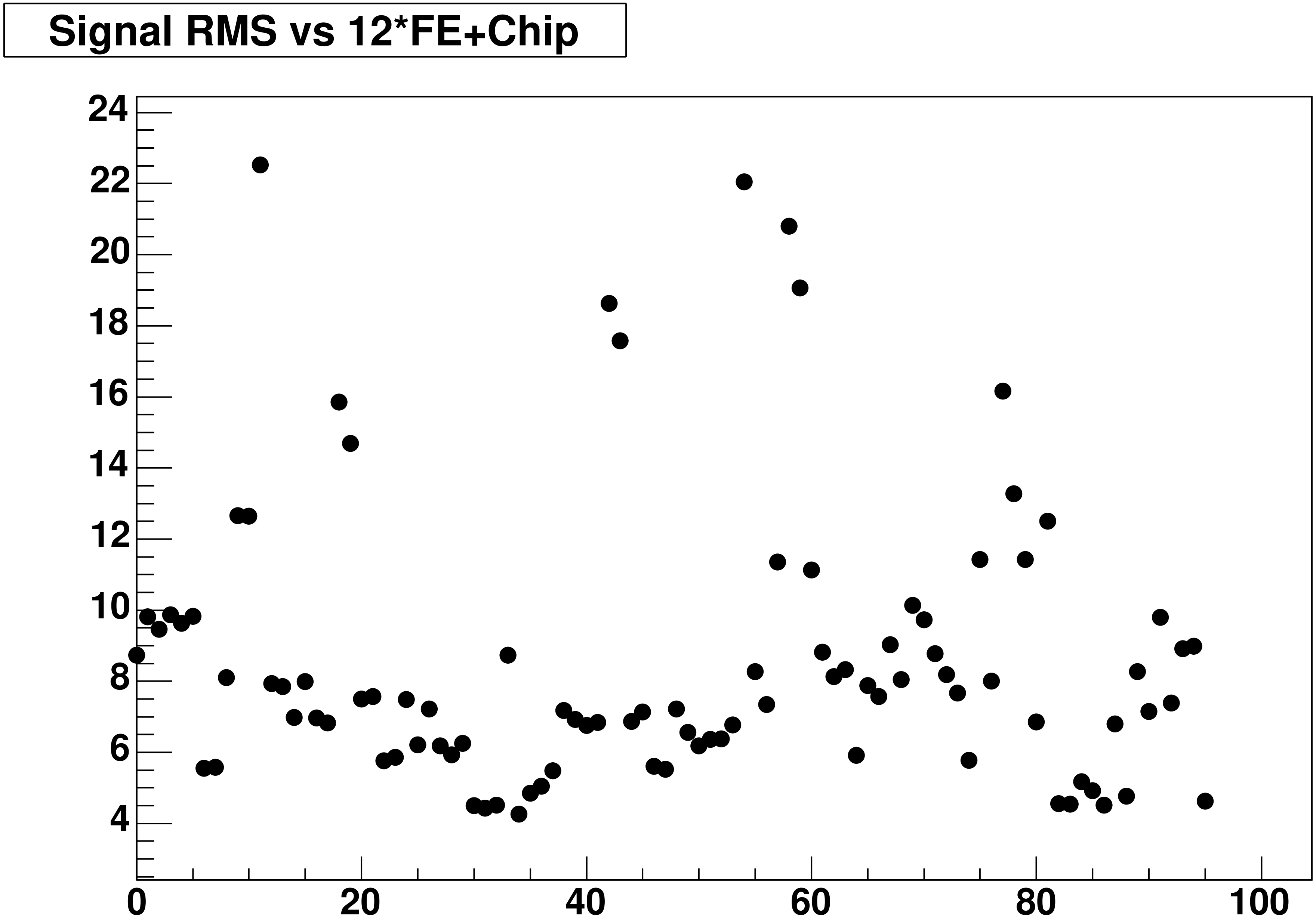

Pedestal RMS vs 12*FE+Chip
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
19300
19250
19200
19150
19100
19050
19000
18950
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
24
22
20
18
16
14
12
10
8
6
4
0
20
40
60
80
100



Signal vs 12*FE+Chip
19250
19200
19150
19100
19050
19000
18950
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
24
22
20
18
16
14
12
10
8
6
4
0
20
40
60
80
100