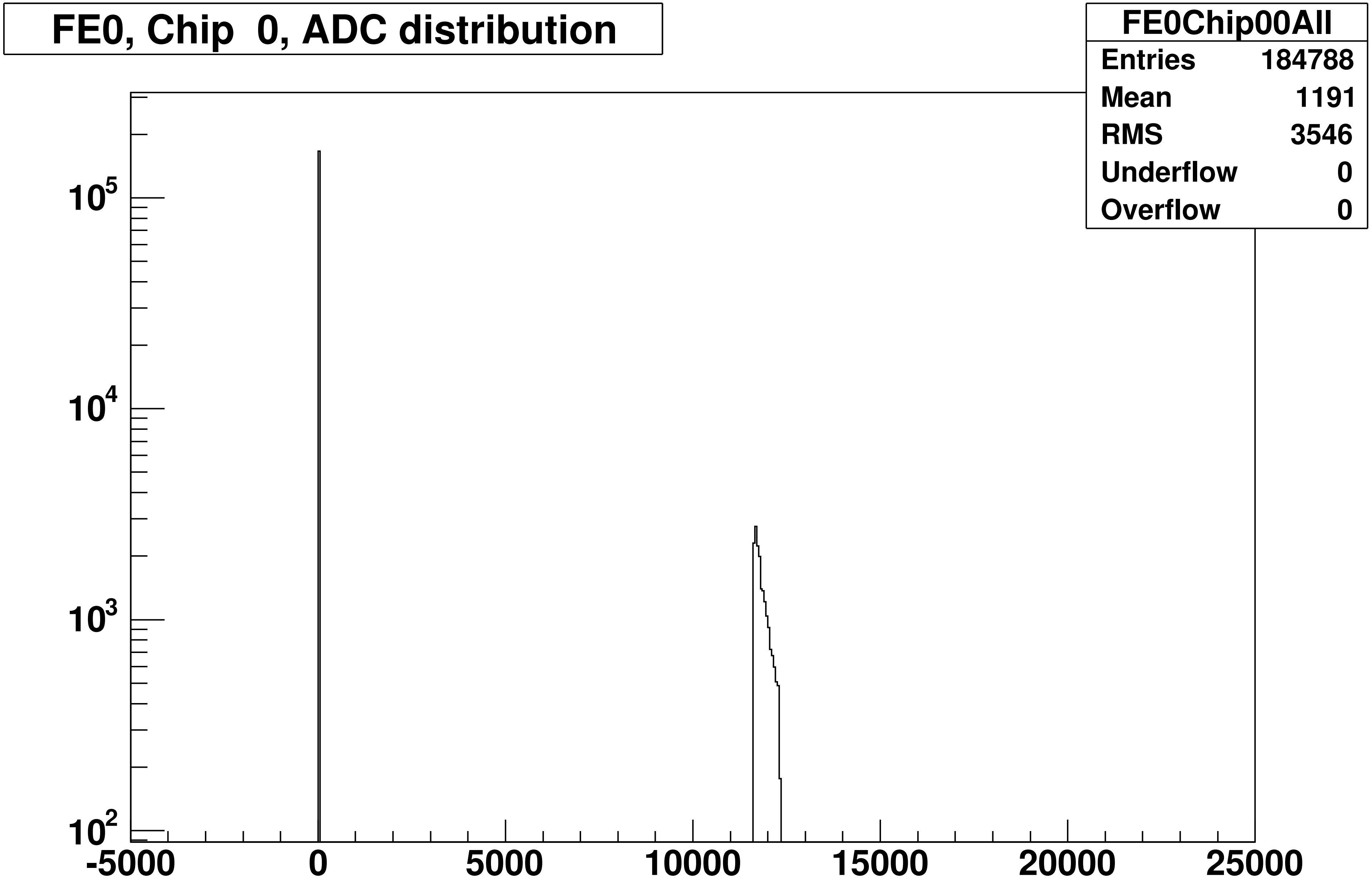
FE0, Chip 0, ADC distribution
FE0Chip00All
Entries 184788
Mean 1191
RMS 3546
Underflow 0
Overflow 0
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10^4
10^3
10^2
-5000
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20000
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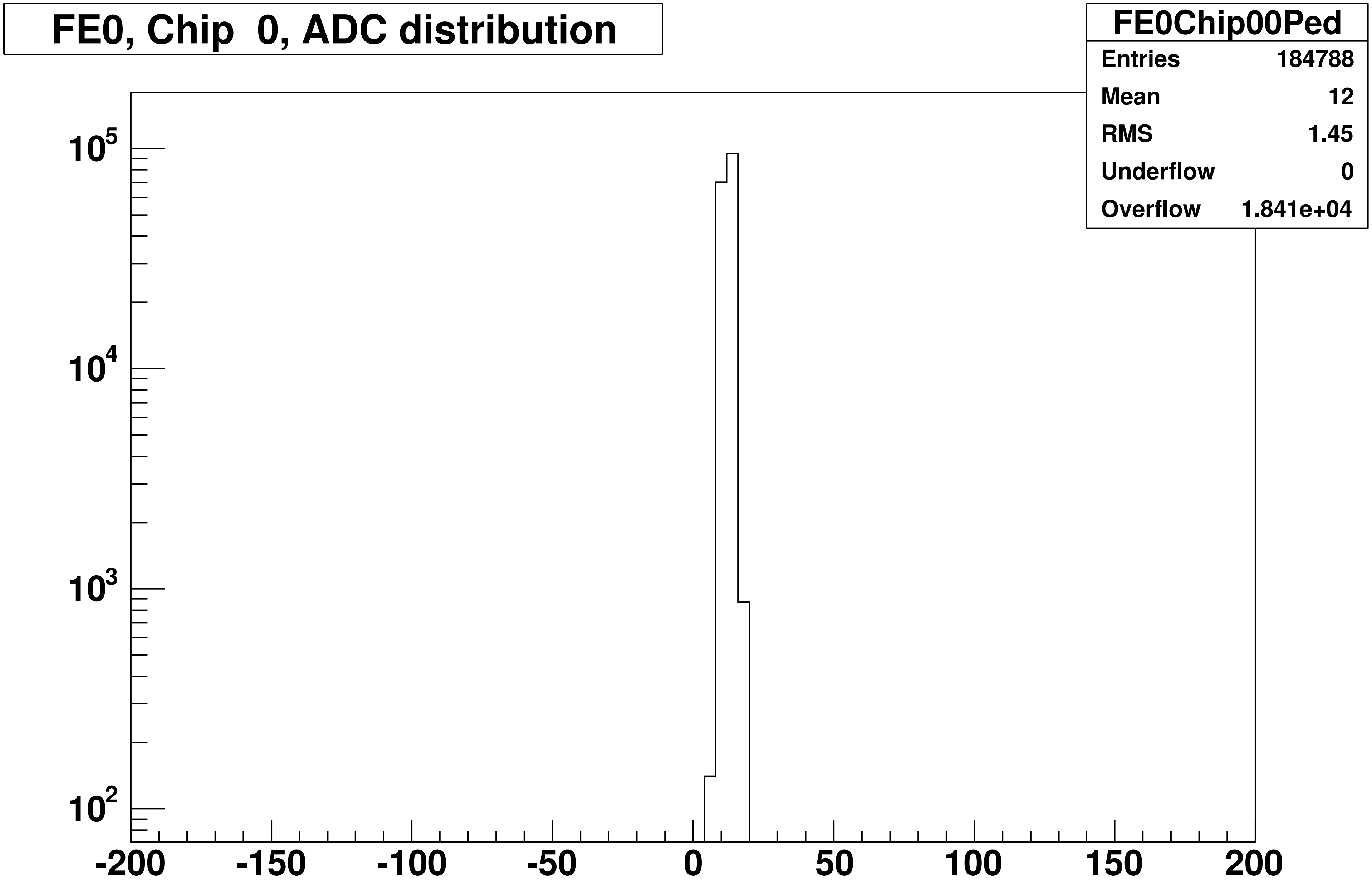
FE0, Chip 0, ADC distribution
FE0Chip00Ped
Entries 184788
Mean 12
RMS 1.45
Underflow 0
Overflow 1.841e+04
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10^4
10^3
10^2
-200
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-100
-50
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150
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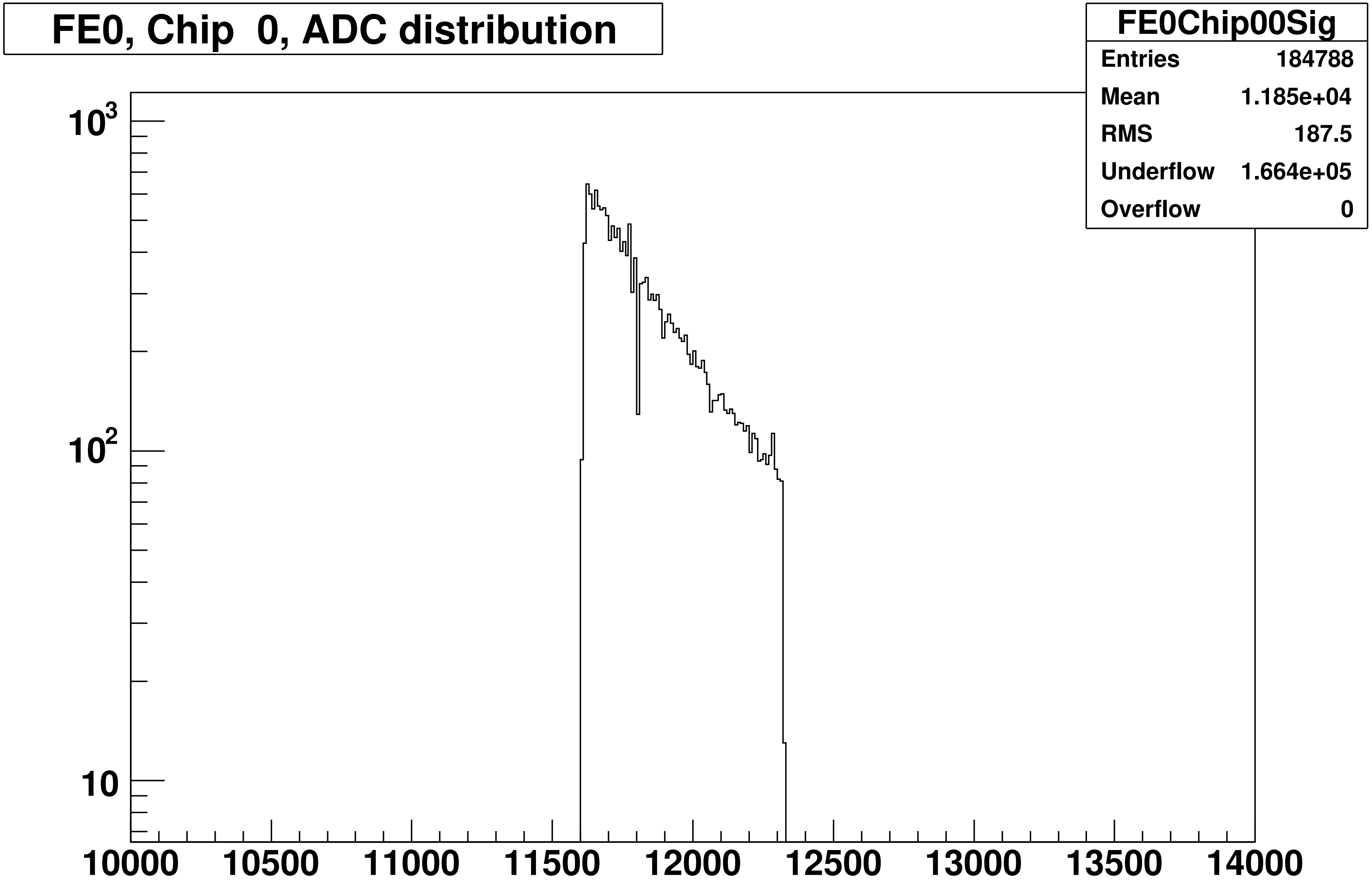
FE0, Chip 0, ADC distribution
FE0Chip00Sig
Entries 184788
Mean 1.185e+04
RMS 187.5
Underflow 1.664e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
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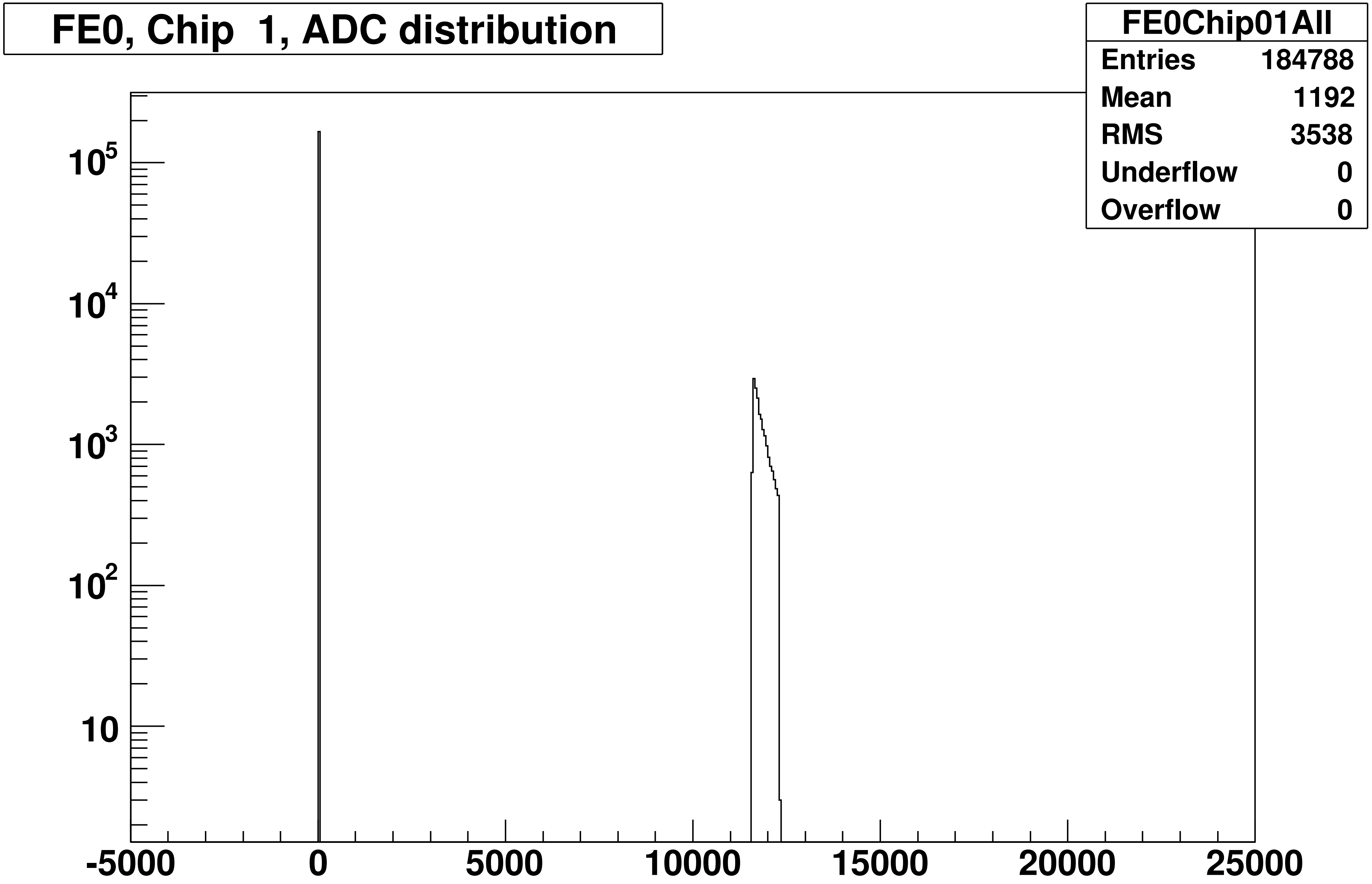

FE0, Chip 1, ADC distribution
FE0Chip01All
Entries 184788
Mean 1192
RMS 3538
Underflow 0
Overflow 0
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10^2
10^3
10^4
10^5
-5000
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10000
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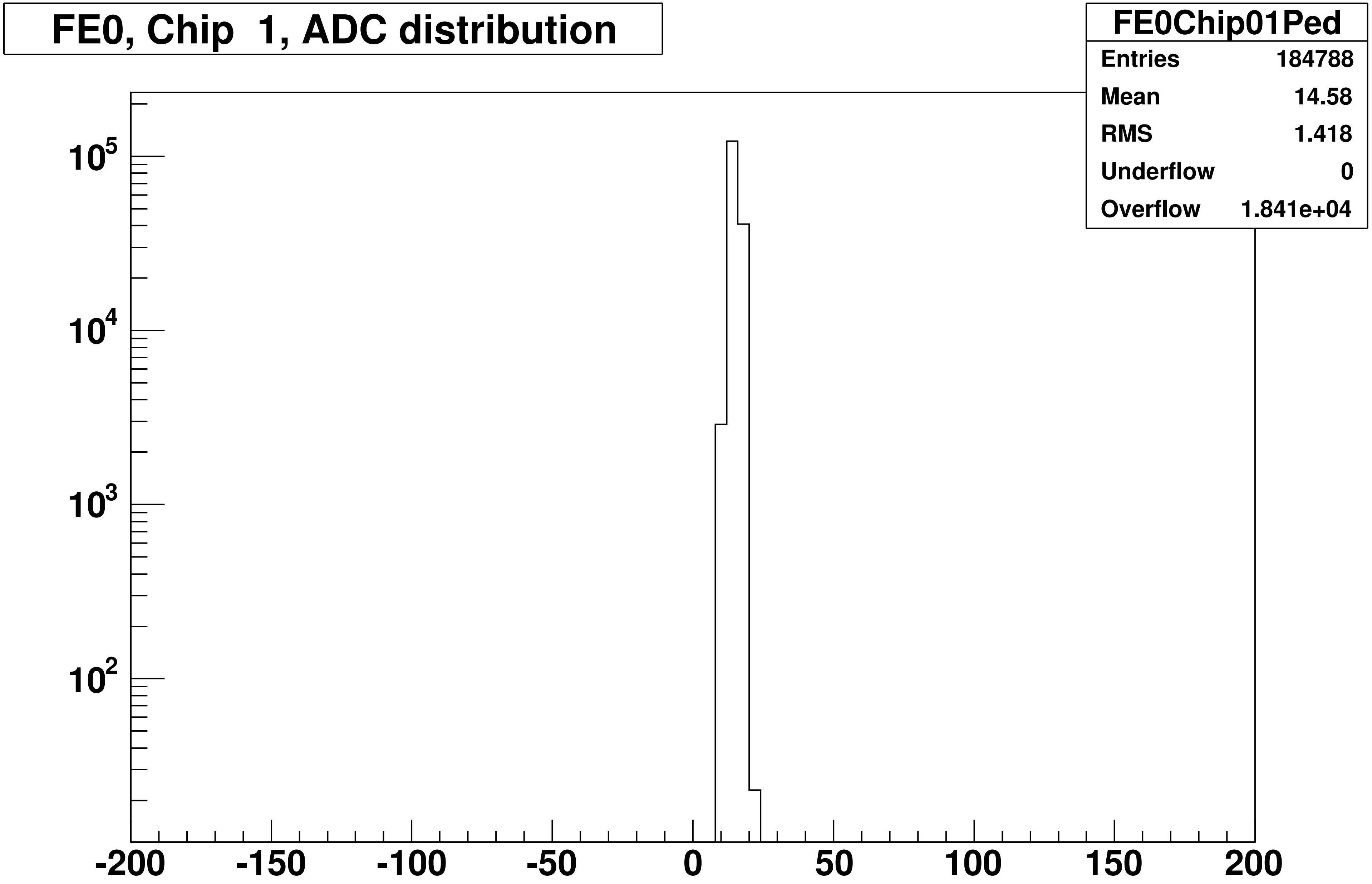
FE0, Chip 1, ADC distribution
FE0Chip01Ped
Entries 184788
Mean 14.58
RMS 1.418
Underflow 0
Overflow 1.841e+04
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10^4
10^3
10^2
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150
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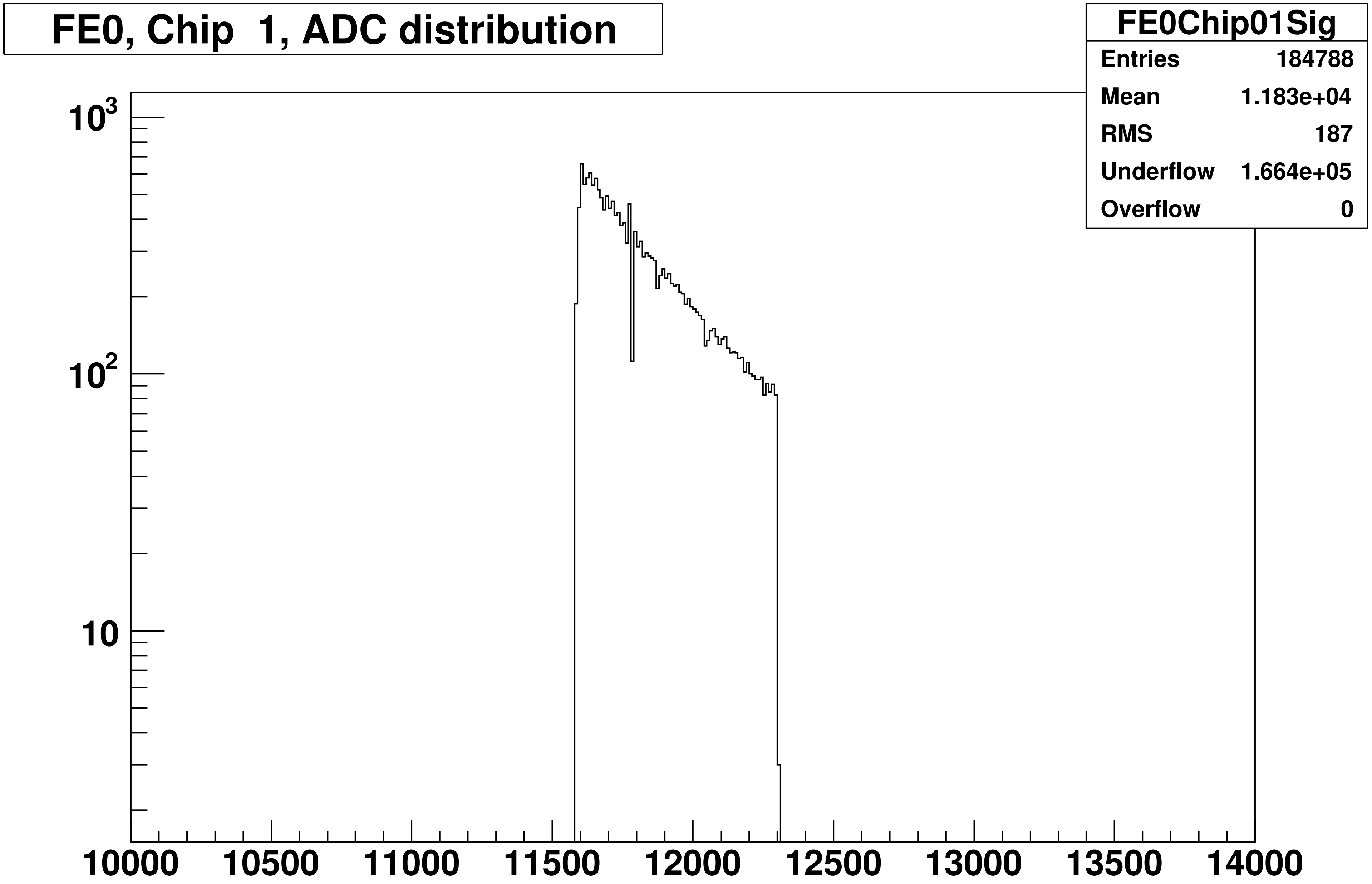
FE0, Chip 1, ADC distribution
FE0Chip01Sig
Entries 184788
Mean 1.183e+04
RMS 187
Underflow 1.664e+05
Overflow 0
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10000
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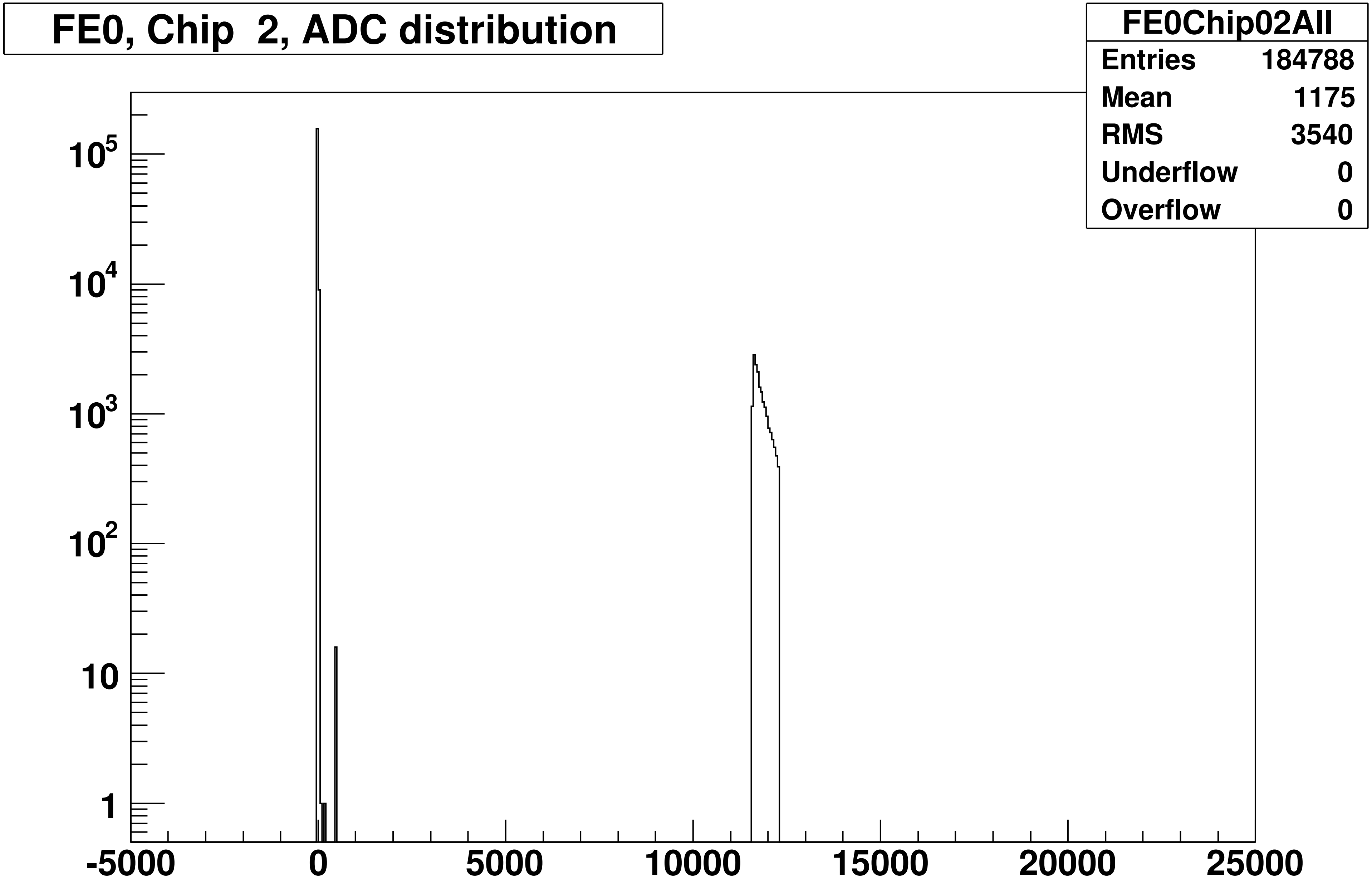
FE0, Chip 2, ADC distribution
FE0Chip02All
Entries 184788
Mean 1175
RMS 3540
Underflow 0
Overflow 0
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10^4
10^3
10^2
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10000
15000
20000
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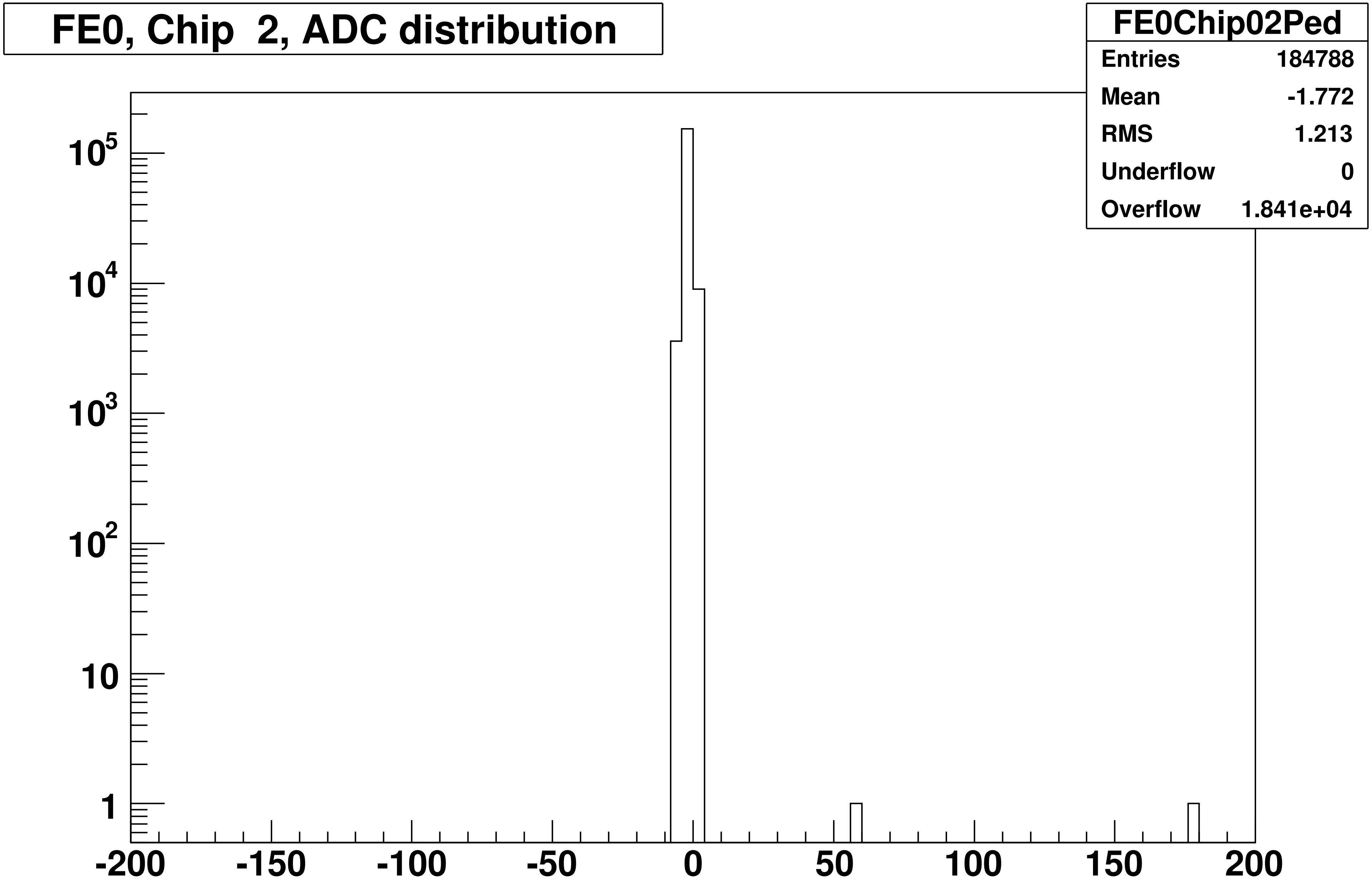
FE0, Chip 2, ADC distribution
FE0Chip02Ped
Entries 184788
Mean -1.772
RMS 1.213
Underflow 0
Overflow 1.841e+04
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10^4
10^3
10^2
10
1
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150
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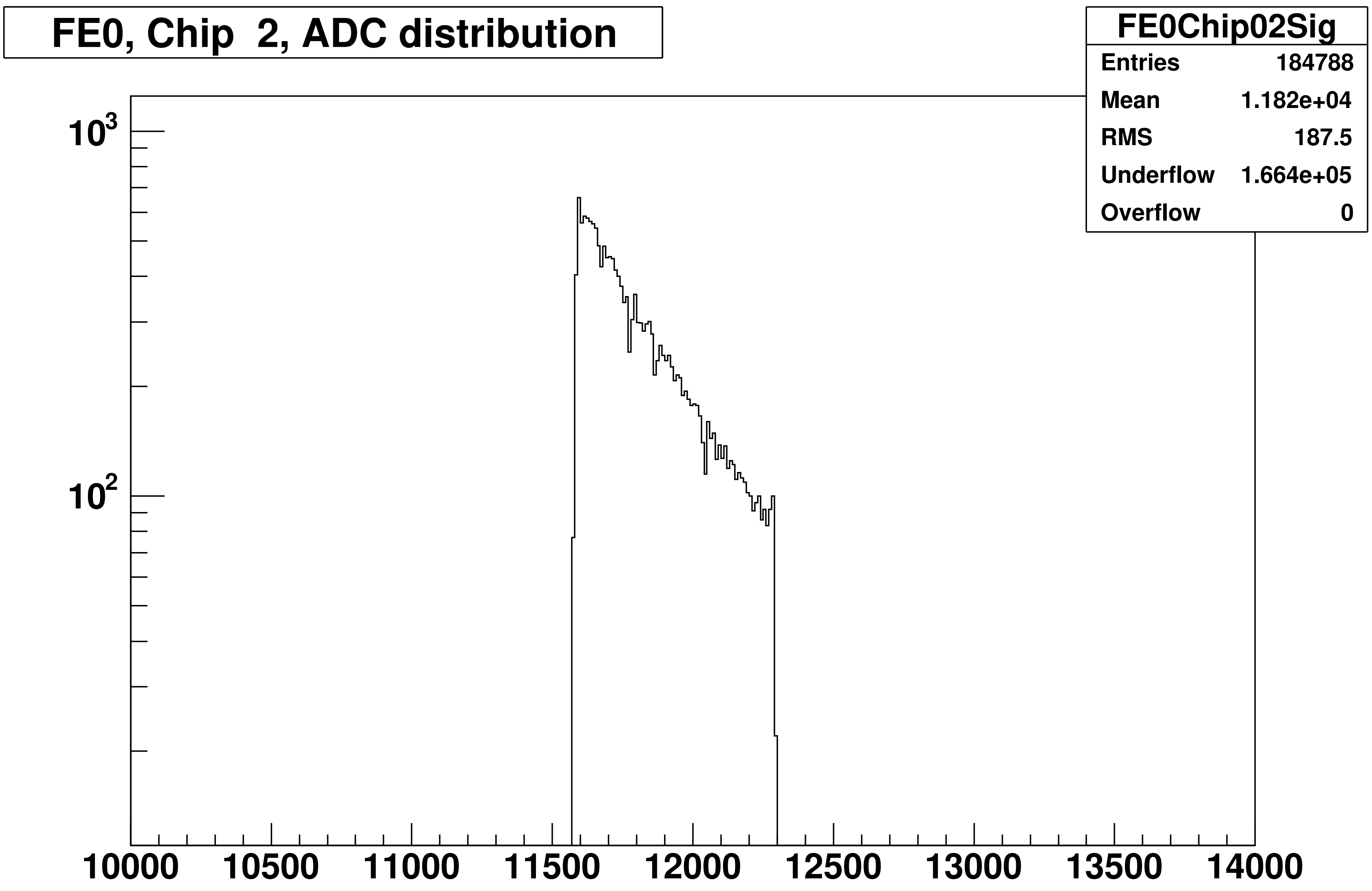
FE0, Chip 2, ADC distribution
FE0Chip02Sig
Entries 184788
Mean 1.182e+04
RMS 187.5
Underflow 1.664e+05
Overflow 0
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10^2
10000
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11500
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13500
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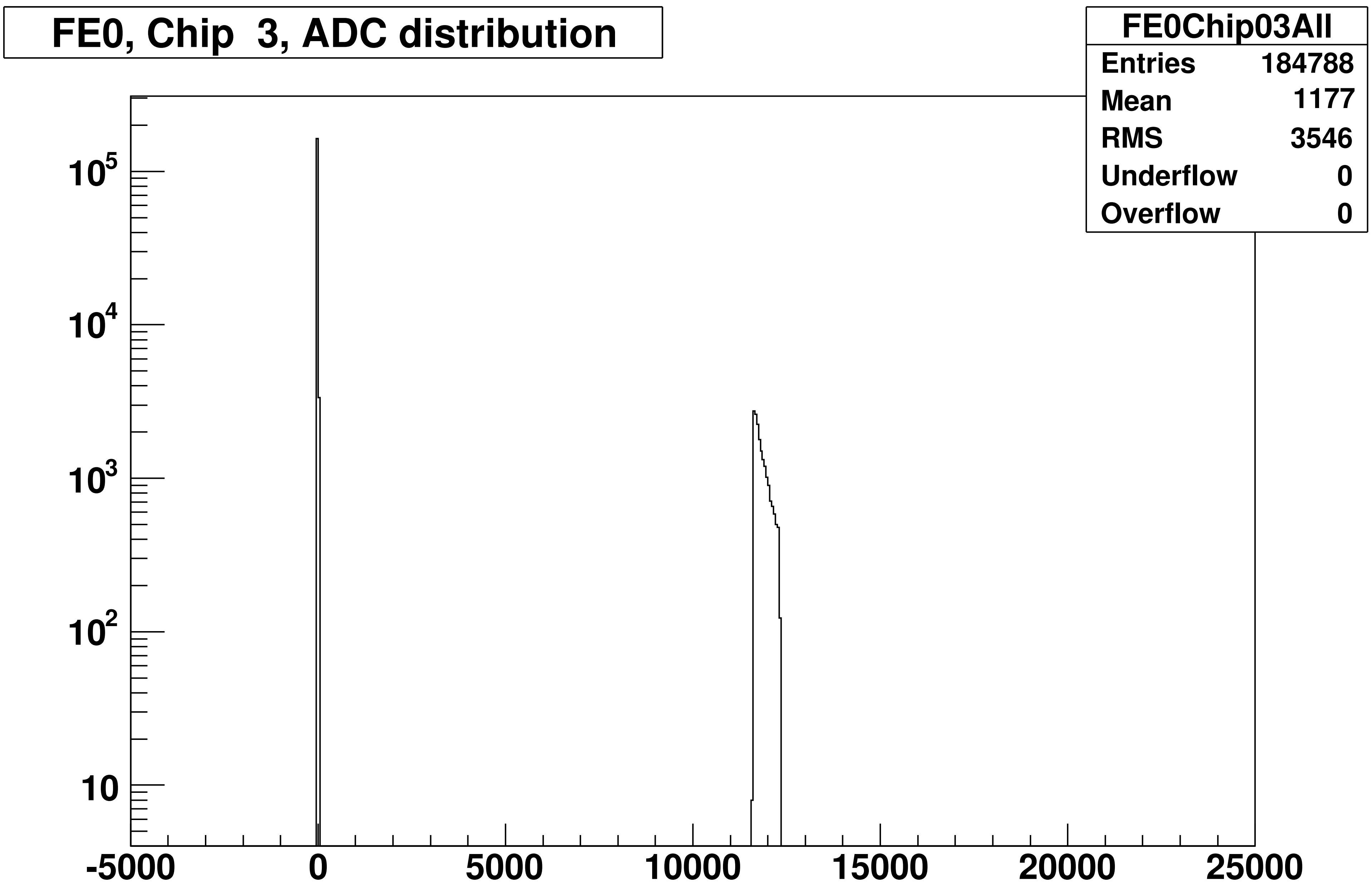

FE0, Chip 3, ADC distribution
FE0Chip03All
Entries 184788
Mean 1177
RMS 3546
Underflow 0
Overflow 0
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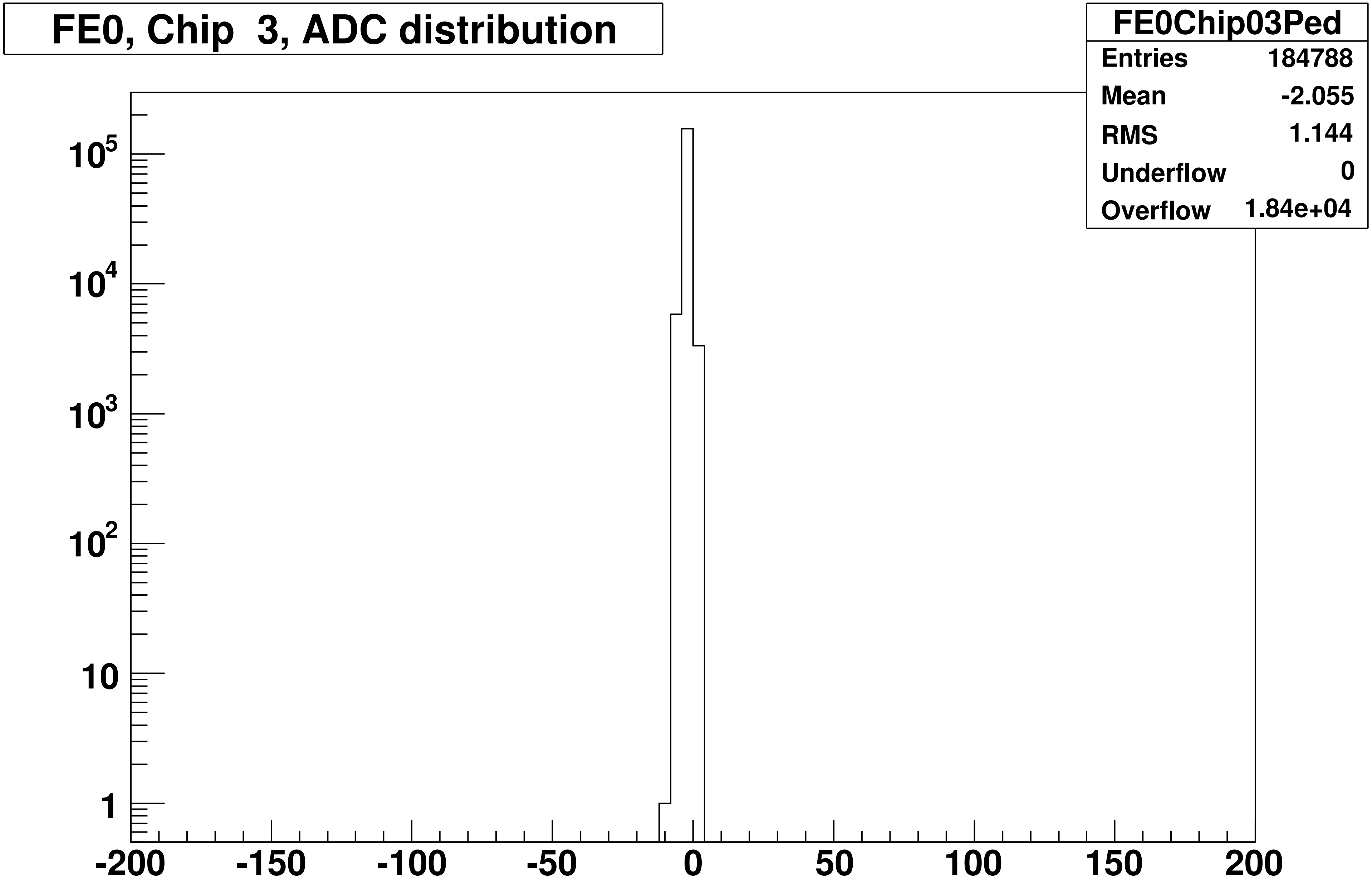
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE0, Chip 3, ADC distribution
FE0Chip03Ped
Entries 184788
Mean -2.055
RMS 1.144
Underflow 0
Overflow 1.84e+04
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10^4
10^3
10^2
10
1
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-150
-100
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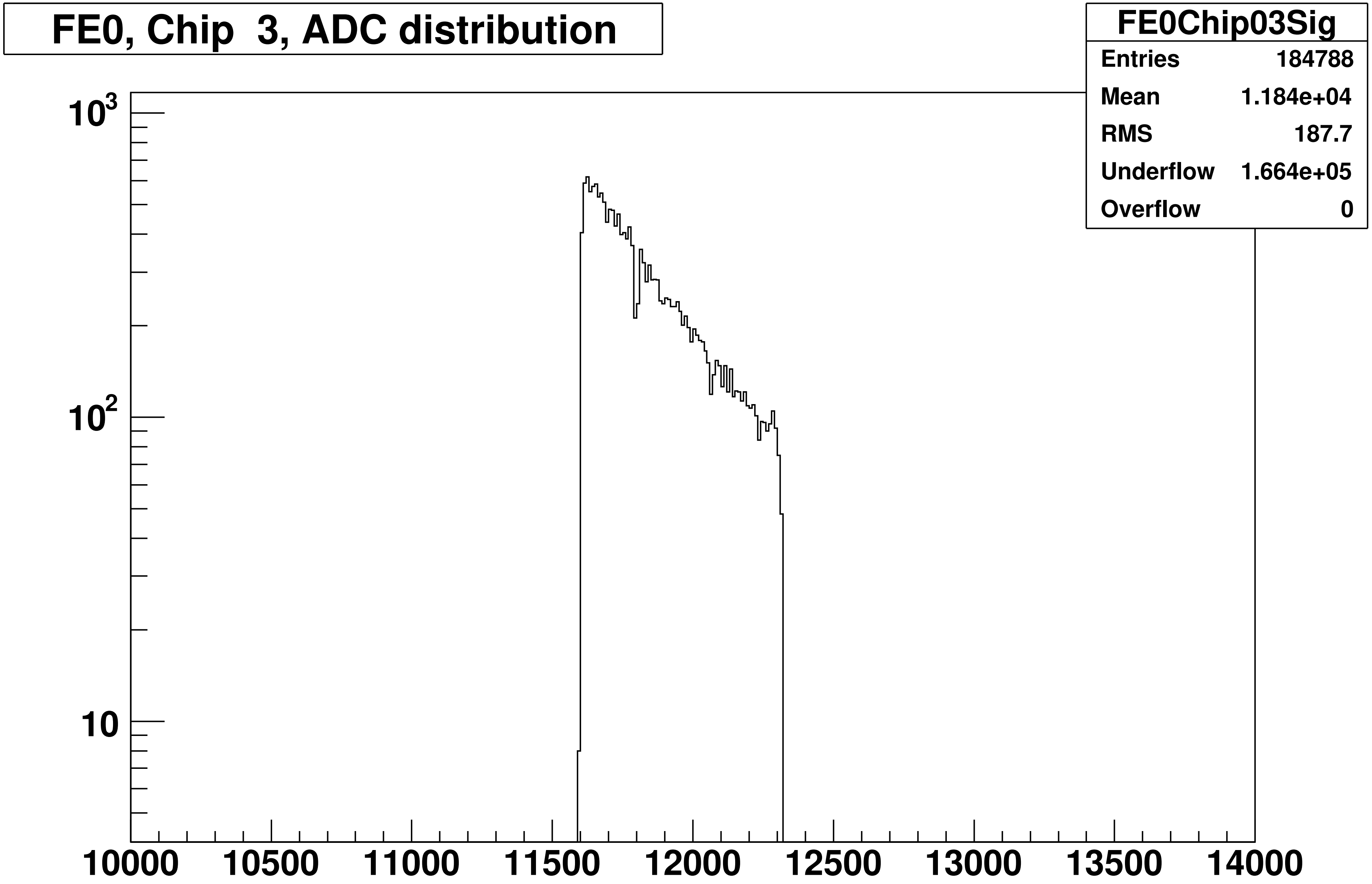
0
50
100
150
200


FE0, Chip 3, ADC distribution
FE0Chip03Sig
Entries 184788
Mean 1.184e+04
RMS 187.7
Underflow 1.664e+05
Overflow 0
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10^2
10
10000
10500
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11500
12000
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13000
13500
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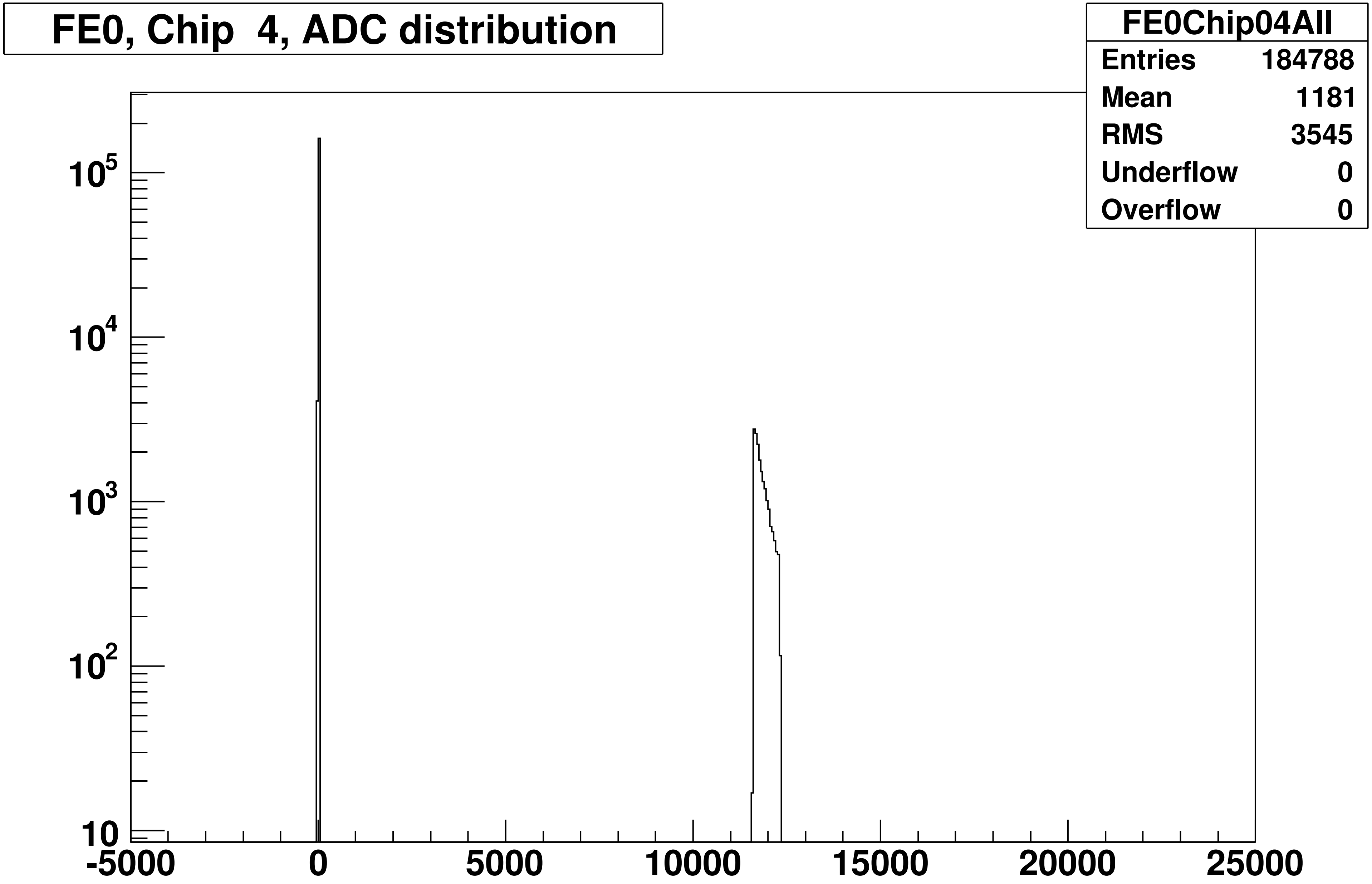
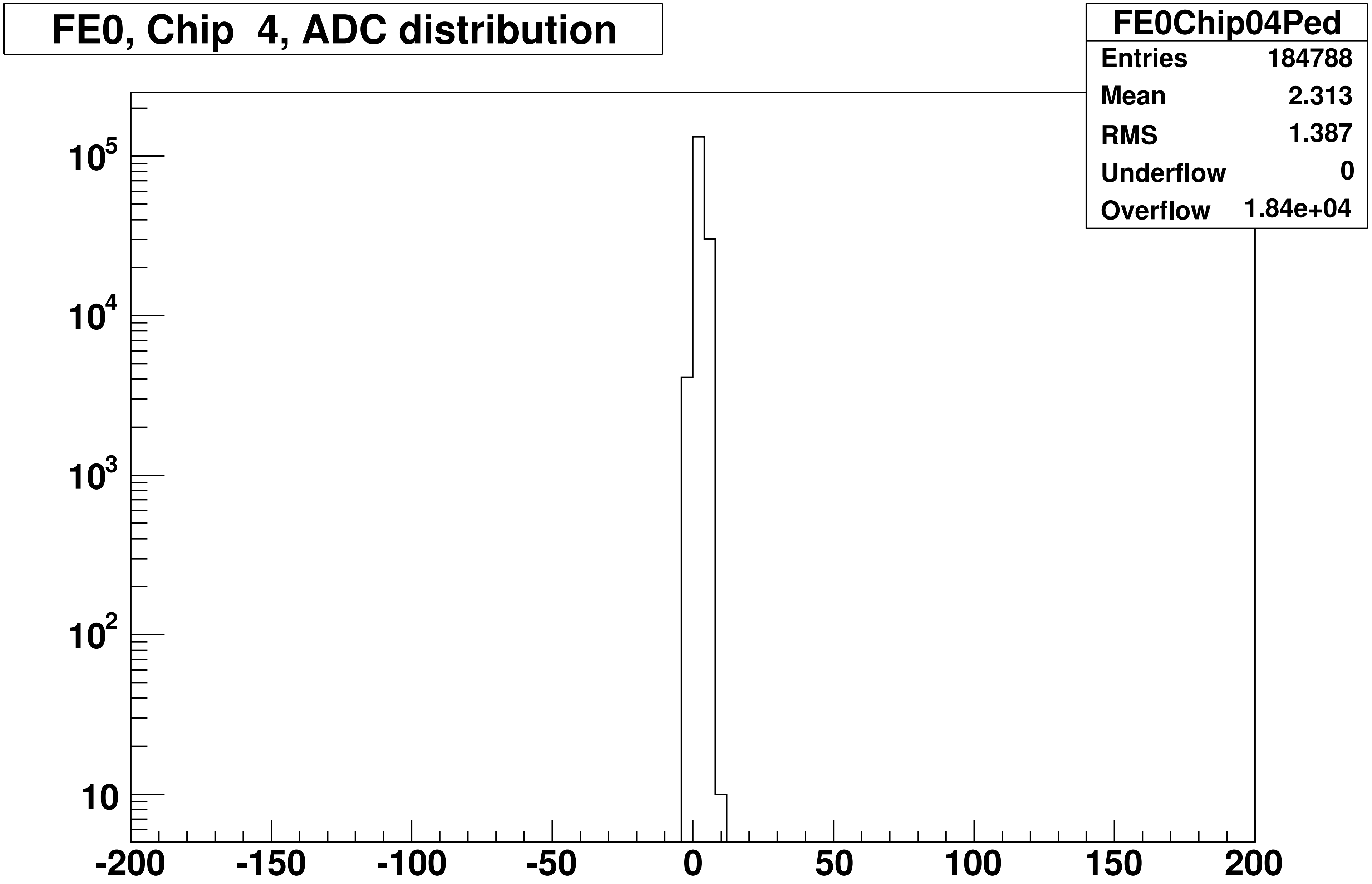


FE0, Chip 4, ADC distribution
FE0Chip04All
Entries 184788
Mean 1181
RMS 3545
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 4, ADC distribution
FE0Chip04Ped
Entries 184788
Mean 2.313
RMS 1.387
Underflow 0
Overflow 1.84e+04
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10^4
10^3
10^2
10
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-100
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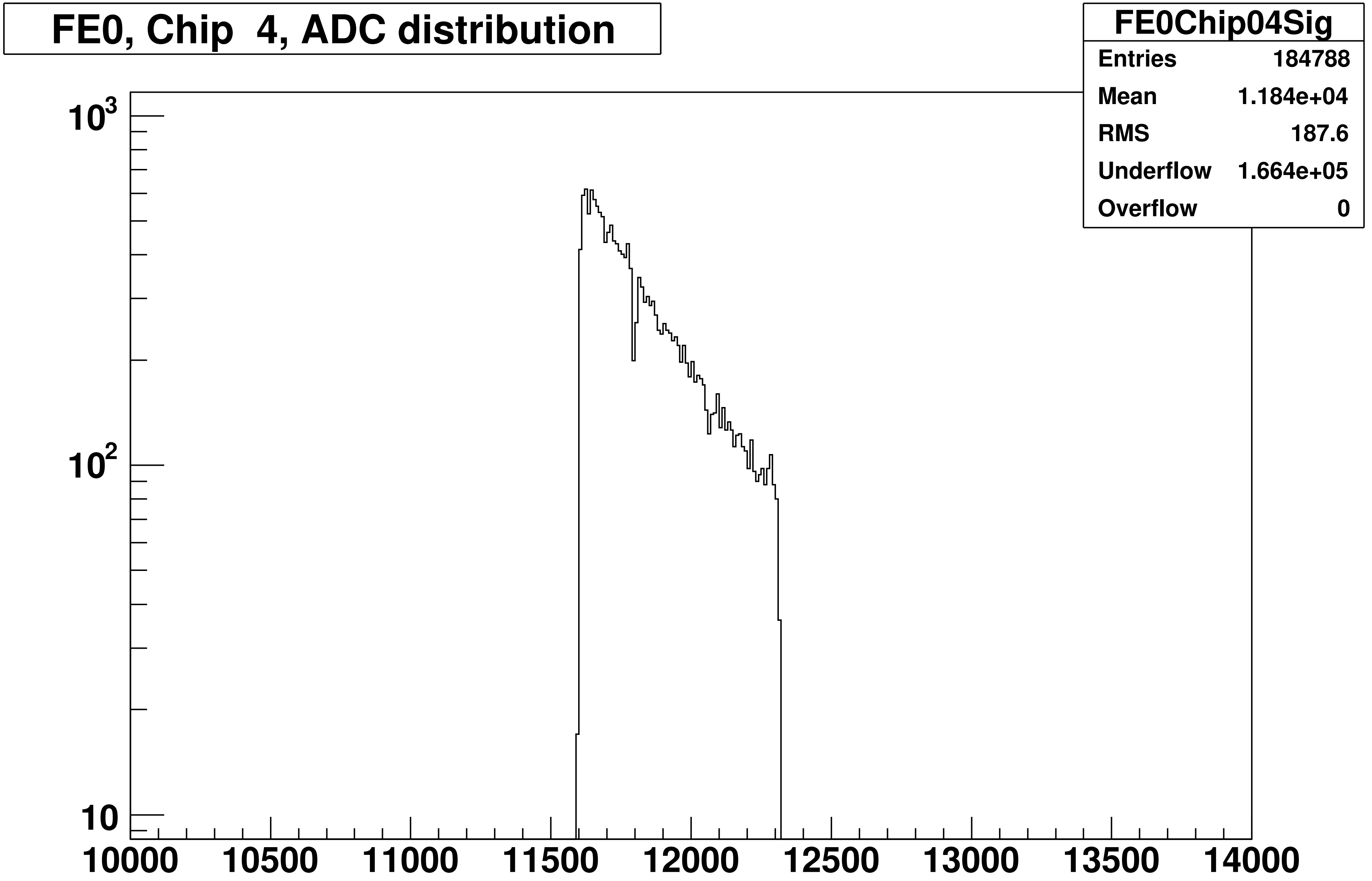
0
50
100
150
200


FE0, Chip 4, ADC distribution
FE0Chip04Sig
Entries 184788
Mean 1.184e+04
RMS 187.6
Underflow 1.664e+05
Overflow 0
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10^2
10
10000
10500
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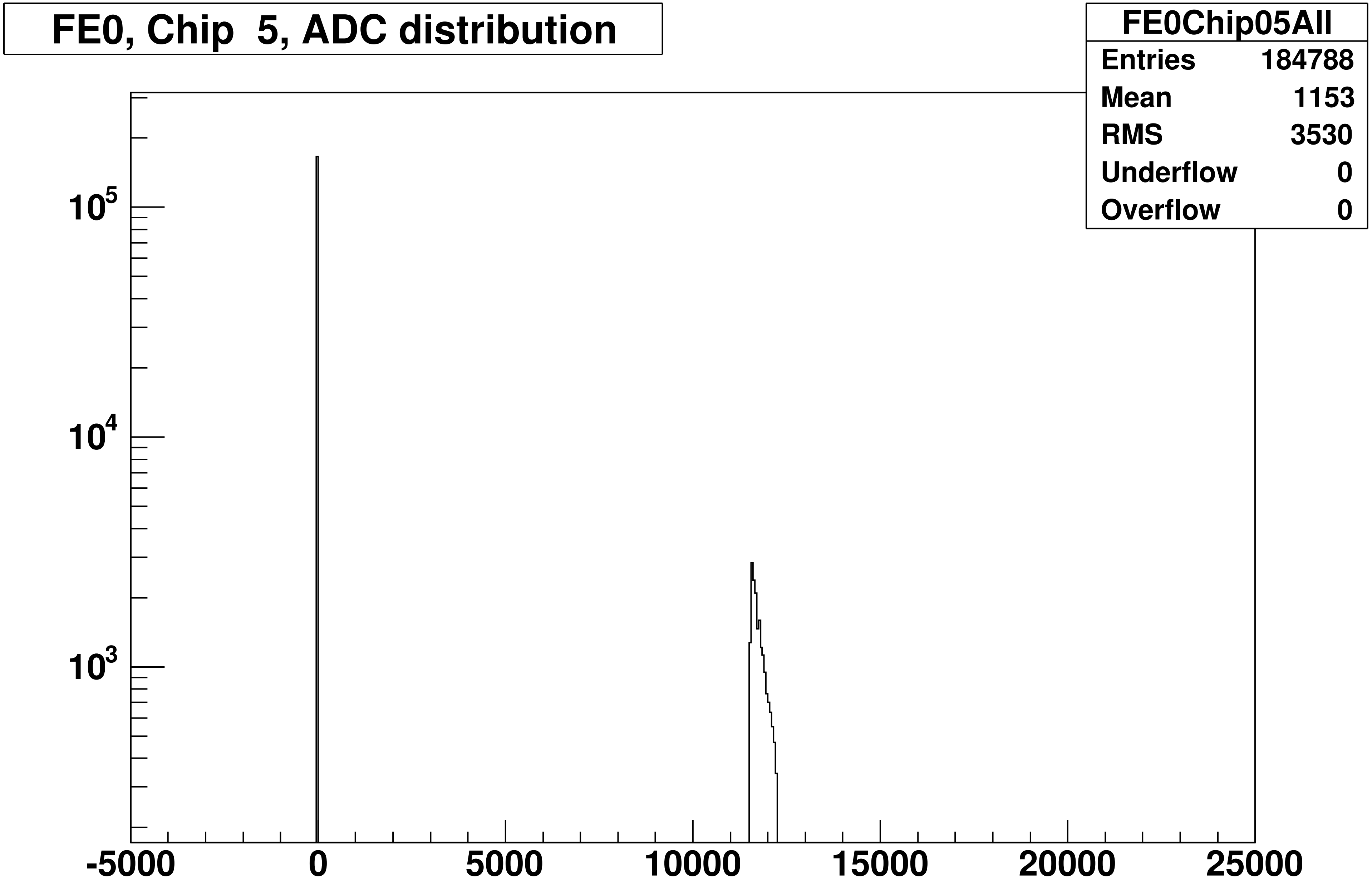
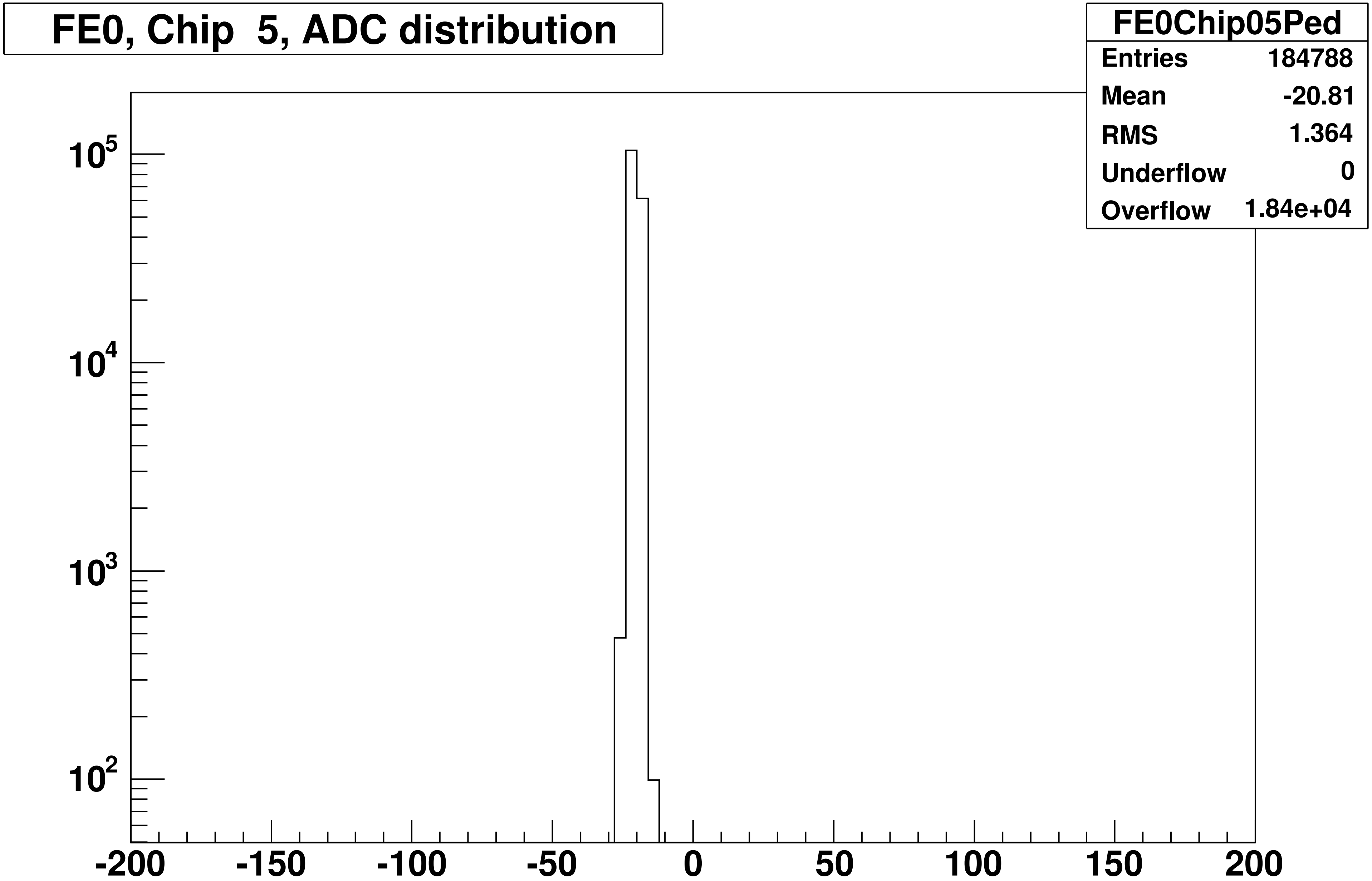
11500
12000
12500
13000
13500
14000



FE0, Chip 5, ADC distribution
FE0Chip05All
Entries 184788
Mean 1153
RMS 3530
Underflow 0
Overflow 0
10^5
10^4
10^3
-5000
0
5000
10000
15000
20000
25000


FE0, Chip 5, ADC distribution
FE0Chip05Ped
Entries 184788
Mean -20.81
RMS 1.364
Underflow 0
Overflow 1.84e+04
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10^4
10^3
10^2
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-100
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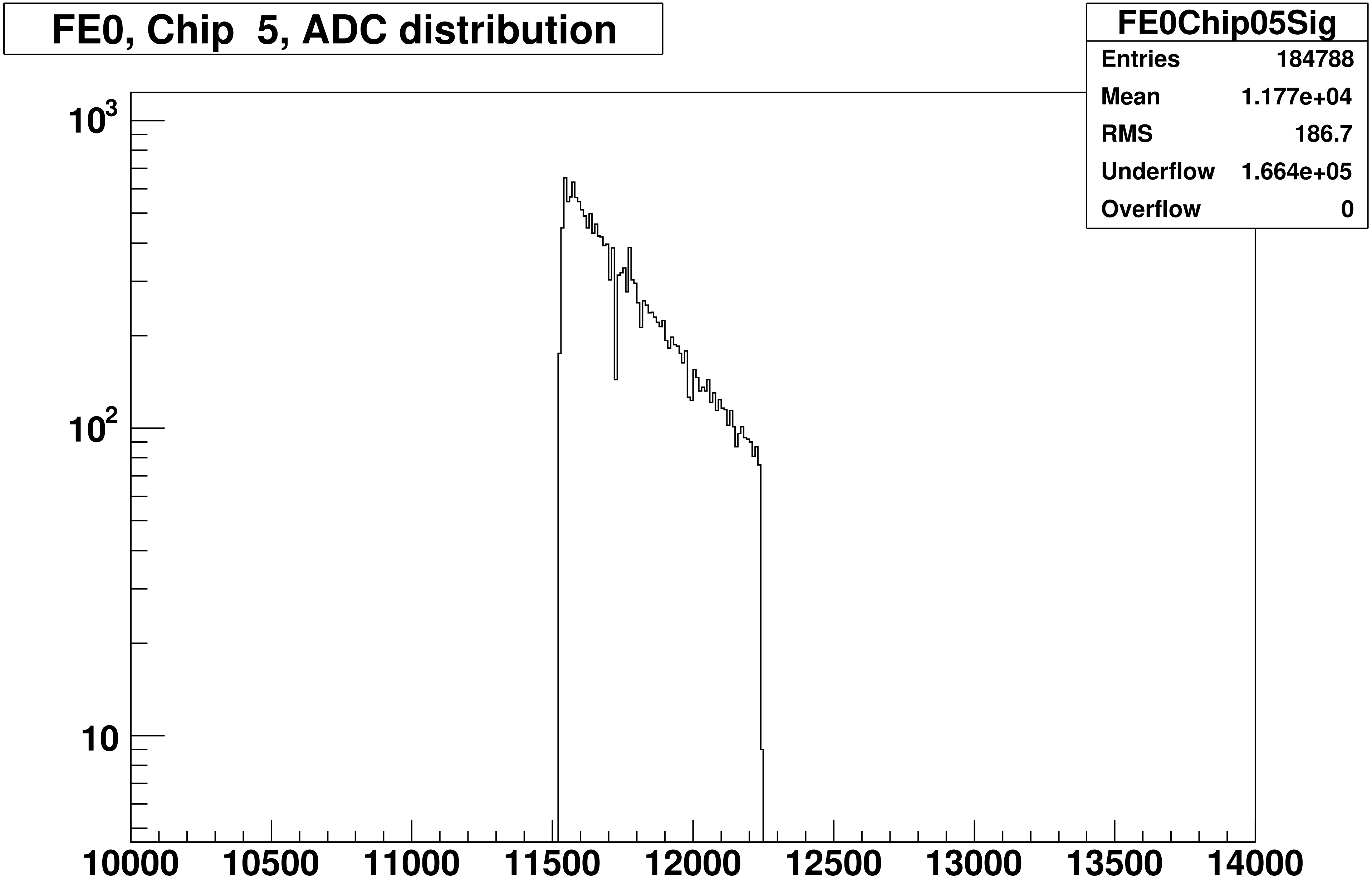
100
150
200


FE0, Chip 5, ADC distribution
FE0Chip05Sig
Entries 184788
Mean 1.177e+04
RMS 186.7
Underflow 1.664e+05
Overflow 0
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10^2
10
10000
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11000
11500
12000
12500
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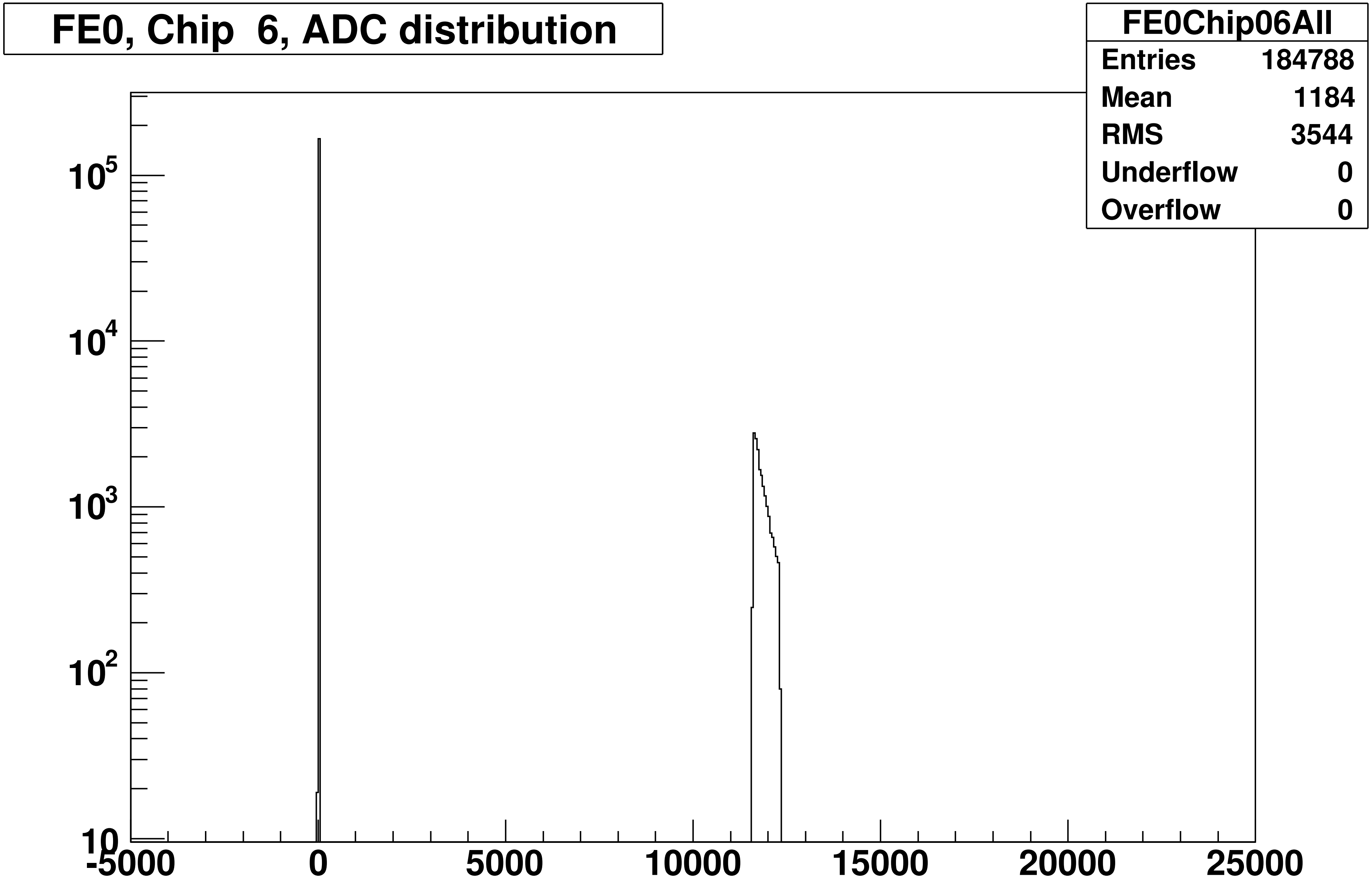
13500
14000


FE0, Chip 6, ADC distribution
FE0Chip06All
Entries 184788
Mean 1184
RMS 3544
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
-5000
0
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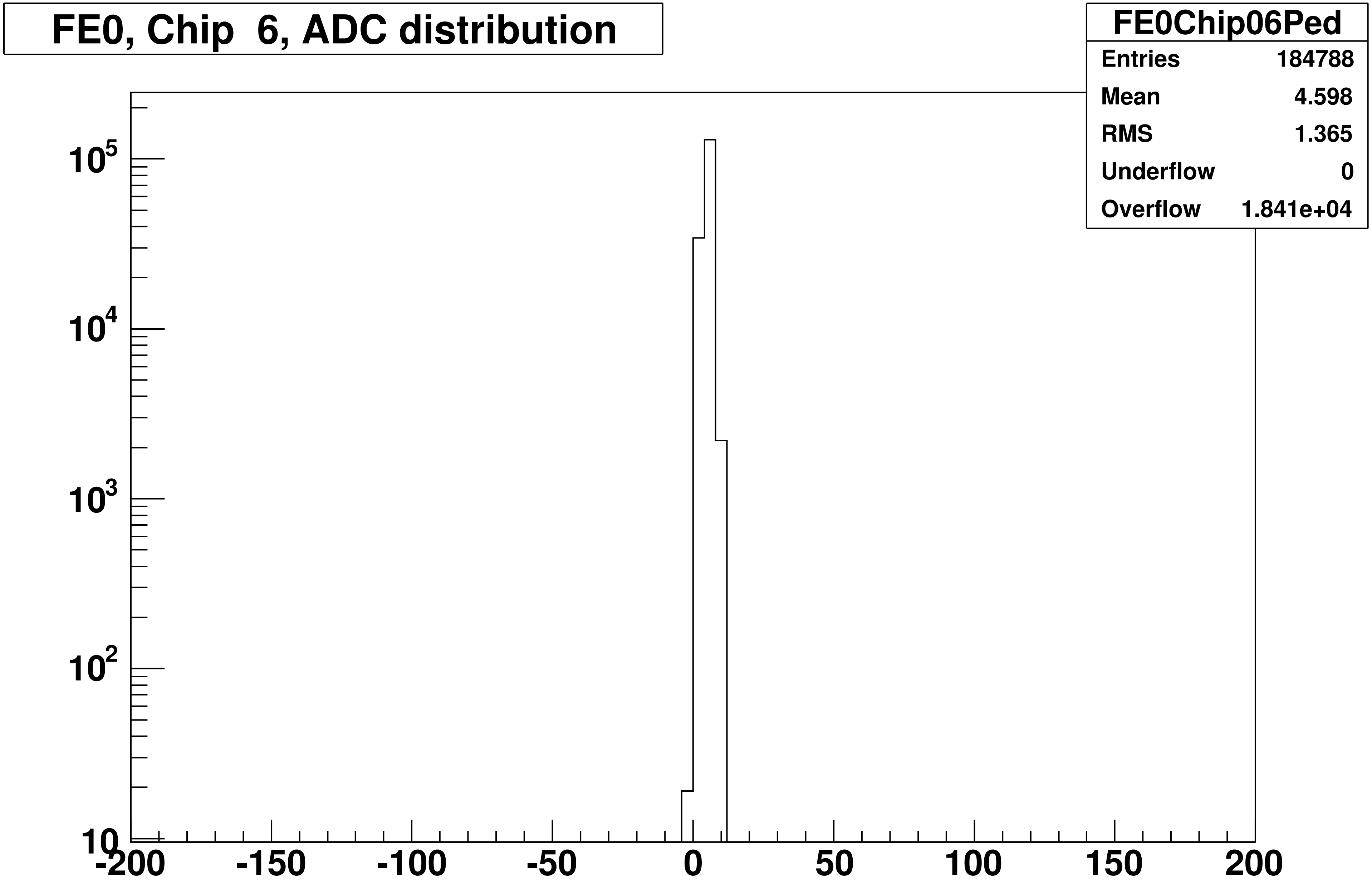
10000
15000
20000
25000


FE0, Chip 6, ADC distribution
FE0Chip06Ped
Entries 184788
Mean 4.598
RMS 1.365
Underflow 0
Overflow 1.841e+04
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10^4
10^3
10^2
10
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-150
-100
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100
150
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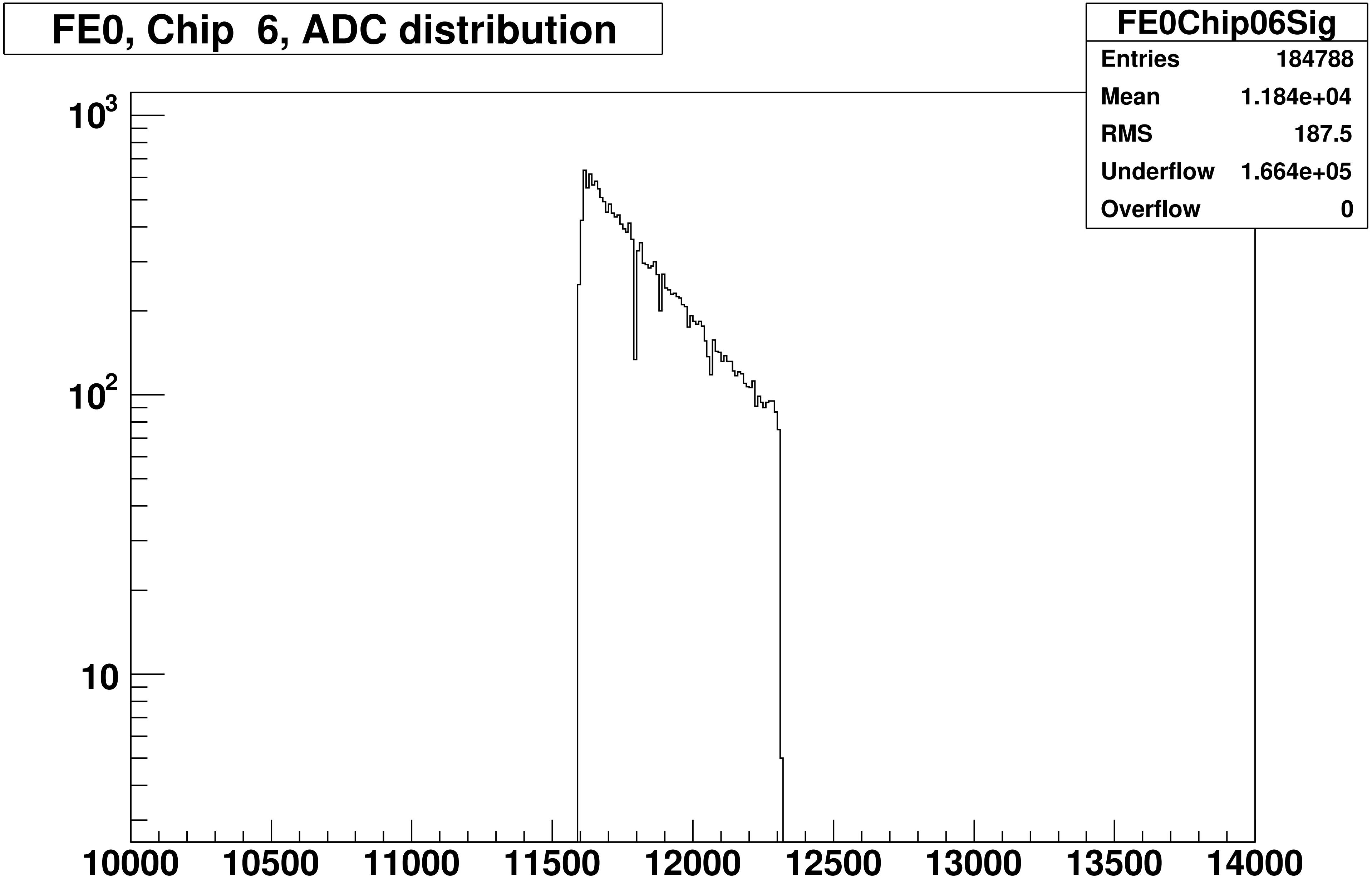
FE0, Chip 6, ADC distribution
FE0Chip06Sig
Entries 184788
Mean 1.184e+04
RMS 187.5
Underflow 1.664e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
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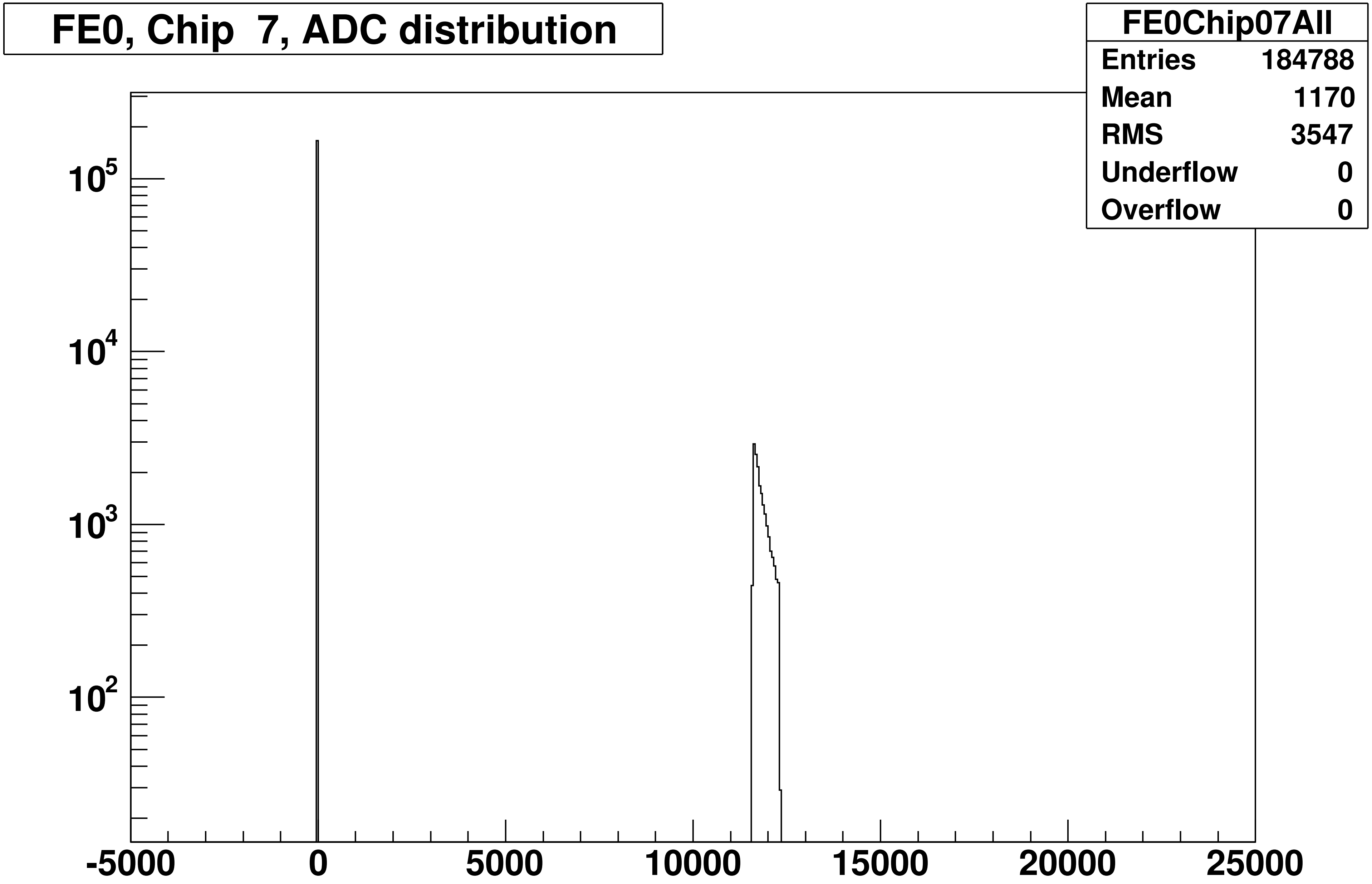
FE0, Chip 7, ADC distribution
FE0Chip07All
Entries 184788
Mean 1170
RMS 3547
Underflow 0
Overflow 0
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10^3
10^2
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0
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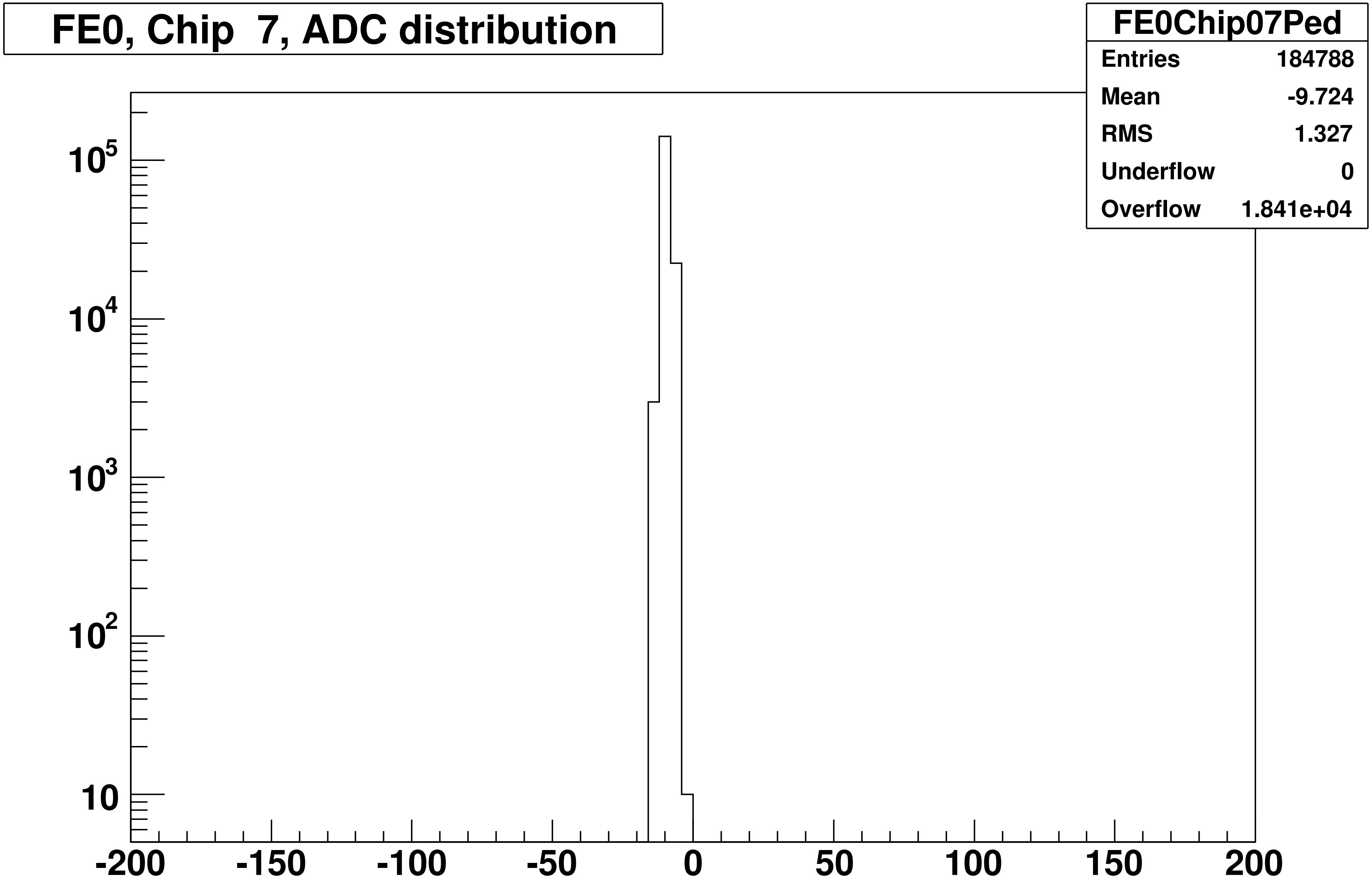
20000
25000


FE0, Chip 7, ADC distribution
FE0Chip07Ped
Entries 184788
Mean -9.724
RMS 1.327
Underflow 0
Overflow 1.841e+04
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10^4
10^3
10^2
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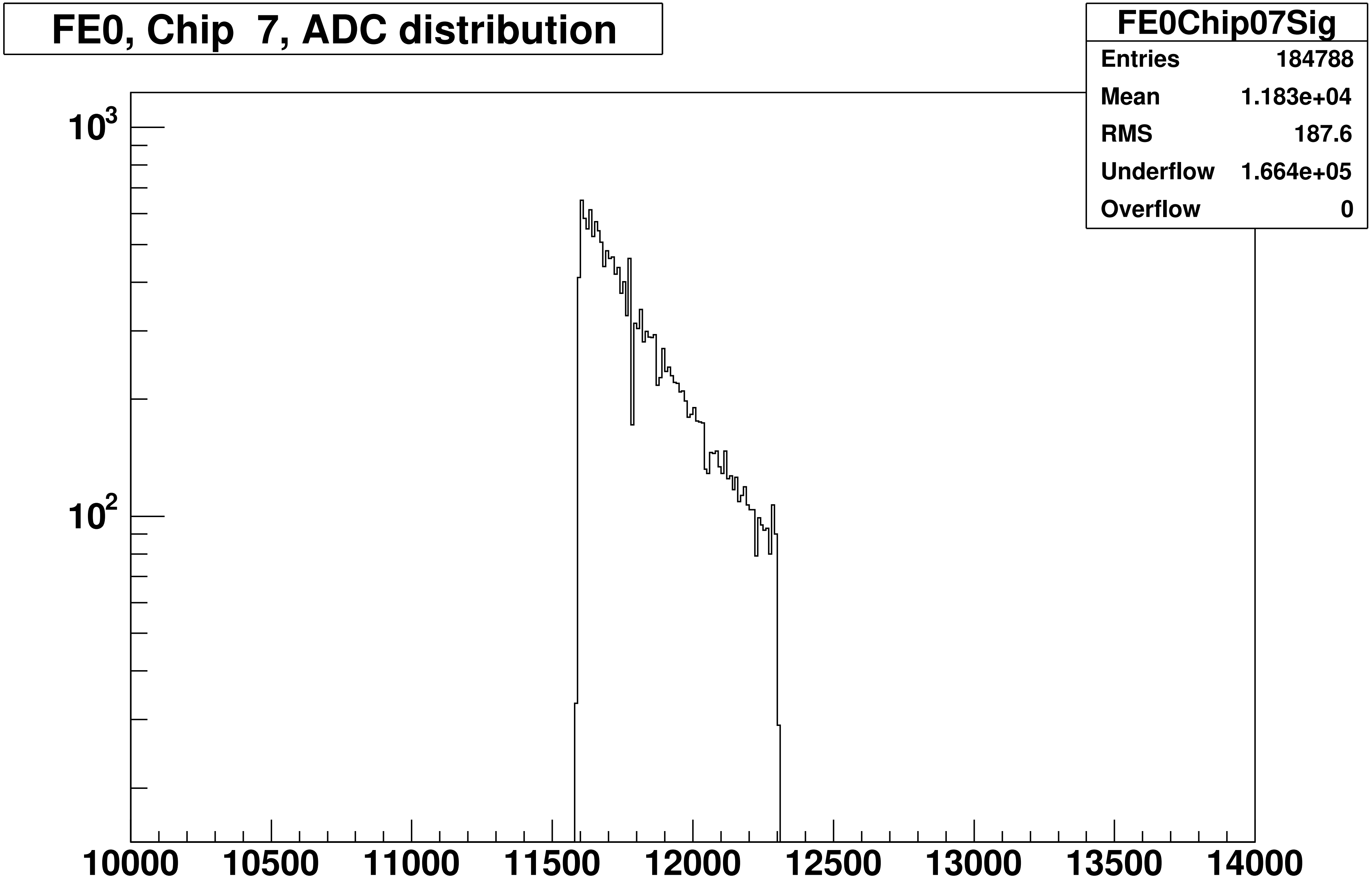
FE0, Chip 7, ADC distribution
FE0Chip07Sig
Entries 184788
Mean 1.183e+04
RMS 187.6
Underflow 1.664e+05
Overflow 0
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10^2
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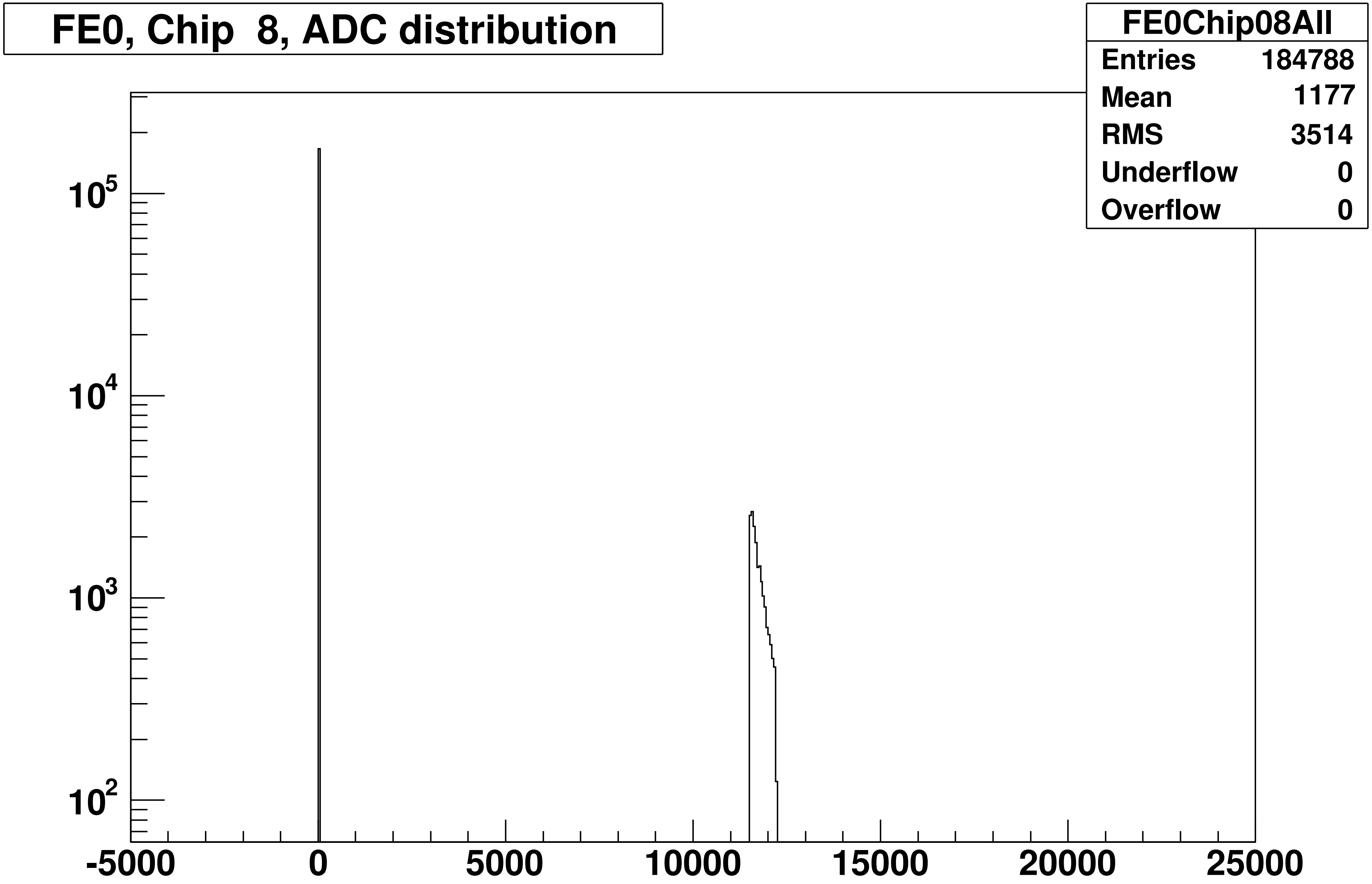
FE0, Chip 8, ADC distribution
FE0Chip08All
Entries 184788
Mean 1177
RMS 3514
Underflow 0
Overflow 0
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10^4
10^3
10^2
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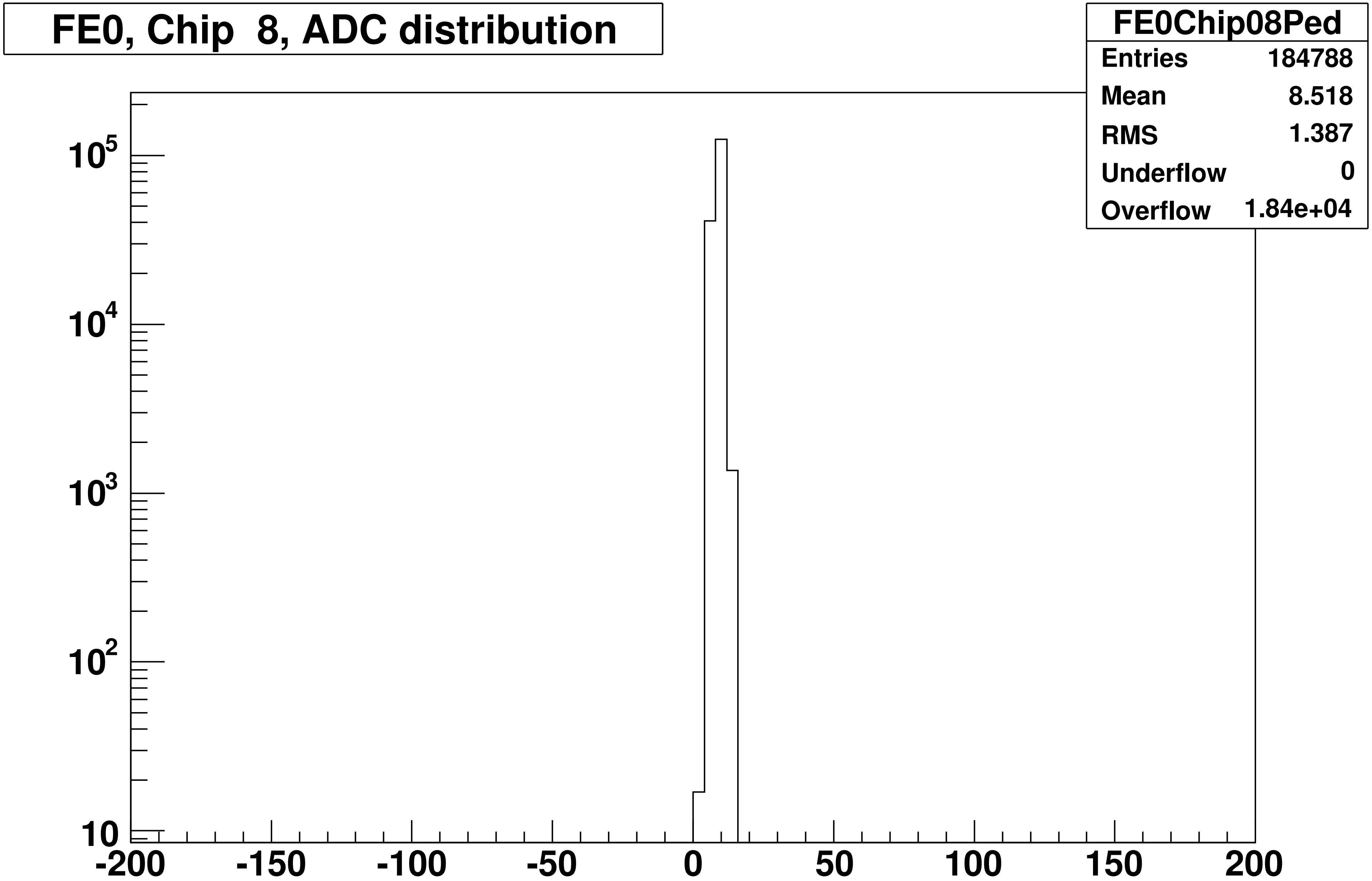
FE0, Chip 8, ADC distribution
FE0Chip08Ped
Entries 184788
Mean 8.518
RMS 1.387
Underflow 0
Overflow 1.84e+04
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10^3
10^4
10^5
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-100
-50
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100
150
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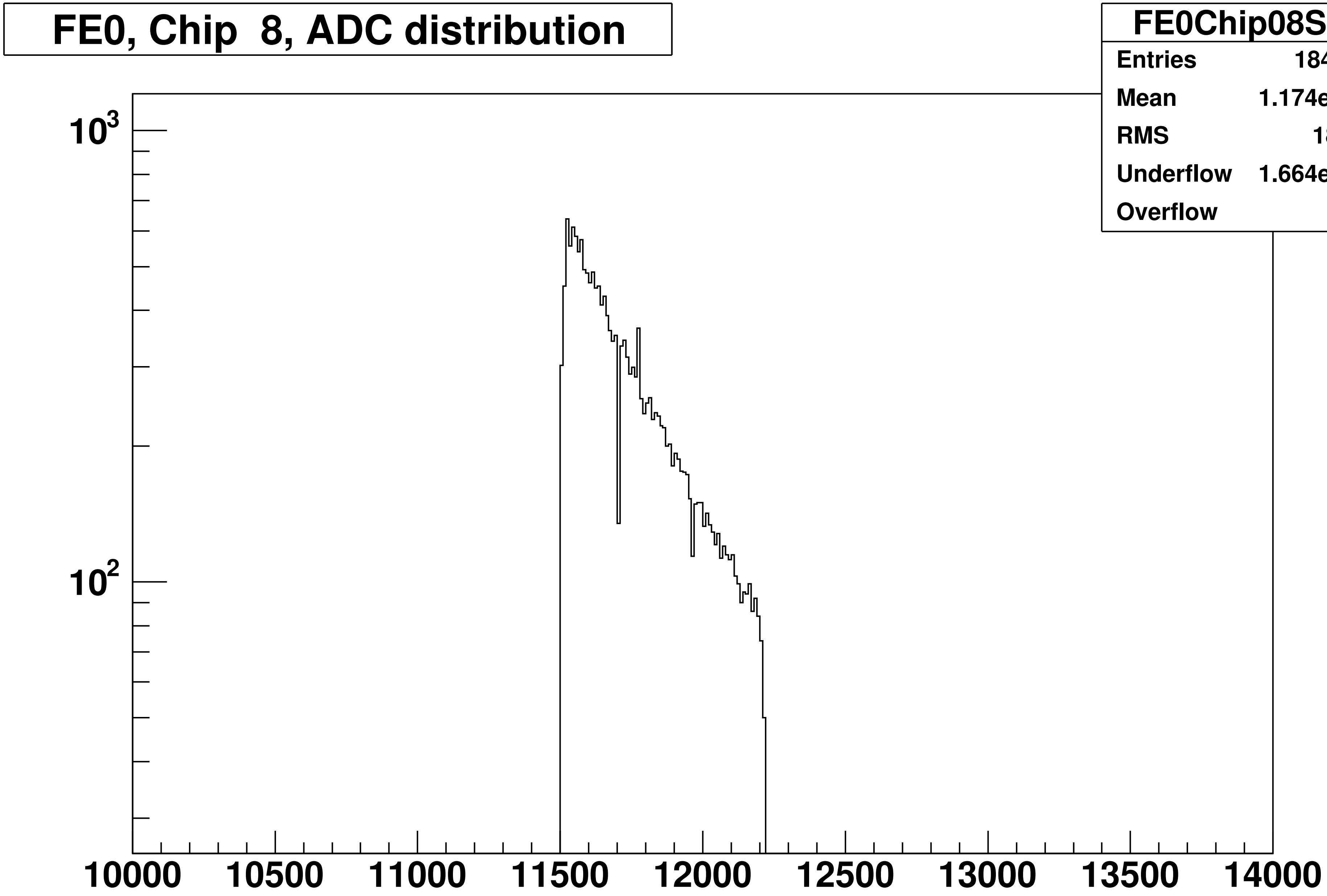
FE0, Chip 8, ADC distribution
FE0Chip08Sig
Entries 184788
Mean 1.174e+04
RMS 185.9
Underflow 1.664e+05
Overflow 0
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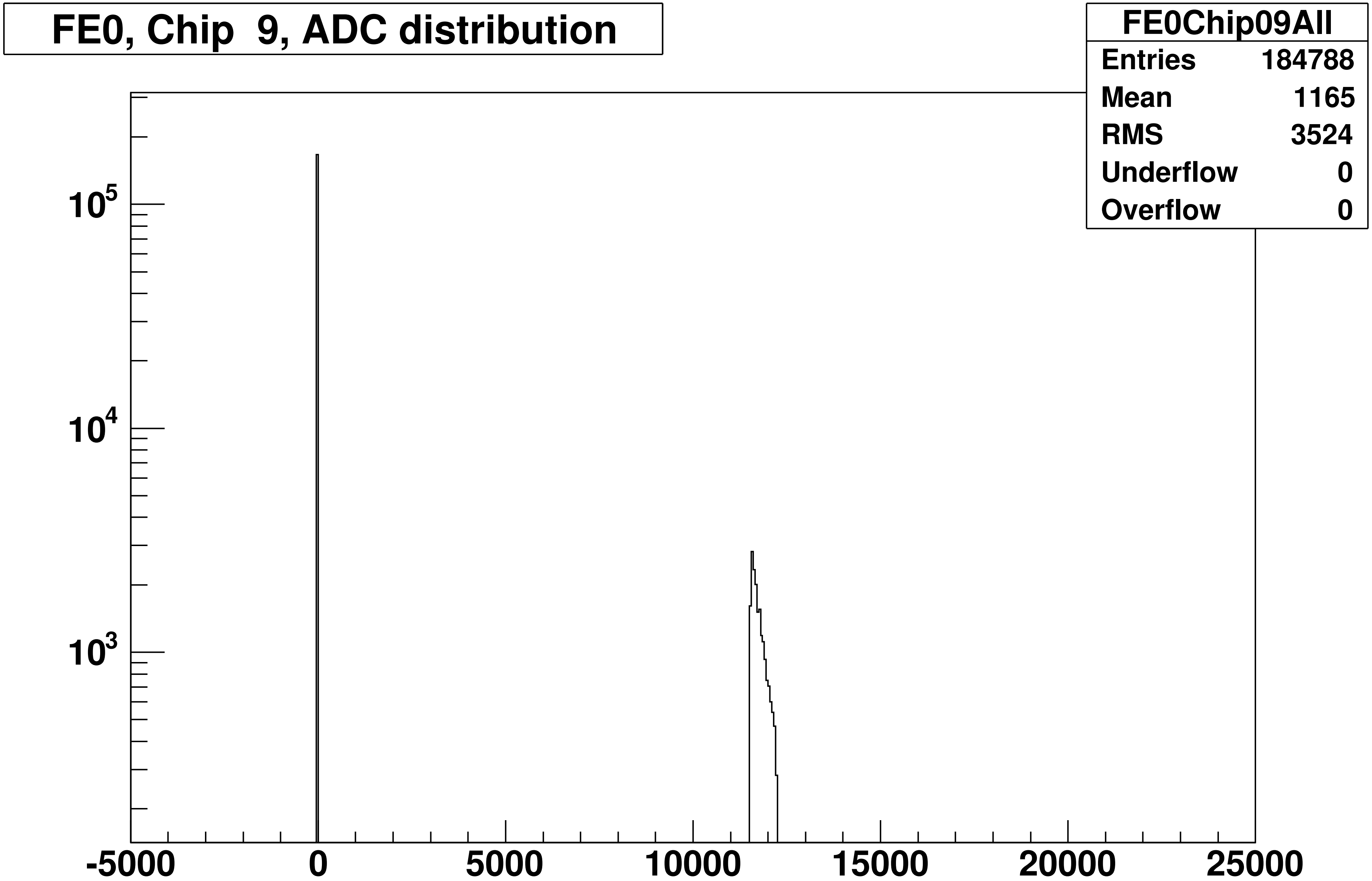
FE0, Chip 9, ADC distribution
FE0Chip09All
Entries 184788
Mean 1165
RMS 3524
Underflow 0
Overflow 0
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10^4
10^3
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0
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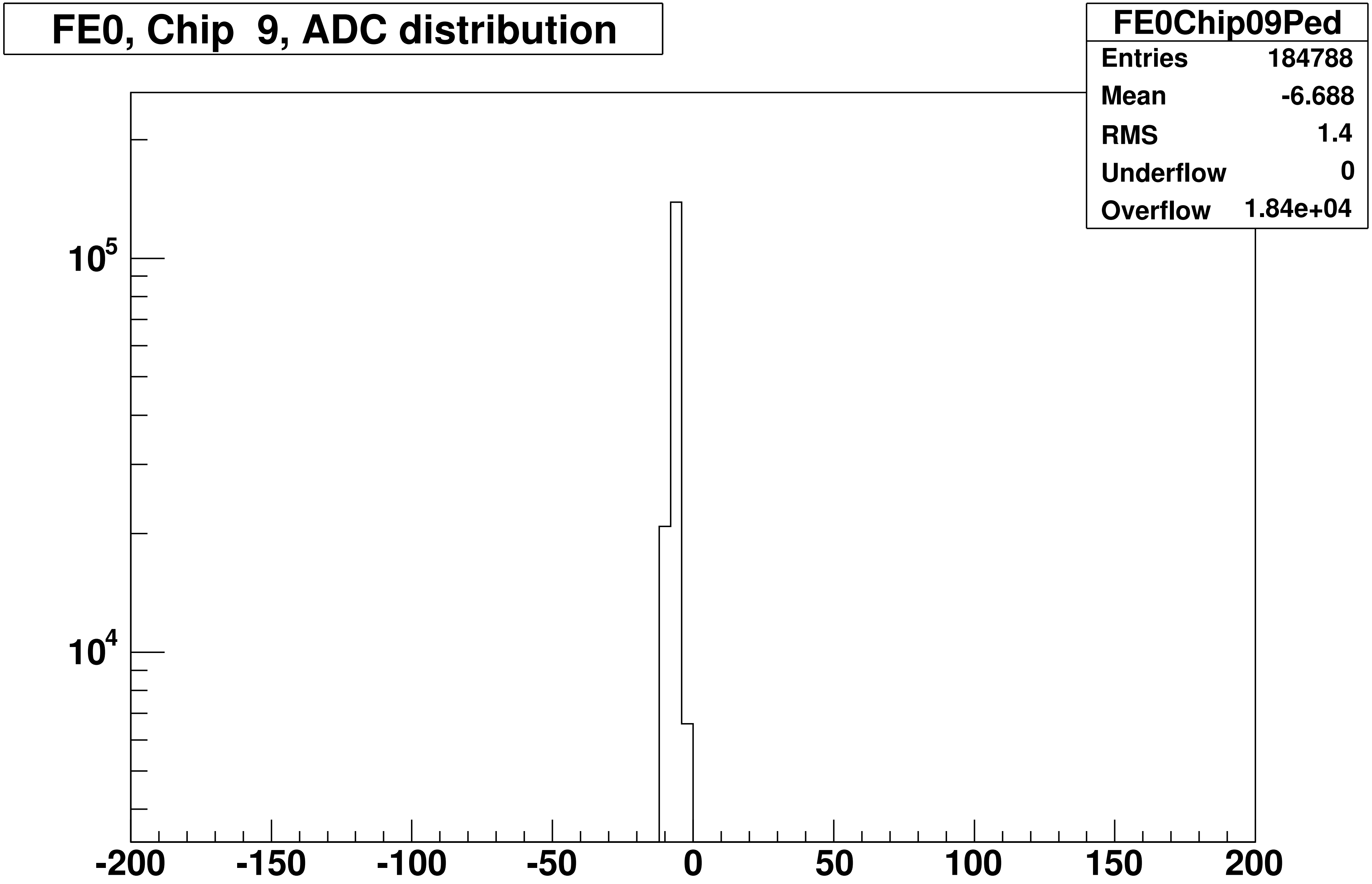
20000
25000


FE0, Chip 9, ADC distribution
FE0Chip09Ped
Entries 184788
Mean -6.688
RMS 1.4
Underflow 0
Overflow 1.84e+04
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10^4
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-150
-100
-50
0
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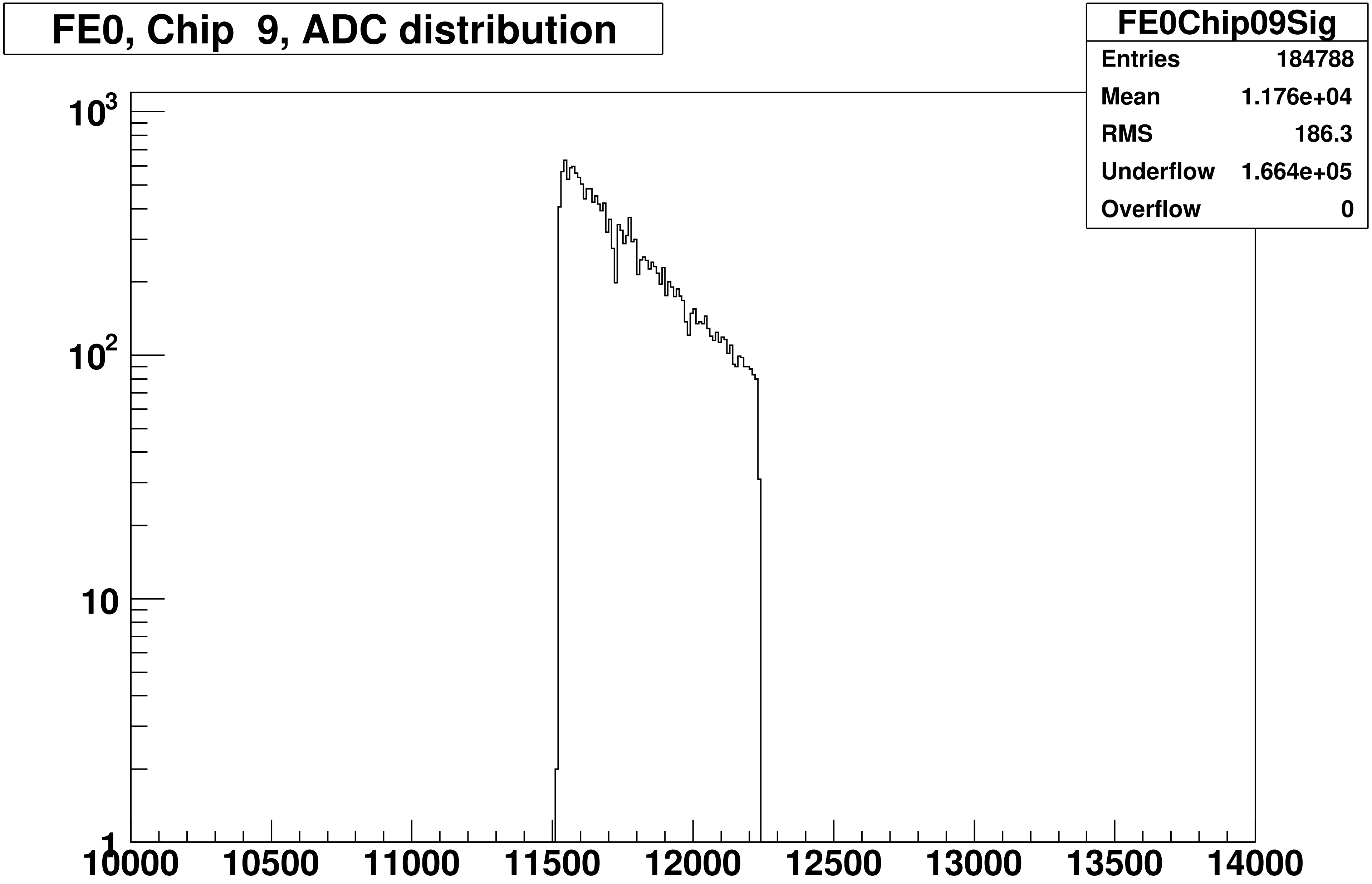
150
200



FE0, Chip 9, ADC distribution
FE0Chip09Sig
Entries 184788
Mean 1.176e+04
RMS 186.3
Underflow 1.664e+05
Overflow 0
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10^2
10
1
10000
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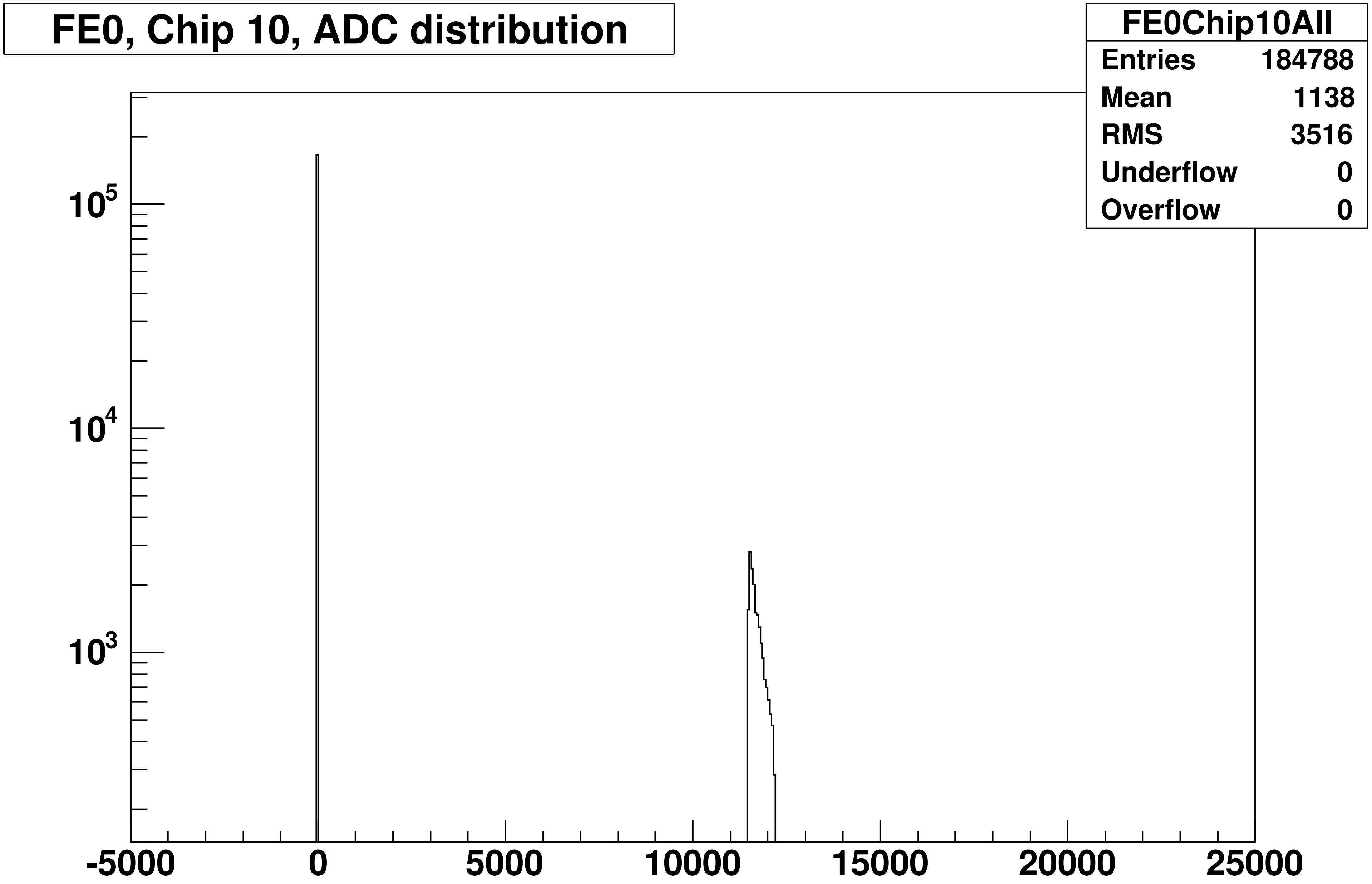
FE0, Chip 10, ADC distribution
FE0Chip10All
Entries 184788
Mean 1138
RMS 3516
Underflow 0
Overflow 0
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10^4
10^3
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0
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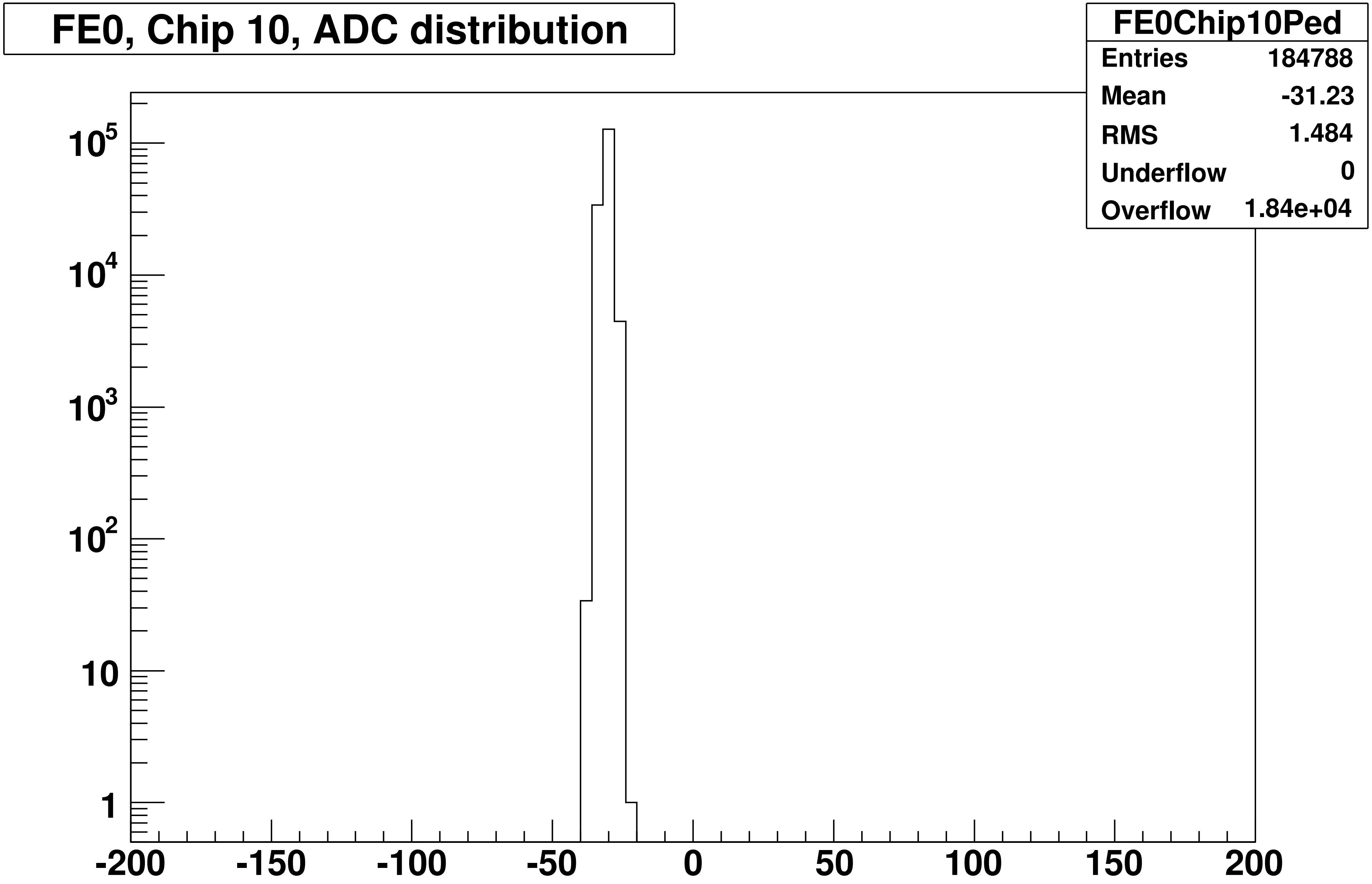
20000
25000


FE0, Chip 10, ADC distribution
FE0Chip10Ped
Entries 184788
Mean -31.23
RMS 1.484
Underflow 0
Overflow 1.84e+04
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10^3
10^2
10
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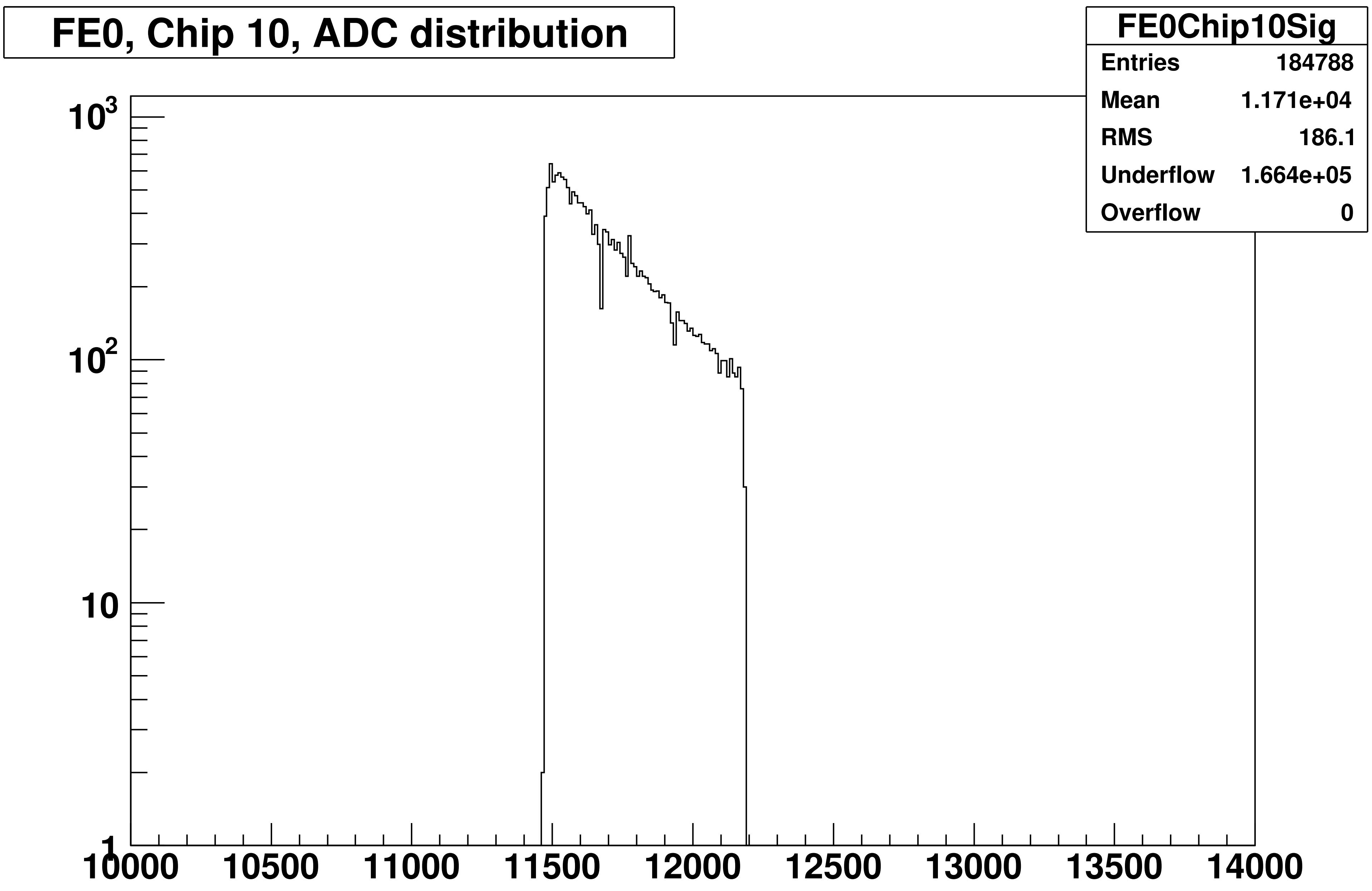
150
200


FE0, Chip 10, ADC distribution
FE0Chip10Sig
Entries 184788
Mean 1.171e+04
RMS 186.1
Underflow 1.664e+05
Overflow 0
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10^2
10
1
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11500
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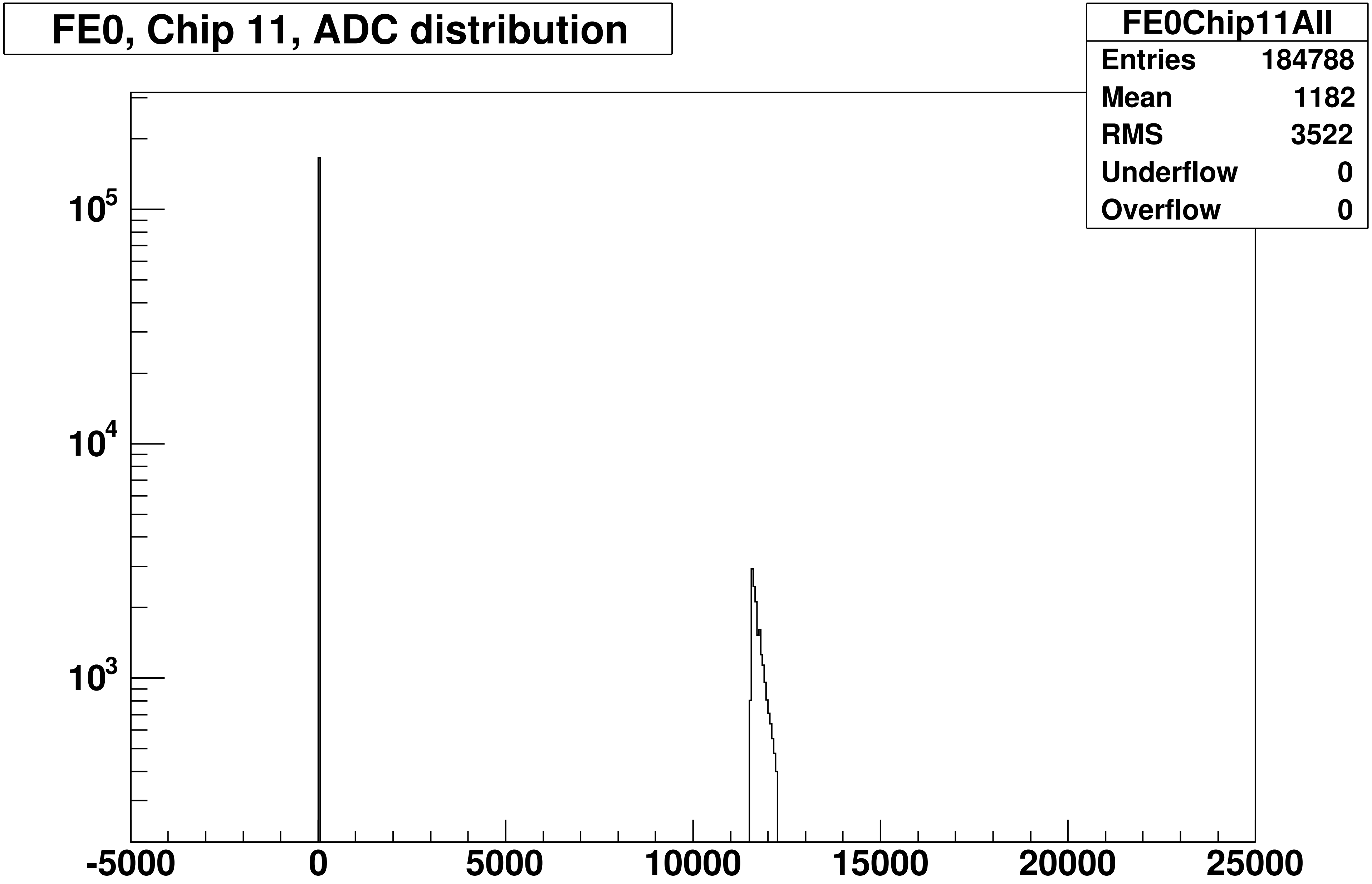
FE0, Chip 11, ADC distribution
FE0Chip11All
Entries 184788
Mean 1182
RMS 3522
Underflow 0
Overflow 0
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10^4
10^3
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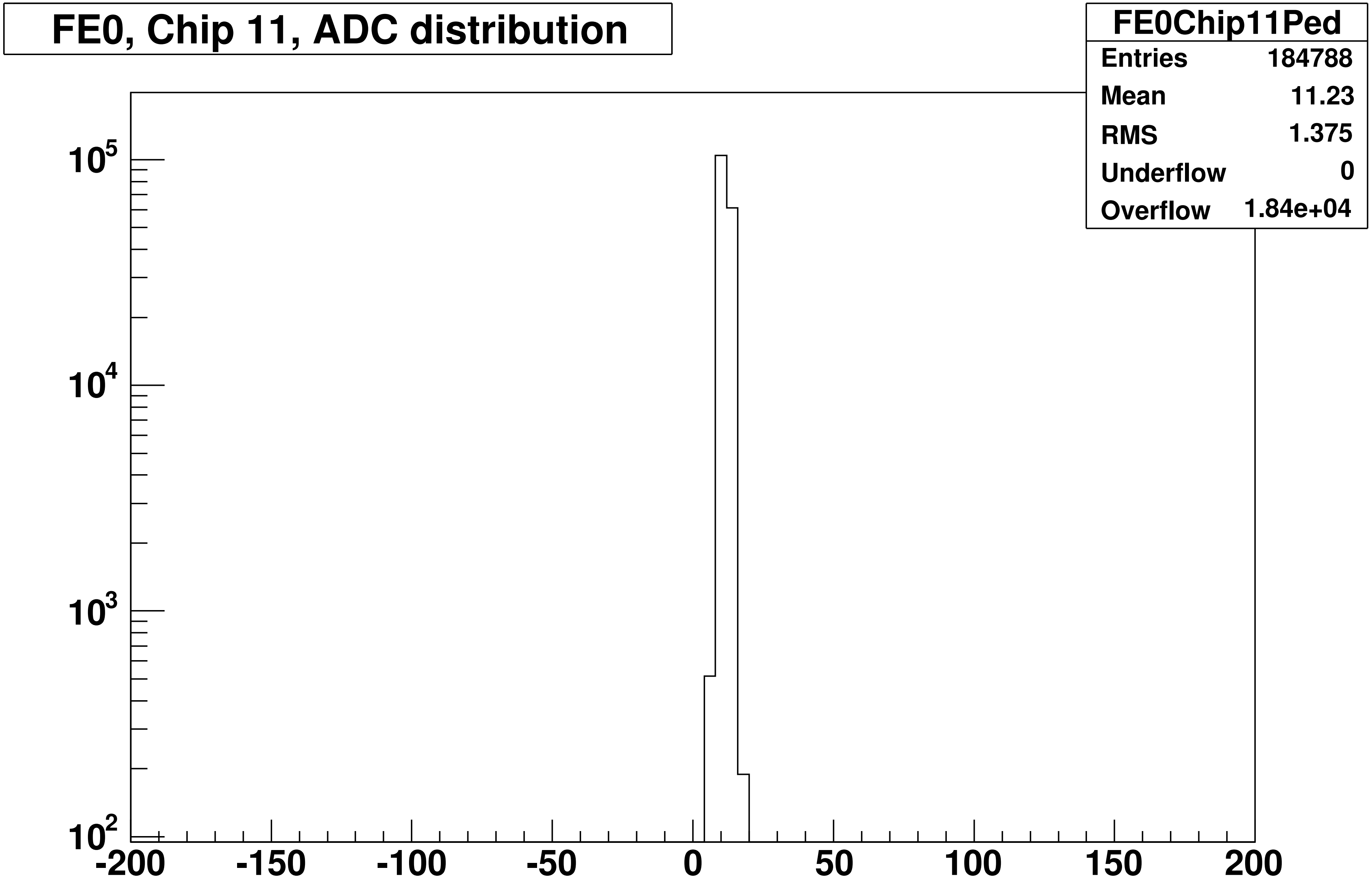
10000
15000
20000
25000


FE0, Chip 11, ADC distribution
FE0Chip11Ped
Entries 184788
Mean 11.23
RMS 1.375
Underflow 0
Overflow 1.84e+04
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10^4
10^3
10^2
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-100
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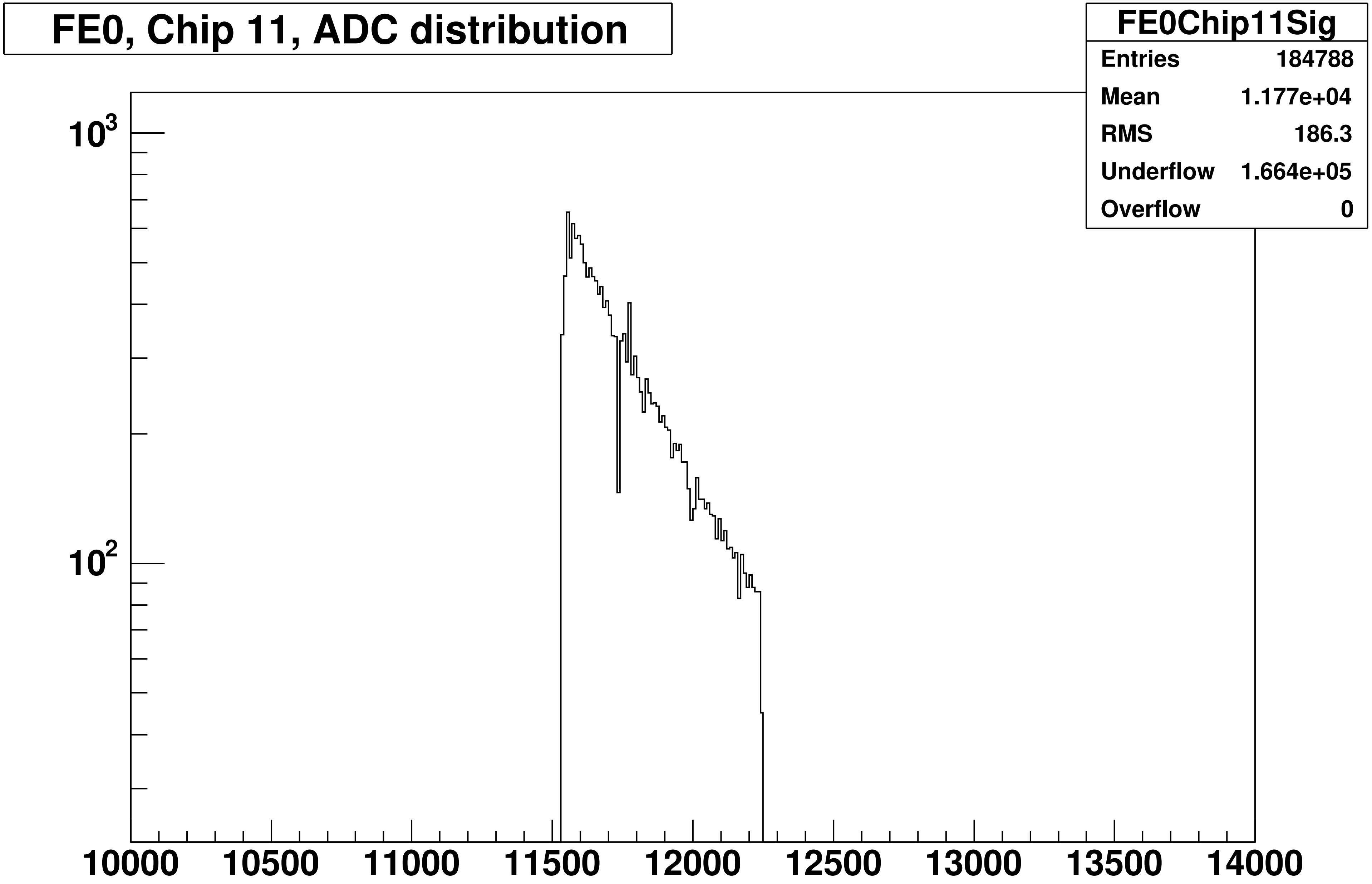
200


FE0, Chip 11, ADC distribution
FE0Chip11Sig
Entries 184788
Mean 1.177e+04
RMS 186.3
Underflow 1.664e+05
Overflow 0
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10^2
10000
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11500
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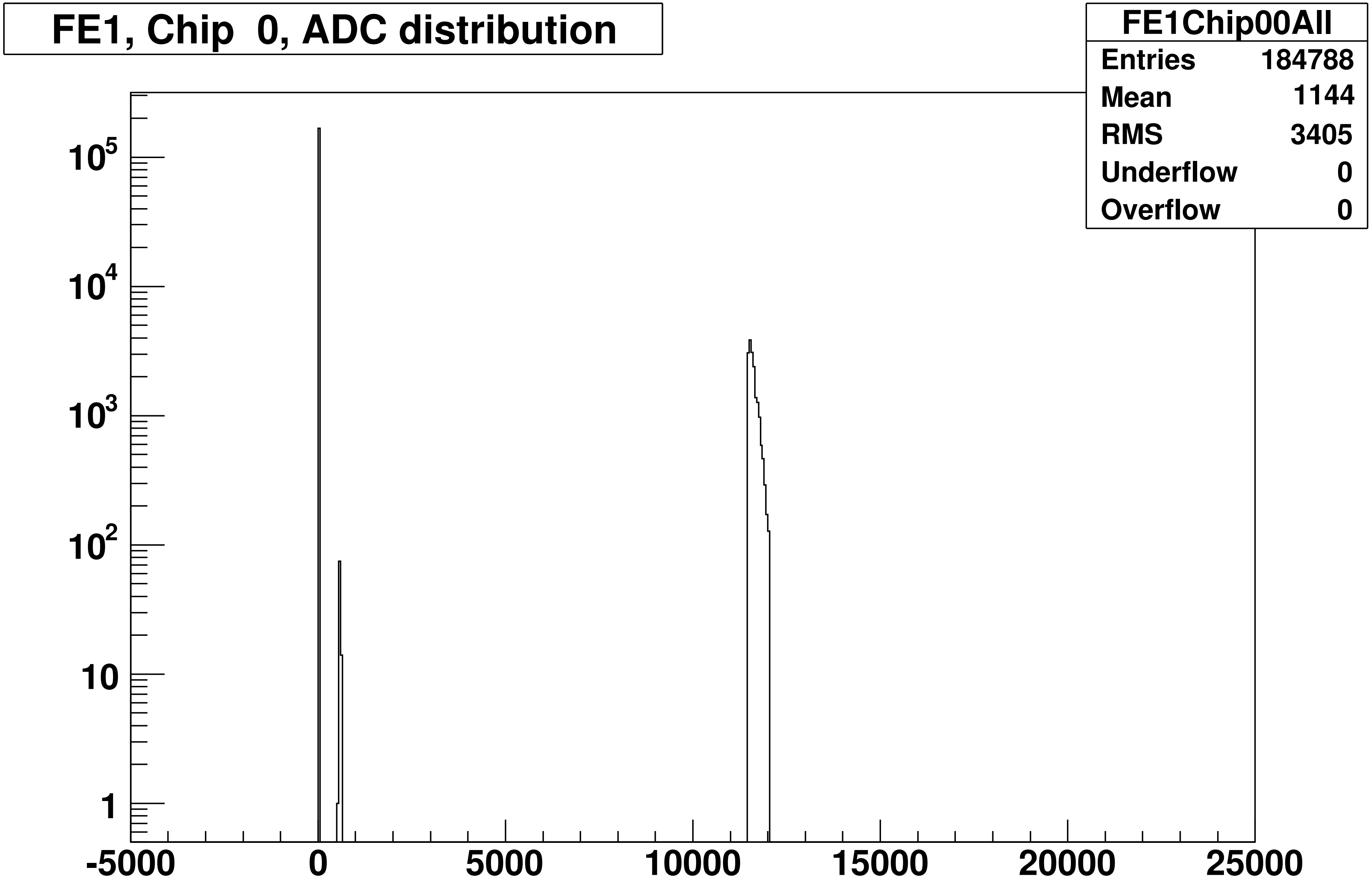
FE1, Chip 0, ADC distribution
FE1Chip00All
Entries 184788
Mean 1144
RMS 3405
Underflow 0
Overflow 0
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10^4
10^3
10^2
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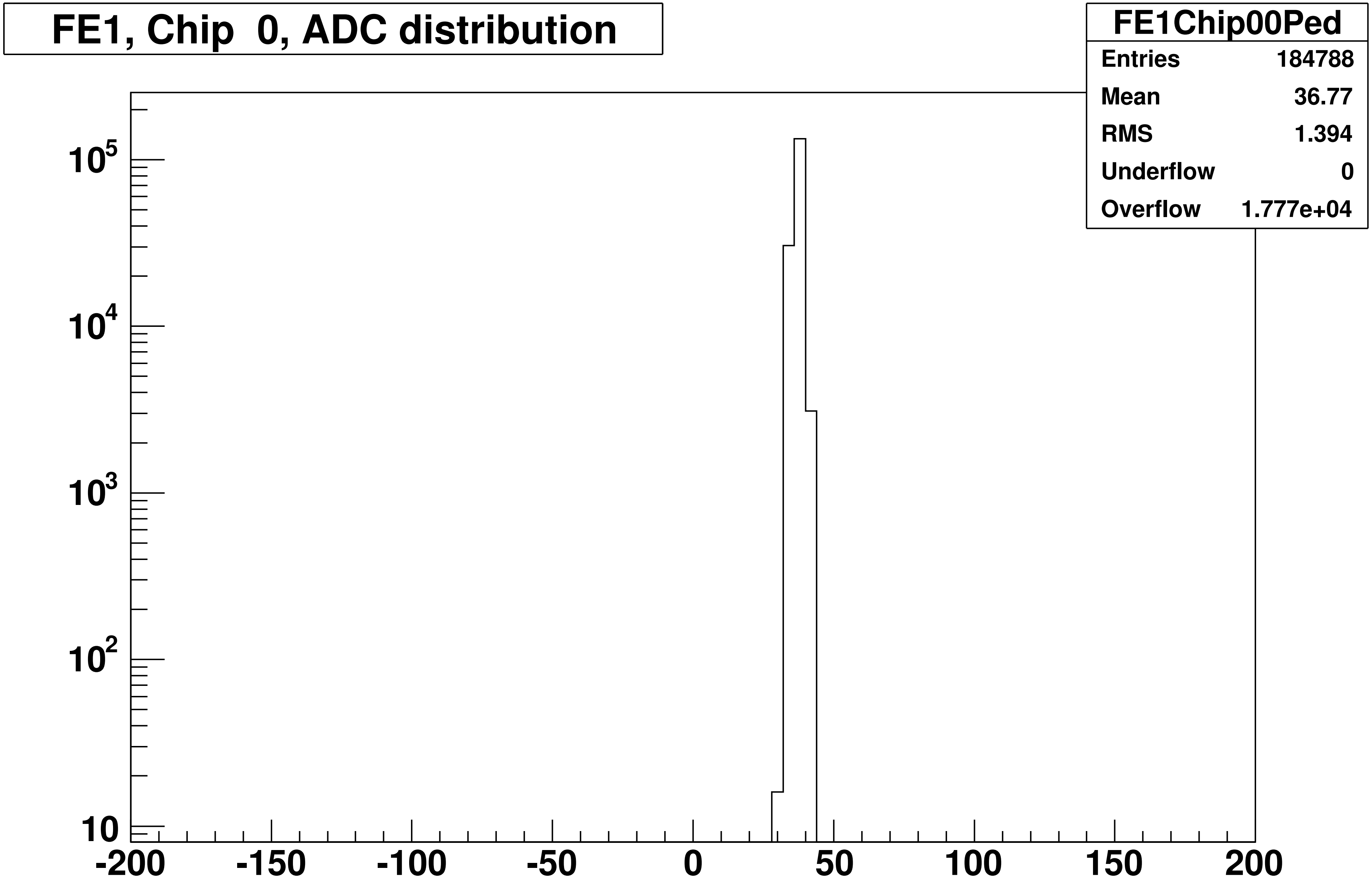
FE1, Chip 0, ADC distribution
FE1Chip00Ped
Entries 184788
Mean 36.77
RMS 1.394
Underflow 0
Overflow 1.777e+04
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10^3
10^4
10^5
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-100
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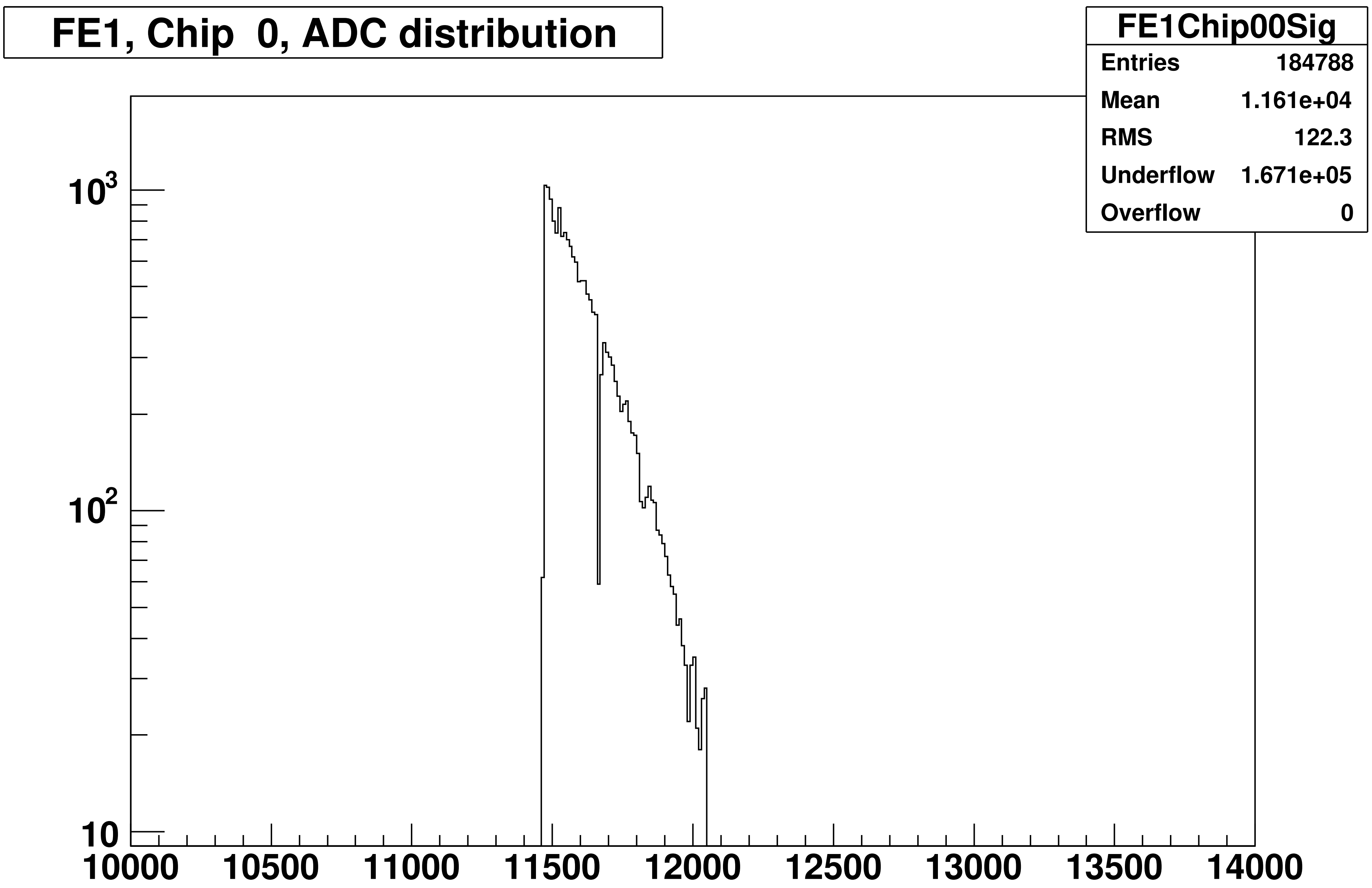
100
150
200


FE1, Chip 0, ADC distribution
FE1Chip00Sig
Entries 184788
Mean 1.161e+04
RMS 122.3
Underflow 1.671e+05
Overflow 0
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10^2
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10000
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11500
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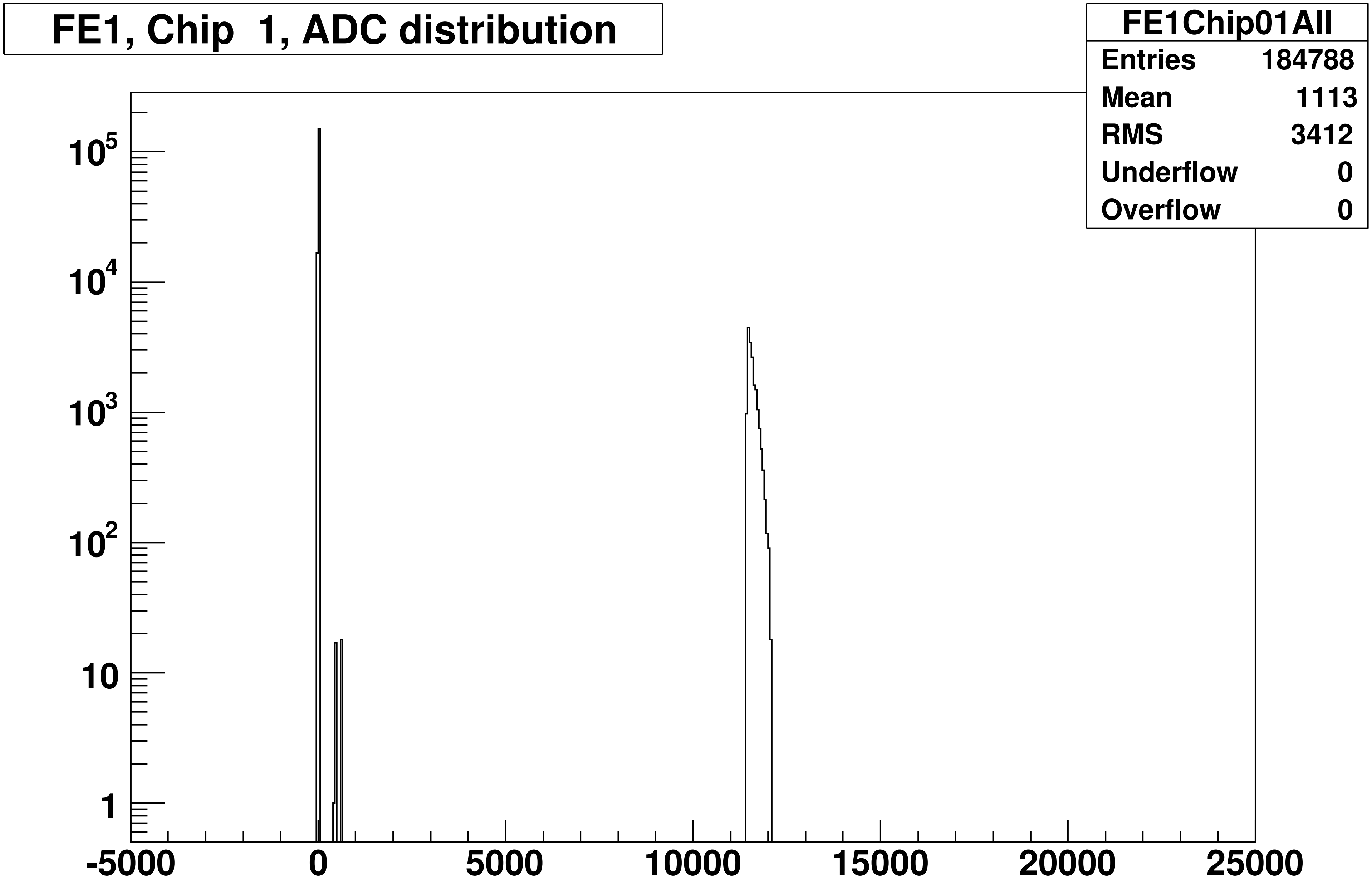
13500
14000


FE1, Chip 1, ADC distribution
FE1Chip01All
Entries 184788
Mean 1113
RMS 3412
Underflow 0
Overflow 0
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10^4
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10^2
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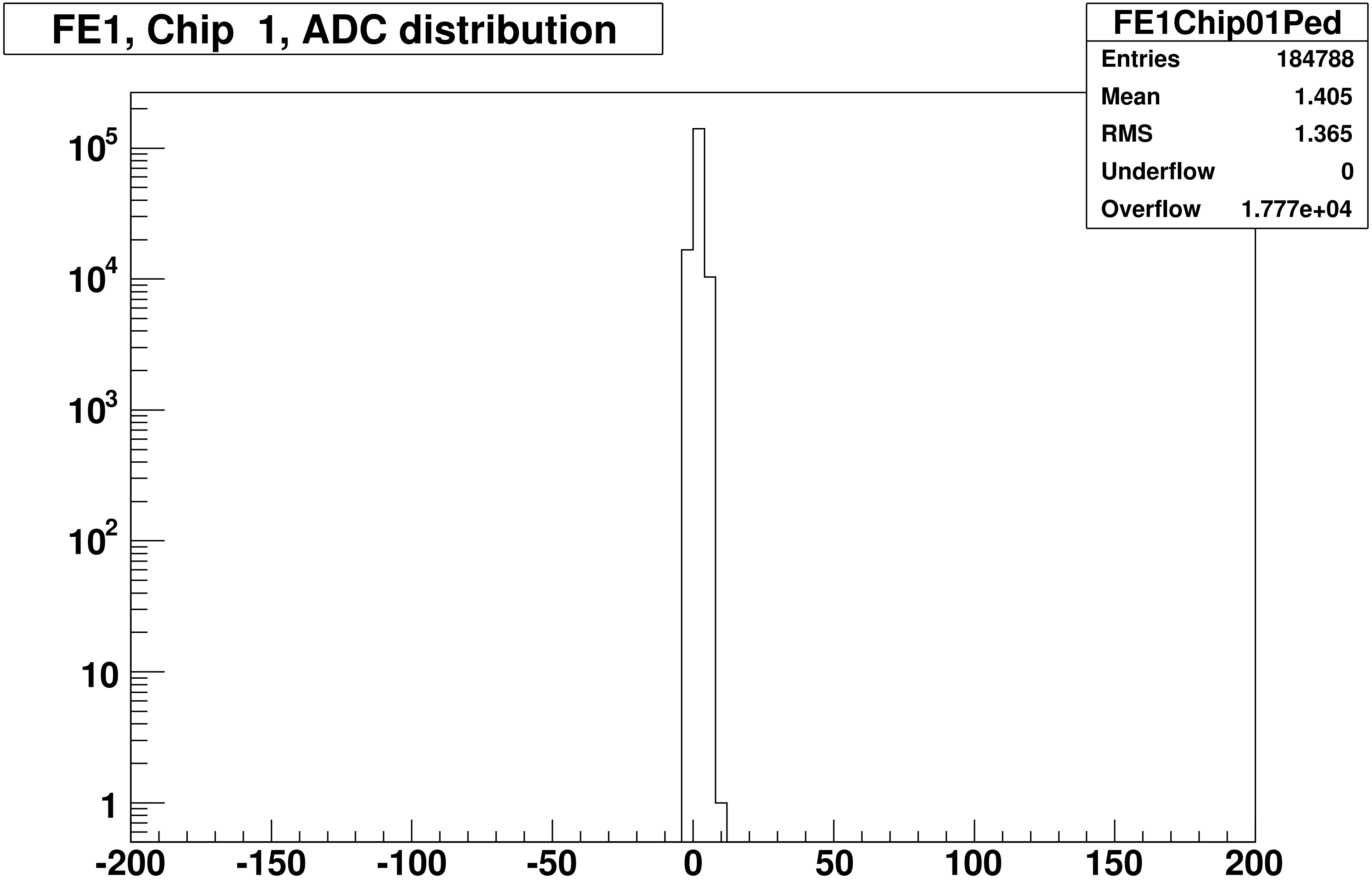
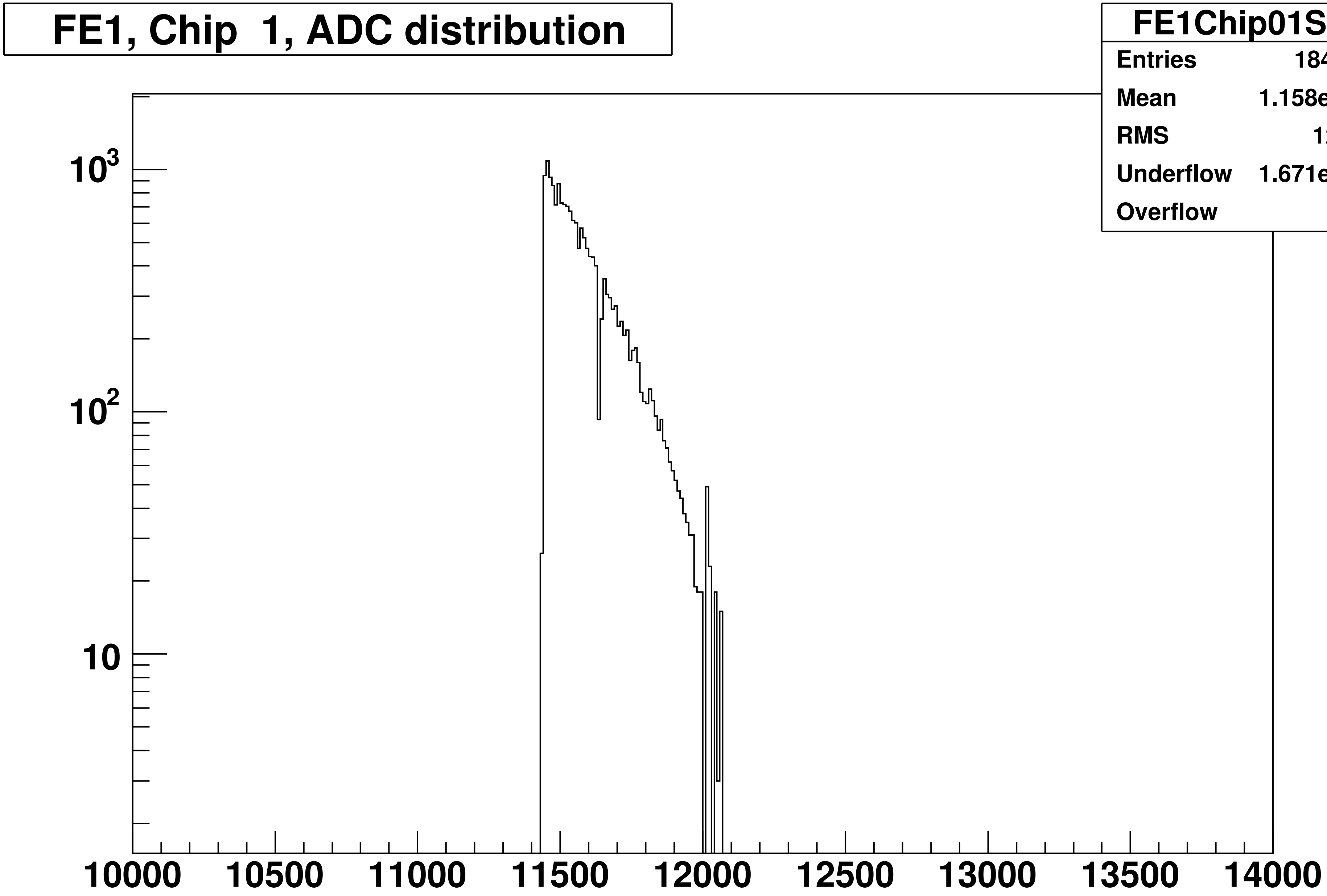
25000



FE1, Chip 1, ADC distribution
FE1Chip01Ped
Entries 184788
Mean 1.405
RMS 1.365
Underflow 0
Overflow 1.777e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 1, ADC distribution
FE1Chip01Sig
Entries 184788
Mean 1.158e+04
RMS 124.3
Underflow 1.671e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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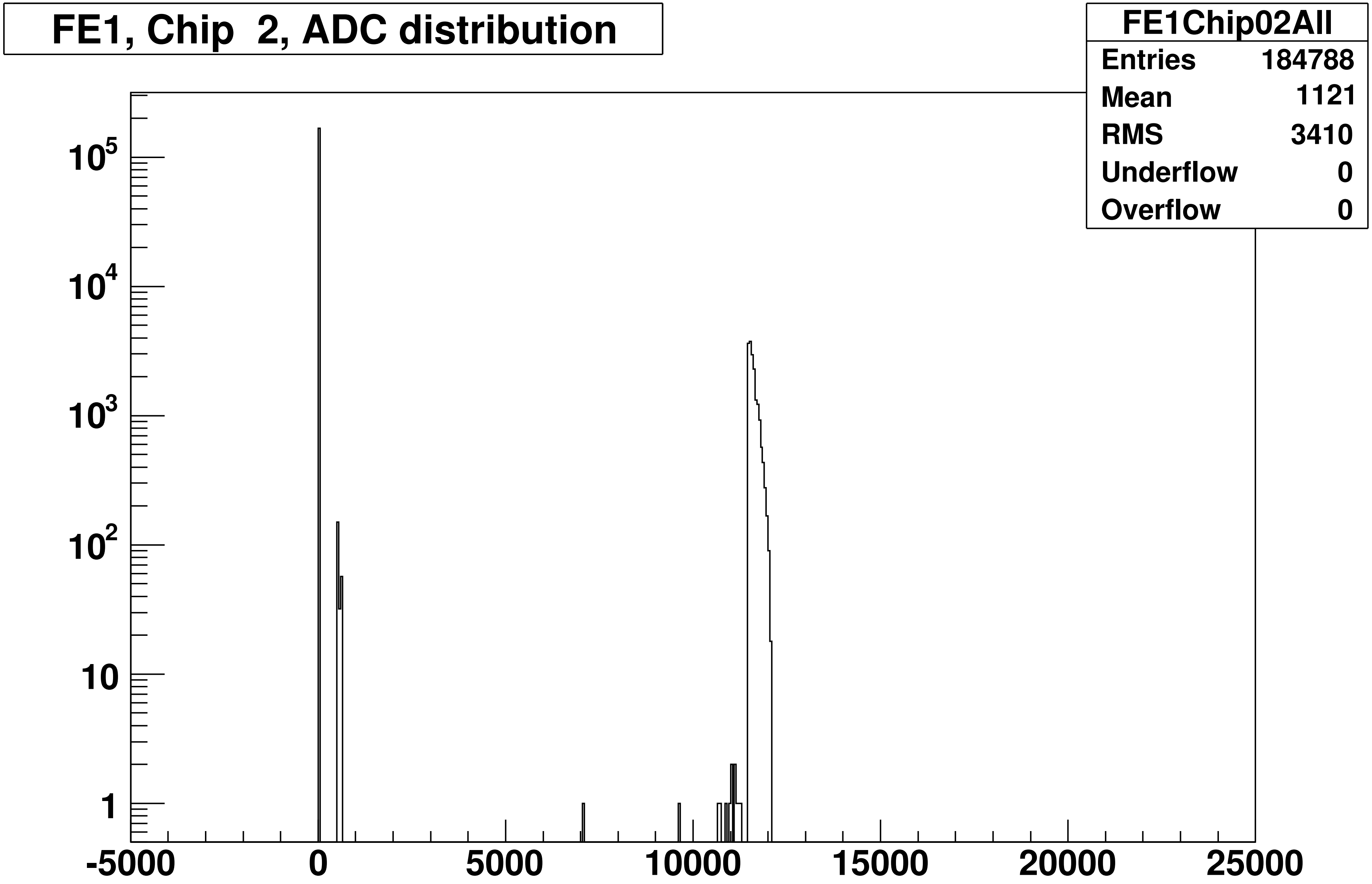
13500
14000


FE1, Chip 2, ADC distribution
FE1Chip02All
Entries 184788
Mean 1121
RMS 3410
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
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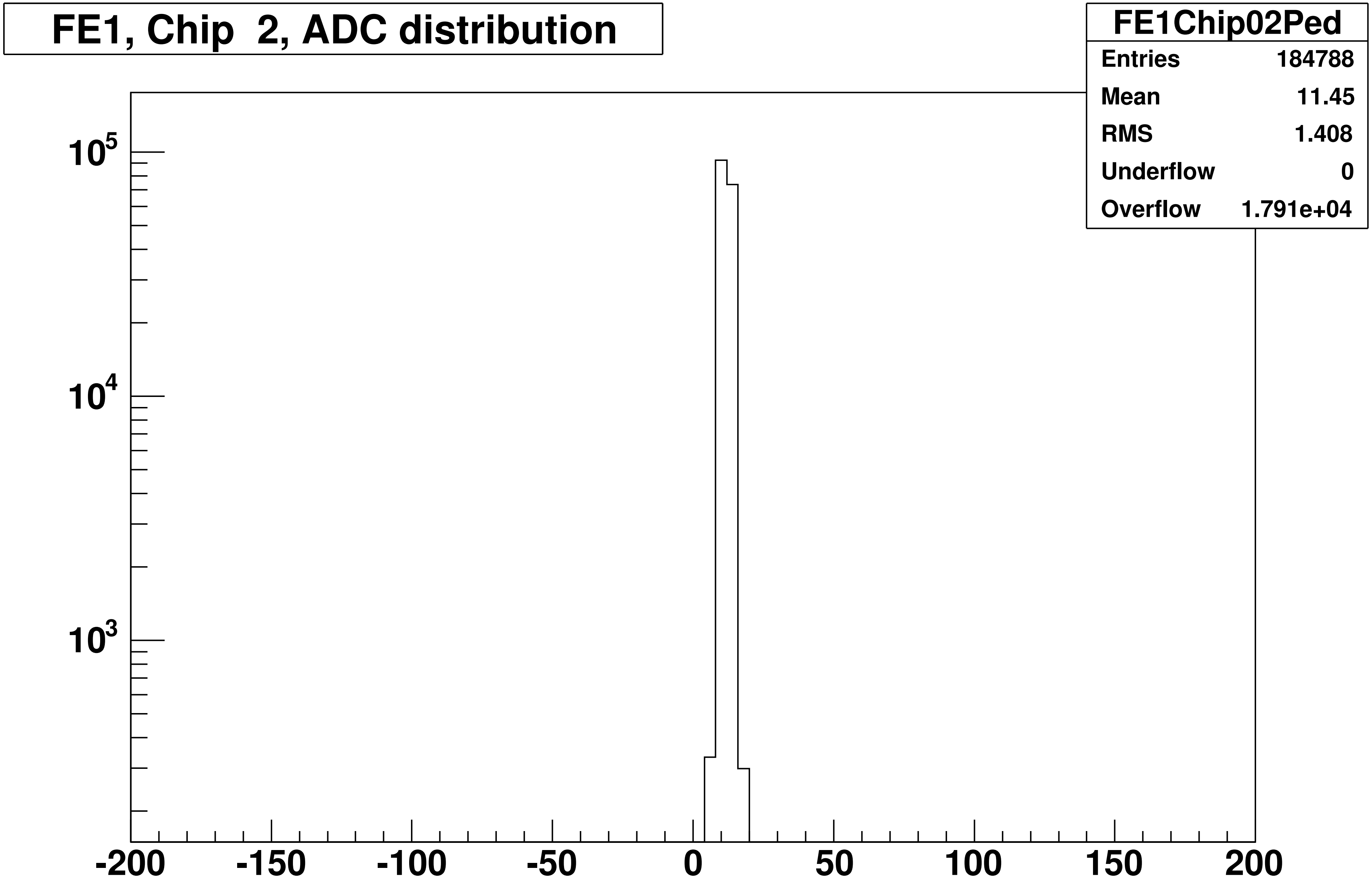
FE1, Chip 2, ADC distribution
FE1Chip02Ped
Entries 184788
Mean 11.45
RMS 1.408
Underflow 0
Overflow 1.791e+04
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10^4
10^3
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-150
-100
-50
0
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100
150
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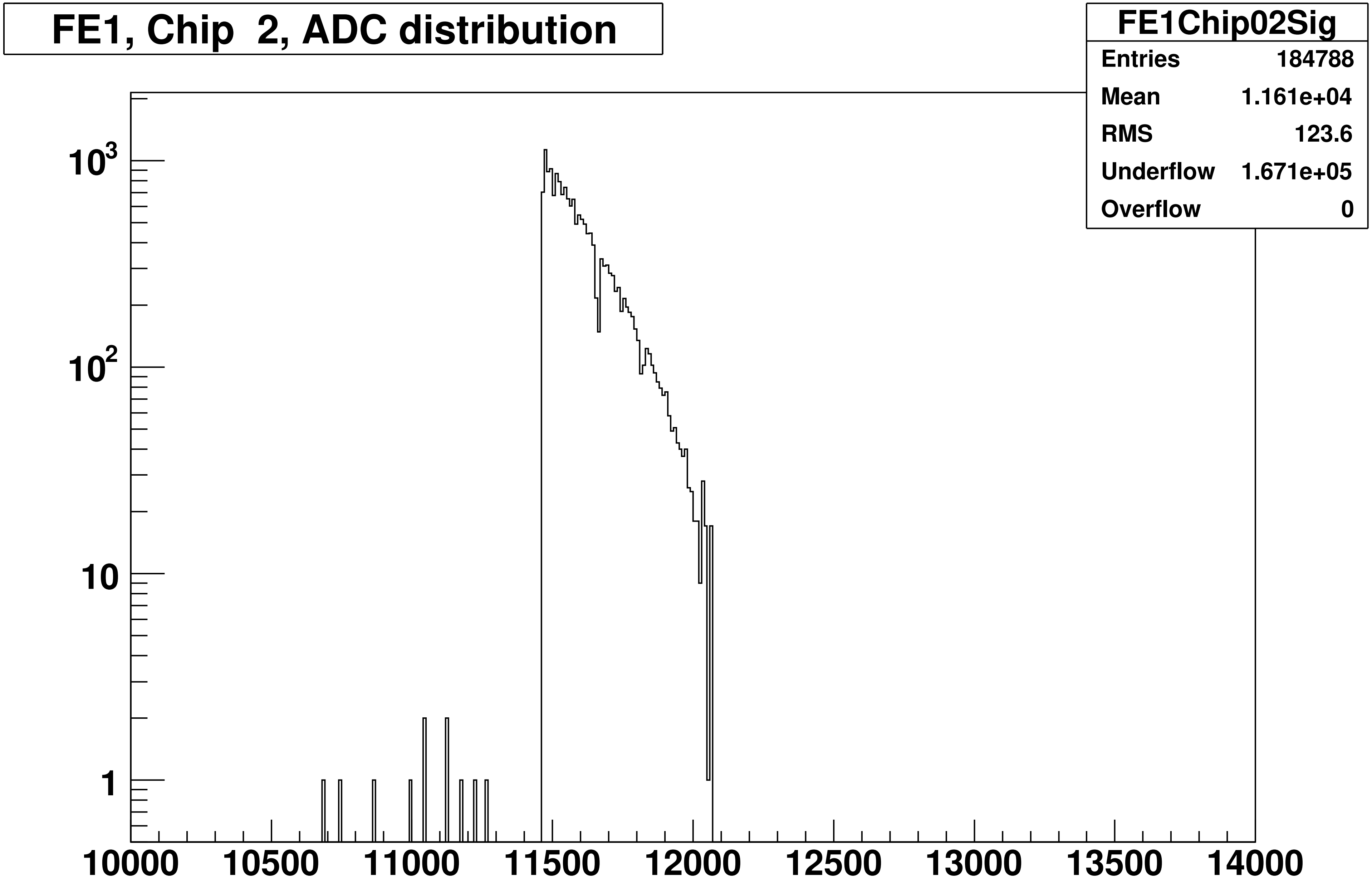
FE1, Chip 2, ADC distribution
FE1Chip02Sig
Entries 184788
Mean 1.161e+04
RMS 123.6
Underflow 1.671e+05
Overflow 0
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10^2
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1
10000
10500
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11500
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13500
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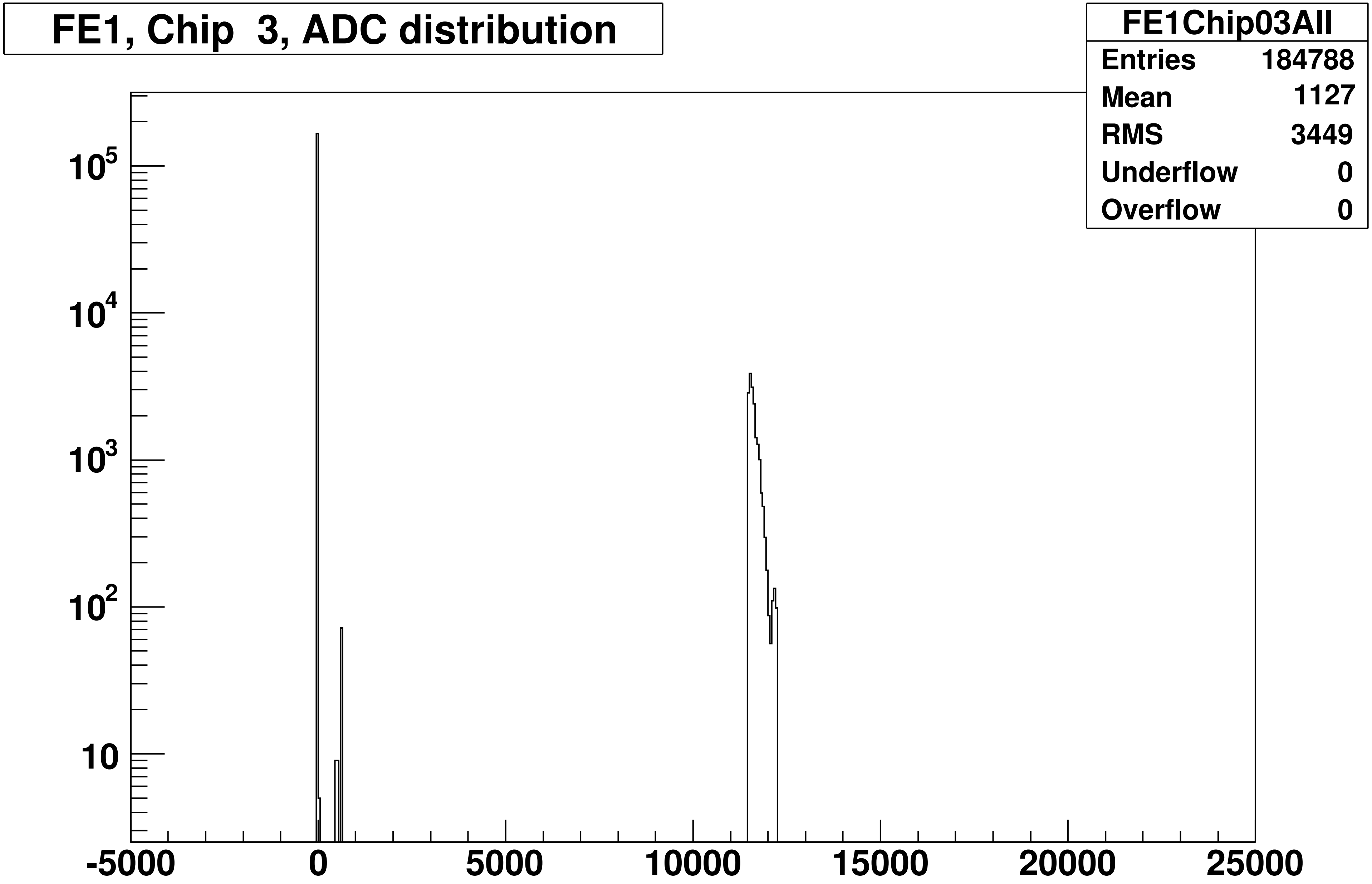
FE1, Chip 3, ADC distribution
FE1Chip03All
Entries 184788
Mean 1127
RMS 3449
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
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5000
10000
15000
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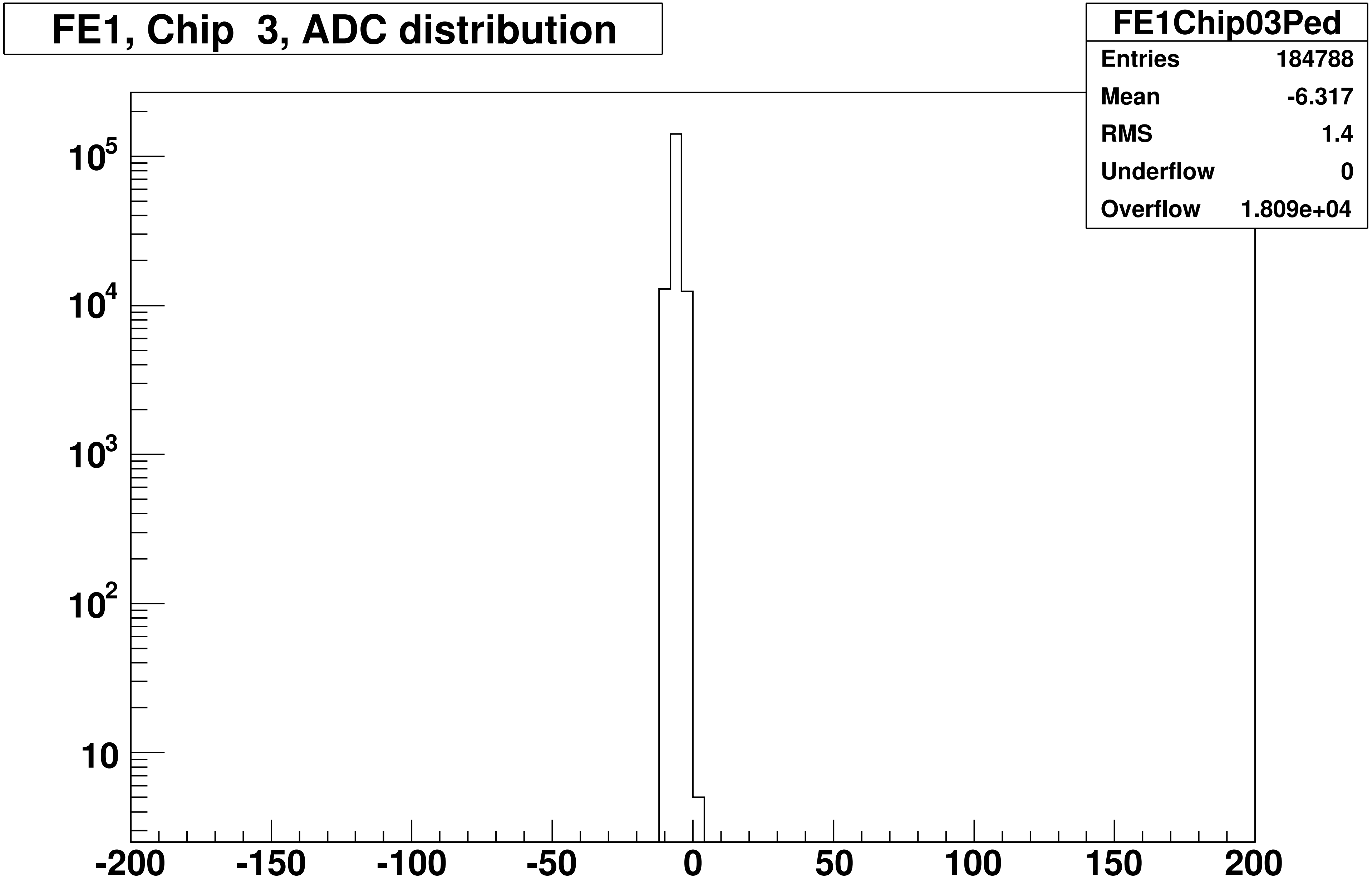
25000


FE1, Chip 3, ADC distribution
FE1Chip03Ped
Entries 184788
Mean -6.317
RMS 1.4
Underflow 0
Overflow 1.809e+04
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10^4
10^3
10^2
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-200
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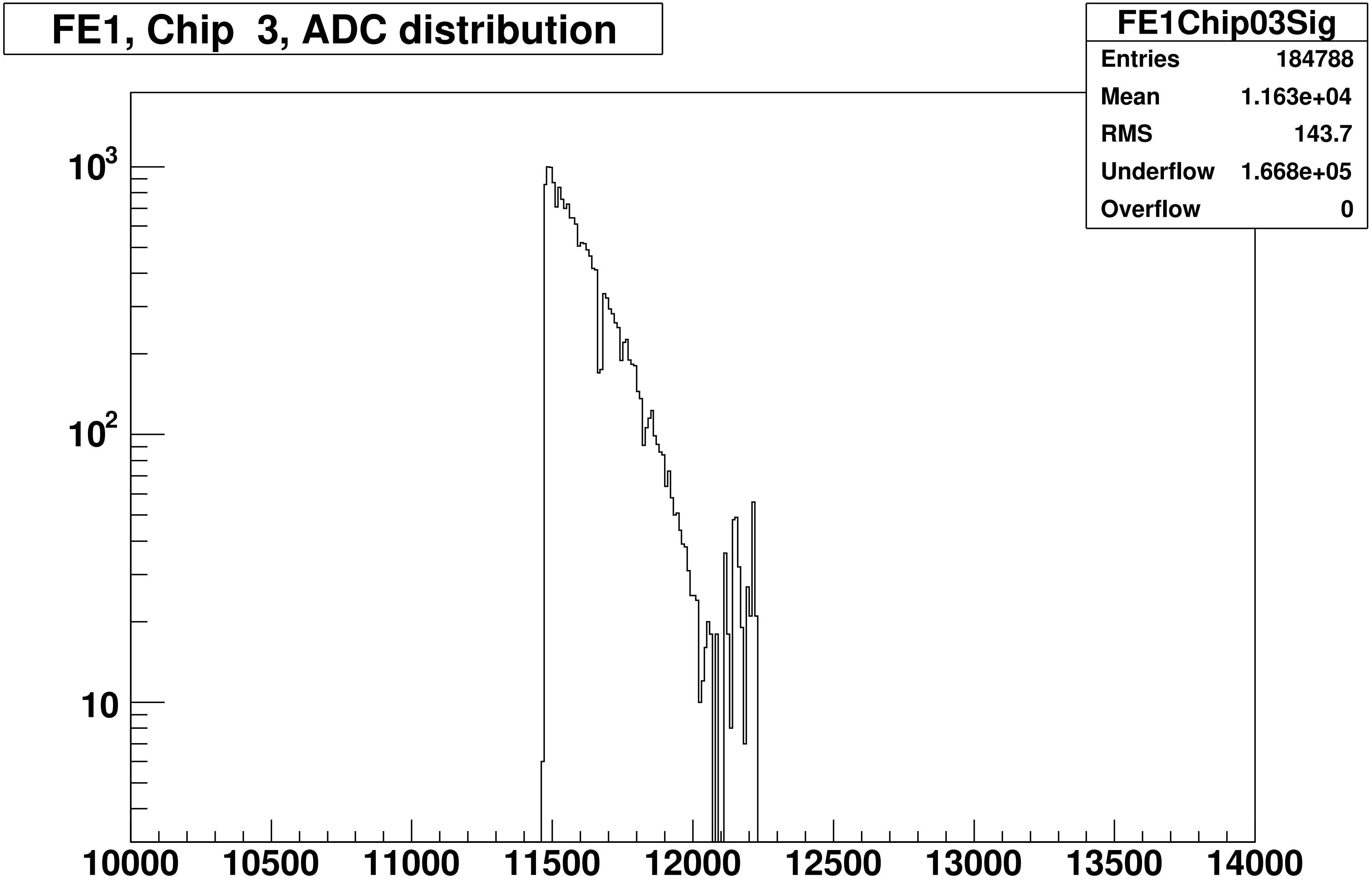
50
100
150
200



FE1, Chip 3, ADC distribution
FE1Chip03Sig
Entries 184788
Mean 1.163e+04
RMS 143.7
Underflow 1.668e+05
Overflow 0
10^3
10^2
10
10000
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11500
12000
12500
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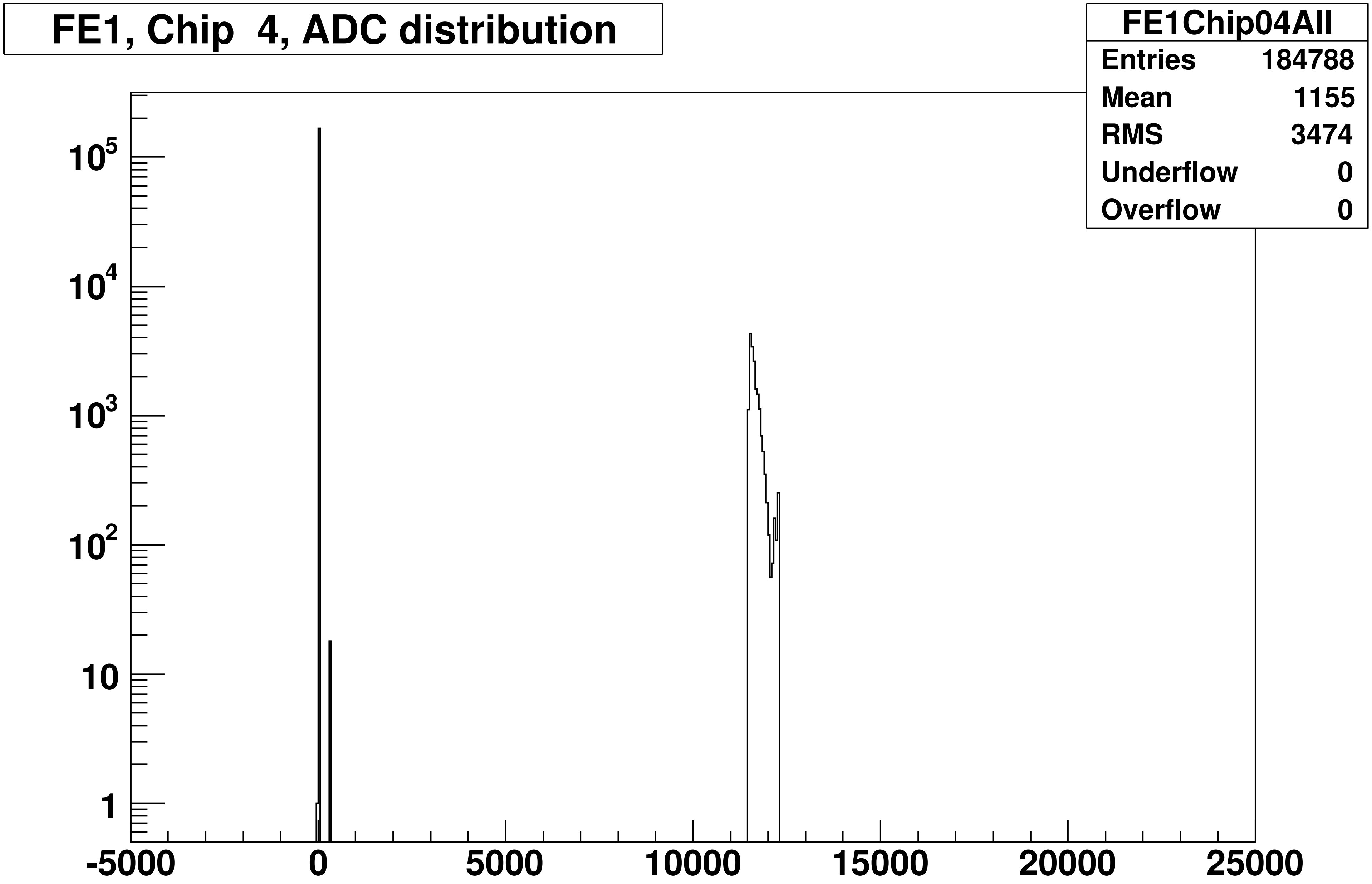
FE1, Chip 4, ADC distribution
FE1Chip04All
Entries 184788
Mean 1155
RMS 3474
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
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10000
15000
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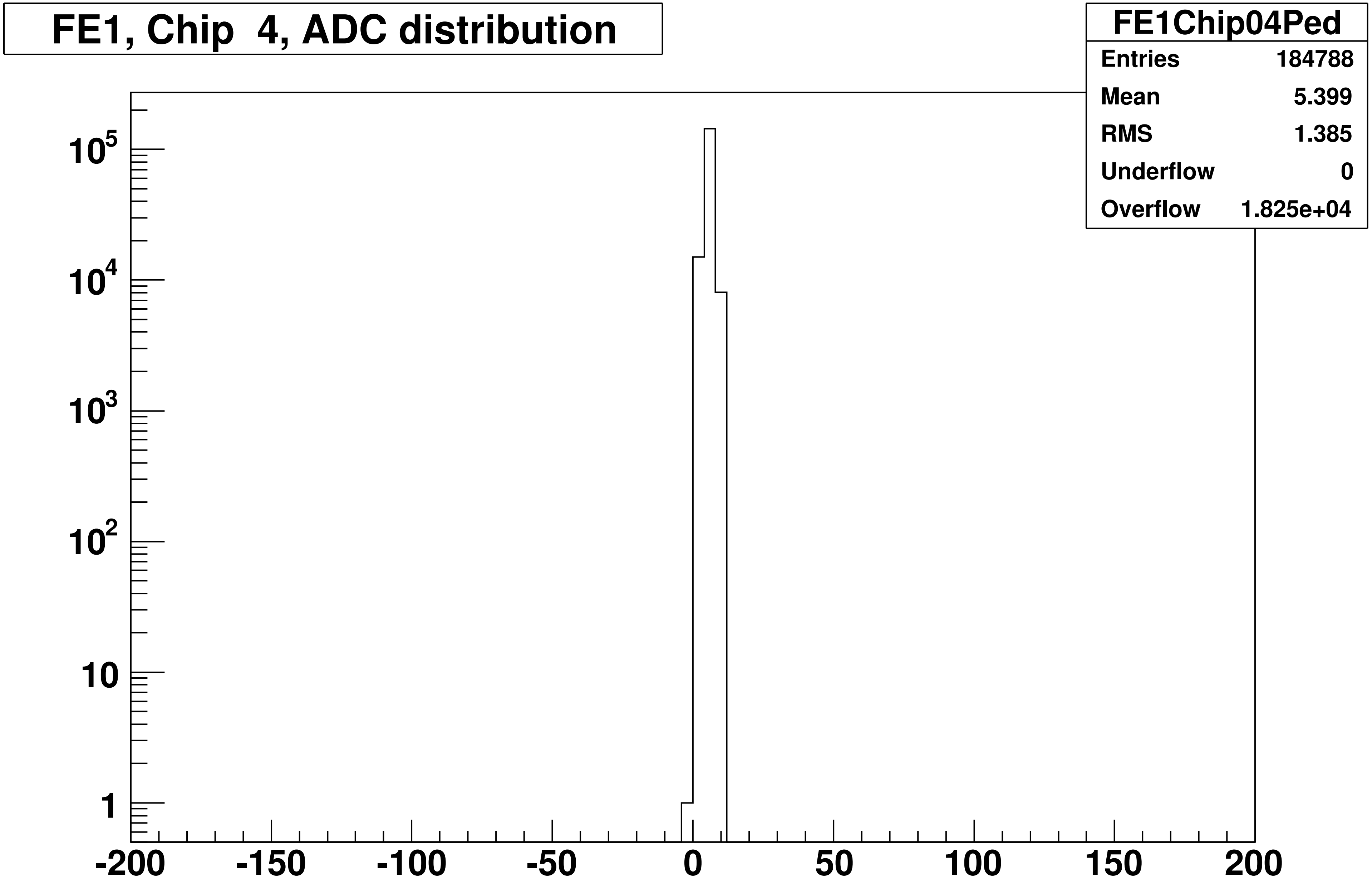
FE1, Chip 4, ADC distribution
FE1Chip04Ped
Entries 184788
Mean 5.399
RMS 1.385
Underflow 0
Overflow 1.825e+04
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10^4
10^3
10^2
10
1
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-150
-100
-50
0
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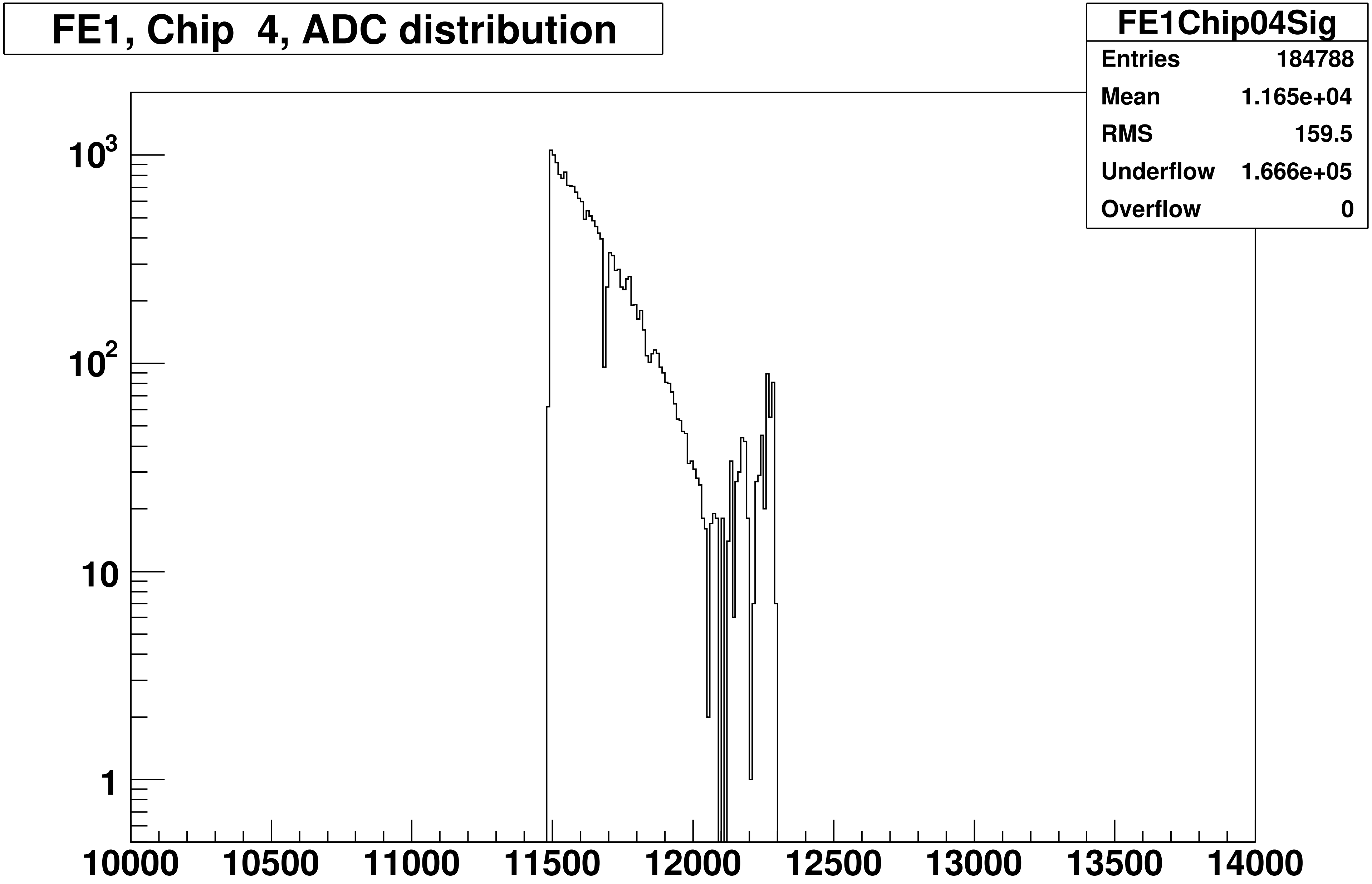
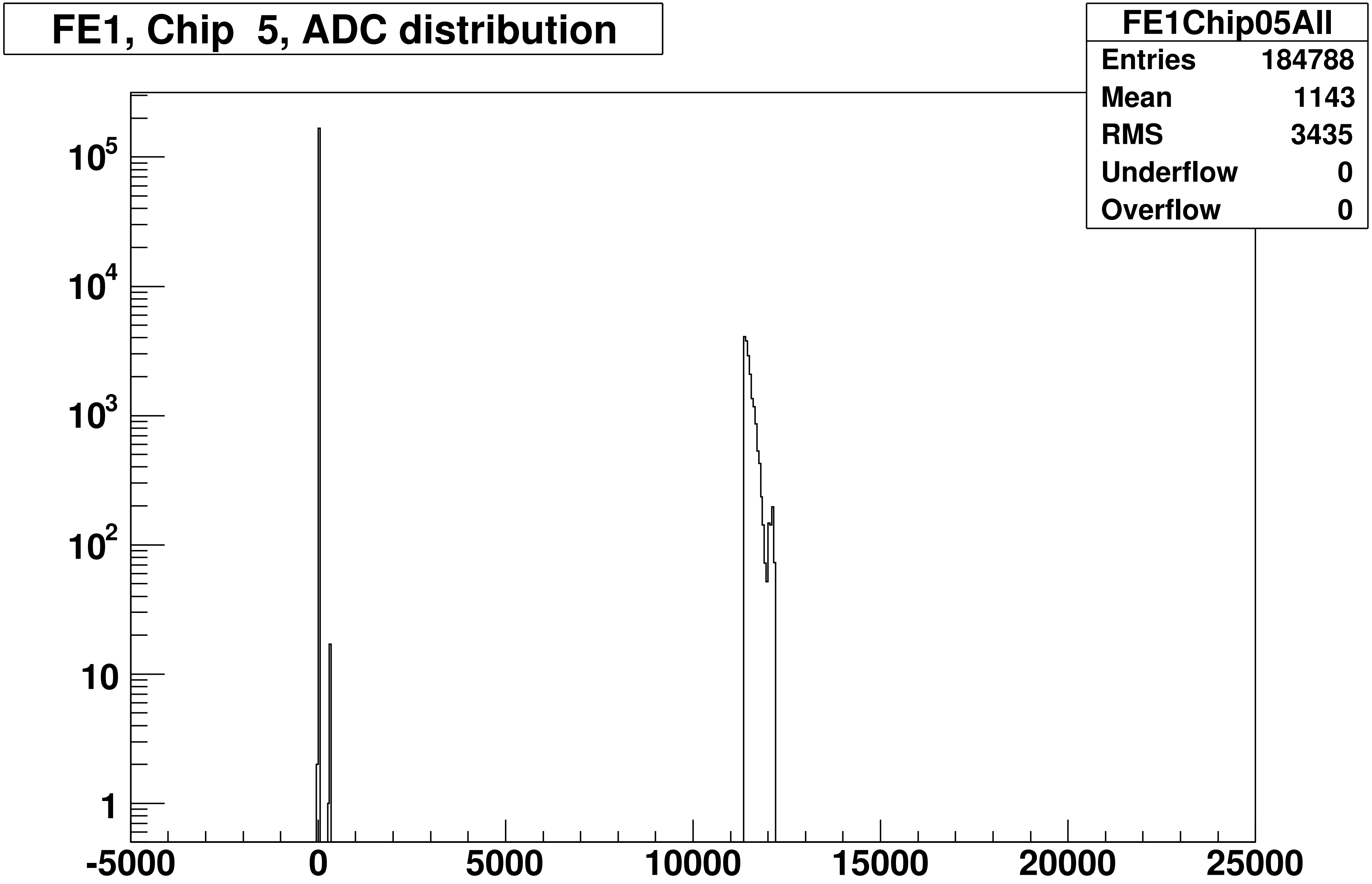
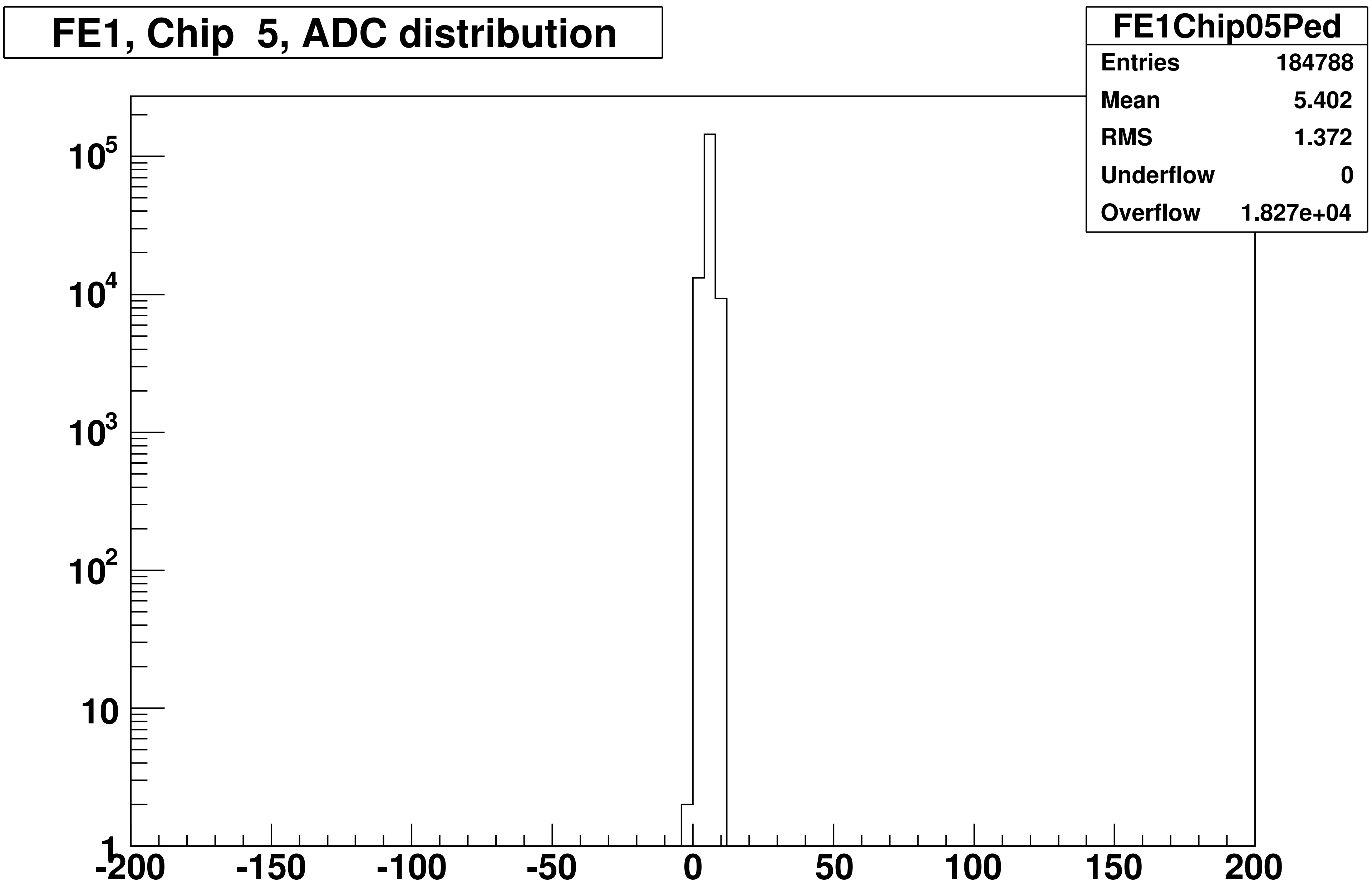
100
150
200

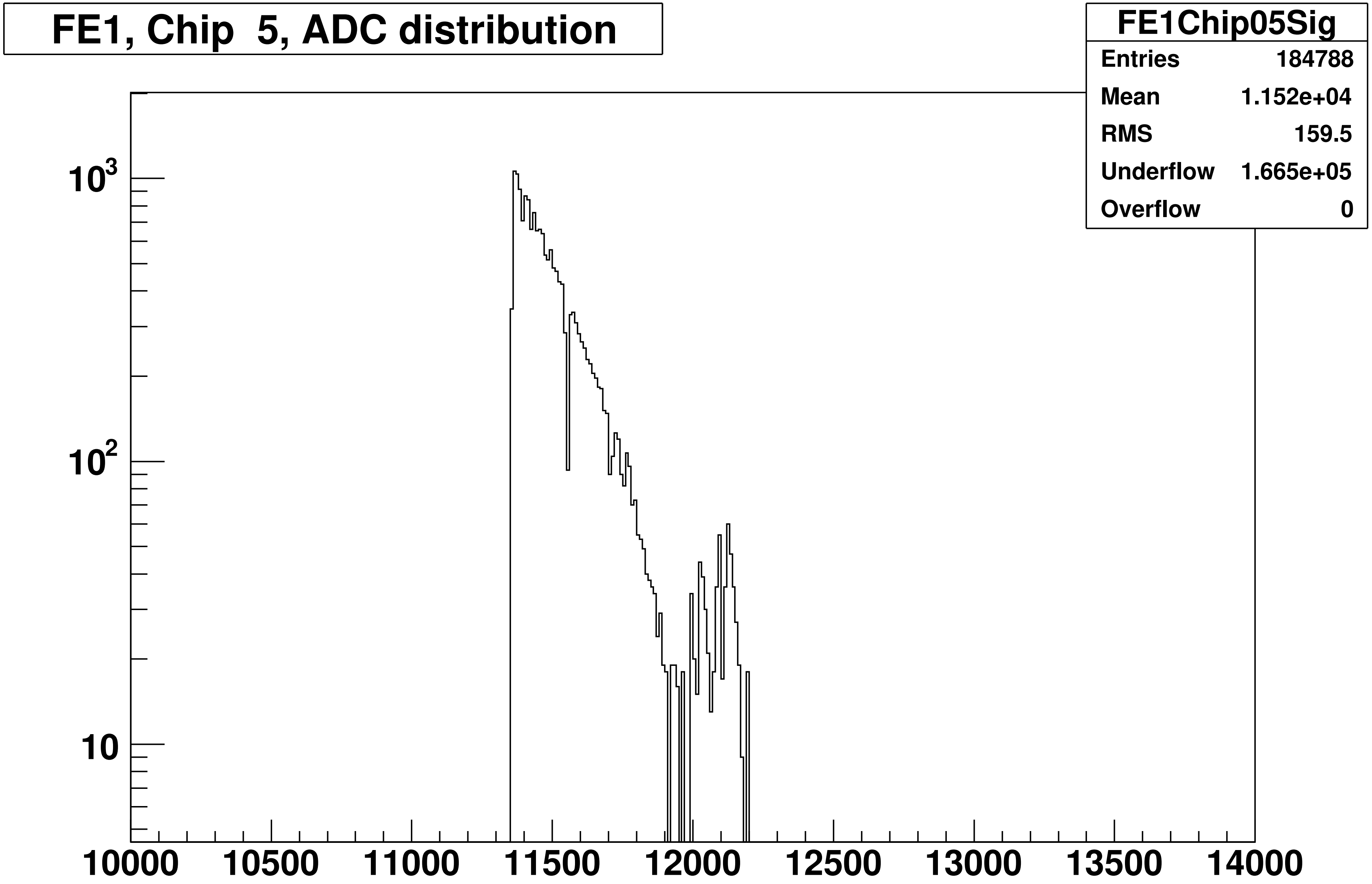

FE1, Chip 4, ADC distribution
FE1Chip04Sig
Entries 184788
Mean 1.165e+04
RMS 159.5
Underflow 1.666e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

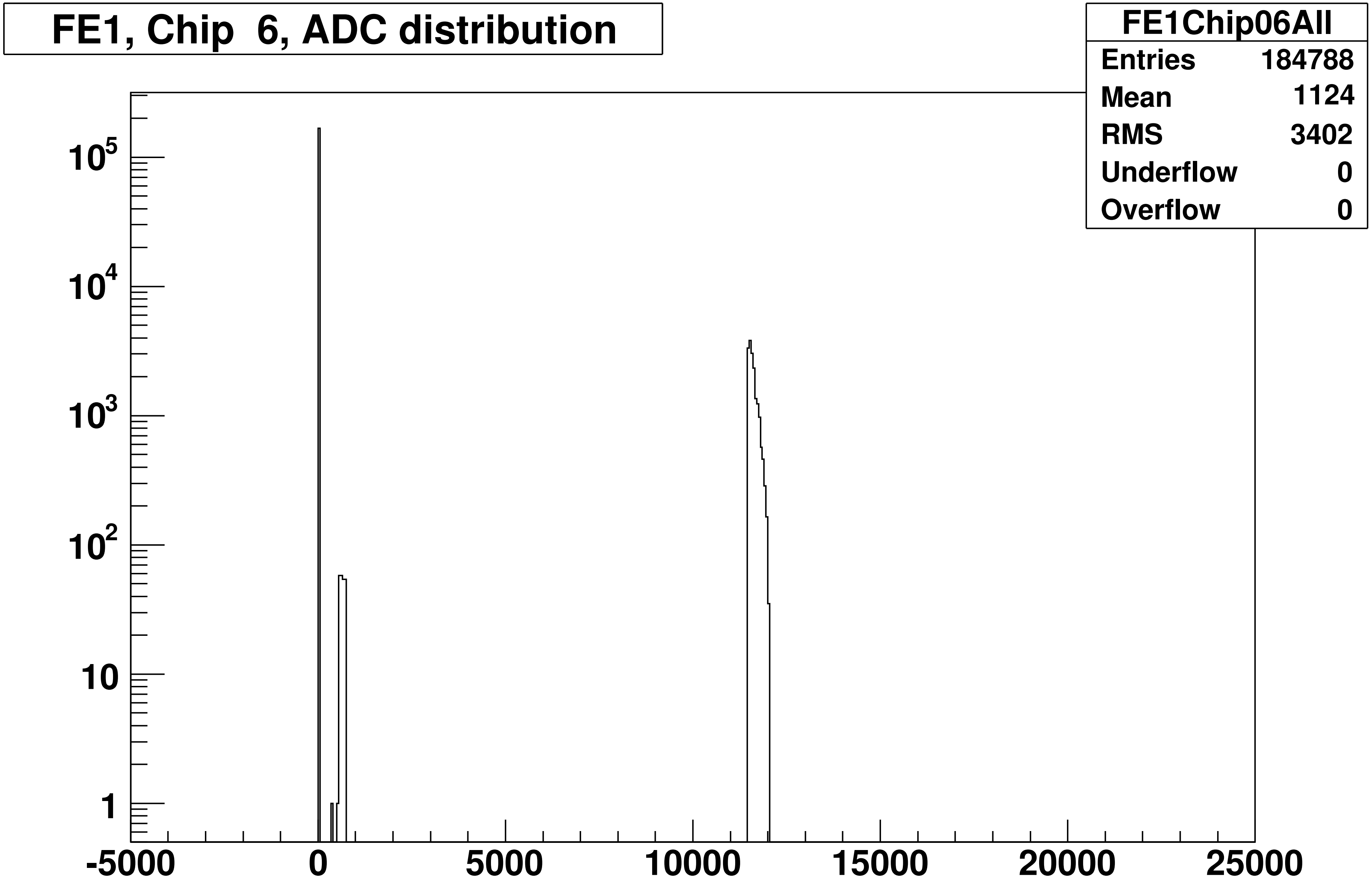


FE1, Chip 5, ADC distribution
FE1Chip05All
Entries 184788
Mean 1143
RMS 3435
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000



FE1, Chip 5, ADC distribution
FE1Chip05Ped
Entries 184788
Mean 5.402
RMS 1.372
Underflow 0
Overflow 1.827e+04
10^5
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 5, ADC distribution
FE1Chip05Sig
Entries 184788
Mean 1.152e+04
RMS 159.5
Underflow 1.665e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE1, Chip 6, ADC distribution
FE1Chip06All
Entries 184788
Mean 1124
RMS 3402
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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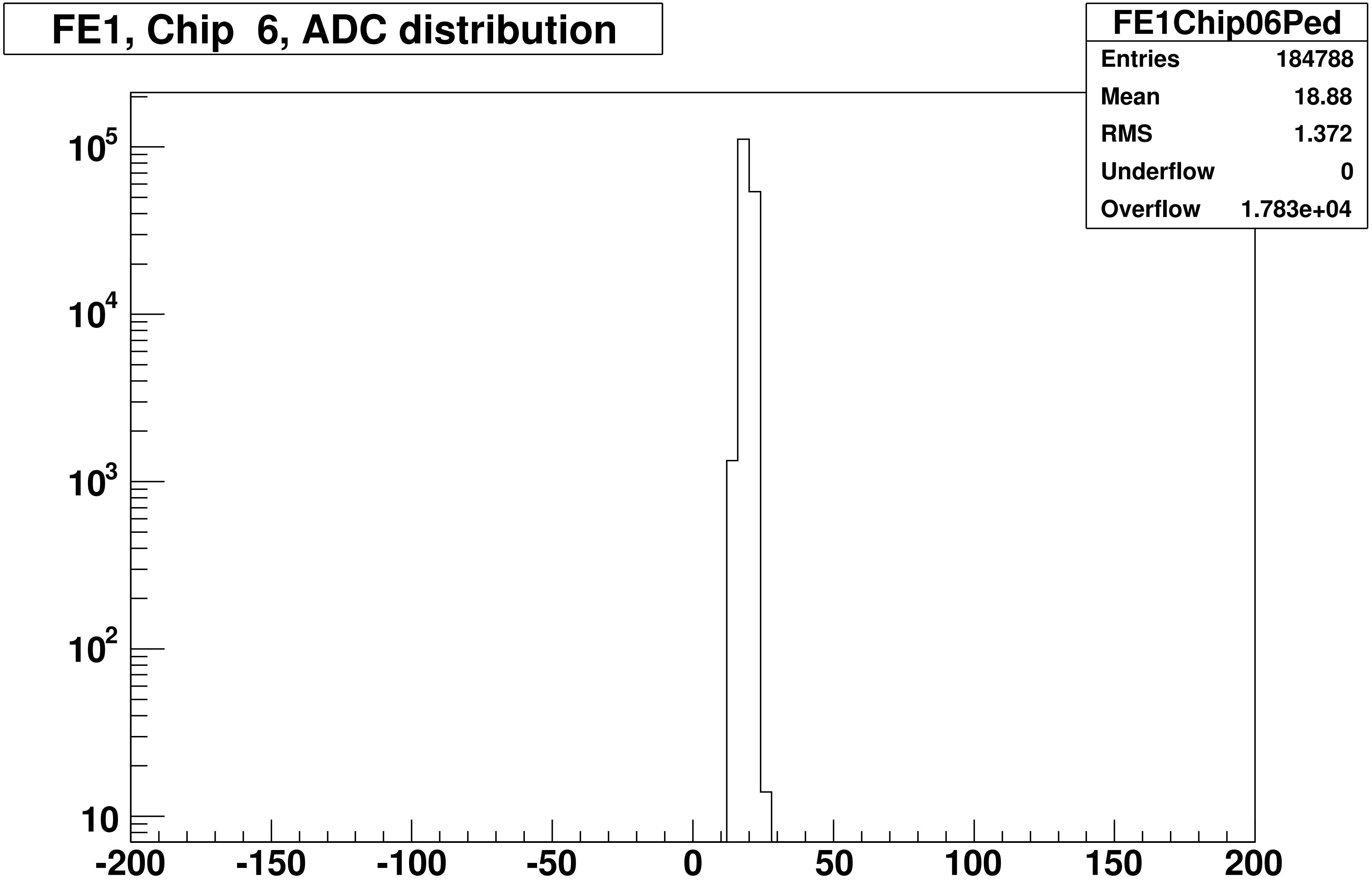
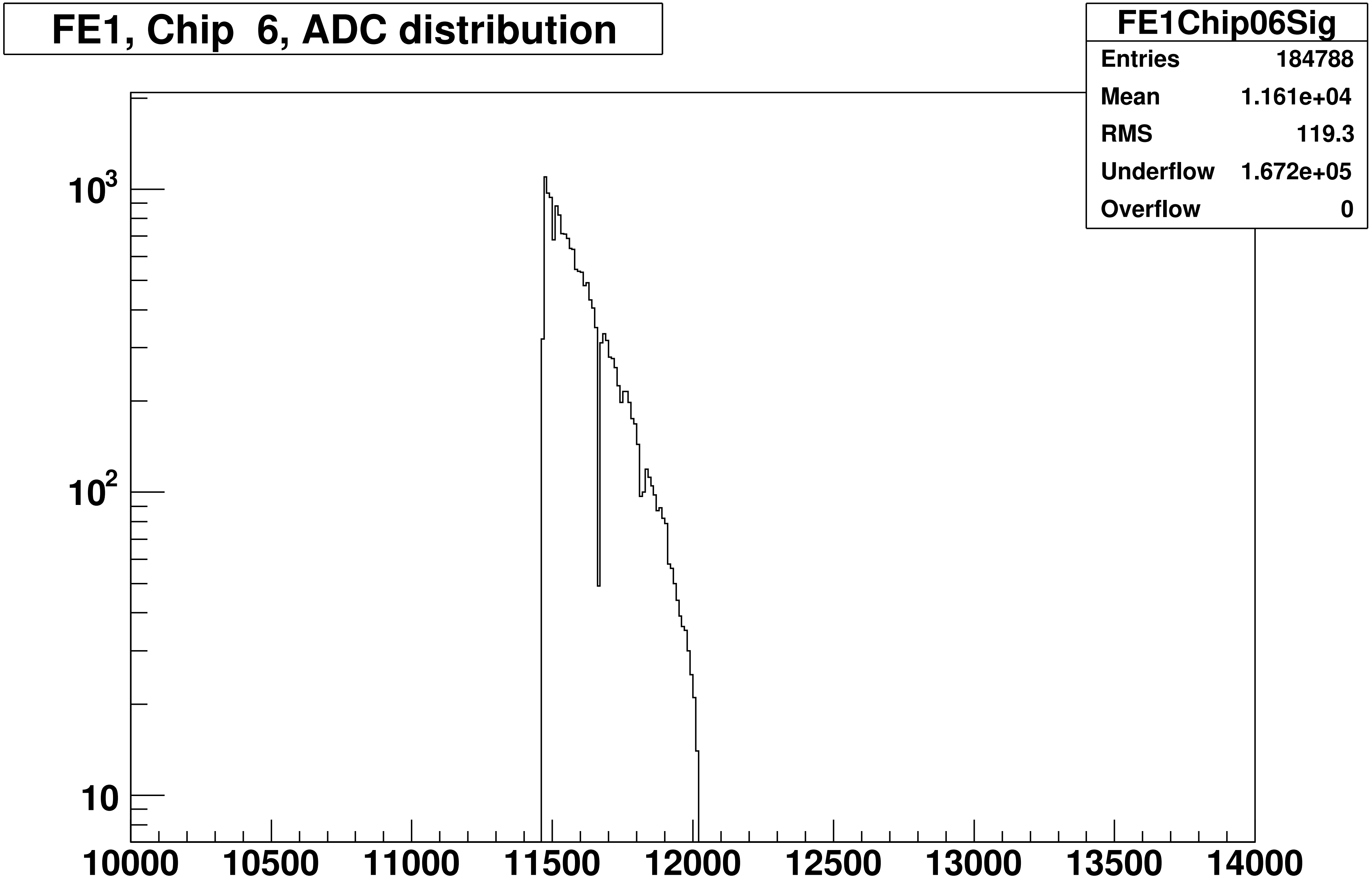
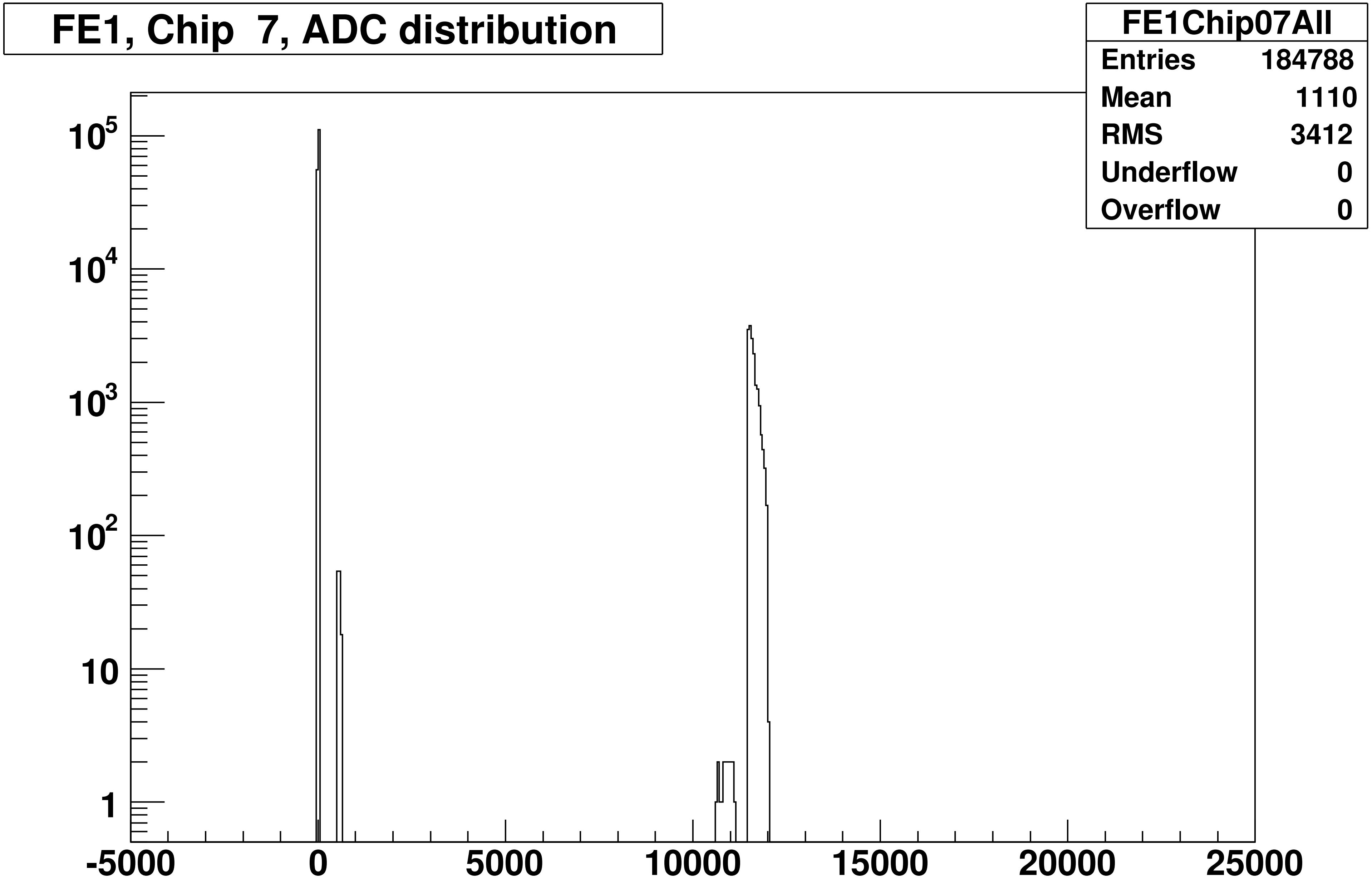
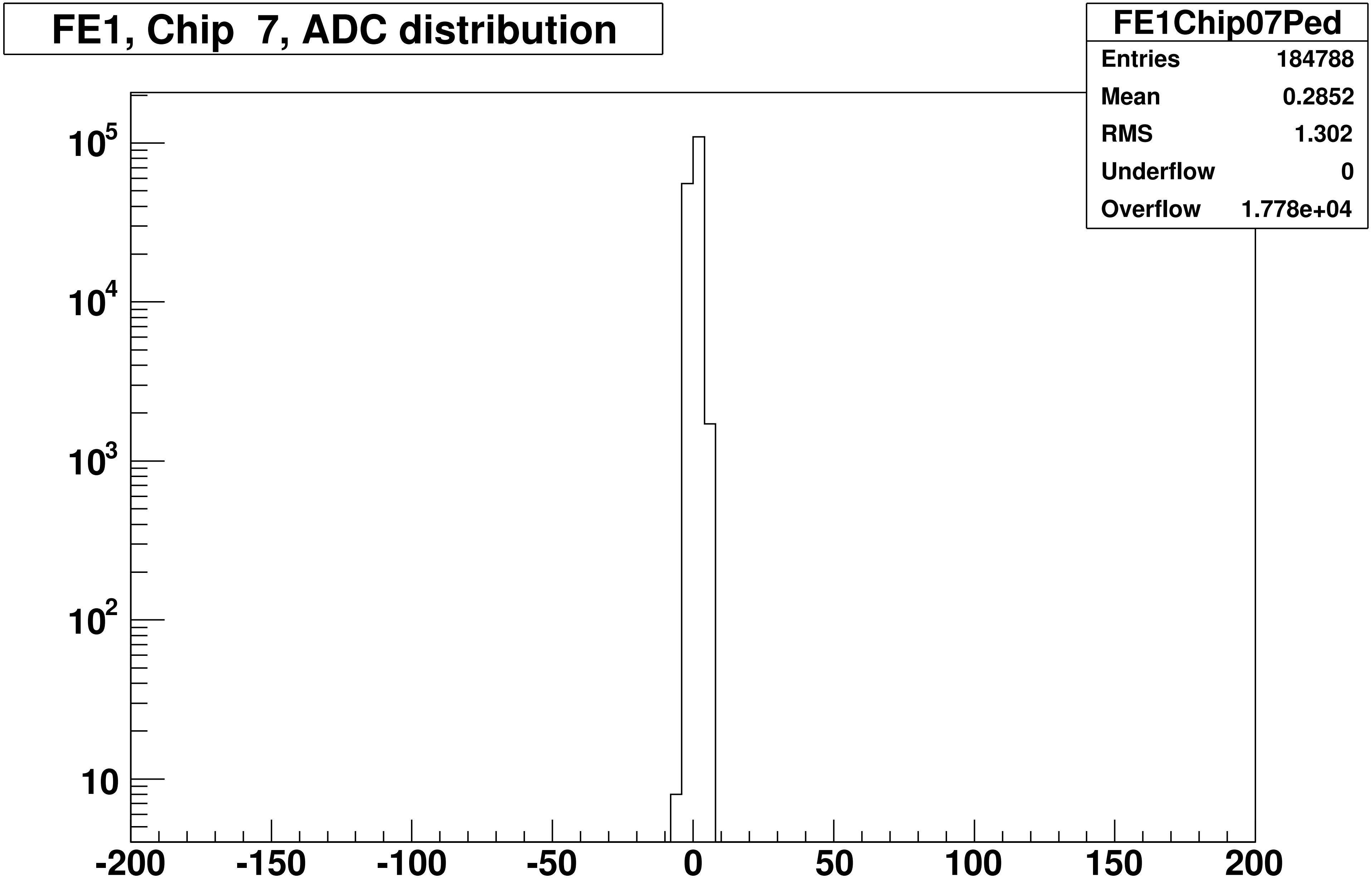
10000
15000
20000
25000


FE1, Chip 6, ADC distribution
FE1Chip06Ped
Entries 184788
Mean 18.88
RMS 1.372
Underflow 0
Overflow 1.783e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 6, ADC distribution
FE1Chip06Sig
Entries 184788
Mean 1.161e+04
RMS 119.3
Underflow 1.672e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE1, Chip 7, ADC distribution
FE1Chip07All
Entries 184788
Mean 1110
RMS 3412
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 7, ADC distribution
FE1Chip07Ped
Entries 184788
Mean 0.2852
RMS 1.302
Underflow 0
Overflow 1.778e+04
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10^4
10^3
10^2
10
-200
-150
-100
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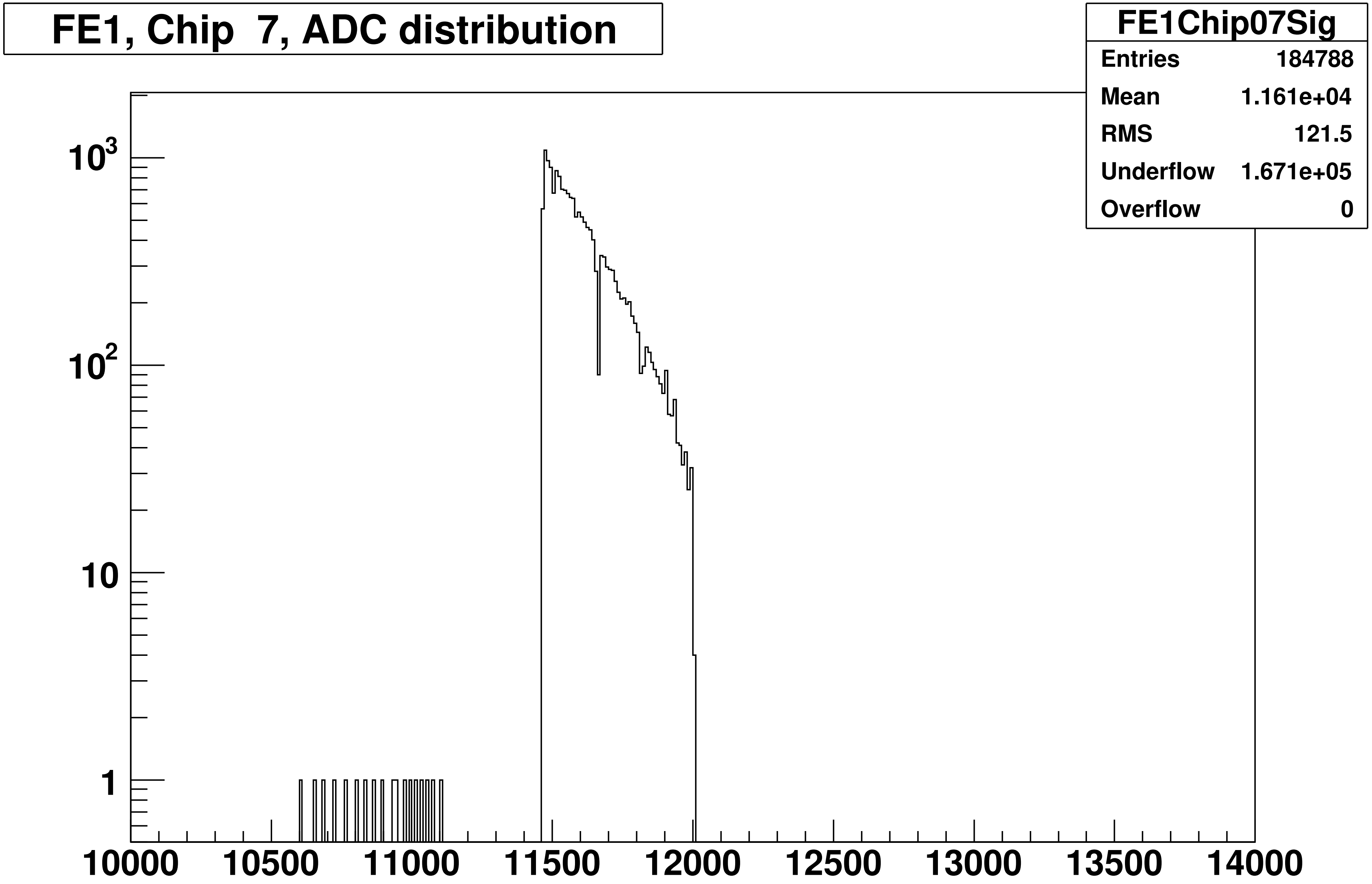
100
150
200


FE1, Chip 7, ADC distribution
FE1Chip07Sig
Entries 184788
Mean 1.161e+04
RMS 121.5
Underflow 1.671e+05
Overflow 0
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10^2
10
1
10000
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11500
12000
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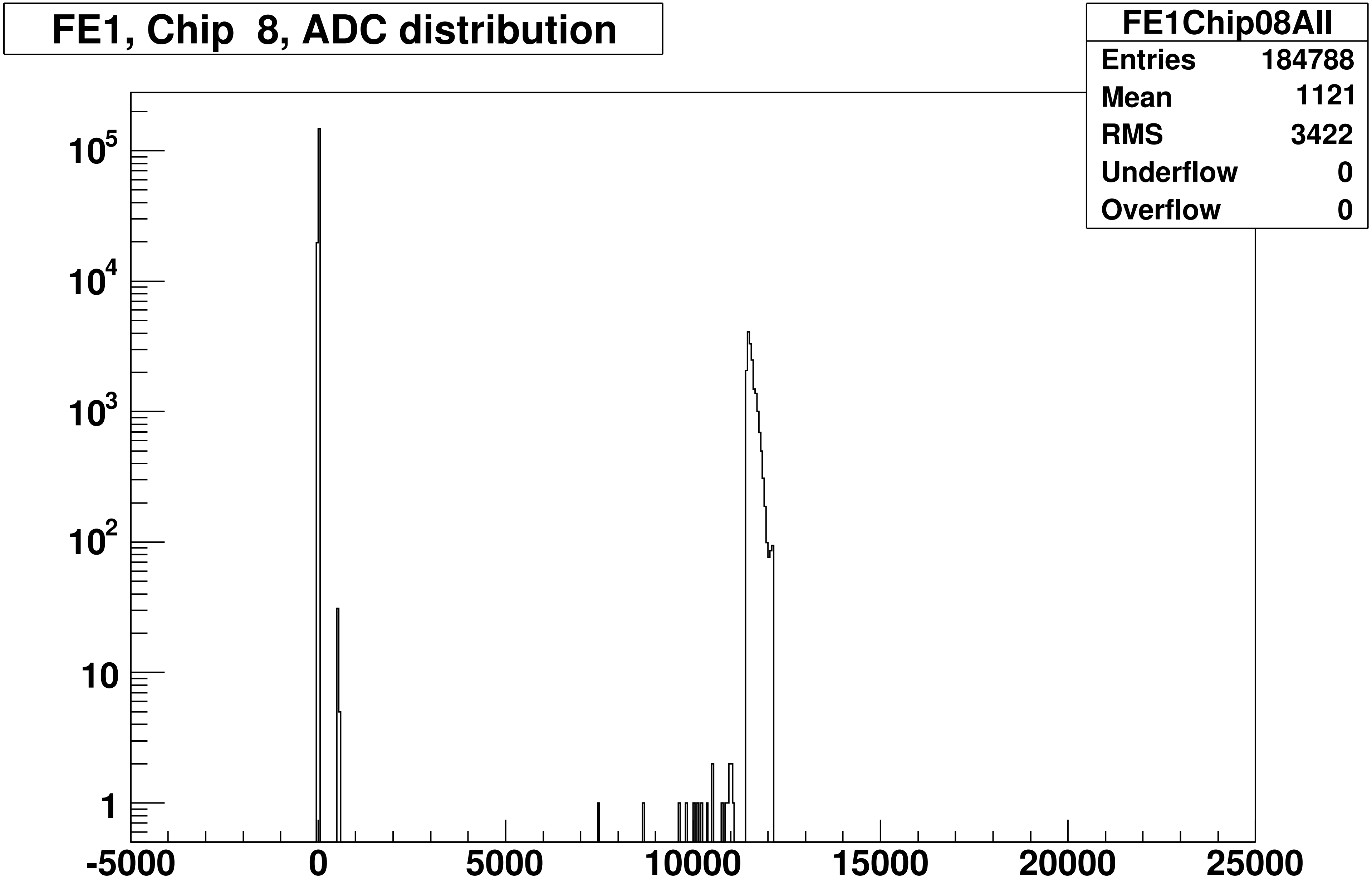

FE1, Chip 8, ADC distribution
FE1Chip08All
Entries 184788
Mean 1121
RMS 3422
Underflow 0
Overflow 0
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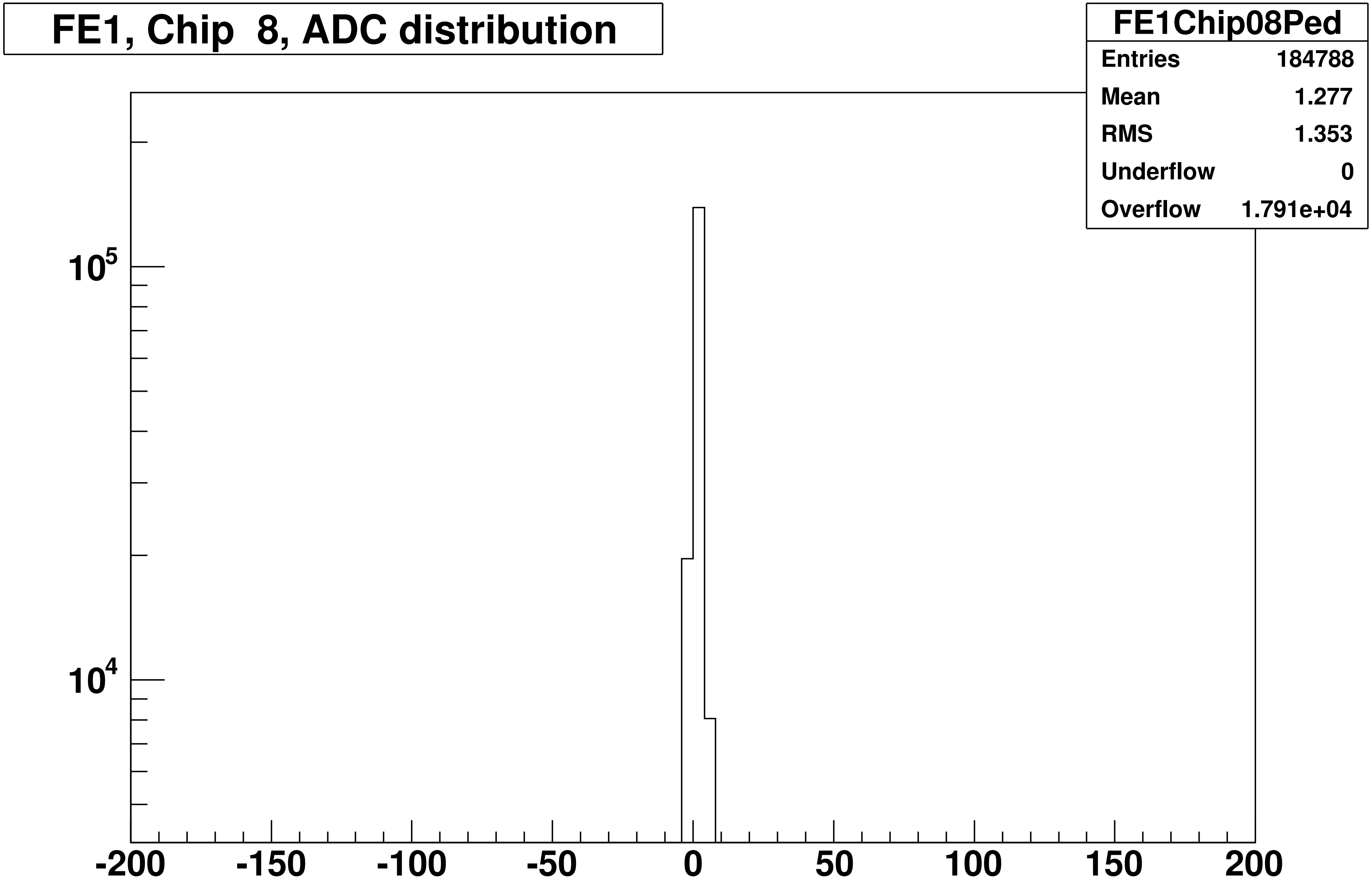
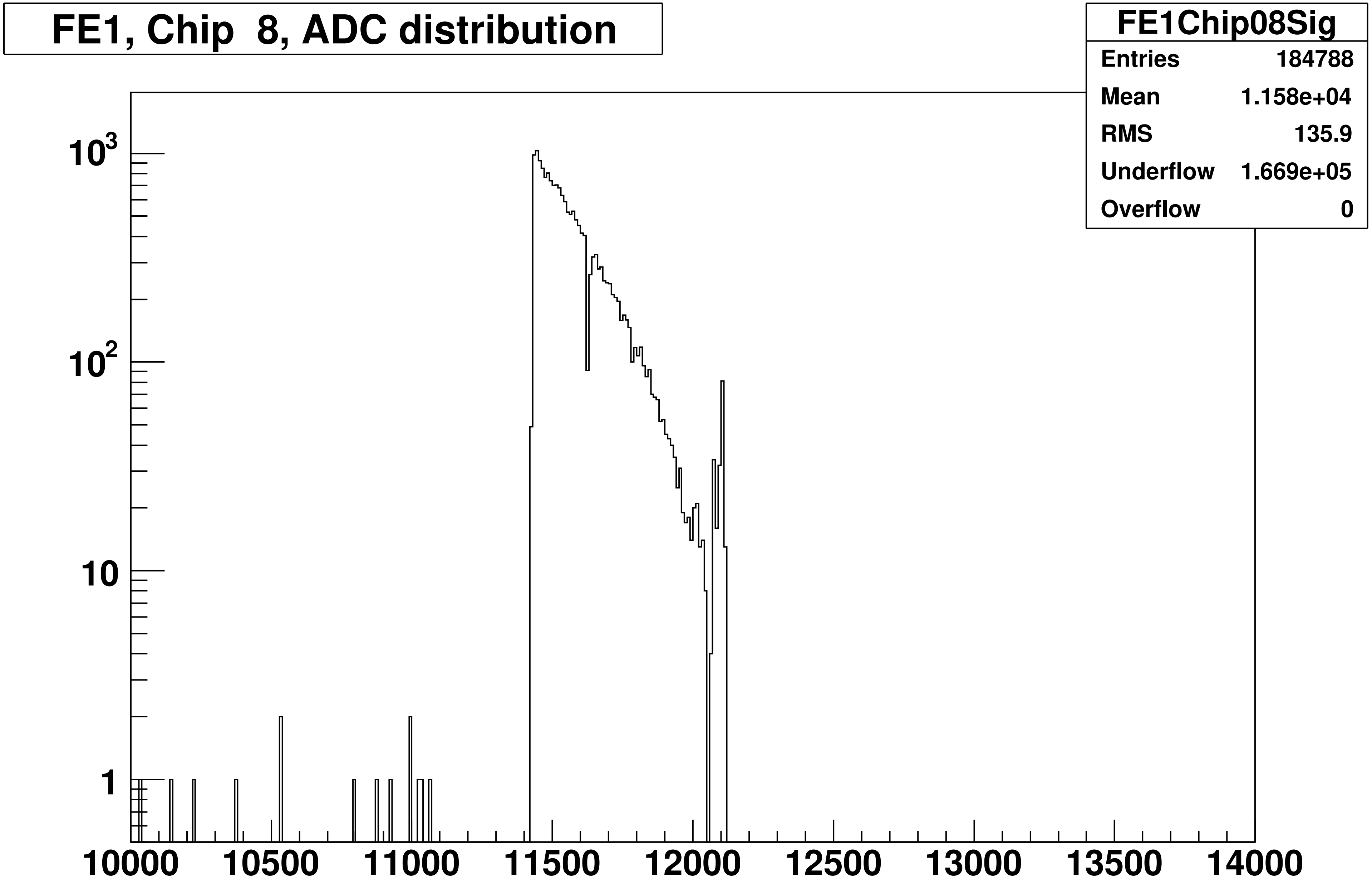
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 8, ADC distribution
FE1Chip08Ped
Entries 184788
Mean 1.277
RMS 1.353
Underflow 0
Overflow 1.791e+04
10^5
10^4
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 8, ADC distribution
FE1Chip08Sig
Entries 184788
Mean 1.158e+04
RMS 135.9
Underflow 1.669e+05
Overflow 0
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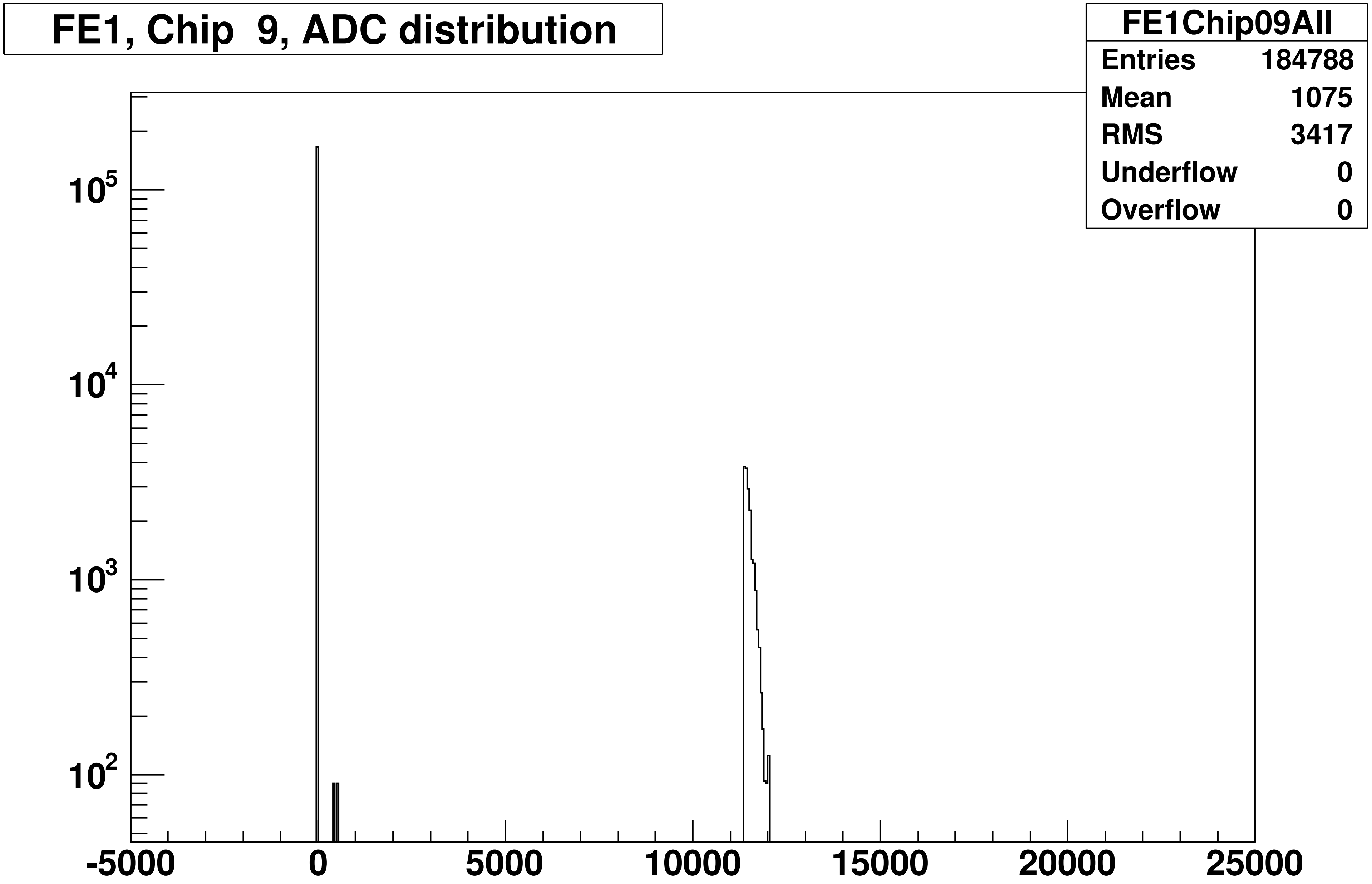
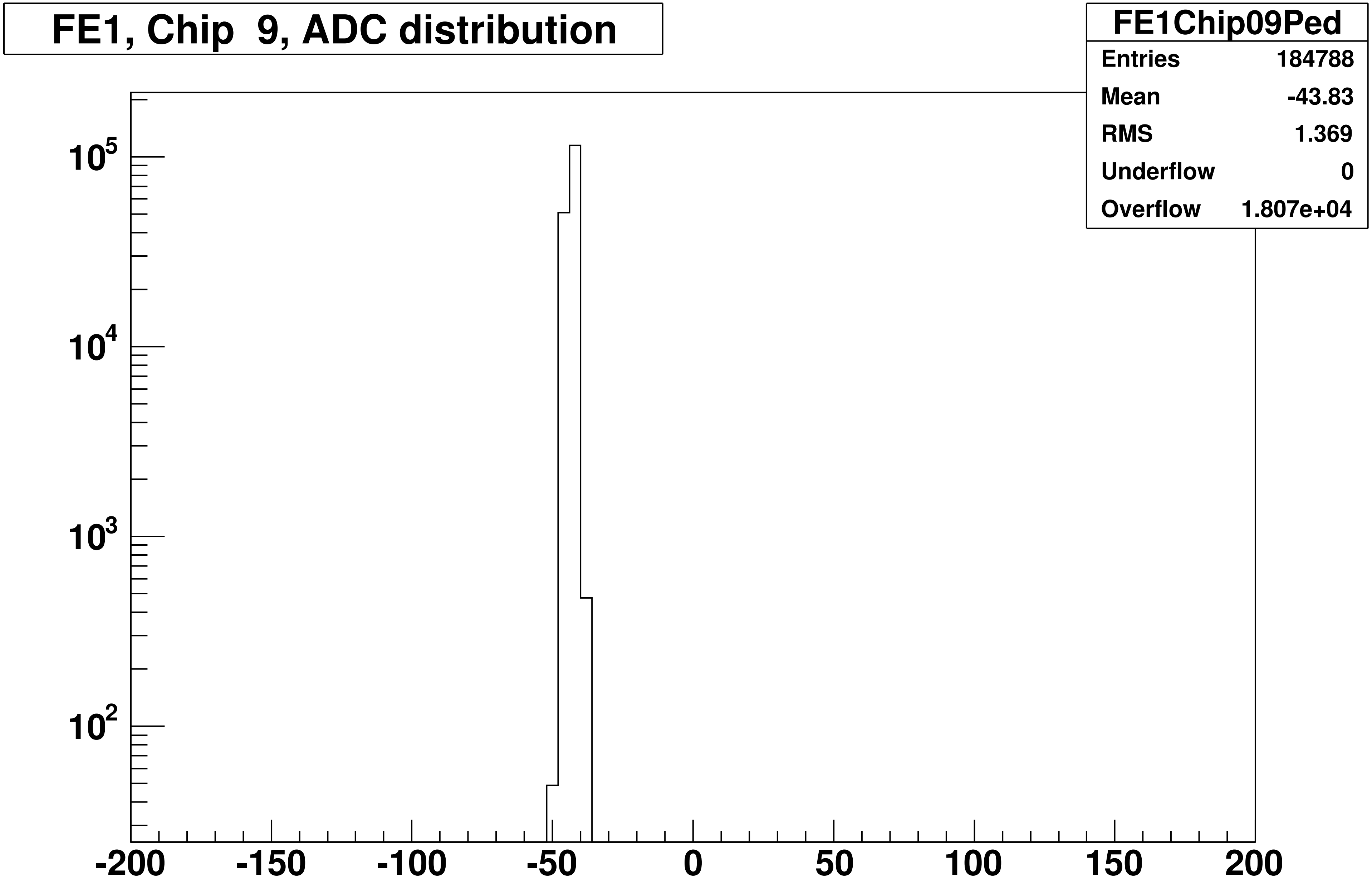
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE1, Chip 9, ADC distribution
FE1Chip09All
Entries 184788
Mean 1075
RMS 3417
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 9, ADC distribution
FE1Chip09Ped
Entries 184788
Mean -43.83
RMS 1.369
Underflow 0
Overflow 1.807e+04
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10^4
10^3
10^2
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-100
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0
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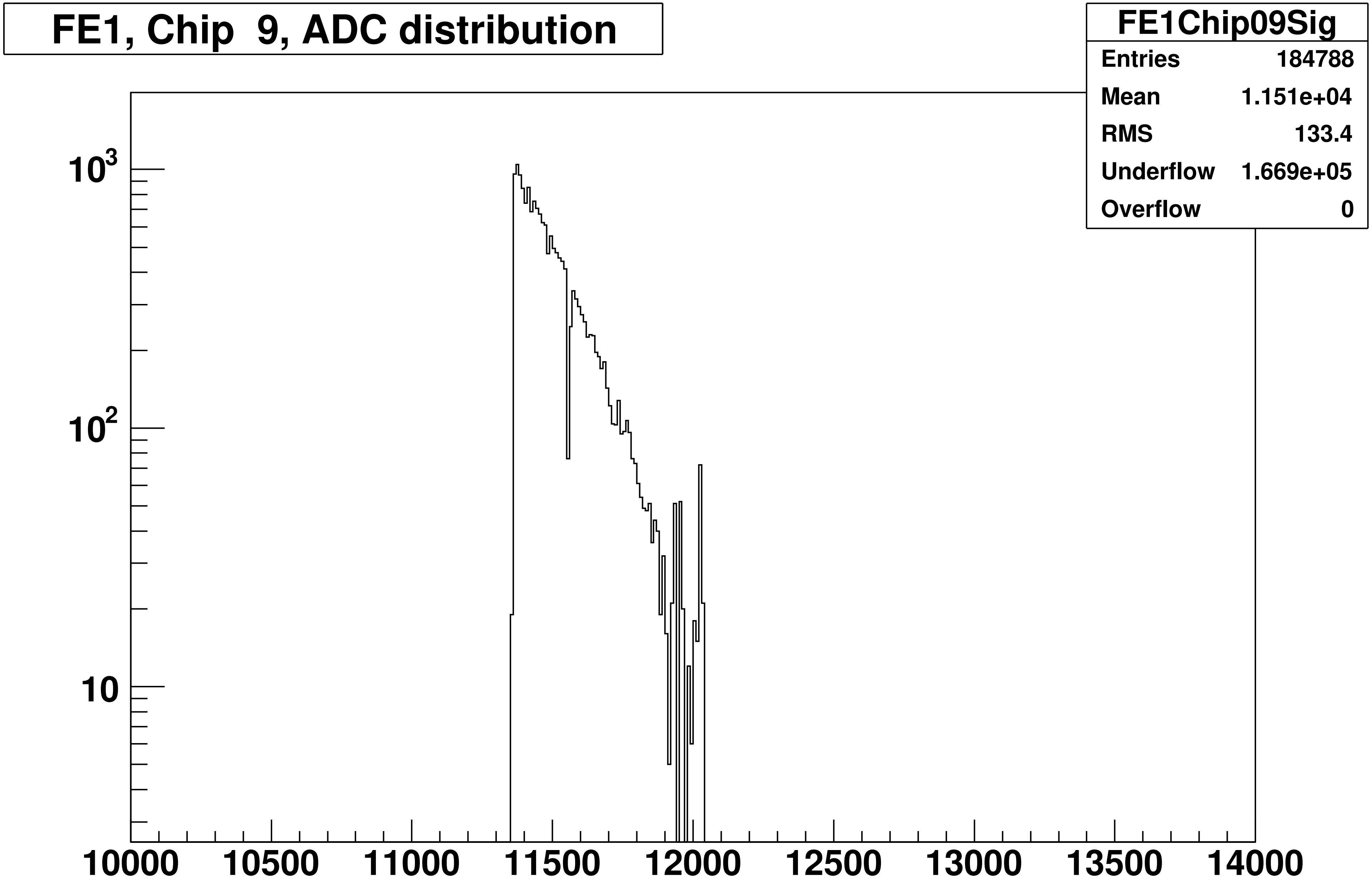
100
150
200



FE1, Chip 9, ADC distribution
FE1Chip09Sig
Entries 184788
Mean 1.151e+04
RMS 133.4
Underflow 1.669e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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13500
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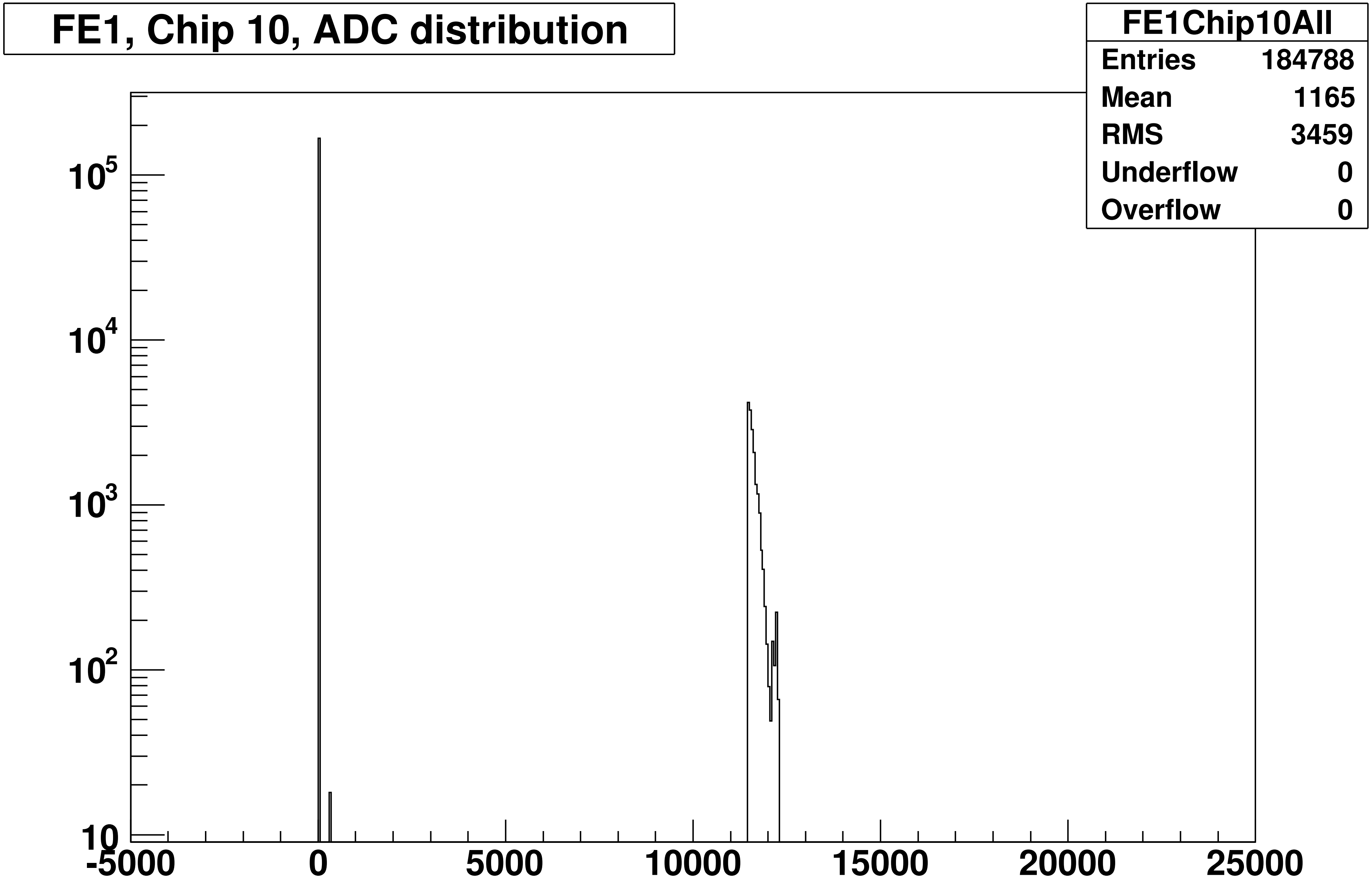
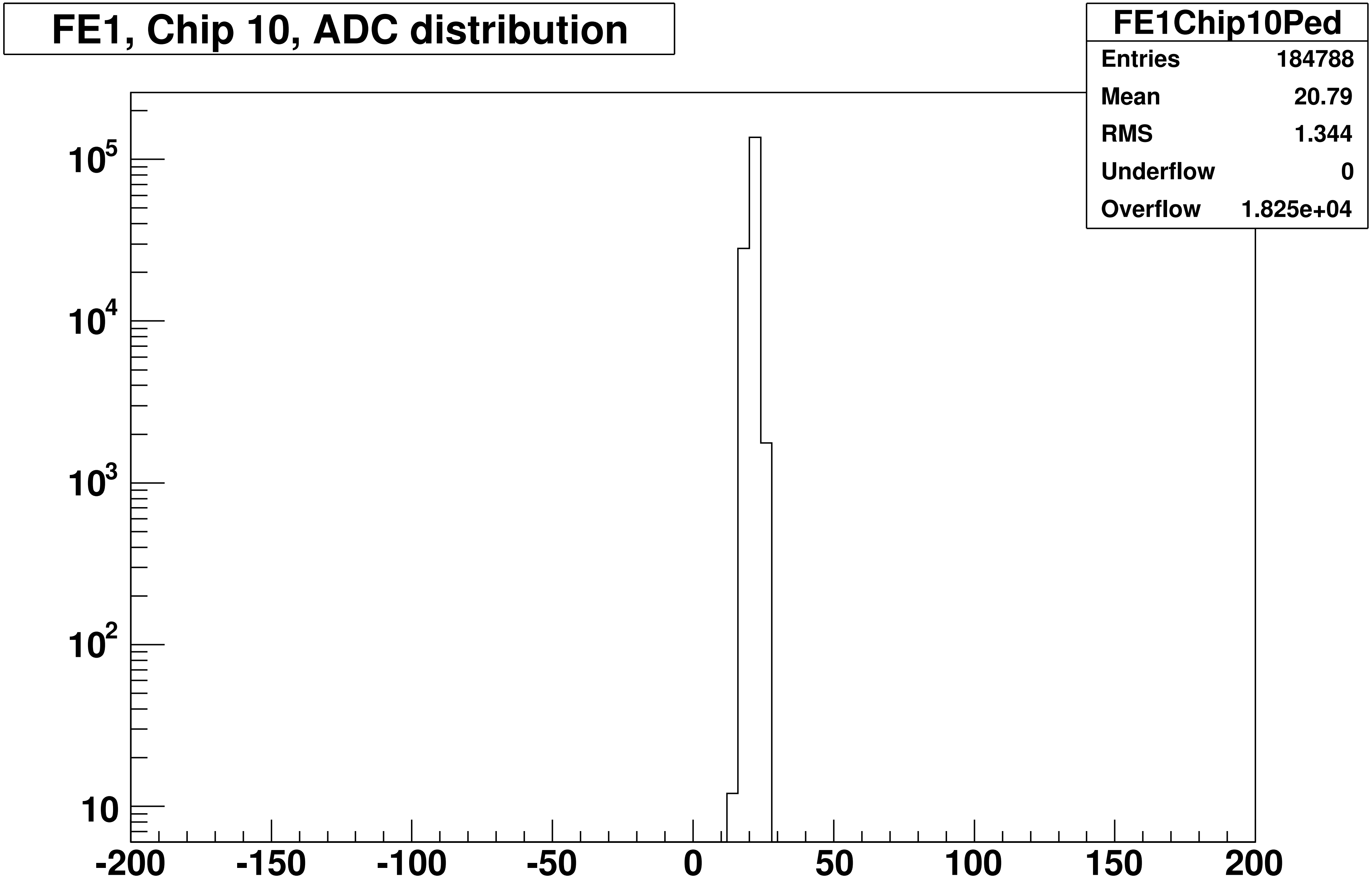

FE1, Chip 10, ADC distribution
FE1Chip10All
Entries 184788
Mean 1165
RMS 3459
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 10, ADC distribution
FE1Chip10Ped
Entries 184788
Mean 20.79
RMS 1.344
Underflow 0
Overflow 1.825e+04
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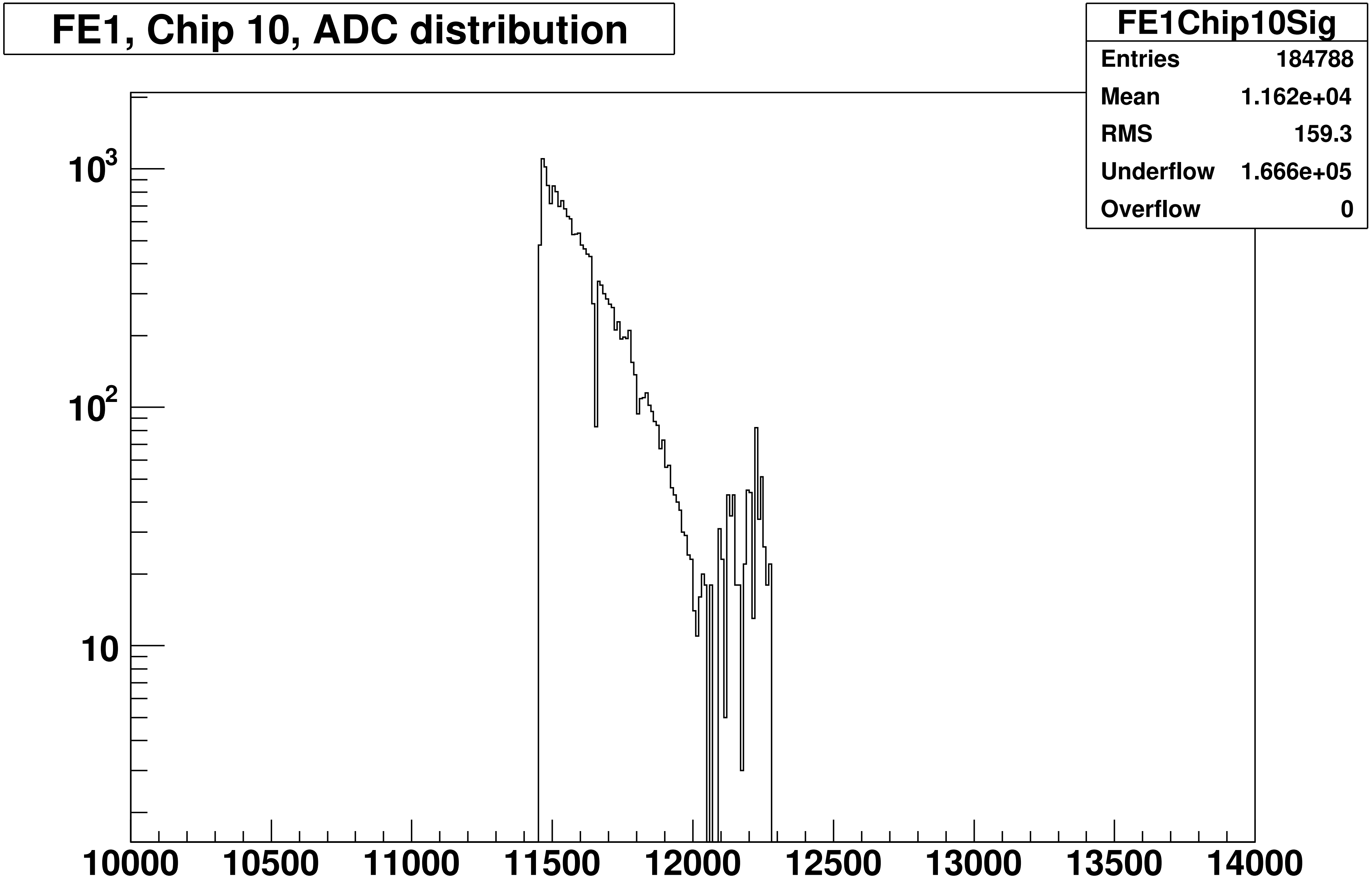
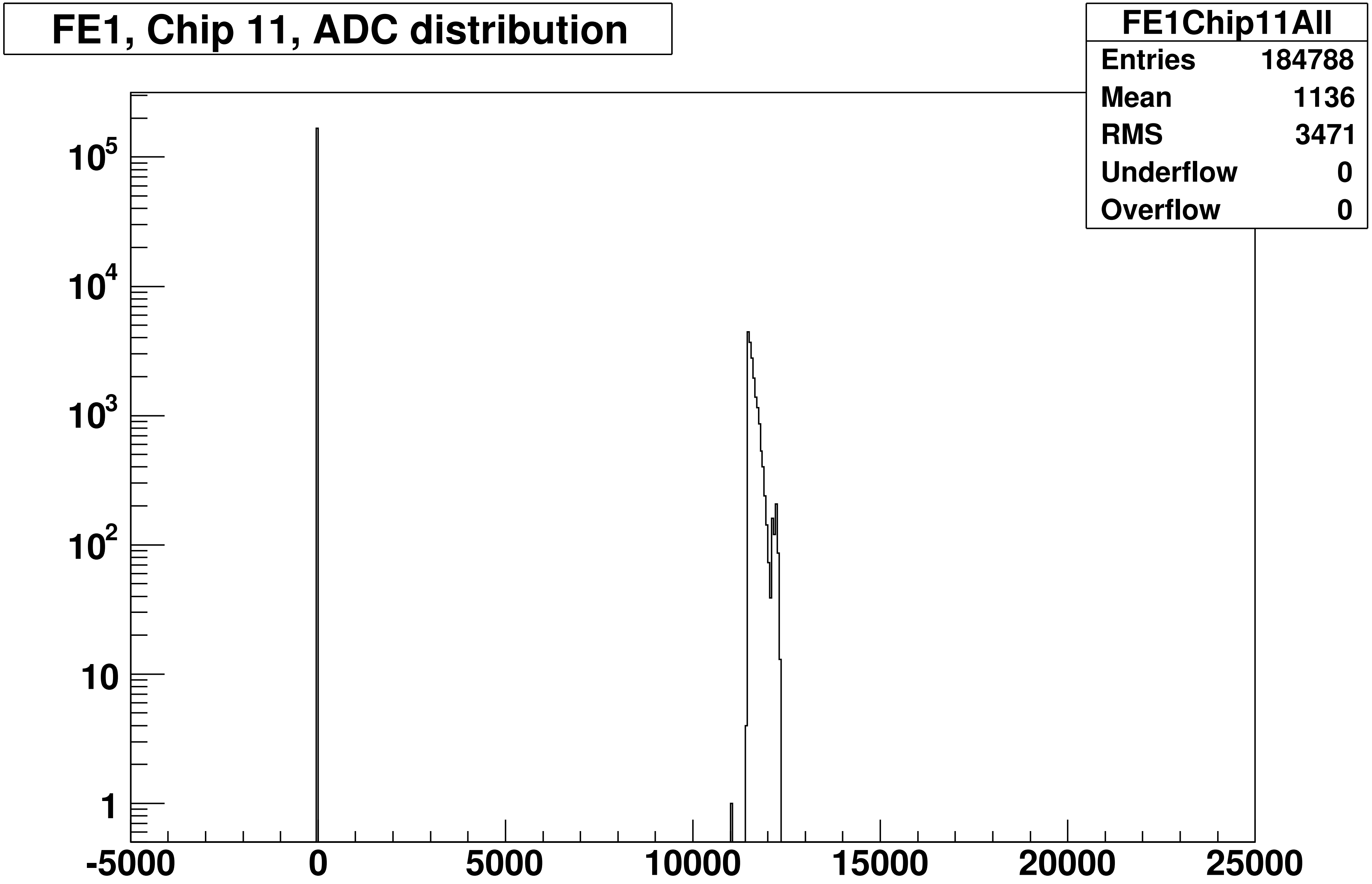
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE1, Chip 10, ADC distribution
FE1Chip10Sig
Entries 184788
Mean 1.162e+04
RMS 159.3
Underflow 1.666e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE1, Chip 11, ADC distribution
FE1Chip11All
Entries 184788
Mean 1136
RMS 3471
Underflow 0
Overflow 0
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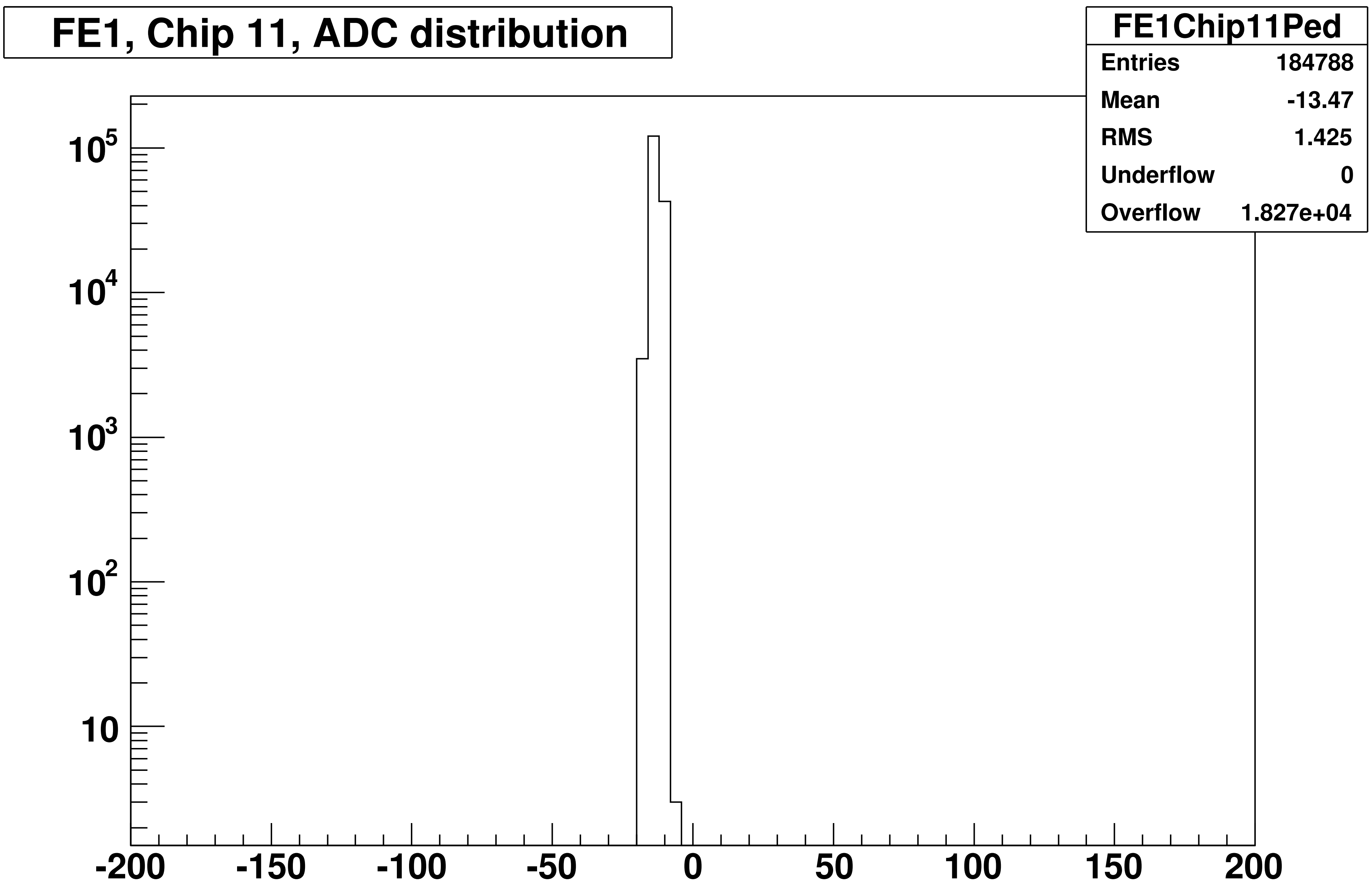
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE1, Chip 11, ADC distribution
FE1Chip11Ped
Entries 184788
Mean -13.47
RMS 1.425
Underflow 0
Overflow 1.827e+04
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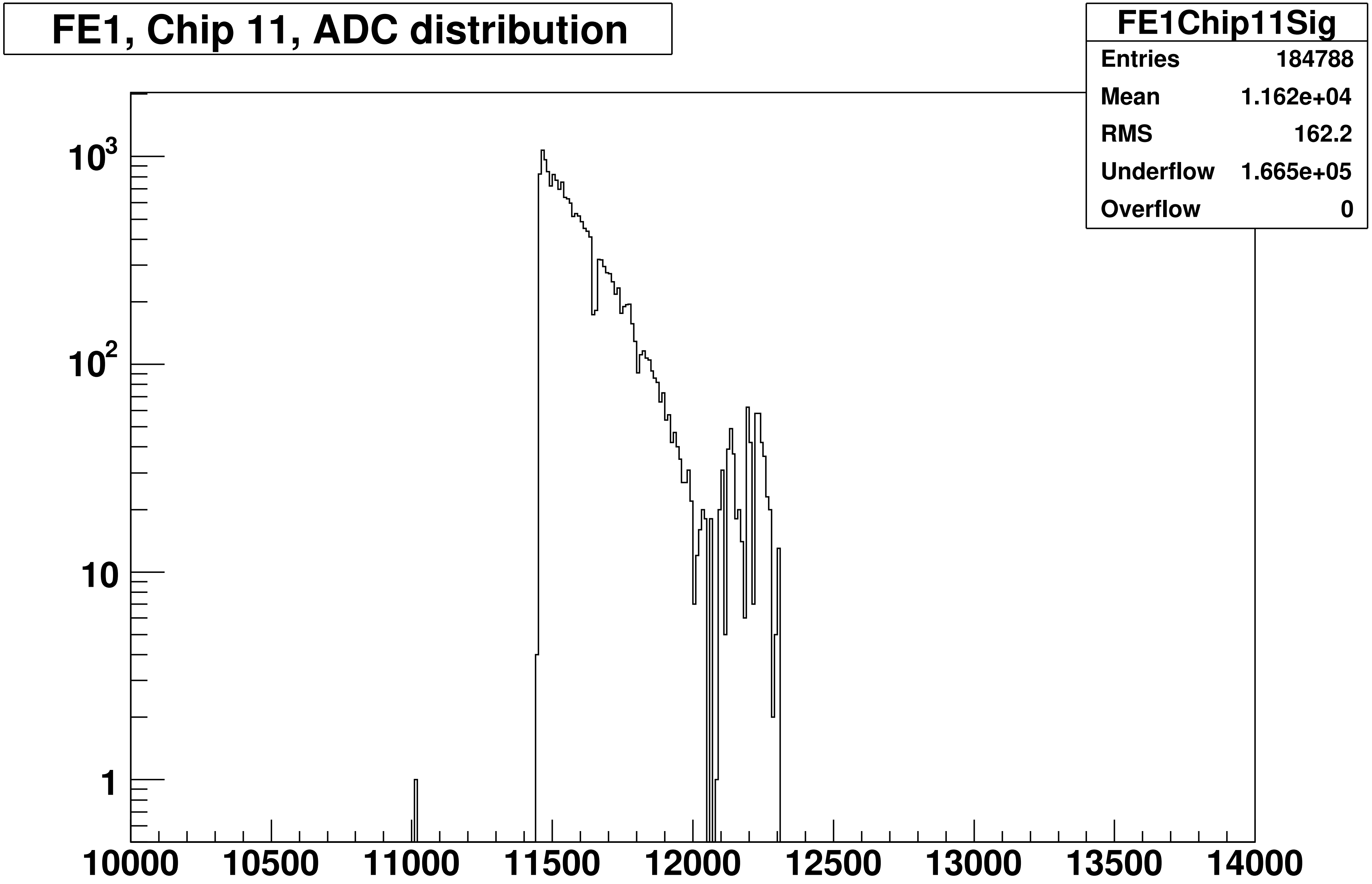
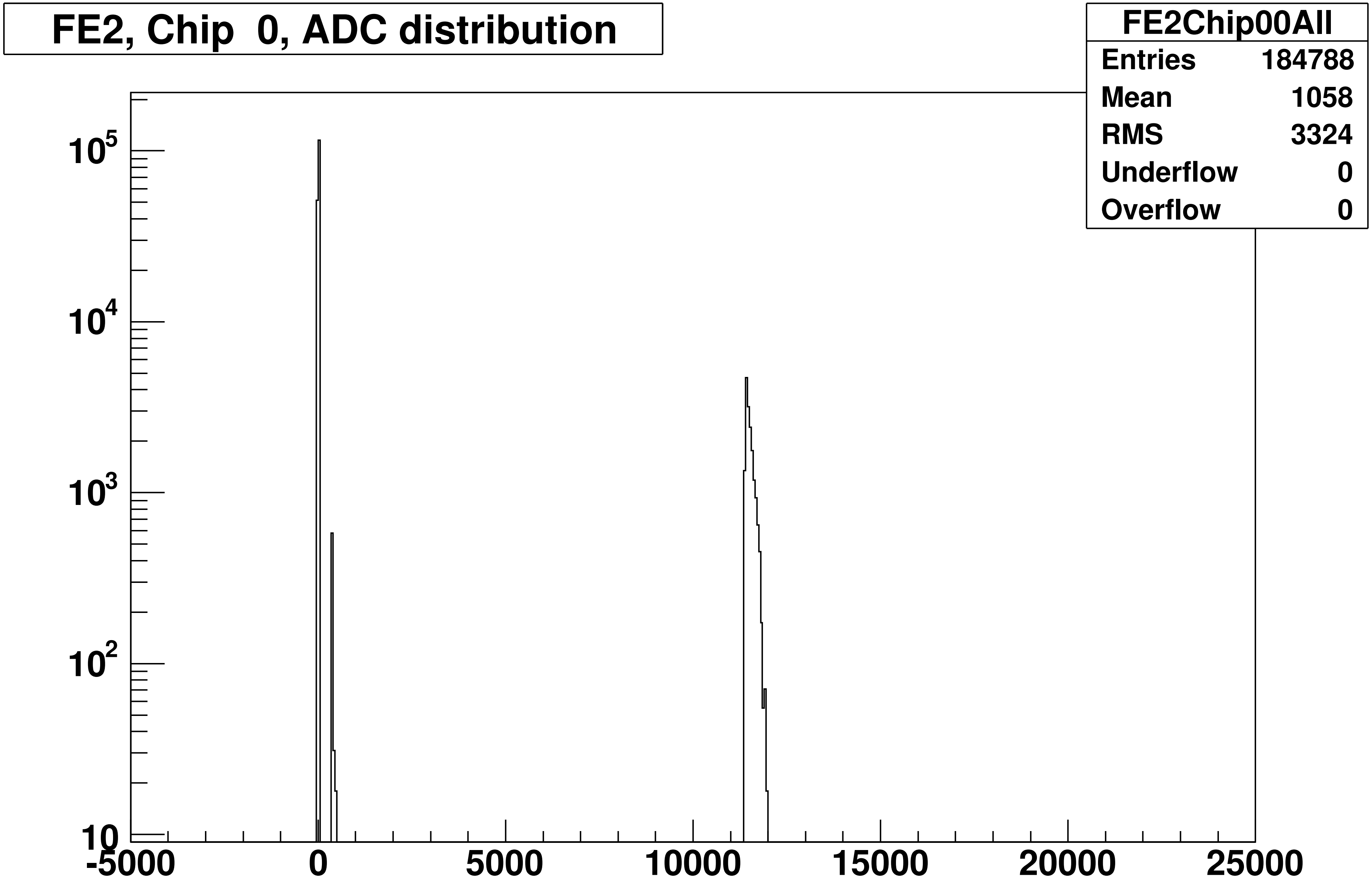
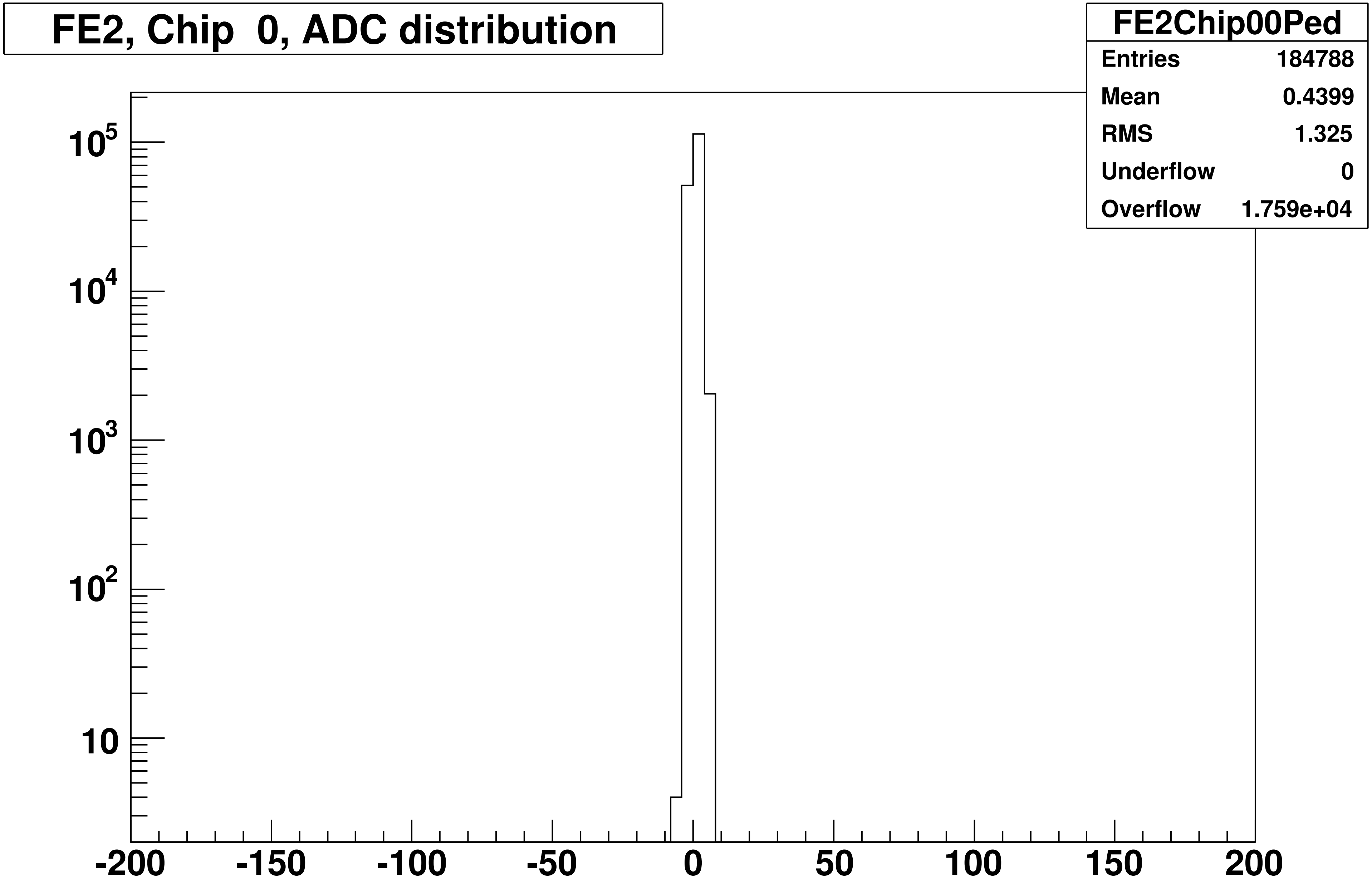
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE1, Chip 11, ADC distribution
FE1Chip11Sig
Entries 184788
Mean 1.162e+04
RMS 162.2
Underflow 1.665e+05
Overflow 0
10³
10²
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE2, Chip 0, ADC distribution
FE2Chip00All
Entries 184788
Mean 1058
RMS 3324
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 0, ADC distribution
FE2Chip00Ped
Entries 184788
Mean 0.4399
RMS 1.325
Underflow 0
Overflow 1.759e+04
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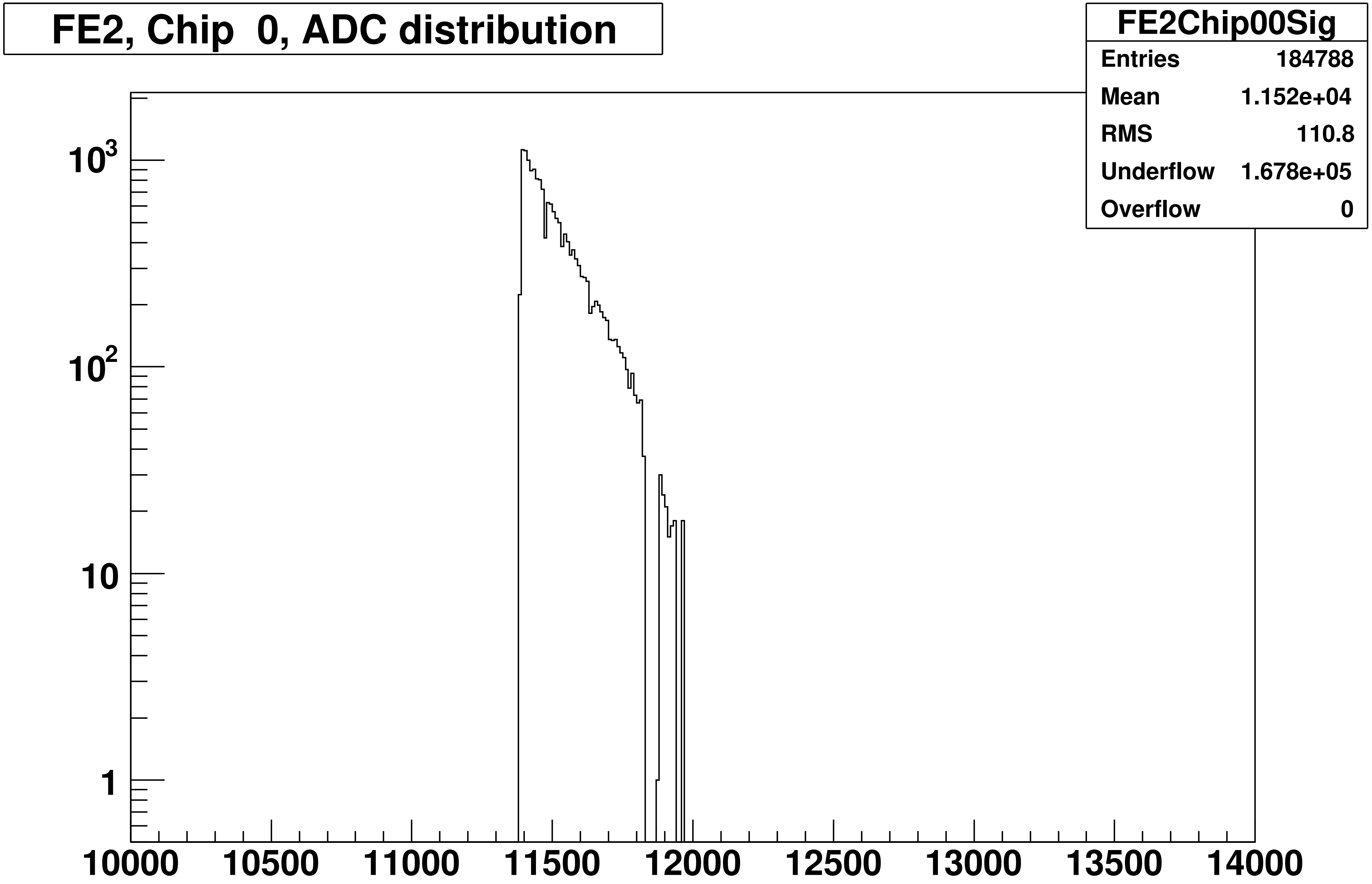
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 0, ADC distribution
FE2Chip00Sig
Entries 184788
Mean 1.152e+04
RMS 110.8
Underflow 1.678e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
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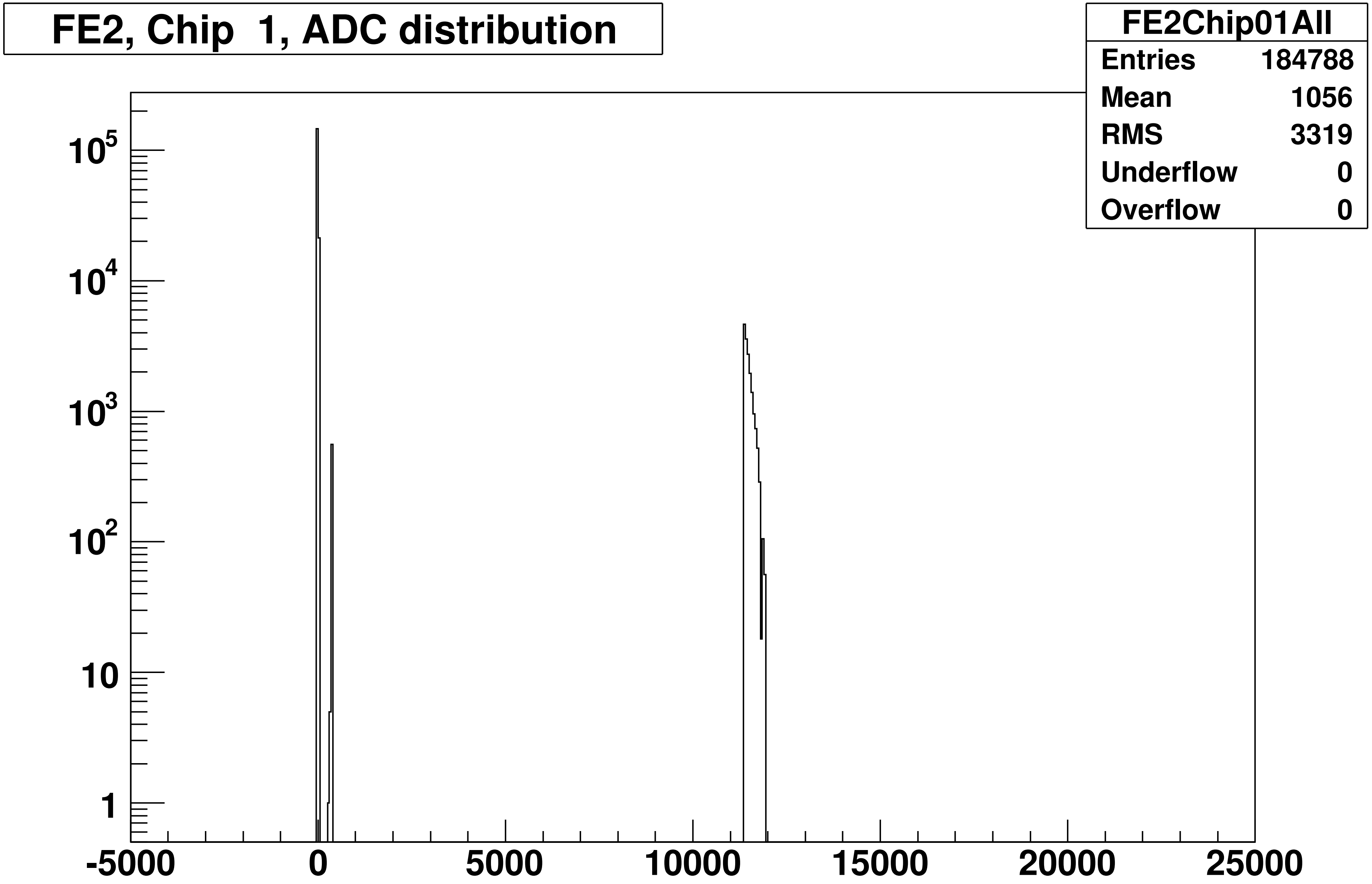
13500
14000



FE2, Chip 1, ADC distribution
FE2Chip01All
Entries 184788
Mean 1056
RMS 3319
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
5000
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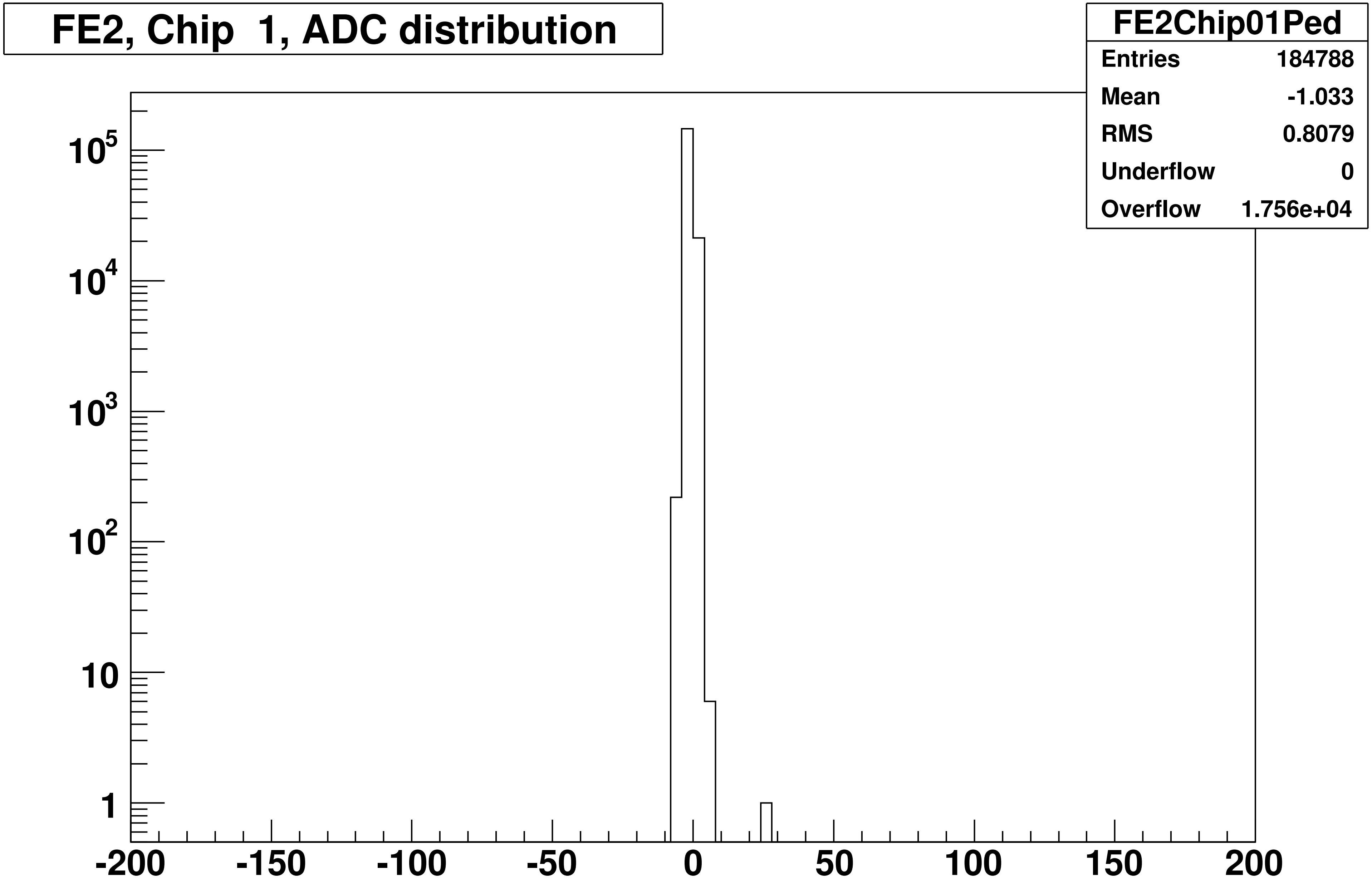
15000
20000
25000


FE2, Chip 1, ADC distribution
FE2Chip01Ped
Entries 184788
Mean -1.033
RMS 0.8079
Underflow 0
Overflow 1.756e+04
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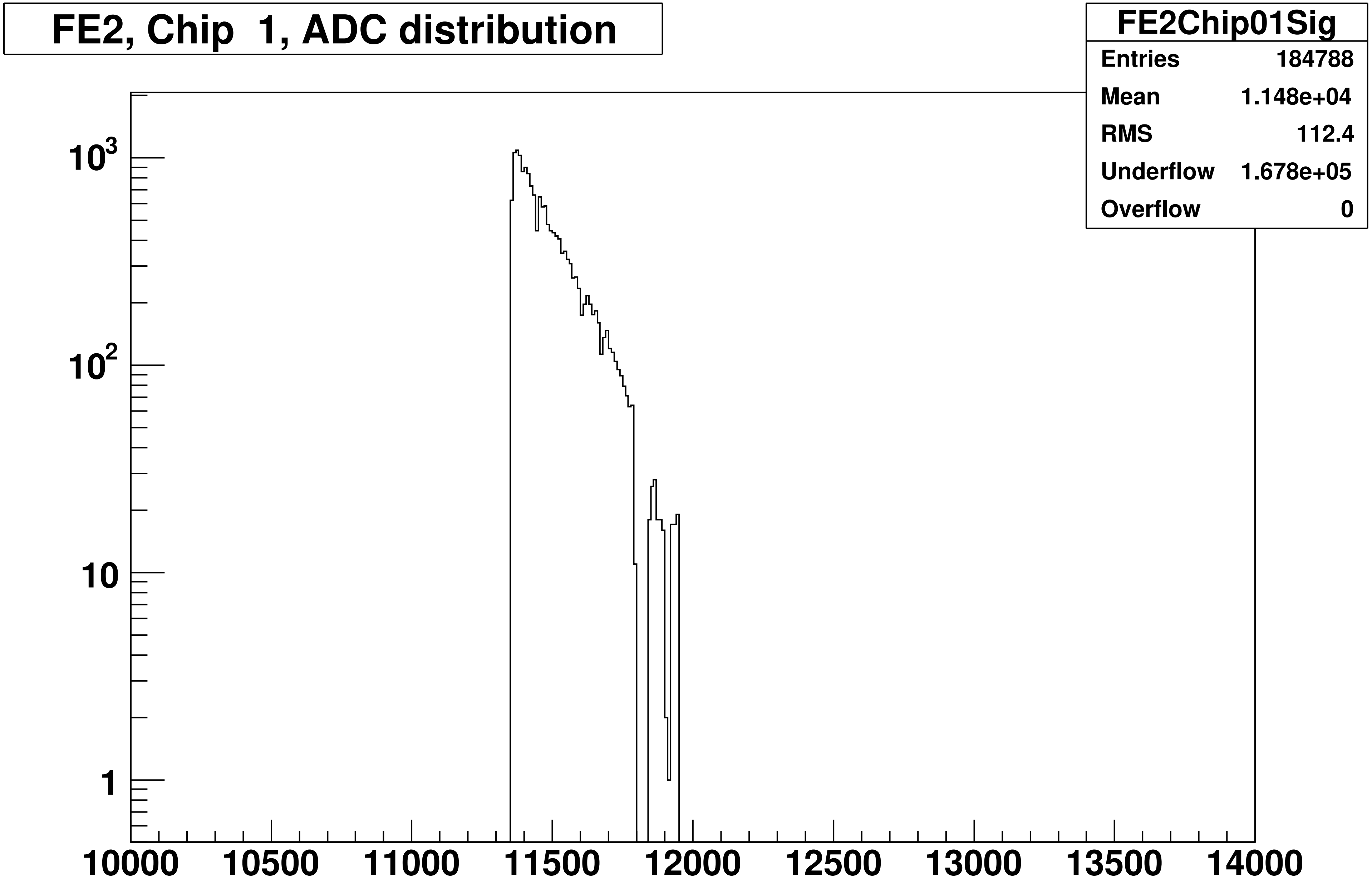
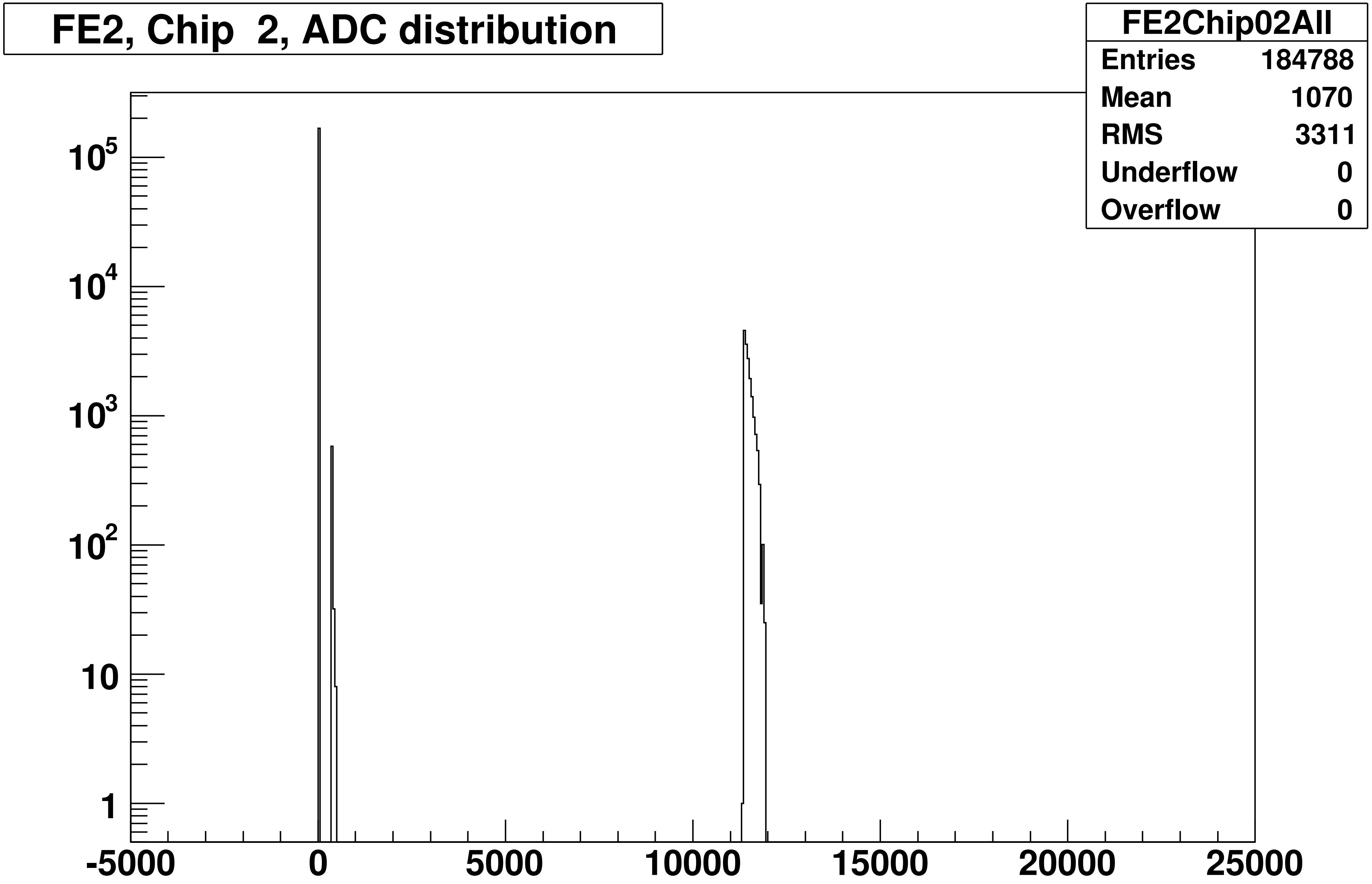
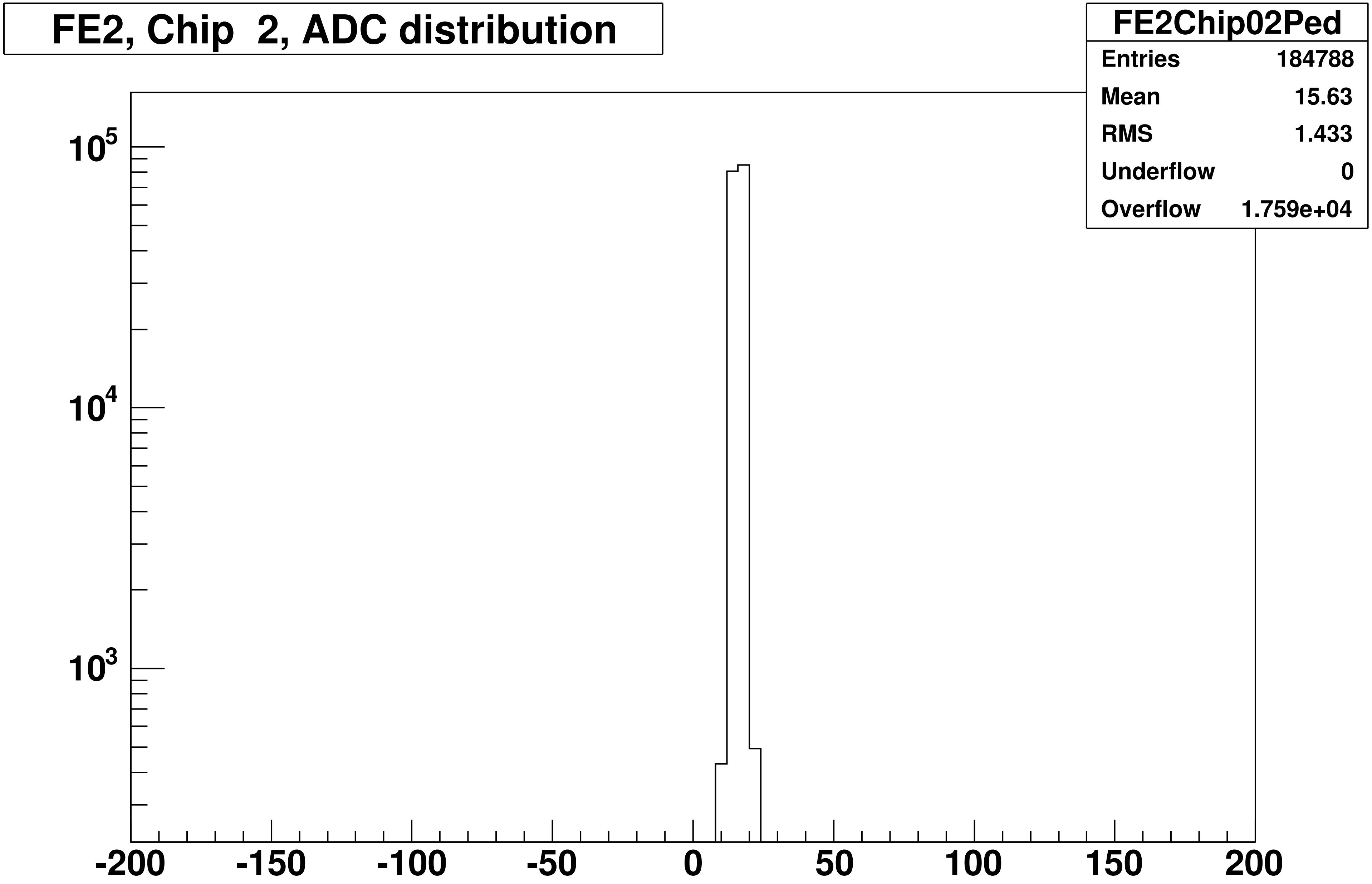
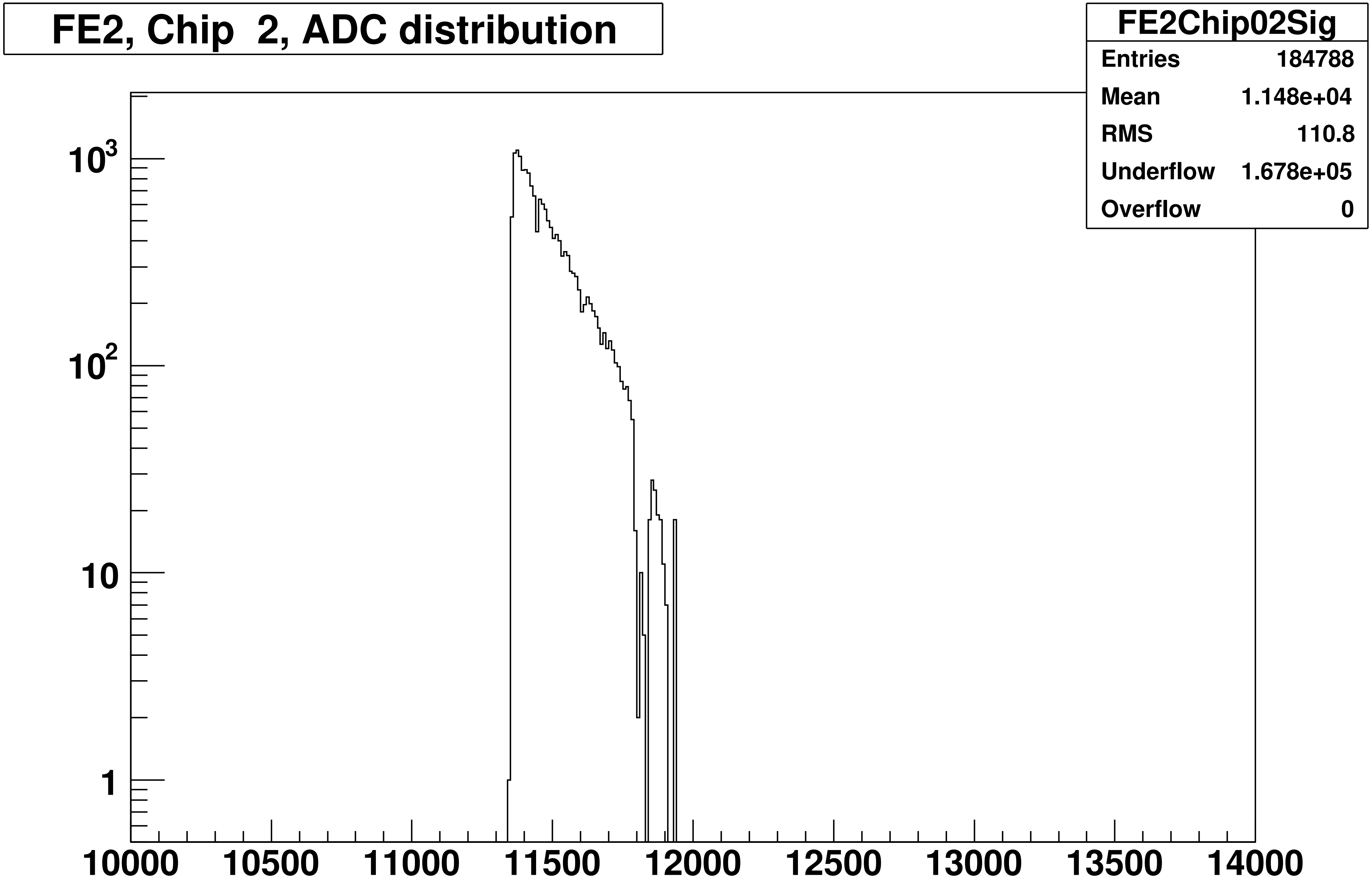
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200



FE2, Chip 1, ADC distribution
FE2Chip01Sig
Entries 184788
Mean 1.148e+04
RMS 112.4
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE2, Chip 2, ADC distribution
FE2Chip02All
Entries 184788
Mean 1070
RMS 3311
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE2, Chip 2, ADC distribution
FE2Chip02Ped
Entries 184788
Mean 15.63
RMS 1.433
Underflow 0
Overflow 1.759e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200


FE2, Chip 2, ADC distribution
FE2Chip02Sig
Entries 184788
Mean 1.148e+04
RMS 110.8
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
1
10000
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11500
12000
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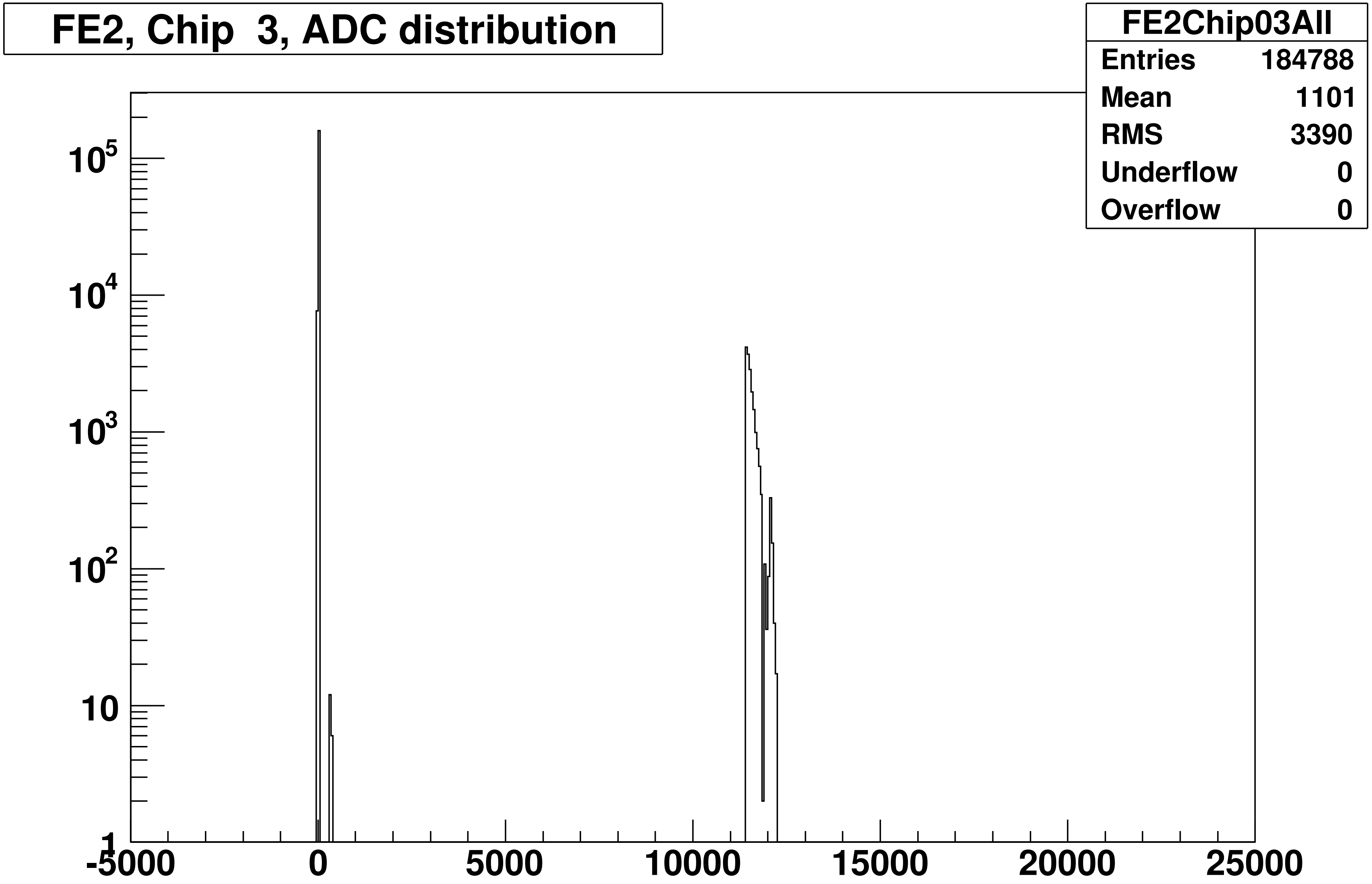
14000


FE2, Chip 3, ADC distribution
FE2Chip03All
Entries 184788
Mean 1101
RMS 3390
Underflow 0
Overflow 0
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10^3
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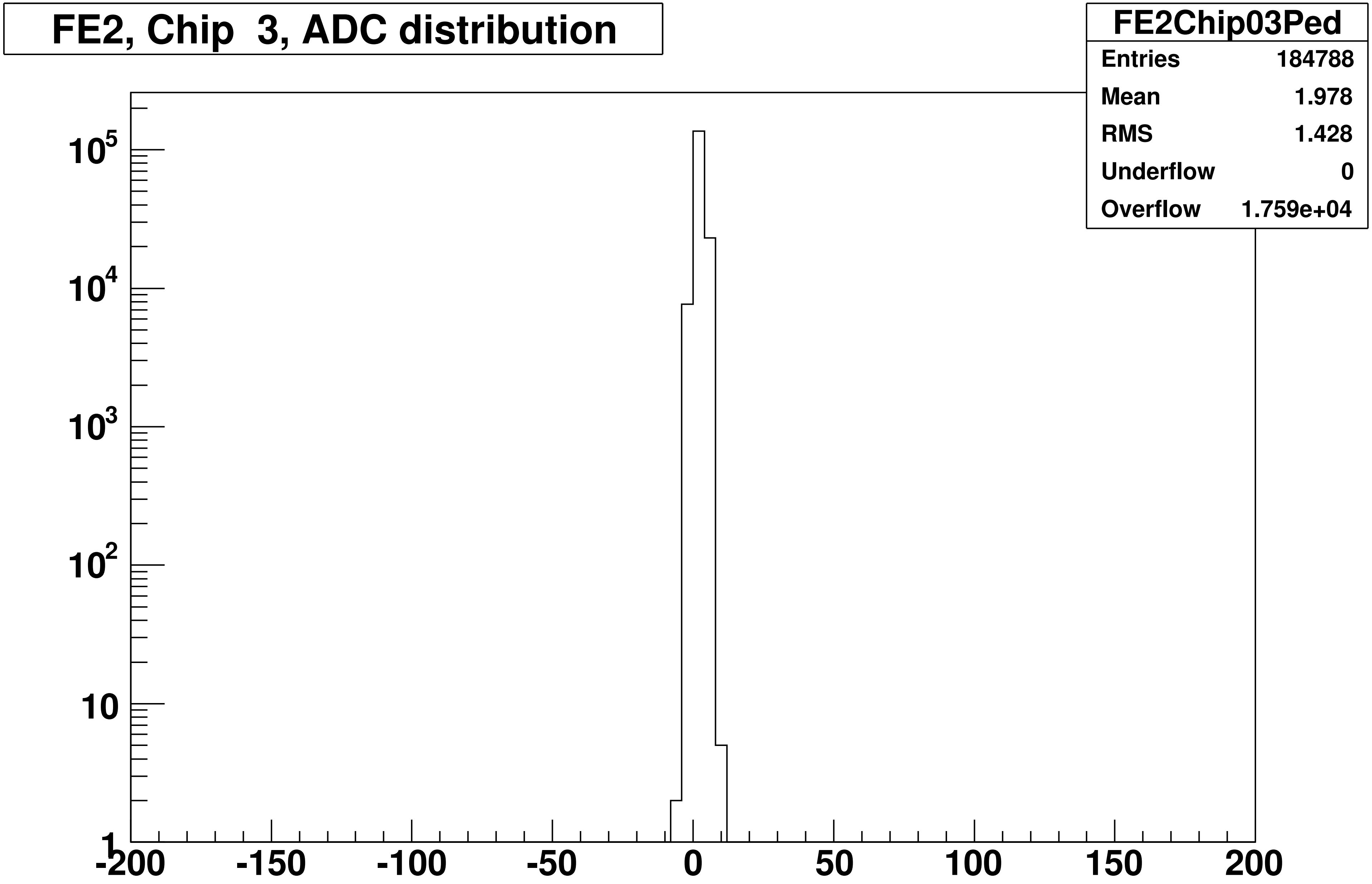
FE2, Chip 3, ADC distribution
FE2Chip03Ped
Entries 184788
Mean 1.978
RMS 1.428
Underflow 0
Overflow 1.759e+04
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10^4
10^3
10^2
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150
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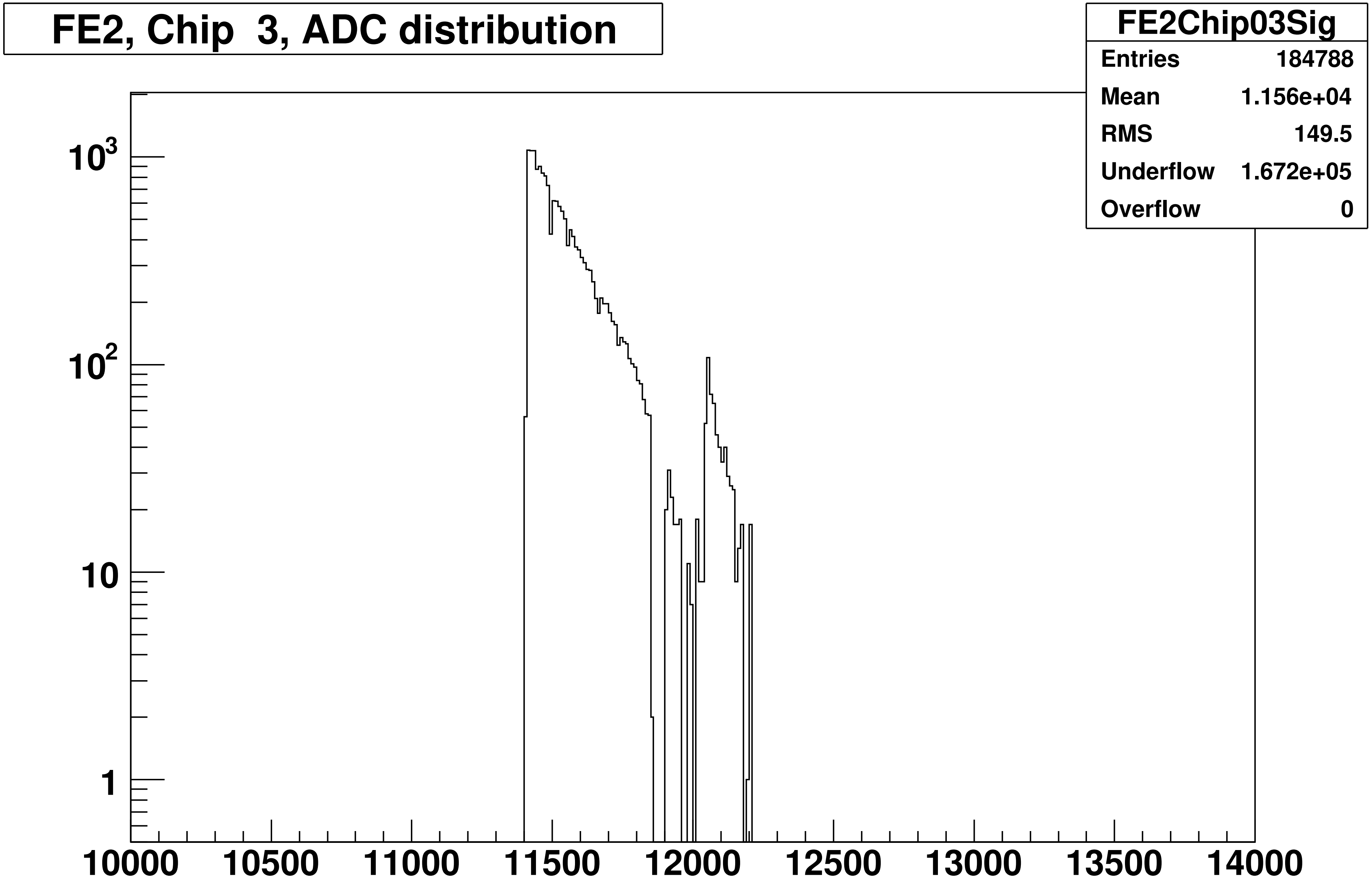
FE2, Chip 3, ADC distribution
FE2Chip03Sig
Entries 184788
Mean 1.156e+04
RMS 149.5
Underflow 1.672e+05
Overflow 0
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10
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10000
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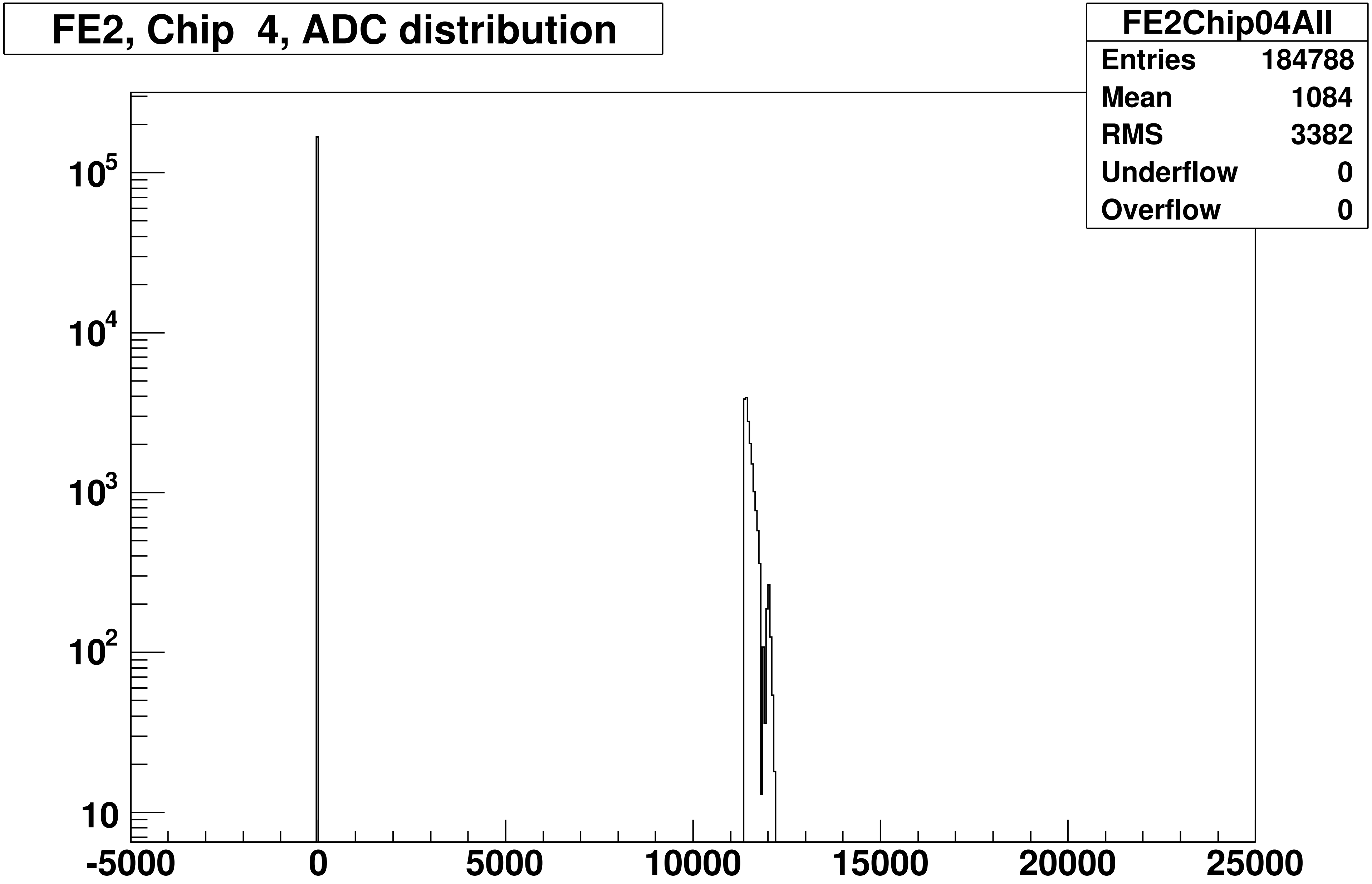

FE2, Chip 4, ADC distribution
FE2Chip04All
Entries 184788
Mean 1084
RMS 3382
Underflow 0
Overflow 0
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10^4
10^3
10^2
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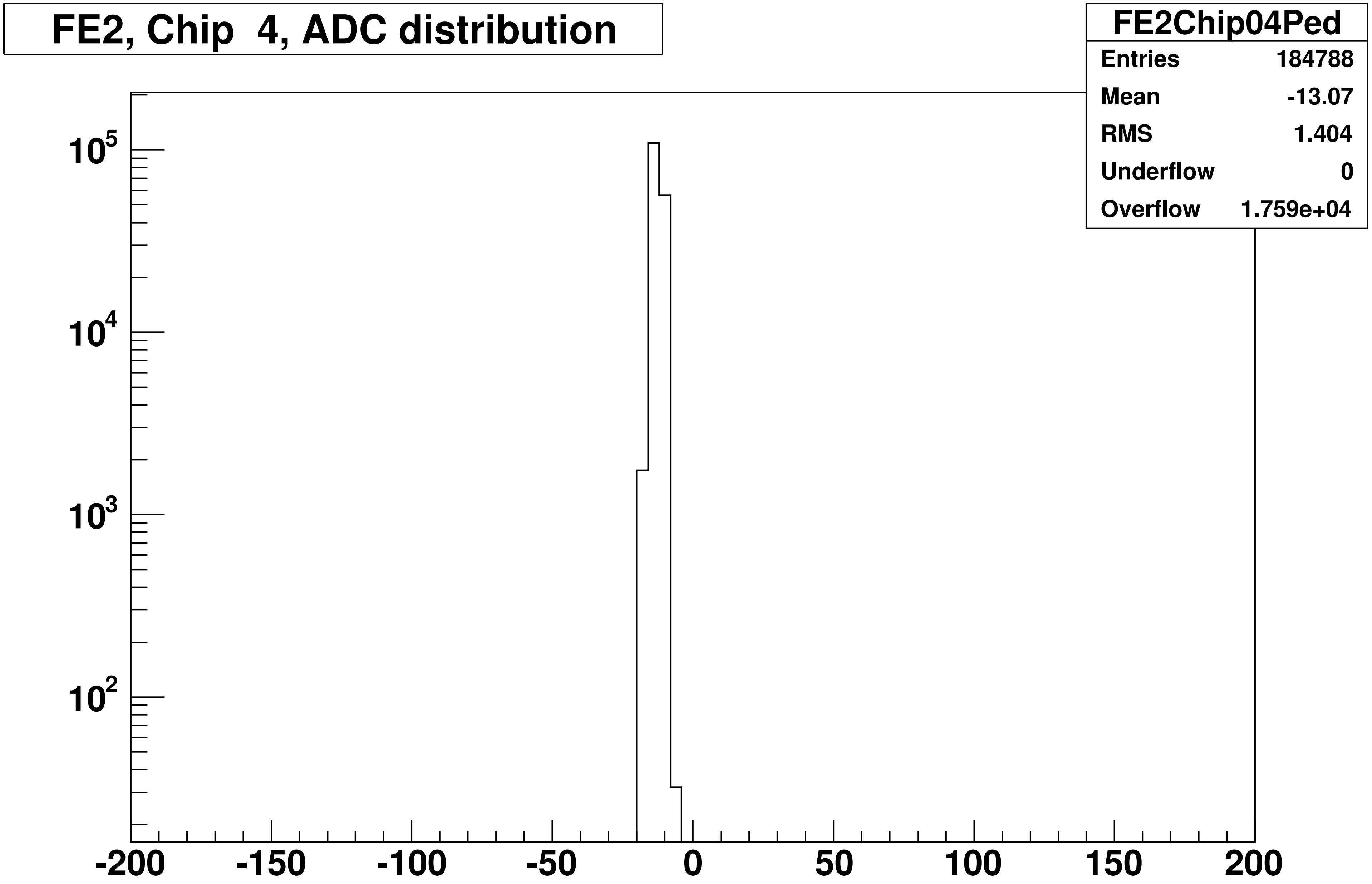
FE2, Chip 4, ADC distribution
FE2Chip04Ped
Entries 184788
Mean -13.07
RMS 1.404
Underflow 0
Overflow 1.759e+04
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10^4
10^3
10^2
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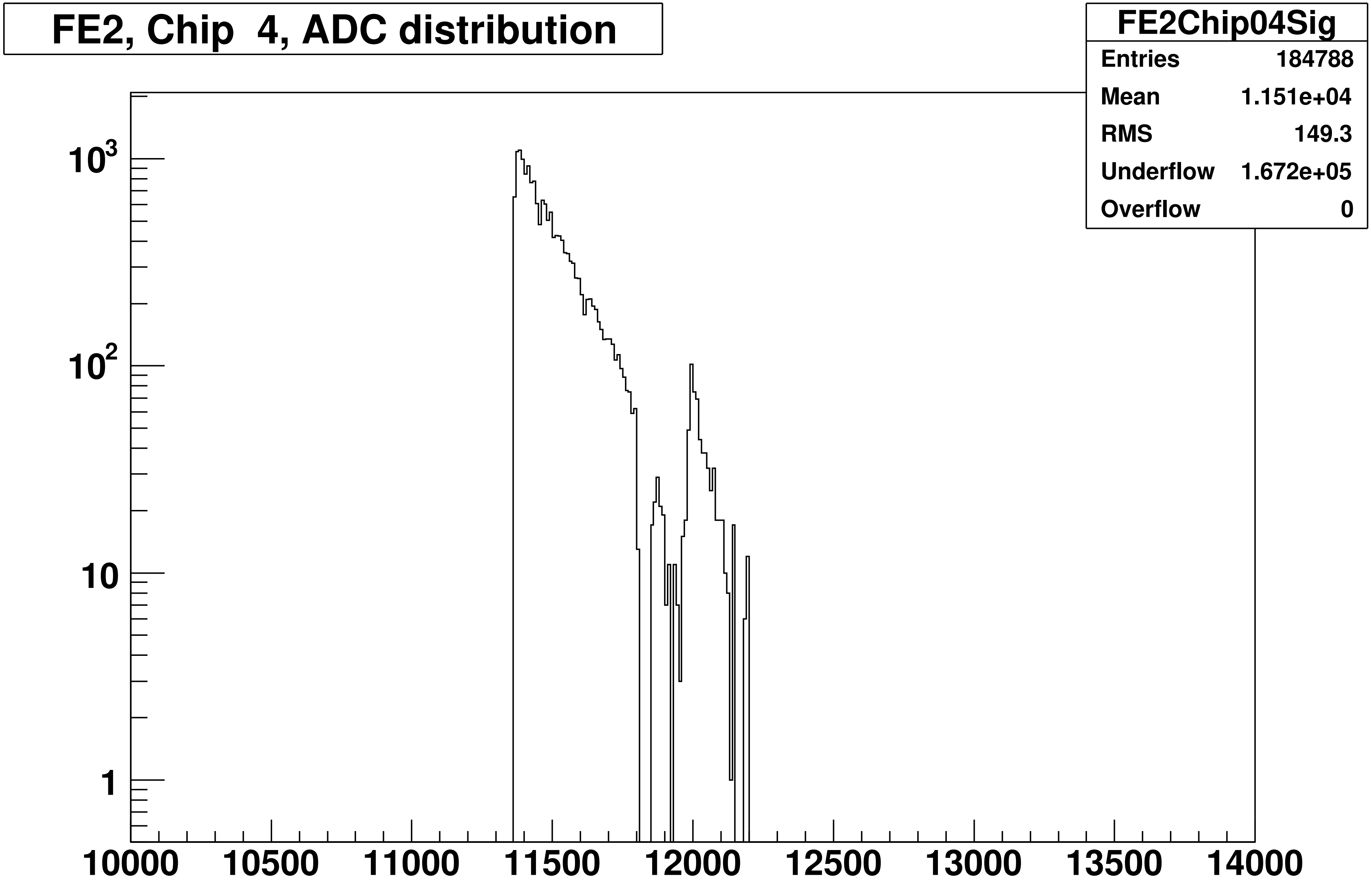
FE2, Chip 4, ADC distribution
FE2Chip04Sig
Entries 184788
Mean 1.151e+04
RMS 149.3
Underflow 1.672e+05
Overflow 0
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10^2
10
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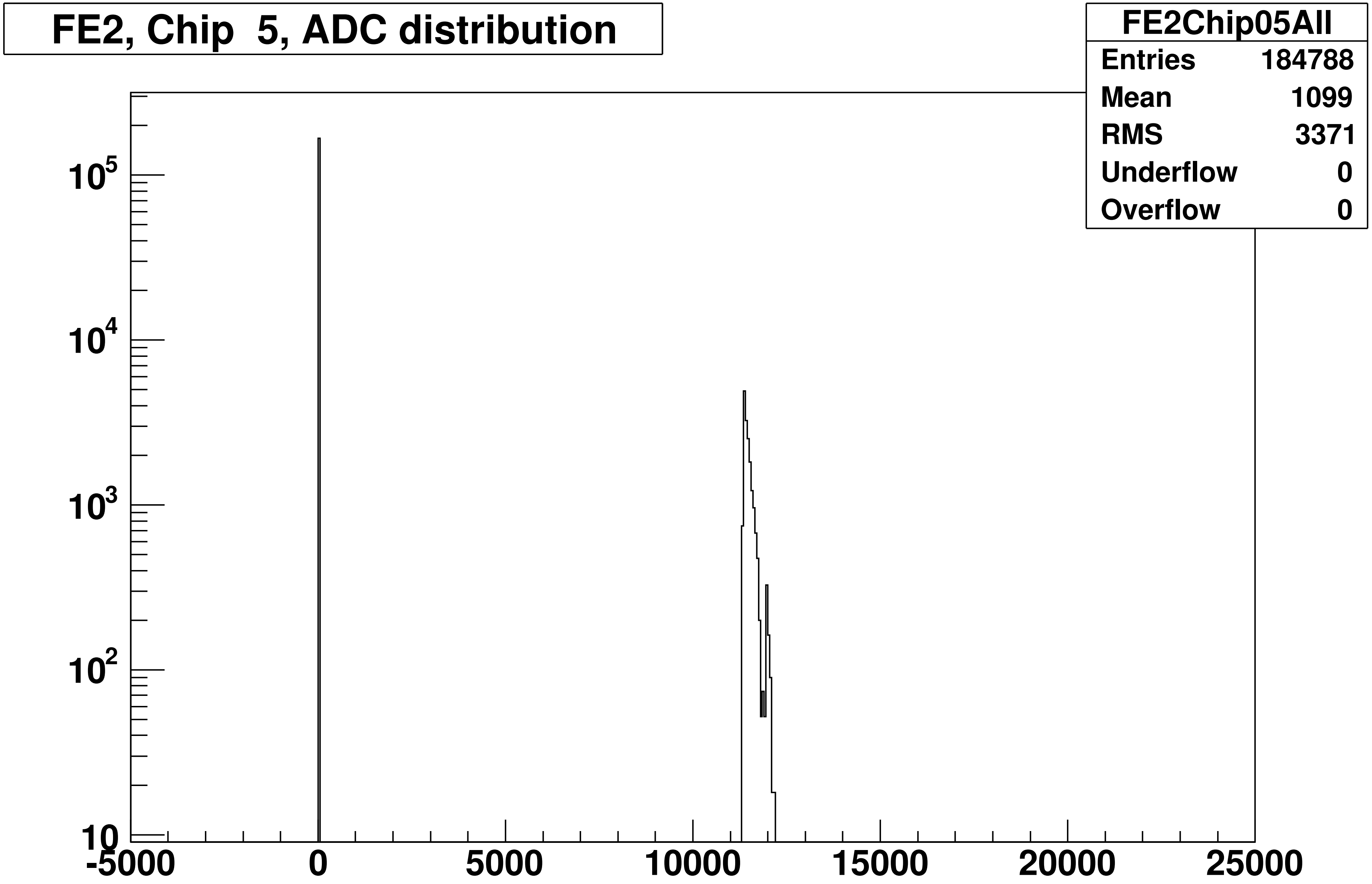

FE2, Chip 5, ADC distribution
FE2Chip05All
Entries 184788
Mean 1099
RMS 3371
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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5000
10000
15000
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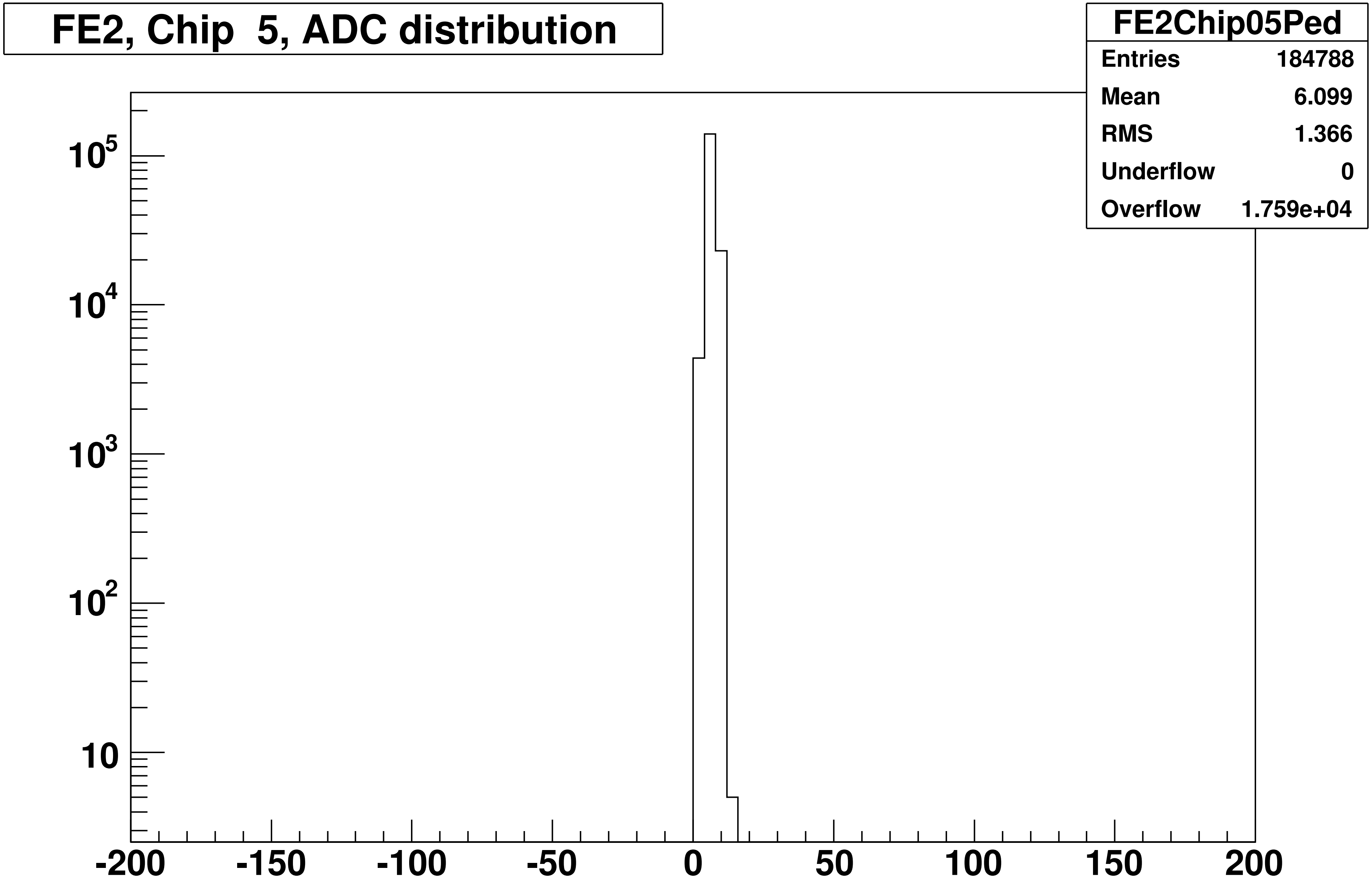
FE2, Chip 5, ADC distribution
FE2Chip05Ped
Entries 184788
Mean 6.099
RMS 1.366
Underflow 0
Overflow 1.759e+04
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10^4
10^3
10^2
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-100
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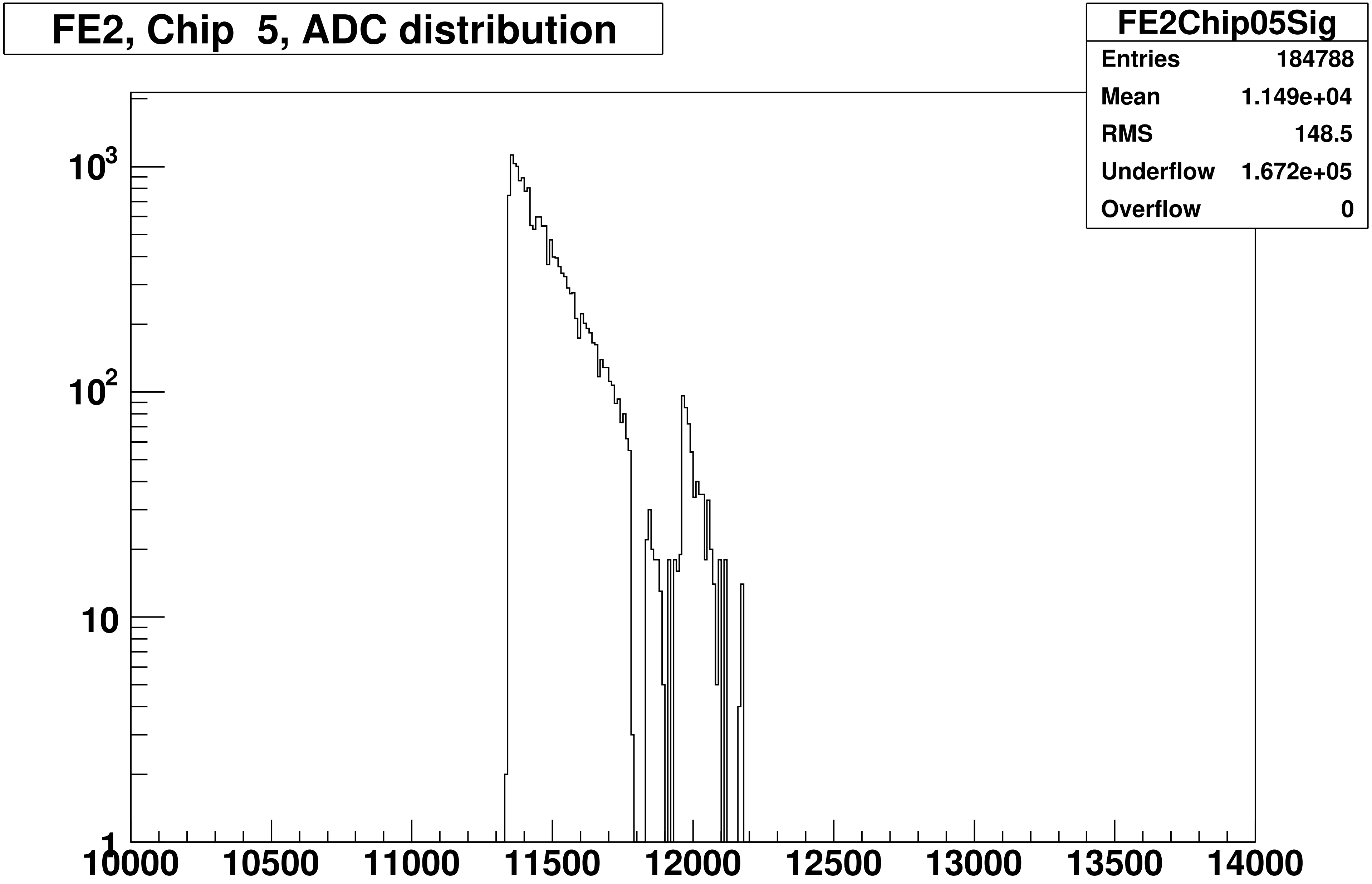
150
200


FE2, Chip 5, ADC distribution
FE2Chip05Sig
Entries 184788
Mean 1.149e+04
RMS 148.5
Underflow 1.672e+05
Overflow 0
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10^2
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1
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11500
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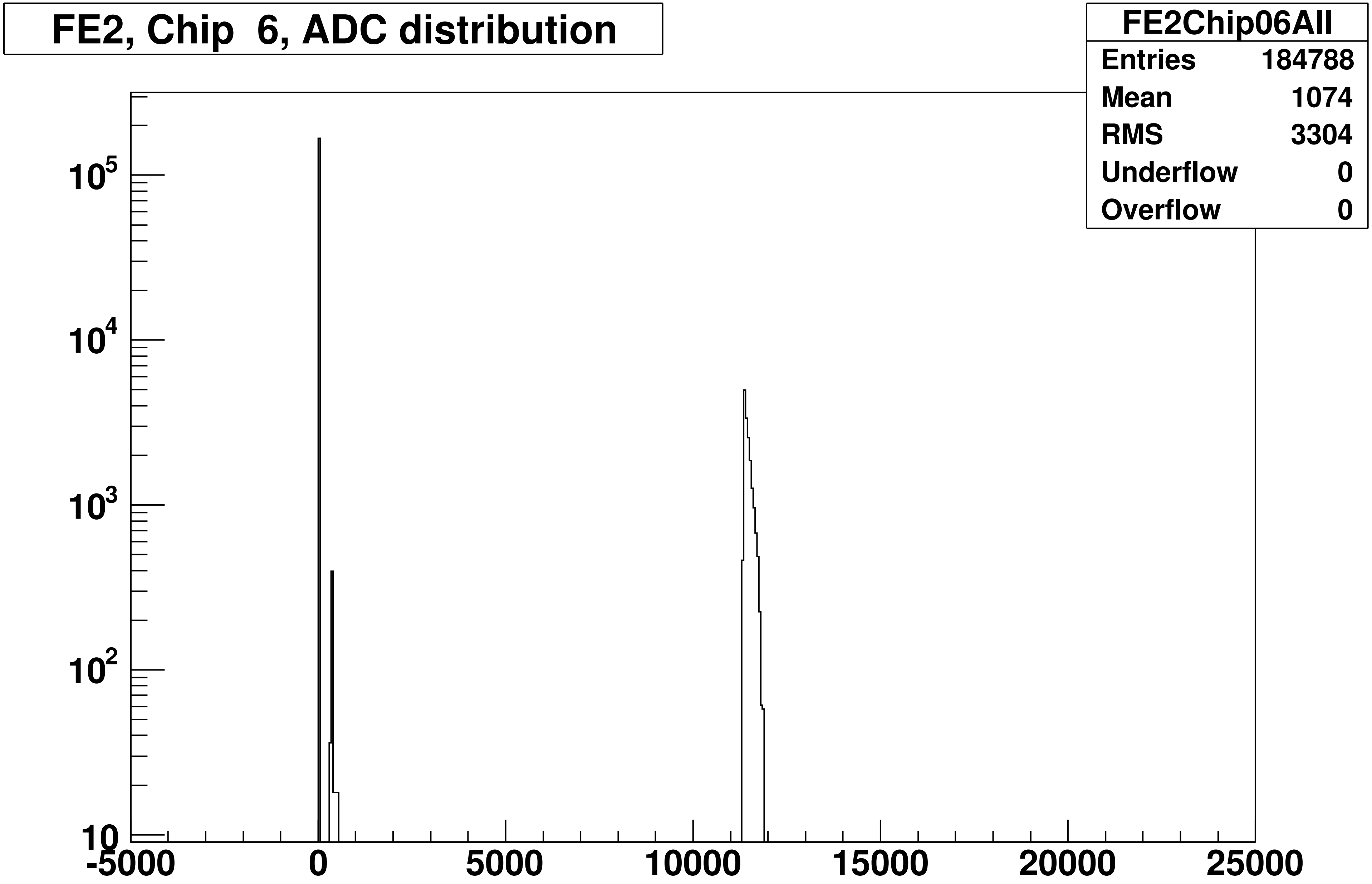
FE2, Chip 6, ADC distribution
FE2Chip06All
Entries 184788
Mean 1074
RMS 3304
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
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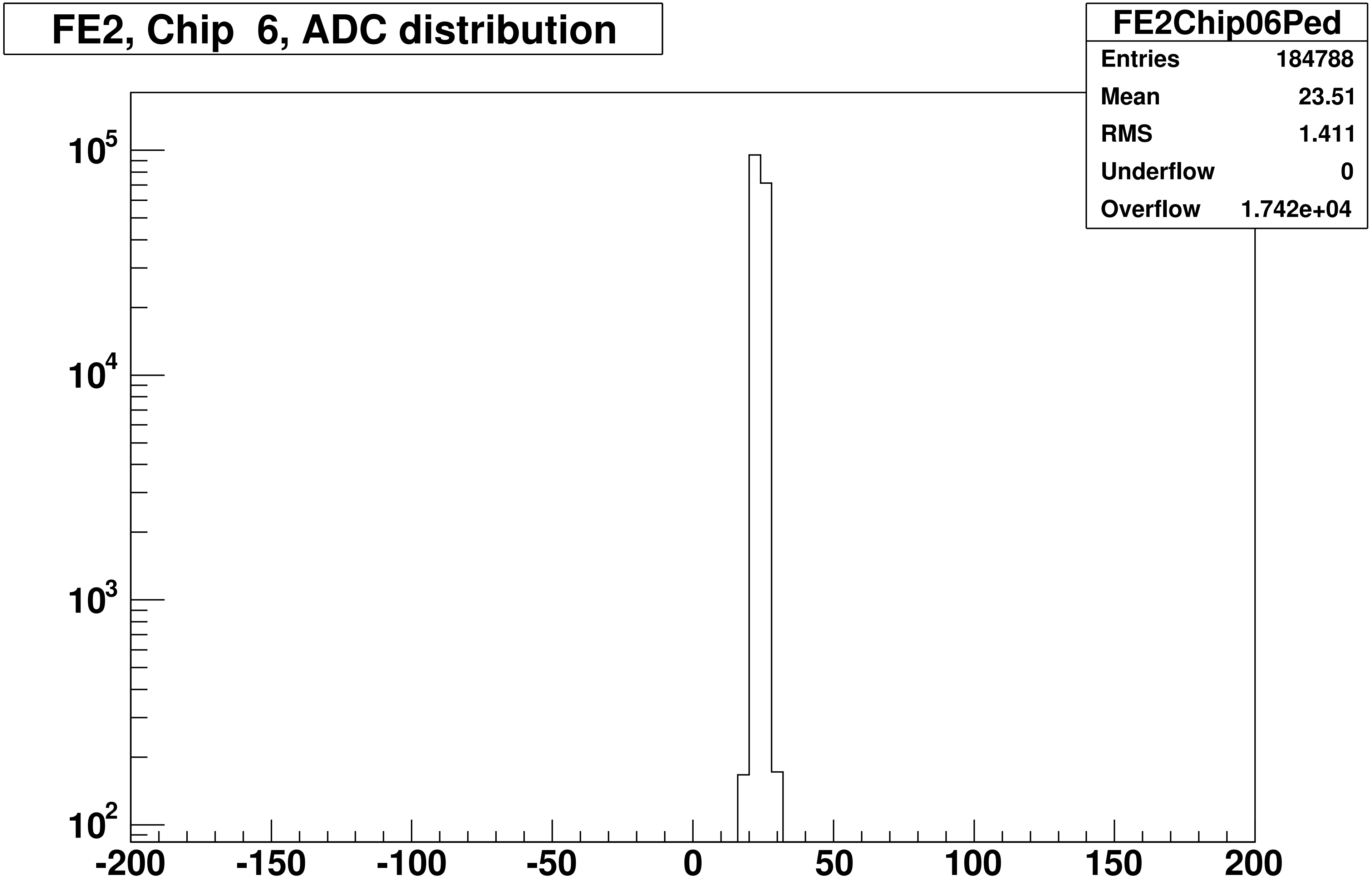
5000
10000
15000
20000
25000


FE2, Chip 6, ADC distribution
FE2Chip06Ped
Entries 184788
Mean 23.51
RMS 1.411
Underflow 0
Overflow 1.742e+04
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10^4
10^3
10^2
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150
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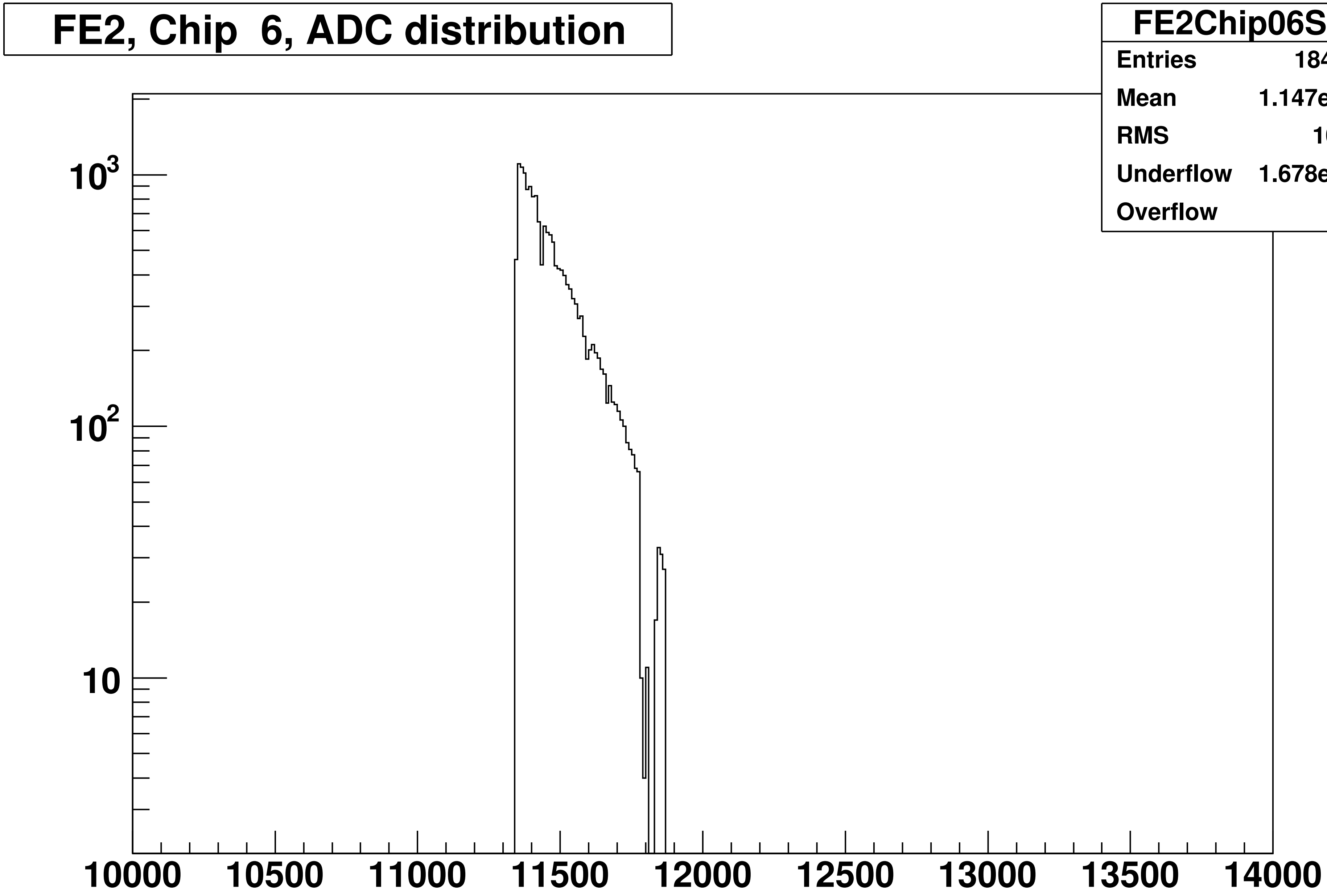
FE2, Chip 6, ADC distribution
FE2Chip06Sig
Entries 184788
Mean 1.147e+04
RMS 108.9
Underflow 1.678e+05
Overflow 0
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10^2
10
10000
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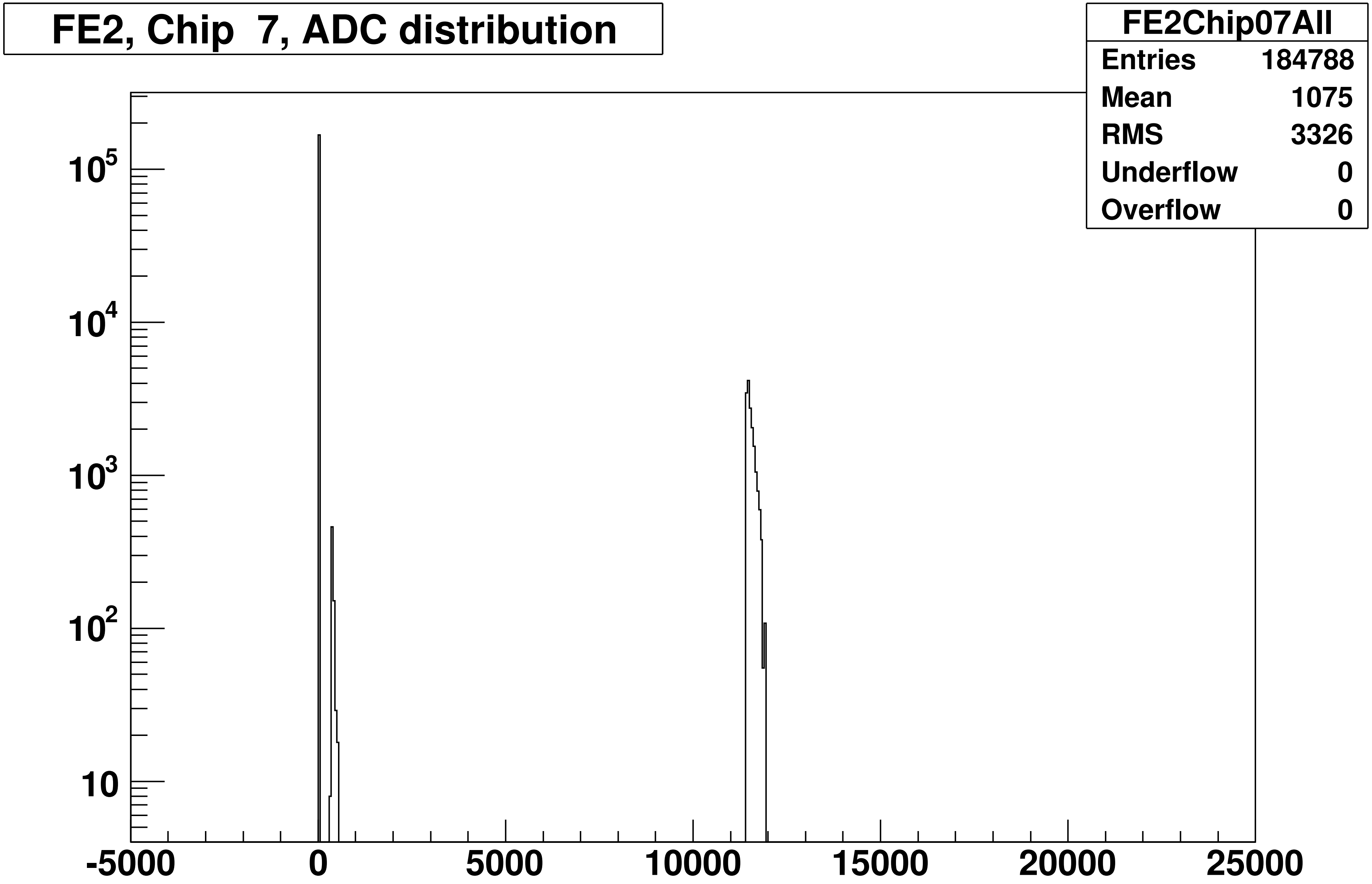
FE2, Chip 7, ADC distribution
FE2Chip07All
Entries 184788
Mean 1075
RMS 3326
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
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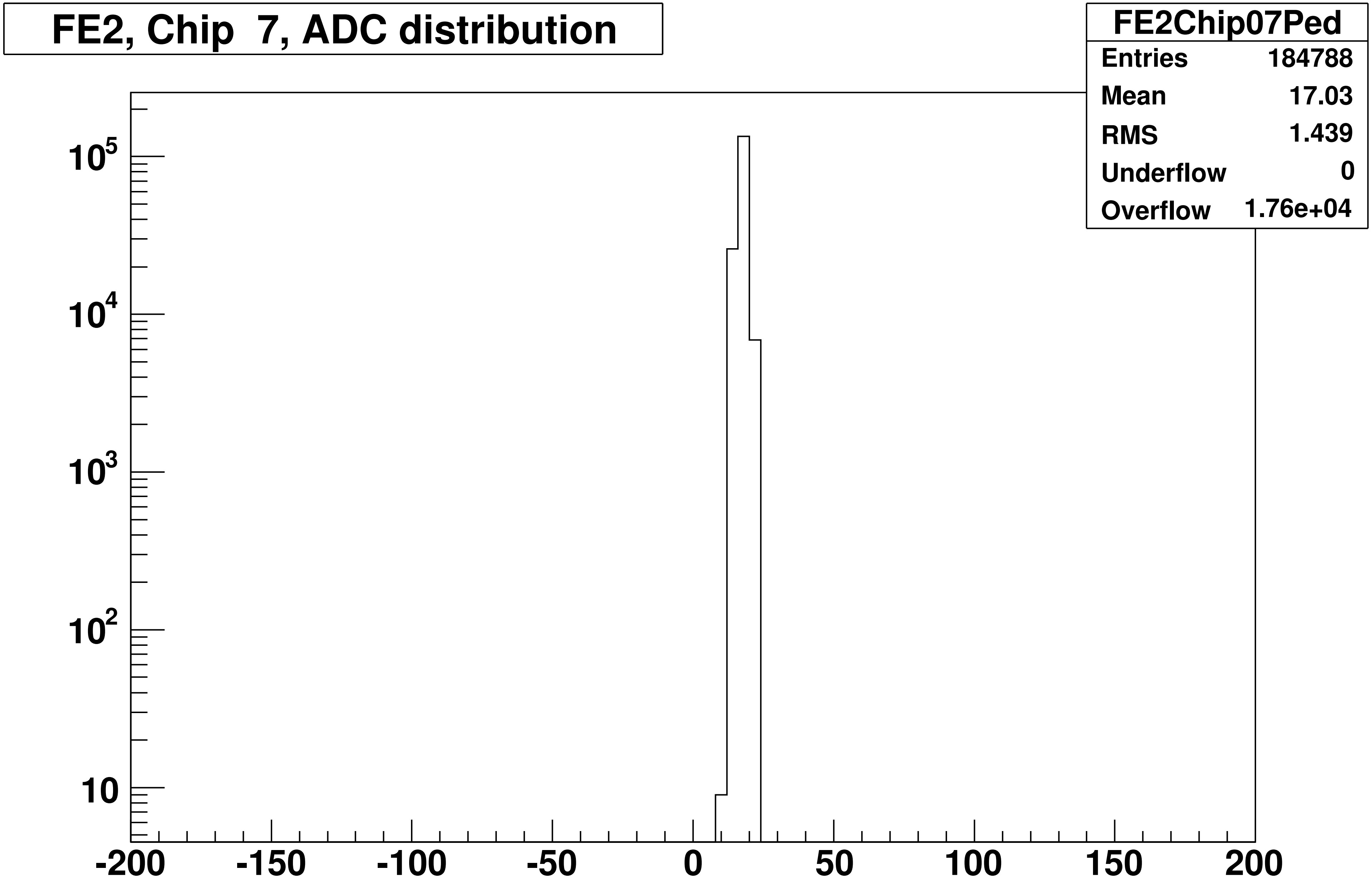
15000
20000
25000


FE2, Chip 7, ADC distribution
FE2Chip07Ped
Entries 184788
Mean 17.03
RMS 1.439
Underflow 0
Overflow 1.76e+04
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10^4
10^3
10^2
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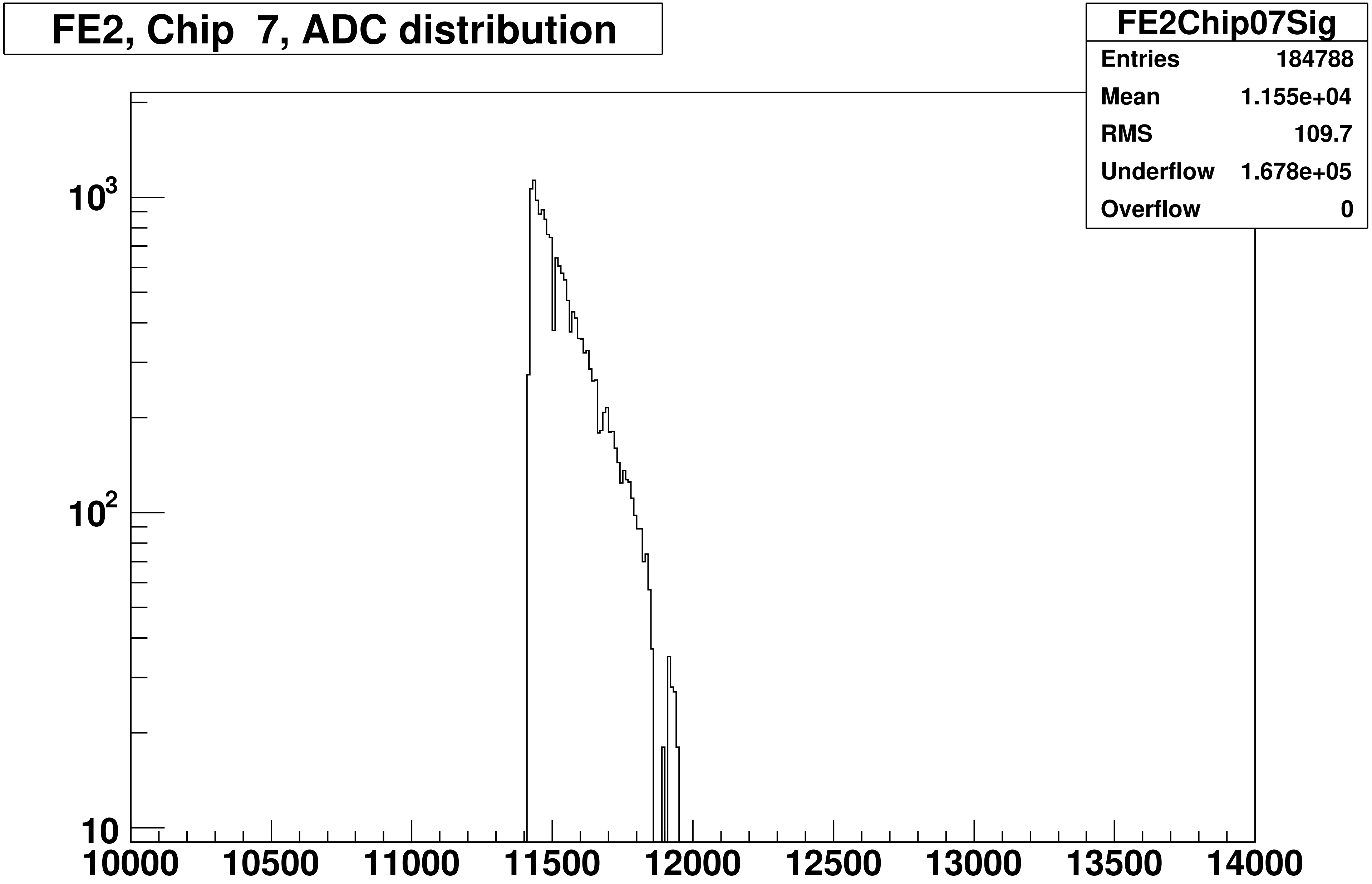
150
200


FE2, Chip 7, ADC distribution
FE2Chip07Sig
Entries 184788
Mean 1.155e+04
RMS 109.7
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
10000
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11500
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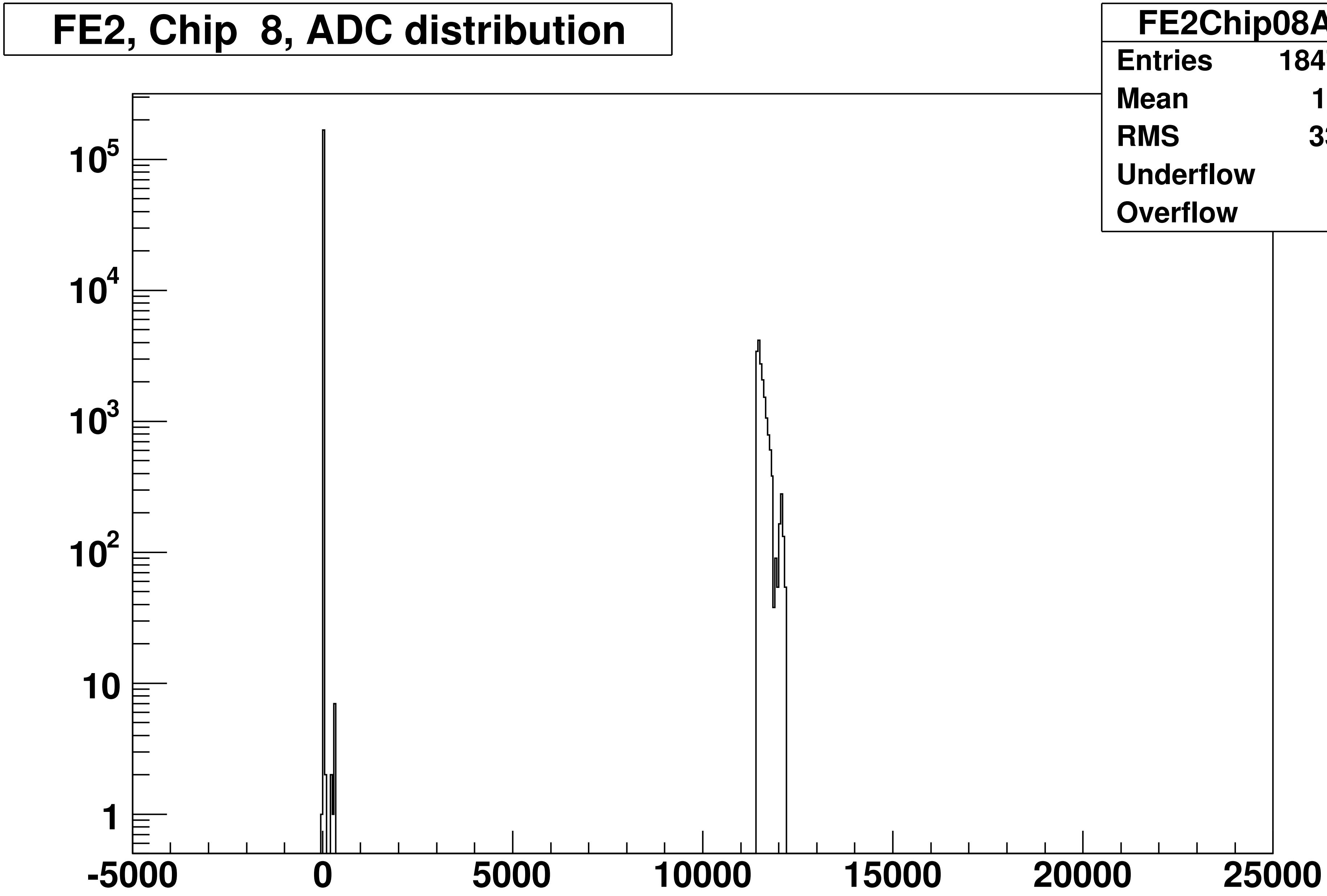
FE2, Chip 8, ADC distribution
FE2Chip08All
Entries 184788
Mean 1106
RMS 3393
Underflow 0
Overflow 0
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10^4
10^3
10^2
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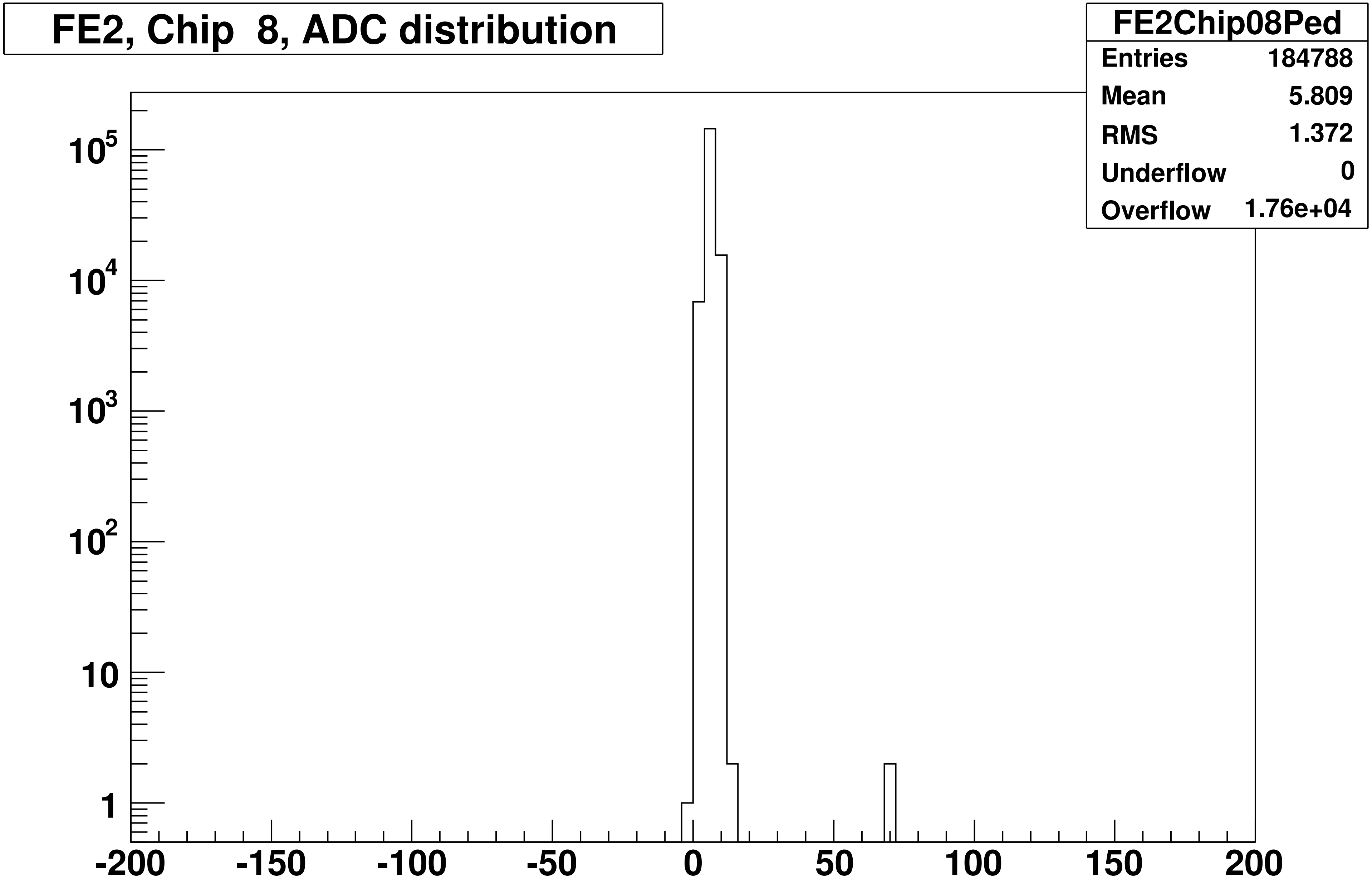
20000
25000


FE2, Chip 8, ADC distribution
FE2Chip08Ped
Entries 184788
Mean 5.809
RMS 1.372
Underflow 0
Overflow 1.76e+04
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10^4
10^3
10^2
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150
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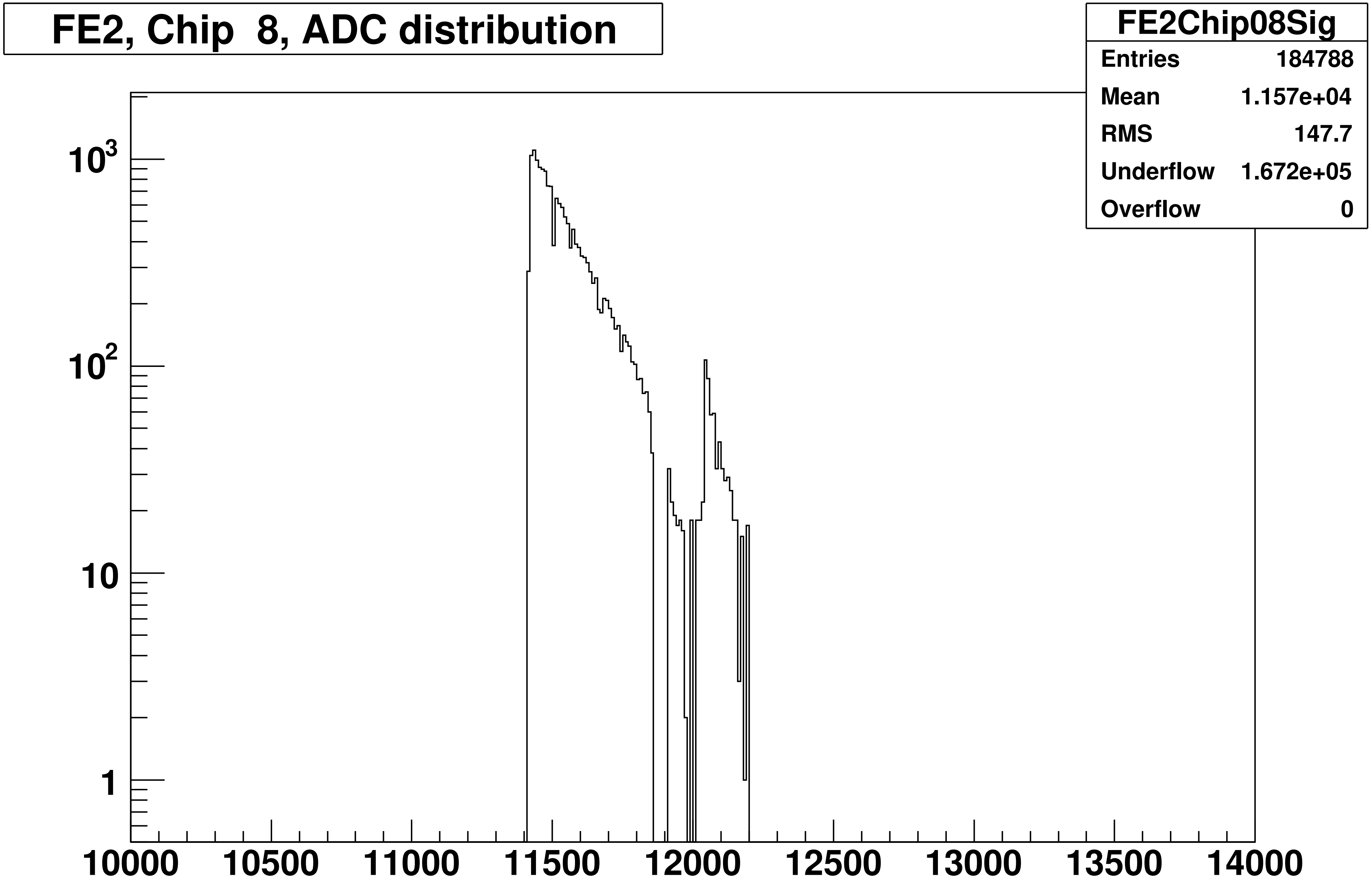

FE2, Chip 8, ADC distribution
FE2Chip08Sig
Entries 184788
Mean 1.157e+04
RMS 147.7
Underflow 1.672e+05
Overflow 0
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10^2
10
1
10000
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11500
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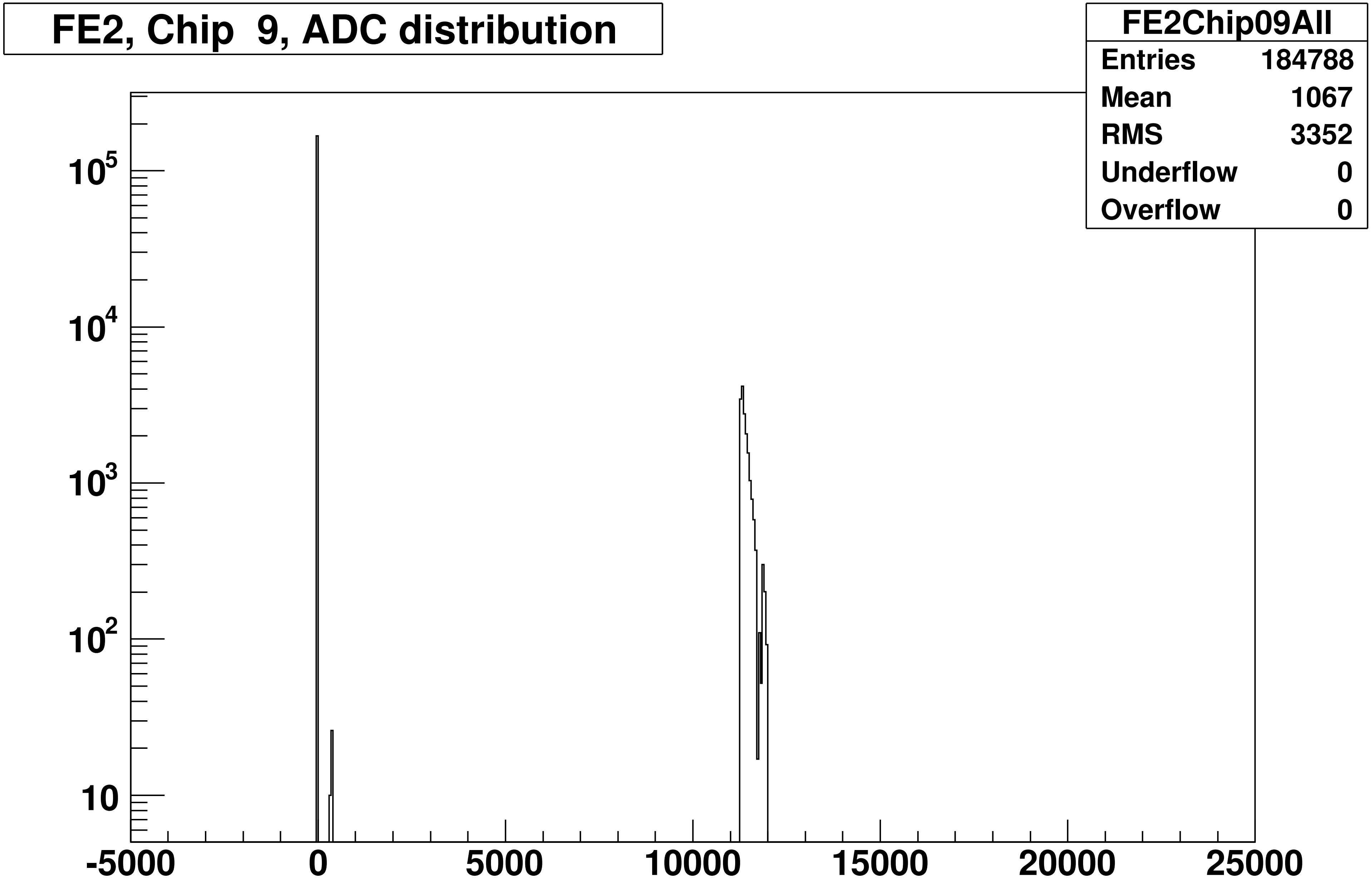
FE2, Chip 9, ADC distribution
FE2Chip09All
Entries 184788
Mean 1067
RMS 3352
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
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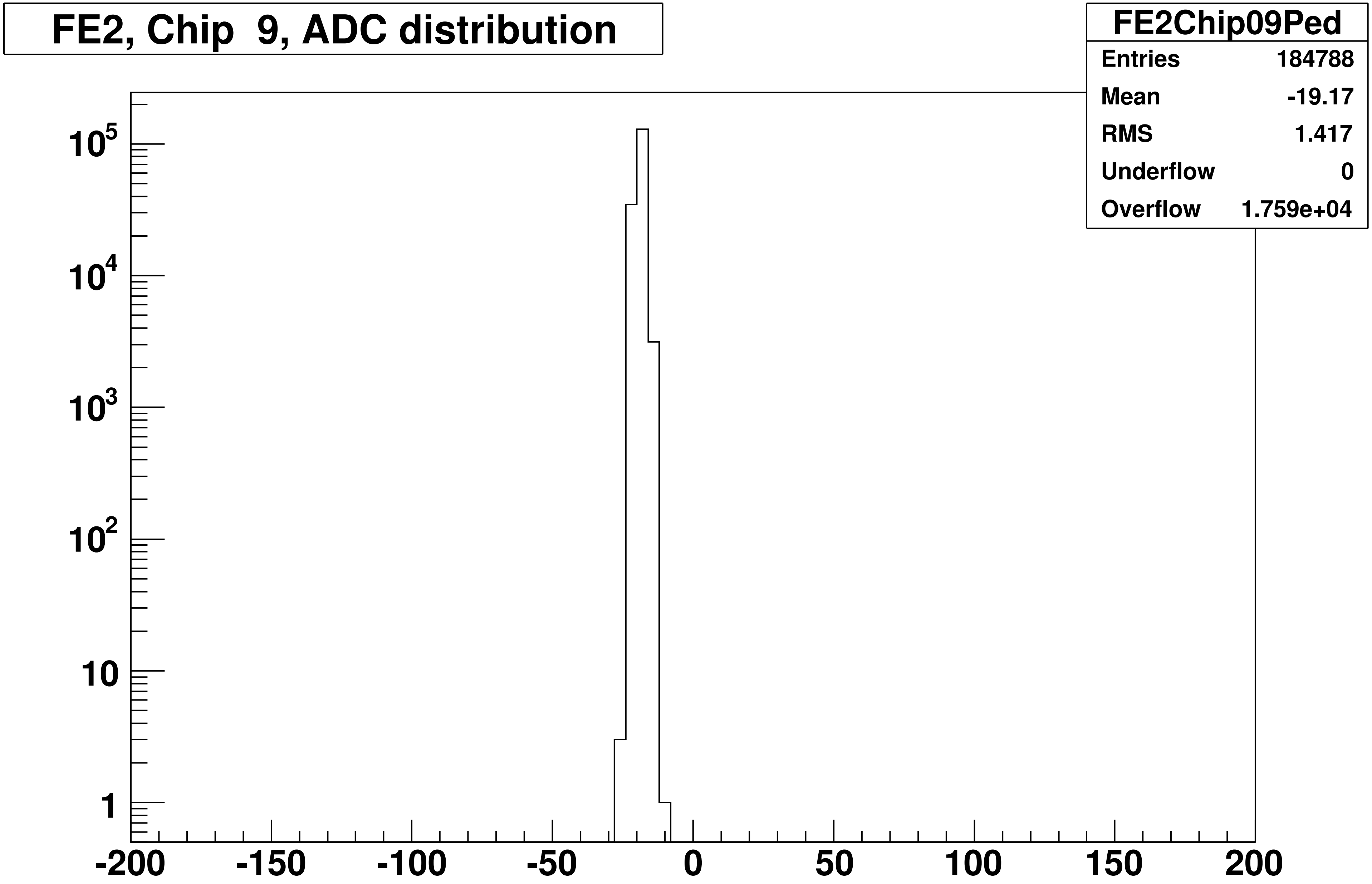
10000
15000
20000
25000


FE2, Chip 9, ADC distribution
FE2Chip09Ped
Entries 184788
Mean -19.17
RMS 1.417
Underflow 0
Overflow 1.759e+04
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10^4
10^3
10^2
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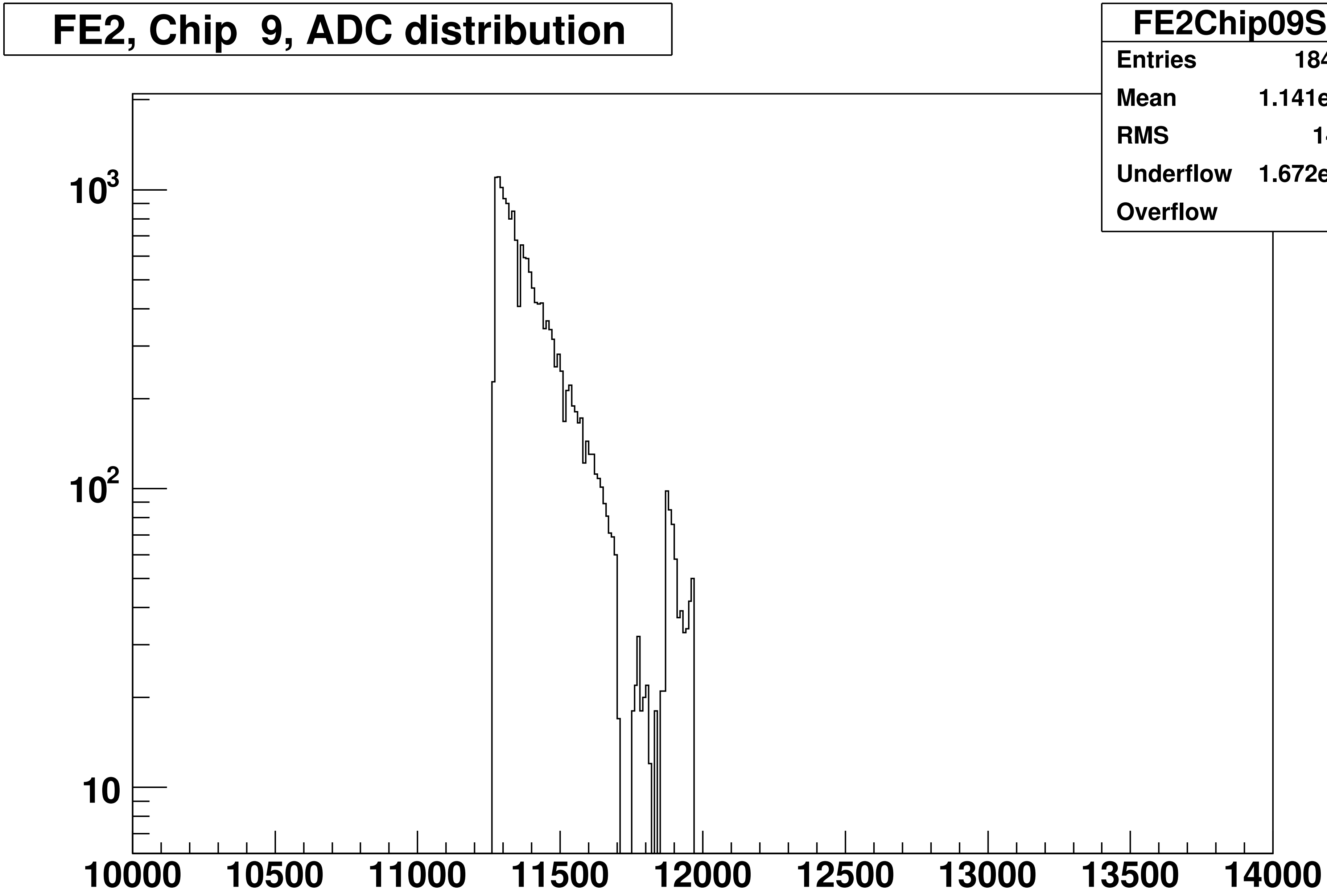
FE2, Chip 9, ADC distribution
FE2Chip09Sig
Entries 184788
Mean 1.141e+04
RMS 142.7
Underflow 1.672e+05
Overflow 0
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10^2
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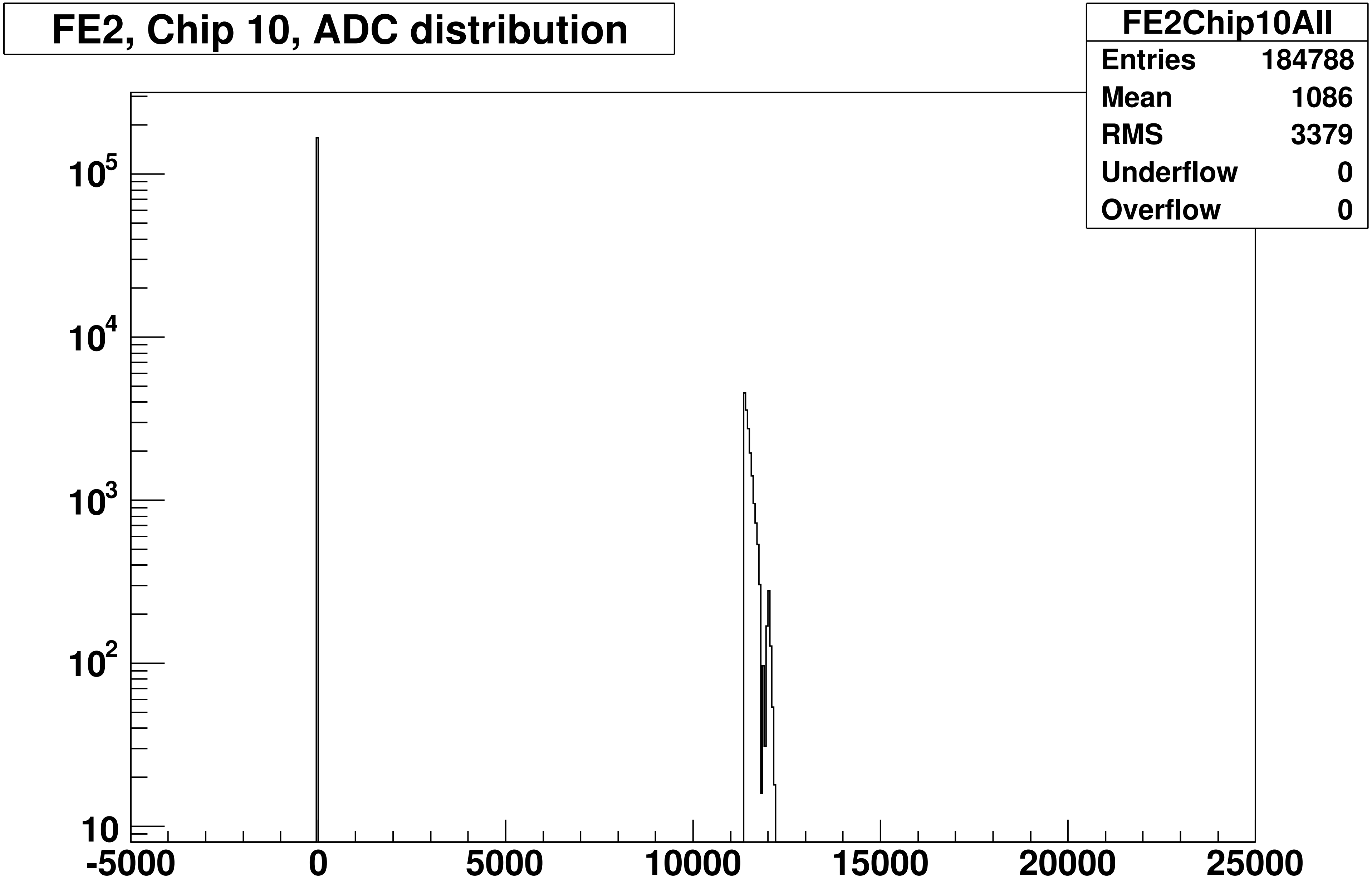
FE2, Chip 10, ADC distribution
FE2Chip10All
Entries 184788
Mean 1086
RMS 3379
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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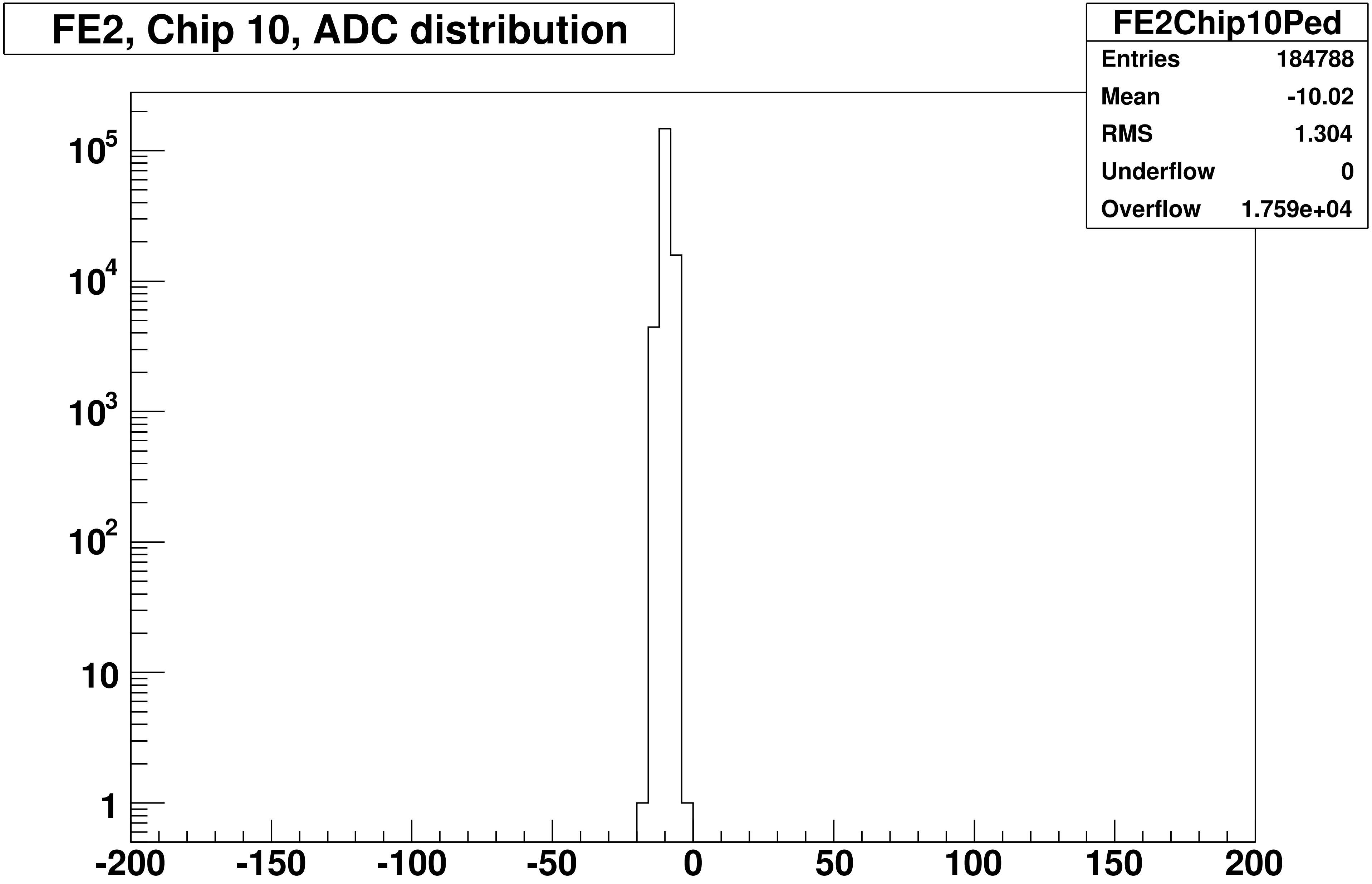
25000


FE2, Chip 10, ADC distribution
FE2Chip10Ped
Entries 184788
Mean -10.02
RMS 1.304
Underflow 0
Overflow 1.759e+04
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10^3
10^2
10
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-100
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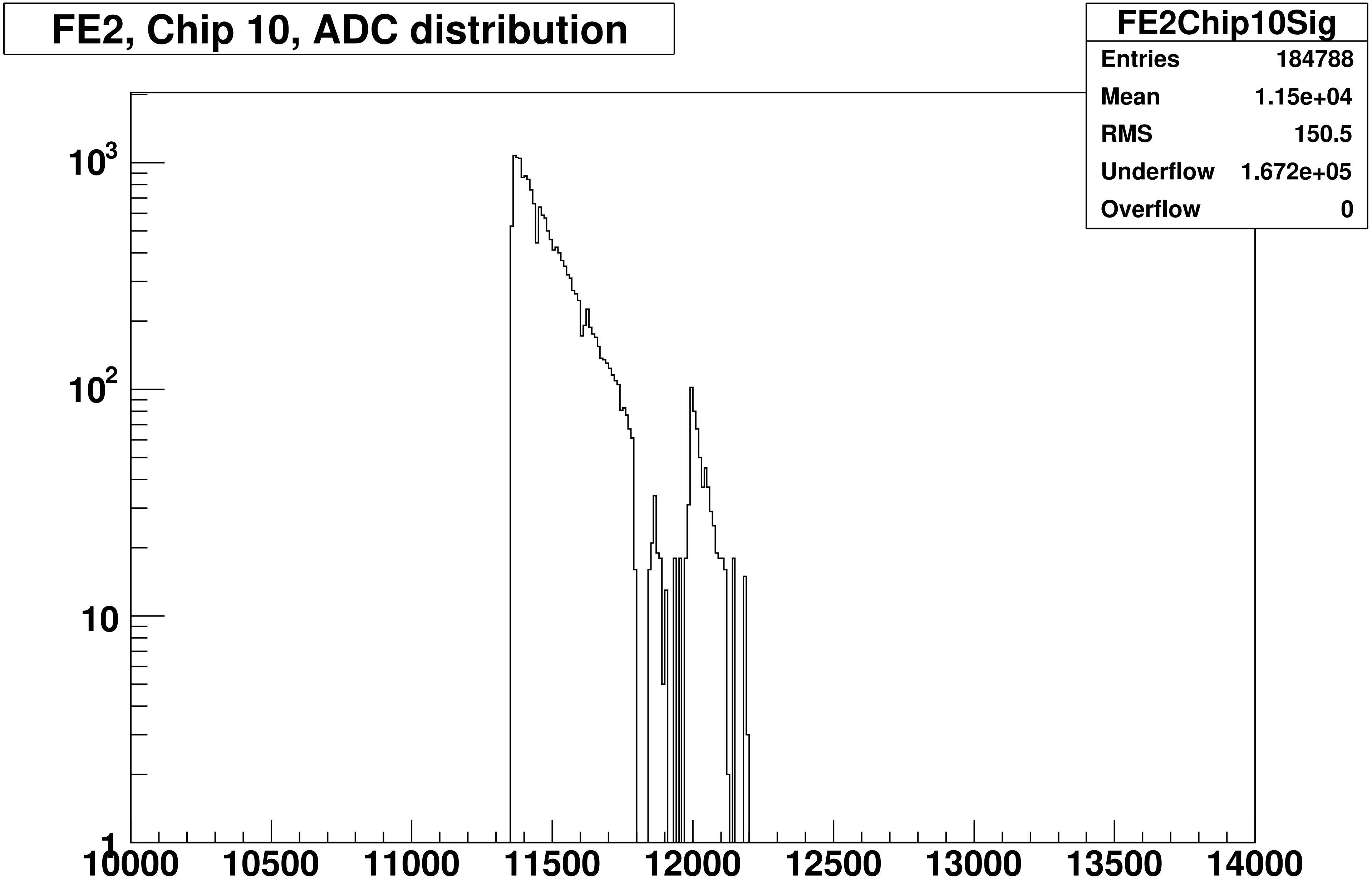
150
200


FE2, Chip 10, ADC distribution
FE2Chip10Sig
Entries 184788
Mean 1.15e+04
RMS 150.5
Underflow 1.672e+05
Overflow 0
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10^2
10
1
10000
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11500
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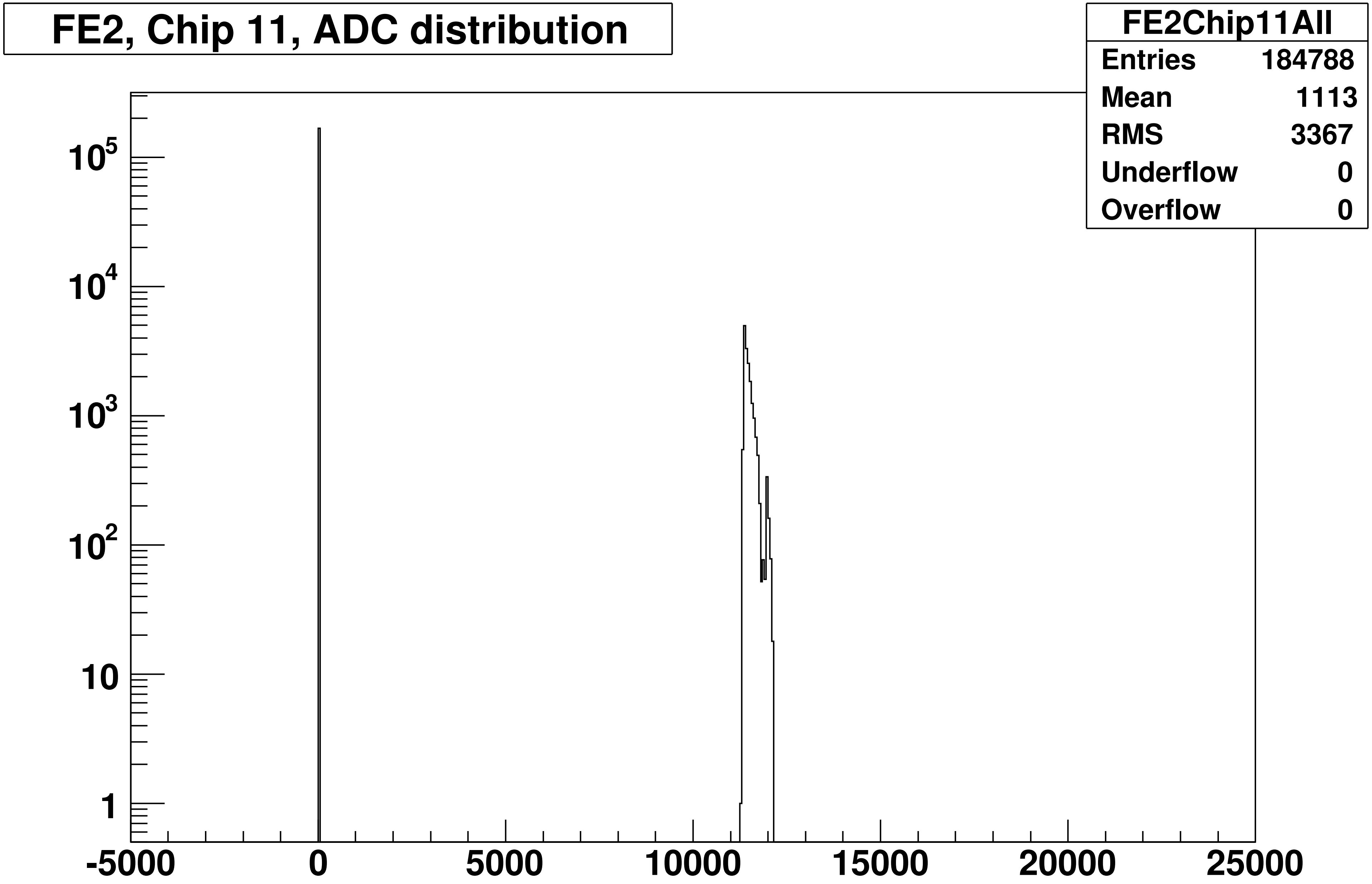
FE2, Chip 11, ADC distribution
FE2Chip11All
Entries 184788
Mean 1113
RMS 3367
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
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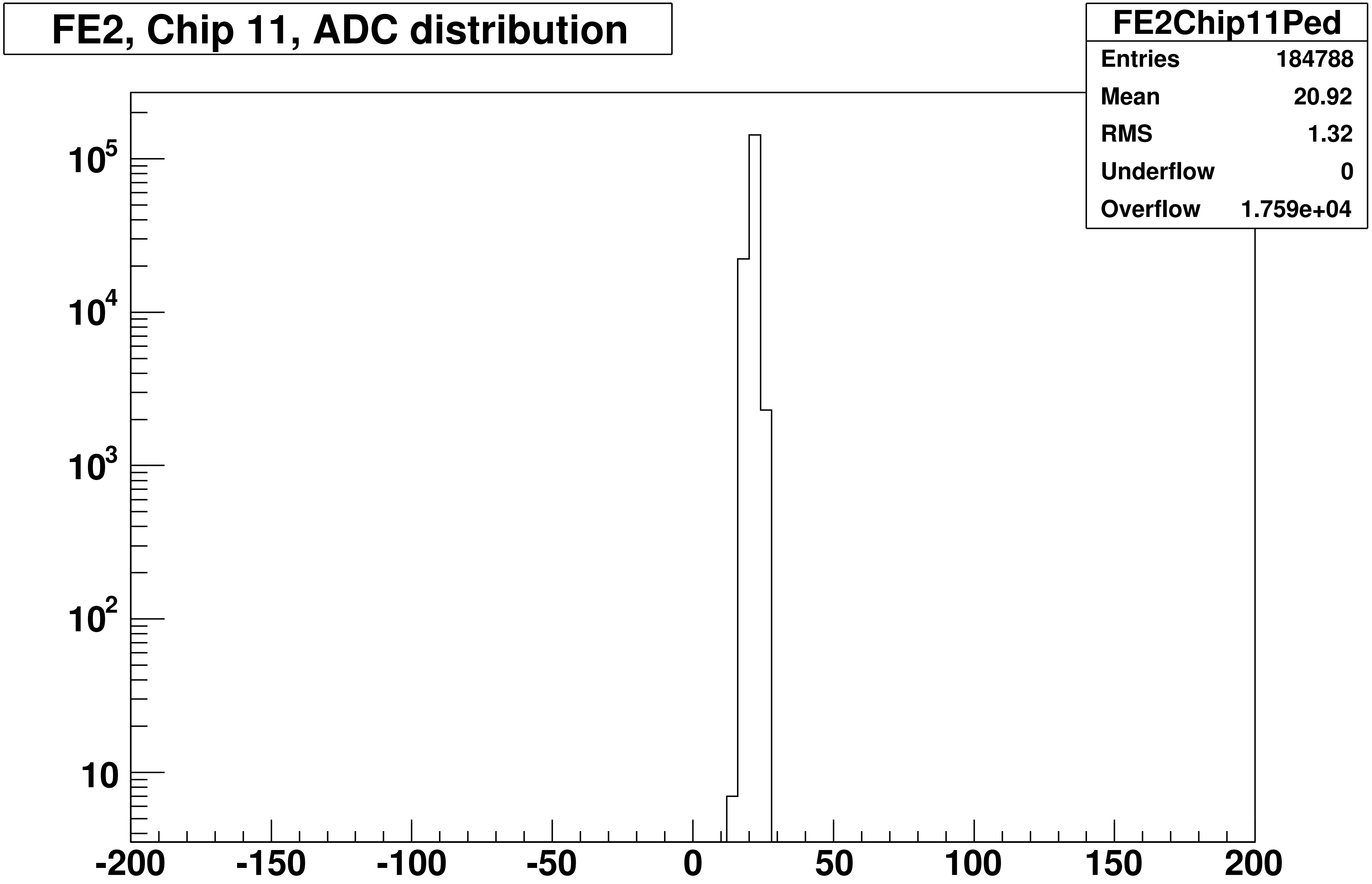
FE2, Chip 11, ADC distribution
FE2Chip11Ped
Entries 184788
Mean 20.92
RMS 1.32
Underflow 0
Overflow 1.759e+04
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10^4
10^3
10^2
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150
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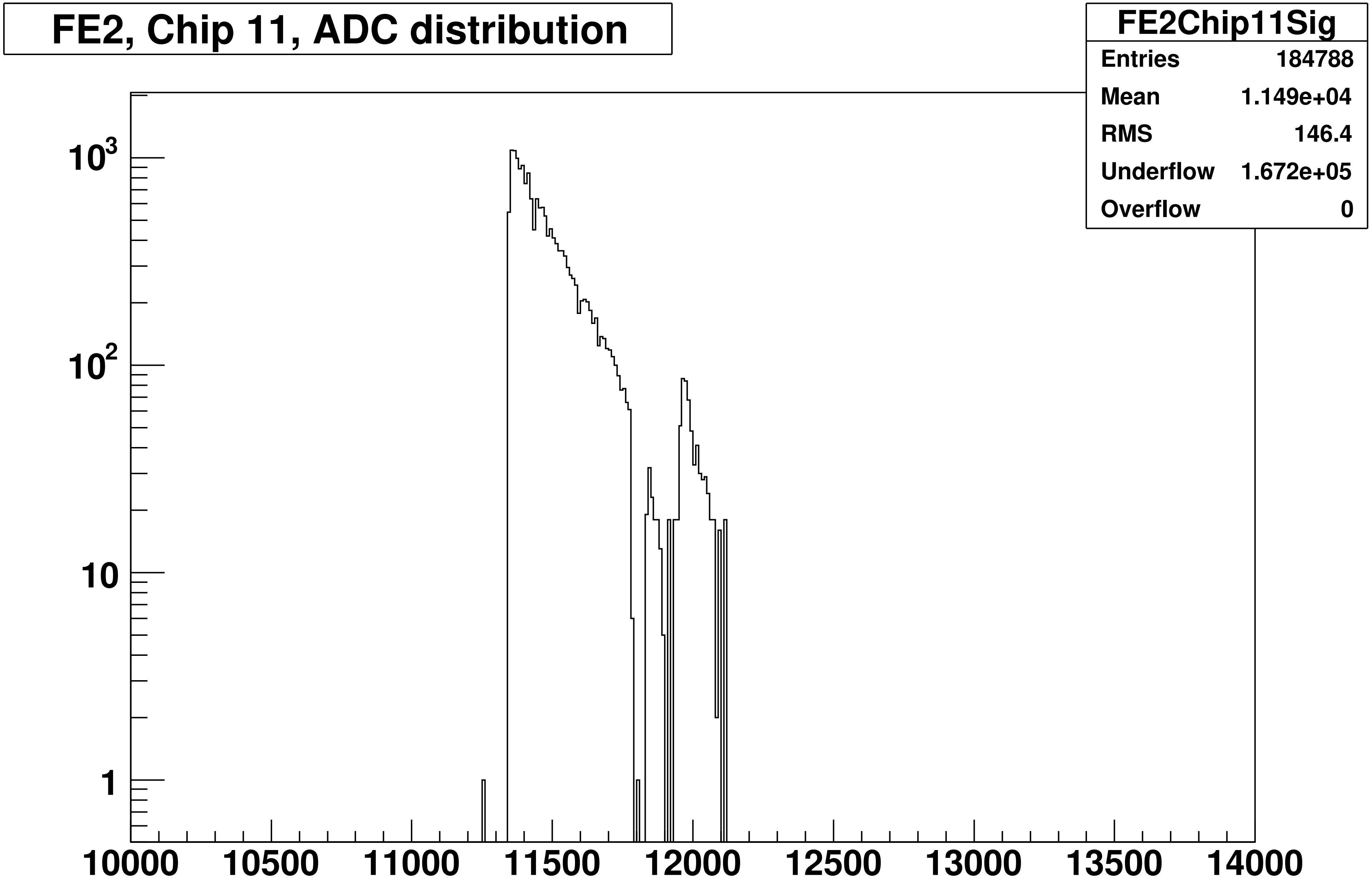

FE2, Chip 11, ADC distribution
FE2Chip11Sig
Entries 184788
Mean 1.149e+04
RMS 146.4
Underflow 1.672e+05
Overflow 0
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10^2
10
1
10000
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11500
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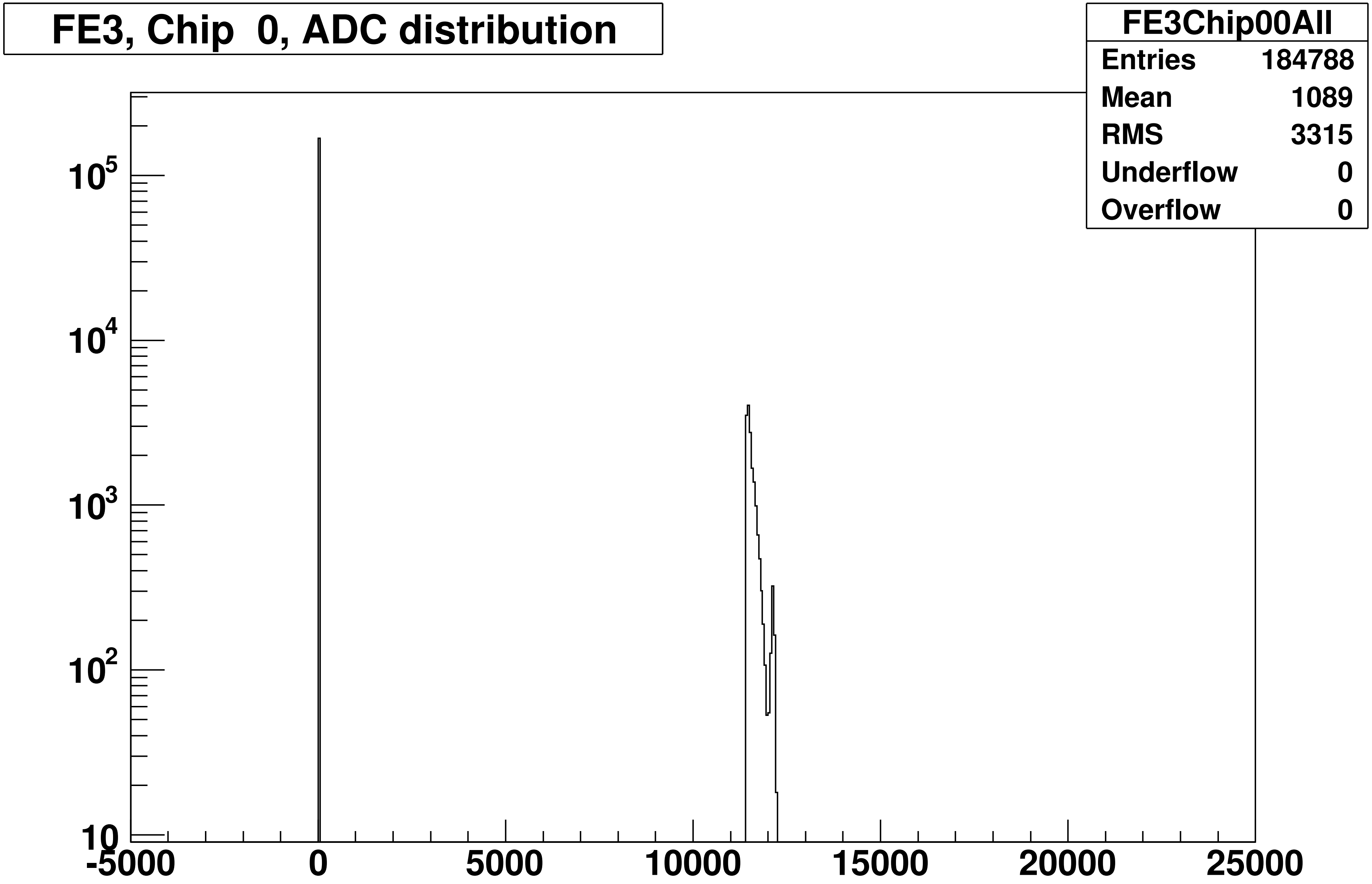
FE3, Chip 0, ADC distribution
FE3Chip00All
Entries 184788
Mean 1089
RMS 3315
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
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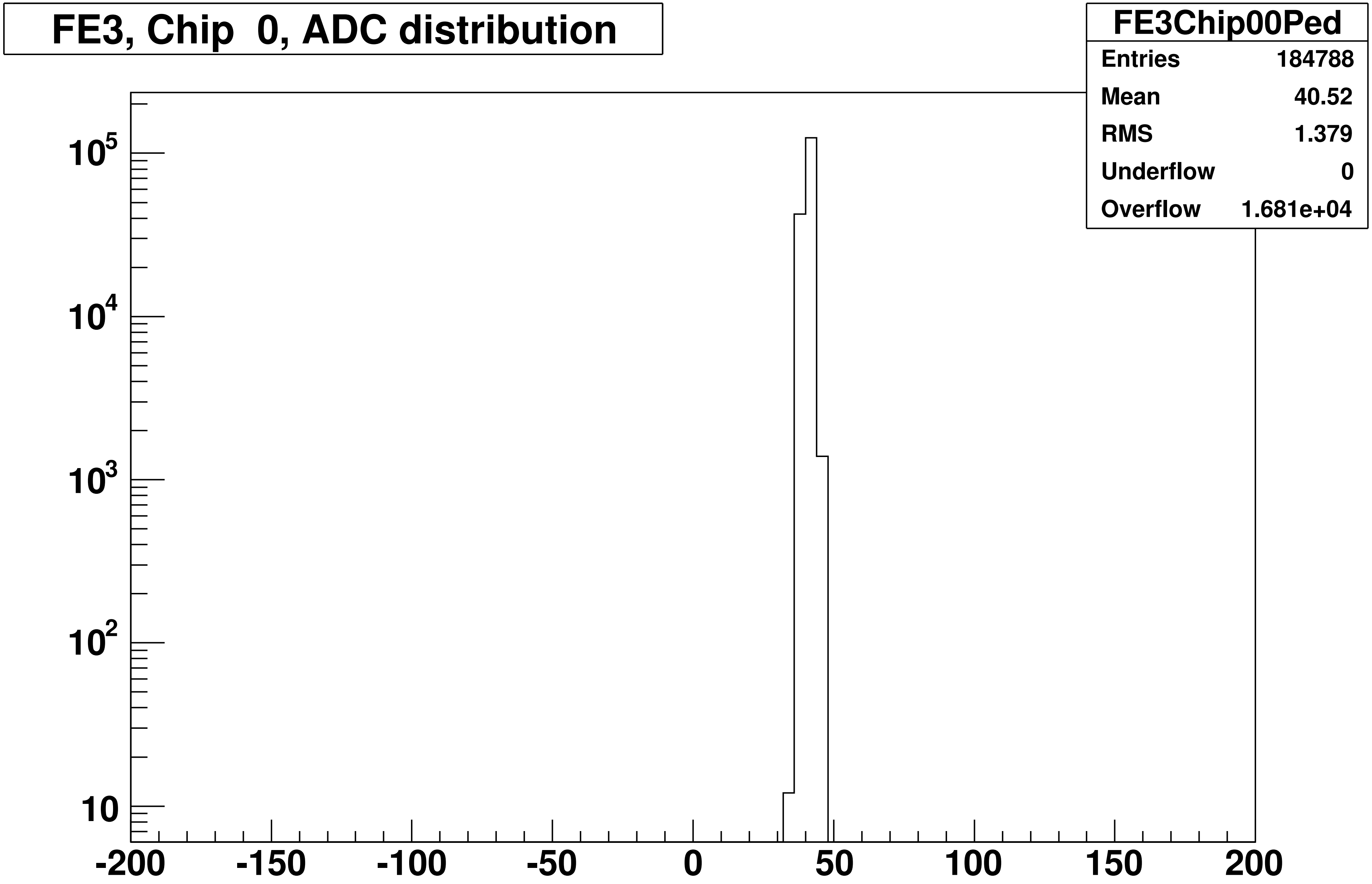
10000
15000
20000
25000


FE3, Chip 0, ADC distribution
FE3Chip00Ped
Entries 184788
Mean 40.52
RMS 1.379
Underflow 0
Overflow 1.681e+04
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10^3
10^4
10^5
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-100
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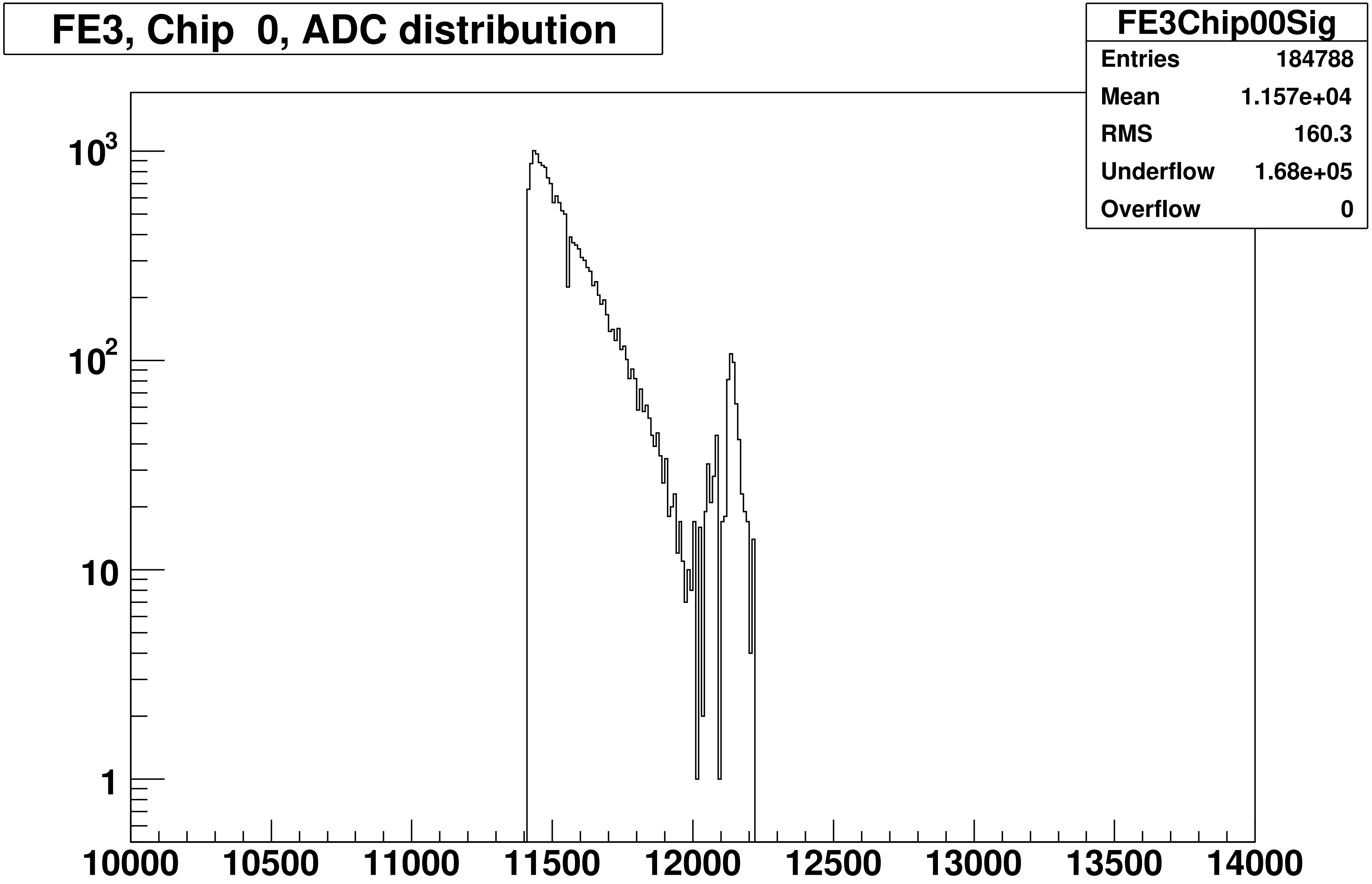
50
100
150
200


FE3, Chip 0, ADC distribution
FE3Chip00Sig
Entries 184788
Mean 1.157e+04
RMS 160.3
Underflow 1.68e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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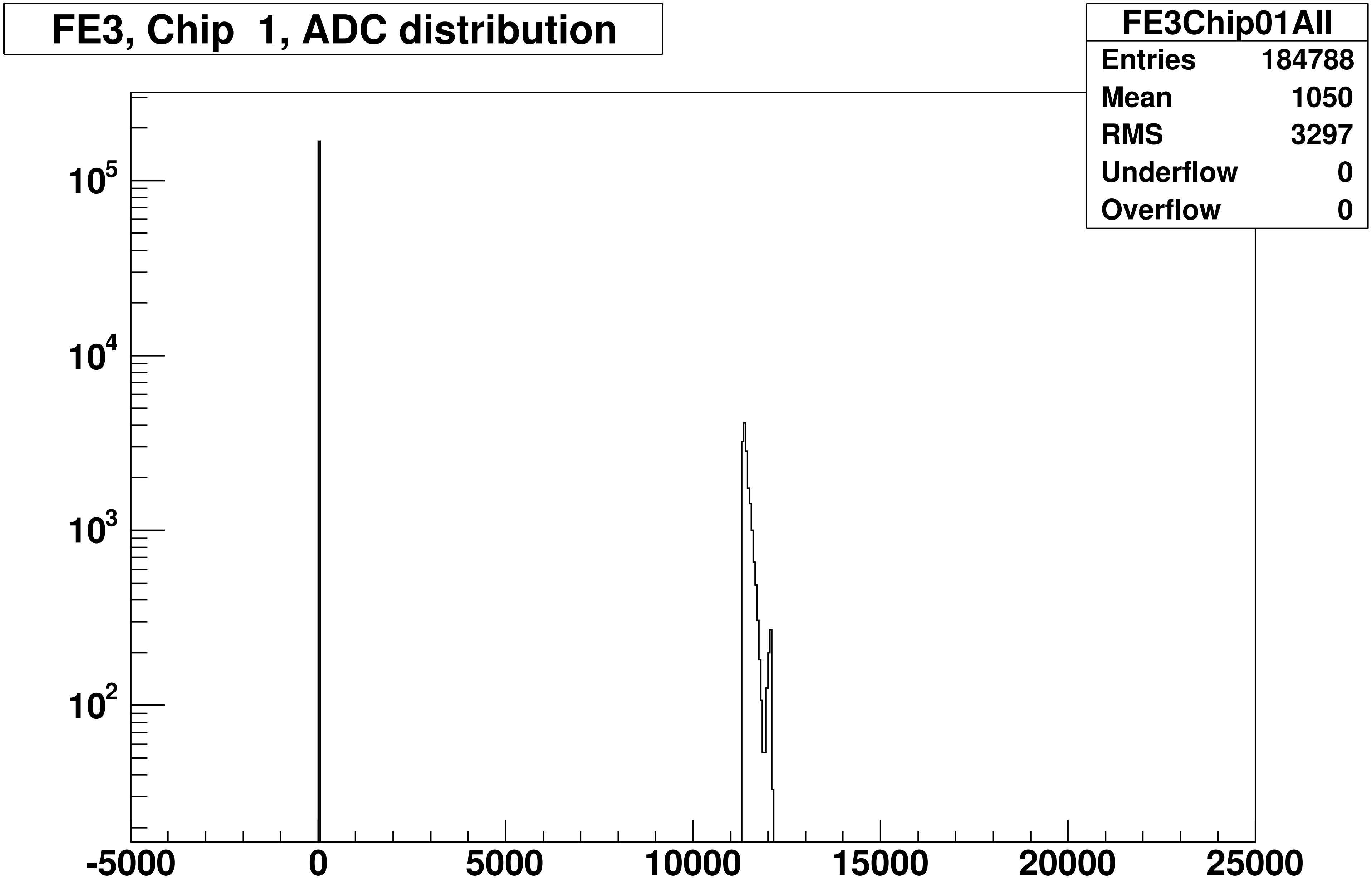
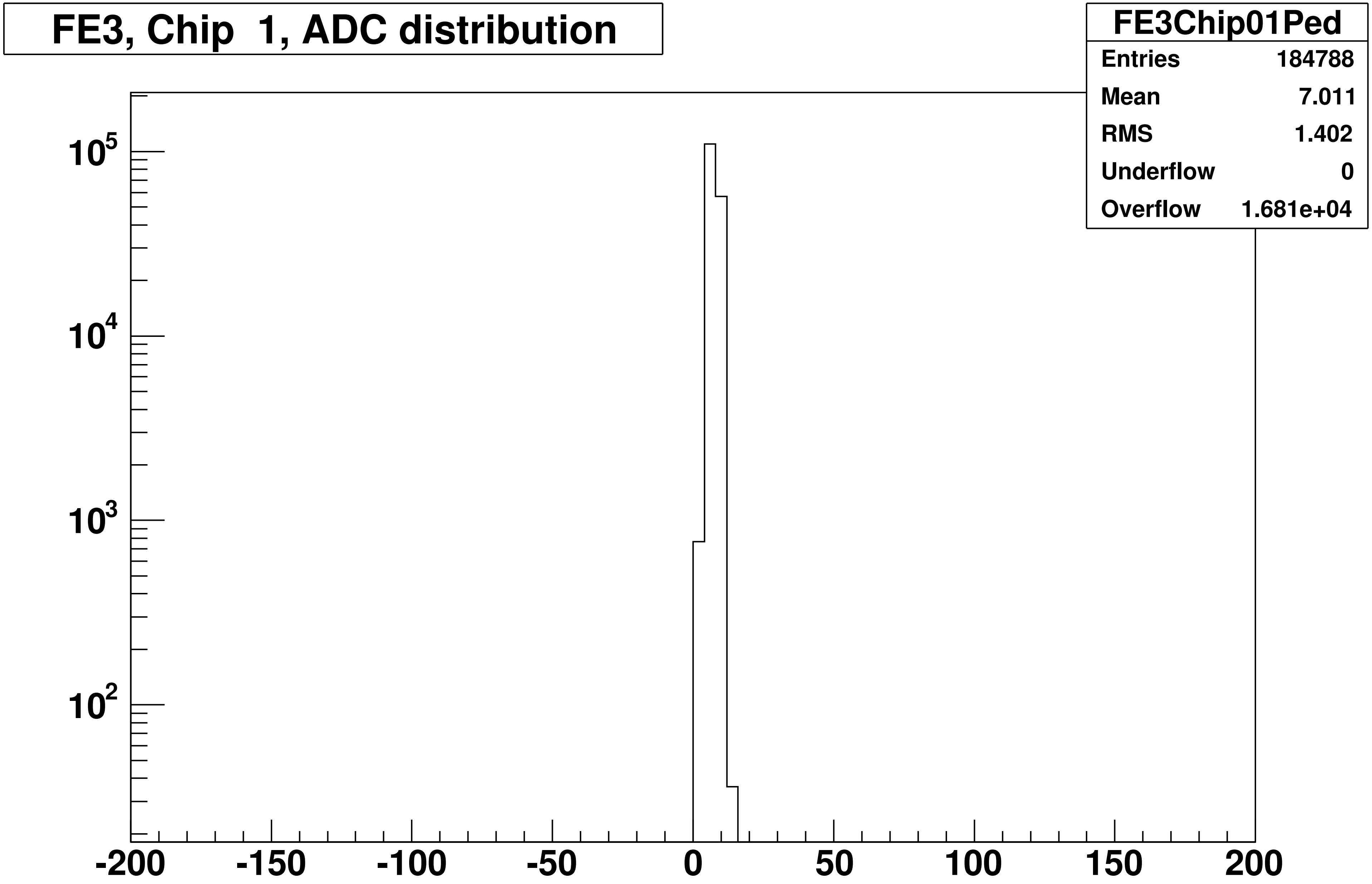

FE3, Chip 1, ADC distribution
FE3Chip01All
Entries 184788
Mean 1050
RMS 3297
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE3, Chip 1, ADC distribution
FE3Chip01Ped
Entries 184788
Mean 7.011
RMS 1.402
Underflow 0
Overflow 1.681e+04
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10^4
10^3
10^2
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-100
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0
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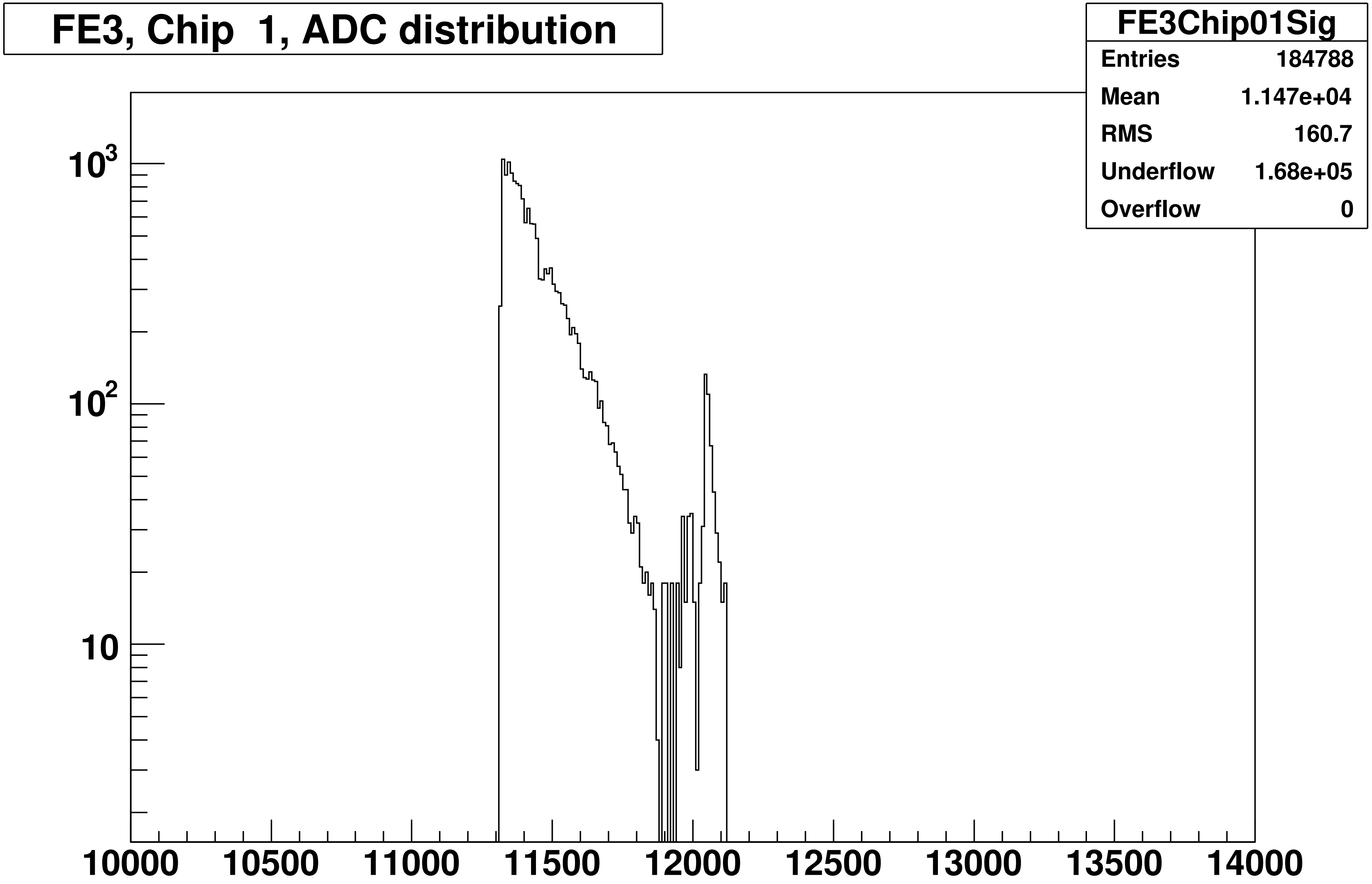
100
150
200


FE3, Chip 1, ADC distribution
FE3Chip01Sig
Entries 184788
Mean 1.147e+04
RMS 160.7
Underflow 1.68e+05
Overflow 0
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10^2
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10000
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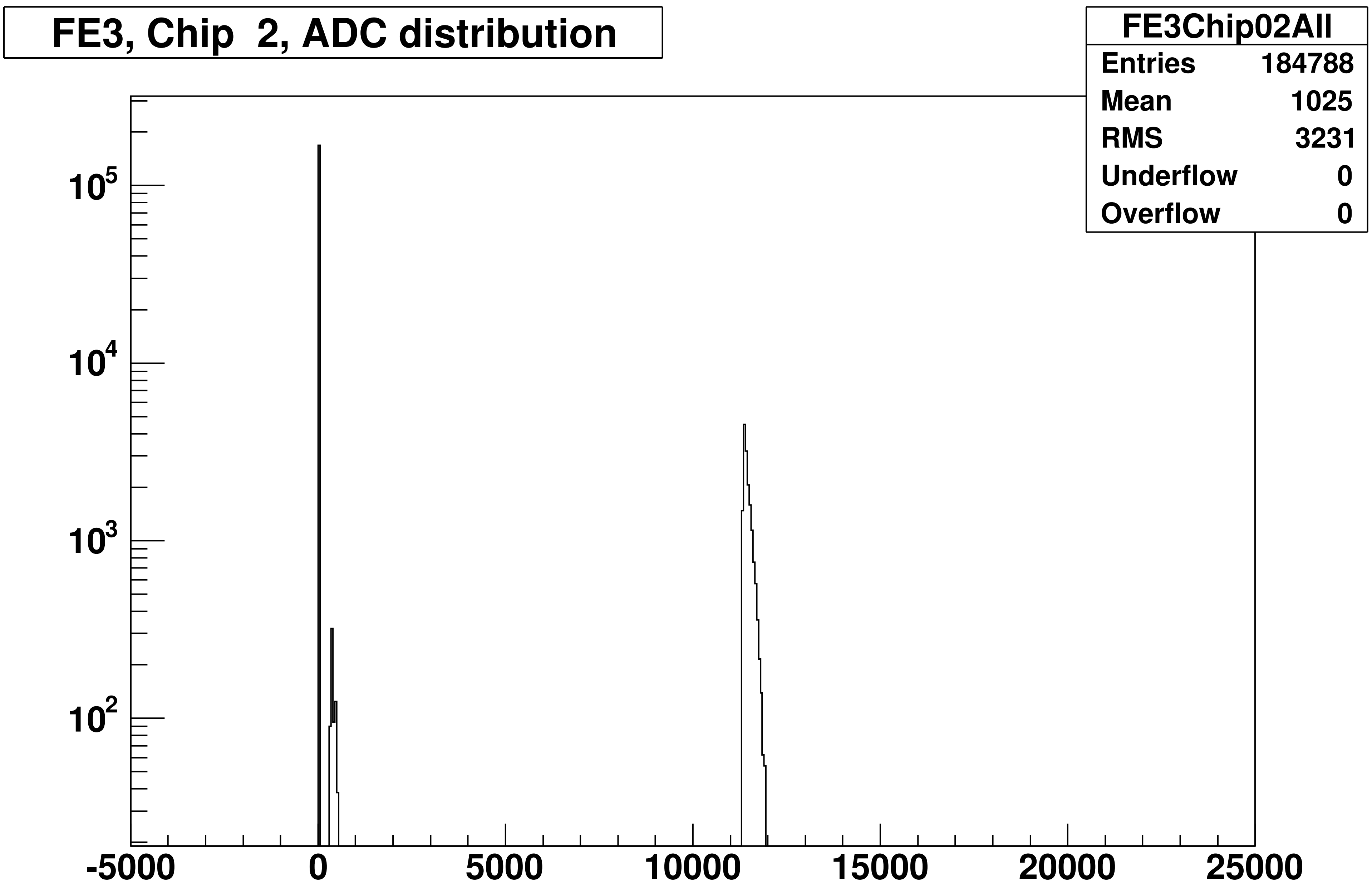
FE3, Chip 2, ADC distribution
FE3Chip02All
Entries 184788
Mean 1025
RMS 3231
Underflow 0
Overflow 0
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10^4
10^3
10^2
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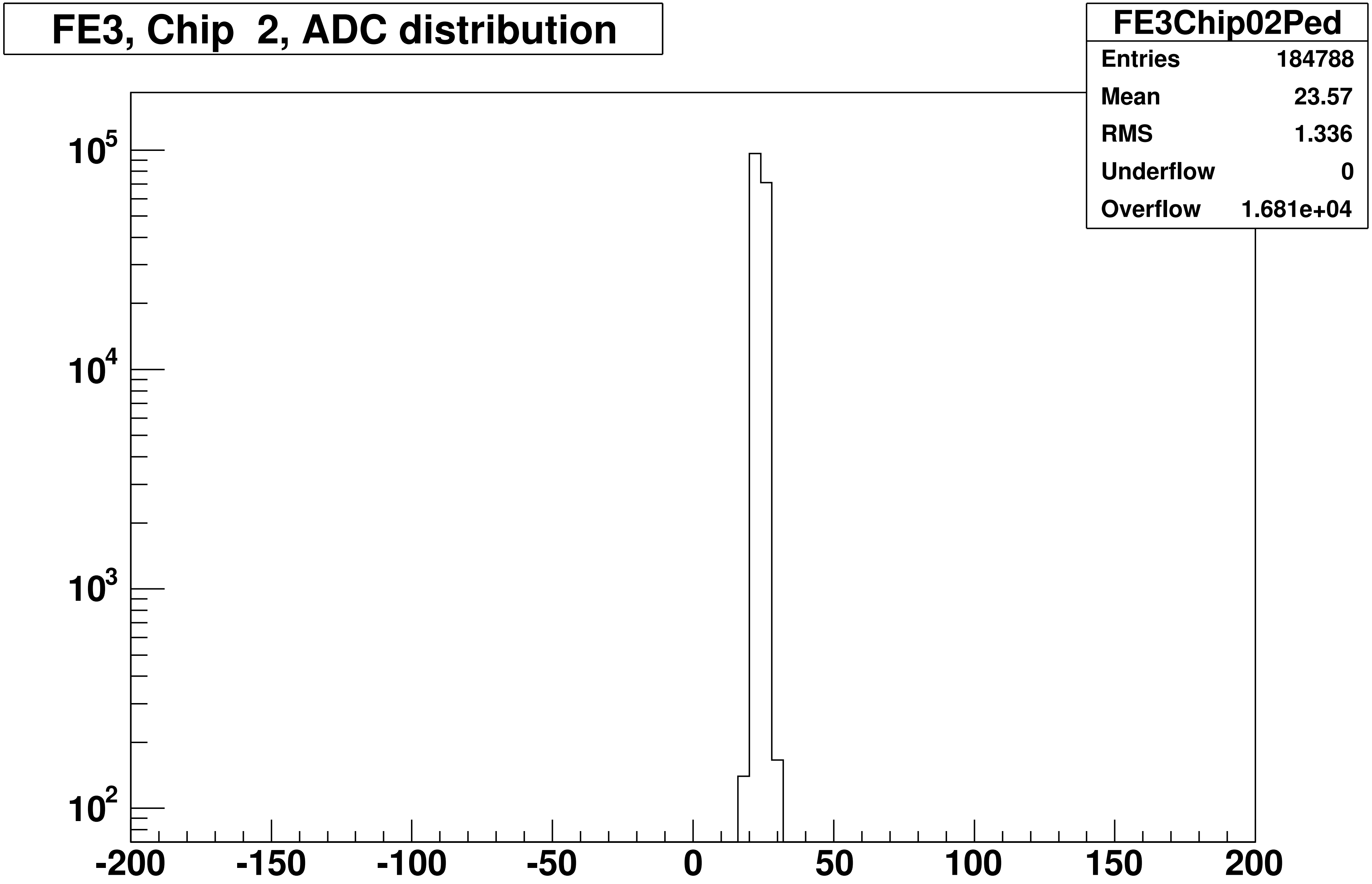
20000
25000



FE3, Chip 2, ADC distribution
FE3Chip02Ped
Entries 184788
Mean 23.57
RMS 1.336
Underflow 0
Overflow 1.681e+04
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10^4
10^3
10^2
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-100
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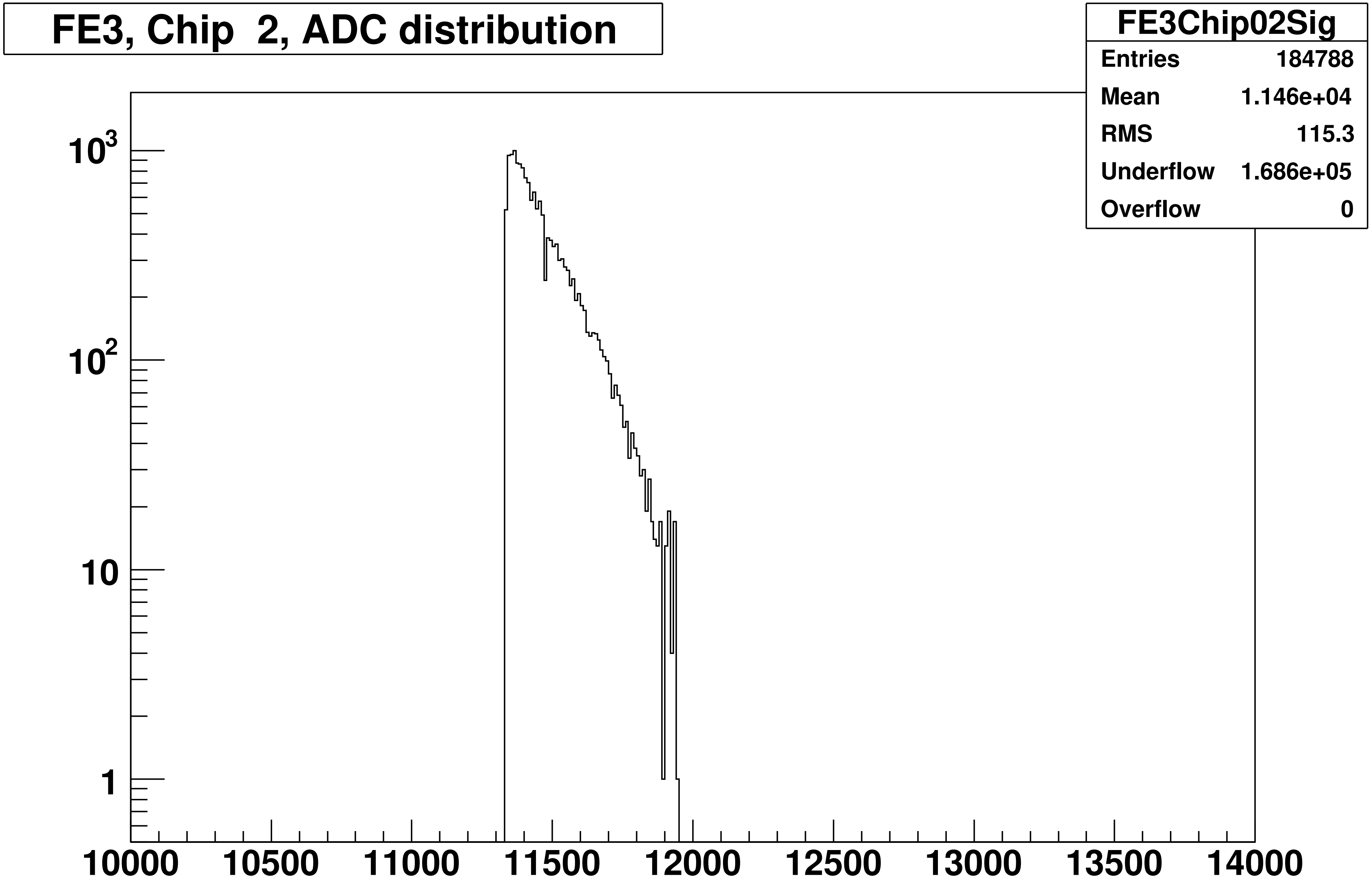
0
50
100
150
200


FE3, Chip 2, ADC distribution
FE3Chip02Sig
Entries 184788
Mean 1.146e+04
RMS 115.3
Underflow 1.686e+05
Overflow 0
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10^2
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10000
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11500
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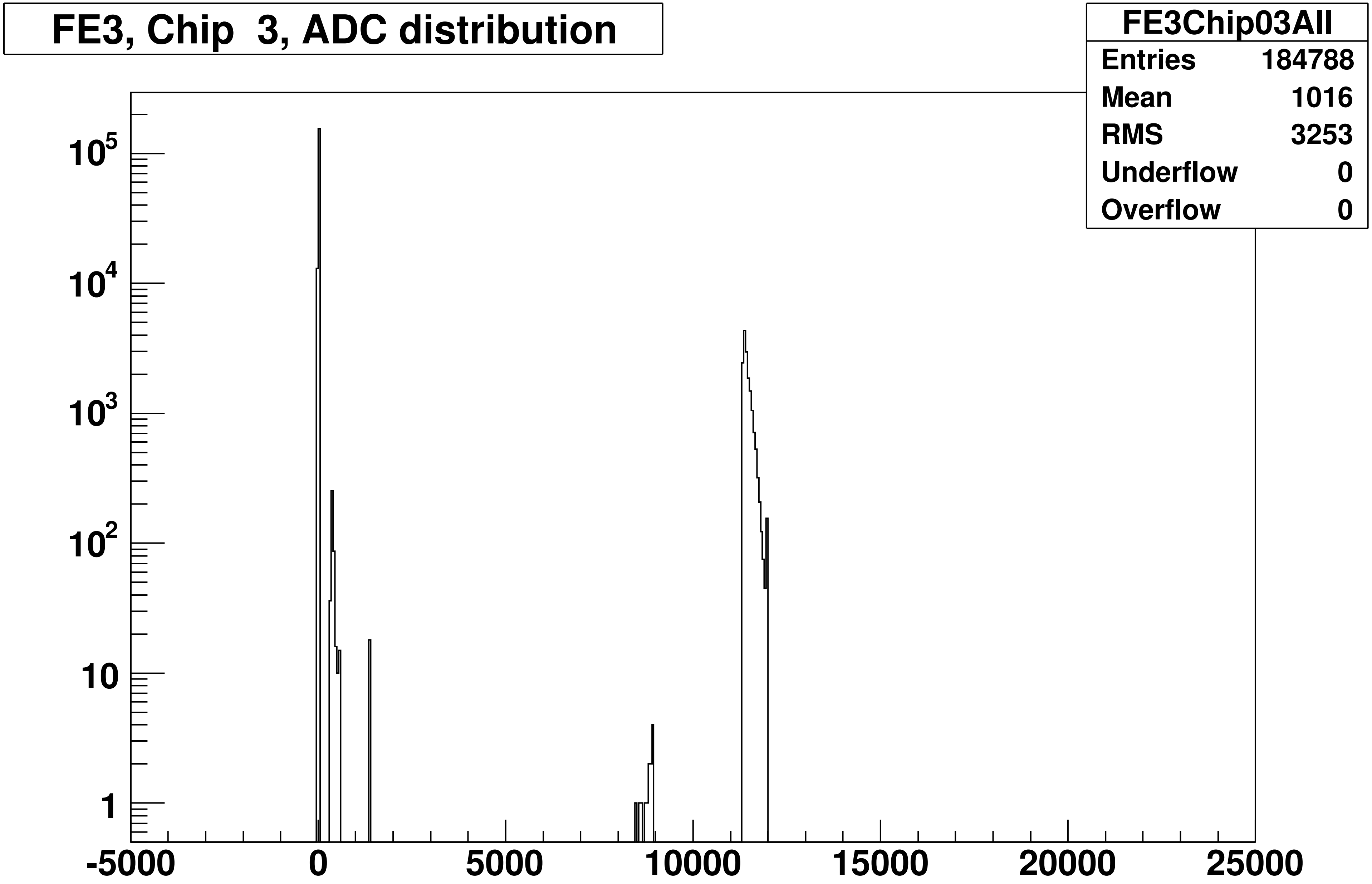

FE3, Chip 3, ADC distribution
FE3Chip03All
Entries 184788
Mean 1016
RMS 3253
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
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5000
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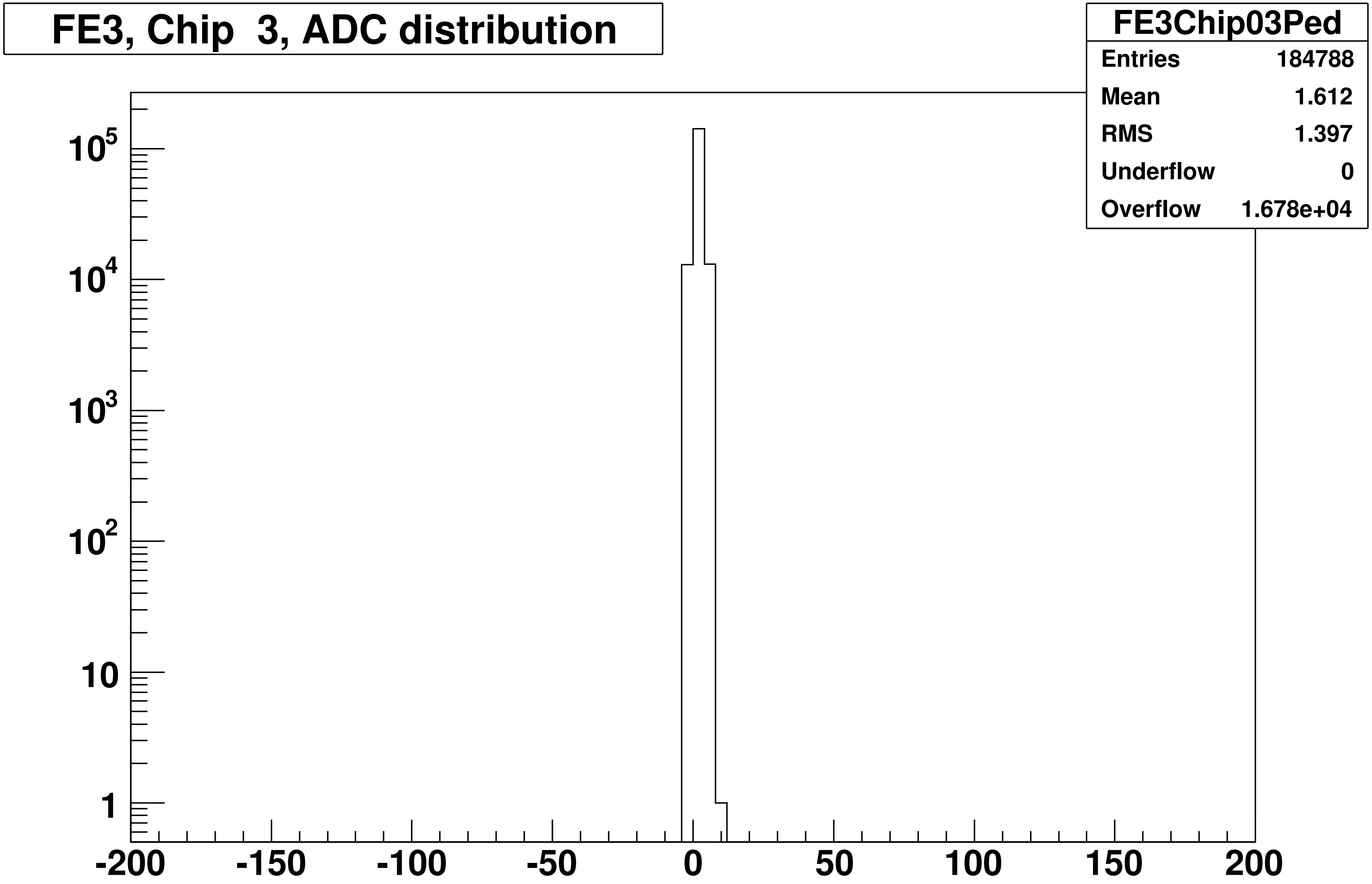
25000


FE3, Chip 3, ADC distribution
FE3Chip03Ped
Entries 184788
Mean 1.612
RMS 1.397
Underflow 0
Overflow 1.678e+04
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10^3
10^2
10
1
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150
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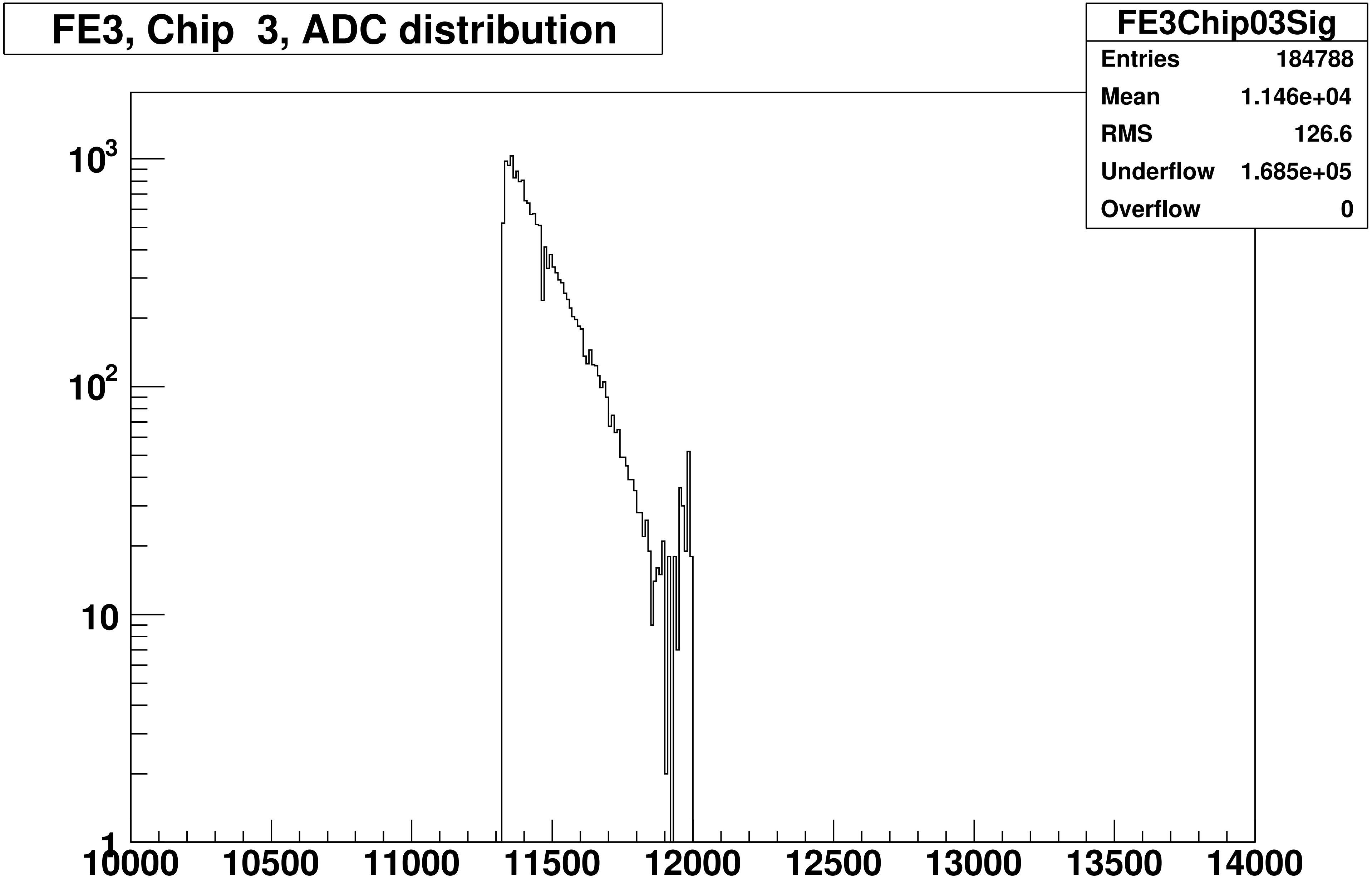
FE3, Chip 3, ADC distribution
FE3Chip03Sig
Entries 184788
Mean 1.146e+04
RMS 126.6
Underflow 1.685e+05
Overflow 0
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10^2
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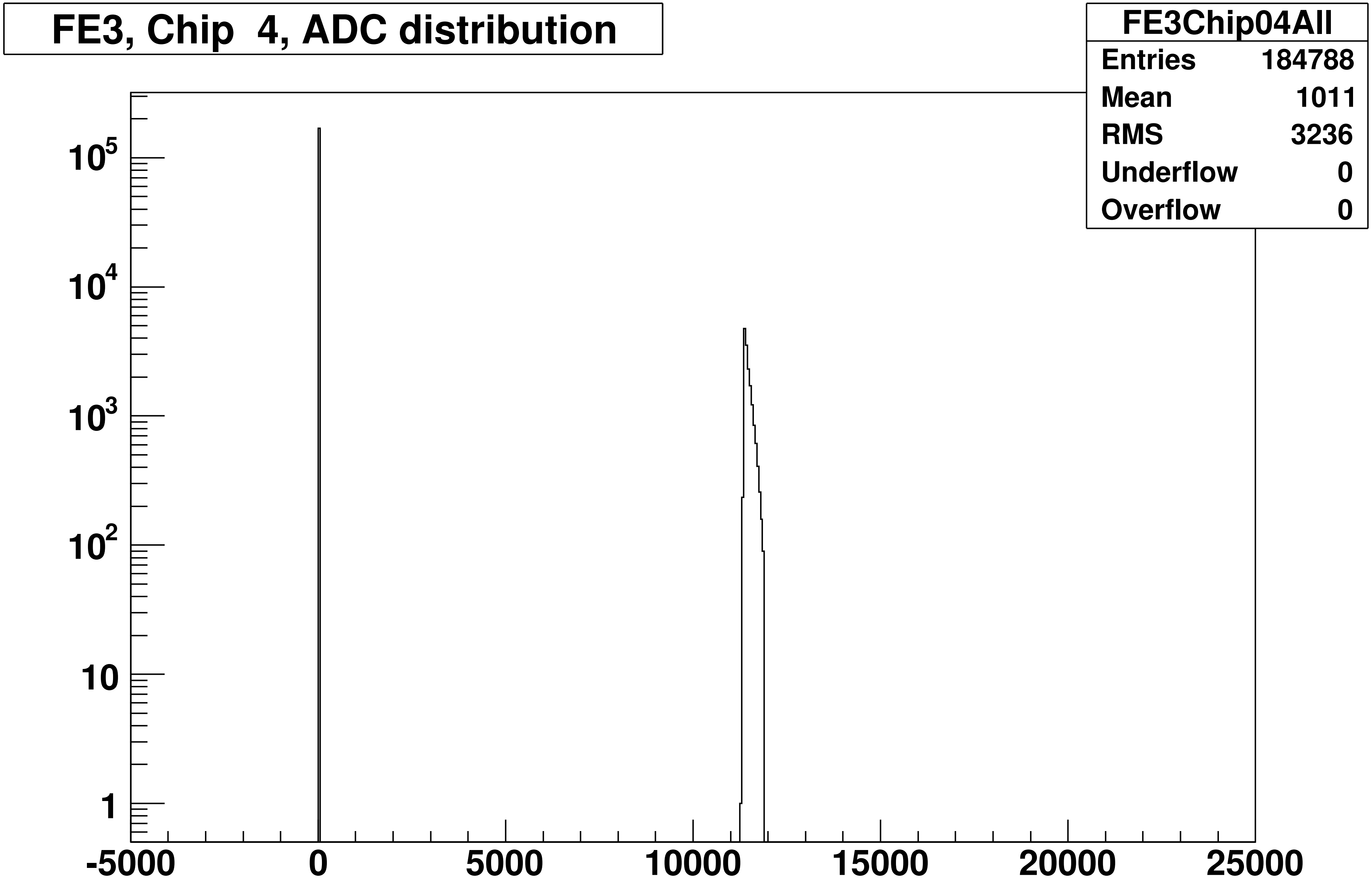
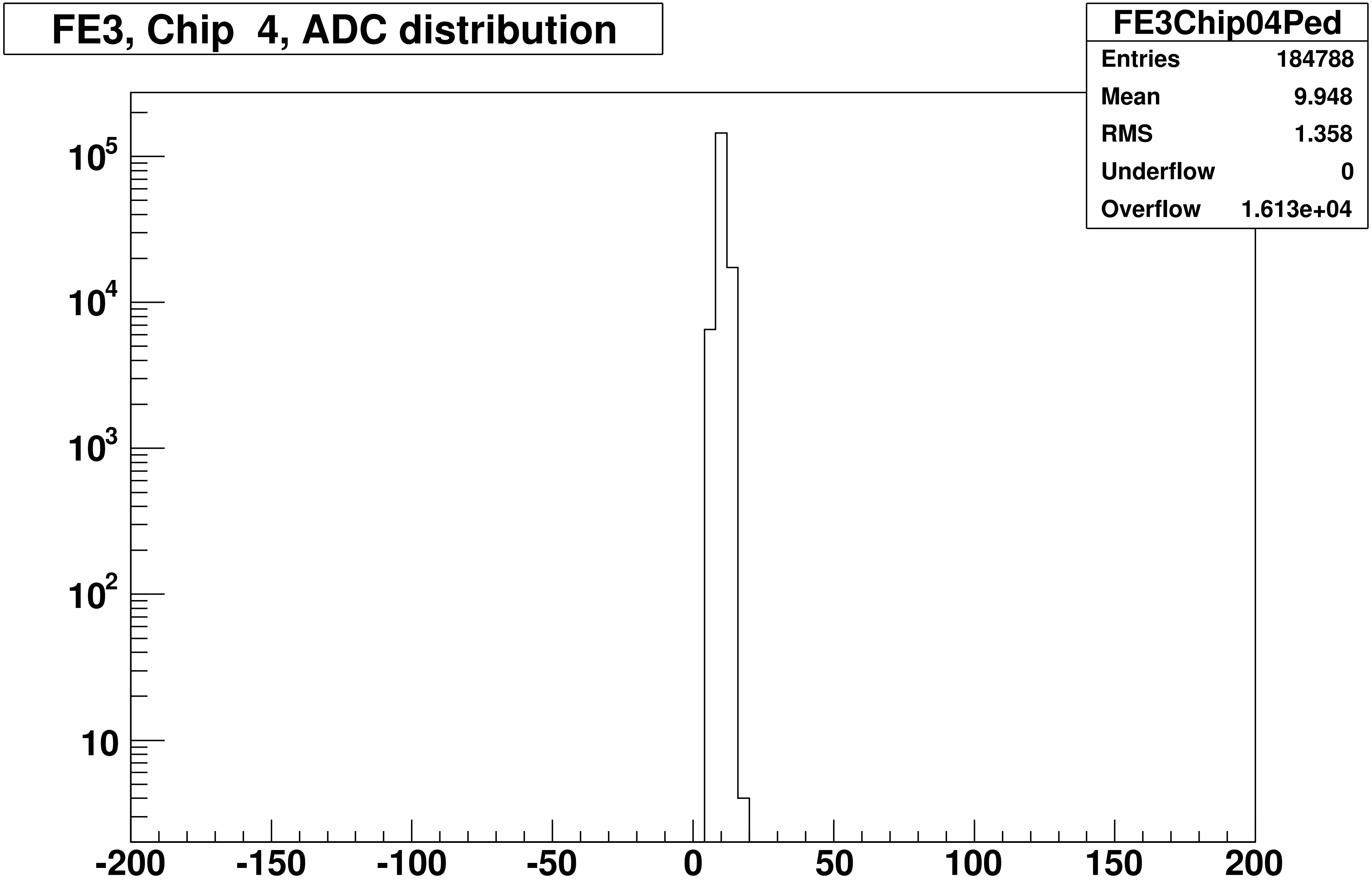

FE3, Chip 4, ADC distribution
FE3Chip04All
Entries 184788
Mean 1011
RMS 3236
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 4, ADC distribution
FE3Chip04Ped
Entries 184788
Mean 9.948
RMS 1.358
Underflow 0
Overflow 1.613e+04
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10^4
10^3
10^2
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150
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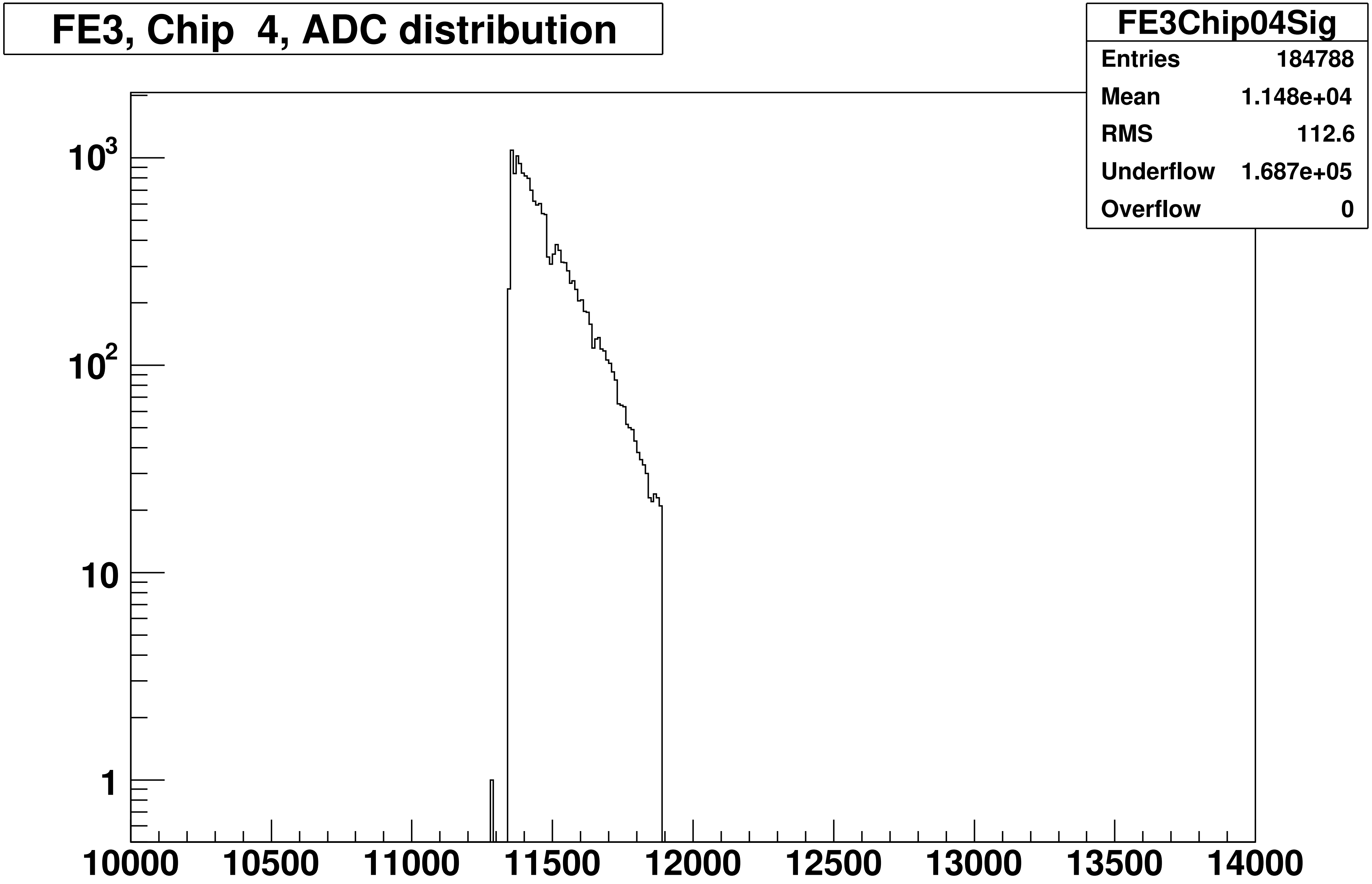
FE3, Chip 4, ADC distribution
FE3Chip04Sig
Entries 184788
Mean 1.148e+04
RMS 112.6
Underflow 1.687e+05
Overflow 0
10^3
10^2
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1
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10500
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11500
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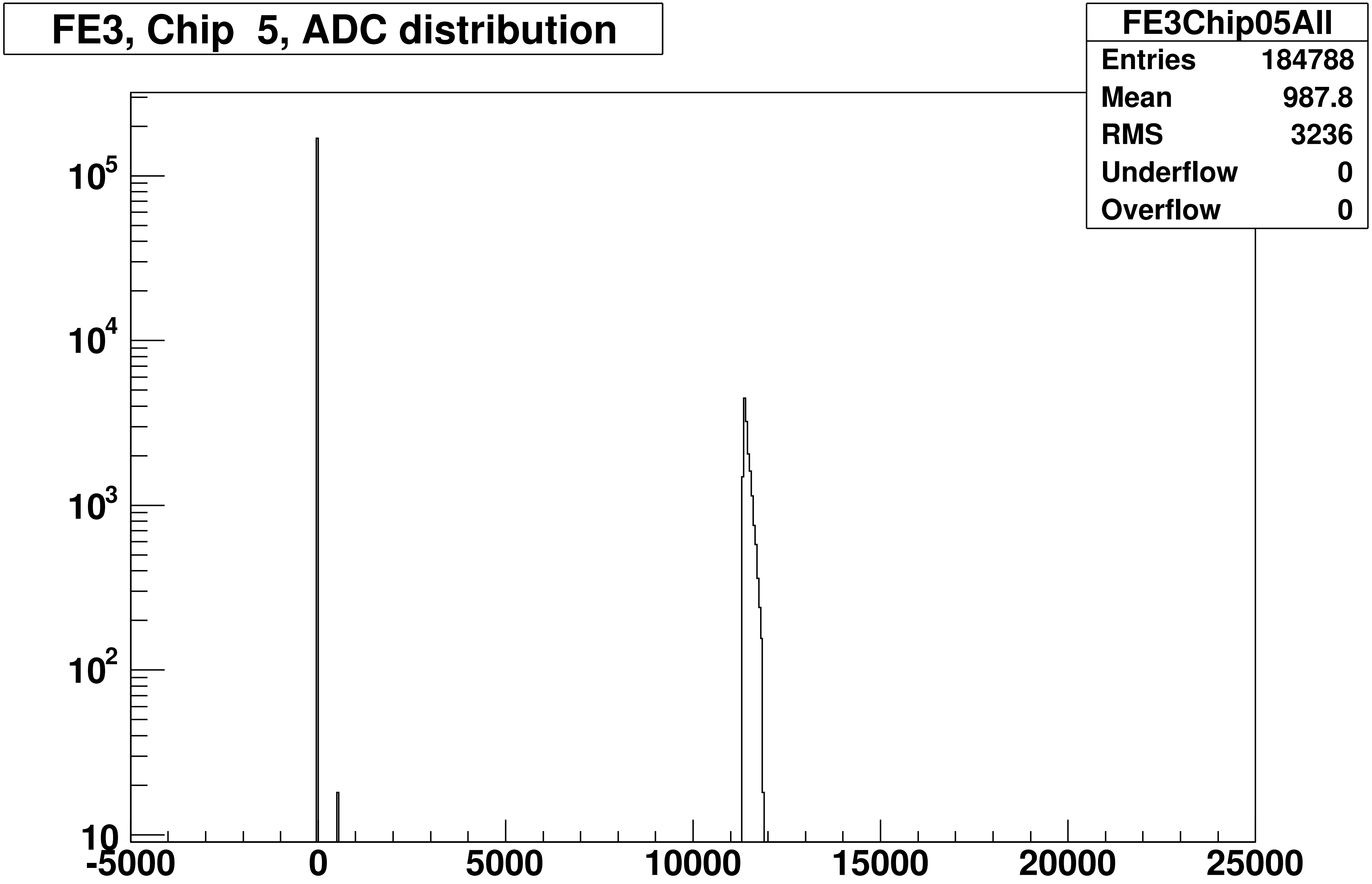
14000


FE3, Chip 5, ADC distribution
FE3Chip05All
Entries 184788
Mean 987.8
RMS 3236
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
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0
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10000
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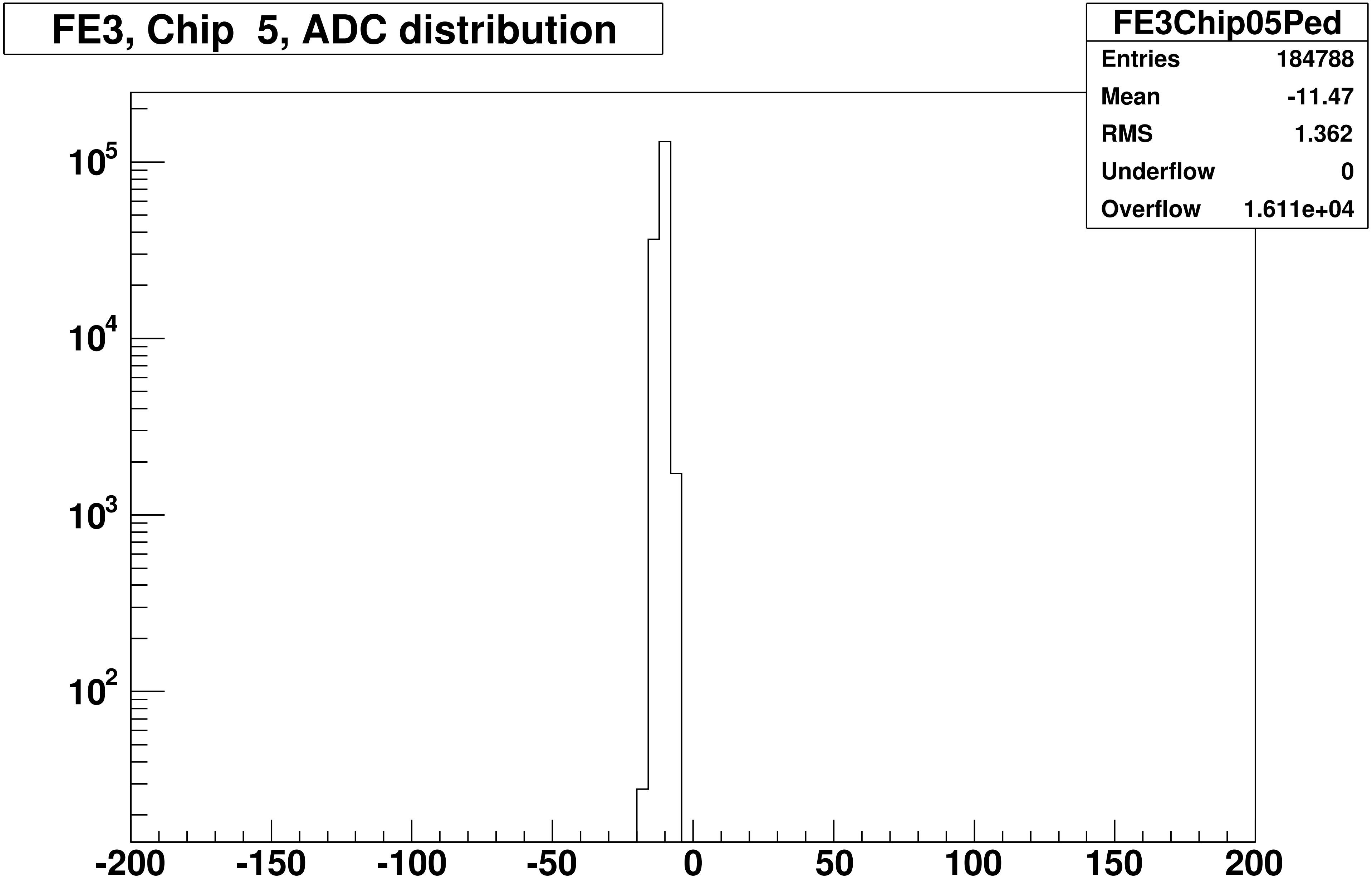
20000
25000


FE3, Chip 5, ADC distribution
FE3Chip05Ped
Entries 184788
Mean -11.47
RMS 1.362
Underflow 0
Overflow 1.611e+04
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10^4
10^3
10^2
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150
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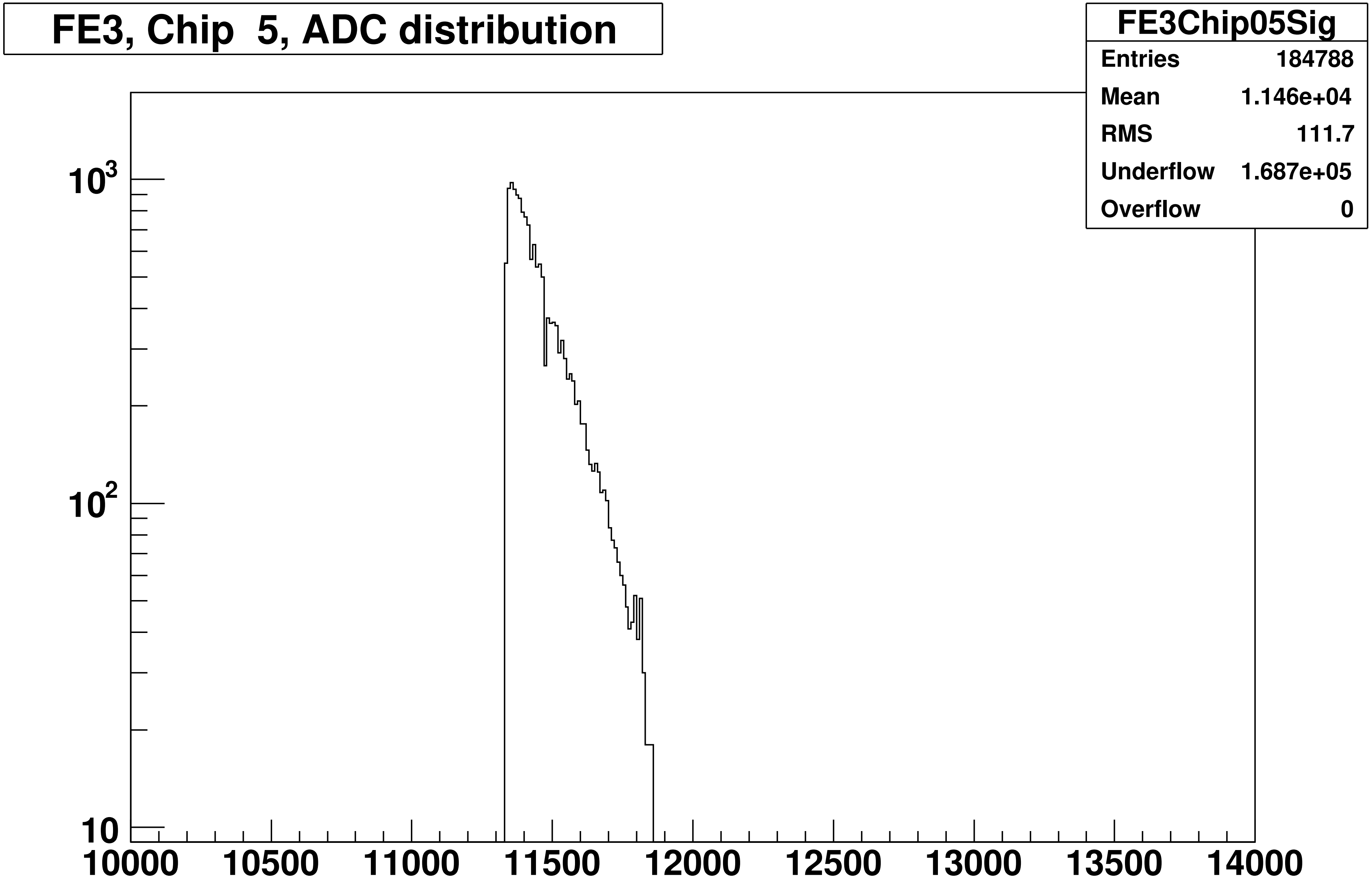

FE3, Chip 5, ADC distribution
FE3Chip05Sig
Entries 184788
Mean 1.146e+04
RMS 111.7
Underflow 1.687e+05
Overflow 0
10^3
10^2
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10000
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11500
12000
12500
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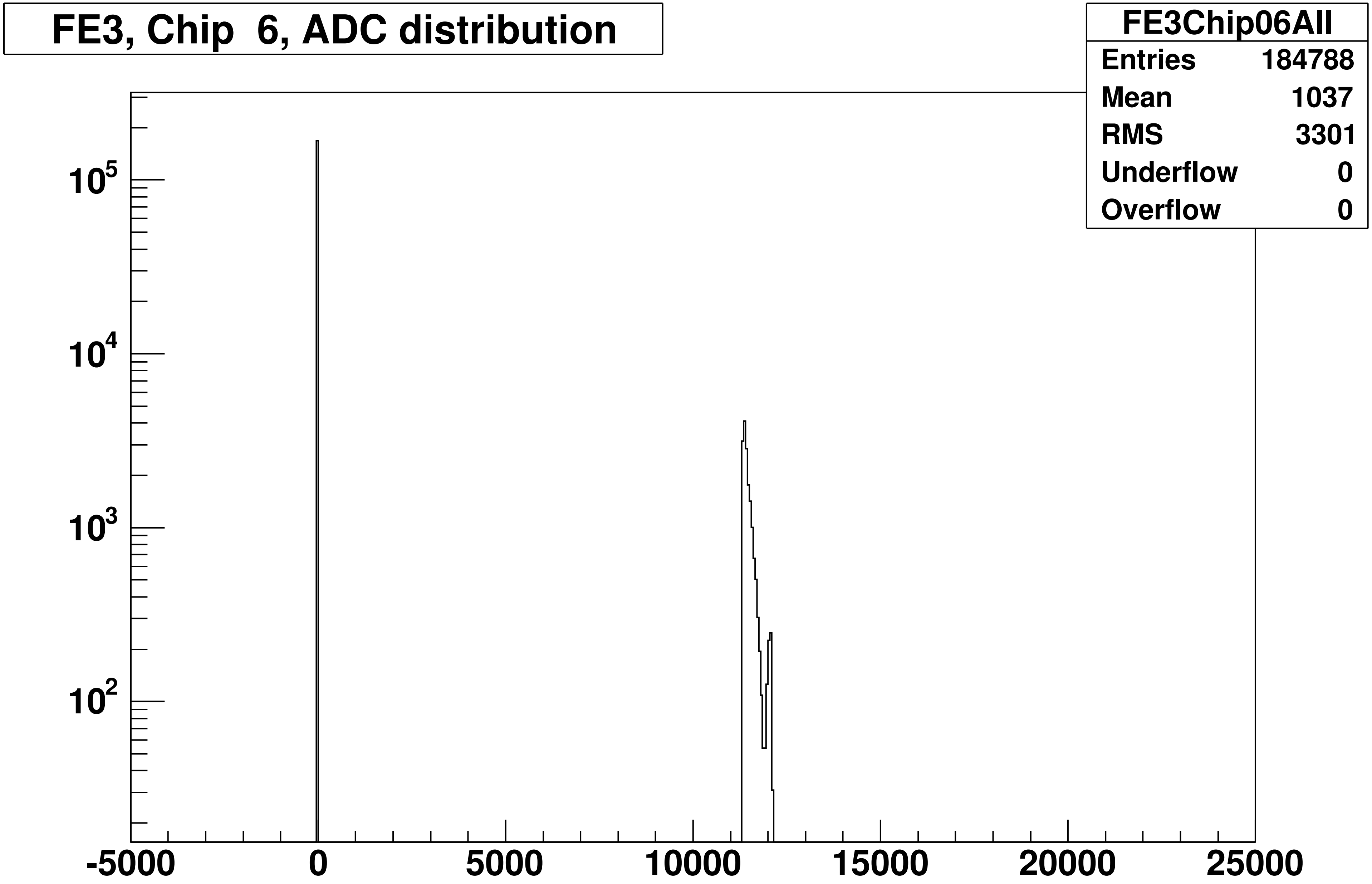
14000


FE3, Chip 6, ADC distribution
FE3Chip06All
Entries 184788
Mean 1037
RMS 3301
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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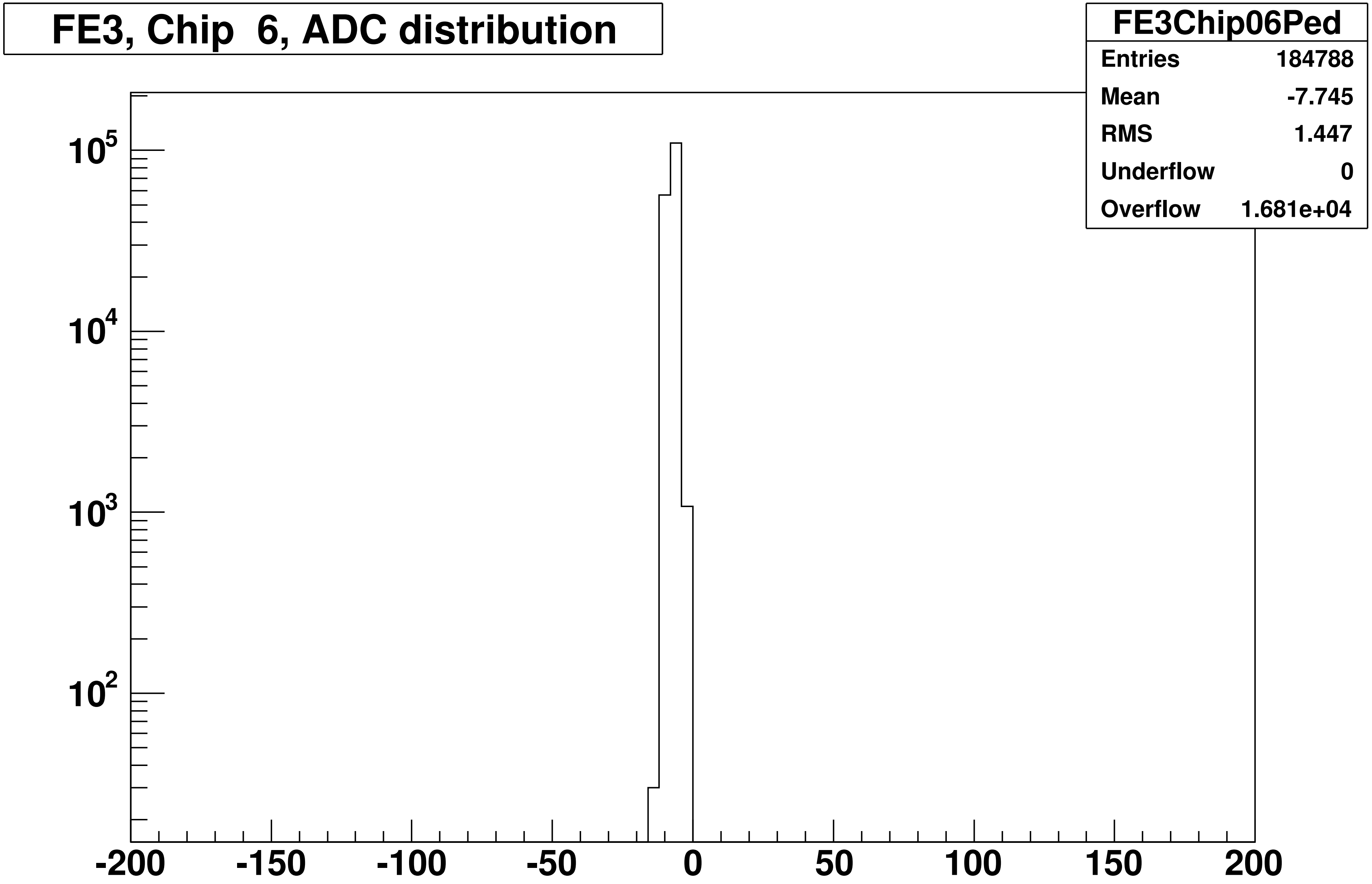
FE3, Chip 6, ADC distribution
FE3Chip06Ped
Entries 184788
Mean -7.745
RMS 1.447
Underflow 0
Overflow 1.681e+04
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10^4
10^3
10^2
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-100
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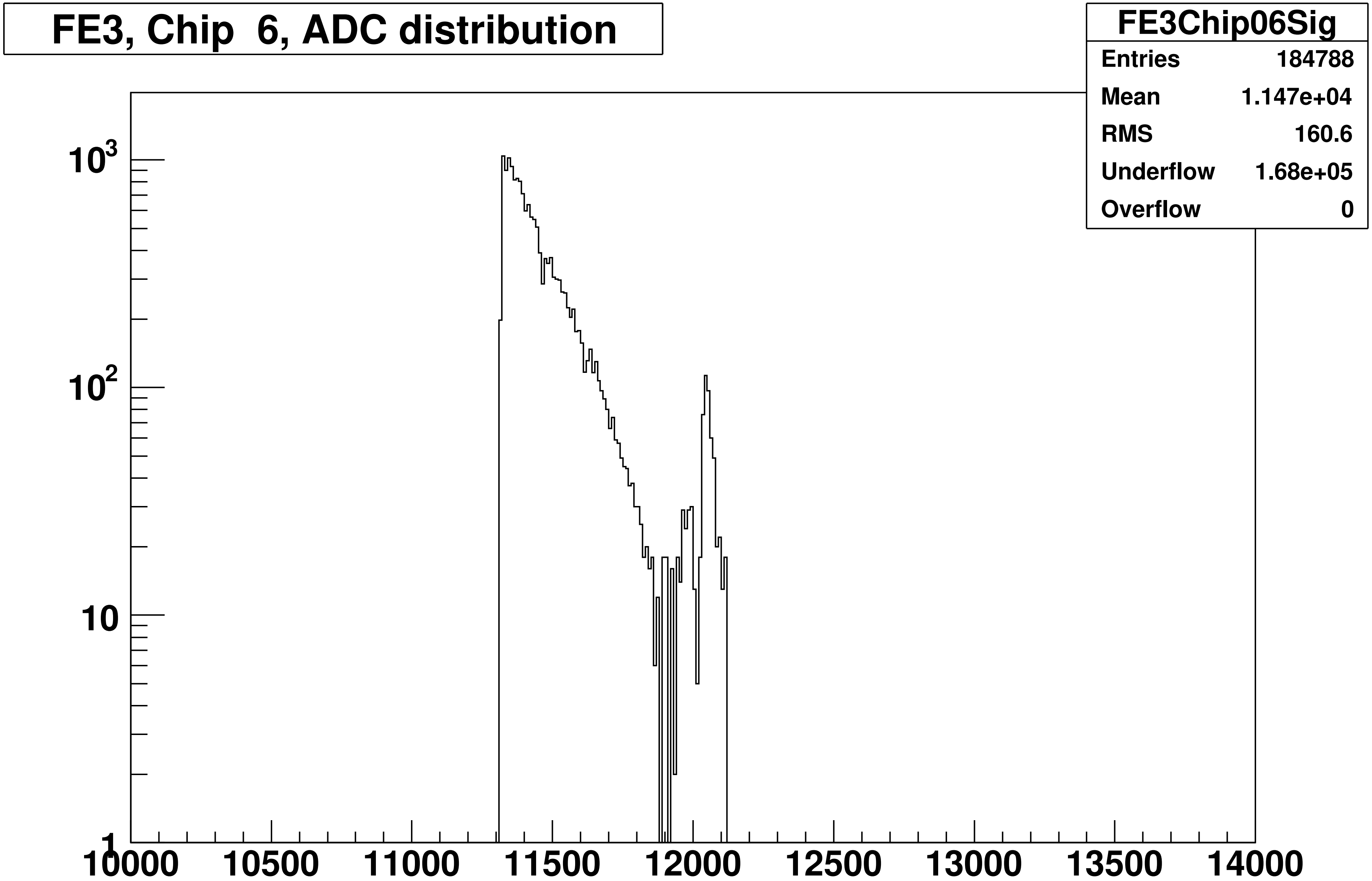
100
150
200


FE3, Chip 6, ADC distribution
FE3Chip06Sig
Entries 184788
Mean 1.147e+04
RMS 160.6
Underflow 1.68e+05
Overflow 0
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10^2
10
1
10000
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11500
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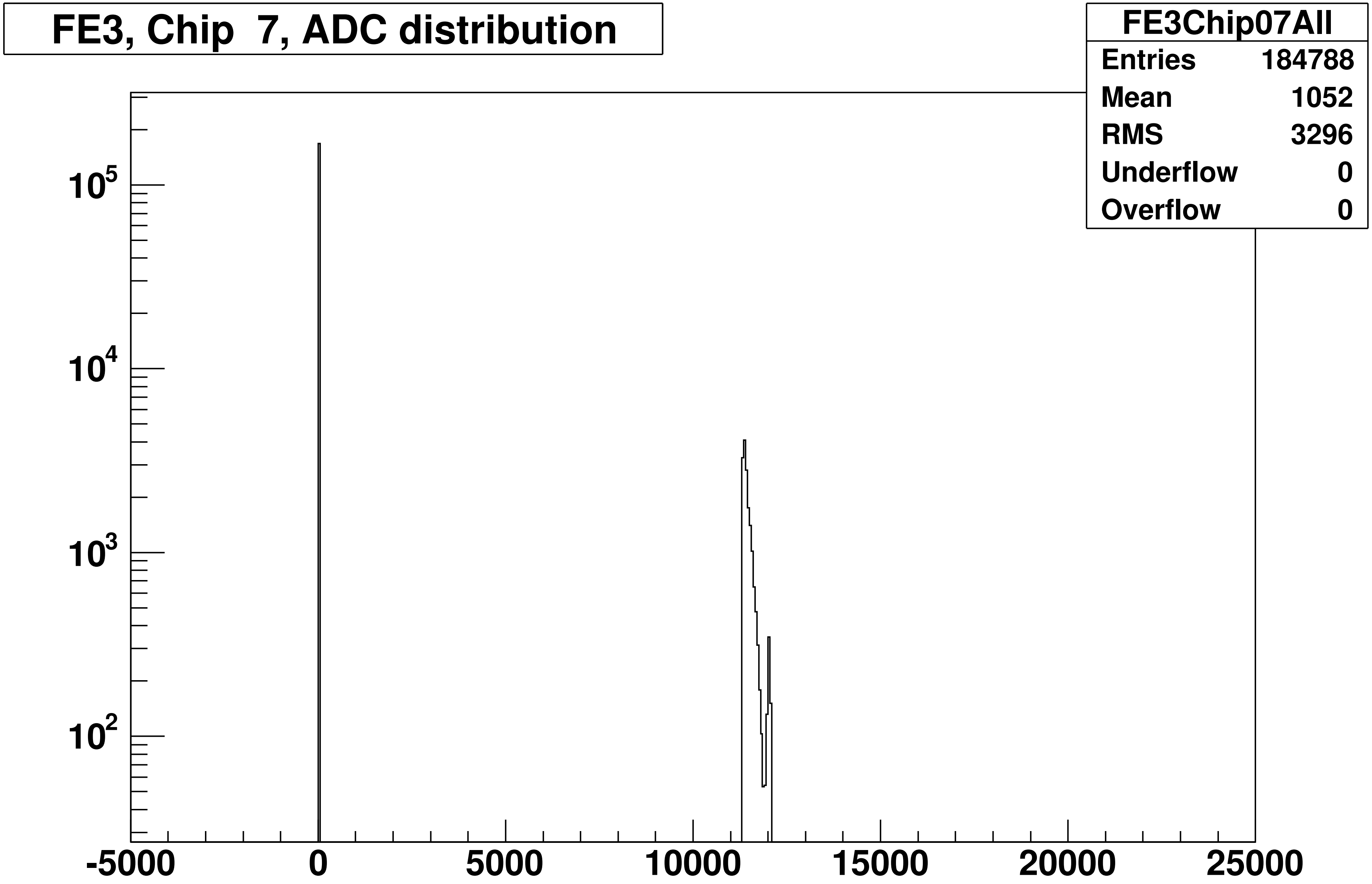
FE3, Chip 7, ADC distribution
FE3Chip07All
Entries 184788
Mean 1052
RMS 3296
Underflow 0
Overflow 0
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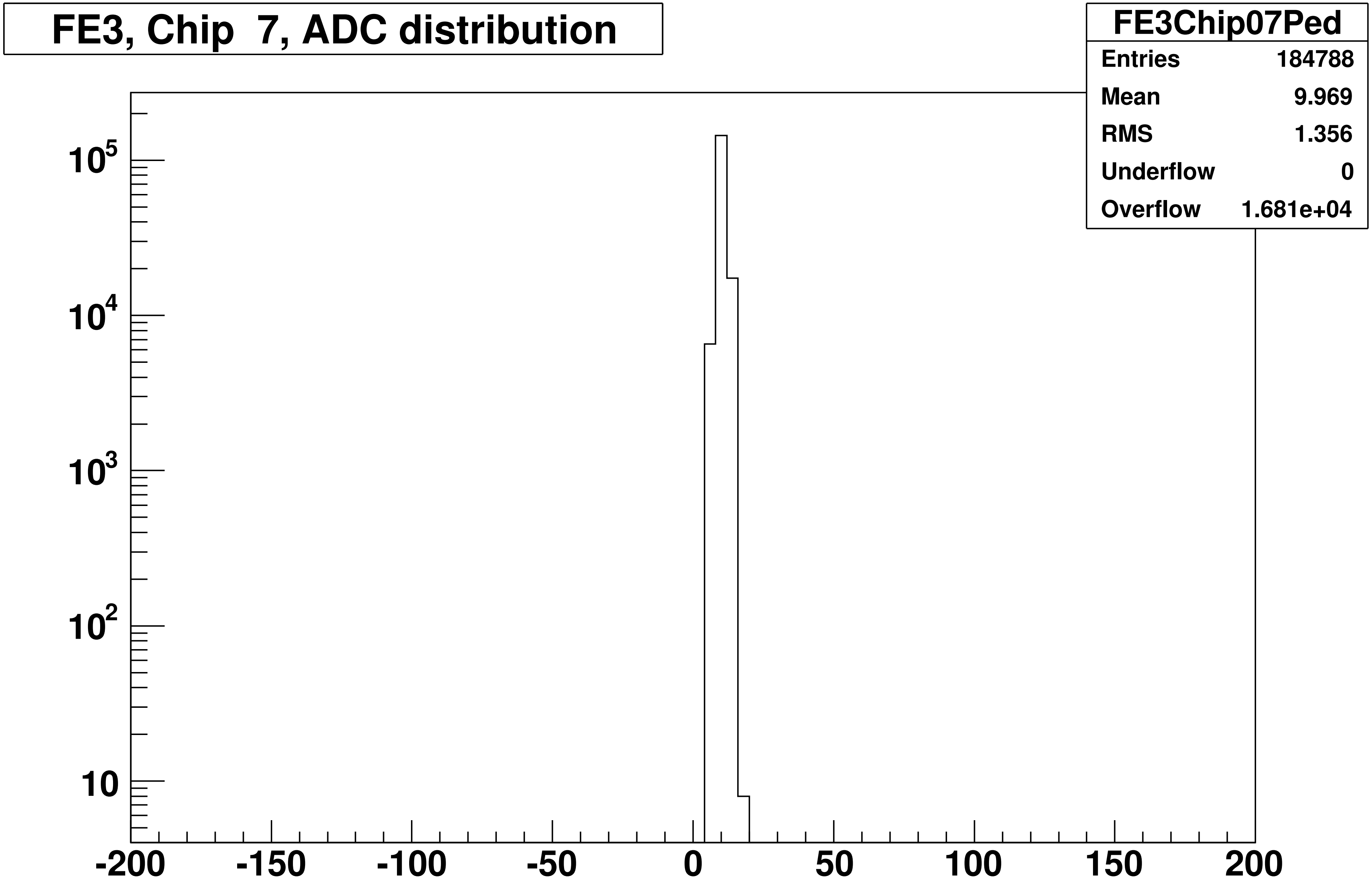
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE3, Chip 7, ADC distribution
FE3Chip07Ped
Entries 184788
Mean 9.969
RMS 1.356
Underflow 0
Overflow 1.681e+04
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10^4
10^3
10^2
10
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-100
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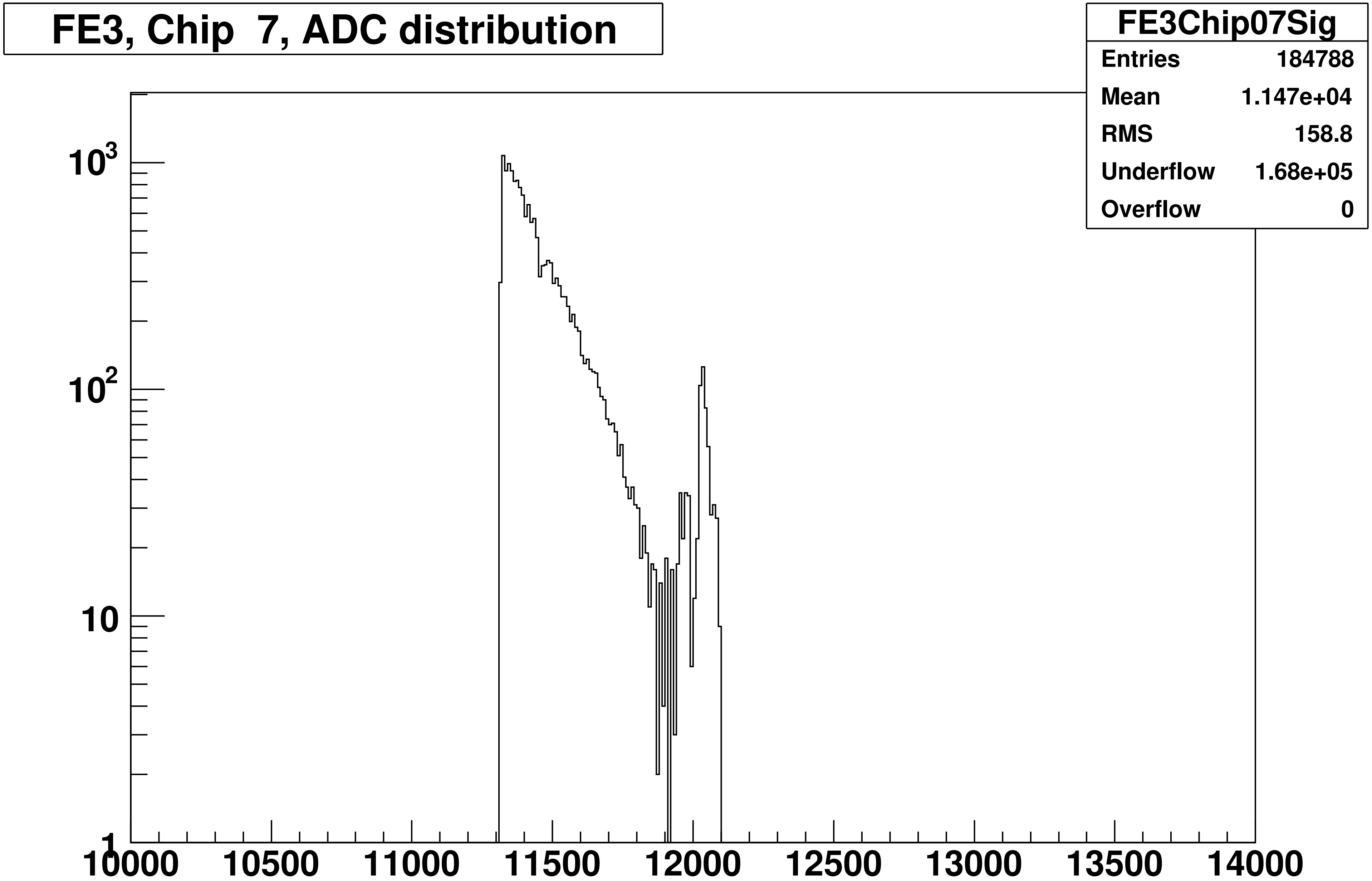
FE3, Chip 7, ADC distribution
FE3Chip07Sig
Entries 184788
Mean 1.147e+04
RMS 158.8
Underflow 1.68e+05
Overflow 0
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10^2
10
1
10000
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11500
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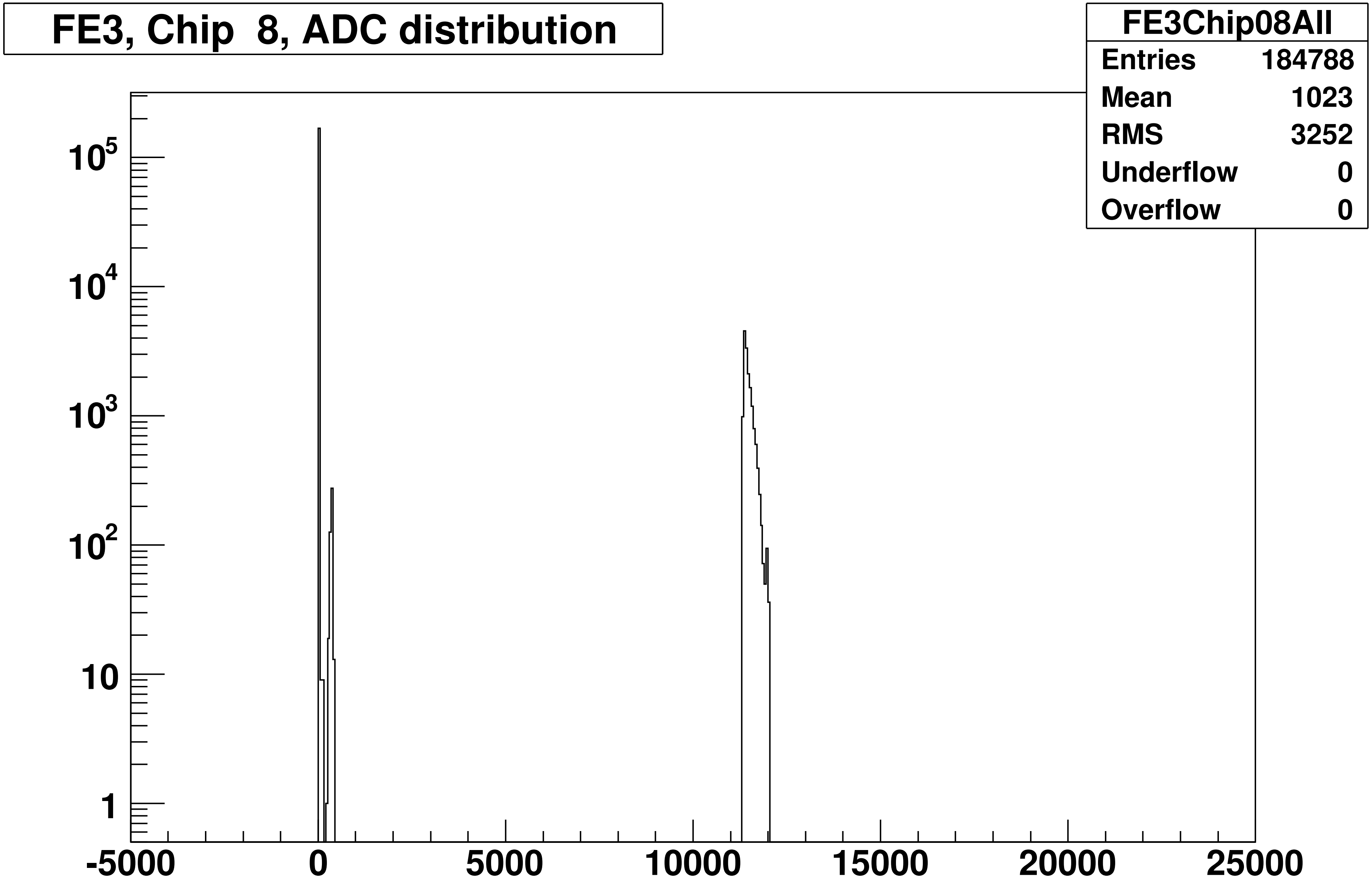
FE3, Chip 8, ADC distribution
FE3Chip08All
Entries 184788
Mean 1023
RMS 3252
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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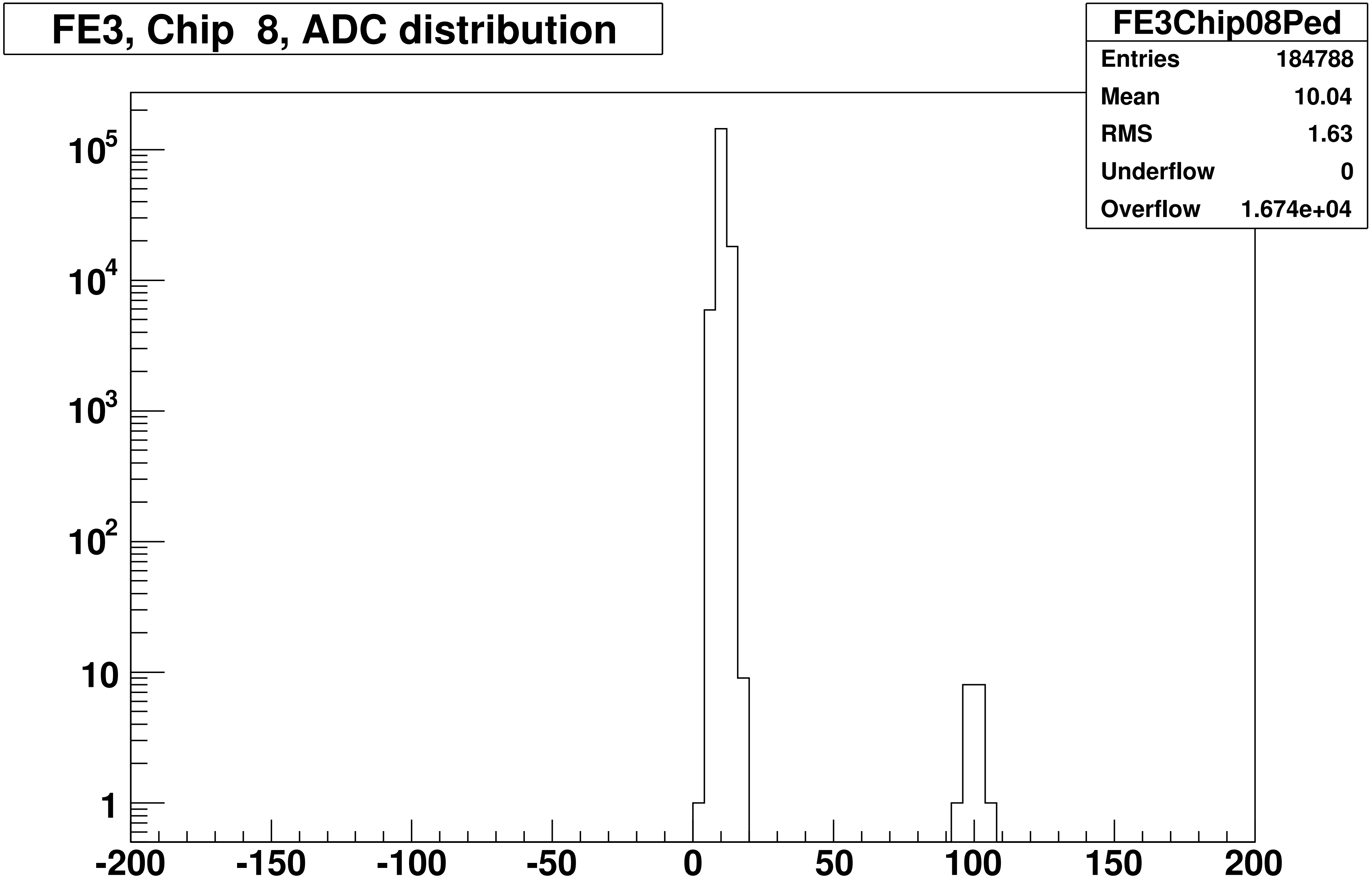
10000
15000
20000
25000


FE3, Chip 8, ADC distribution
FE3Chip08Ped
Entries 184788
Mean 10.04
RMS 1.63
Underflow 0
Overflow 1.674e+04
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10^4
10^3
10^2
10
1
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150
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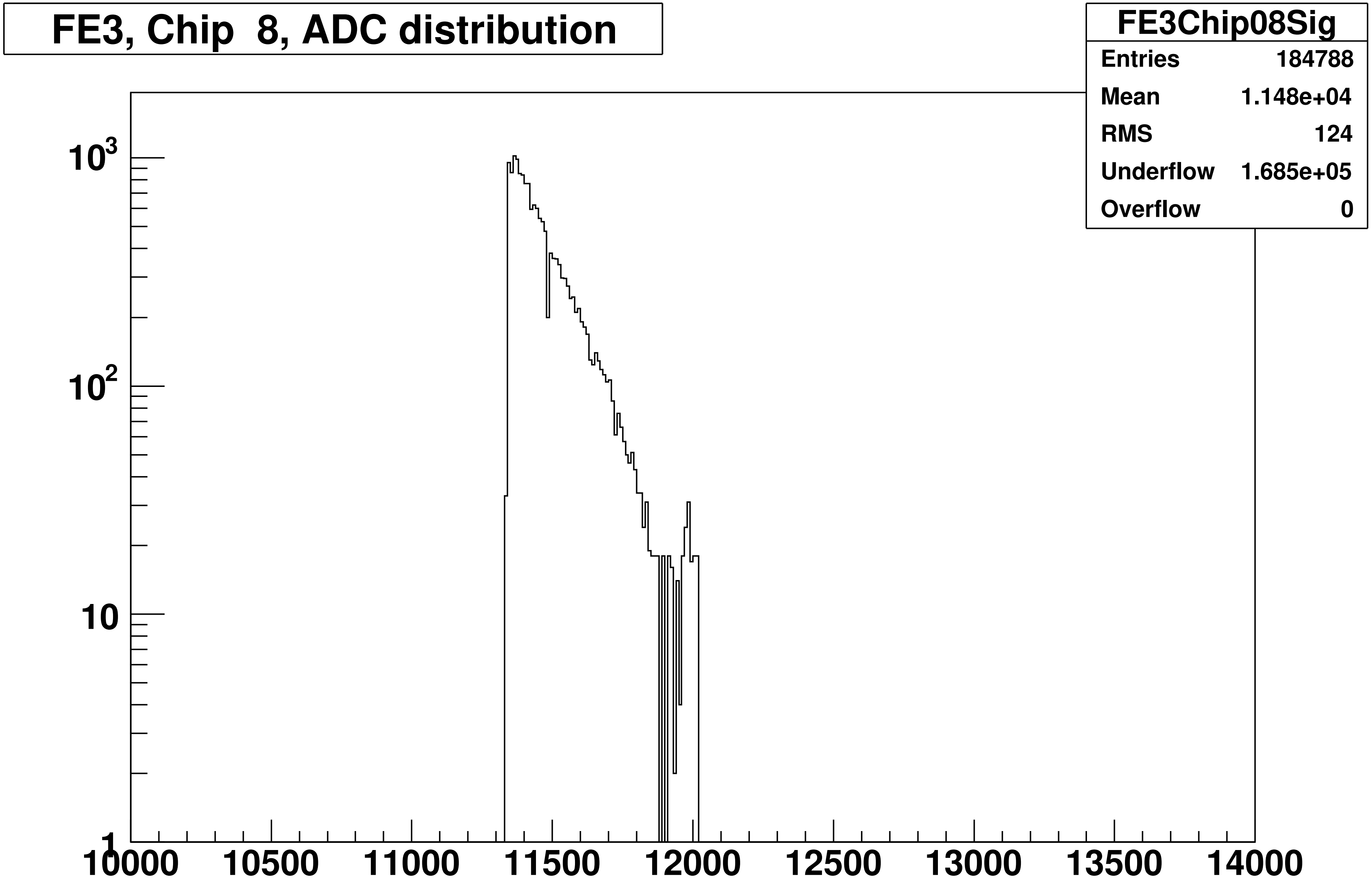

FE3, Chip 8, ADC distribution
FE3Chip08Sig
Entries 184788
Mean 1.148e+04
RMS 124
Underflow 1.685e+05
Overflow 0
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11500
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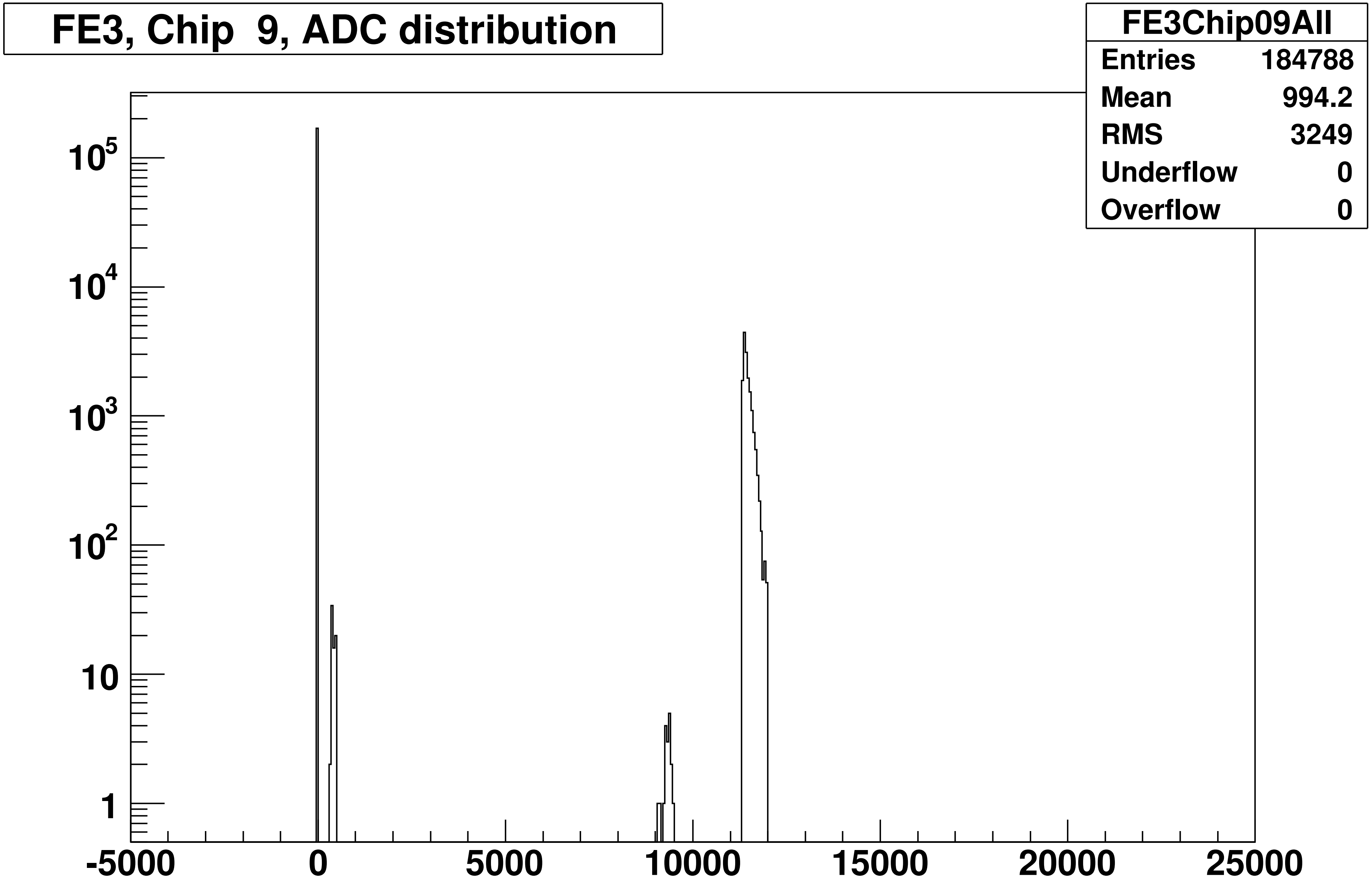
FE3, Chip 9, ADC distribution
FE3Chip09All
Entries 184788
Mean 994.2
RMS 3249
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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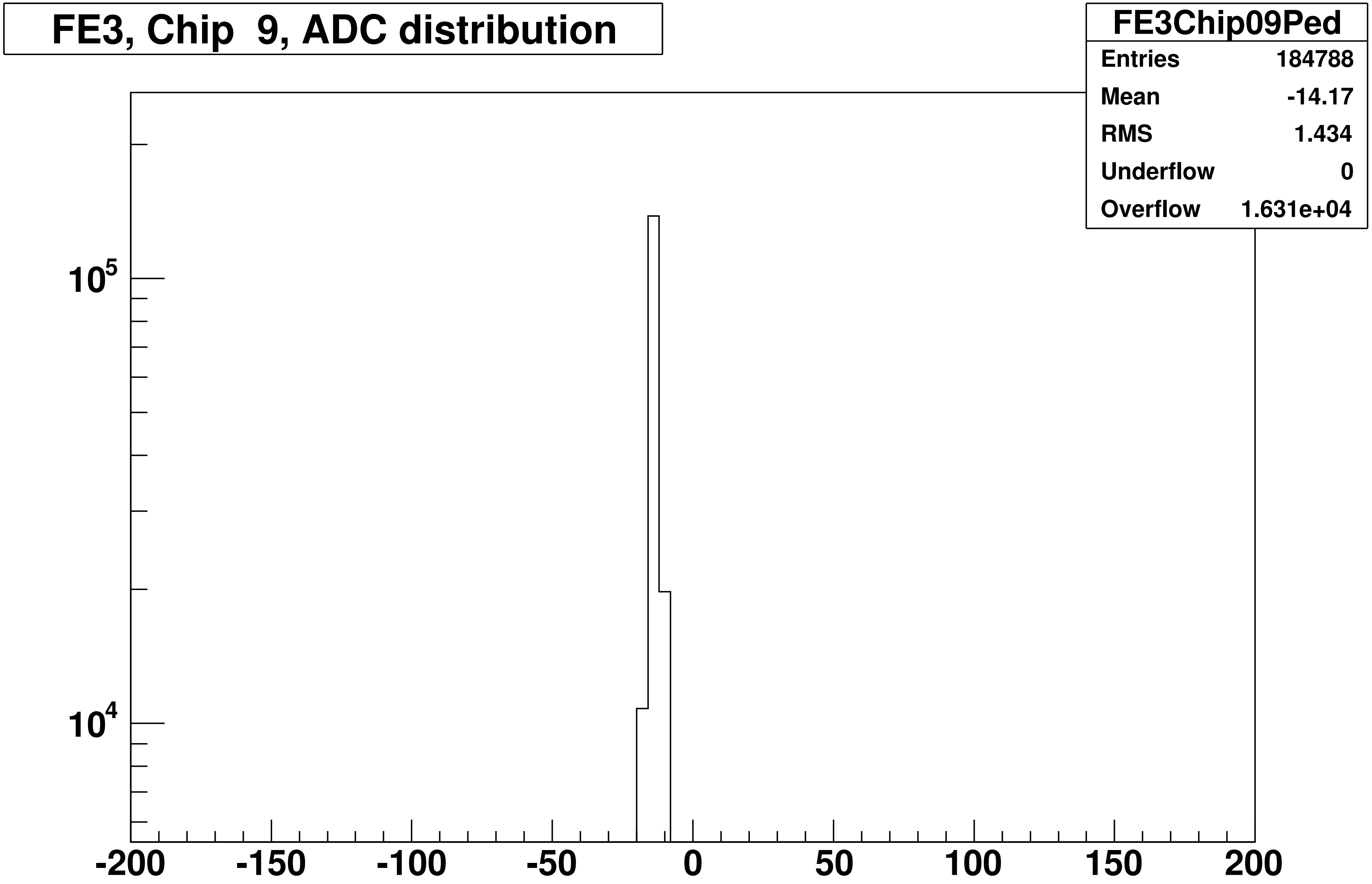
25000


FE3, Chip 9, ADC distribution
FE3Chip09Ped
Entries 184788
Mean -14.17
RMS 1.434
Underflow 0
Overflow 1.631e+04
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10^4
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-100
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0
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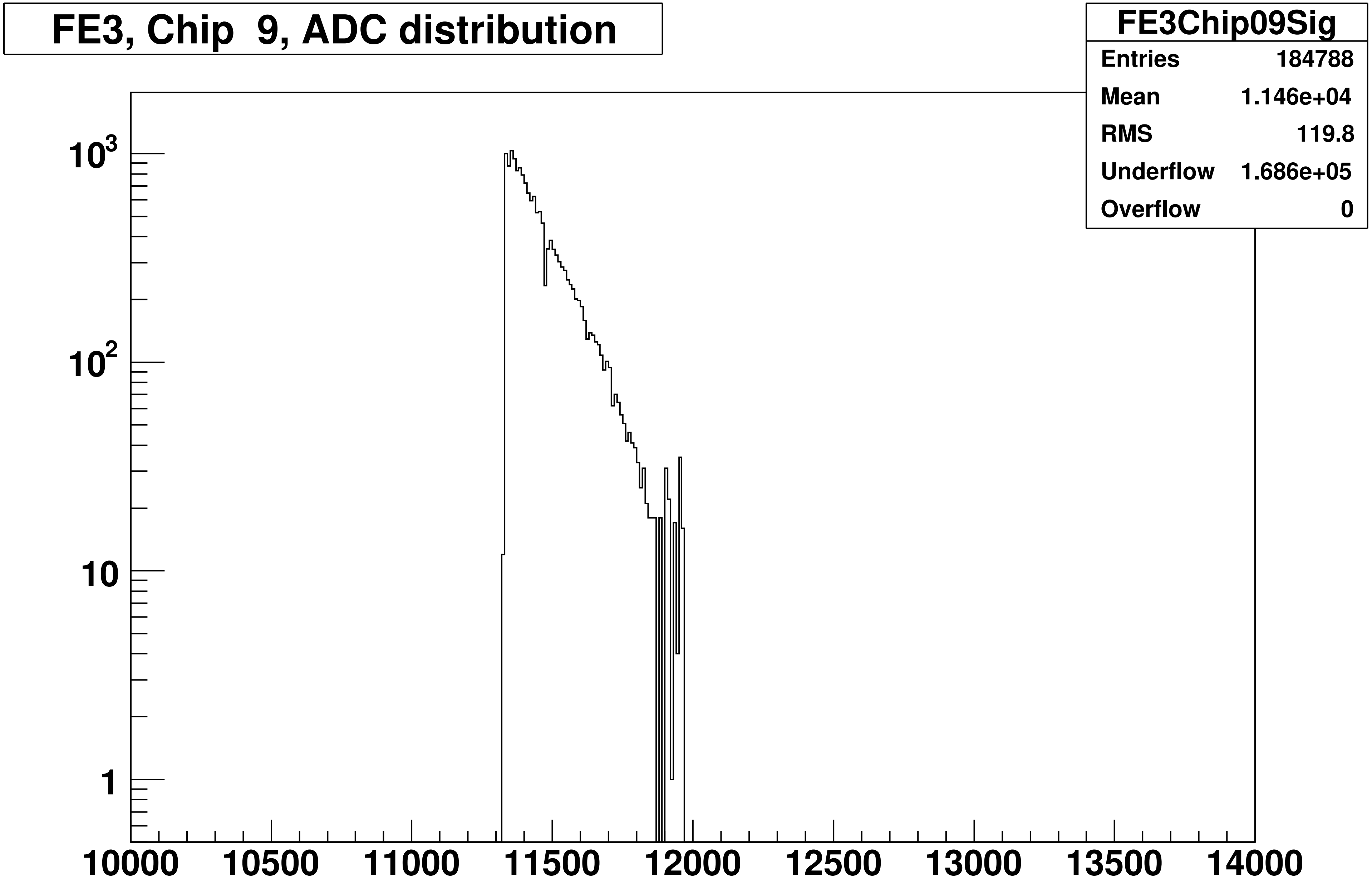
100
150
200



FE3, Chip 9, ADC distribution
FE3Chip09Sig
Entries 184788
Mean 1.146e+04
RMS 119.8
Underflow 1.686e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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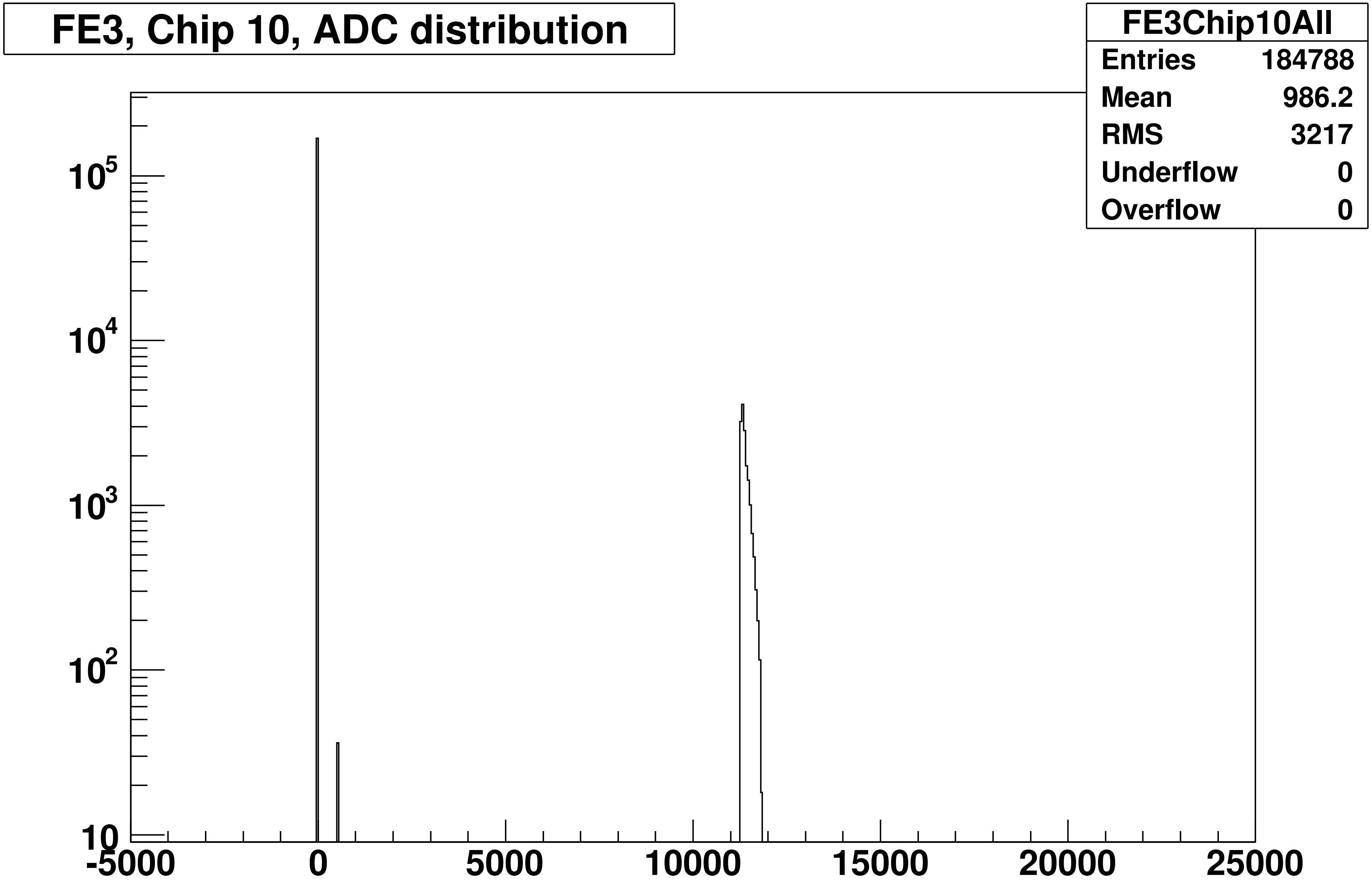
FE3, Chip 10, ADC distribution
FE3Chip10All
Entries 184788
Mean 986.2
RMS 3217
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
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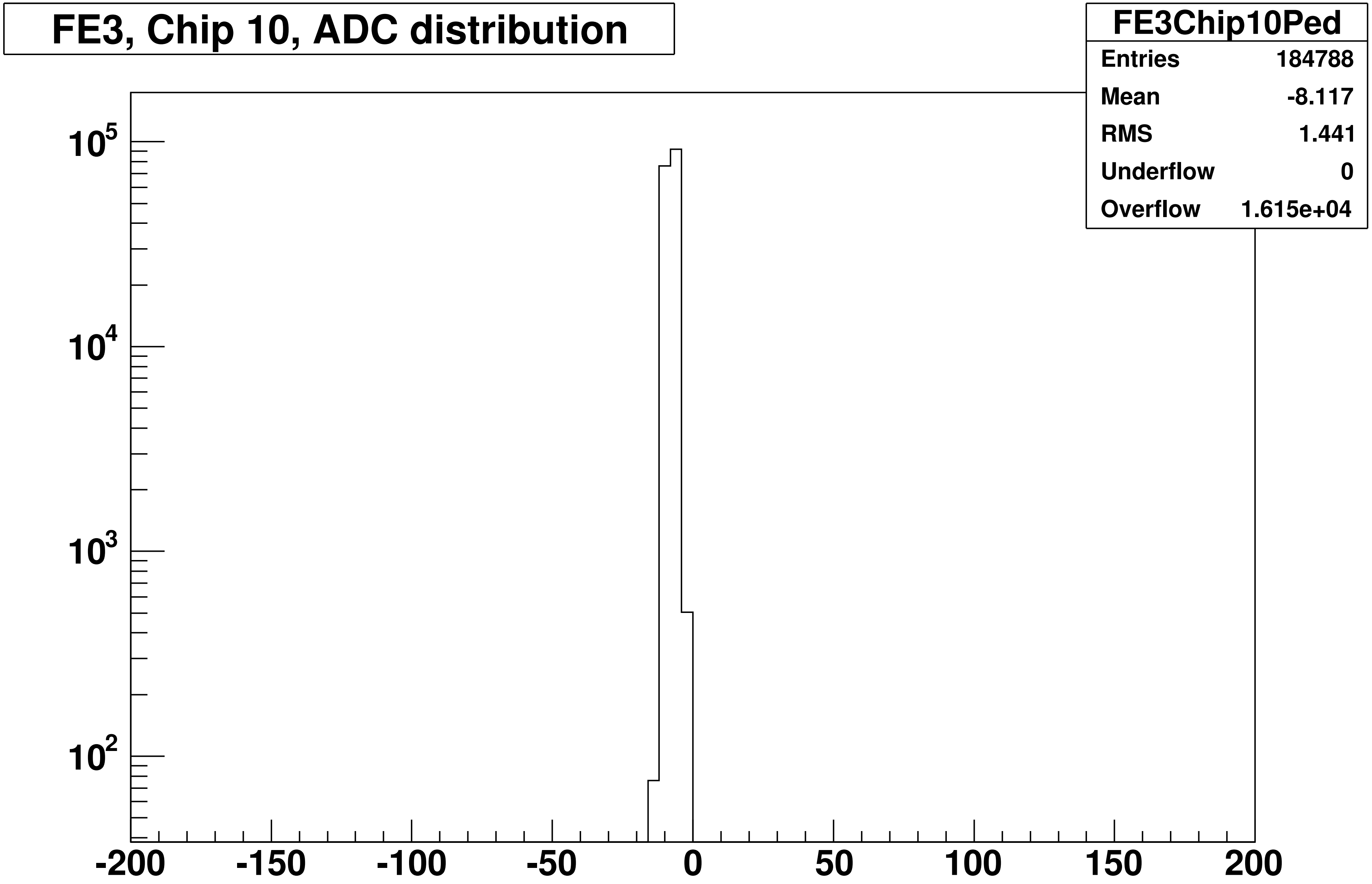
10000
15000
20000
25000


FE3, Chip 10, ADC distribution
FE3Chip10Ped
Entries 184788
Mean -8.117
RMS 1.441
Underflow 0
Overflow 1.615e+04
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10^4
10^3
10^2
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-100
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0
50
100
150
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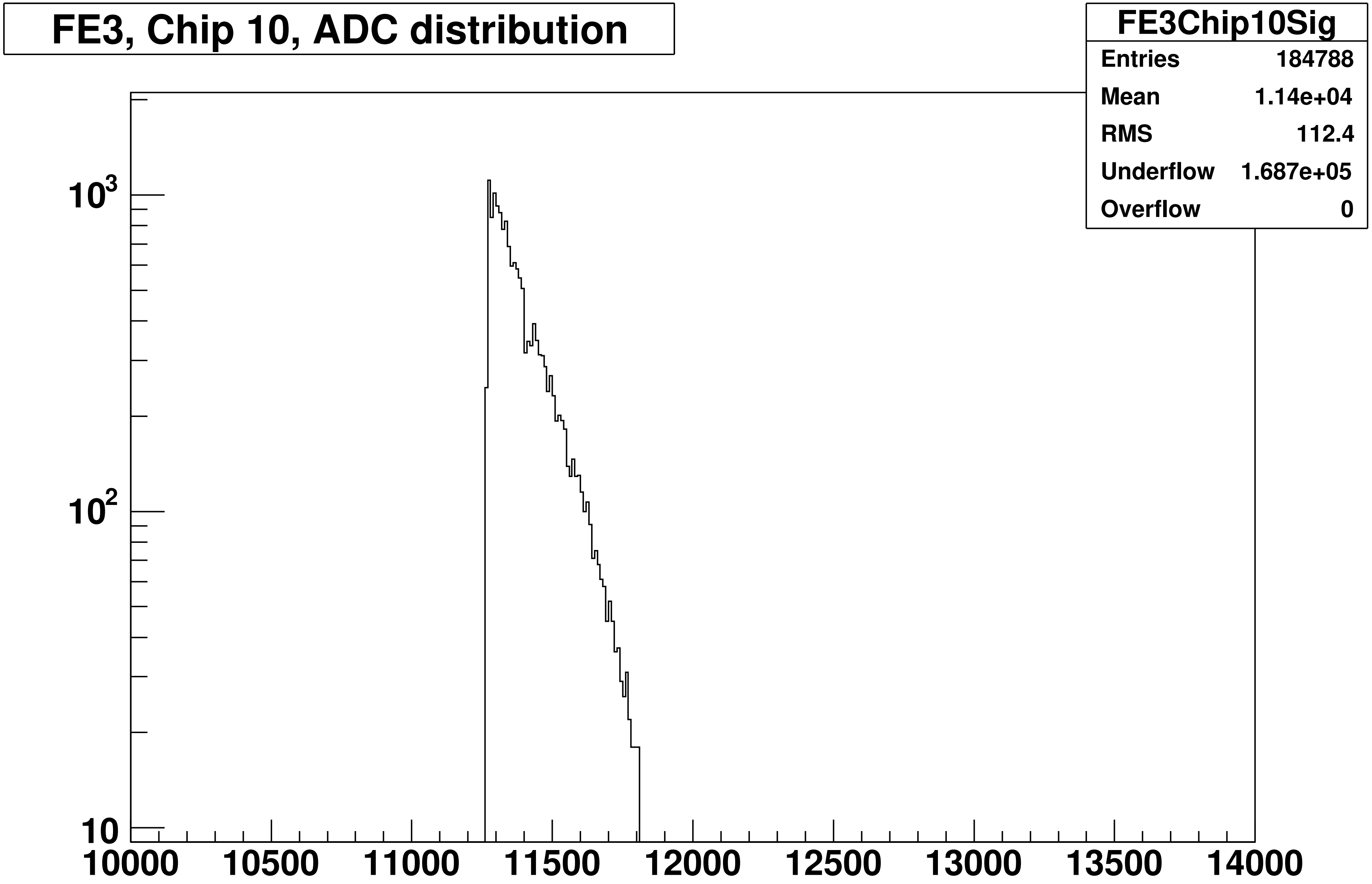

FE3, Chip 10, ADC distribution
FE3Chip10Sig
Entries 184788
Mean 1.14e+04
RMS 112.4
Underflow 1.687e+05
Overflow 0
10^3
10^2
10
10000
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11000
11500
12000
12500
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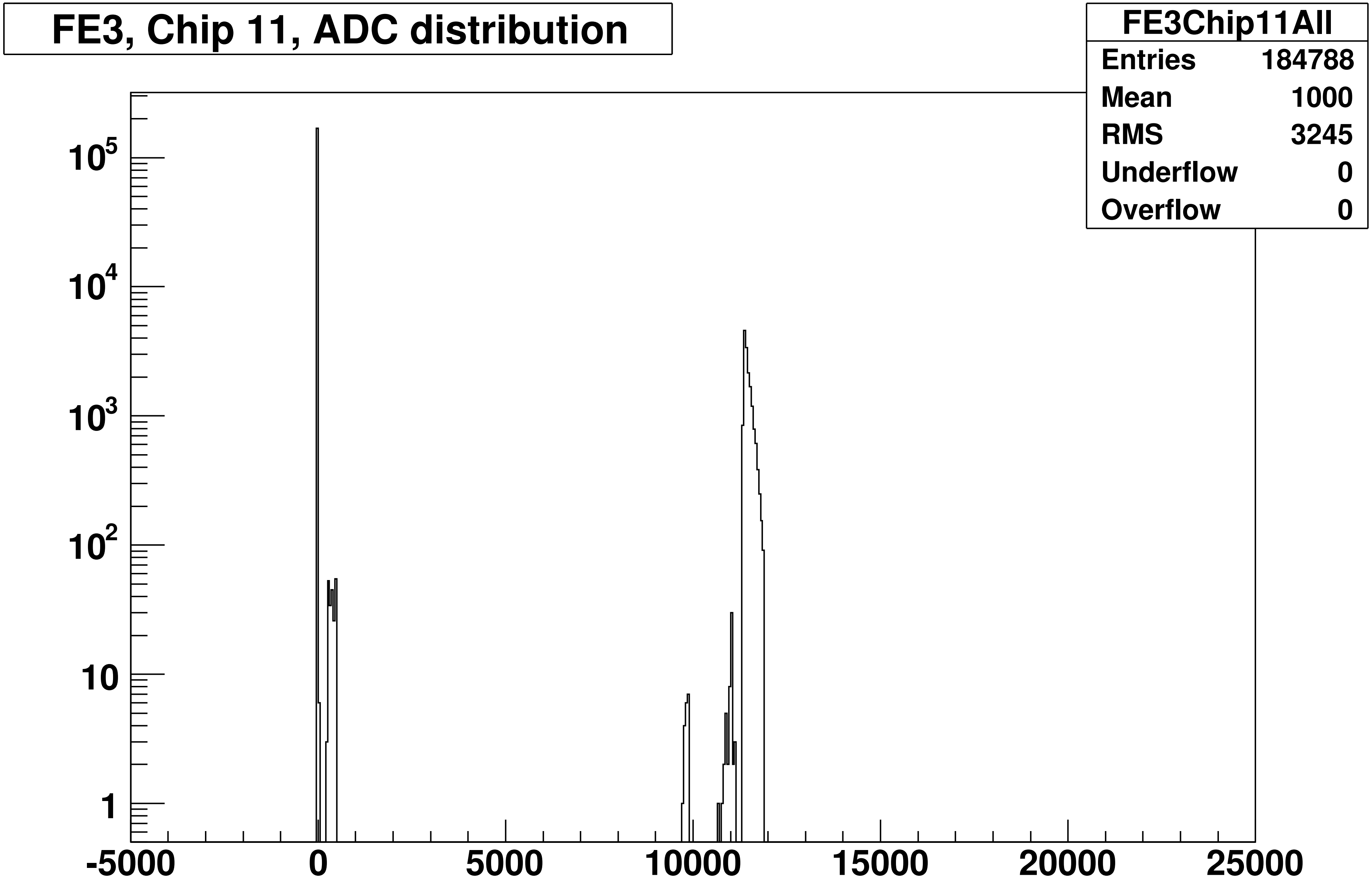
FE3, Chip 11, ADC distribution
FE3Chip11All
Entries 184788
Mean 1000
RMS 3245
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
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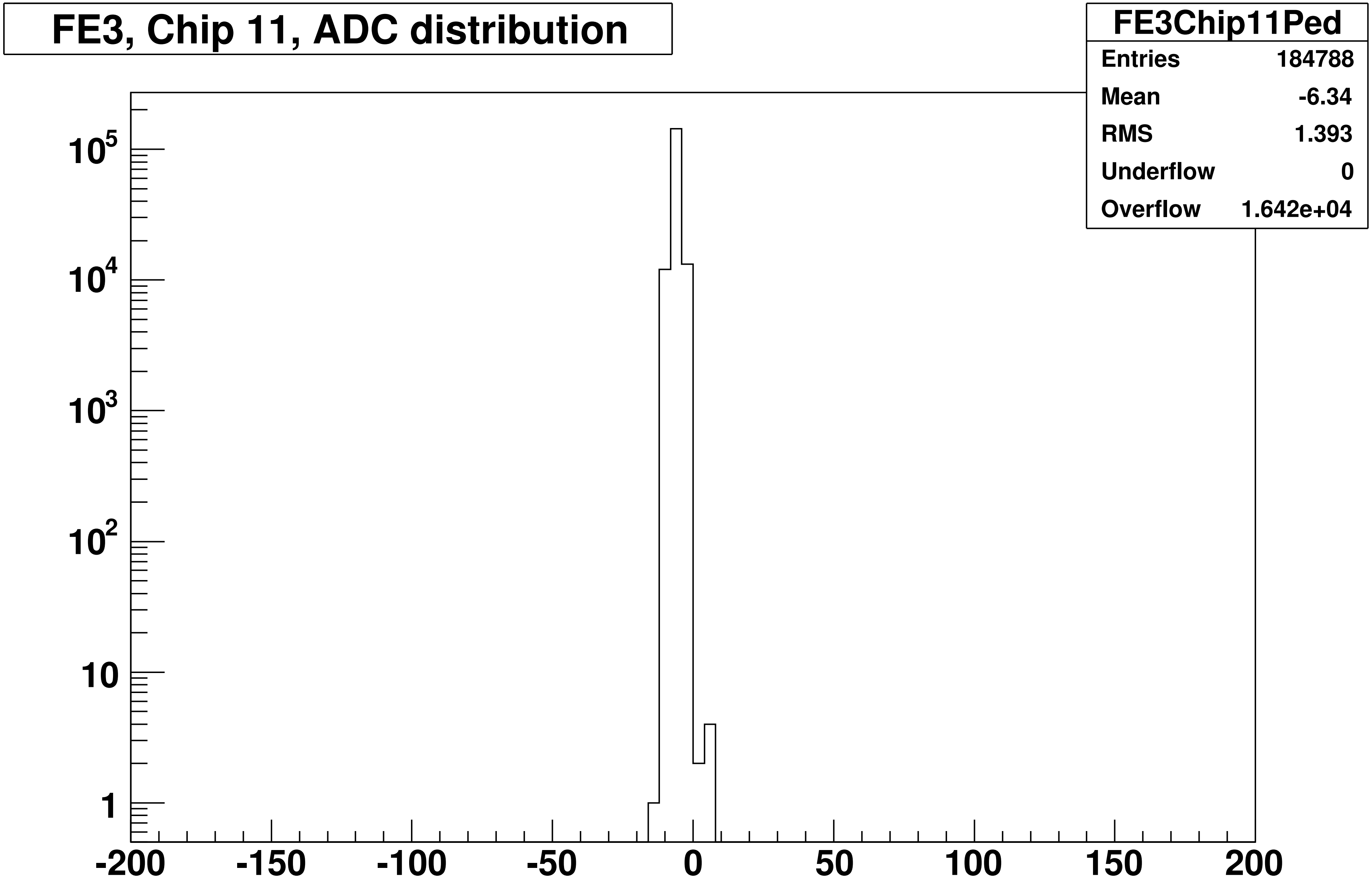
10000
15000
20000
25000


FE3, Chip 11, ADC distribution
FE3Chip11Ped
Entries 184788
Mean -6.34
RMS 1.393
Underflow 0
Overflow 1.642e+04
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10^4
10^3
10^2
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150
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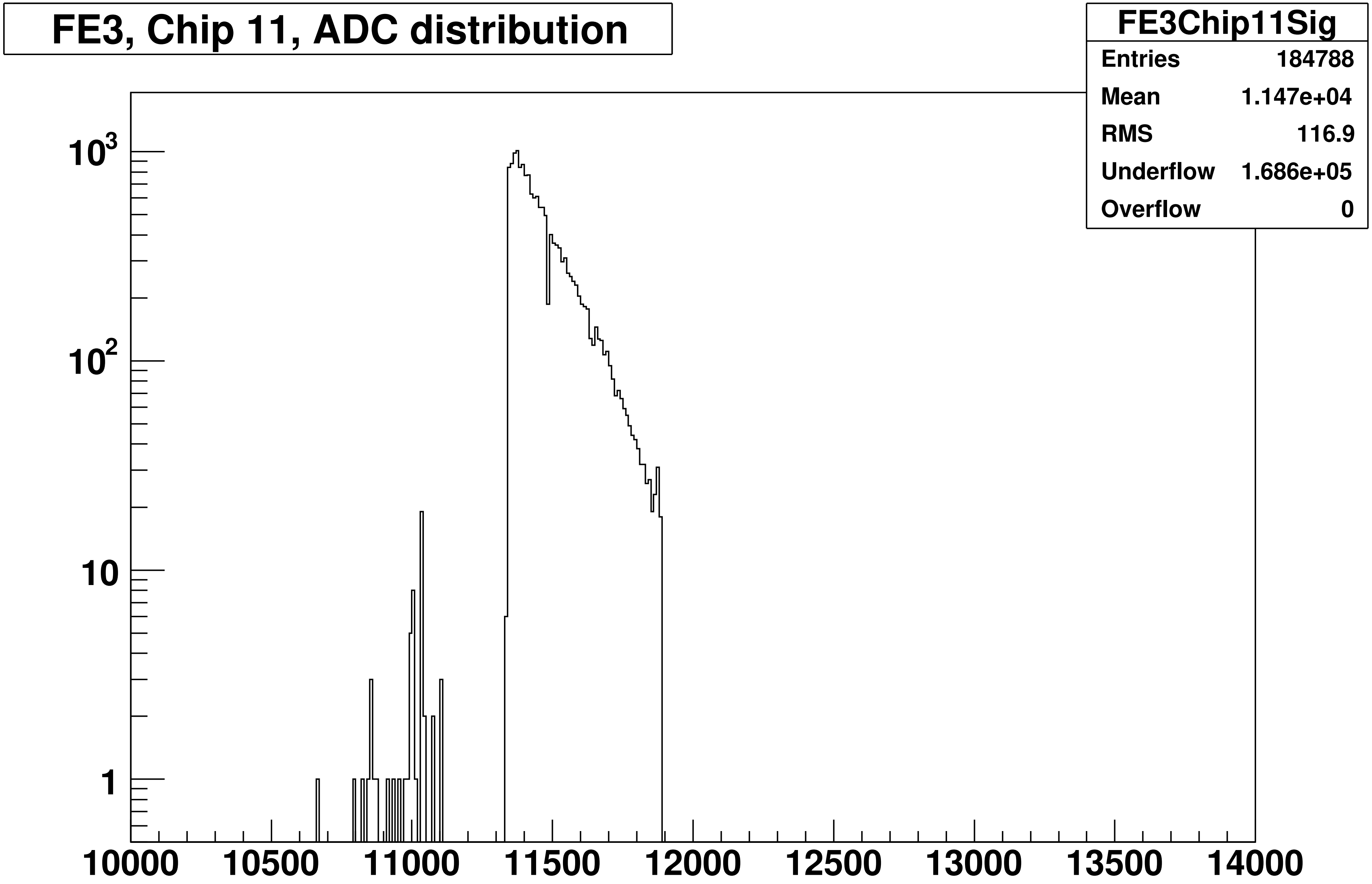

FE3, Chip 11, ADC distribution
FE3Chip11Sig
Entries 184788
Mean 1.147e+04
RMS 116.9
Underflow 1.686e+05
Overflow 0
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10^2
10
1
10000
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11500
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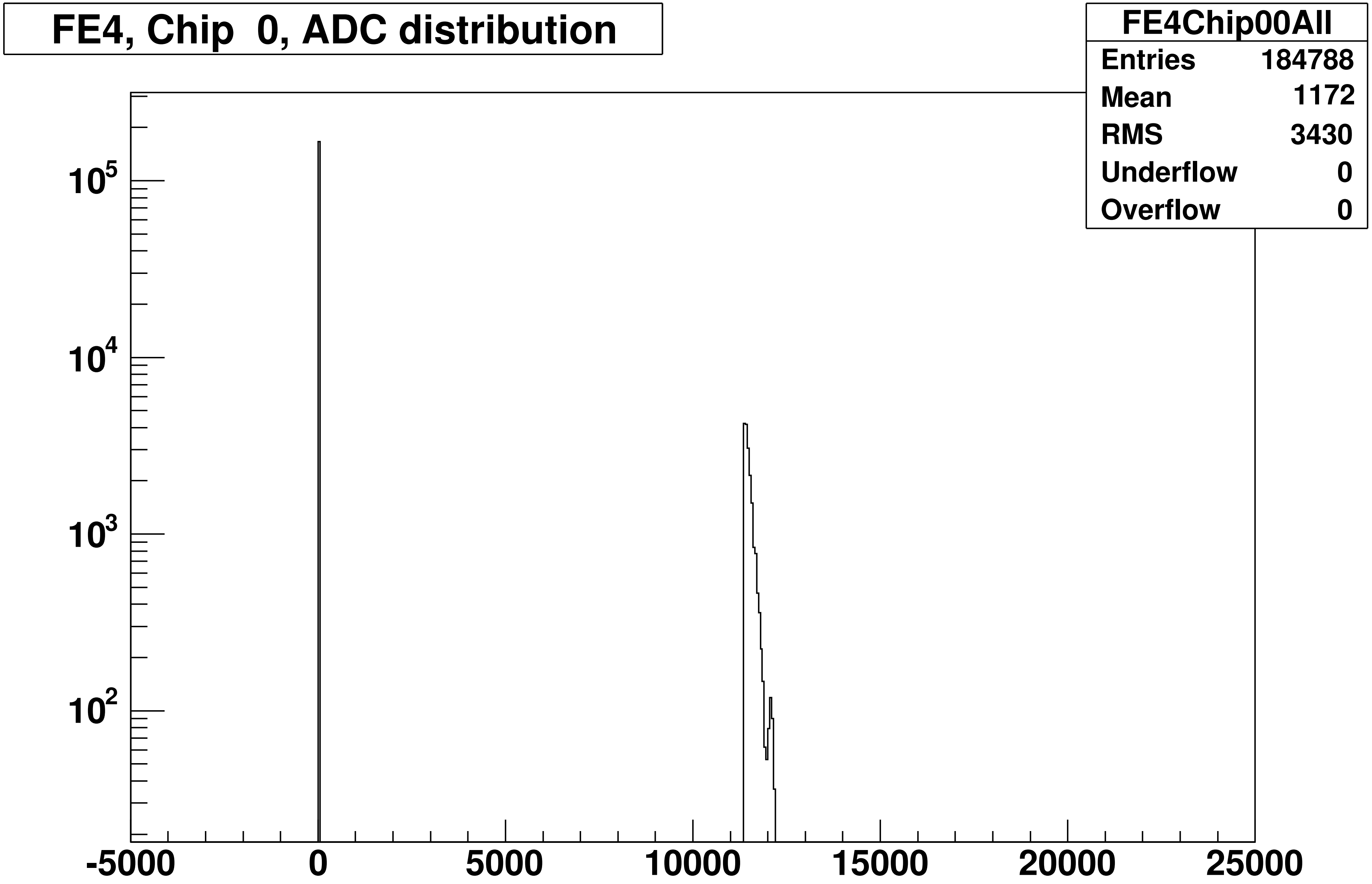
FE4, Chip 0, ADC distribution
FE4Chip00All
Entries 184788
Mean 1172
RMS 3430
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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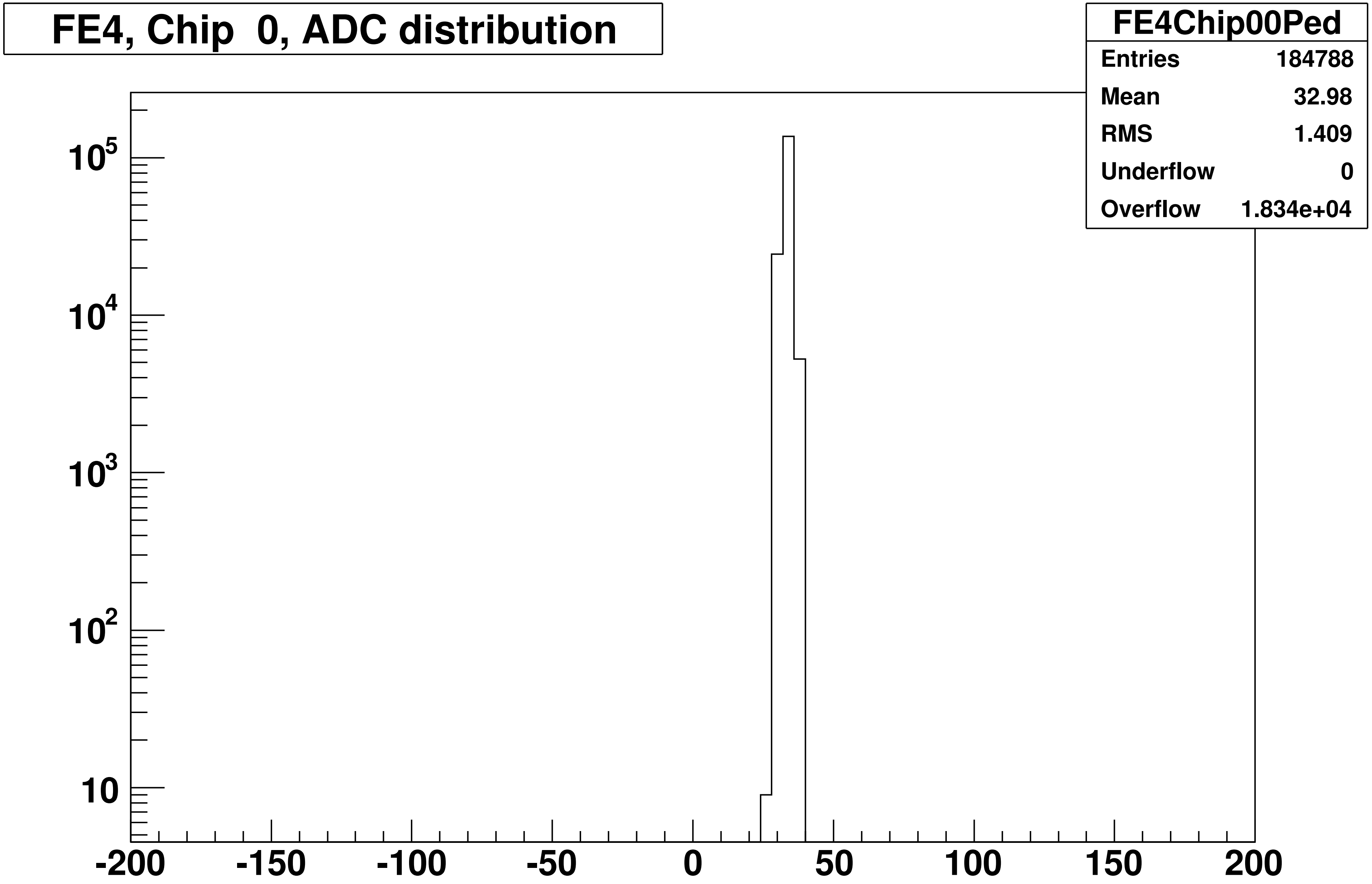
0
5000
10000
15000
20000
25000


FE4, Chip 0, ADC distribution
FE4Chip00Ped
Entries 184788
Mean 32.98
RMS 1.409
Underflow 0
Overflow 1.834e+04
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10^2
10^3
10^4
10^5
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-100
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0
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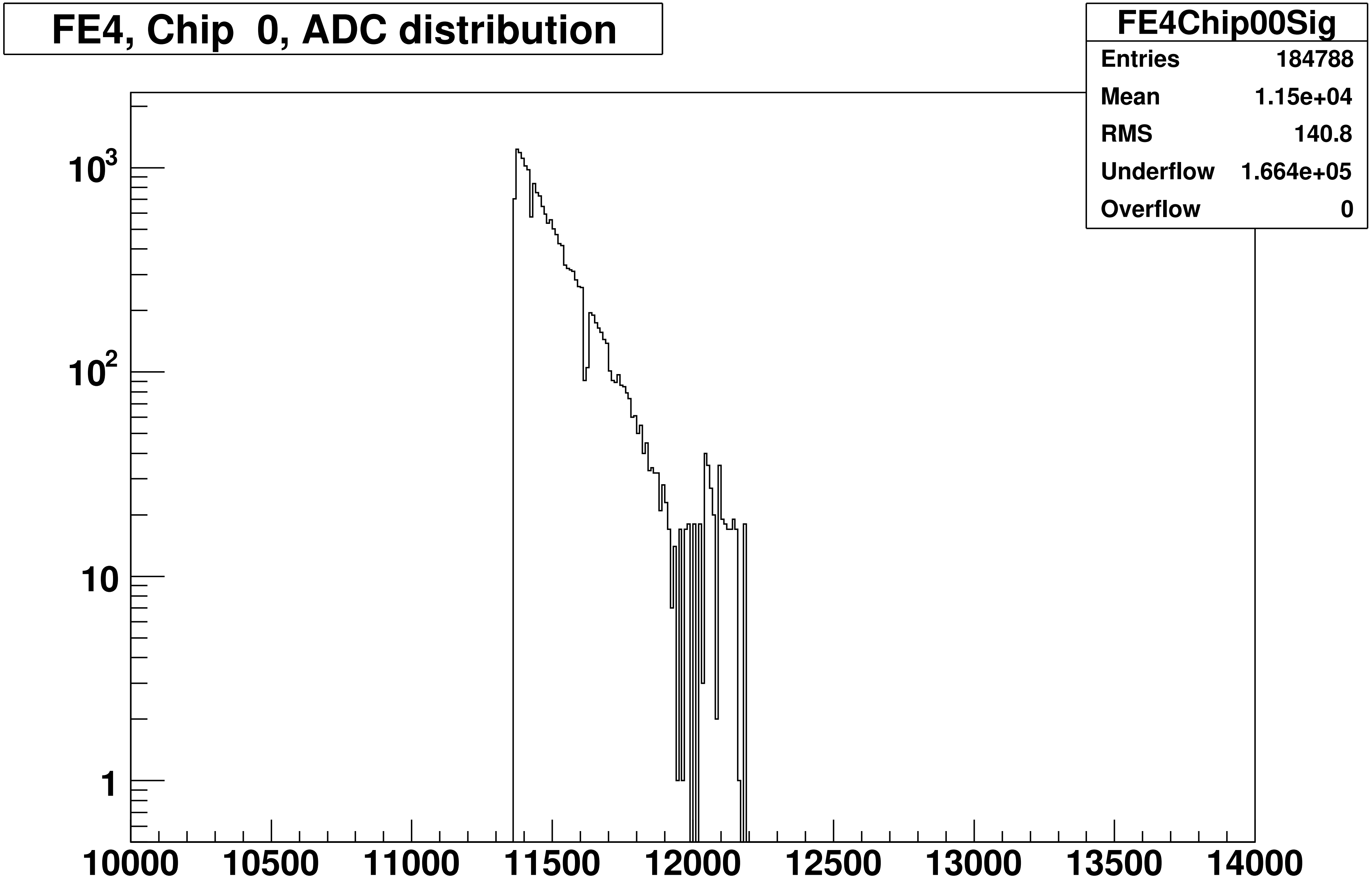
100
150
200


FE4, Chip 0, ADC distribution
FE4Chip00Sig
Entries 184788
Mean 1.15e+04
RMS 140.8
Underflow 1.664e+05
Overflow 0
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10^2
10
1
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11500
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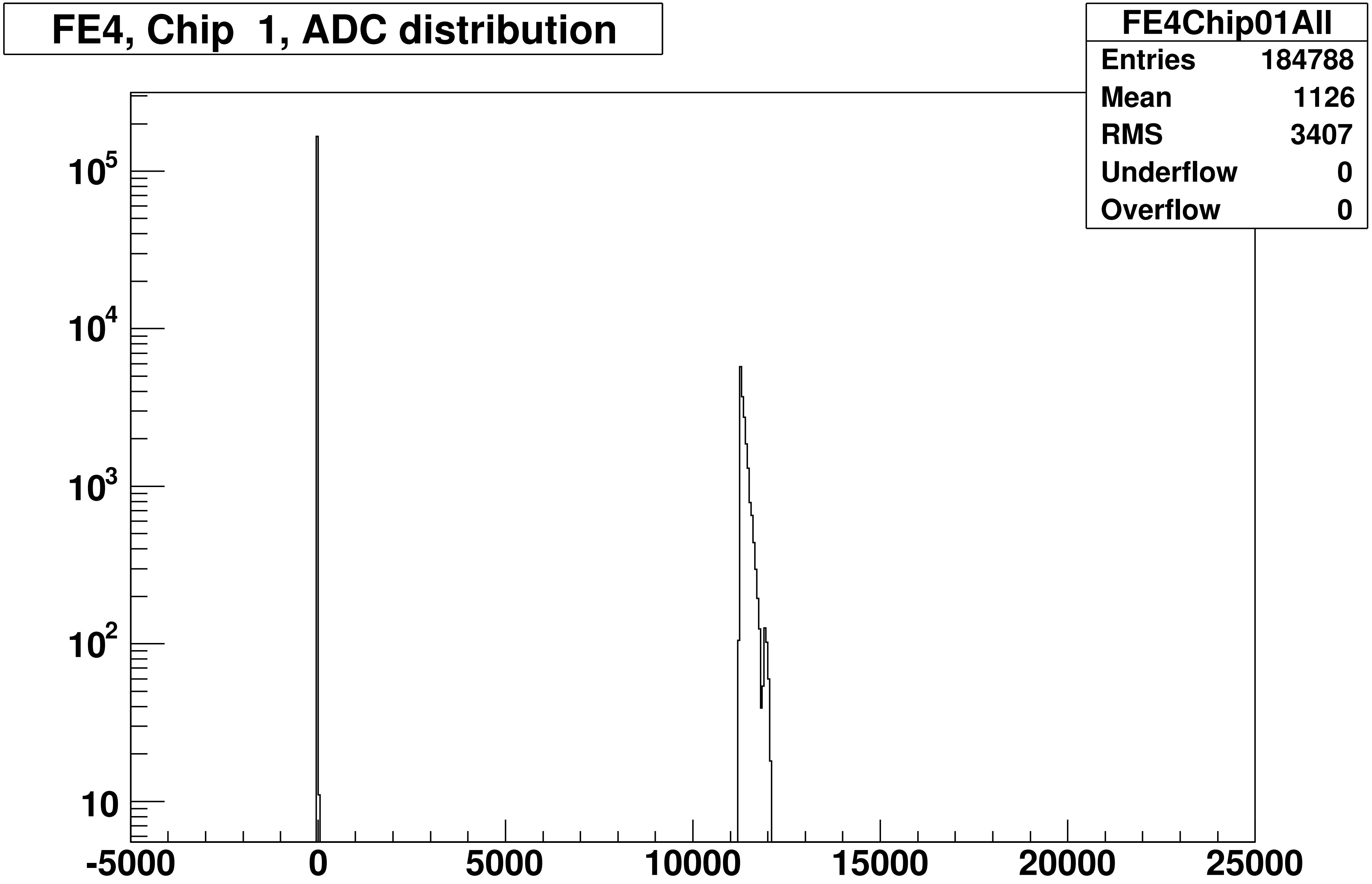
FE4, Chip 1, ADC distribution
FE4Chip01All
Entries 184788
Mean 1126
RMS 3407
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
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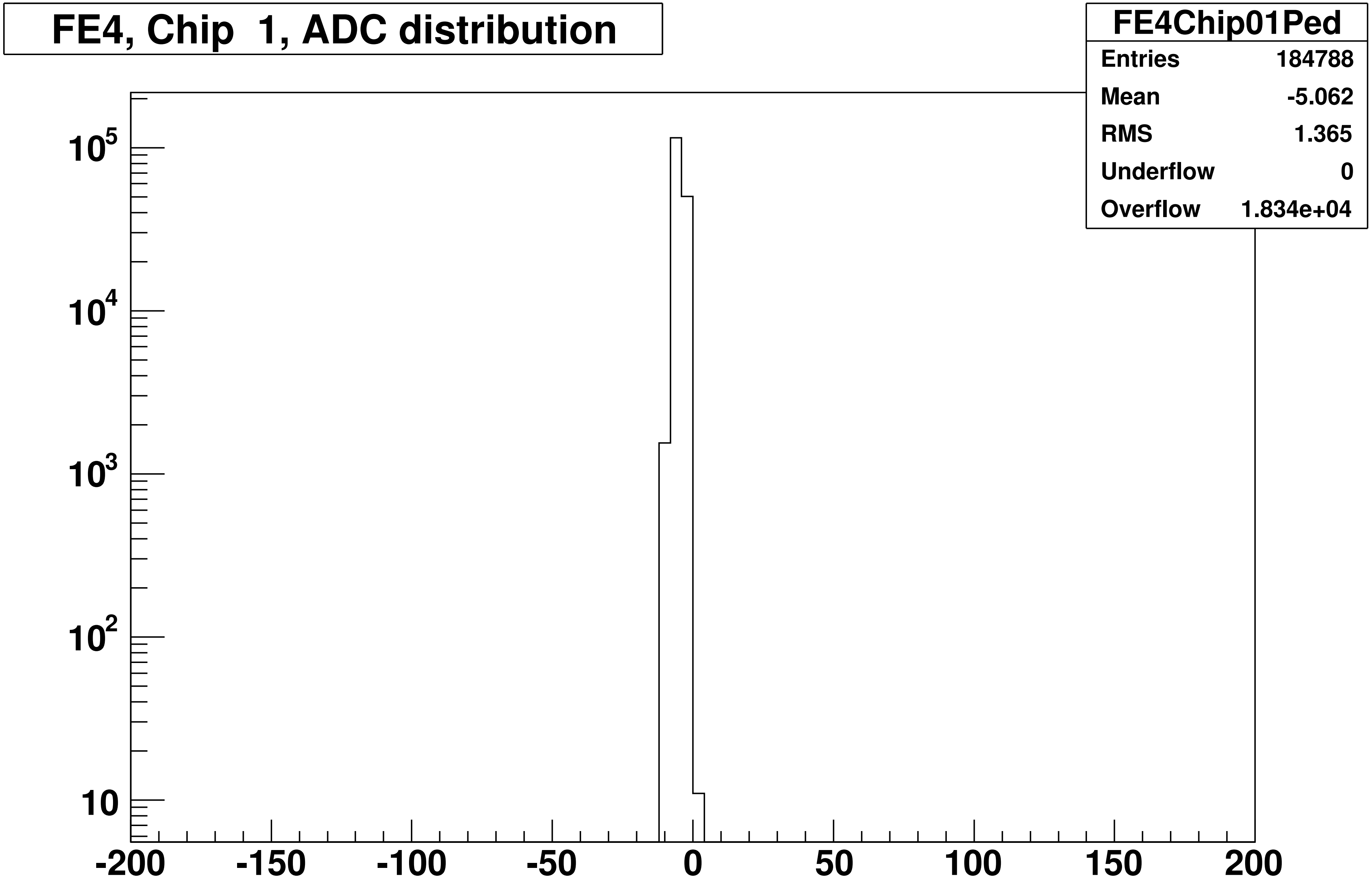
25000


FE4, Chip 1, ADC distribution
FE4Chip01Ped
Entries 184788
Mean -5.062
RMS 1.365
Underflow 0
Overflow 1.834e+04
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10^4
10^3
10^2
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-100
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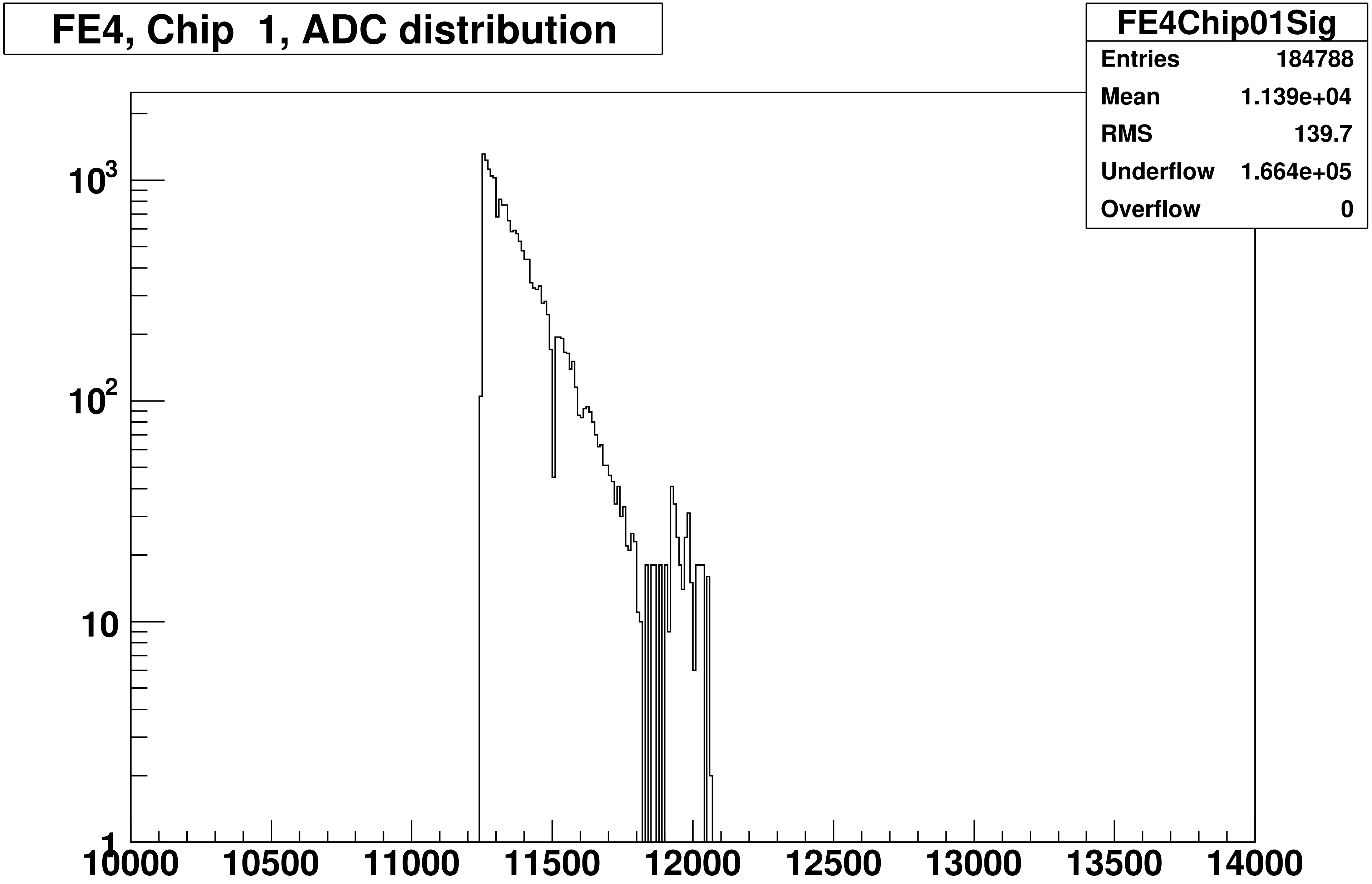
150
200



FE4, Chip 1, ADC distribution
FE4Chip01Sig
Entries 184788
Mean 1.139e+04
RMS 139.7
Underflow 1.664e+05
Overflow 0
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10^2
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1
10000
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11500
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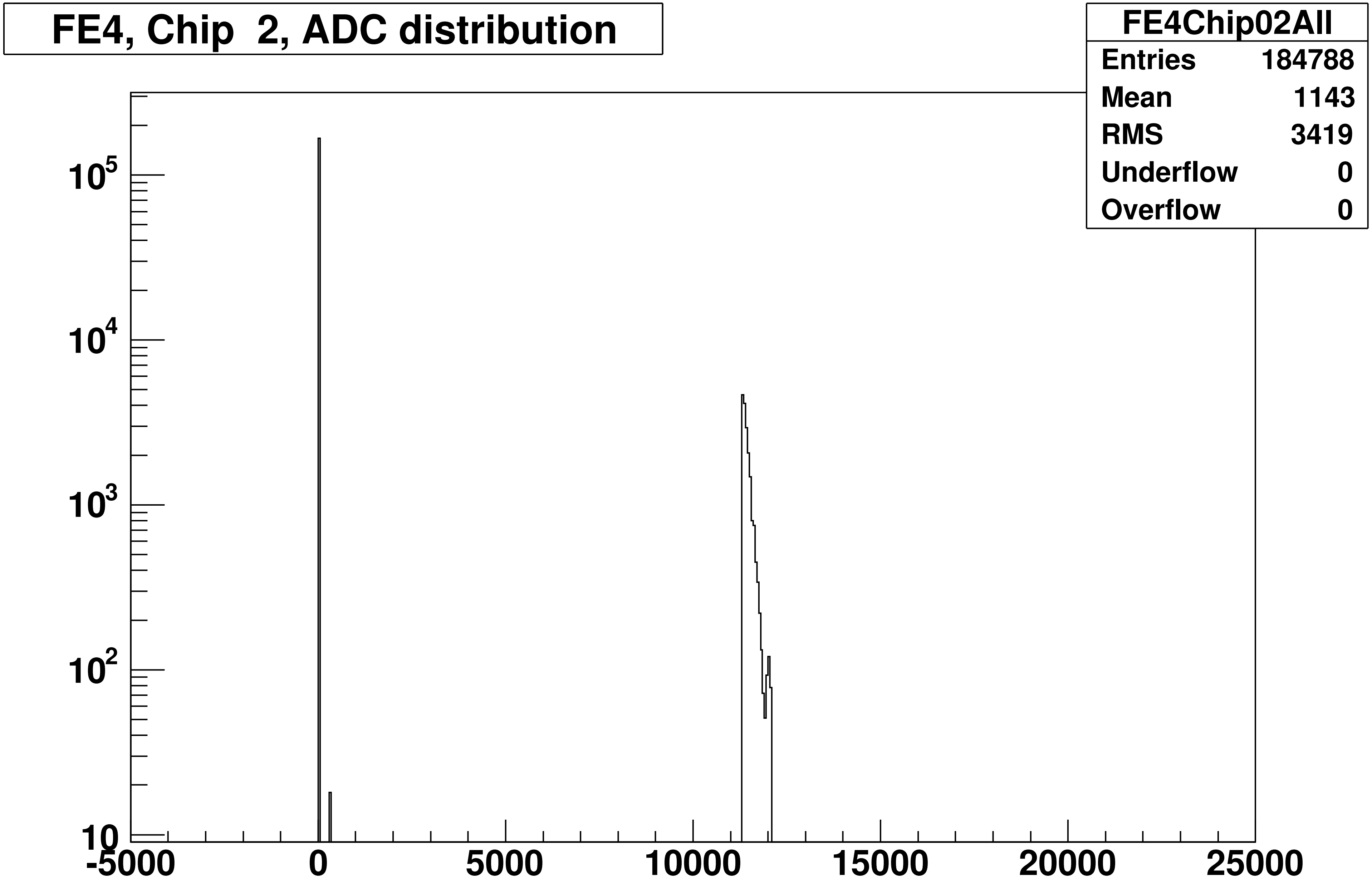
FE4, Chip 2, ADC distribution
FE4Chip02All
Entries 184788
Mean 1143
RMS 3419
Underflow 0
Overflow 0
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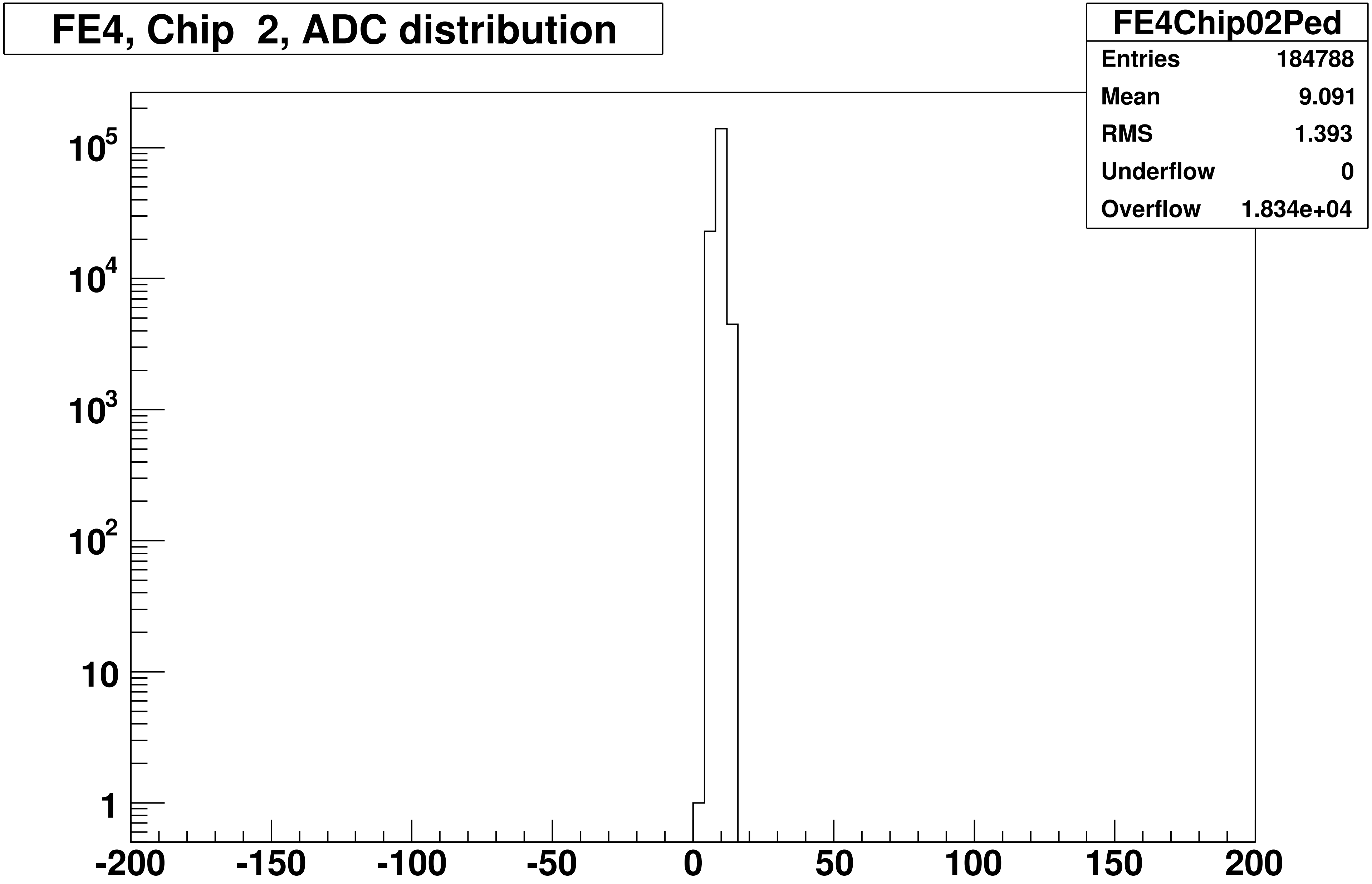
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 2, ADC distribution
FE4Chip02Ped
Entries 184788
Mean 9.091
RMS 1.393
Underflow 0
Overflow 1.834e+04
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10^3
10^2
10
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-100
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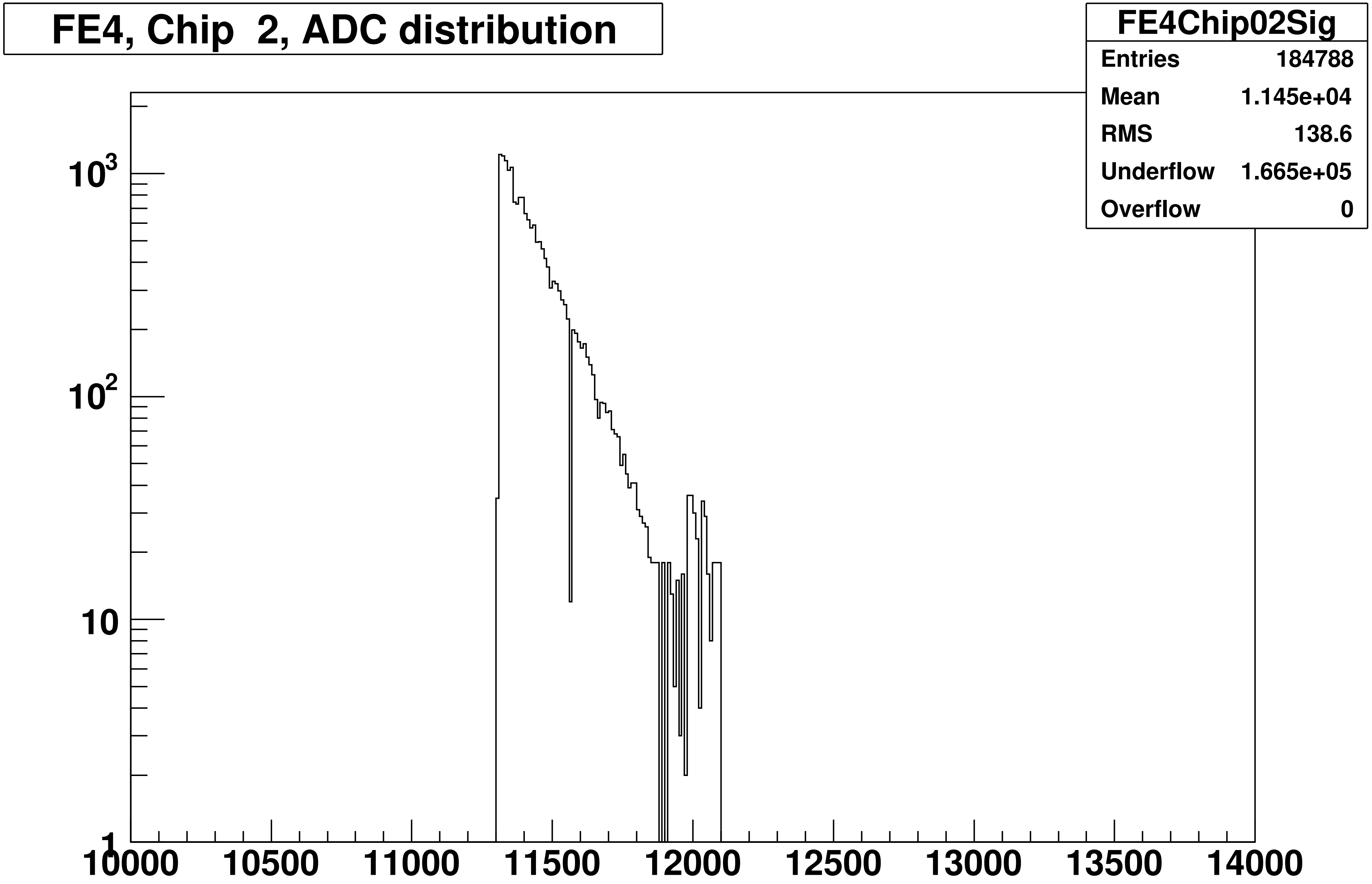
FE4, Chip 2, ADC distribution
FE4Chip02Sig
Entries 184788
Mean 1.145e+04
RMS 138.6
Underflow 1.665e+05
Overflow 0
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11500
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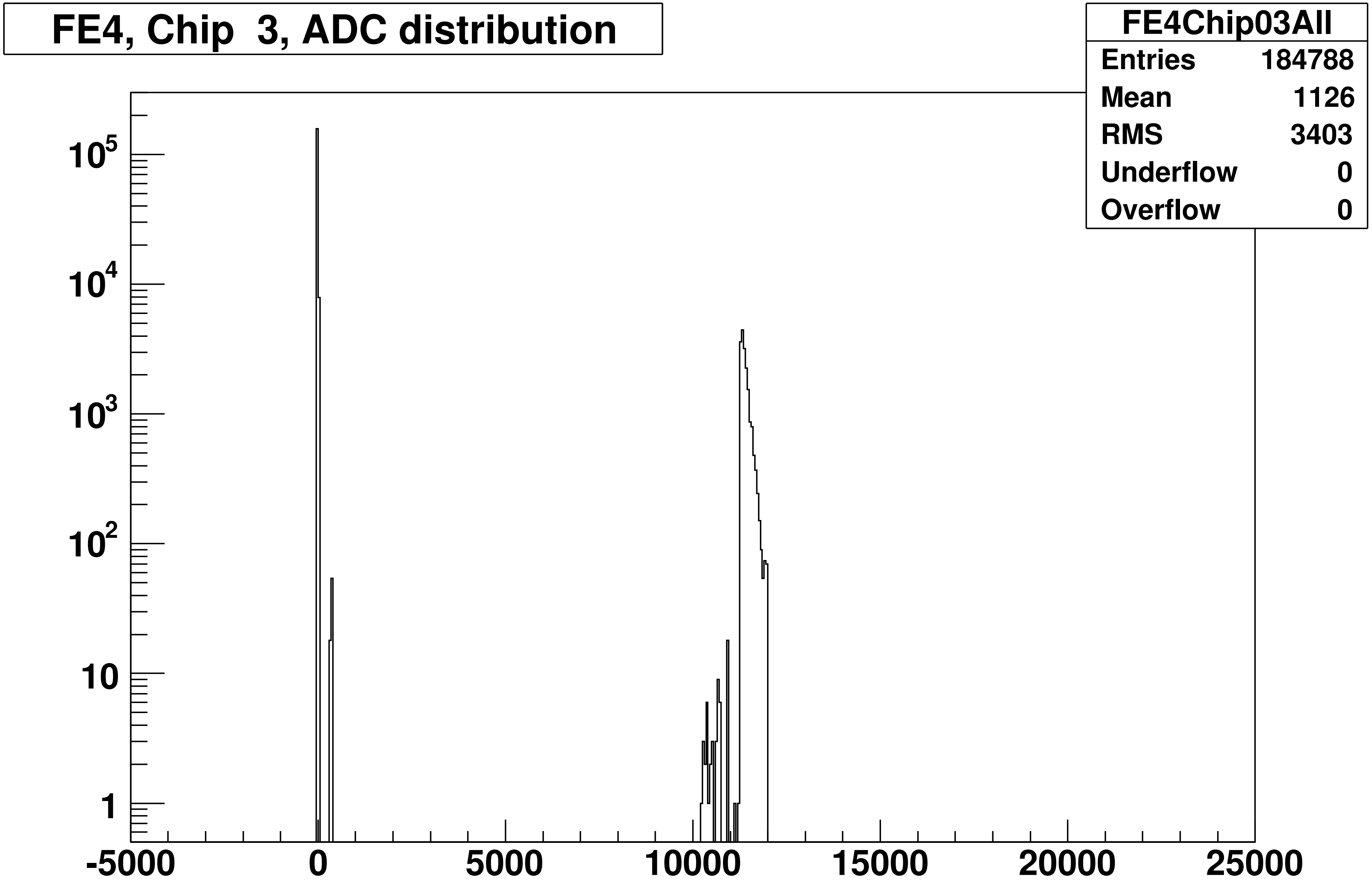
FE4, Chip 3, ADC distribution
FE4Chip03All
Entries 184788
Mean 1126
RMS 3403
Underflow 0
Overflow 0
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10^4
10^3
10^2
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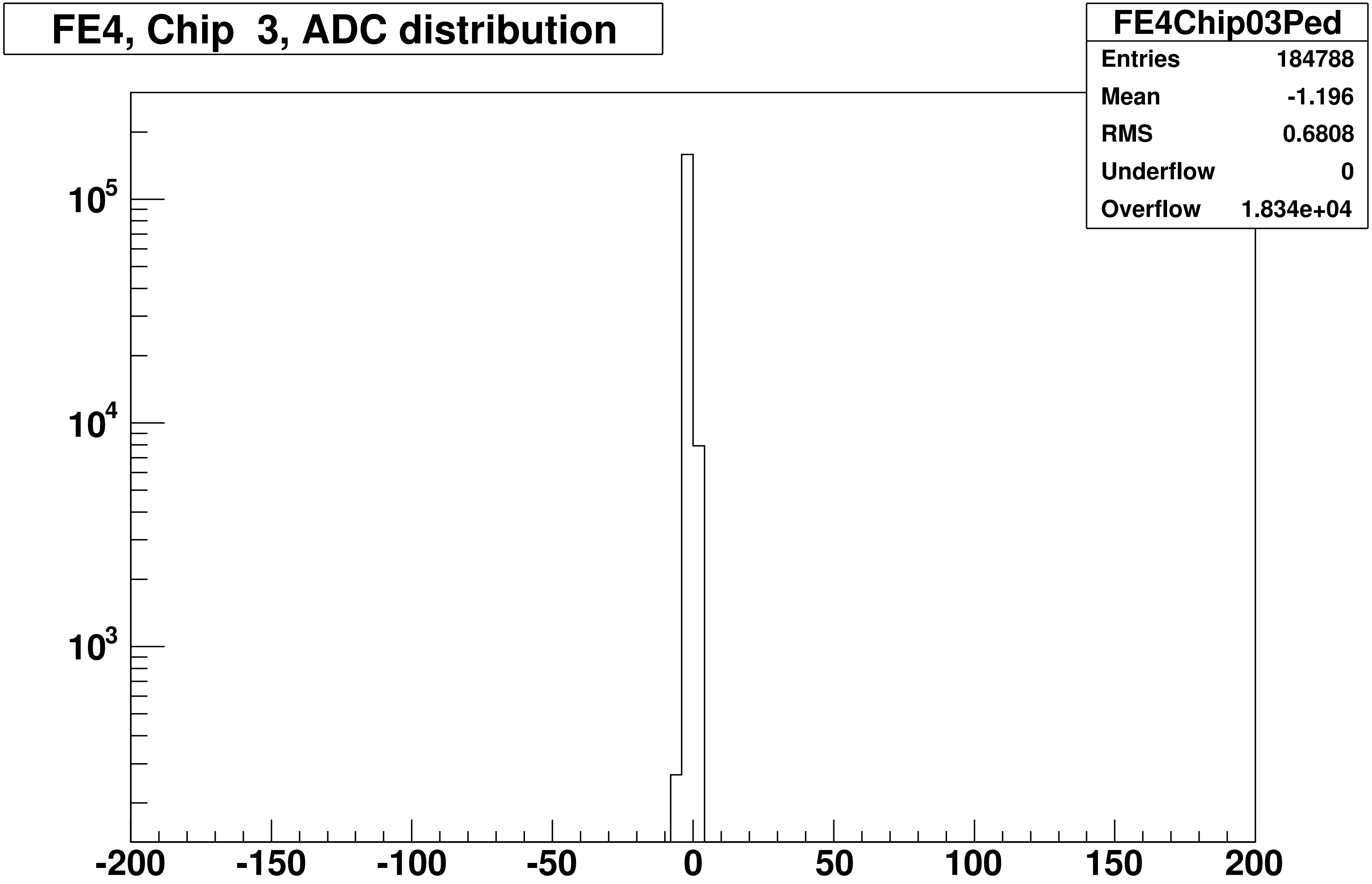
FE4, Chip 3, ADC distribution
FE4Chip03Ped
Entries 184788
Mean -1.196
RMS 0.6808
Underflow 0
Overflow 1.834e+04
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10^4
10^3
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-100
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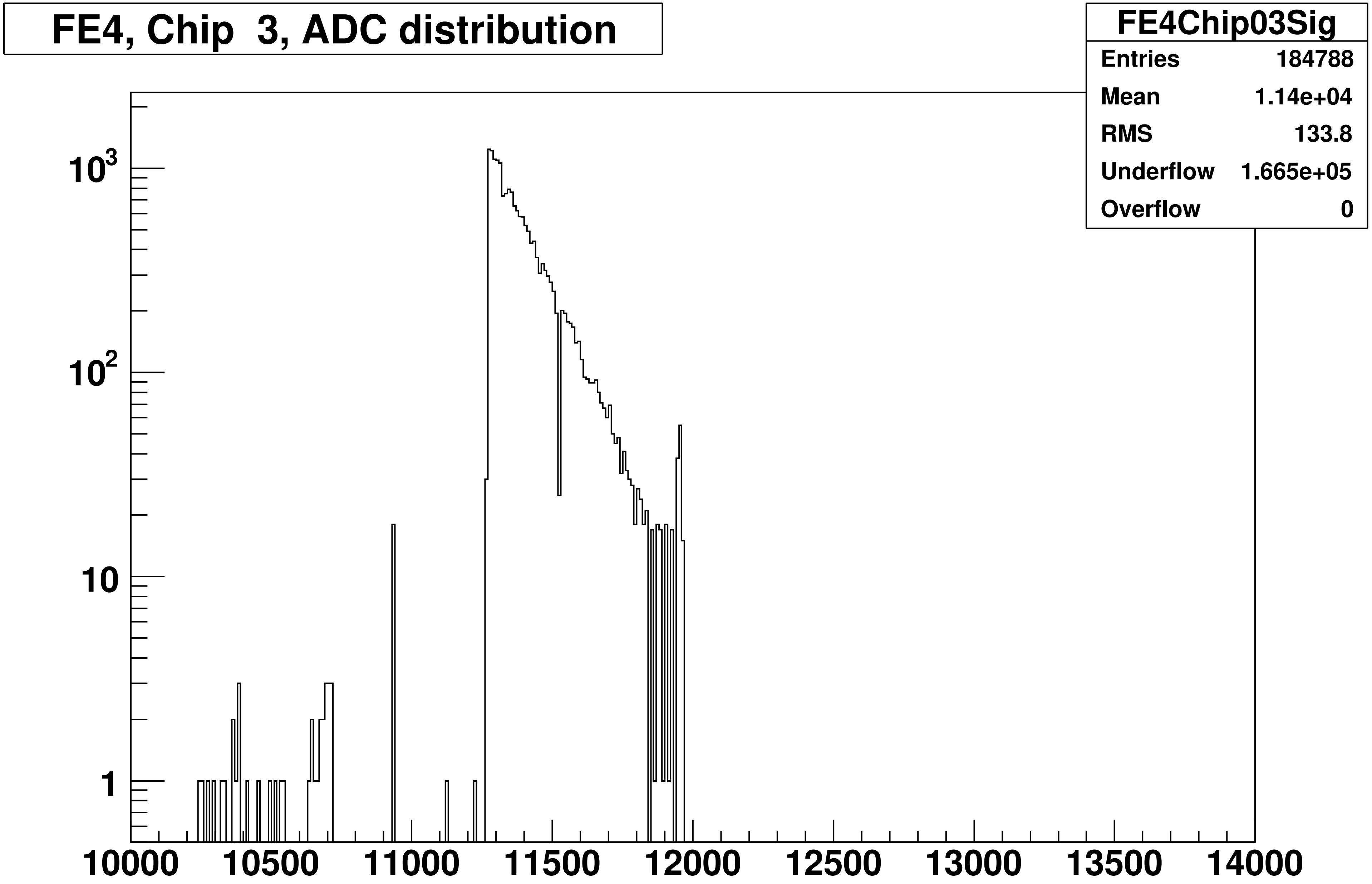

FE4, Chip 3, ADC distribution
FE4Chip03Sig
Entries 184788
Mean 1.14e+04
RMS 133.8
Underflow 1.665e+05
Overflow 0
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10^2
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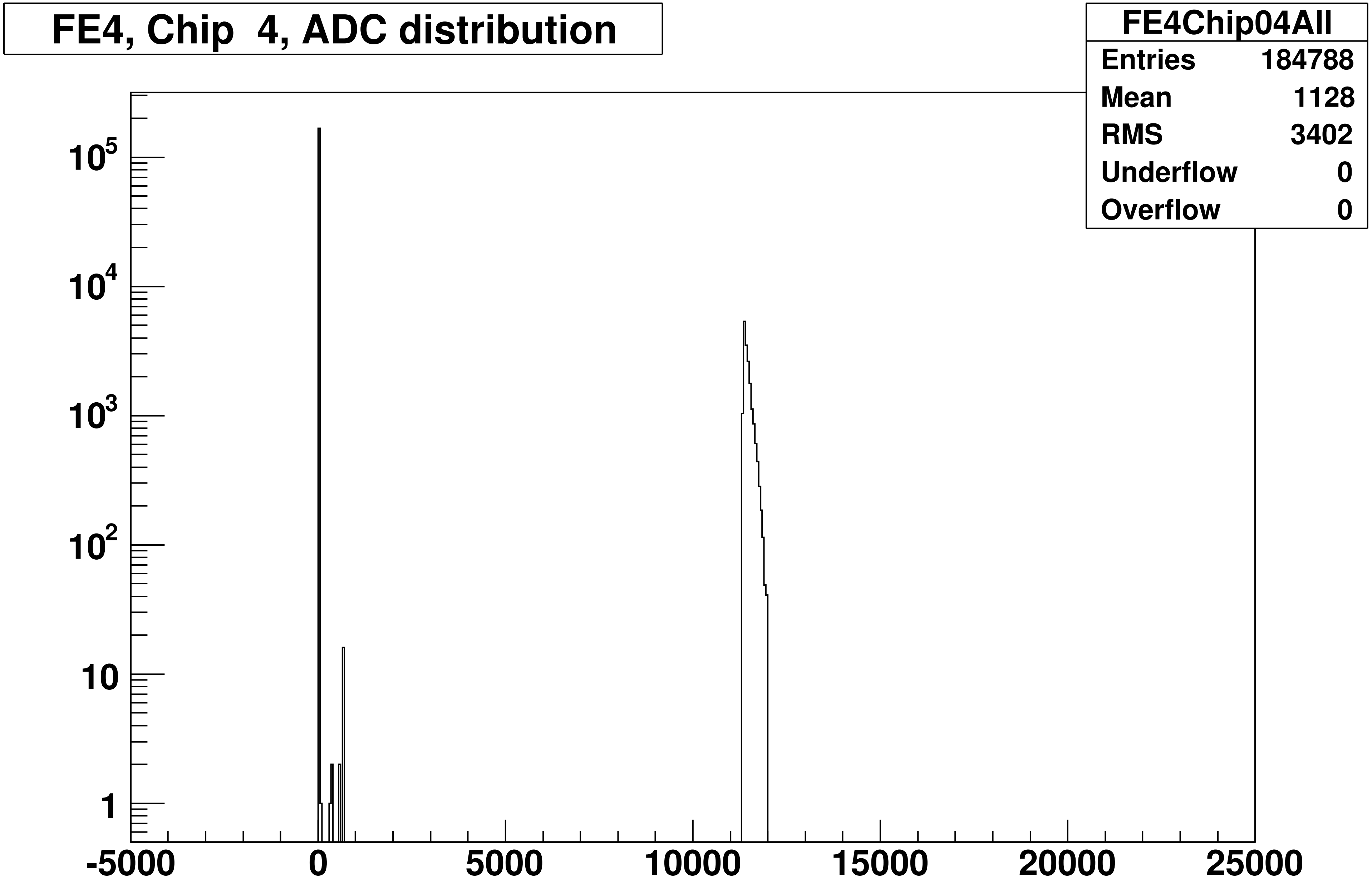
FE4, Chip 4, ADC distribution
FE4Chip04All
Entries 184788
Mean 1128
RMS 3402
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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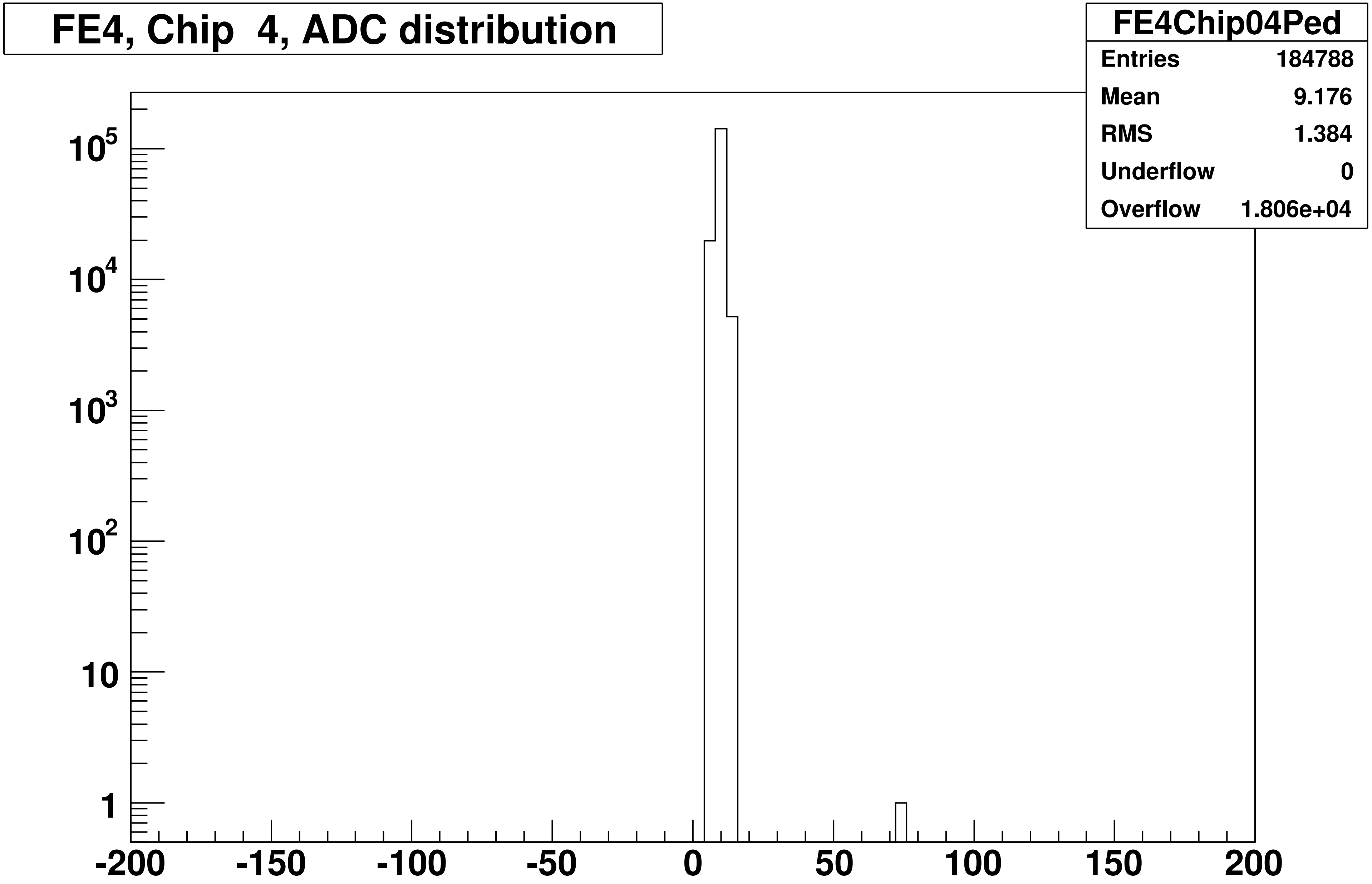
FE4, Chip 4, ADC distribution
FE4Chip04Ped
Entries 184788
Mean 9.176
RMS 1.384
Underflow 0
Overflow 1.806e+04
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10^3
10^2
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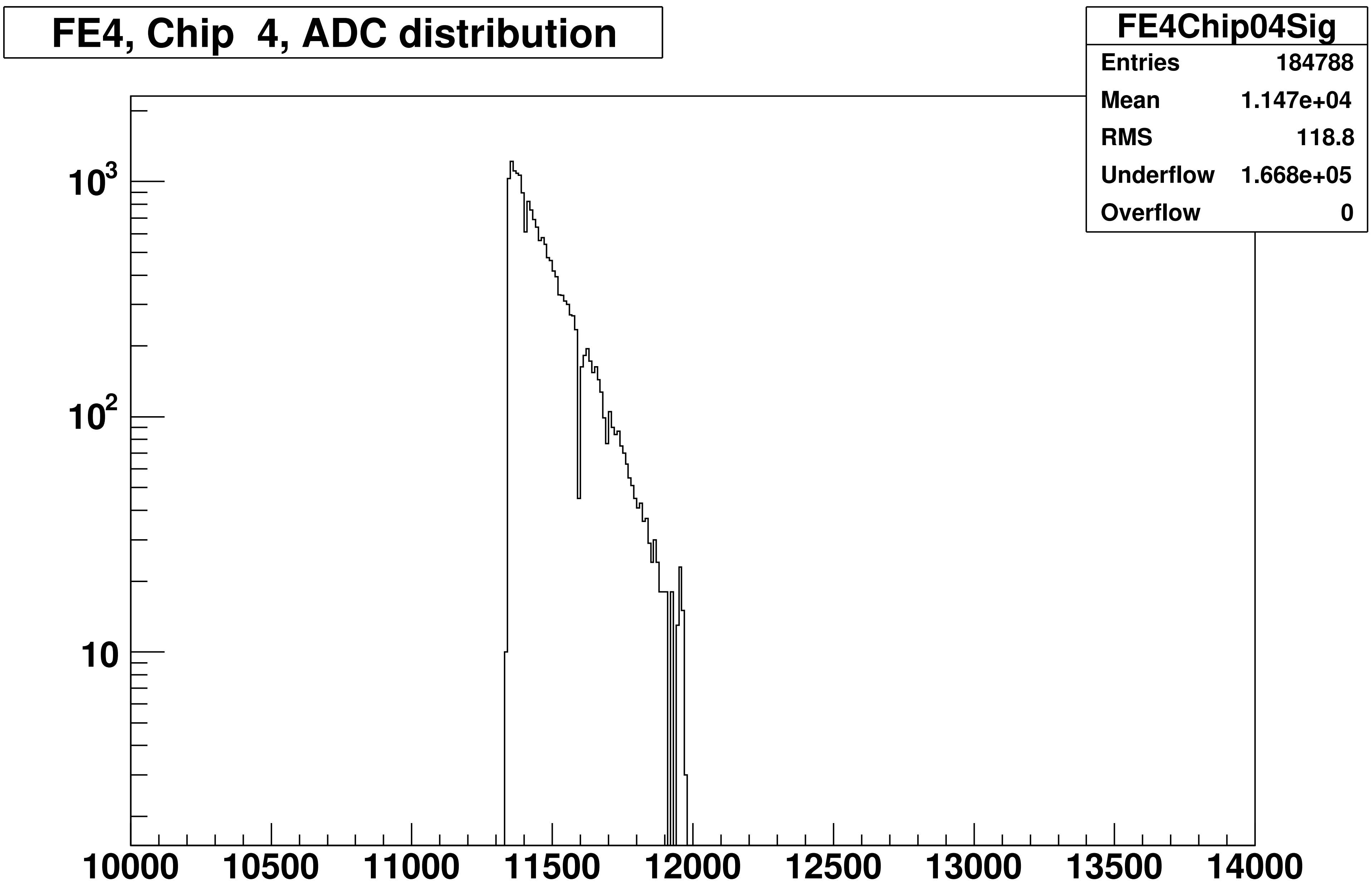
200


FE4, Chip 4, ADC distribution
FE4Chip04Sig
Entries 184788
Mean 1.147e+04
RMS 118.8
Underflow 1.668e+05
Overflow 0
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10^2
10
10000
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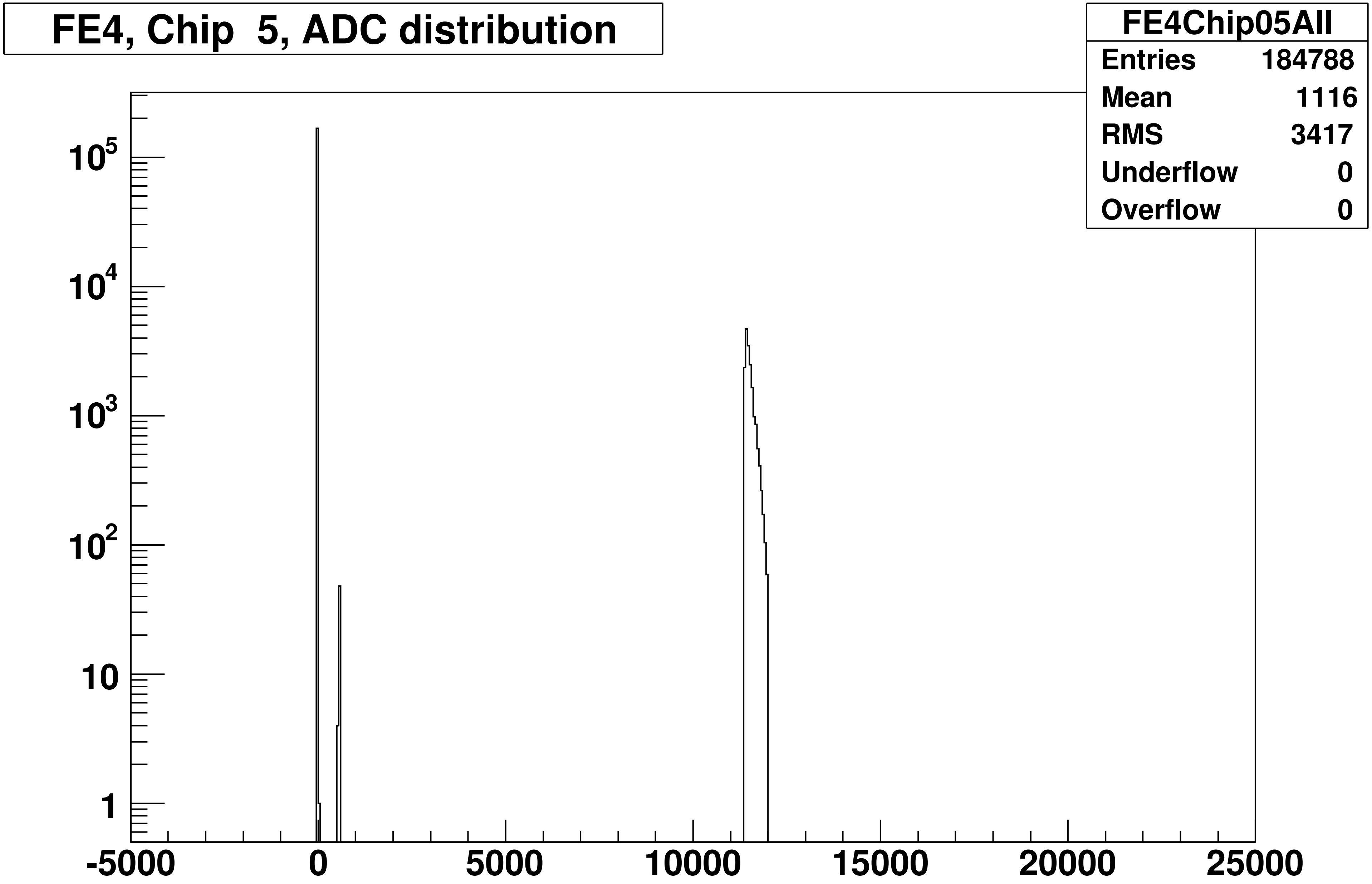
FE4, Chip 5, ADC distribution
FE4Chip05All
Entries 184788
Mean 1116
RMS 3417
Underflow 0
Overflow 0
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10^4
10^3
10^2
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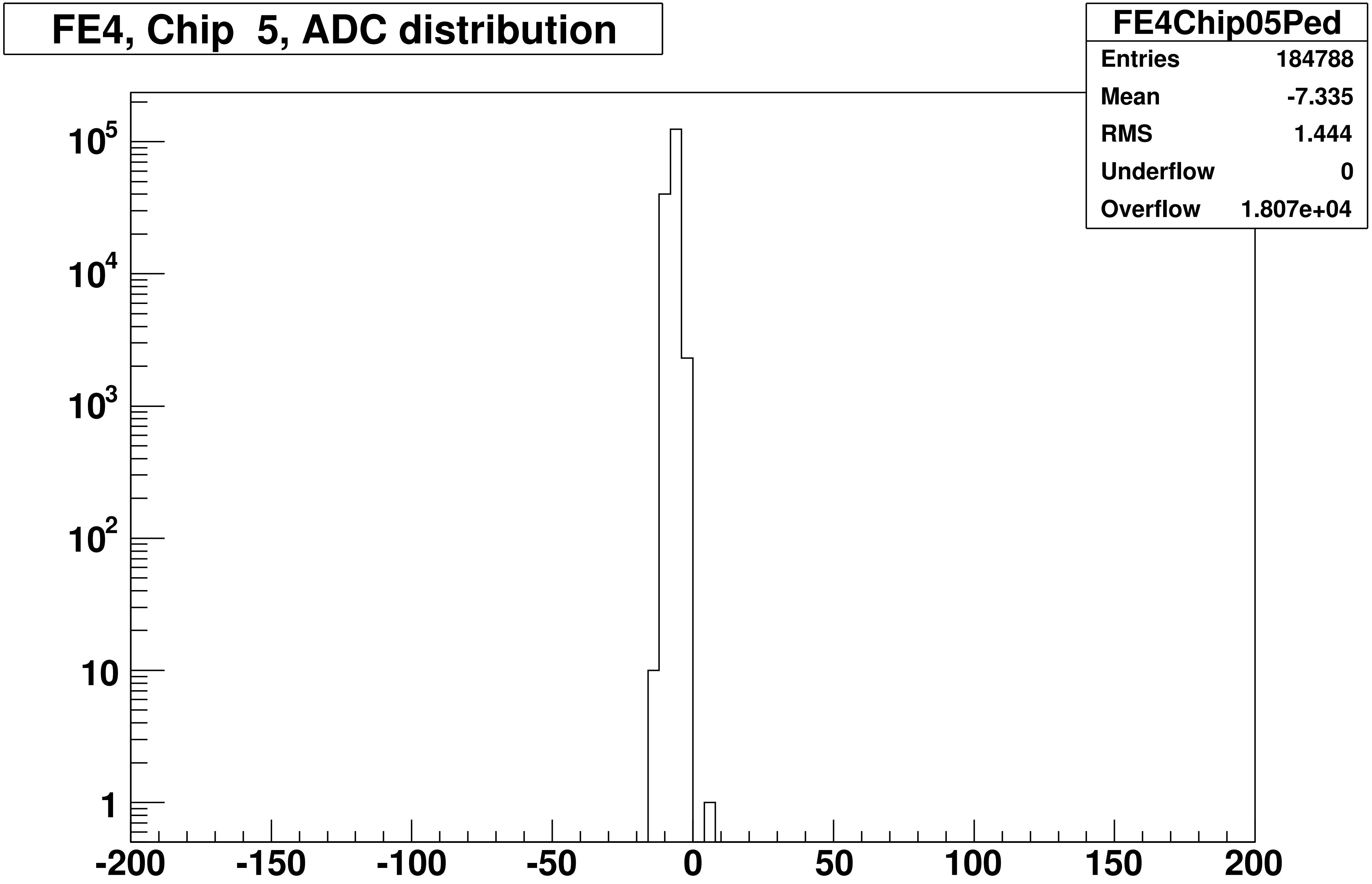

FE4, Chip 5, ADC distribution
FE4Chip05Ped
Entries 184788
Mean -7.335
RMS 1.444
Underflow 0
Overflow 1.807e+04
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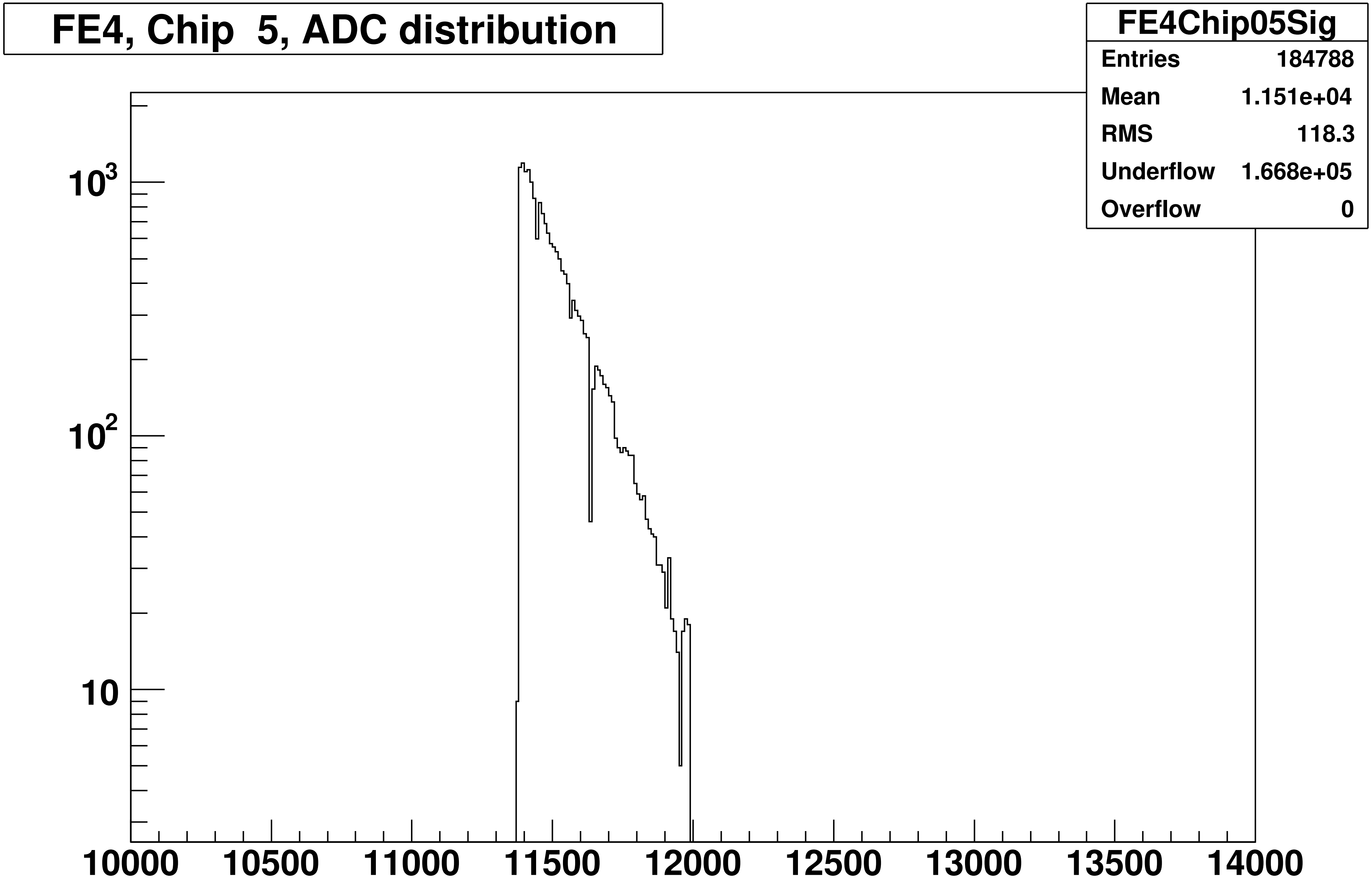
10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 5, ADC distribution
FE4Chip05Sig
Entries 184788
Mean 1.151e+04
RMS 118.3
Underflow 1.668e+05
Overflow 0
10³
10²
10
10000
10500
11000
11500
12000
12500
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13500
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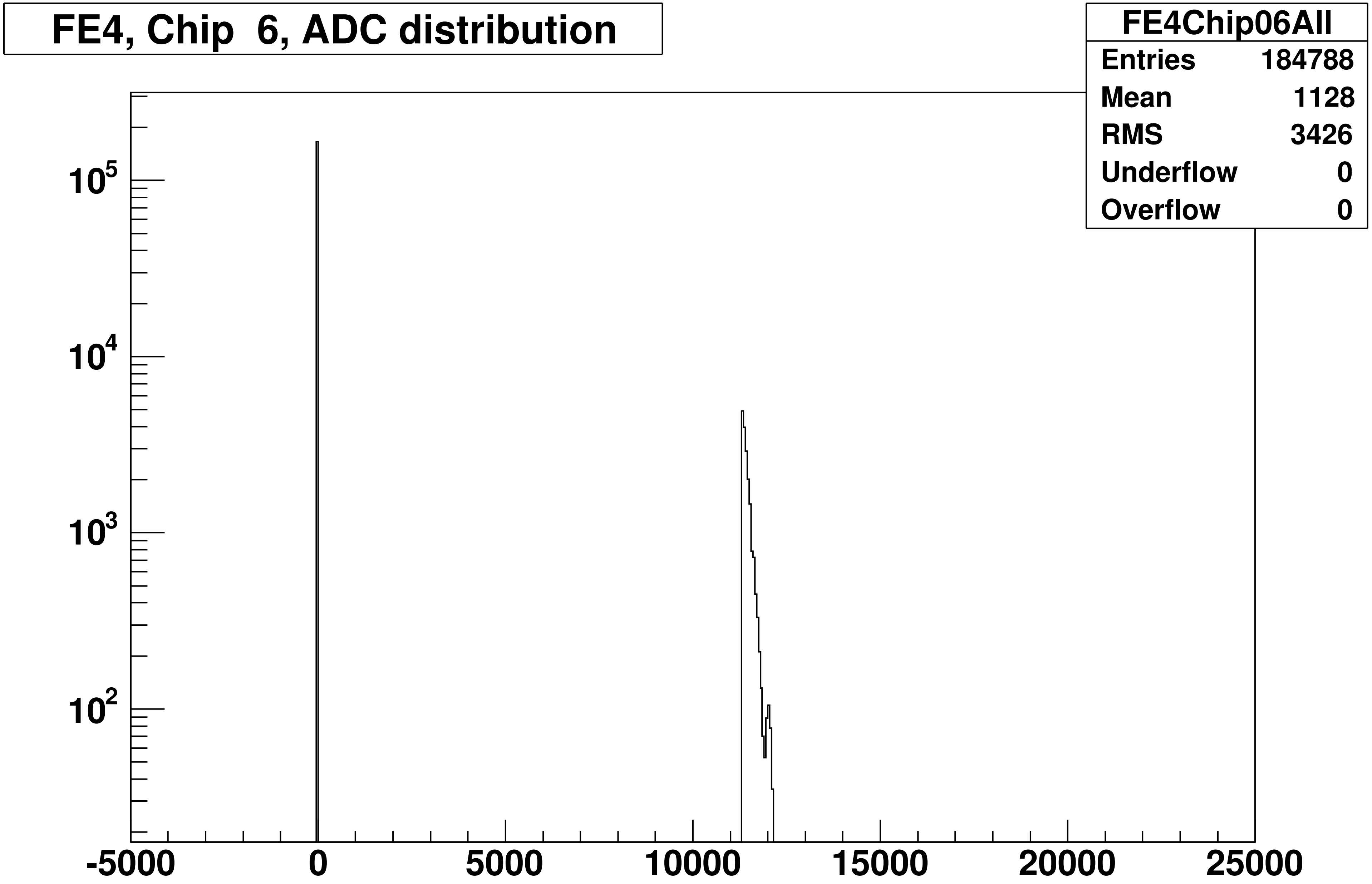
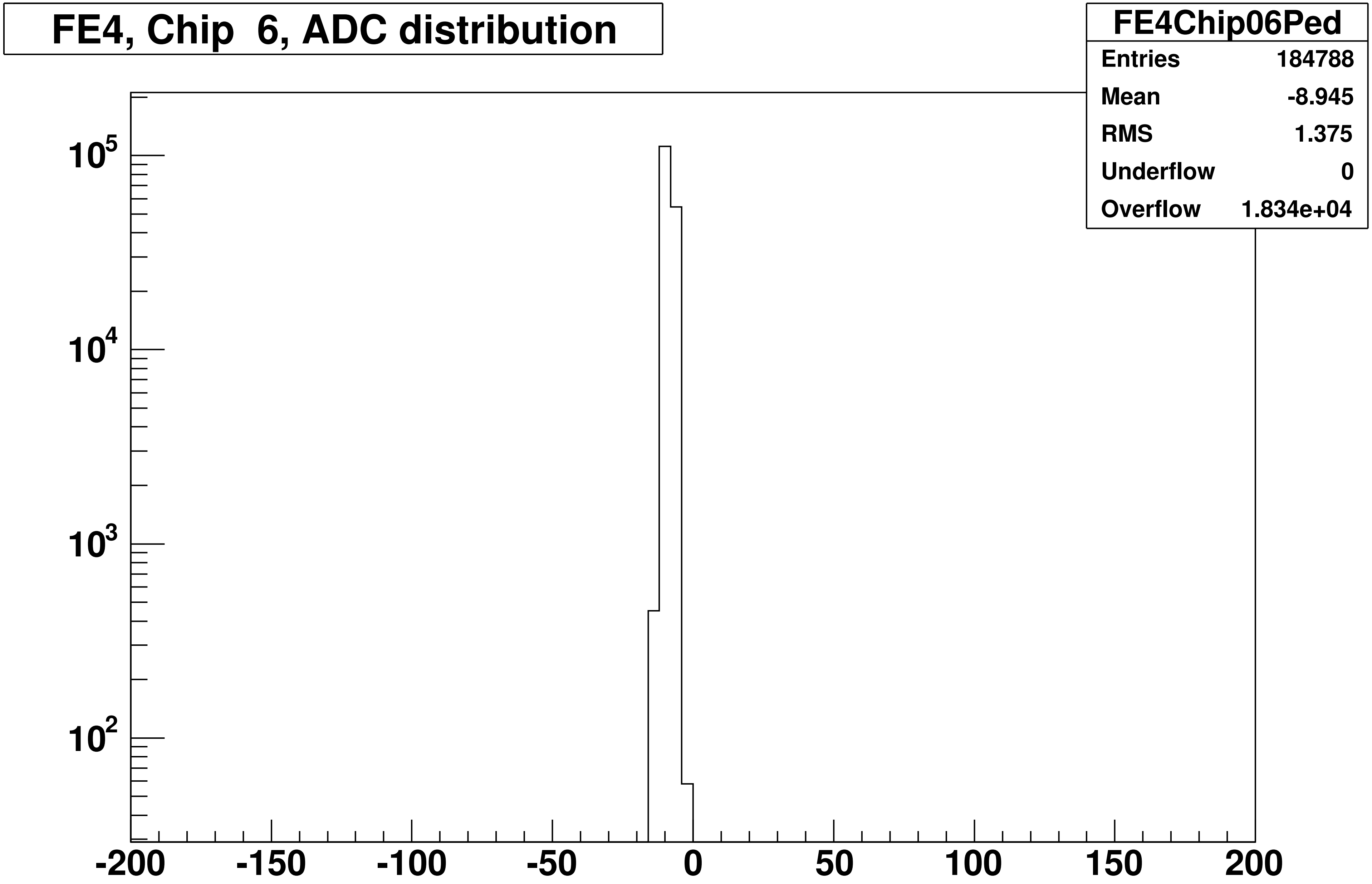


FE4, Chip 6, ADC distribution
FE4Chip06All
Entries 184788
Mean 1128
RMS 3426
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 6, ADC distribution
FE4Chip06Ped
Entries 184788
Mean -8.945
RMS 1.375
Underflow 0
Overflow 1.834e+04
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10^4
10^3
10^2
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-100
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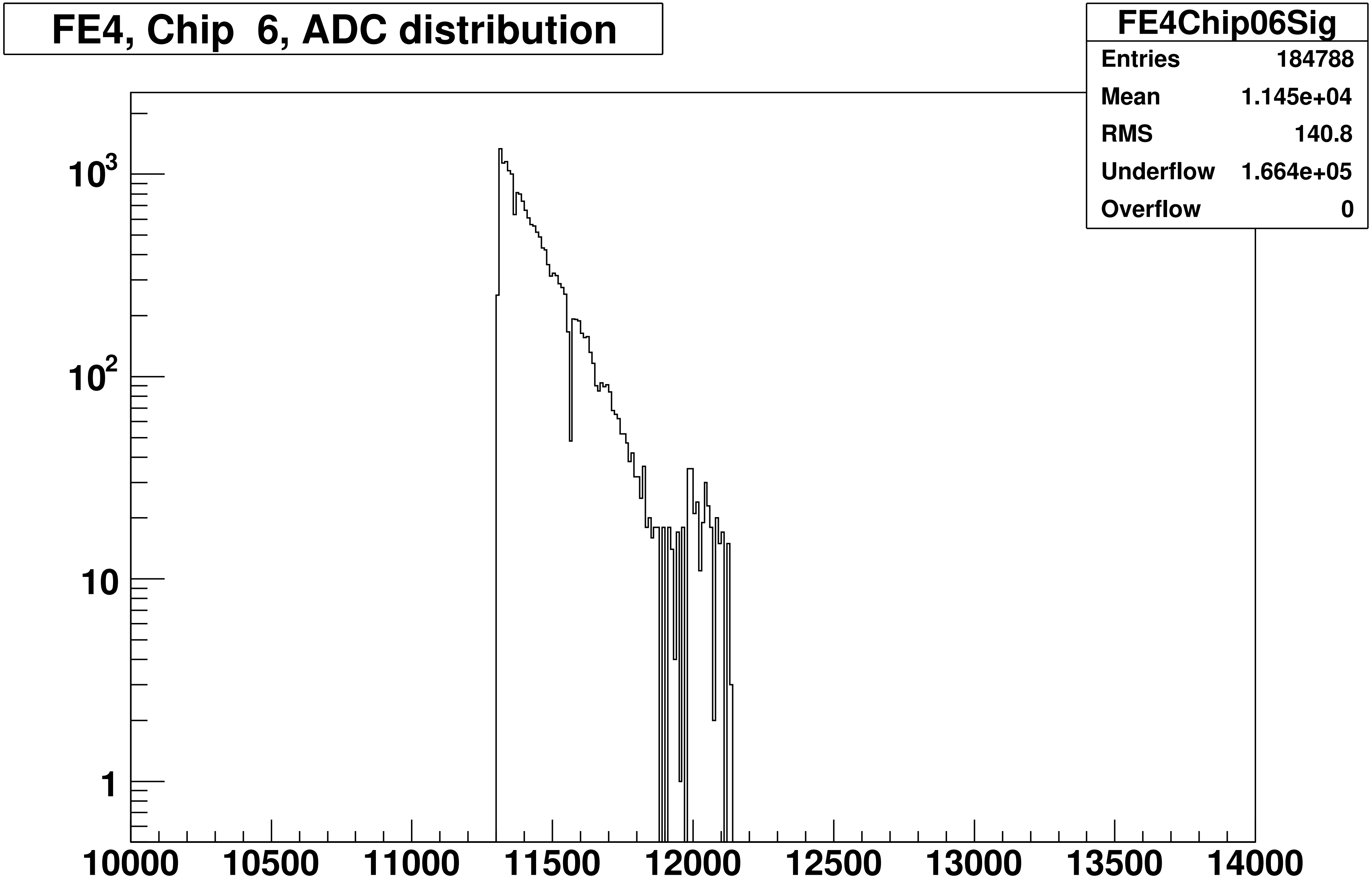
0
50
100
150
200


FE4, Chip 6, ADC distribution
FE4Chip06Sig
Entries 184788
Mean 1.145e+04
RMS 140.8
Underflow 1.664e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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13000
13500
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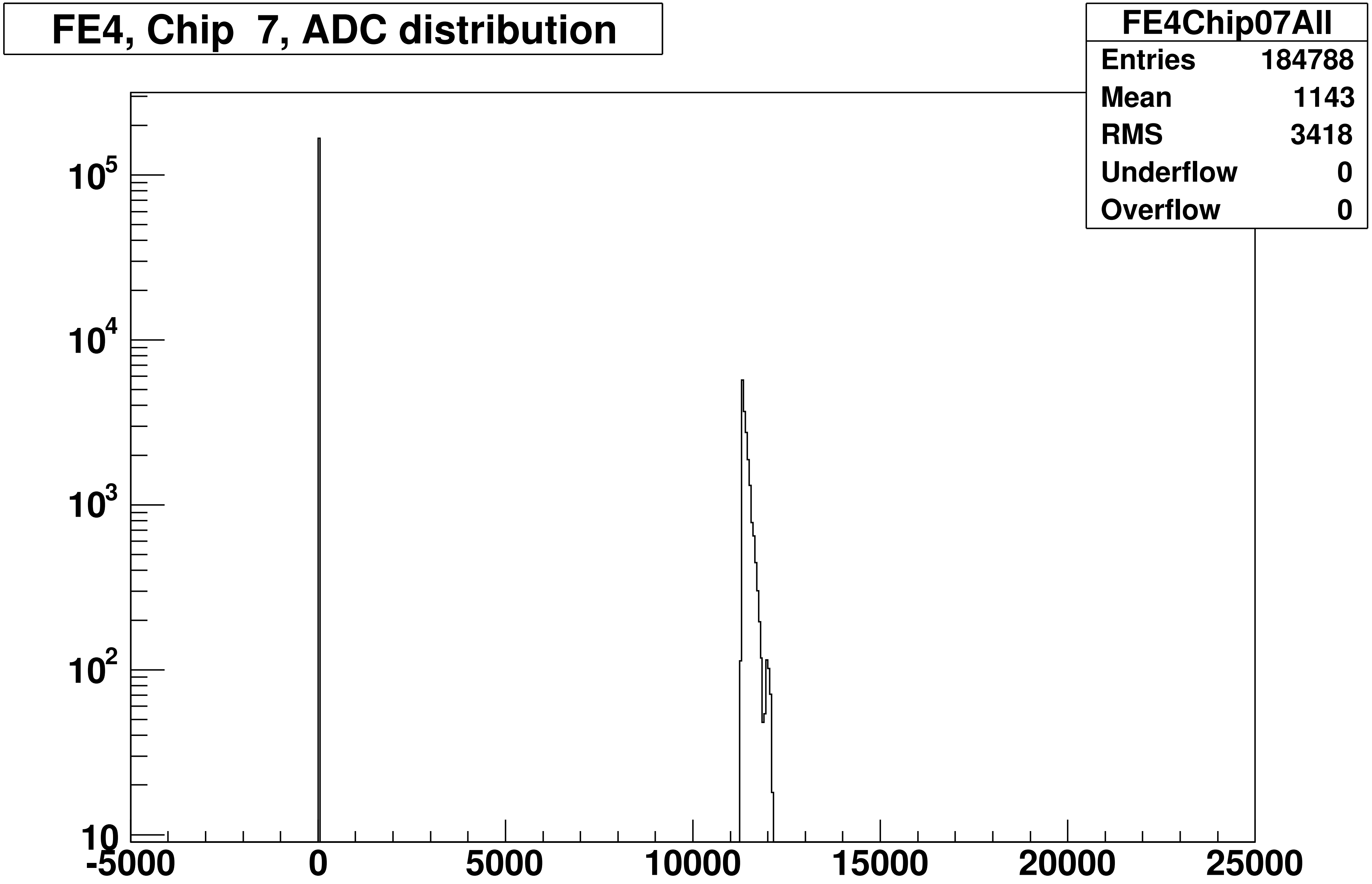
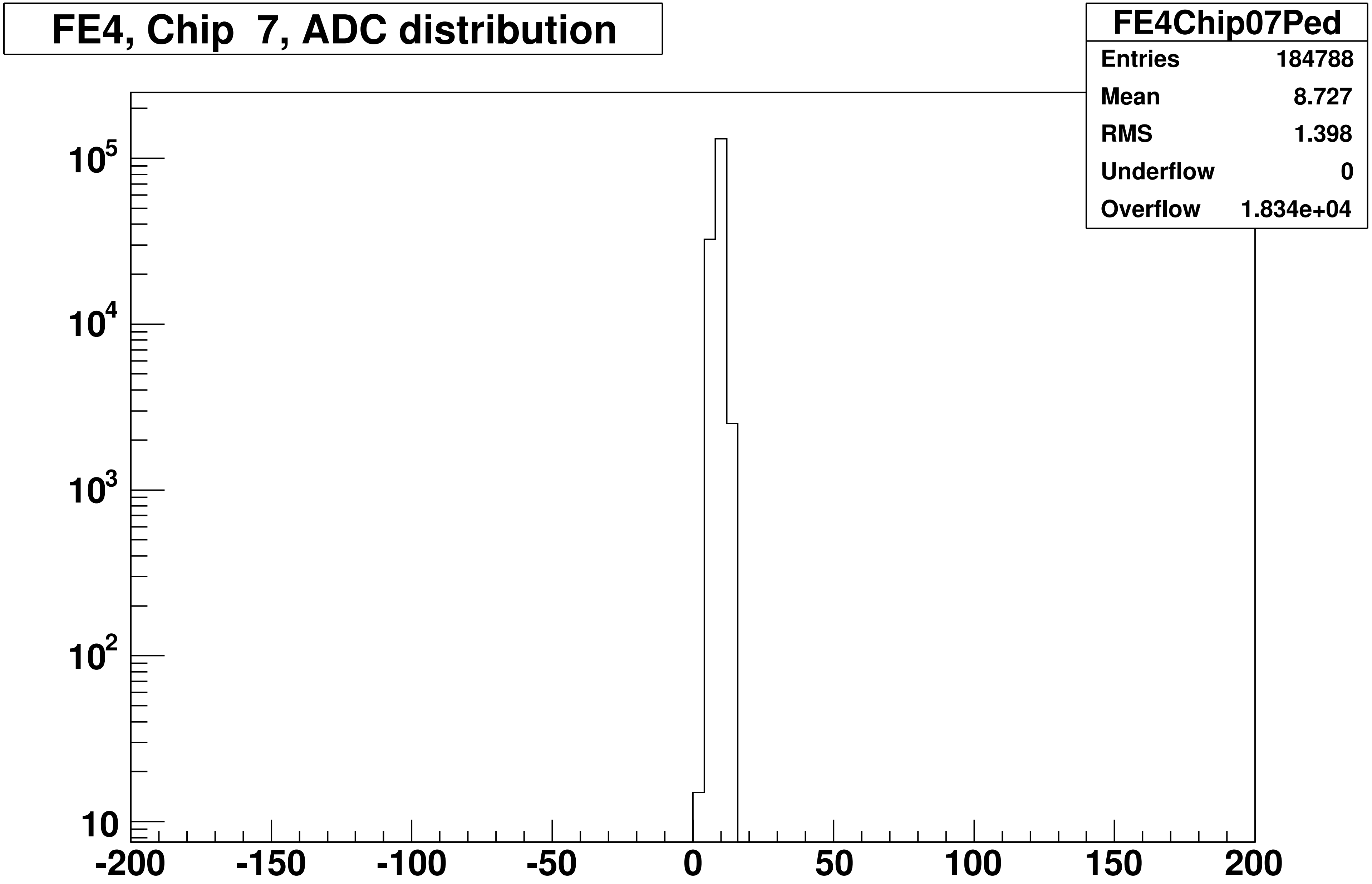

FE4, Chip 7, ADC distribution
FE4Chip07All
Entries 184788
Mean 1143
RMS 3418
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 7, ADC distribution
FE4Chip07Ped
Entries 184788
Mean 8.727
RMS 1.398
Underflow 0
Overflow 1.834e+04
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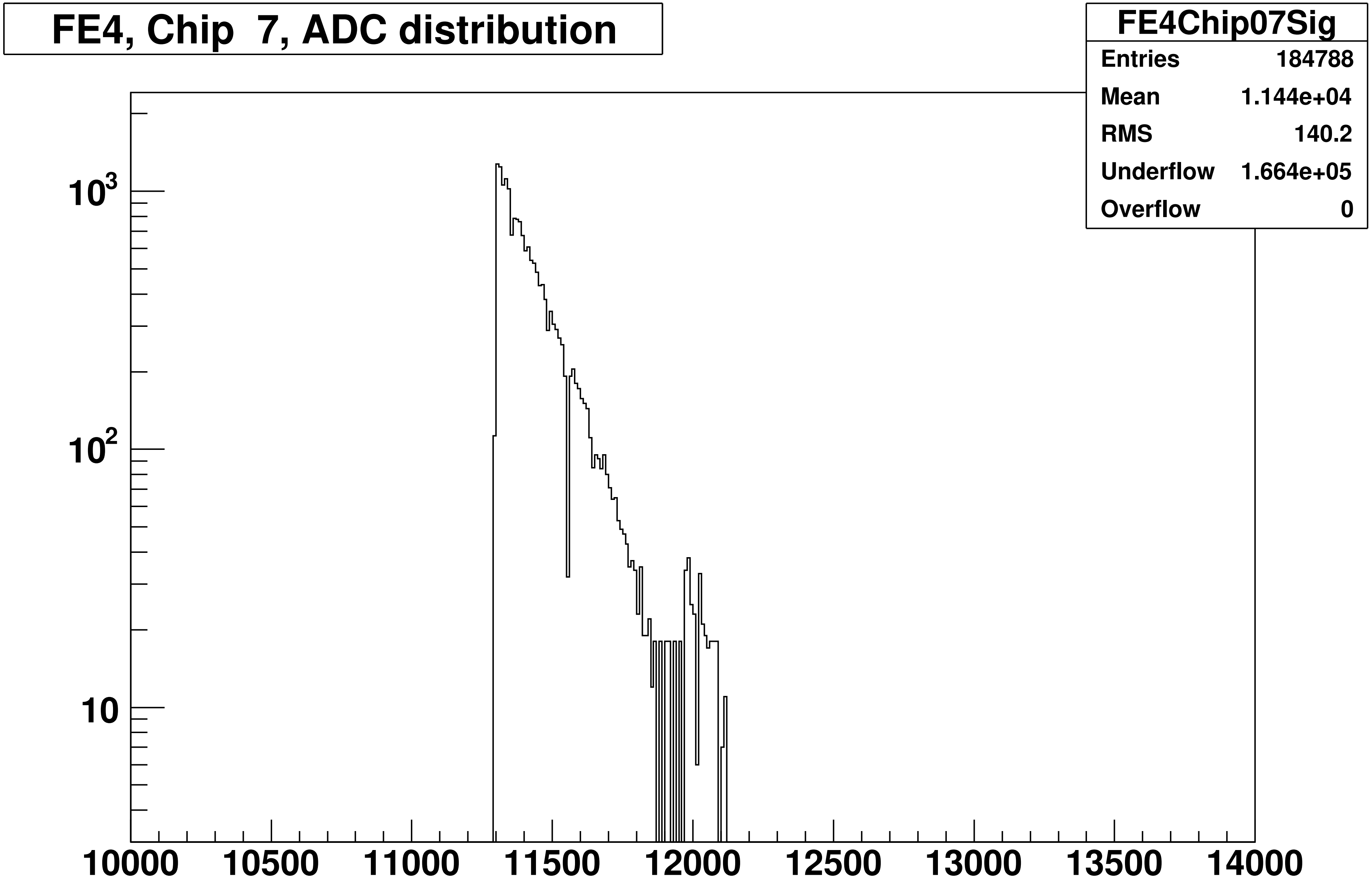
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 7, ADC distribution
FE4Chip07Sig
Entries 184788
Mean 1.144e+04
RMS 140.2
Underflow 1.664e+05
Overflow 0
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10^2
10
10000
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11500
12000
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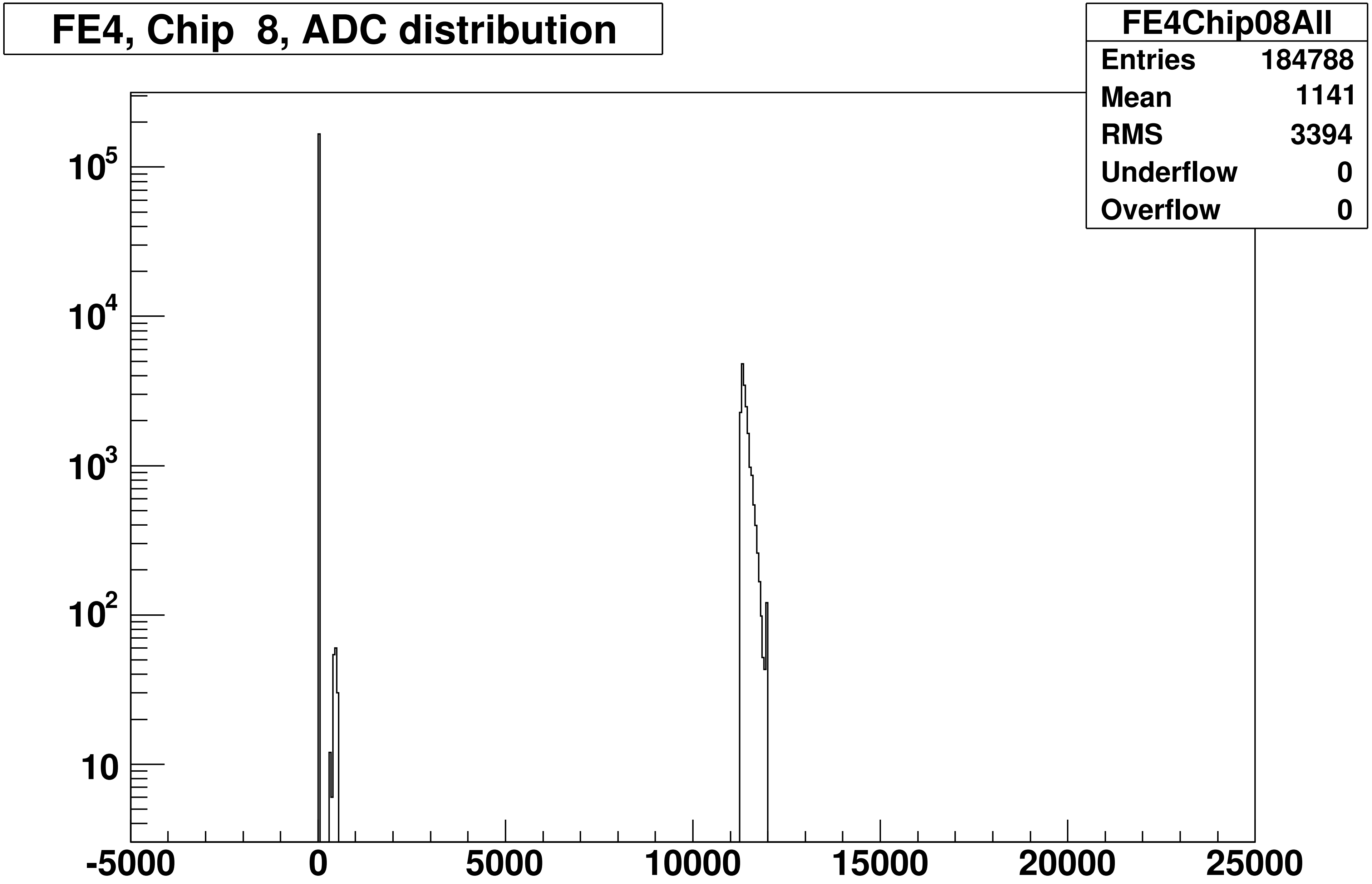
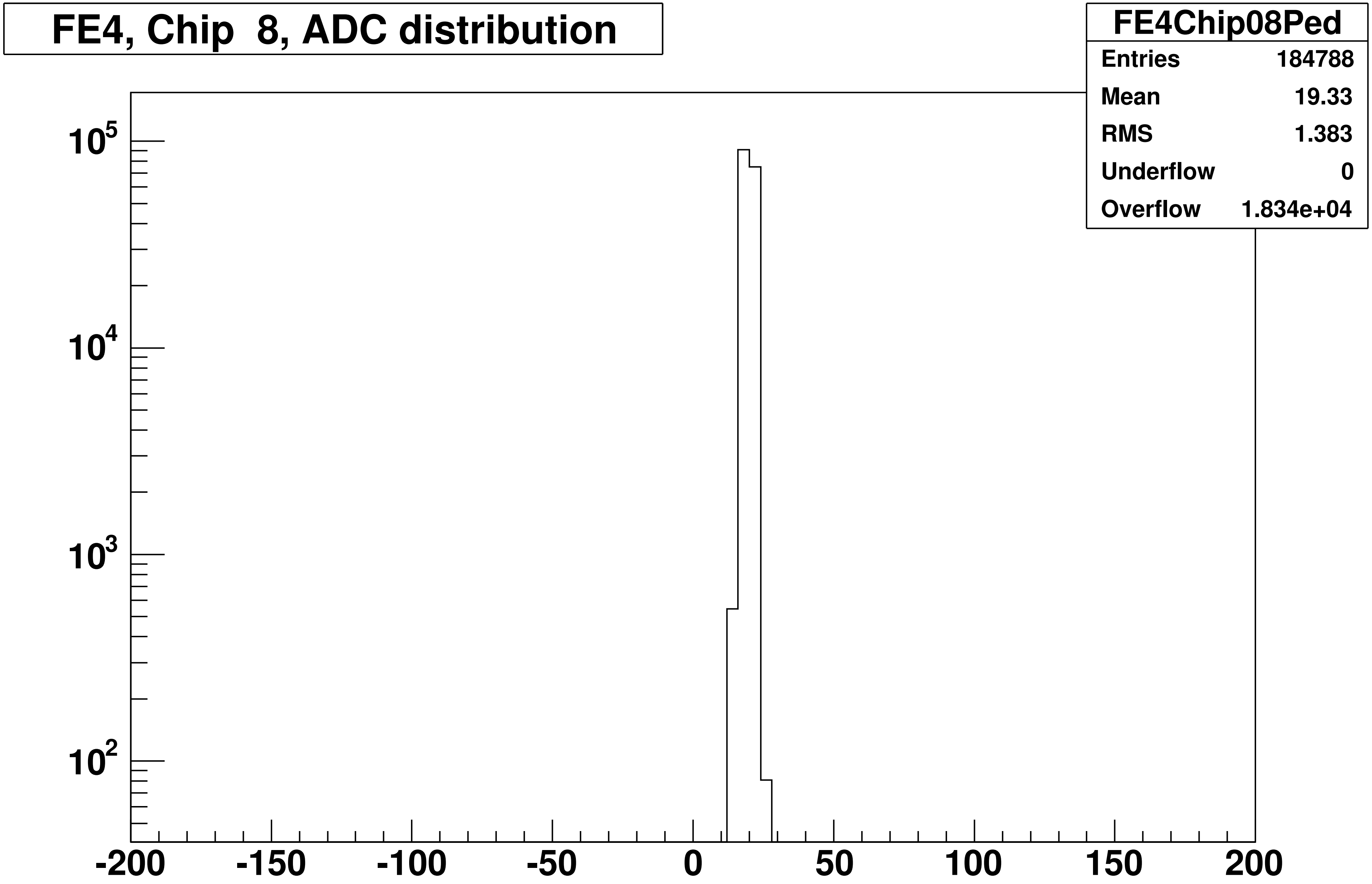


FE4, Chip 8, ADC distribution
FE4Chip08All
Entries 184788
Mean 1141
RMS 3394
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE4, Chip 8, ADC distribution
FE4Chip08Ped
Entries 184788
Mean 19.33
RMS 1.383
Underflow 0
Overflow 1.834e+04
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10^4
10^3
10^2
-200
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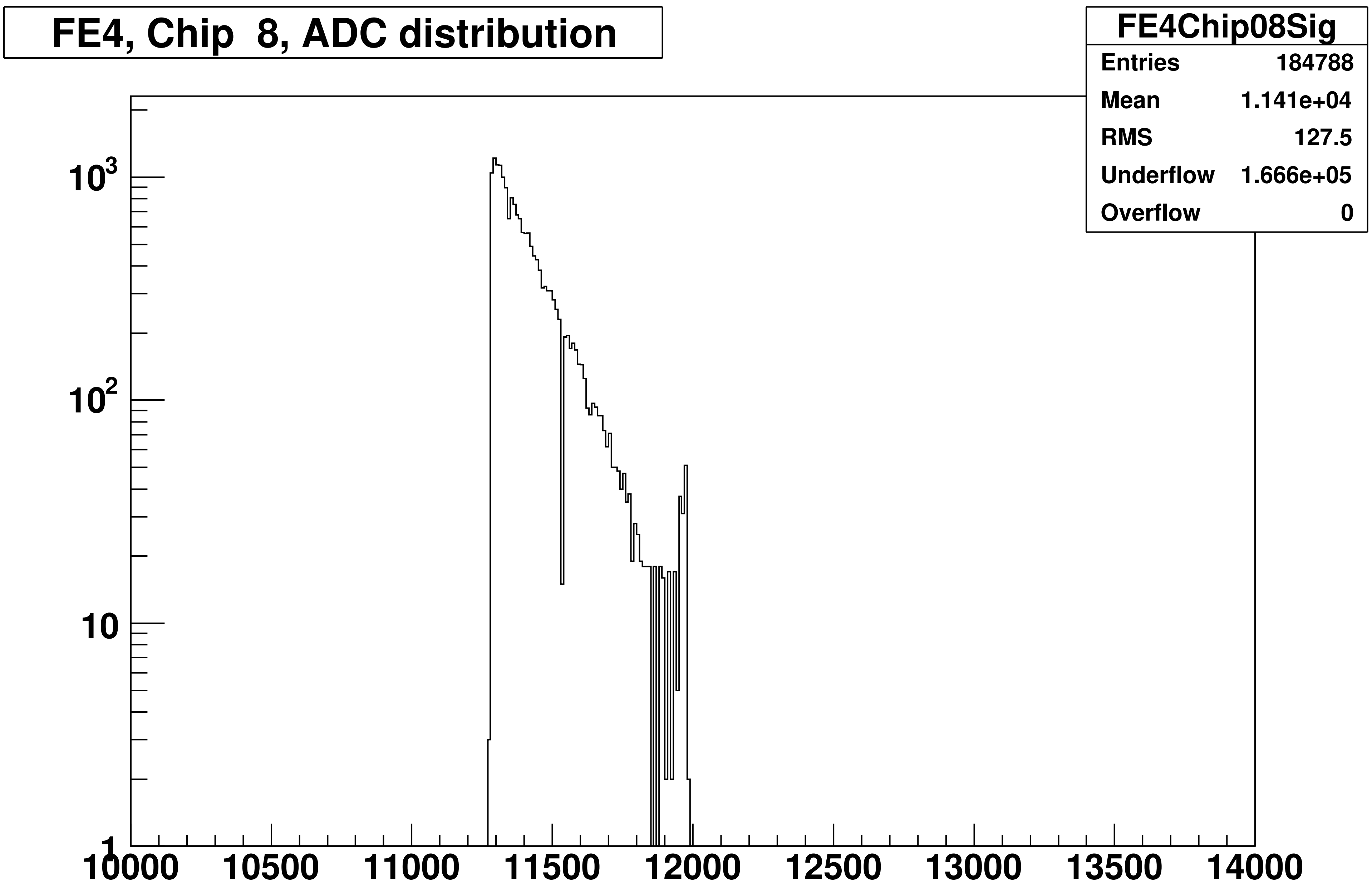
-100
-50
0
50
100
150
200


FE4, Chip 8, ADC distribution
FE4Chip08Sig
Entries 184788
Mean 1.141e+04
RMS 127.5
Underflow 1.666e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
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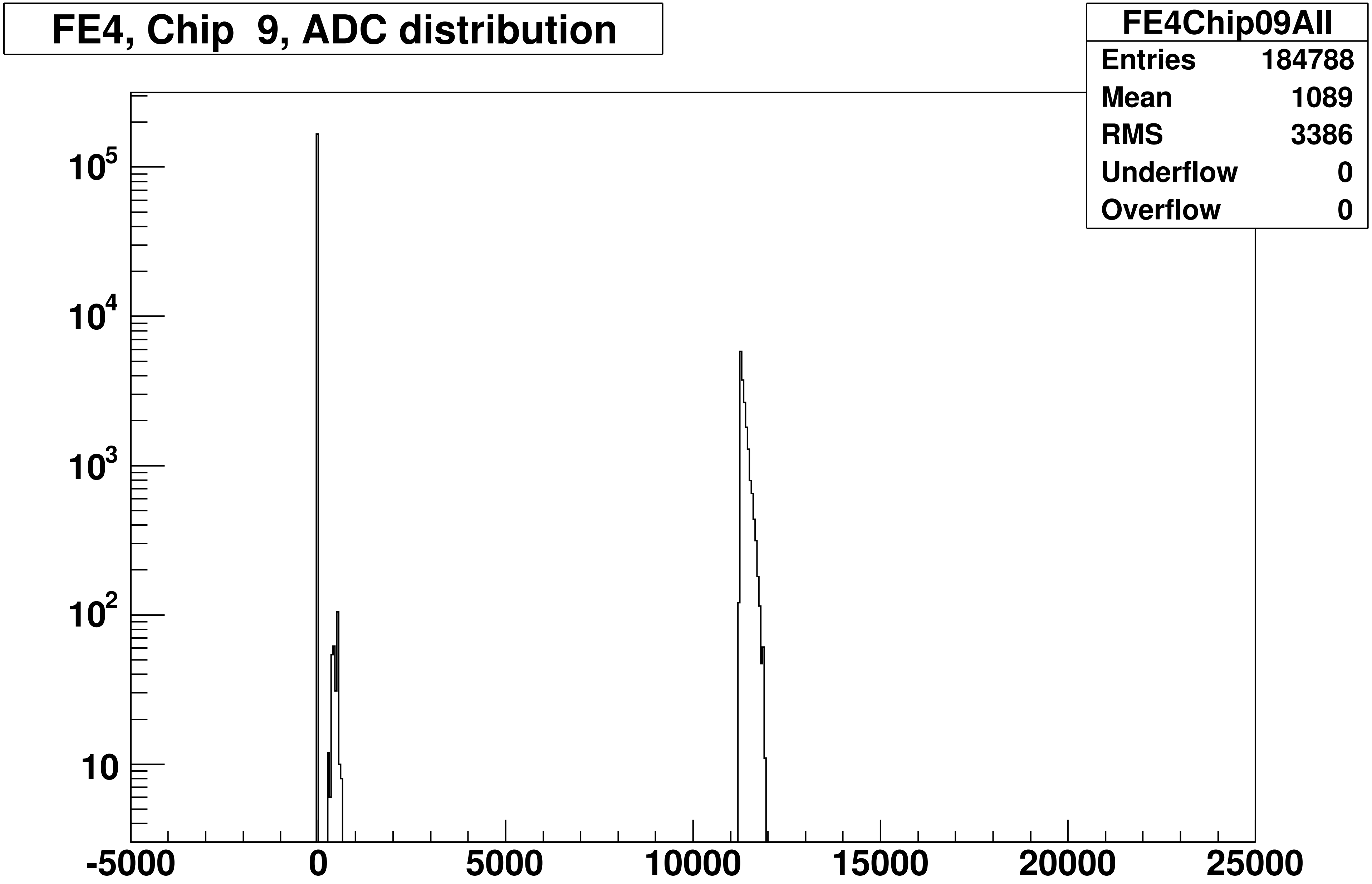
FE4, Chip 9, ADC distribution
FE4Chip09All
Entries 184788
Mean 1089
RMS 3386
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
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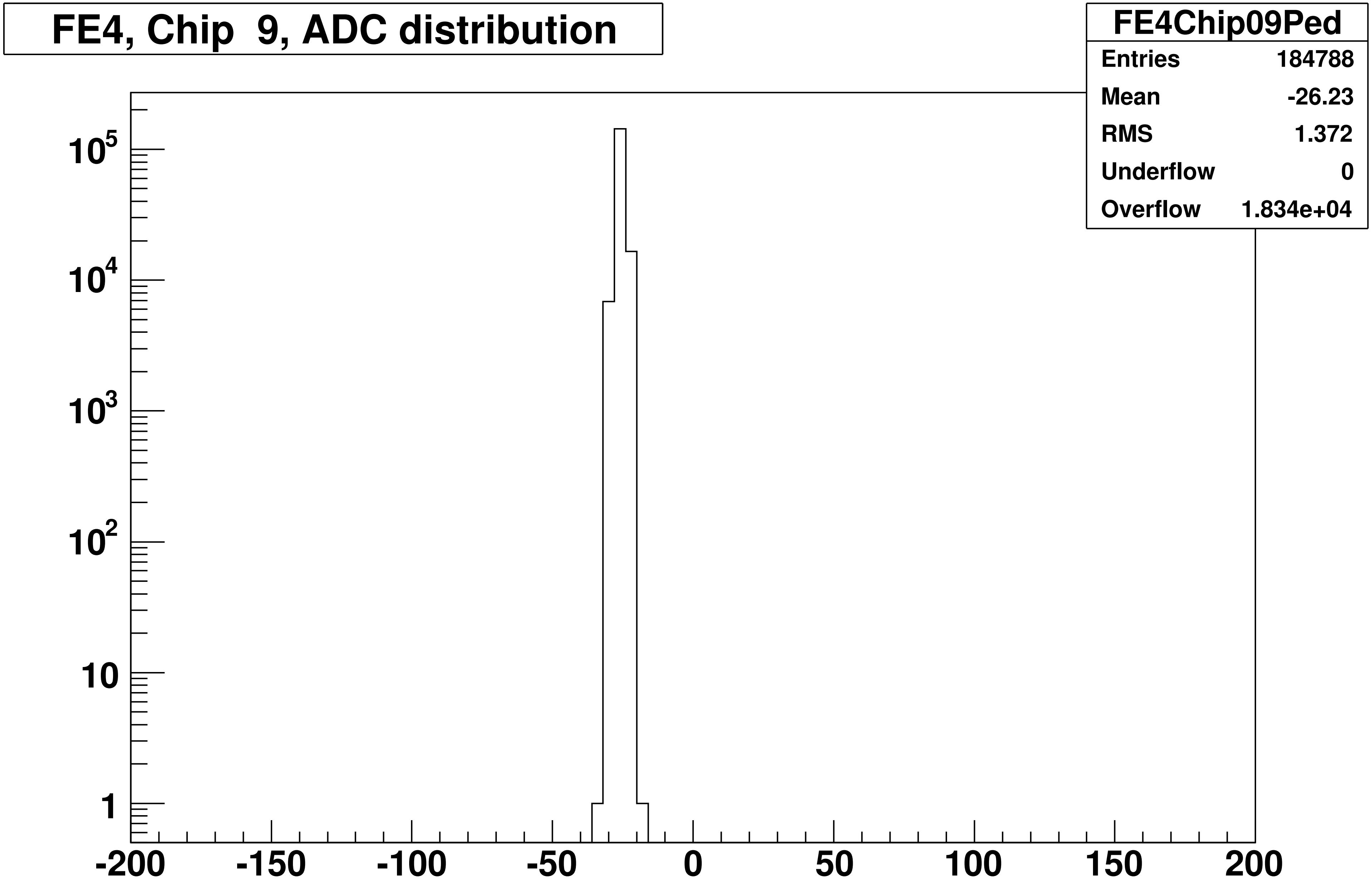
5000
10000
15000
20000
25000



FE4, Chip 9, ADC distribution
FE4Chip09Ped
Entries 184788
Mean -26.23
RMS 1.372
Underflow 0
Overflow 1.834e+04
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10^4
10^3
10^2
10
1
-200
-150
-100
-50
0
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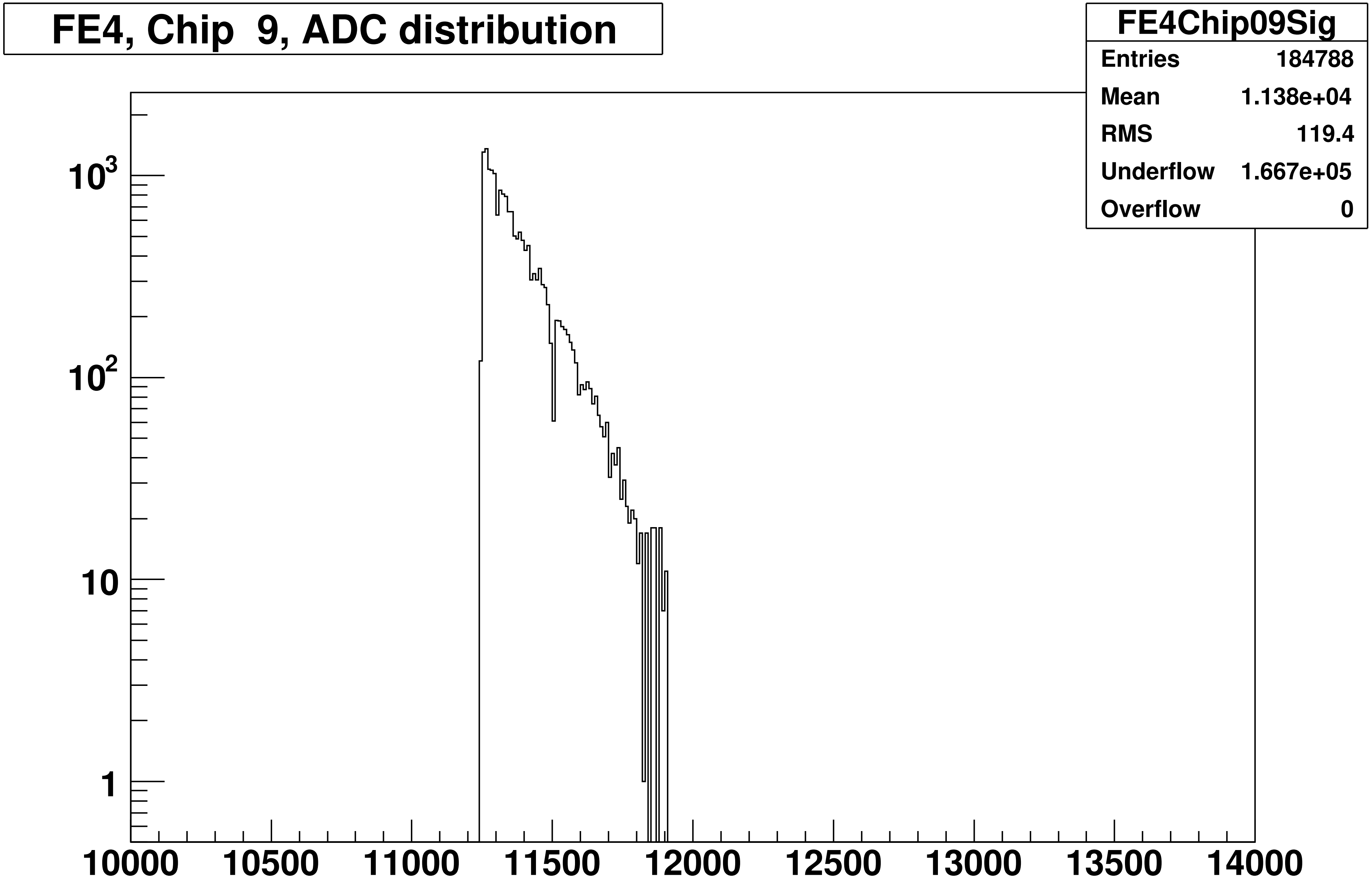
100
150
200


FE4, Chip 9, ADC distribution
FE4Chip09Sig
Entries 184788
Mean 1.138e+04
RMS 119.4
Underflow 1.667e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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13500
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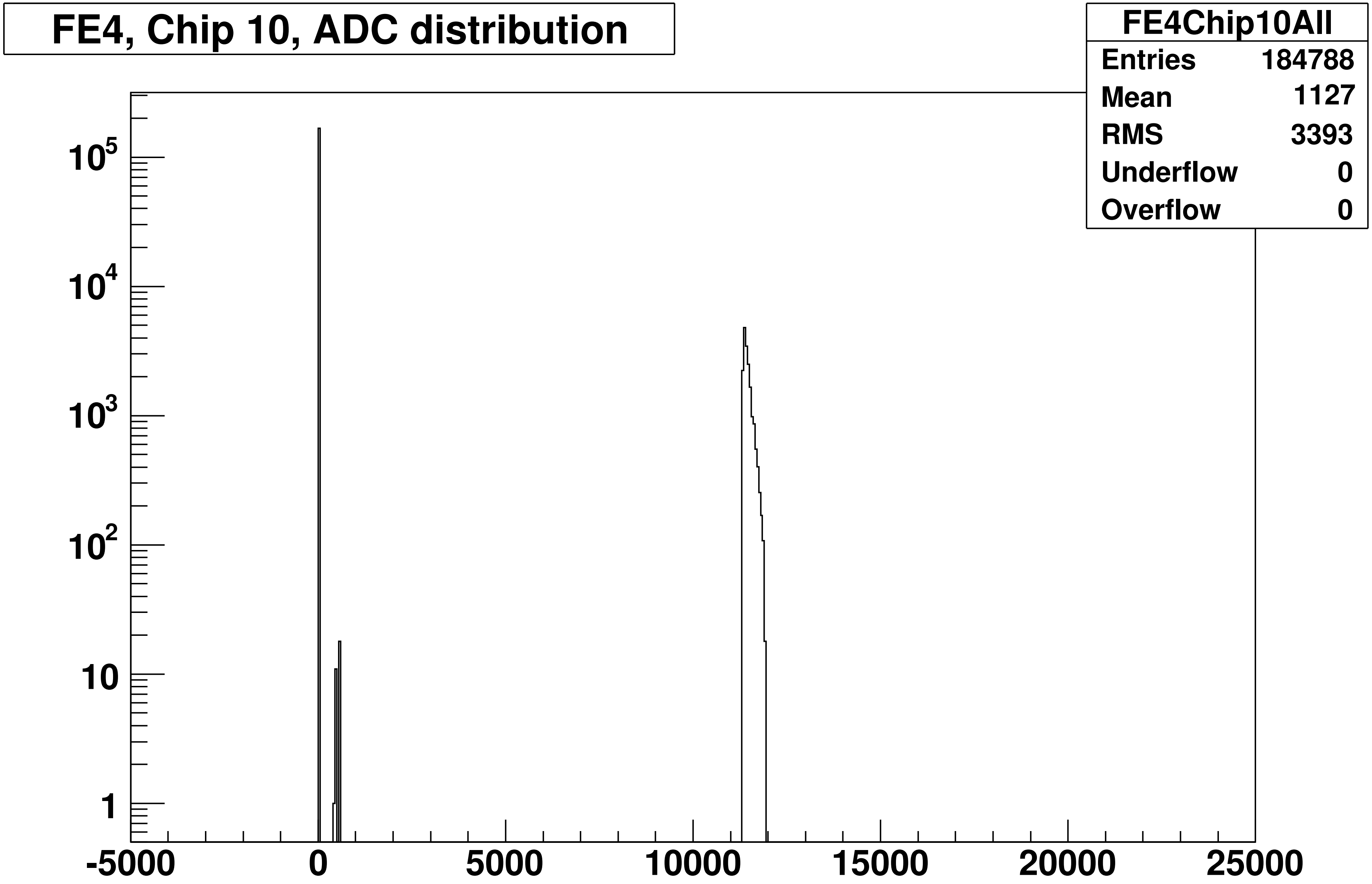
FE4, Chip 10, ADC distribution
FE4Chip10All
Entries 184788
Mean 1127
RMS 3393
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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10000
15000
20000
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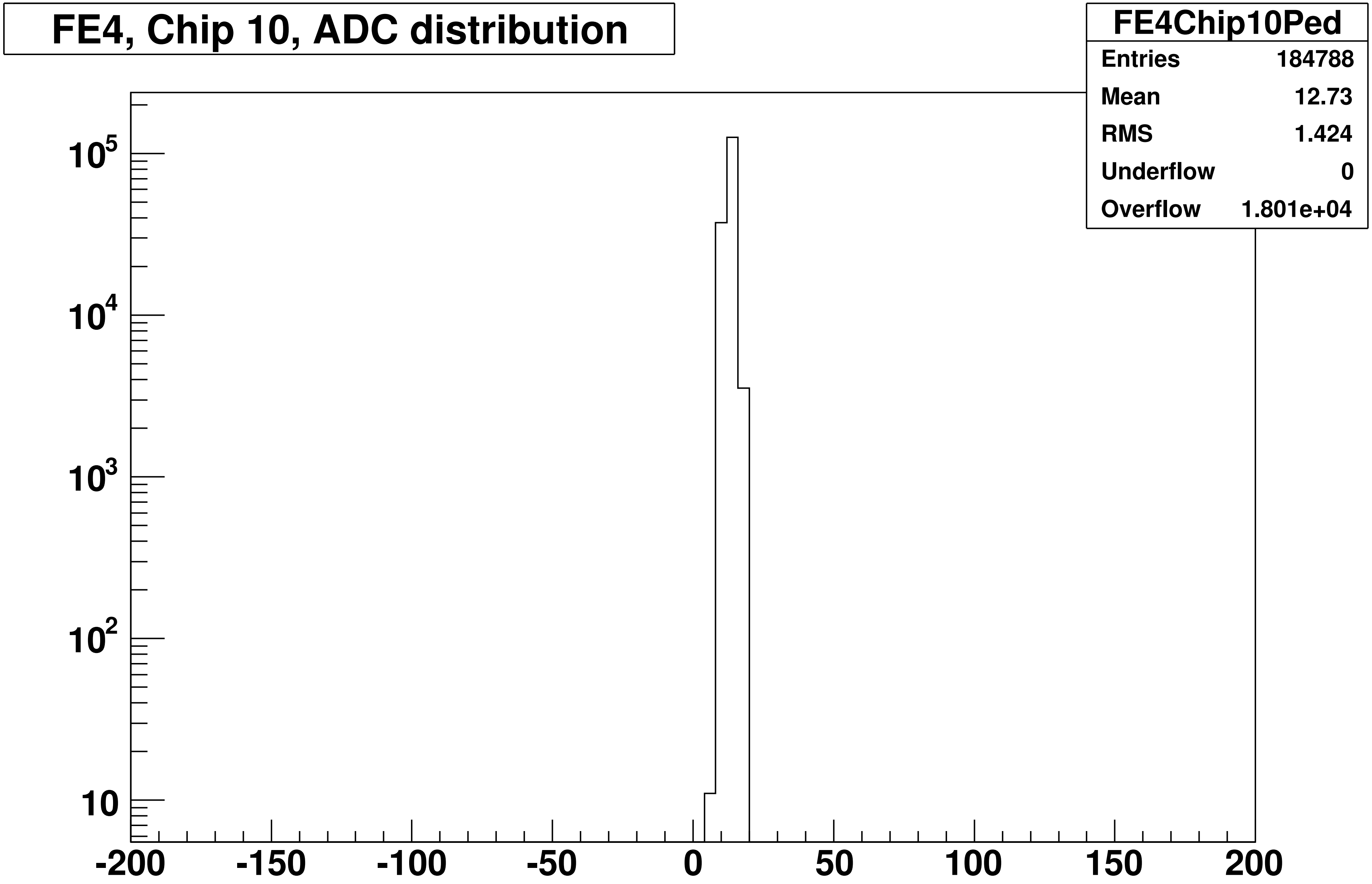
FE4, Chip 10, ADC distribution
FE4Chip10Ped
Entries 184788
Mean 12.73
RMS 1.424
Underflow 0
Overflow 1.801e+04
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10^2
10^3
10^4
10^5
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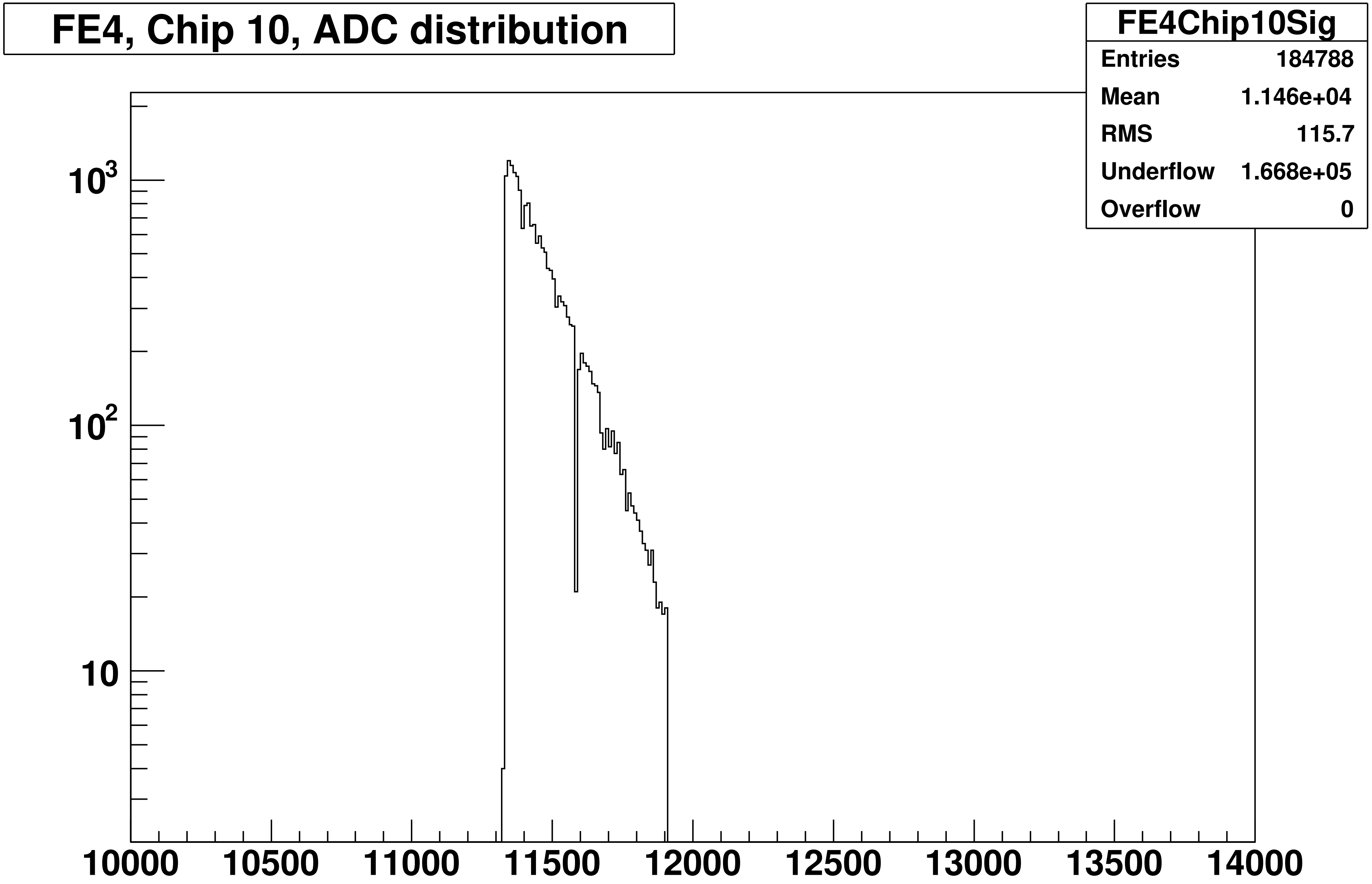
-150
-100
-50
0
50
100
150
200


FE4, Chip 10, ADC distribution
FE4Chip10Sig
Entries 184788
Mean 1.146e+04
RMS 115.7
Underflow 1.668e+05
Overflow 0
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10^2
10
10000
10500
11000
11500
12000
12500
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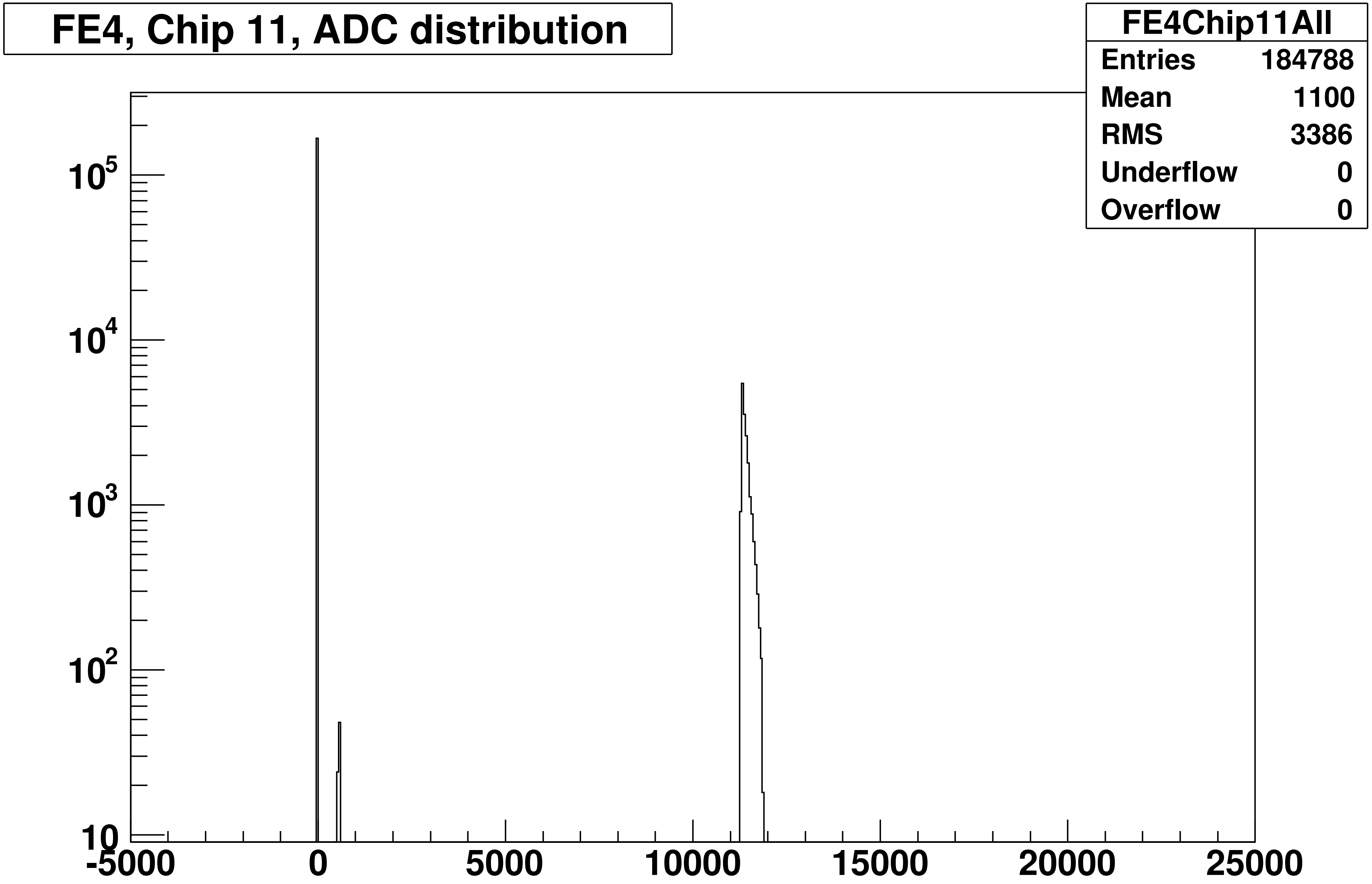
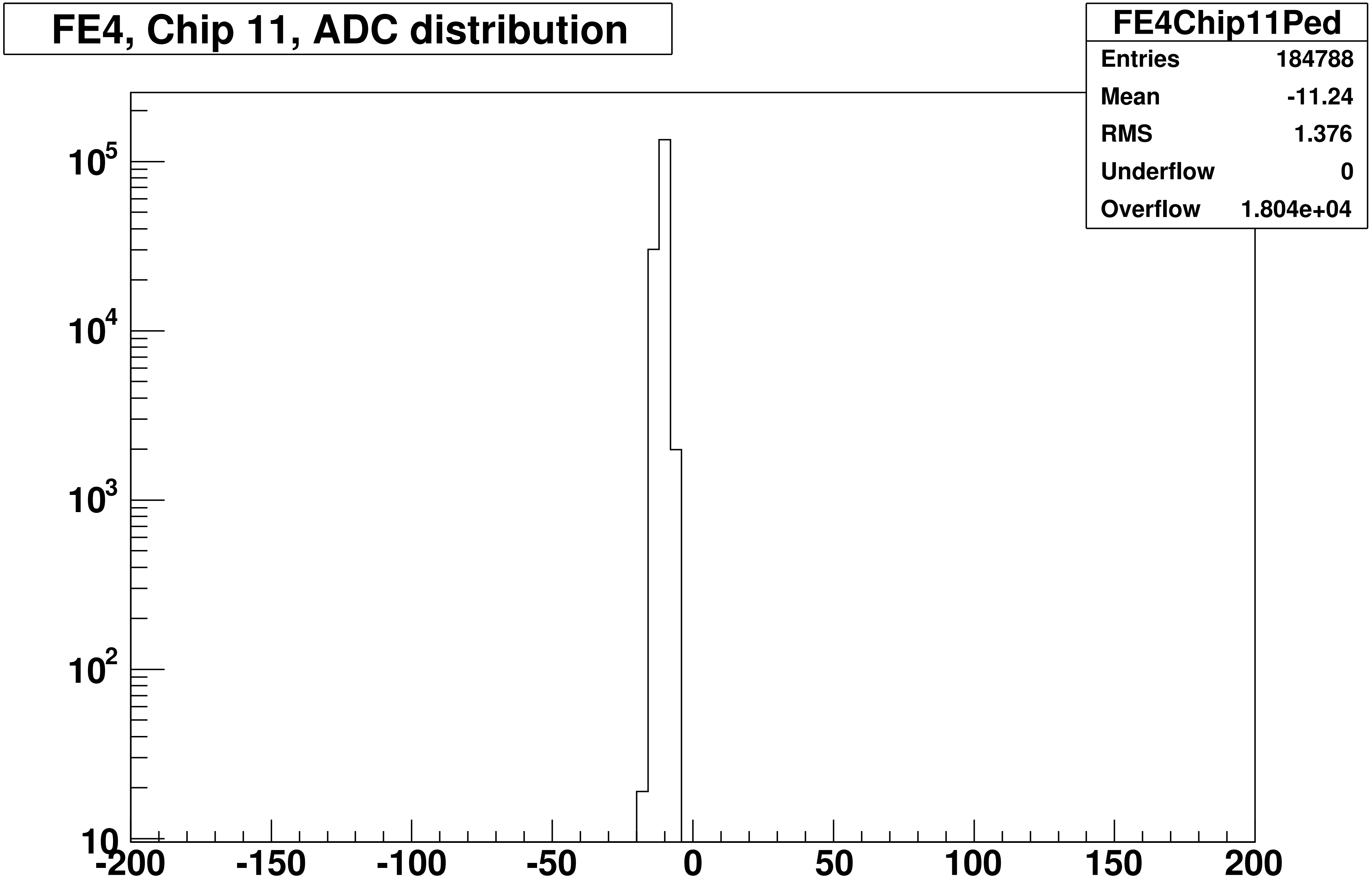
13500
14000


FE4, Chip 11, ADC distribution
FE4Chip11All
Entries 184788
Mean 1100
RMS 3386
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000



FE4, Chip 11, ADC distribution
FE4Chip11Ped
Entries 184788
Mean -11.24
RMS 1.376
Underflow 0
Overflow 1.804e+04
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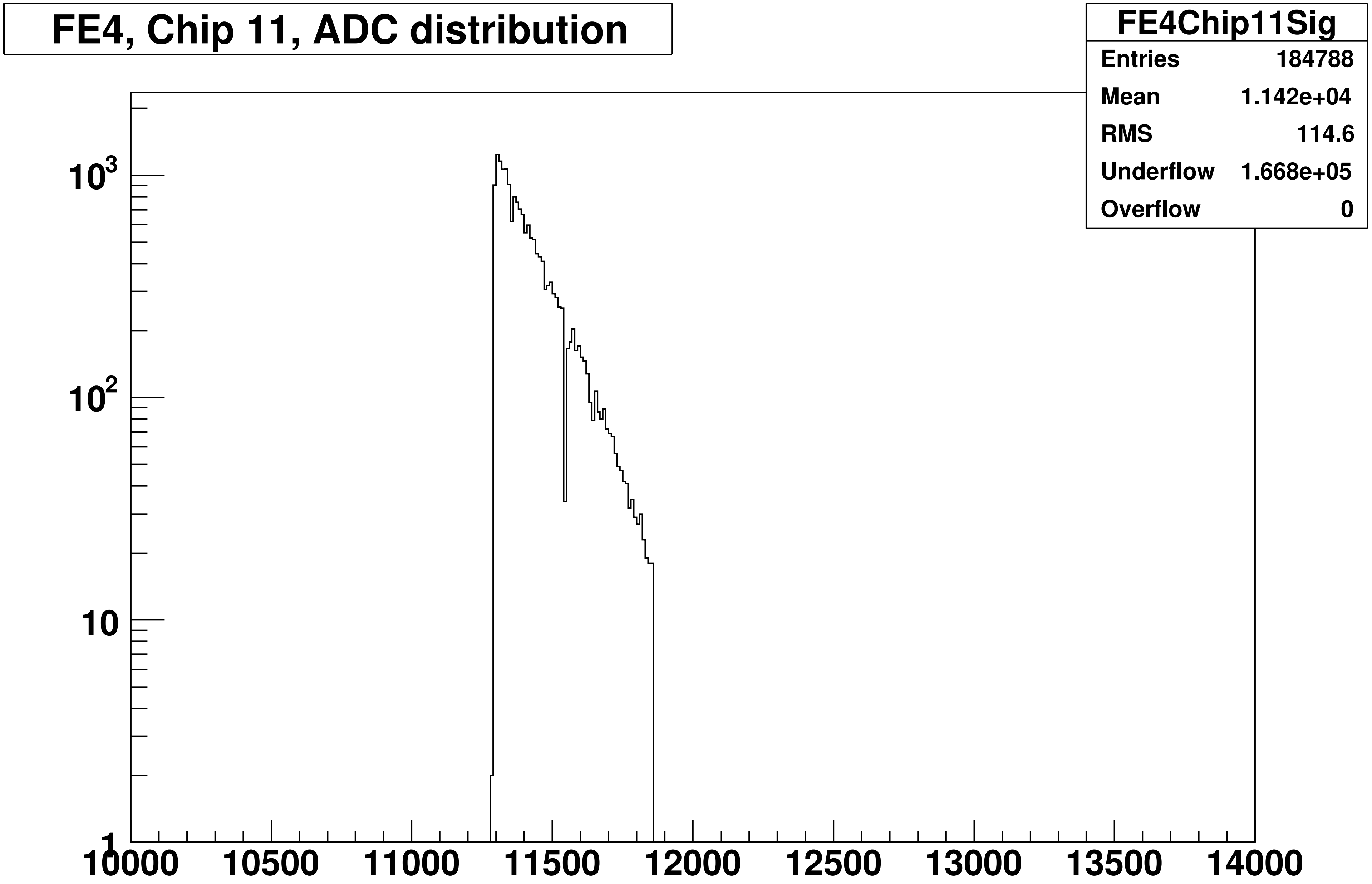
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200


FE4, Chip 11, ADC distribution
FE4Chip11Sig
Entries 184788
Mean 1.142e+04
RMS 114.6
Underflow 1.668e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
12500
13000
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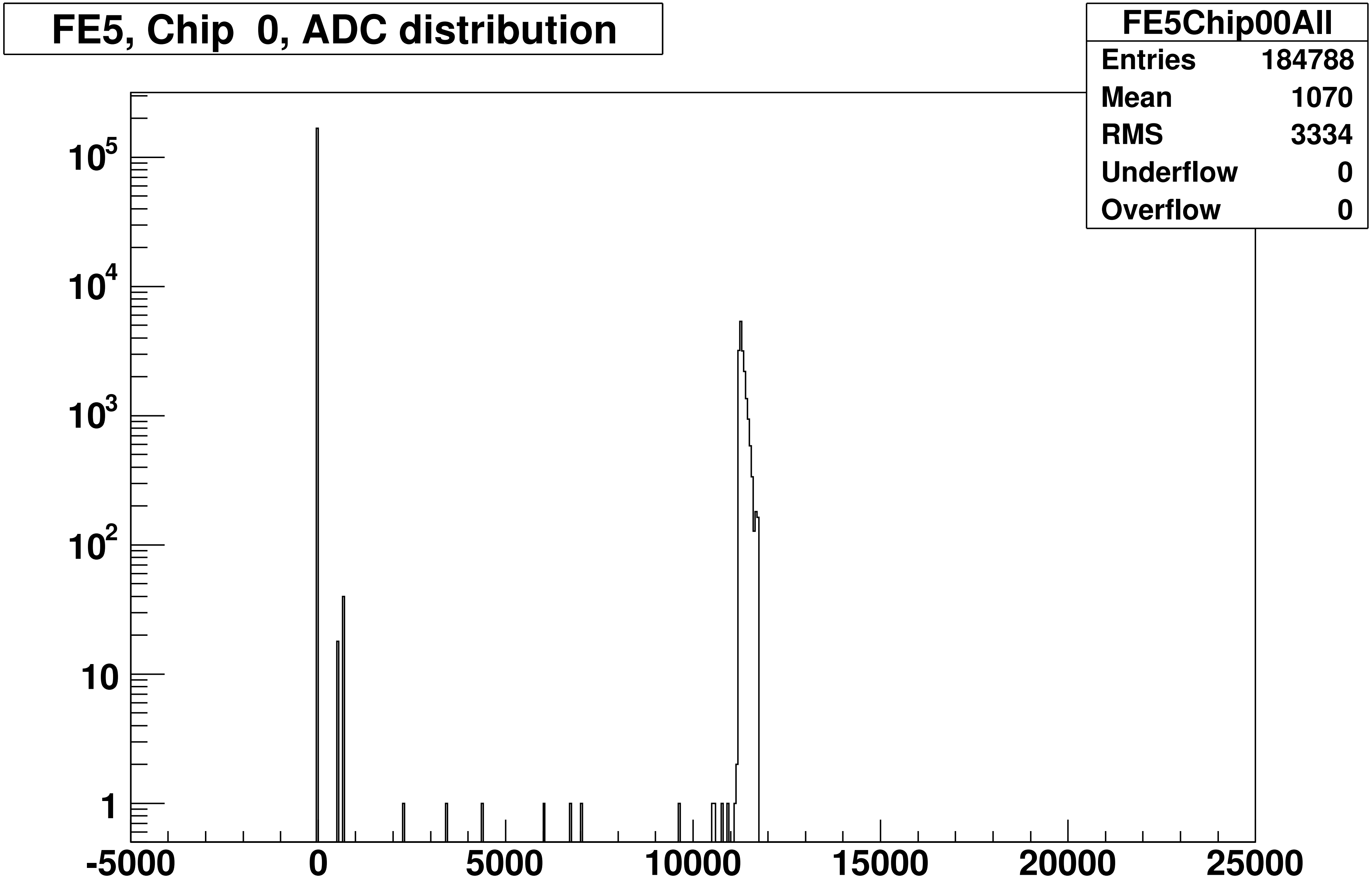
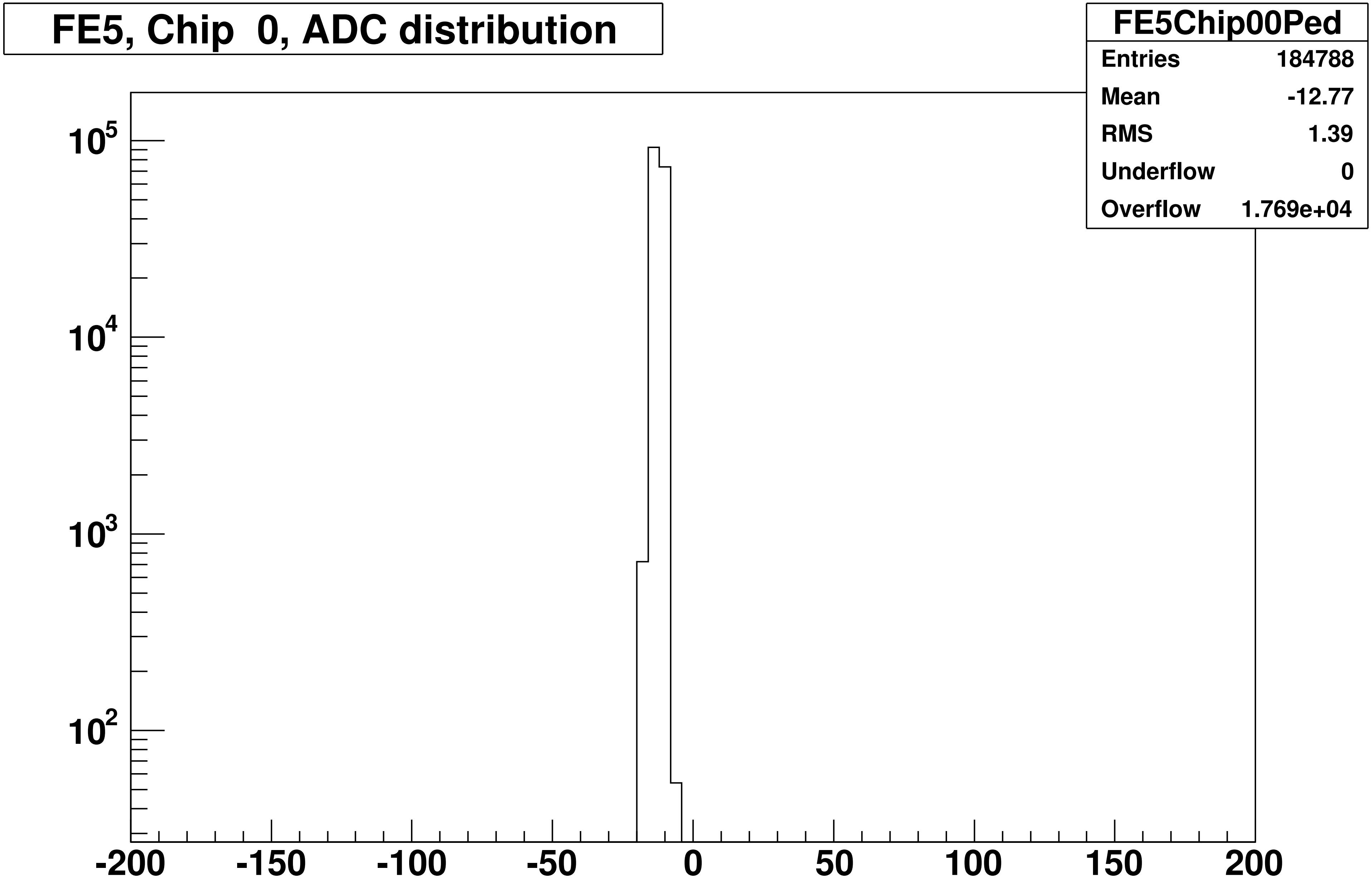

FE5, Chip 0, ADC distribution
FE5Chip00All
Entries 184788
Mean 1070
RMS 3334
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 0, ADC distribution
FE5Chip00Ped
Entries 184788
Mean -12.77
RMS 1.39
Underflow 0
Overflow 1.769e+04
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10^4
10^3
10^2
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-100
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150
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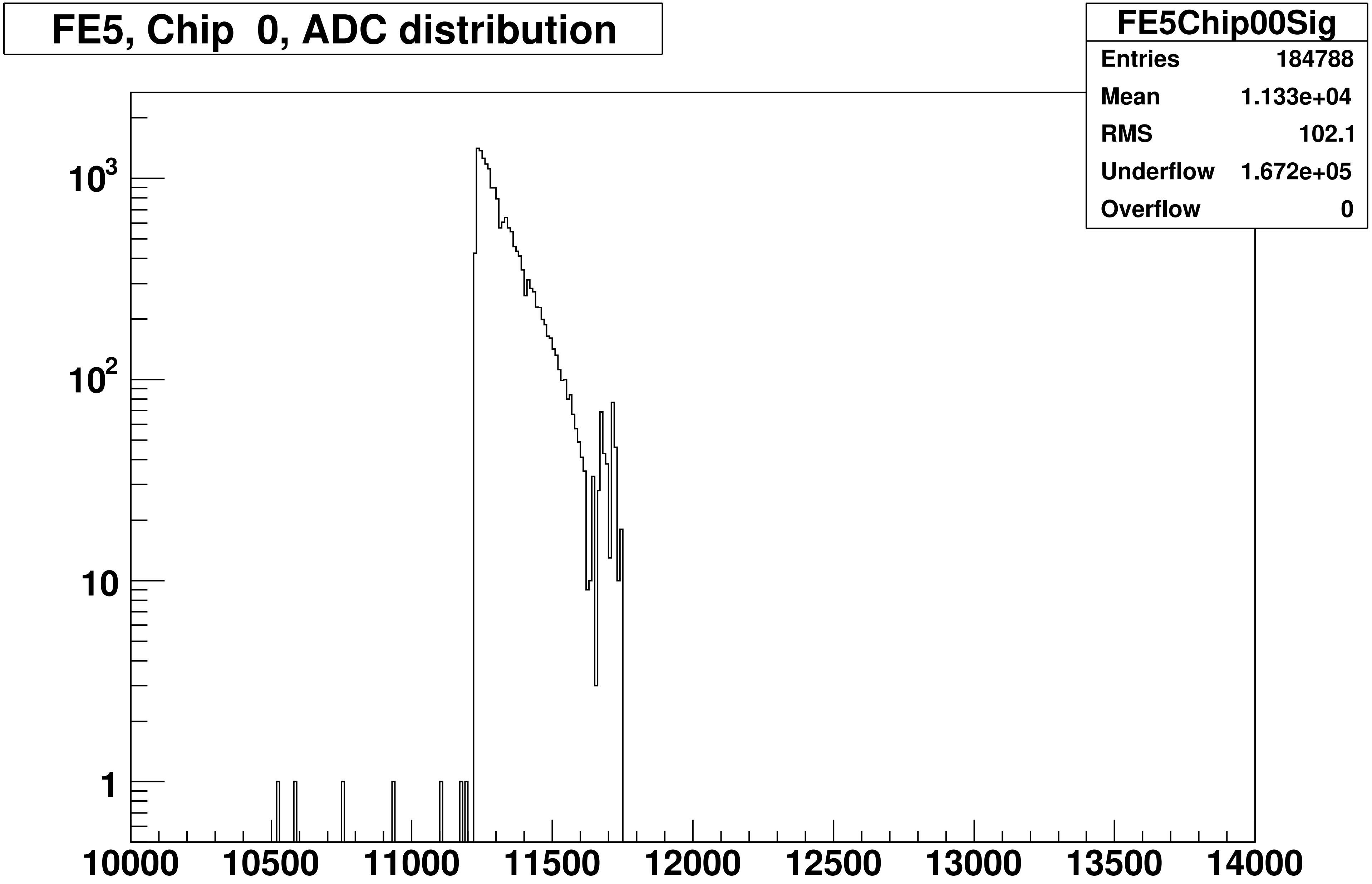
FE5, Chip 0, ADC distribution
FE5Chip00Sig
Entries 184788
Mean 1.133e+04
RMS 102.1
Underflow 1.672e+05
Overflow 0
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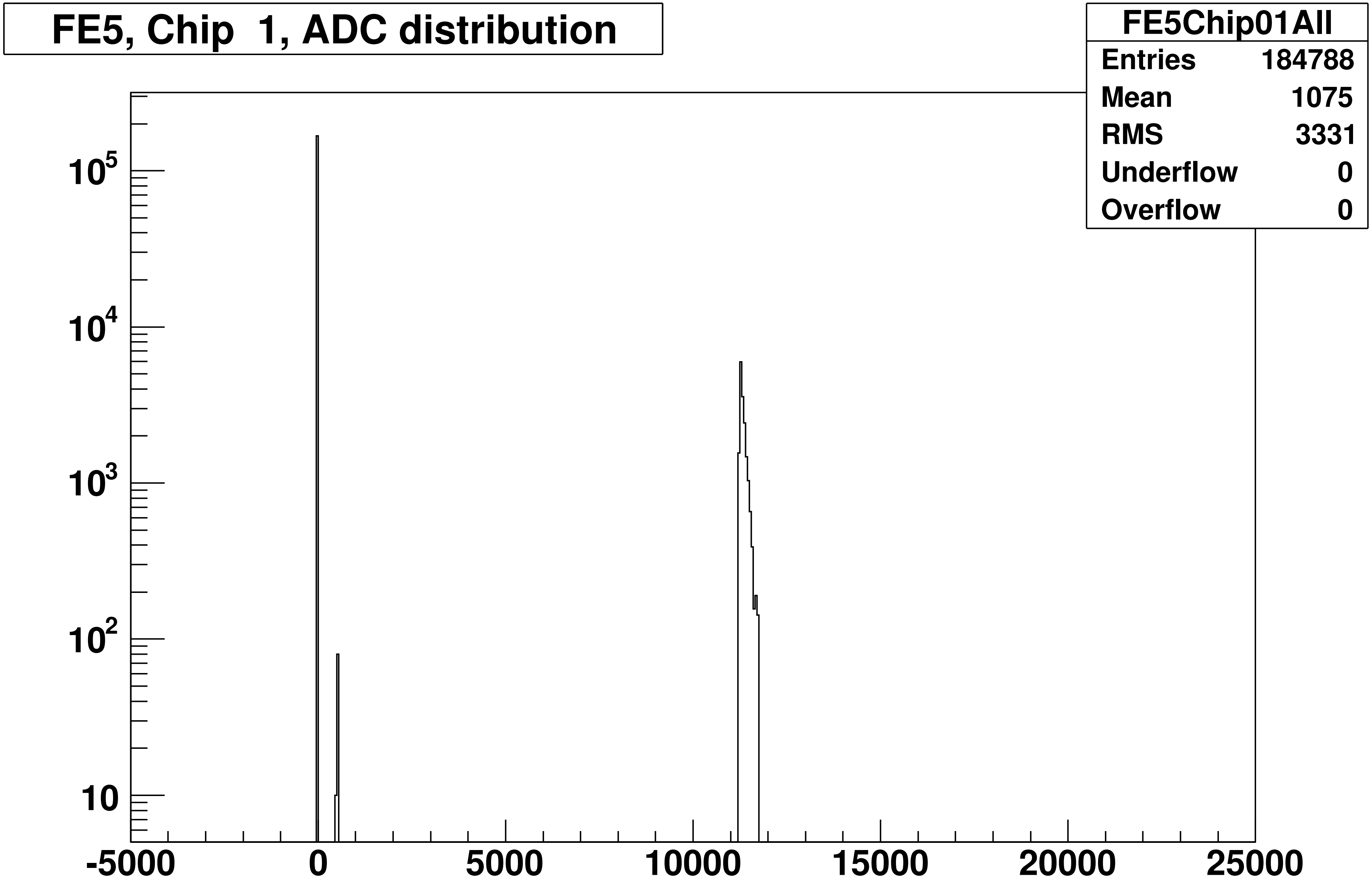
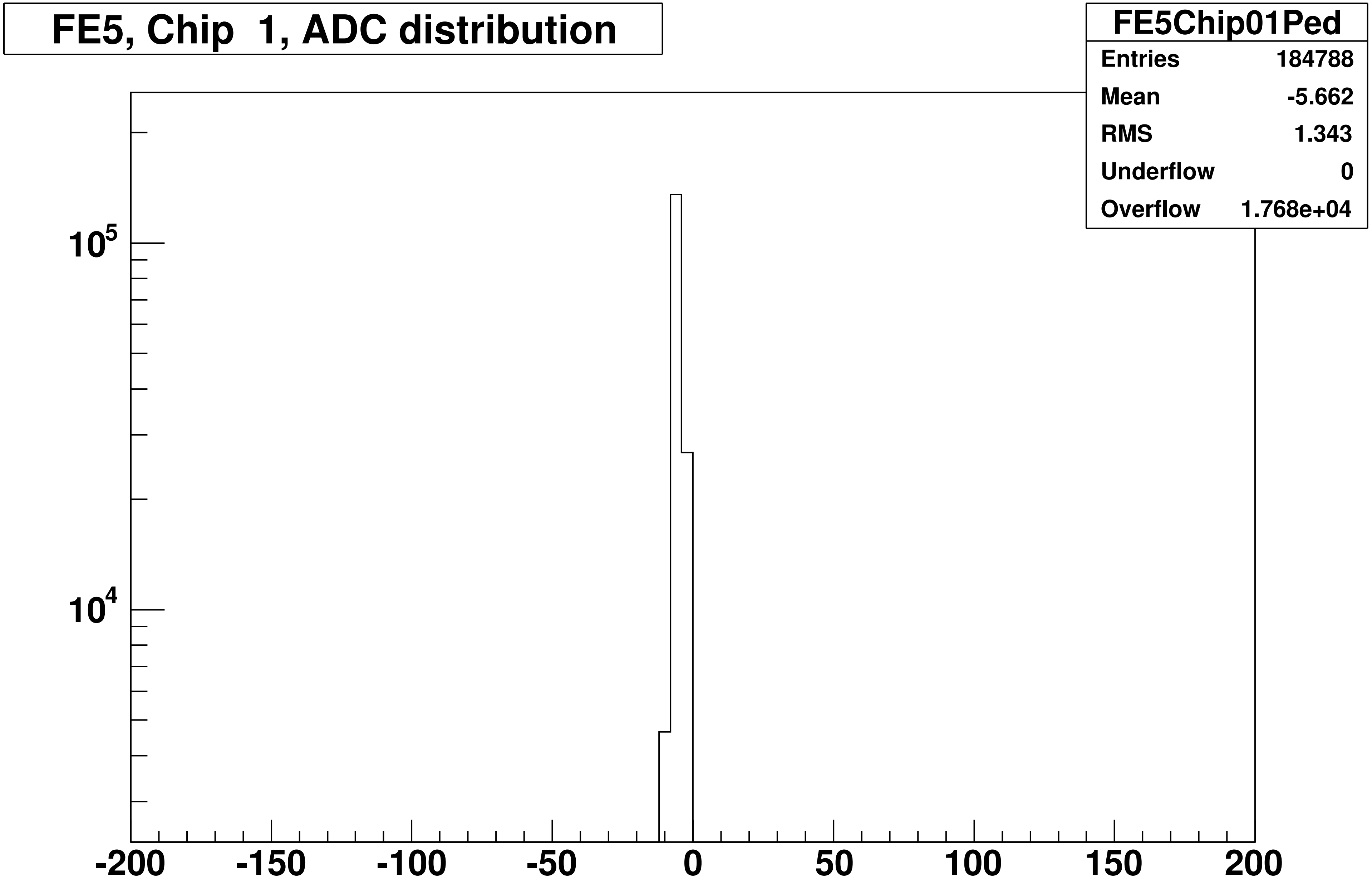
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 1, ADC distribution
FE5Chip01All
Entries 184788
Mean 1075
RMS 3331
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000



FE5, Chip 1, ADC distribution
FE5Chip01Ped
Entries 184788
Mean -5.662
RMS 1.343
Underflow 0
Overflow 1.768e+04
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10^4
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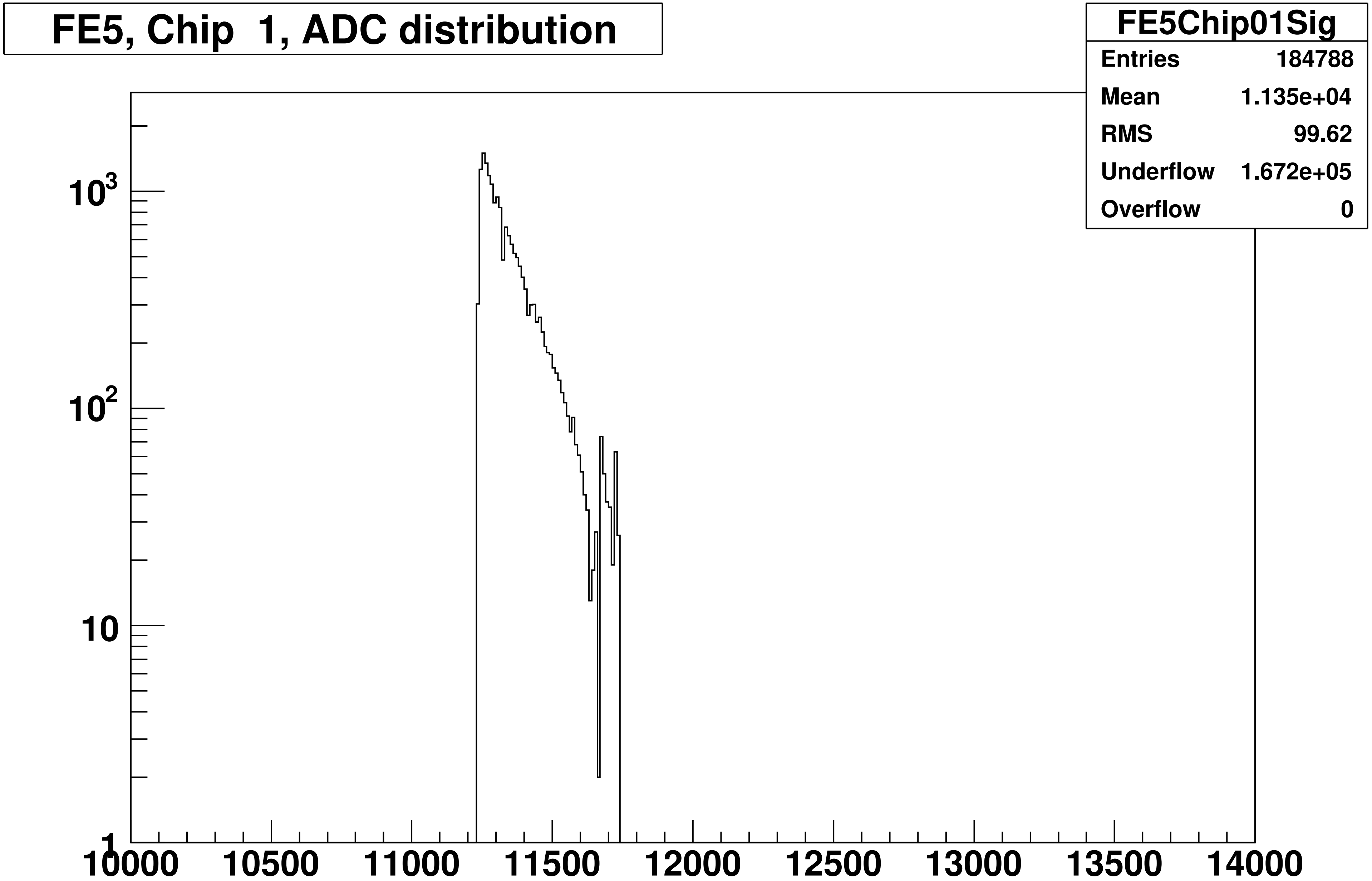
-100
-50
0
50
100
150
200



FE5, Chip 1, ADC distribution
FE5Chip01Sig
Entries 184788
Mean 1.135e+04
RMS 99.62
Underflow 1.672e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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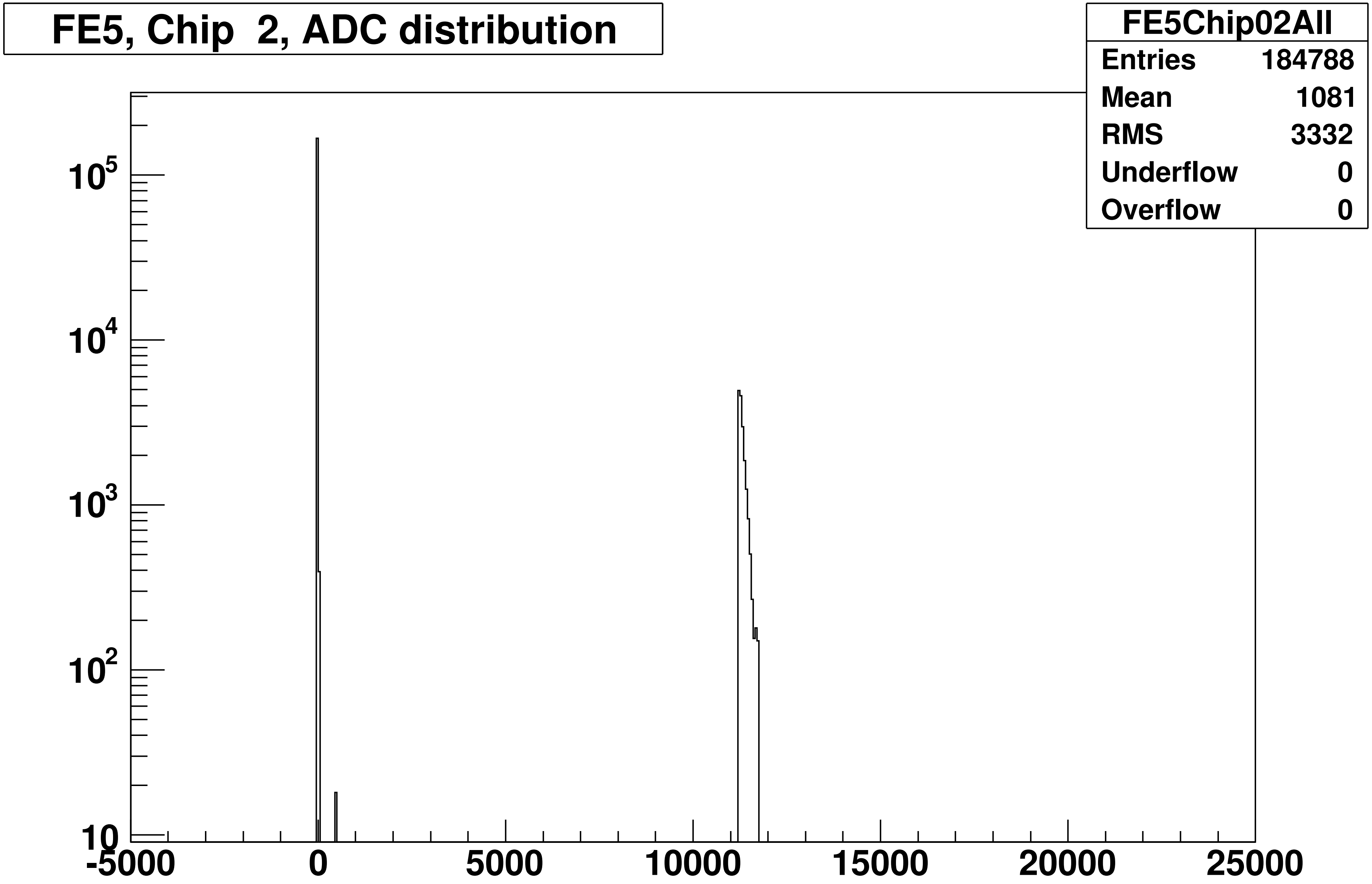
FE5, Chip 2, ADC distribution
FE5Chip02All
Entries 184788
Mean 1081
RMS 3332
Underflow 0
Overflow 0
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10^4
10^3
10^2
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-5000
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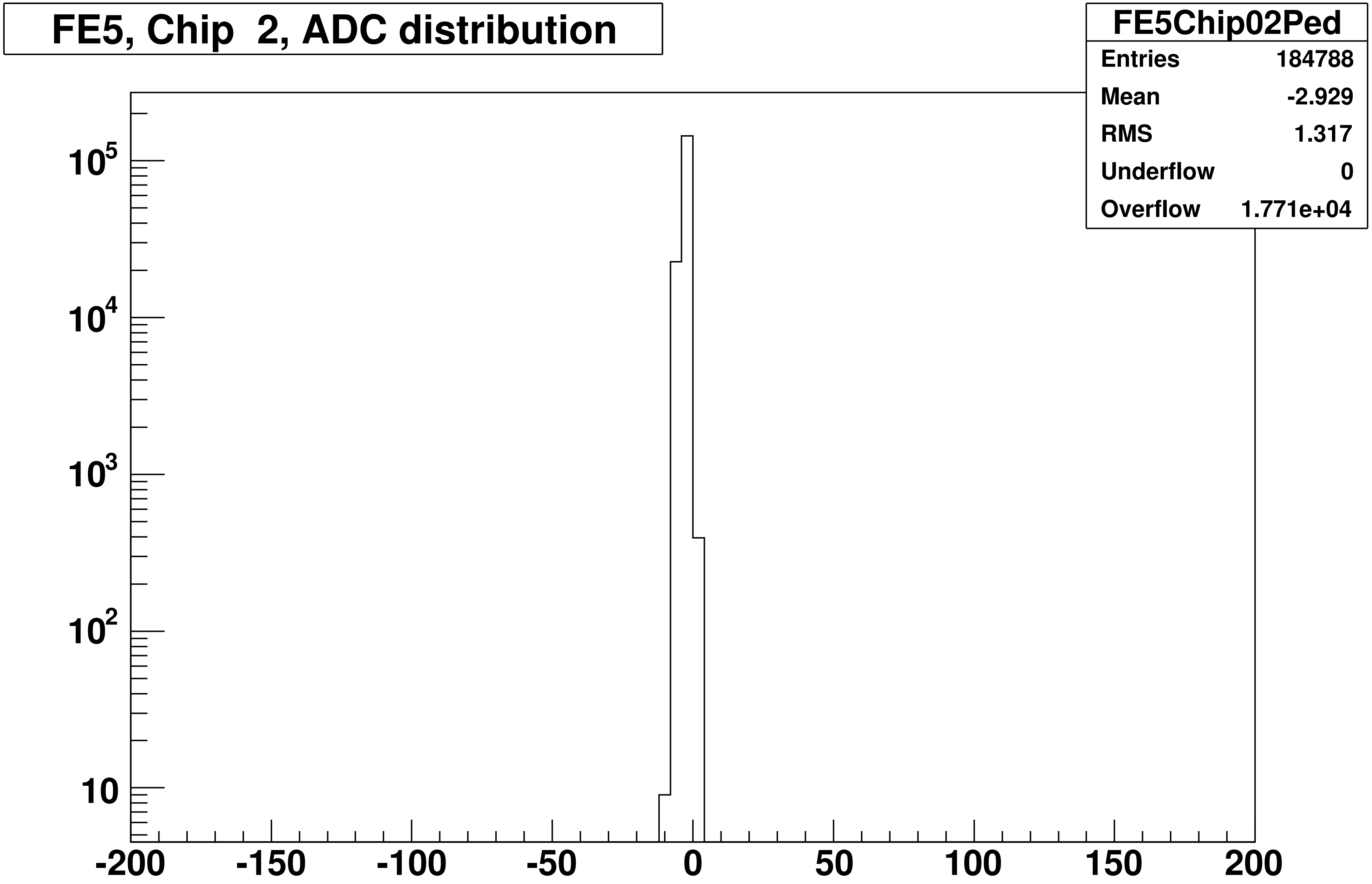
20000
25000



FE5, Chip 2, ADC distribution
FE5Chip02Ped
Entries 184788
Mean -2.929
RMS 1.317
Underflow 0
Overflow 1.771e+04
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10^4
10^3
10^2
10
-200
-150
-100
-50
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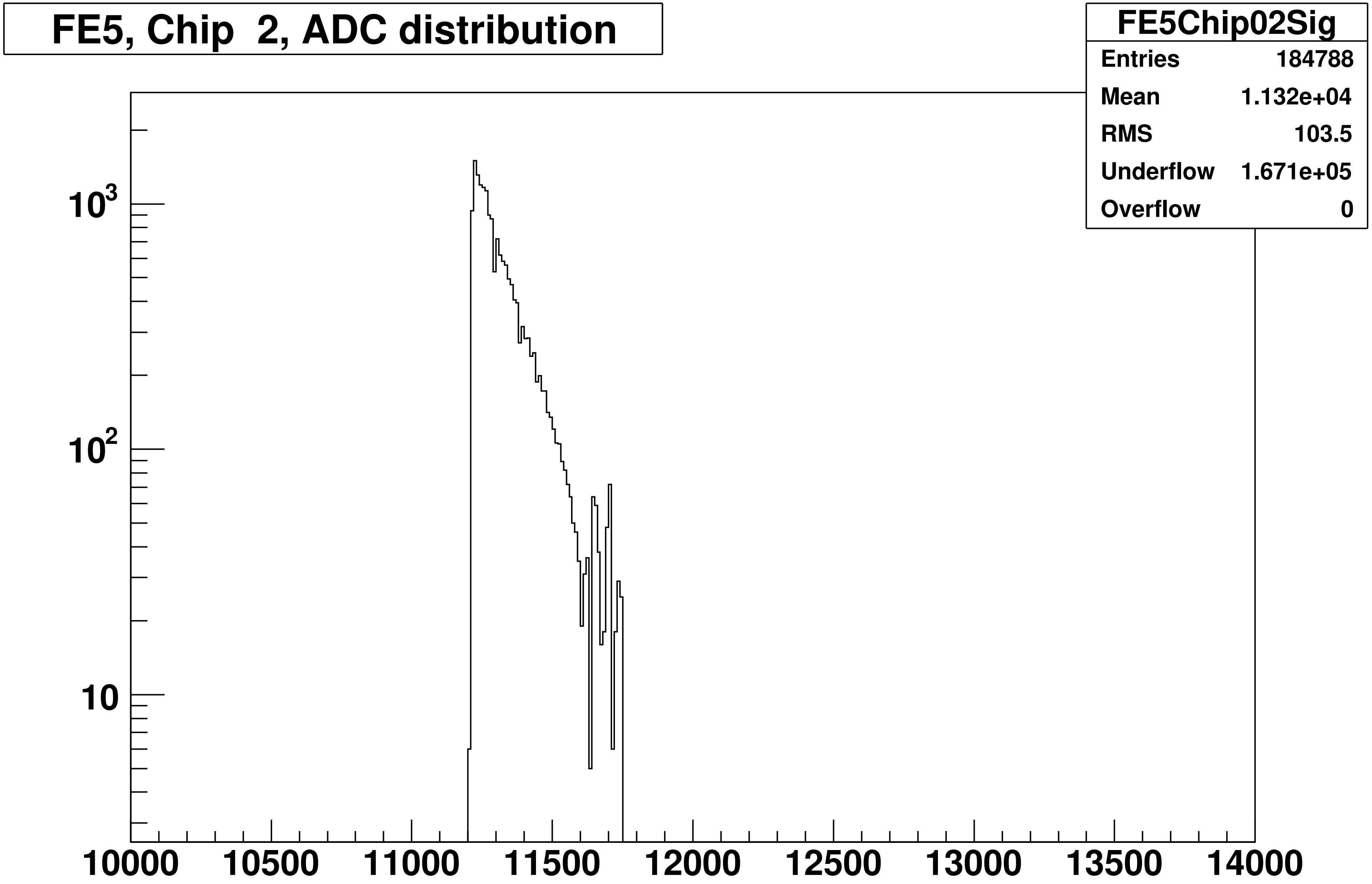
100
150
200


FE5, Chip 2, ADC distribution
FE5Chip02Sig
Entries 184788
Mean 1.132e+04
RMS 103.5
Underflow 1.671e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
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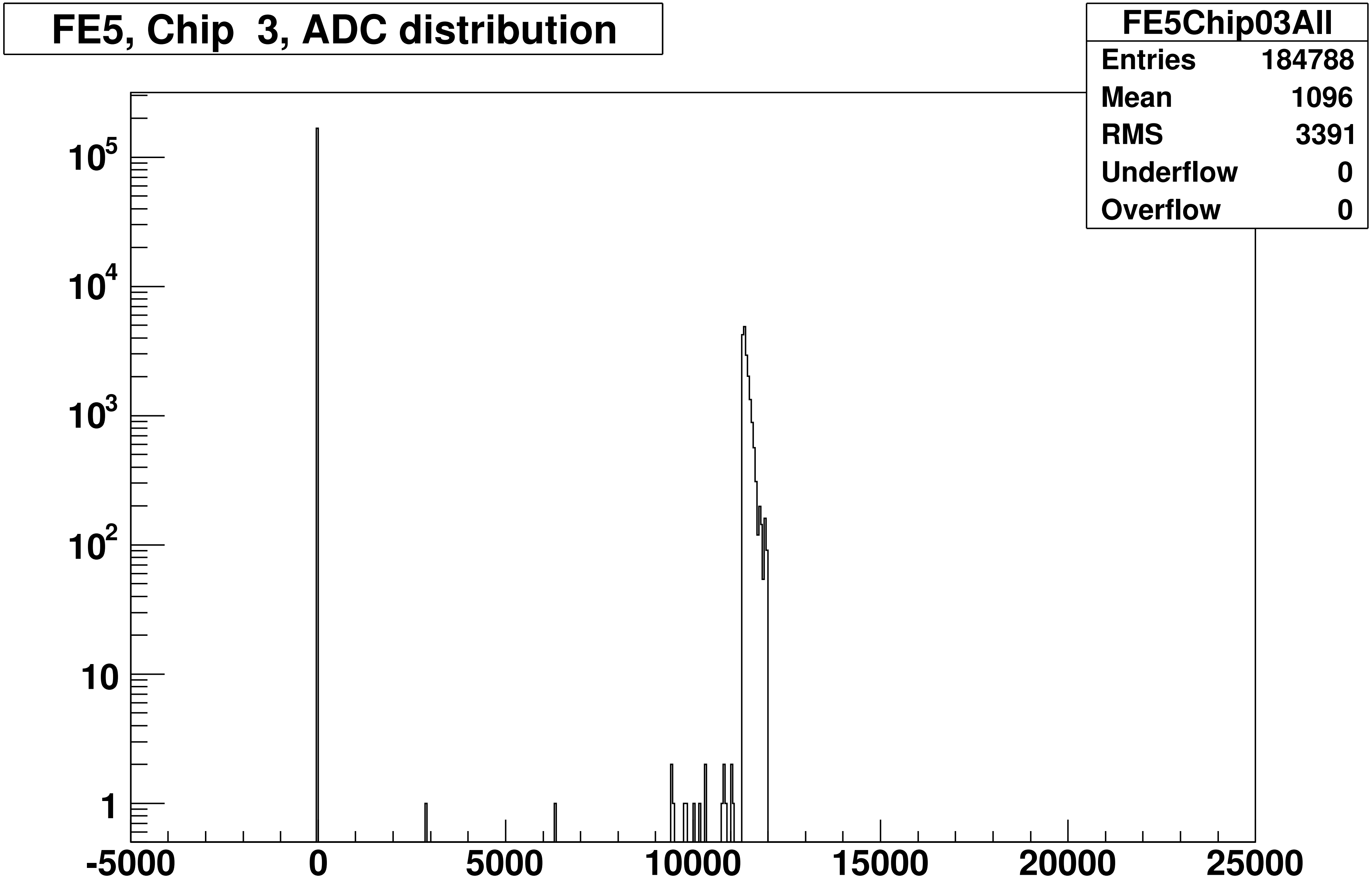
14000



FE5, Chip 3, ADC distribution
FE5Chip03All
Entries 184788
Mean 1096
RMS 3391
Underflow 0
Overflow 0
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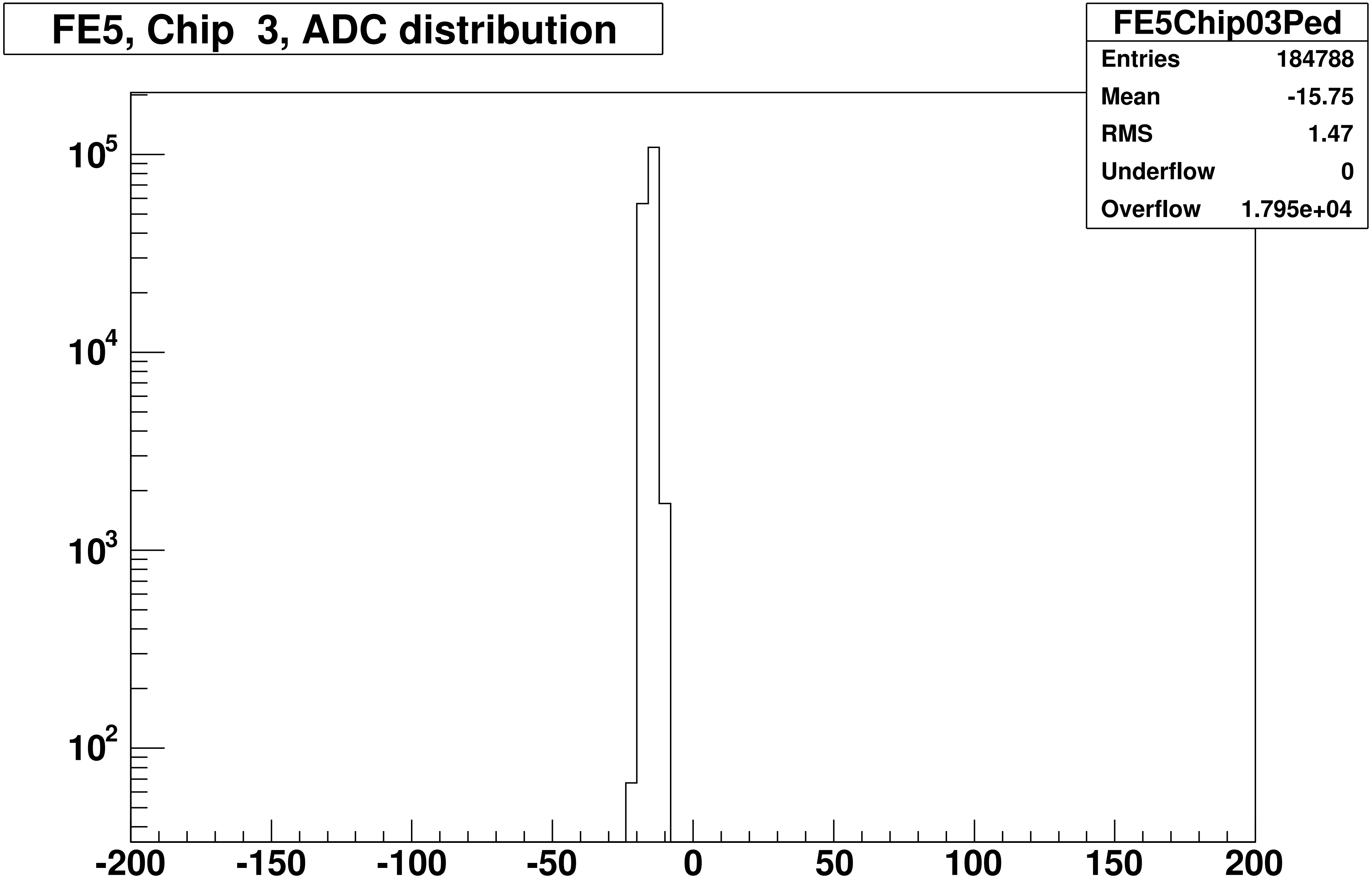
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE5, Chip 3, ADC distribution
FE5Chip03Ped
Entries 184788
Mean -15.75
RMS 1.47
Underflow 0
Overflow 1.795e+04
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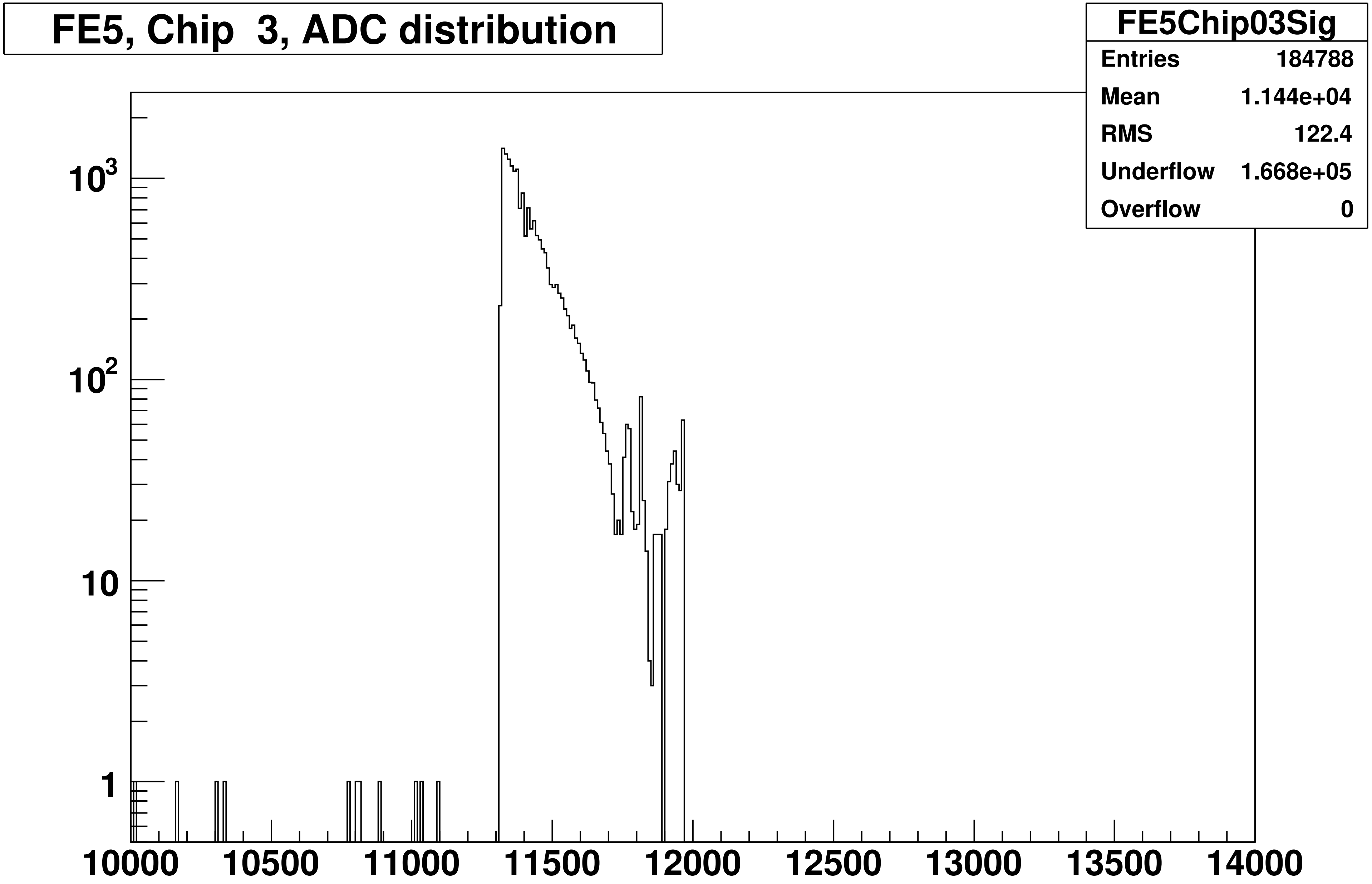
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200


FE5, Chip 3, ADC distribution
FE5Chip03Sig
Entries 184788
Mean 1.144e+04
RMS 122.4
Underflow 1.668e+05
Overflow 0
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10^2
10
1
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11500
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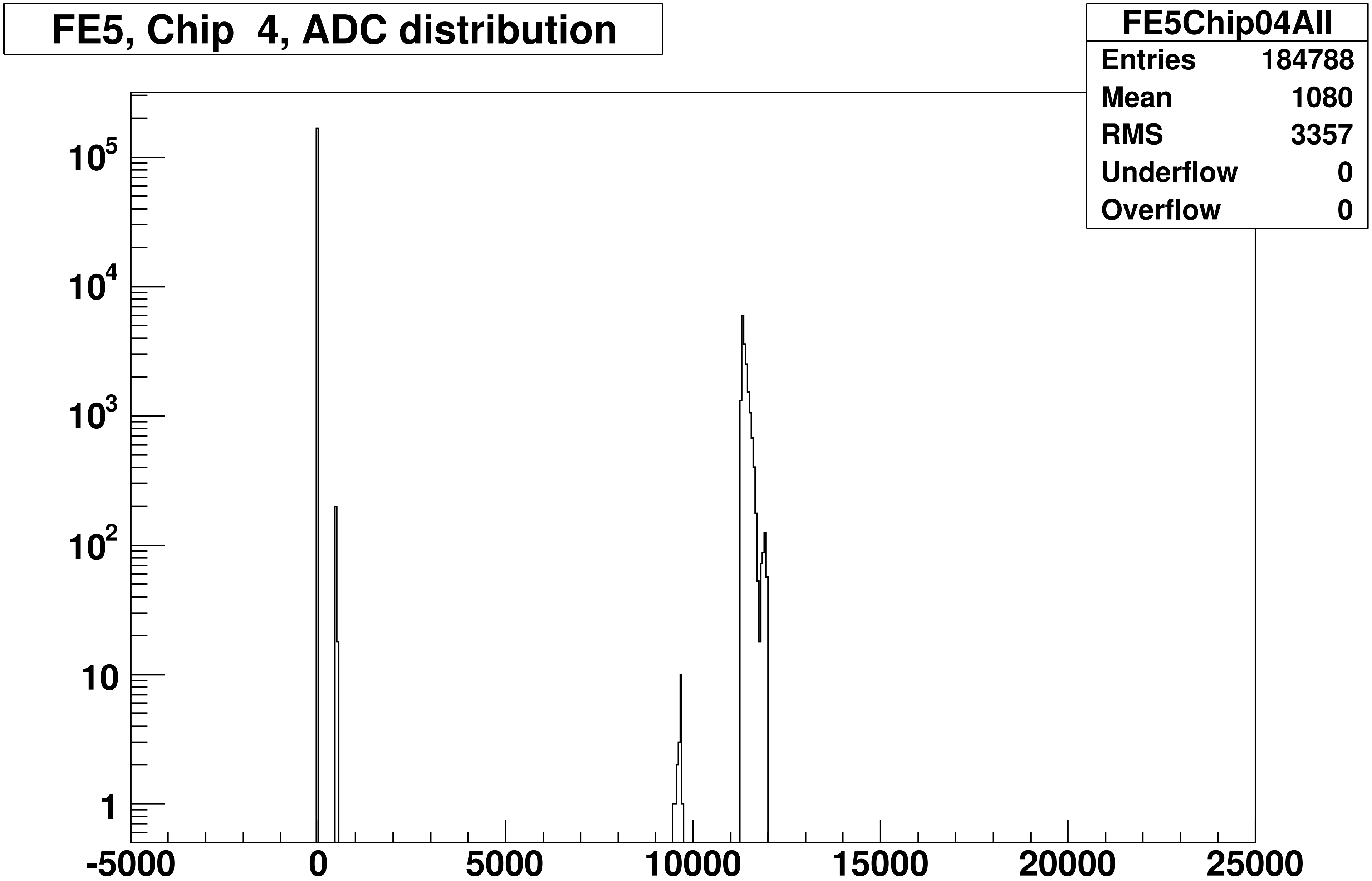

FE5, Chip 4, ADC distribution
FE5Chip04All
Entries 184788
Mean 1080
RMS 3357
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
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-5000
0
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20000
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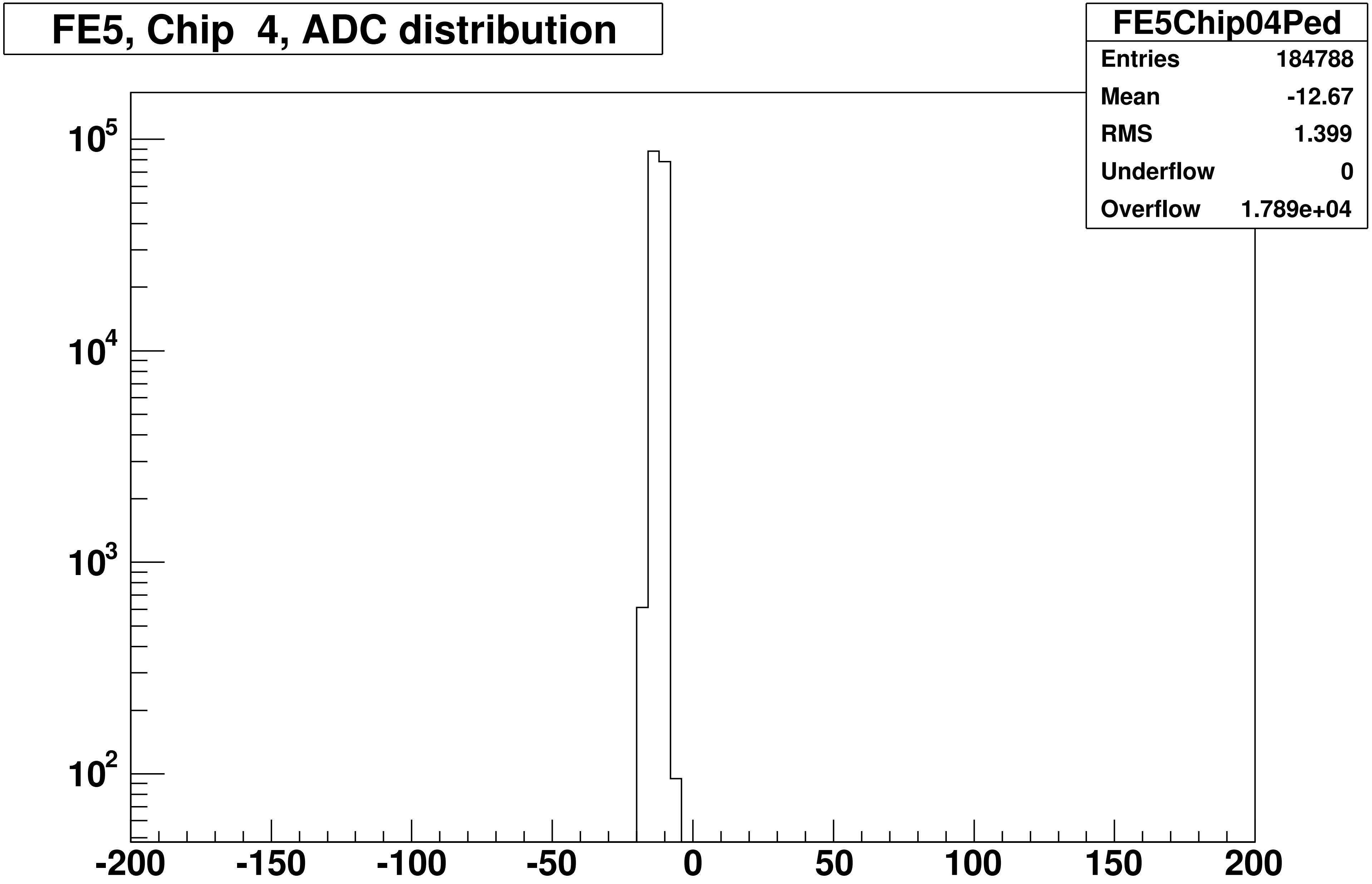
FE5, Chip 4, ADC distribution
FE5Chip04Ped
Entries 184788
Mean -12.67
RMS 1.399
Underflow 0
Overflow 1.789e+04
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10^4
10^3
10^2
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-100
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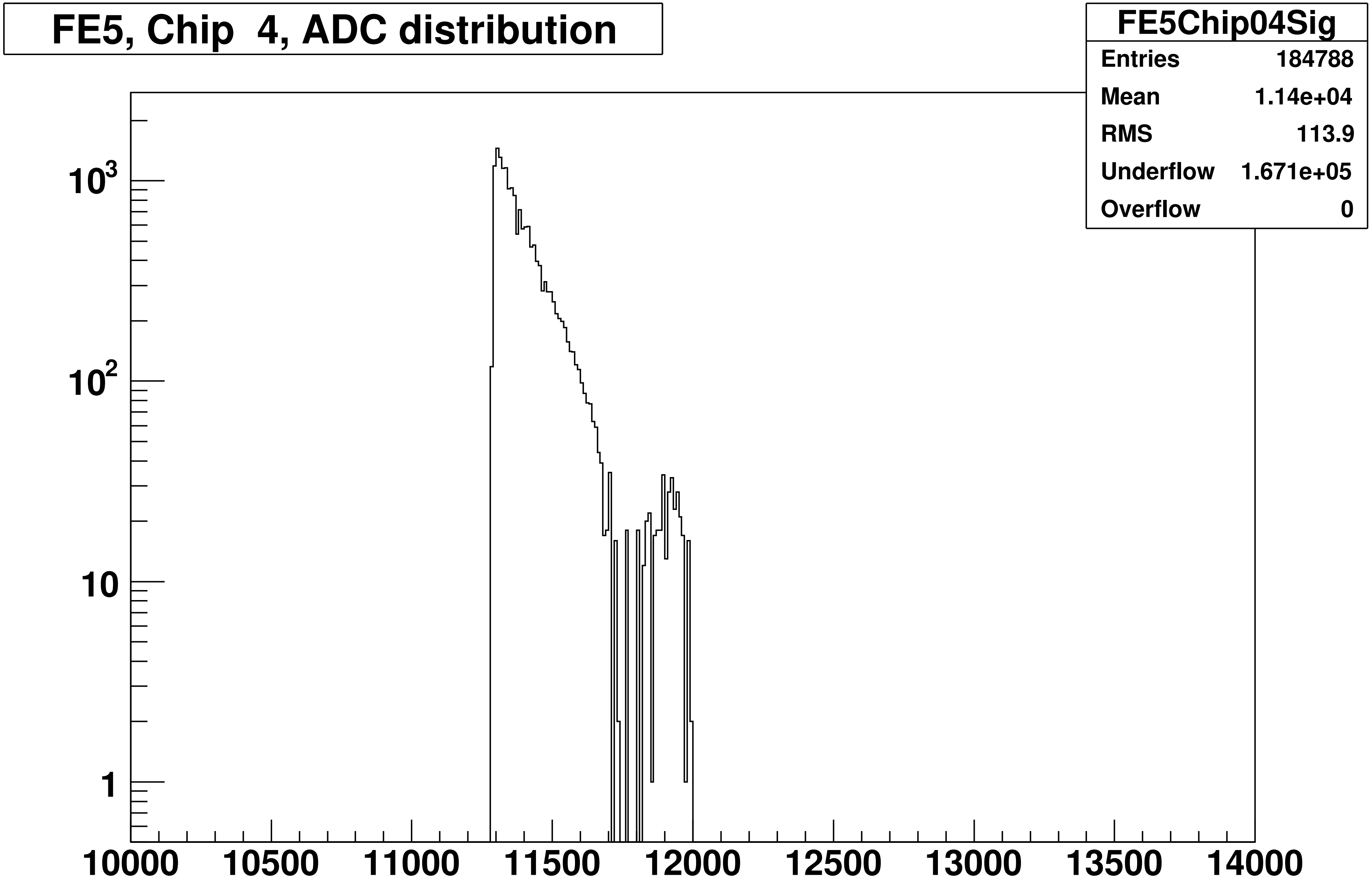
200


FE5, Chip 4, ADC distribution
FE5Chip04Sig
Entries 184788
Mean 1.14e+04
RMS 113.9
Underflow 1.671e+05
Overflow 0
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10^2
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1
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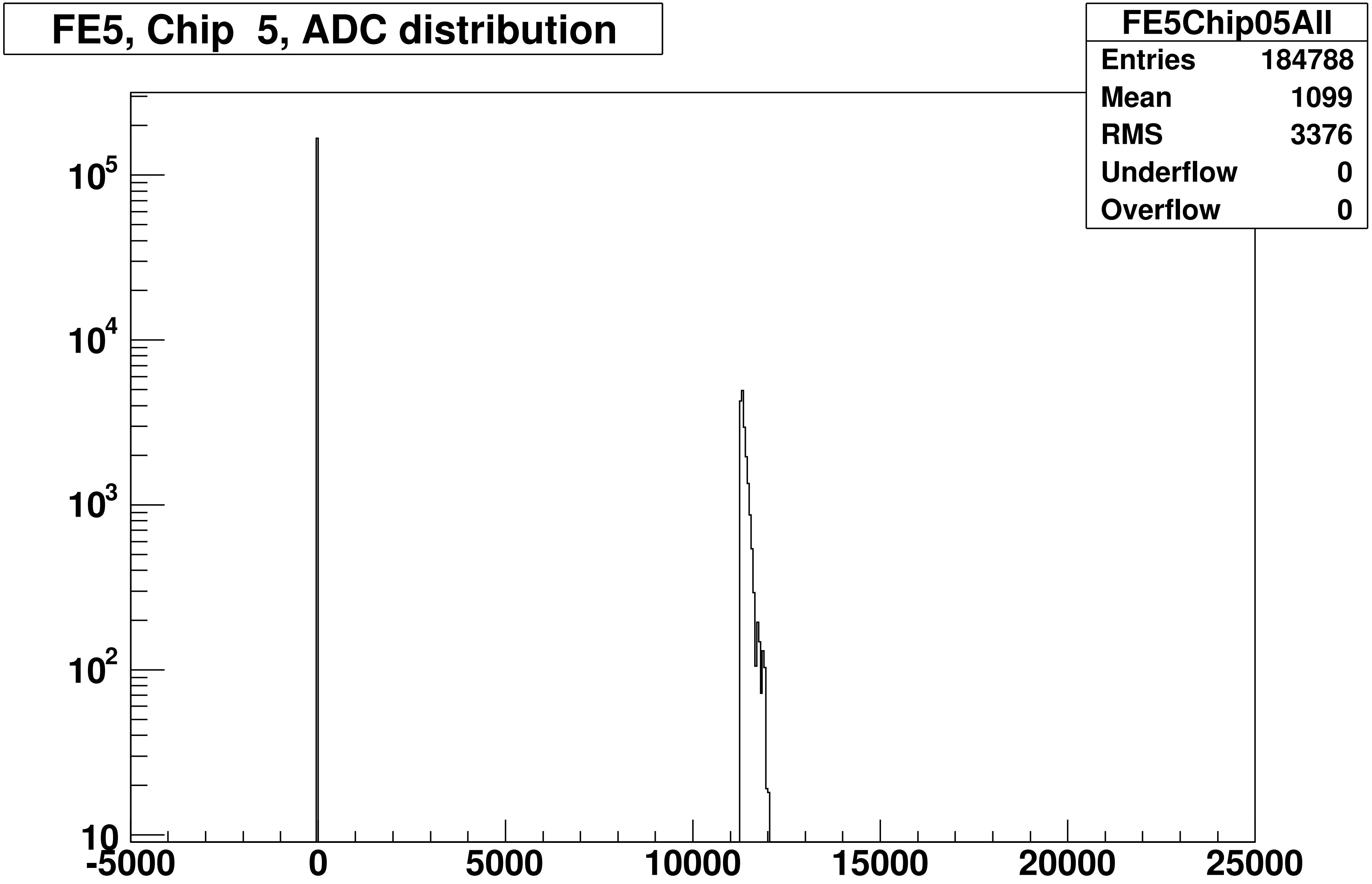
FE5, Chip 5, ADC distribution
FE5Chip05All
Entries 184788
Mean 1099
RMS 3376
Underflow 0
Overflow 0
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10^5
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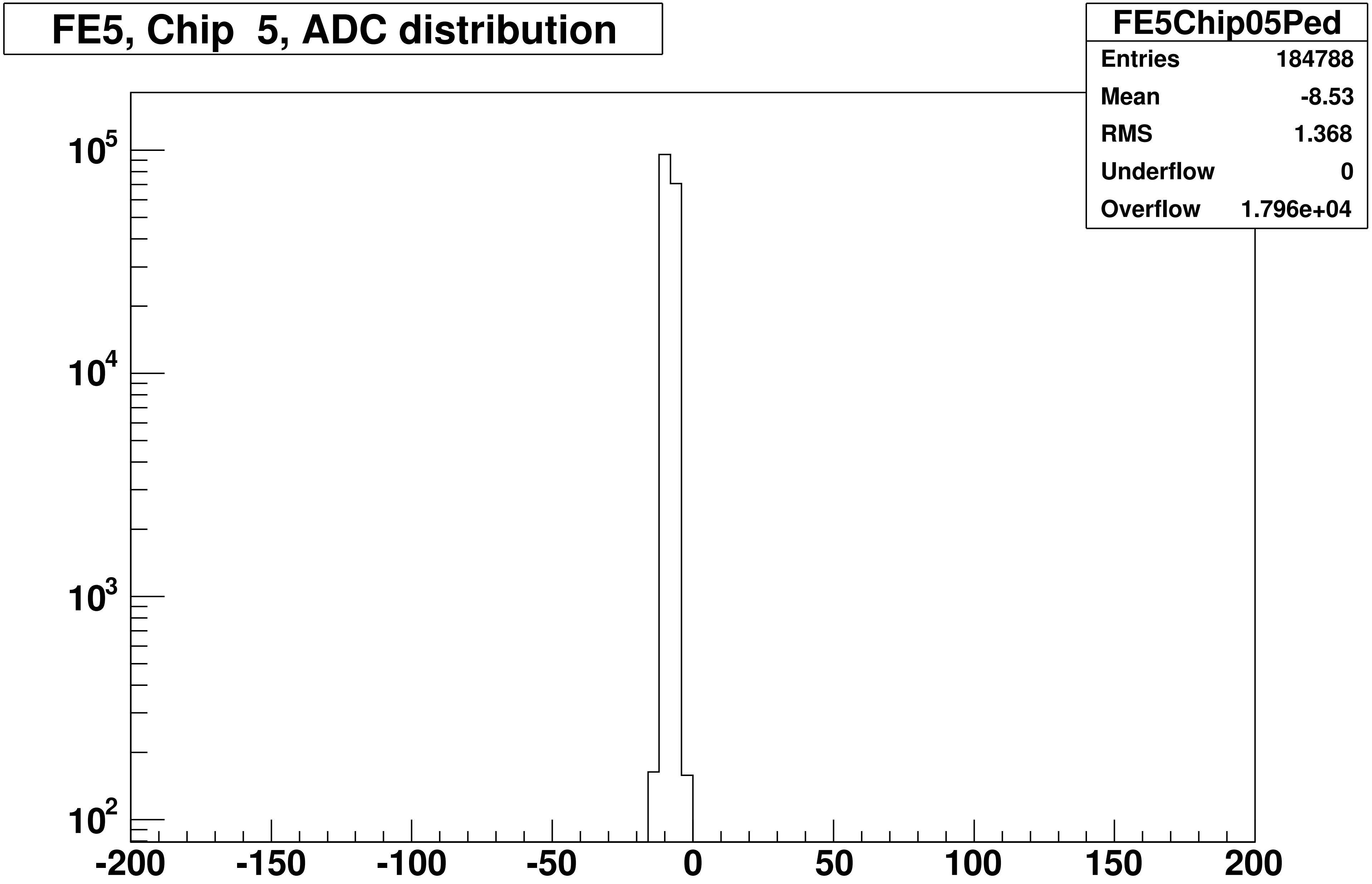
FE5, Chip 5, ADC distribution
FE5Chip05Ped
Entries 184788
Mean -8.53
RMS 1.368
Underflow 0
Overflow 1.796e+04
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10^4
10^3
10^2
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-100
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0
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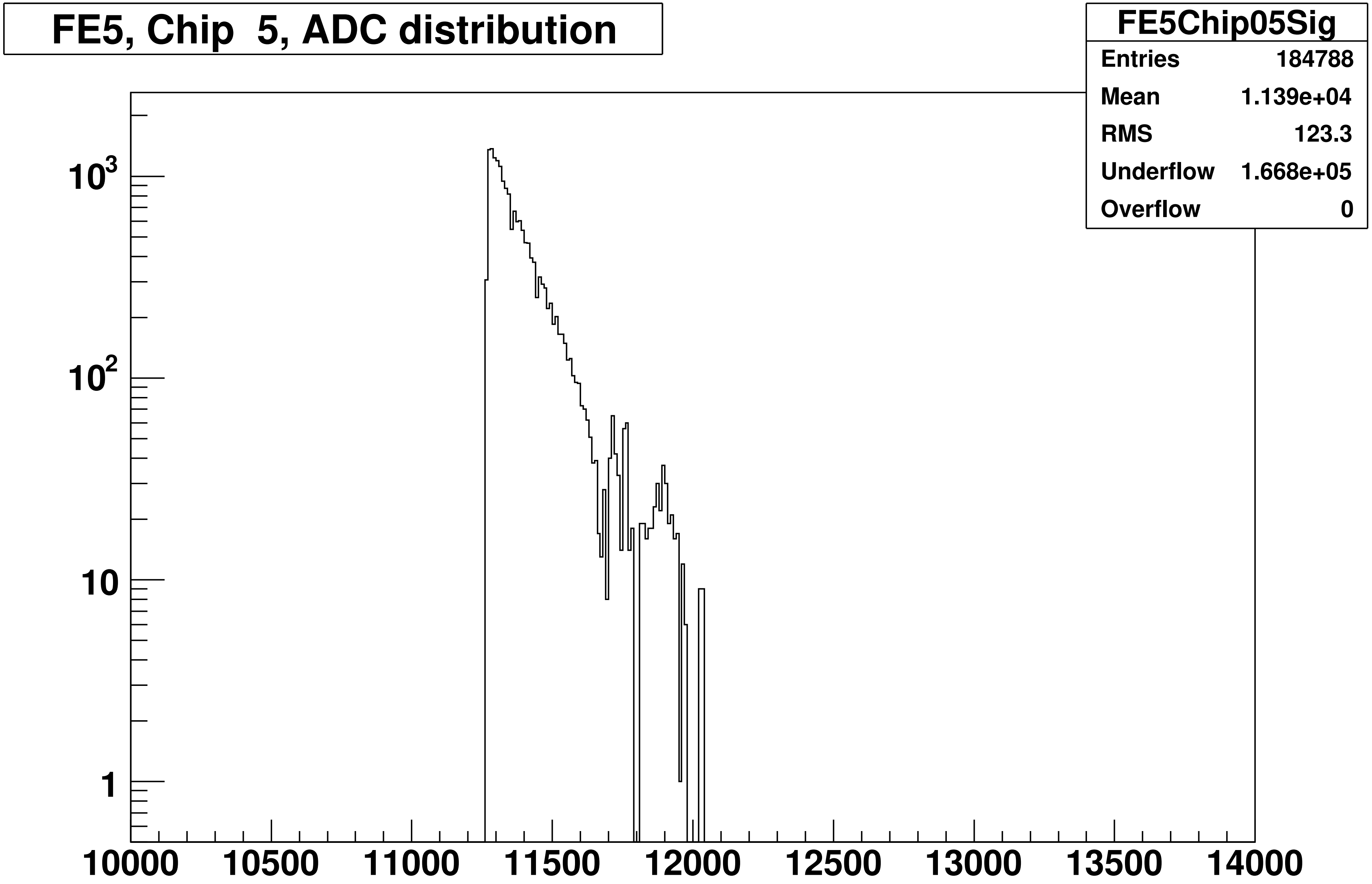
100
150
200


FE5, Chip 5, ADC distribution
FE5Chip05Sig
Entries 184788
Mean 1.139e+04
RMS 123.3
Underflow 1.668e+05
Overflow 0
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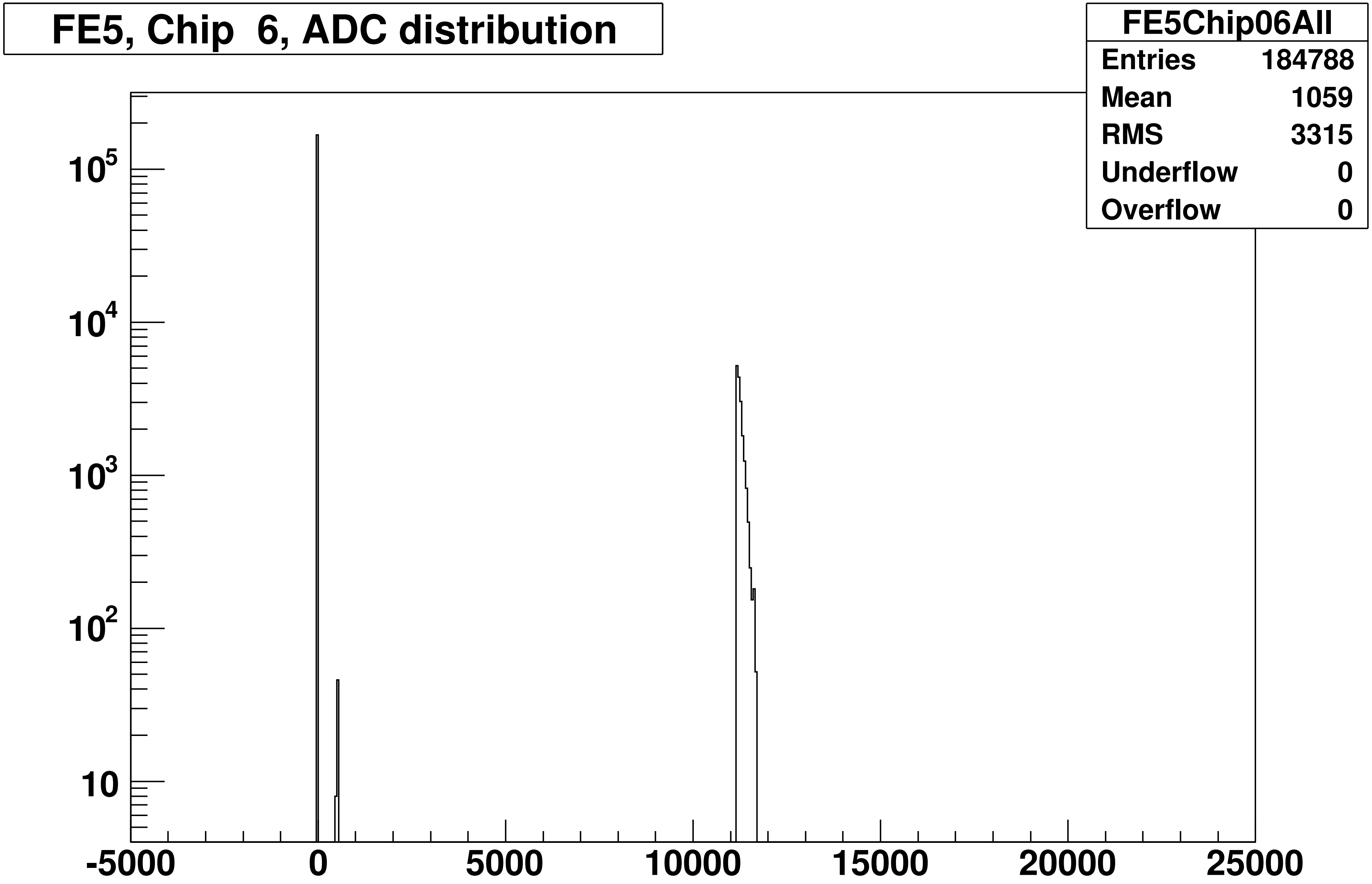
FE5, Chip 6, ADC distribution
FE5Chip06All
Entries 184788
Mean 1059
RMS 3315
Underflow 0
Overflow 0
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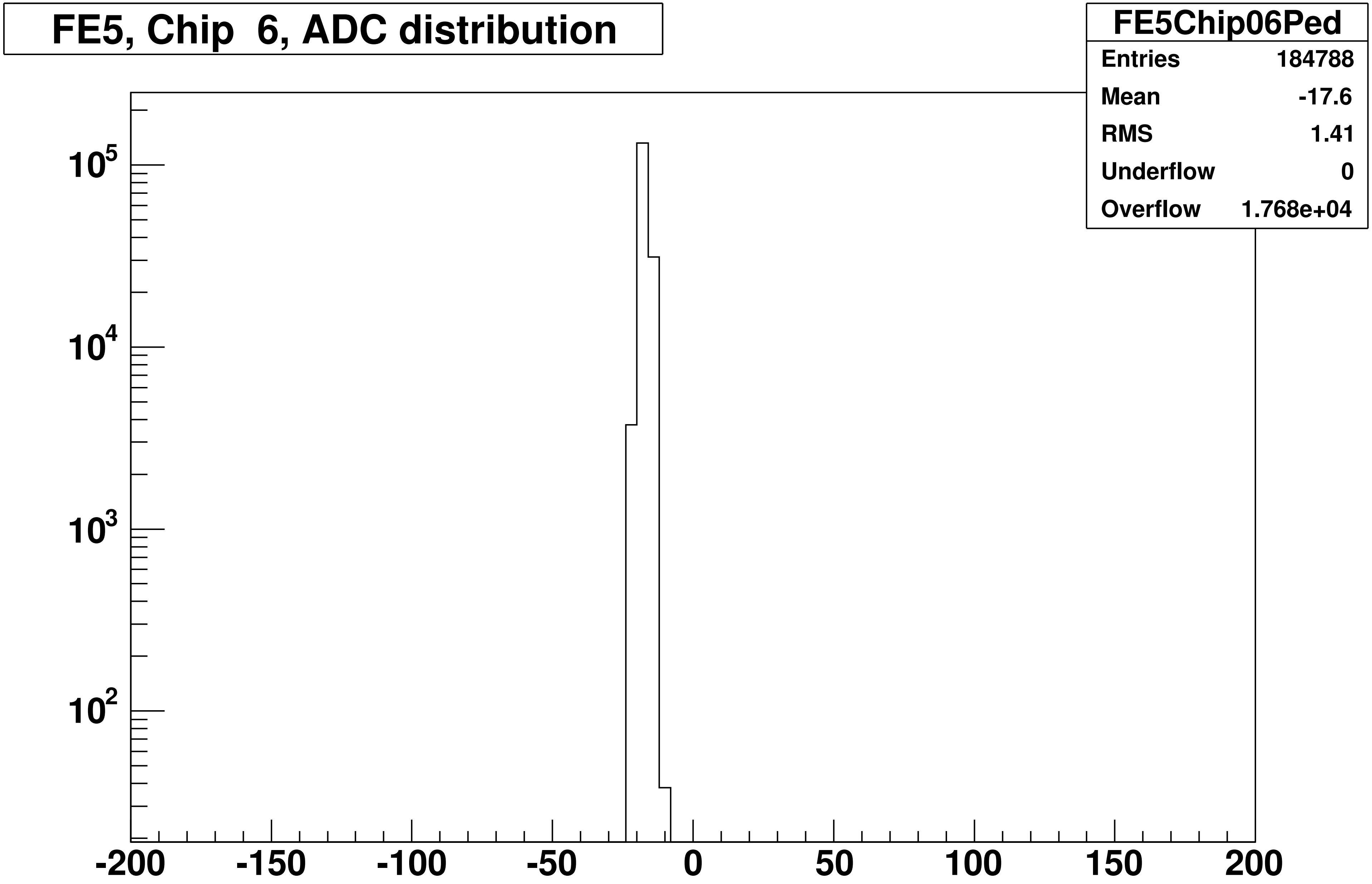
FE5, Chip 6, ADC distribution
FE5Chip06Ped
Entries 184788
Mean -17.6
RMS 1.41
Underflow 0
Overflow 1.768e+04
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10^4
10^3
10^2
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-100
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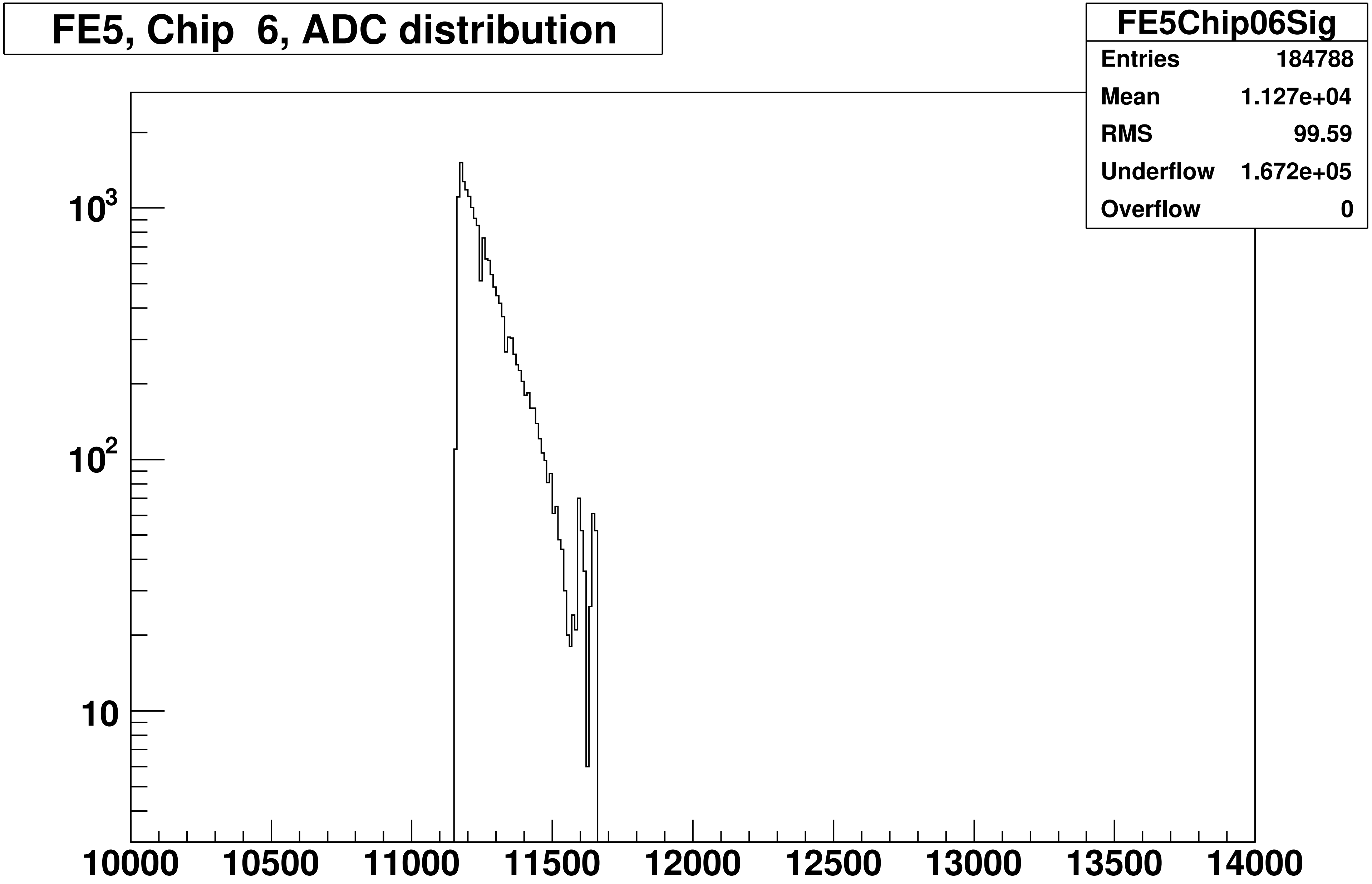
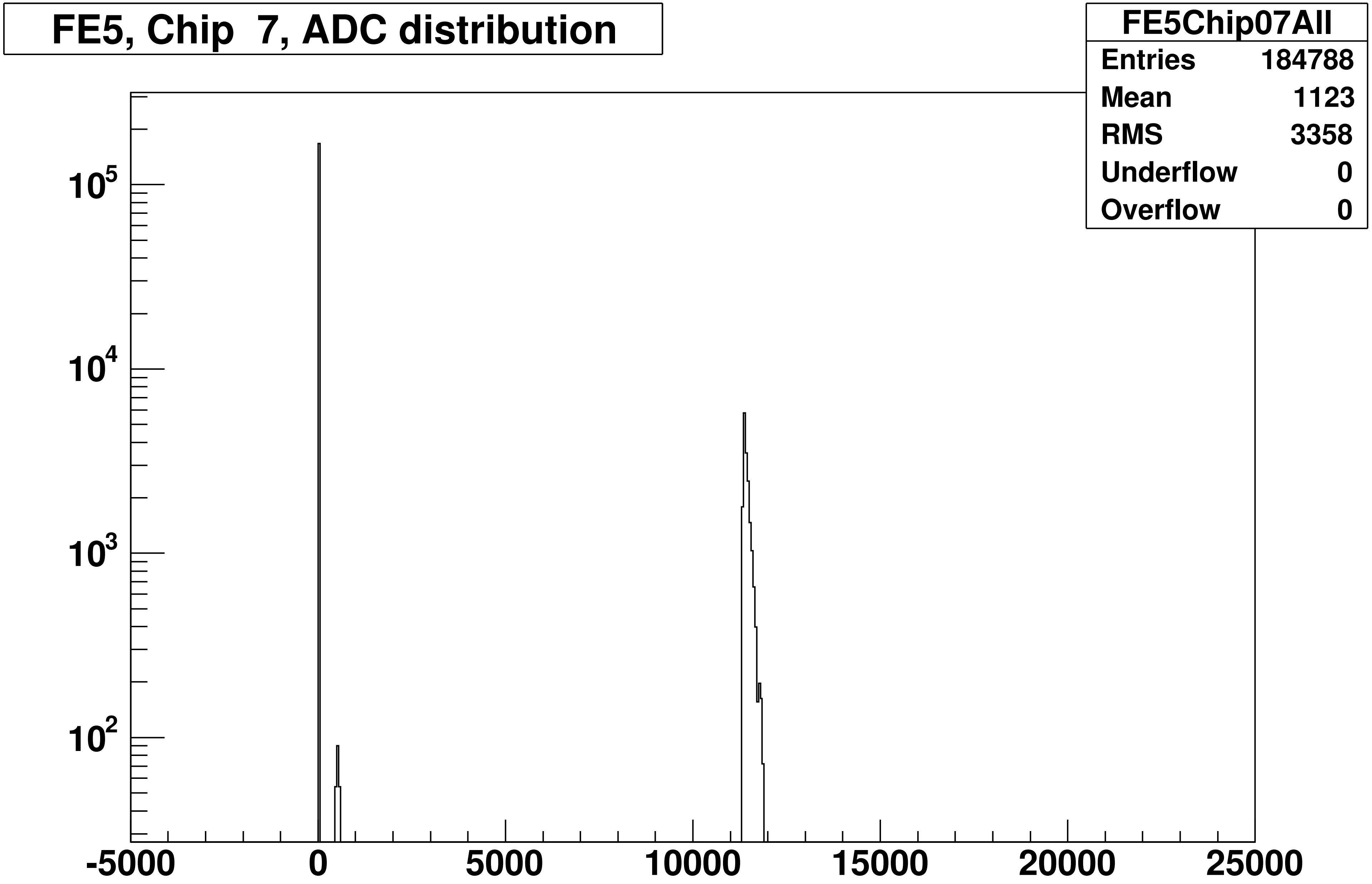
100
150
200


FE5, Chip 6, ADC distribution
FE5Chip06Sig
Entries 184788
Mean 1.127e+04
RMS 99.59
Underflow 1.672e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE5, Chip 7, ADC distribution
FE5Chip07All
Entries 184788
Mean 1123
RMS 3358
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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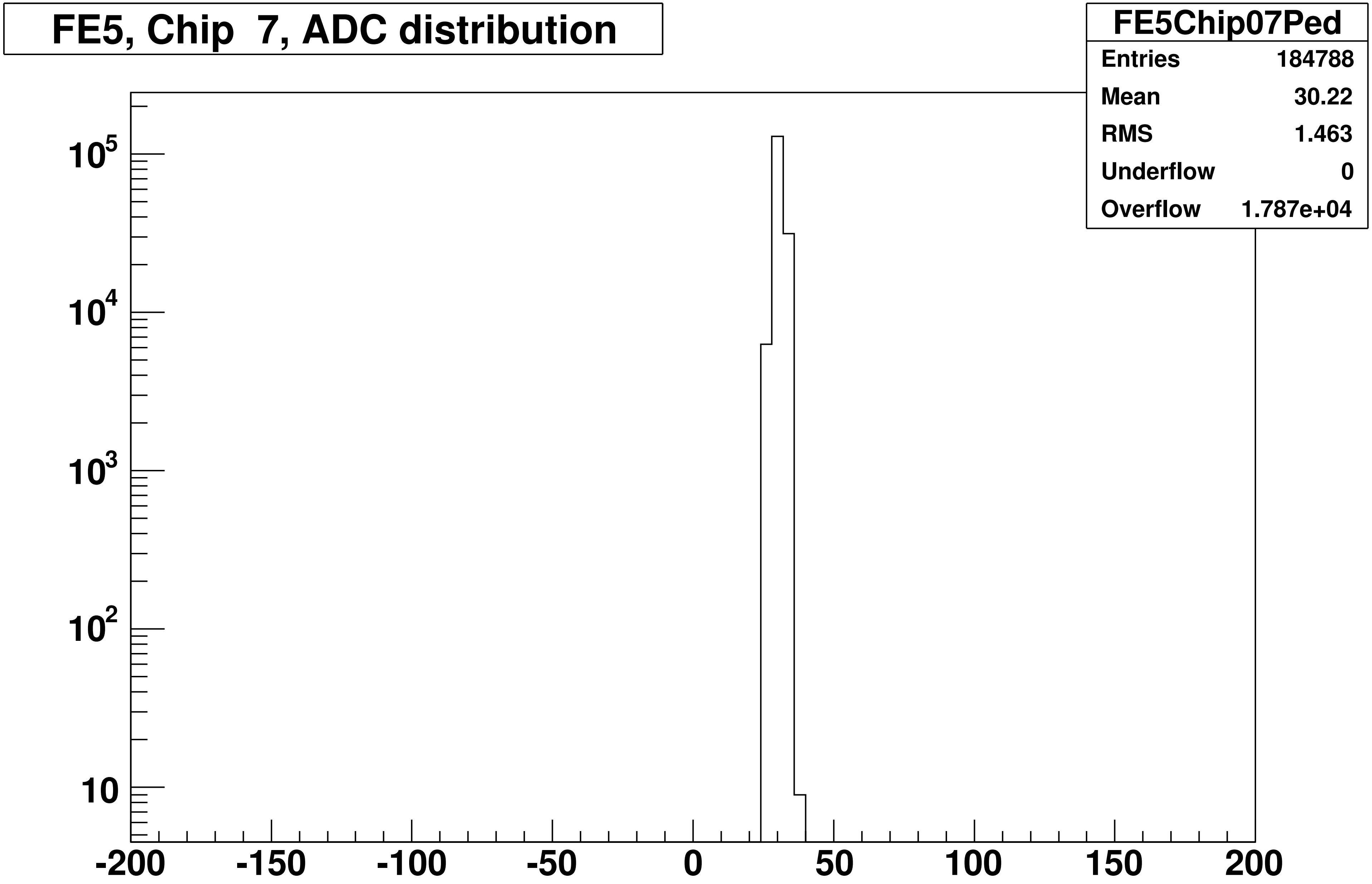
20000
25000



FE5, Chip 7, ADC distribution
FE5Chip07Ped
Entries 184788
Mean 30.22
RMS 1.463
Underflow 0
Overflow 1.787e+04
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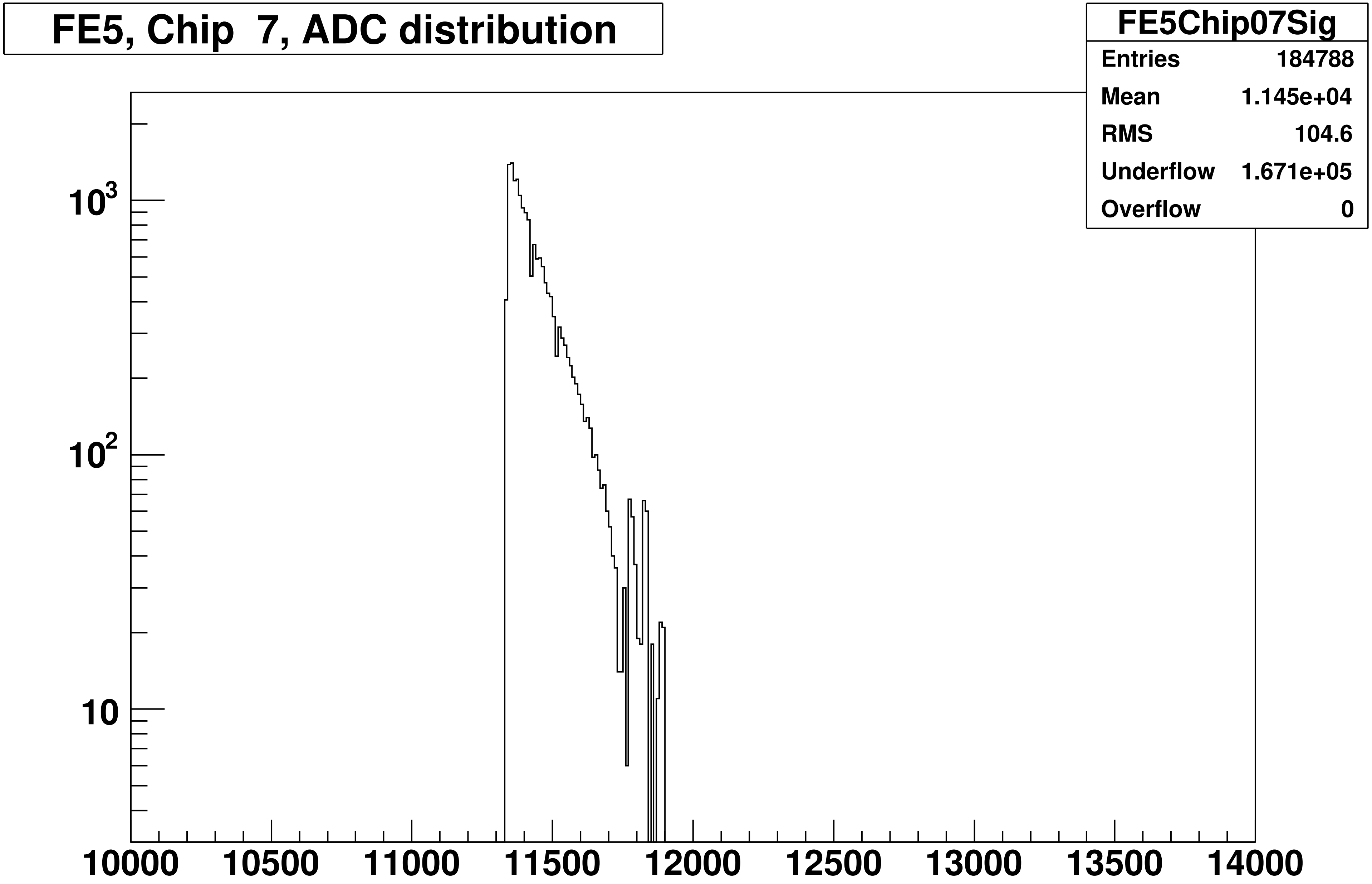
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200


FE5, Chip 7, ADC distribution
FE5Chip07Sig
Entries 184788
Mean 1.145e+04
RMS 104.6
Underflow 1.671e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
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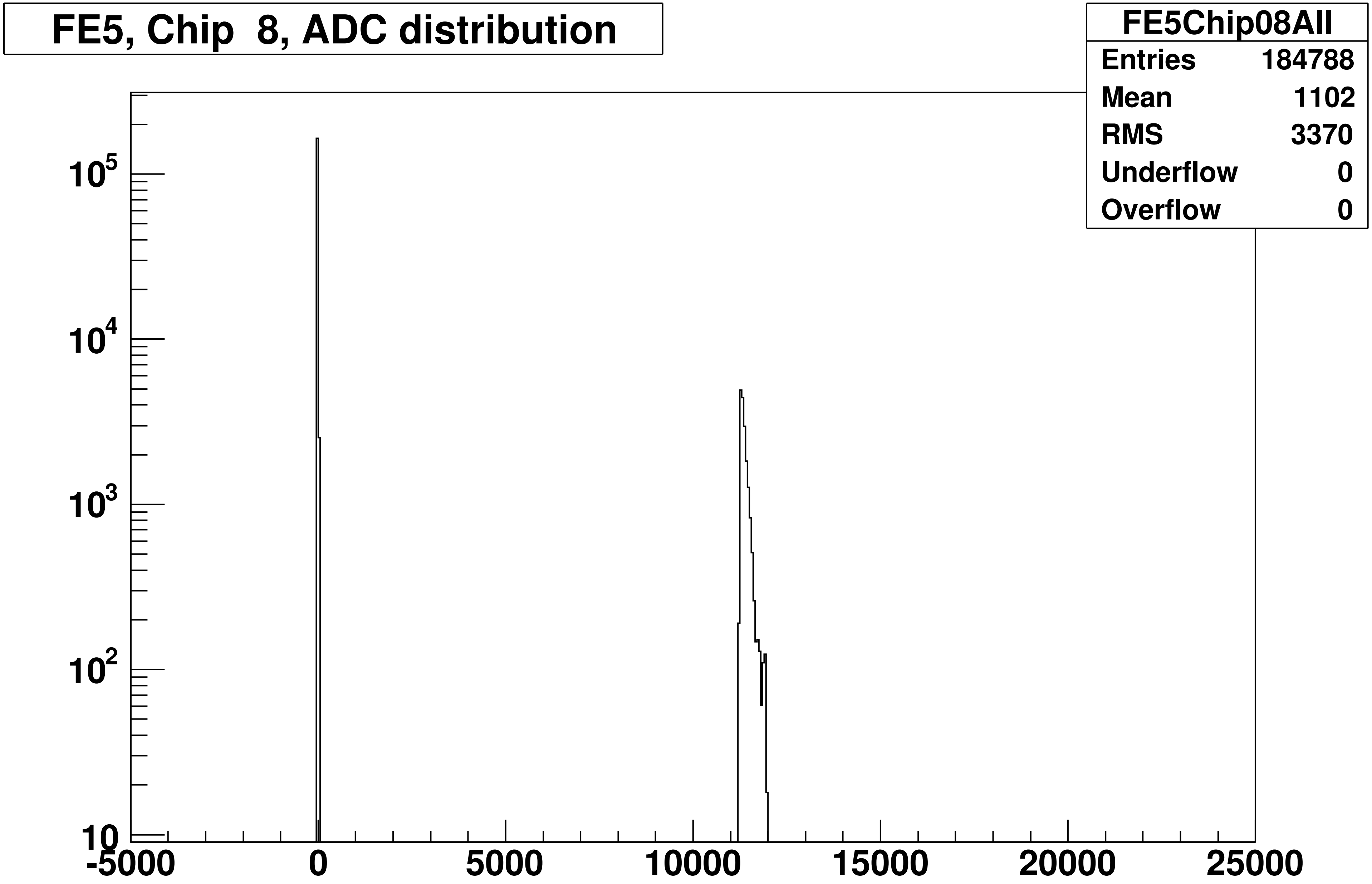
13500
14000


FE5, Chip 8, ADC distribution
FE5Chip08All
Entries 184788
Mean 1102
RMS 3370
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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-5000
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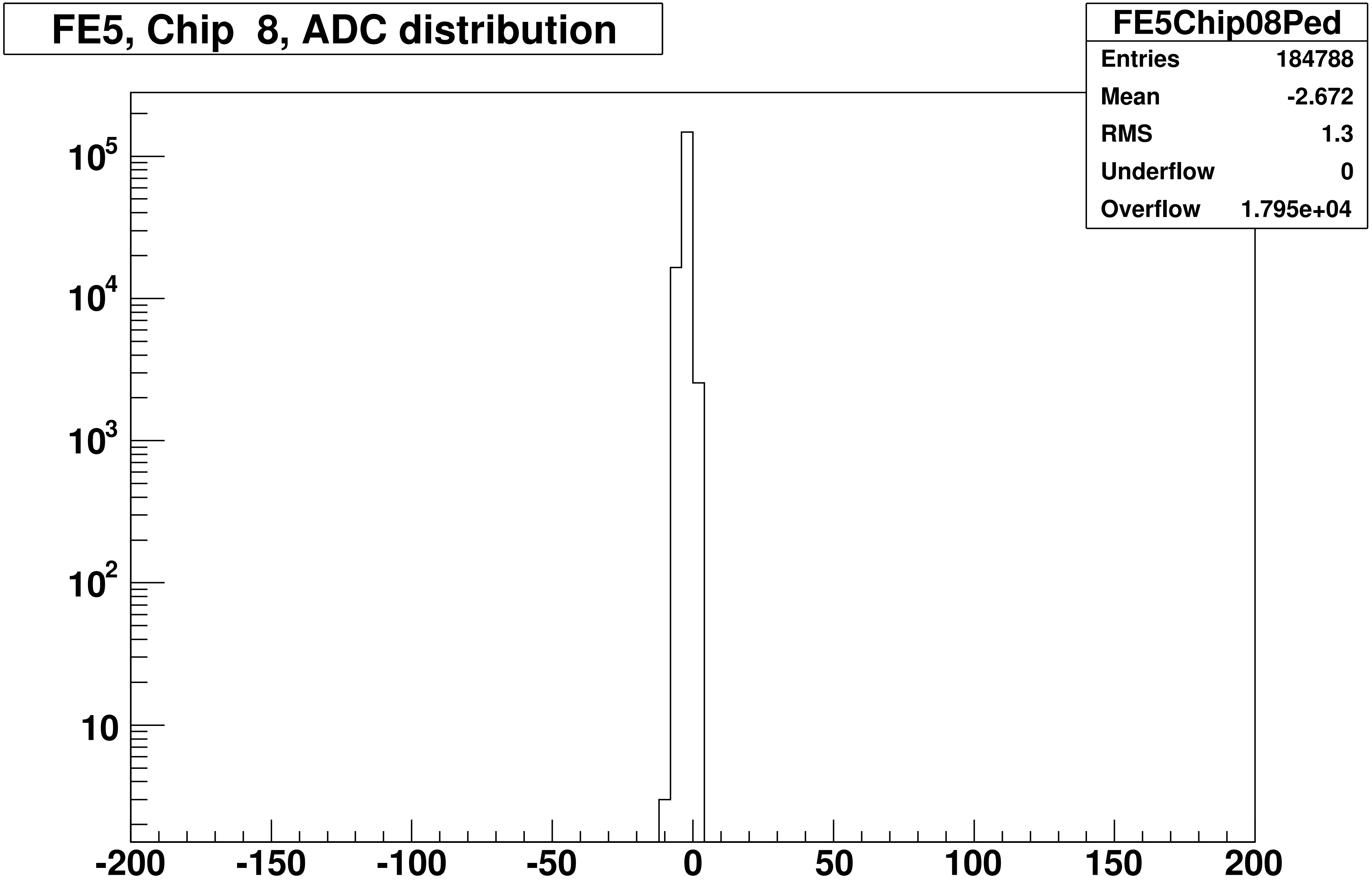
FE5, Chip 8, ADC distribution
FE5Chip08Ped
Entries 184788
Mean -2.672
RMS 1.3
Underflow 0
Overflow 1.795e+04
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10^4
10^3
10^2
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100
150
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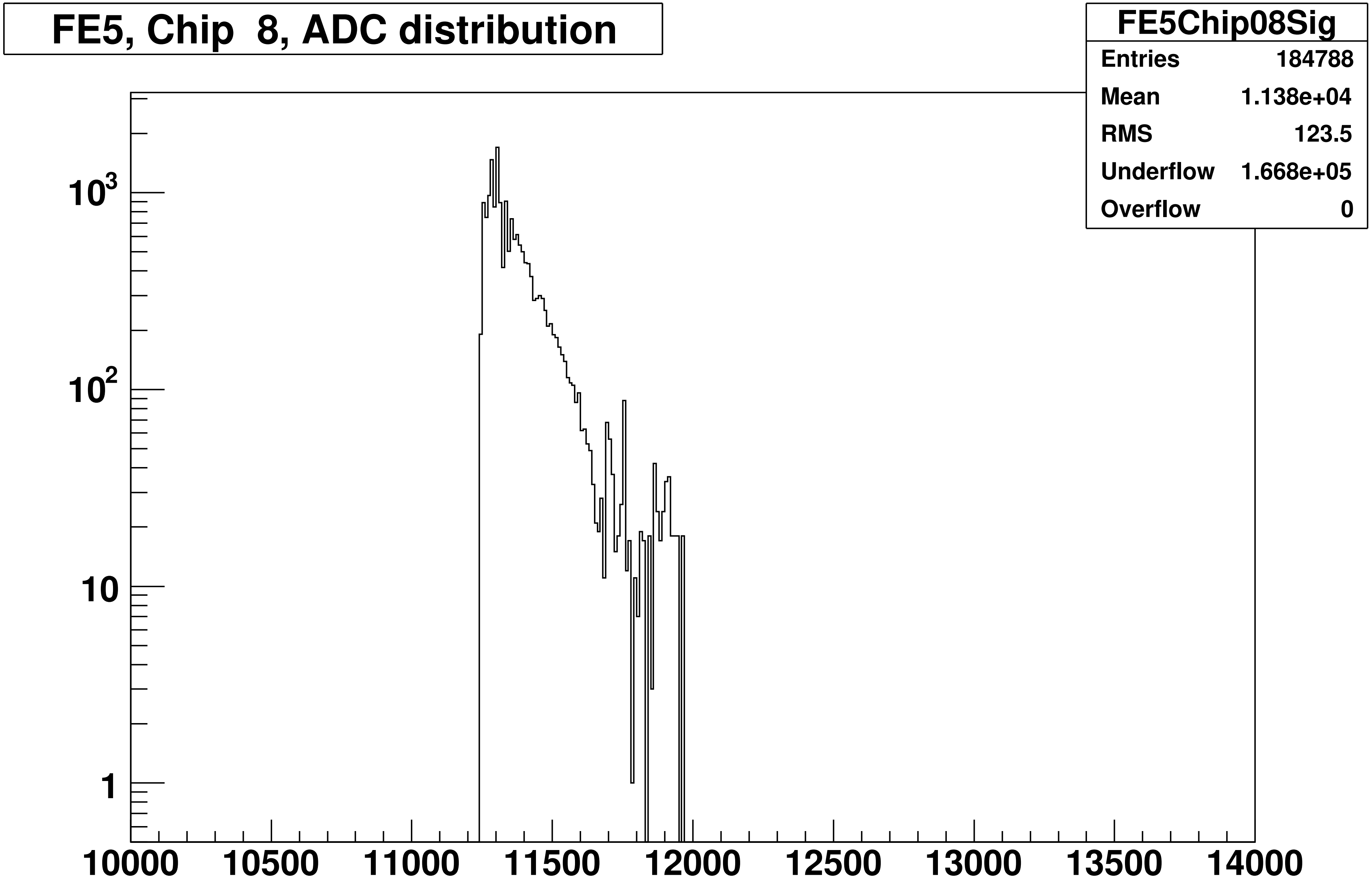
FE5, Chip 8, ADC distribution
FE5Chip08Sig
Entries 184788
Mean 1.138e+04
RMS 123.5
Underflow 1.668e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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13500
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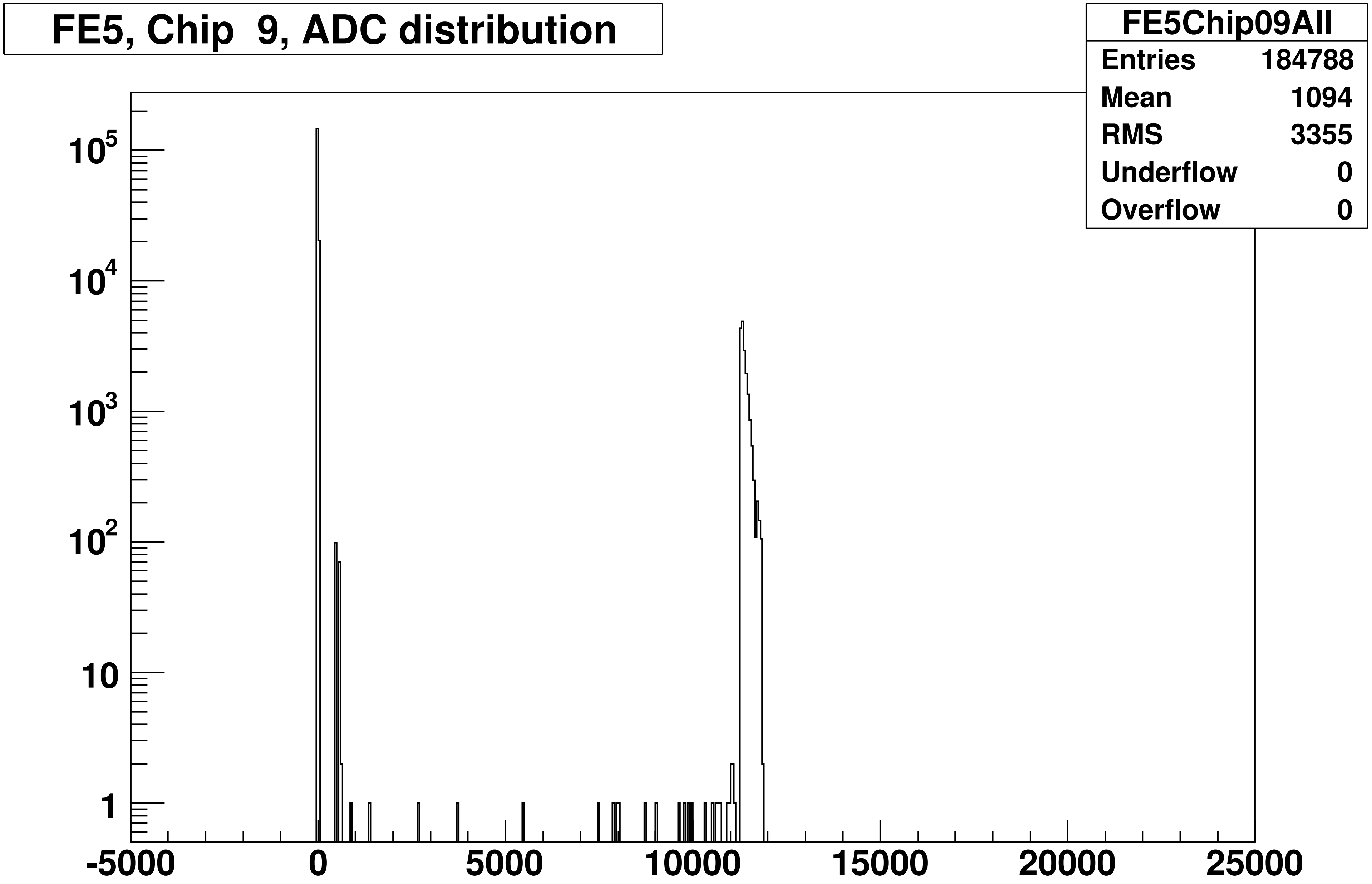

FE5, Chip 9, ADC distribution
FE5Chip09All
Entries 184788
Mean 1094
RMS 3355
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
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10000
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20000
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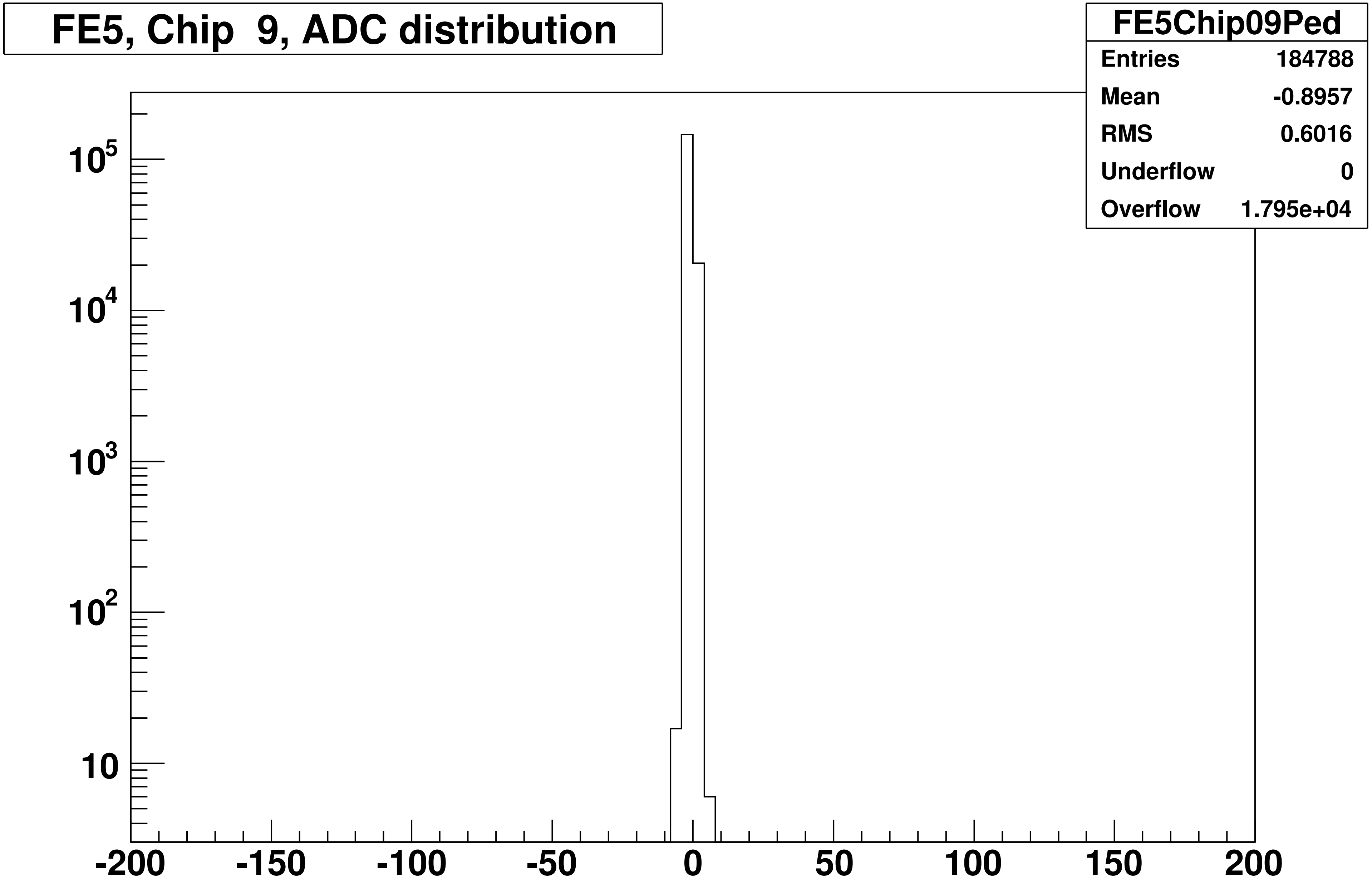
FE5, Chip 9, ADC distribution
FE5Chip09Ped
Entries 184788
Mean -0.8957
RMS 0.6016
Underflow 0
Overflow 1.795e+04
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10^4
10^3
10^2
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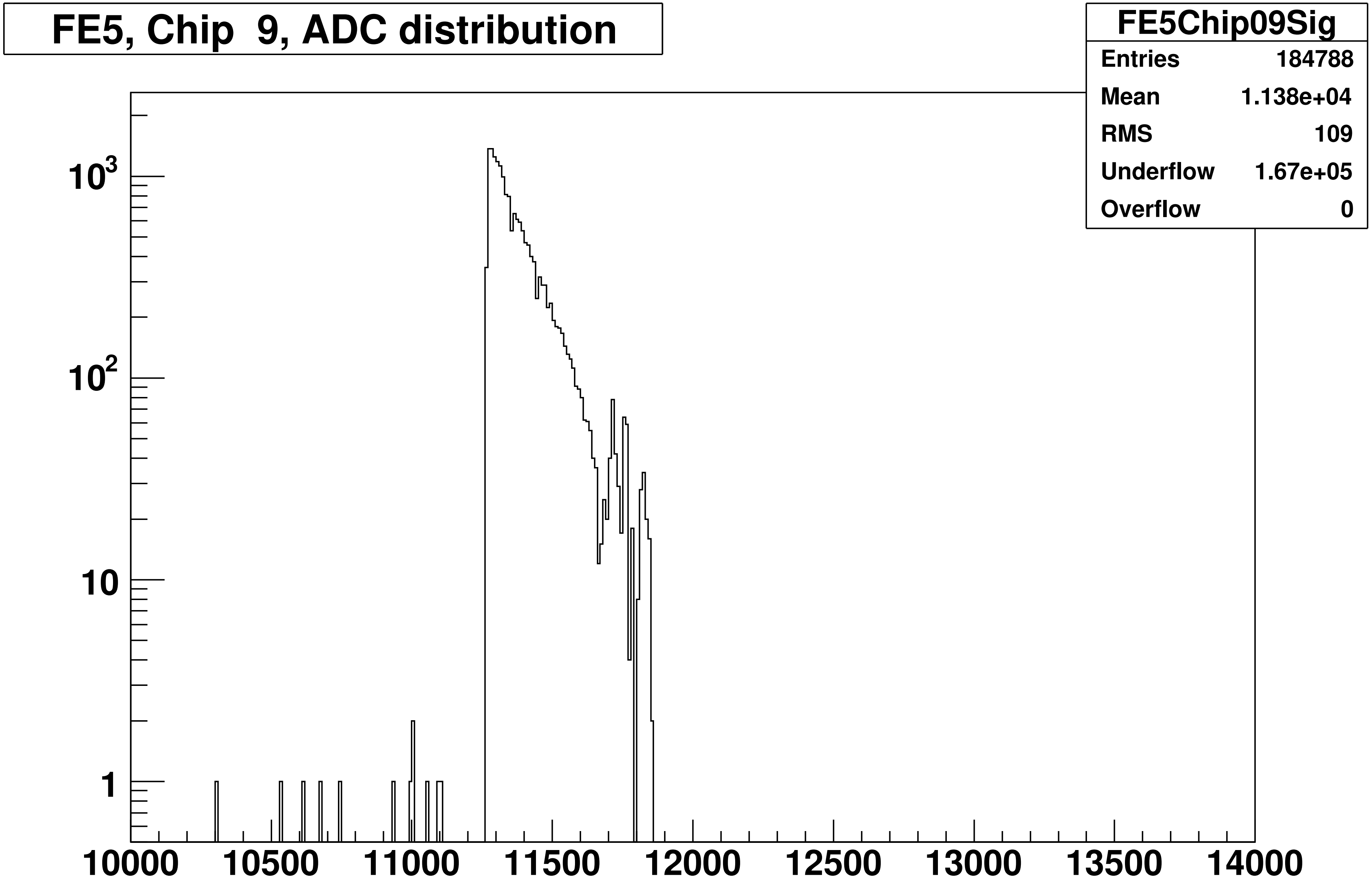
FE5, Chip 9, ADC distribution
FE5Chip09Sig
Entries 184788
Mean 1.138e+04
RMS 109
Underflow 1.67e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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11500
12000
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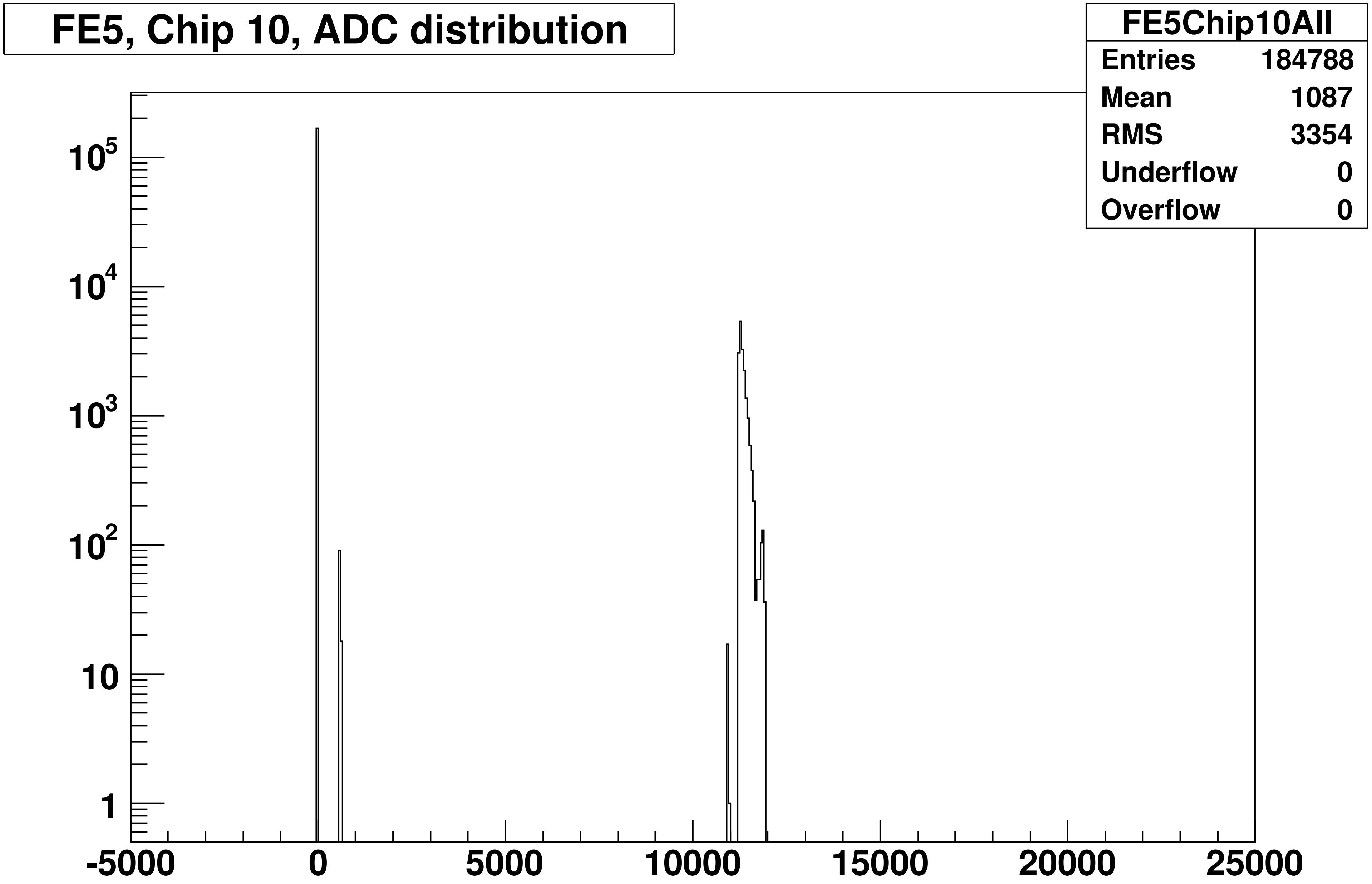
FE5, Chip 10, ADC distribution
FE5Chip10All
Entries 184788
Mean 1087
RMS 3354
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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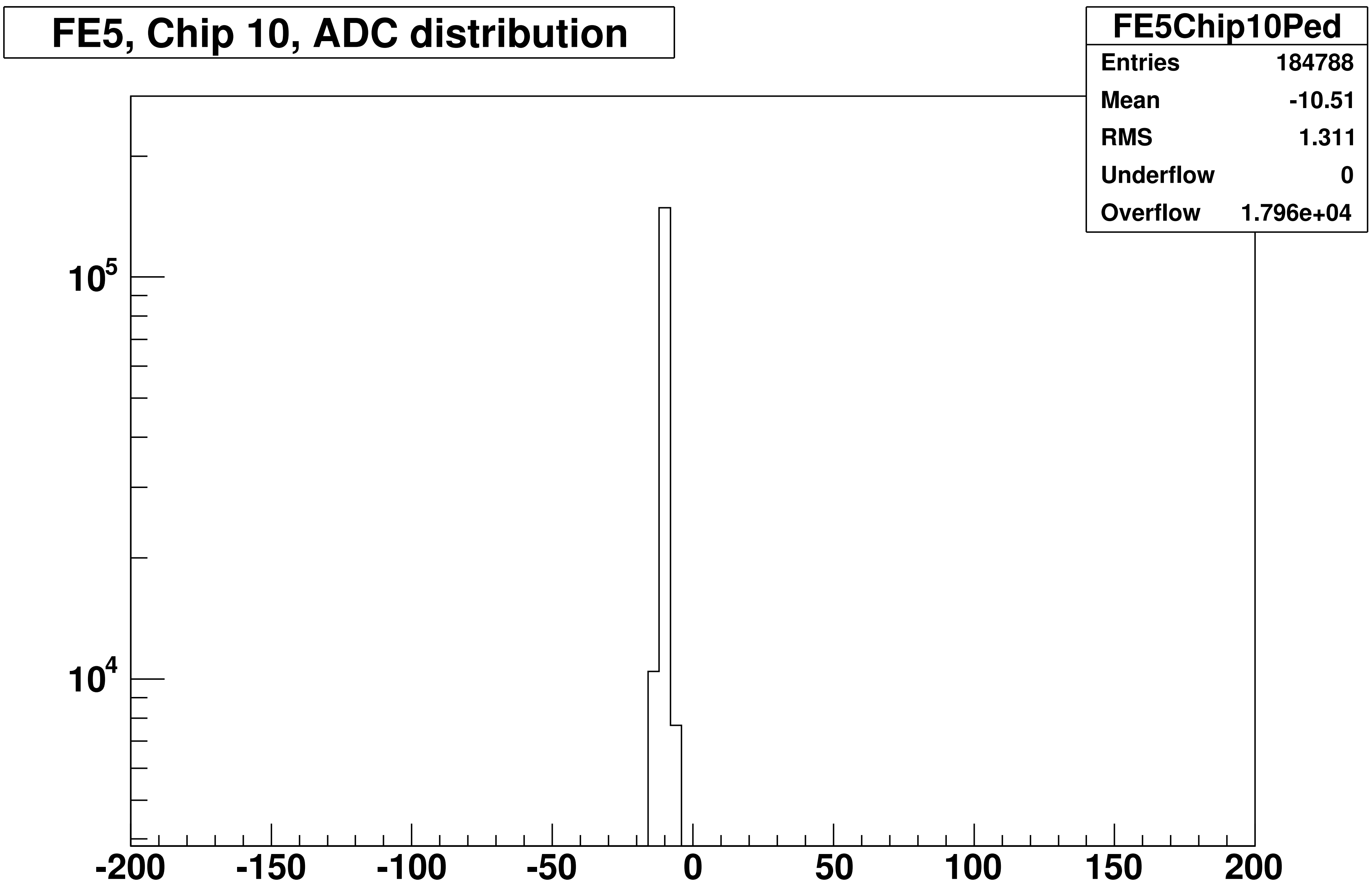
10000
15000
20000
25000


FE5, Chip 10, ADC distribution
FE5Chip10Ped
Entries 184788
Mean -10.51
RMS 1.311
Underflow 0
Overflow 1.796e+04
10^5
10^4
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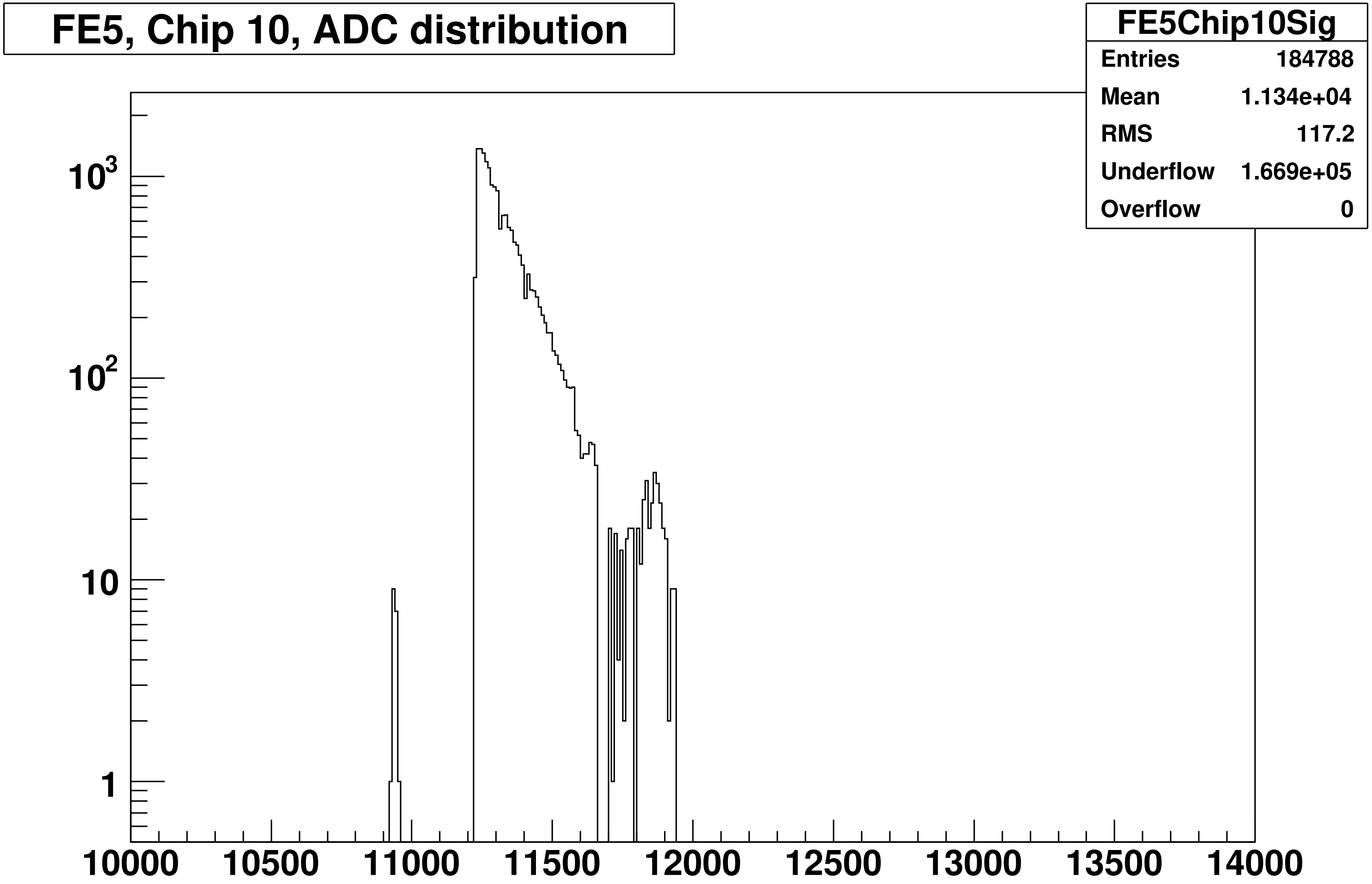
-150
-100
-50
0
50
100
150
200


FE5, Chip 10, ADC distribution
FE5Chip10Sig
Entries 184788
Mean 1.134e+04
RMS 117.2
Underflow 1.669e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
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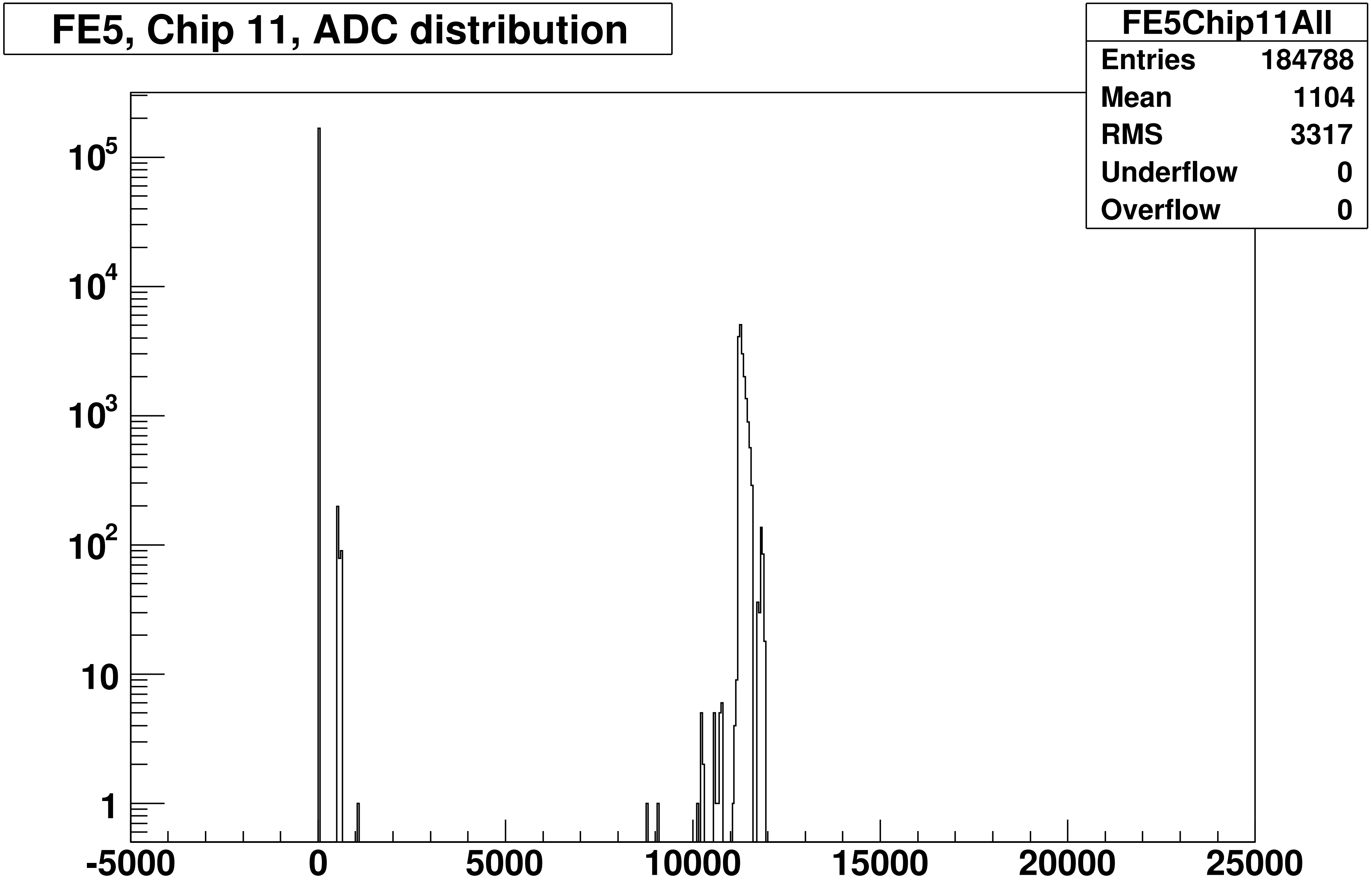
FE5, Chip 11, ADC distribution
FE5Chip11All
Entries 184788
Mean 1104
RMS 3317
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
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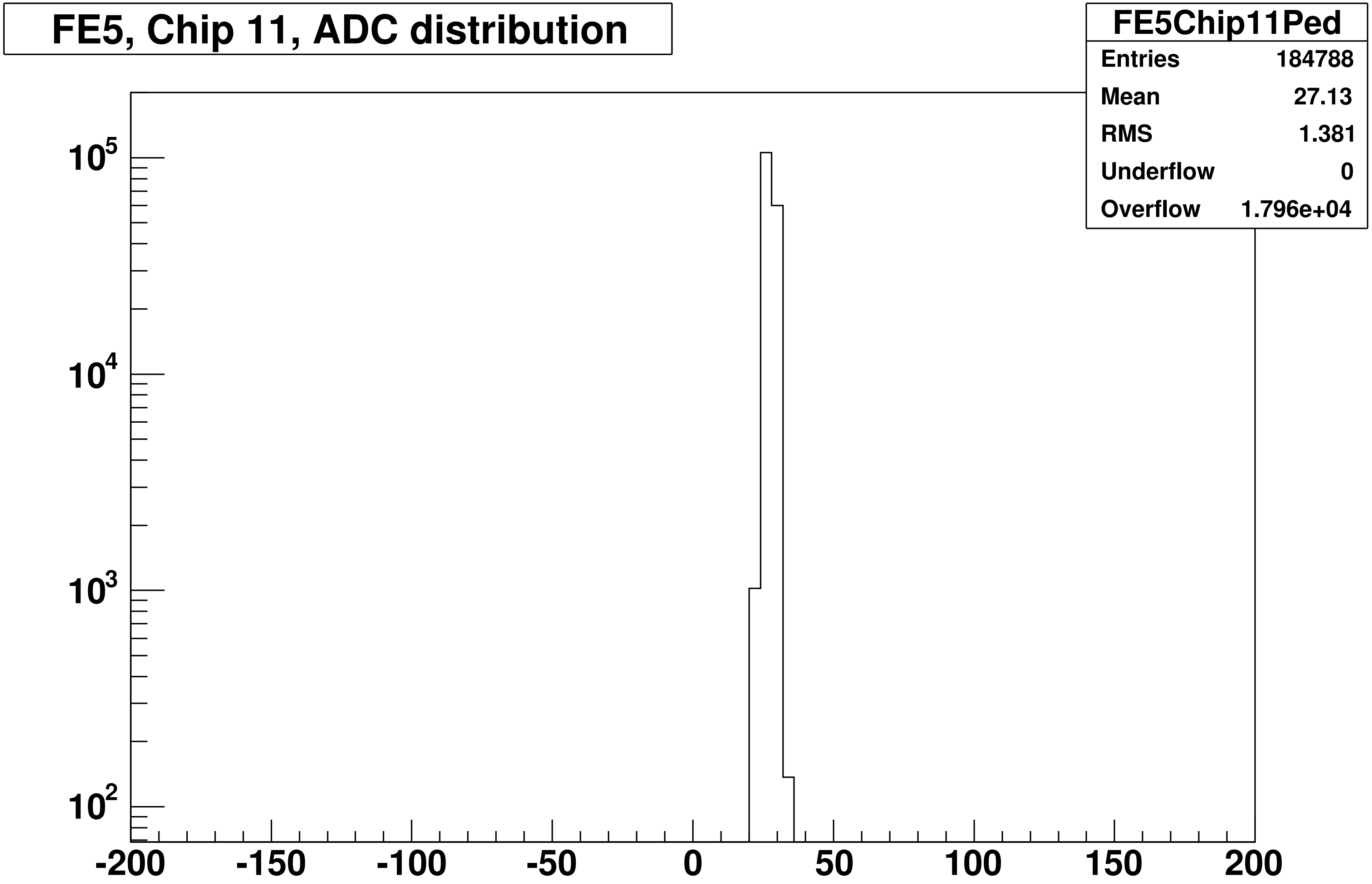
FE5, Chip 11, ADC distribution
FE5Chip11Ped
Entries 184788
Mean 27.13
RMS 1.381
Underflow 0
Overflow 1.796e+04
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10^4
10^3
10^2
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-150
-100
-50
0
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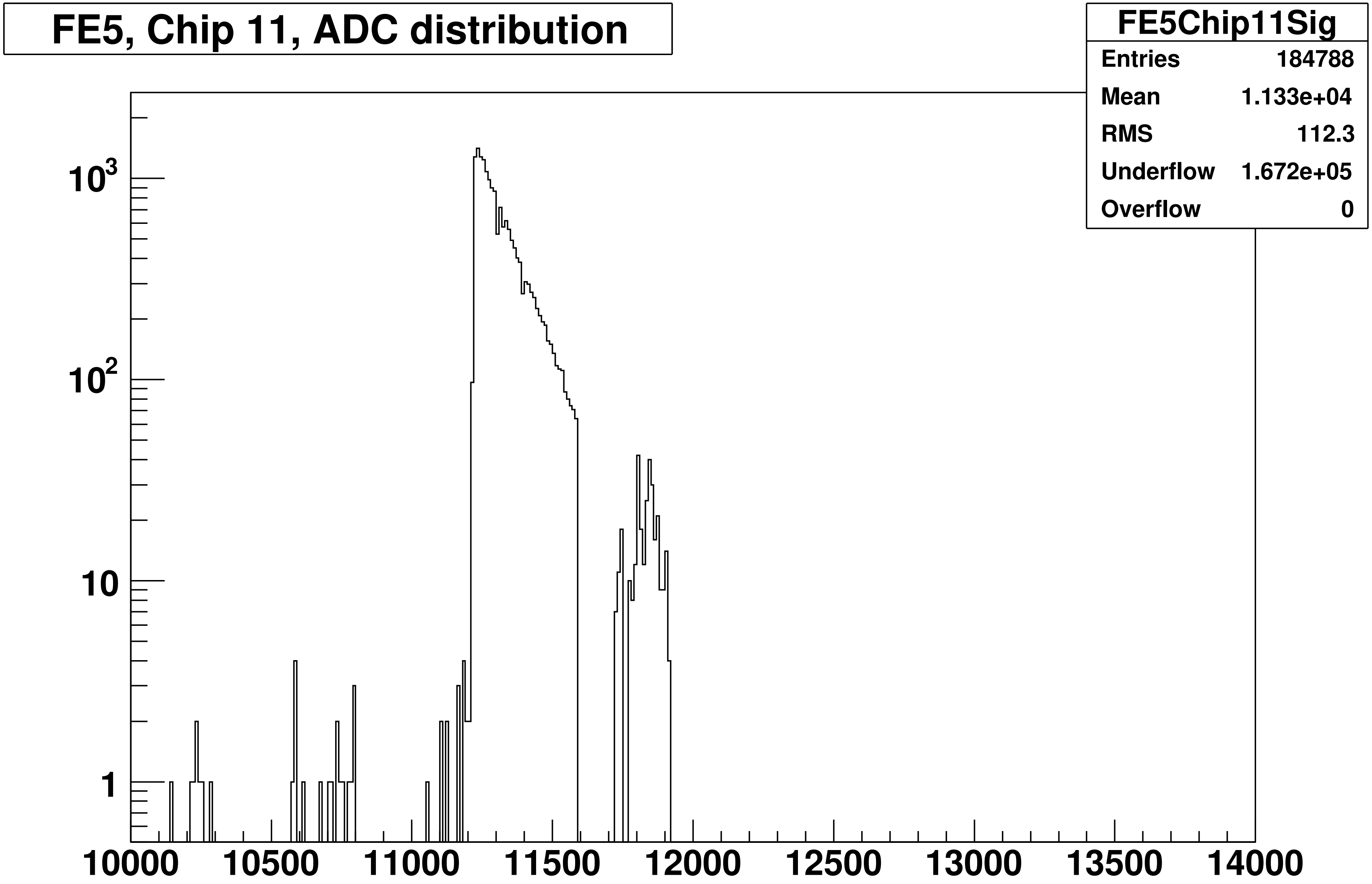
100
150
200


FE5, Chip 11, ADC distribution
FE5Chip11Sig
Entries 184788
Mean 1.133e+04
RMS 112.3
Underflow 1.672e+05
Overflow 0
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10^2
10
1
10000
10500
11000
11500
12000
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13000
13500
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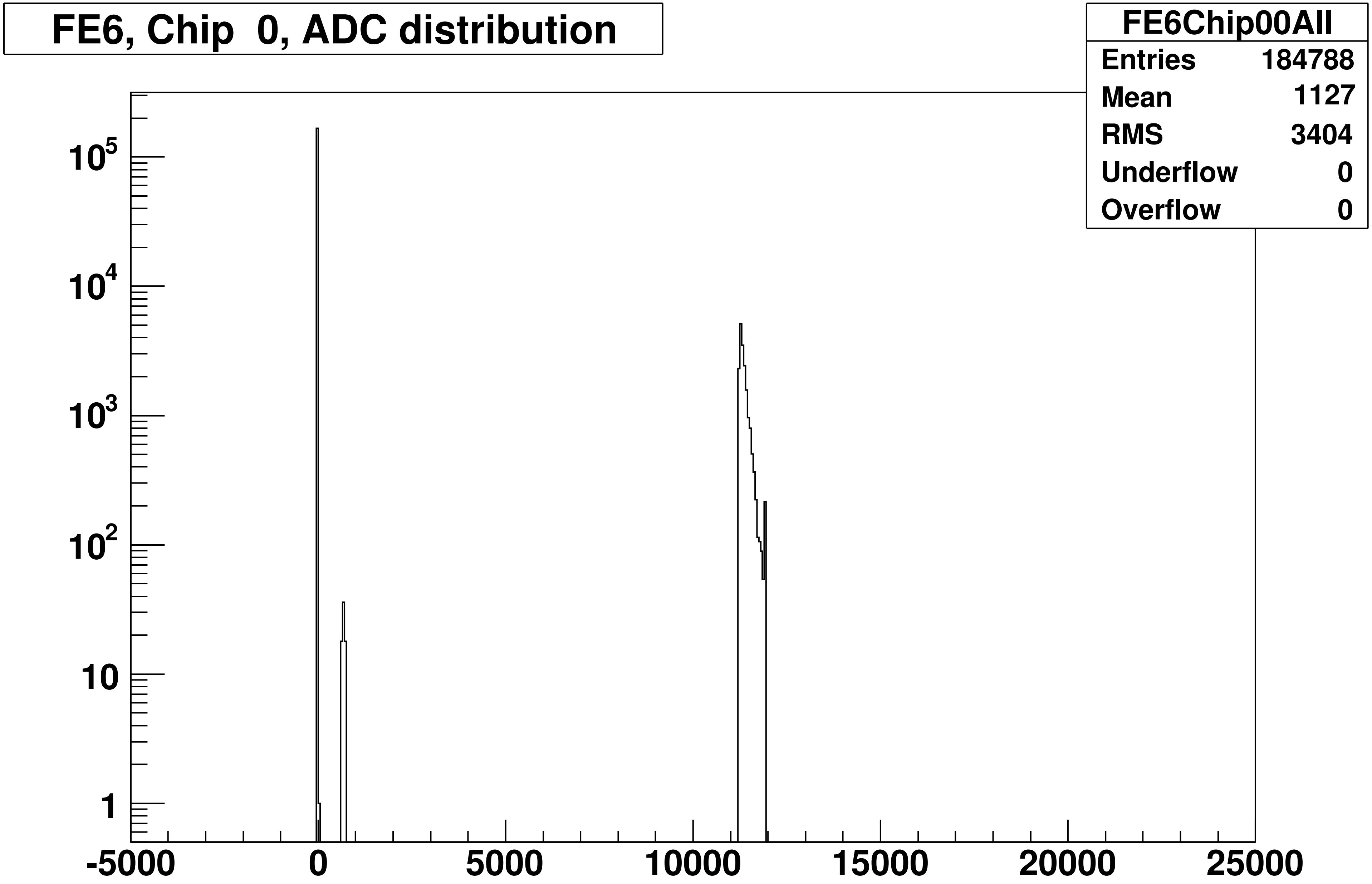

FE6, Chip 0, ADC distribution
FE6Chip00All
Entries 184788
Mean 1127
RMS 3404
Underflow 0
Overflow 0
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10^4
10^3
10^2
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1
-5000
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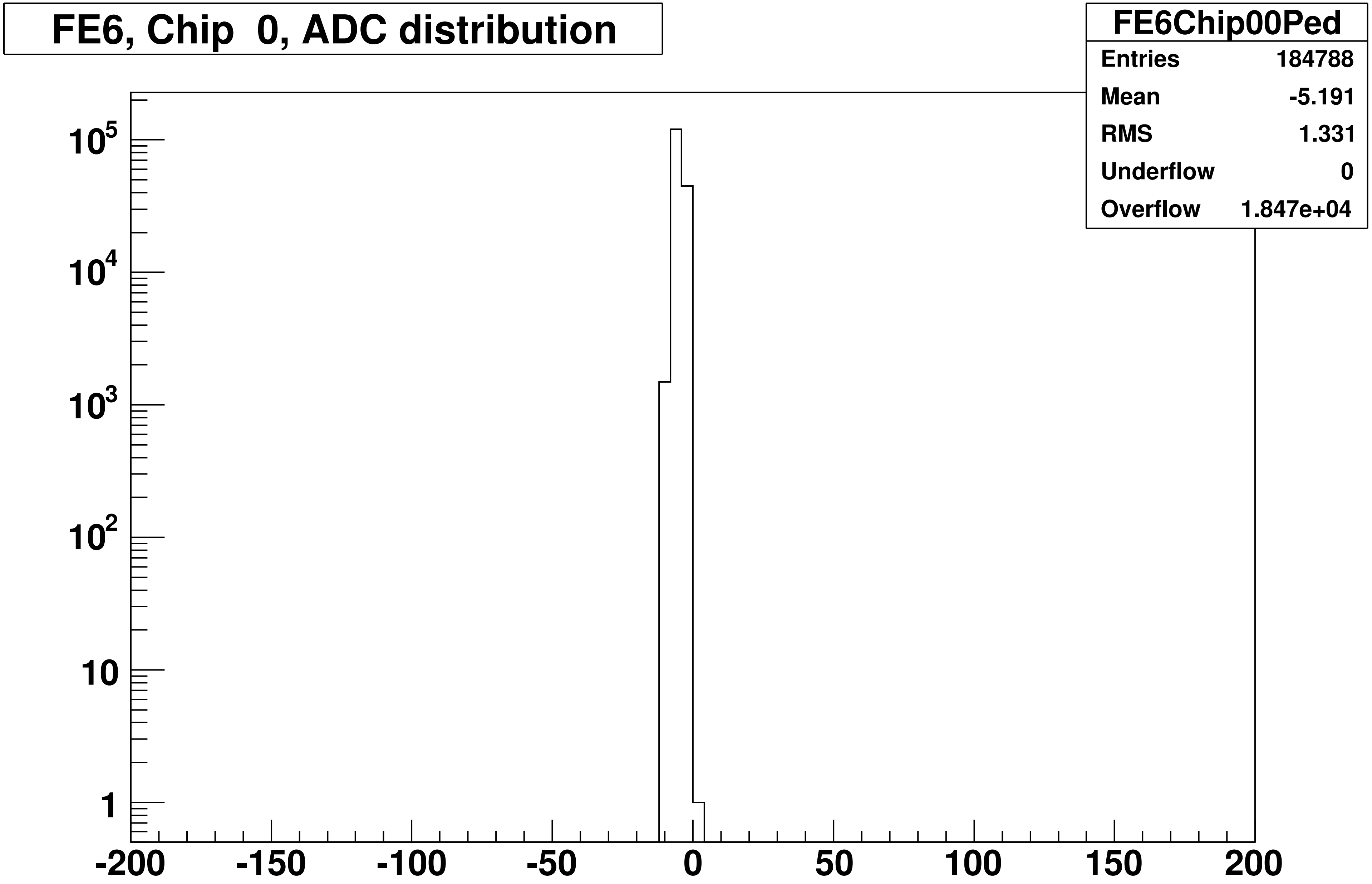
FE6, Chip 0, ADC distribution
FE6Chip00Ped
Entries 184788
Mean -5.191
RMS 1.331
Underflow 0
Overflow 1.847e+04
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10^4
10^3
10^2
10
1
-200
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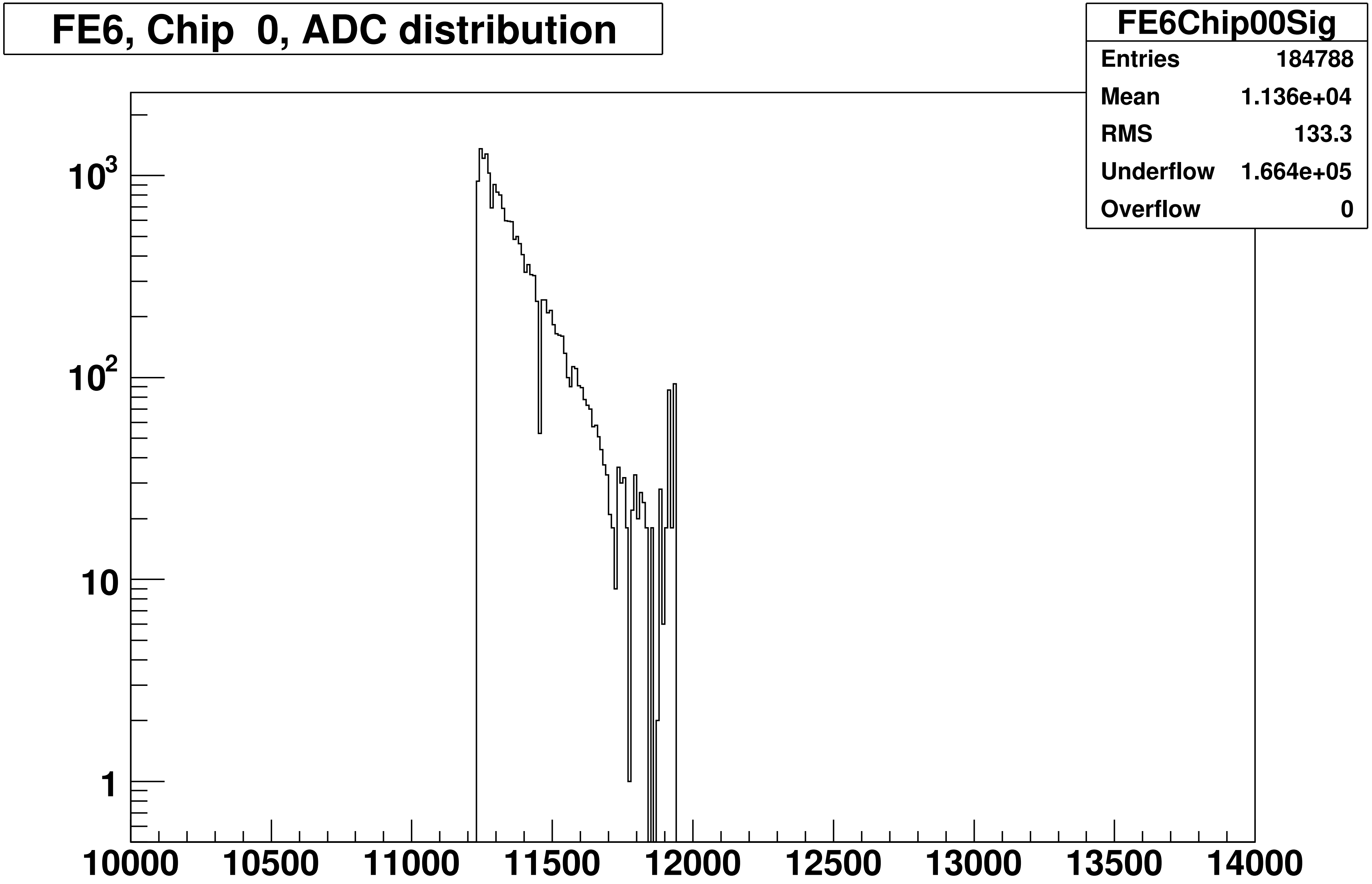
-100
-50
0
50
100
150
200


FE6, Chip 0, ADC distribution
FE6Chip00Sig
Entries 184788
Mean 1.136e+04
RMS 133.3
Underflow 1.664e+05
Overflow 0
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10^2
10
1
10000
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11500
12000
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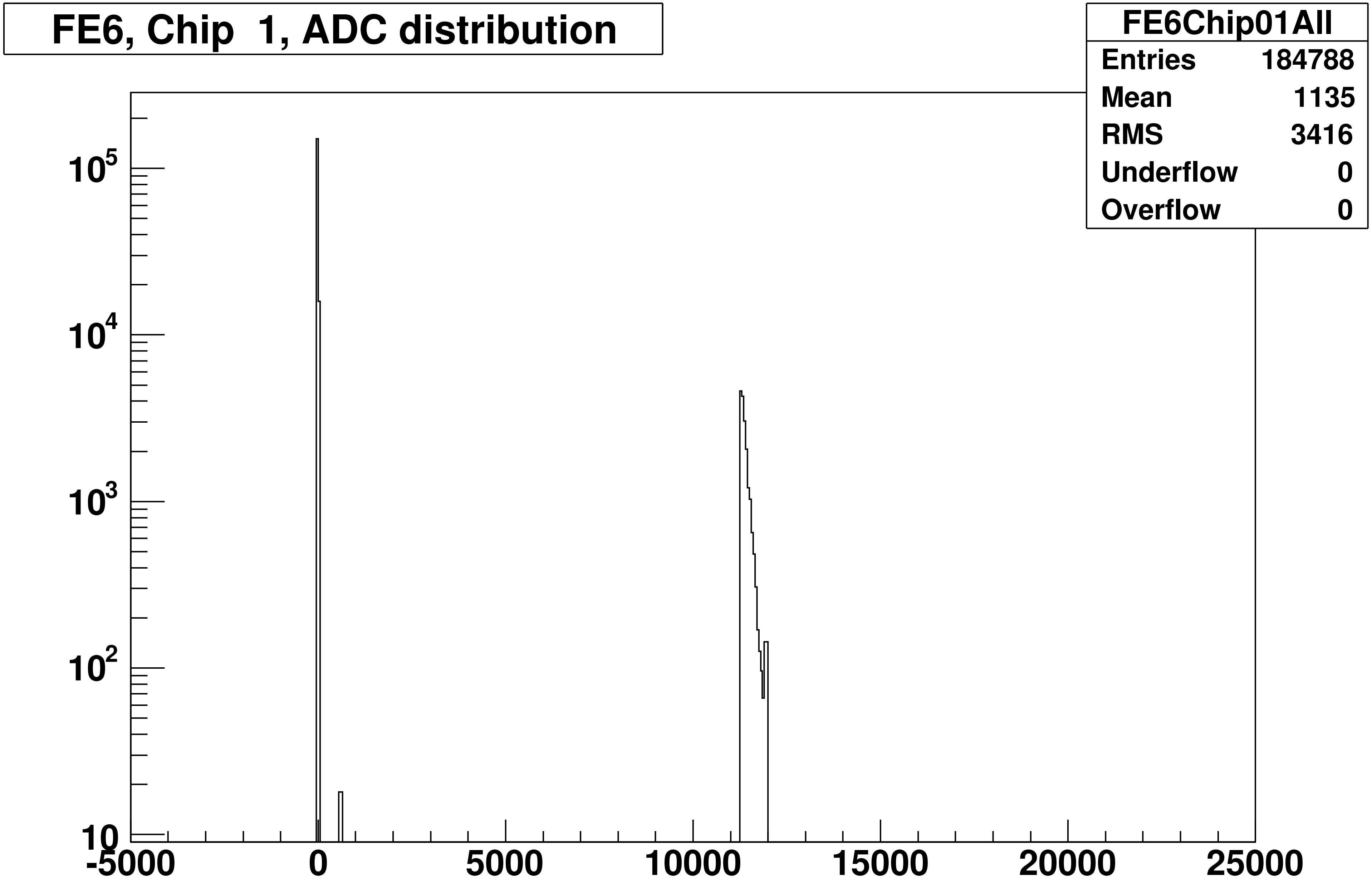
FE6, Chip 1, ADC distribution
FE6Chip01All
Entries 184788
Mean 1135
RMS 3416
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
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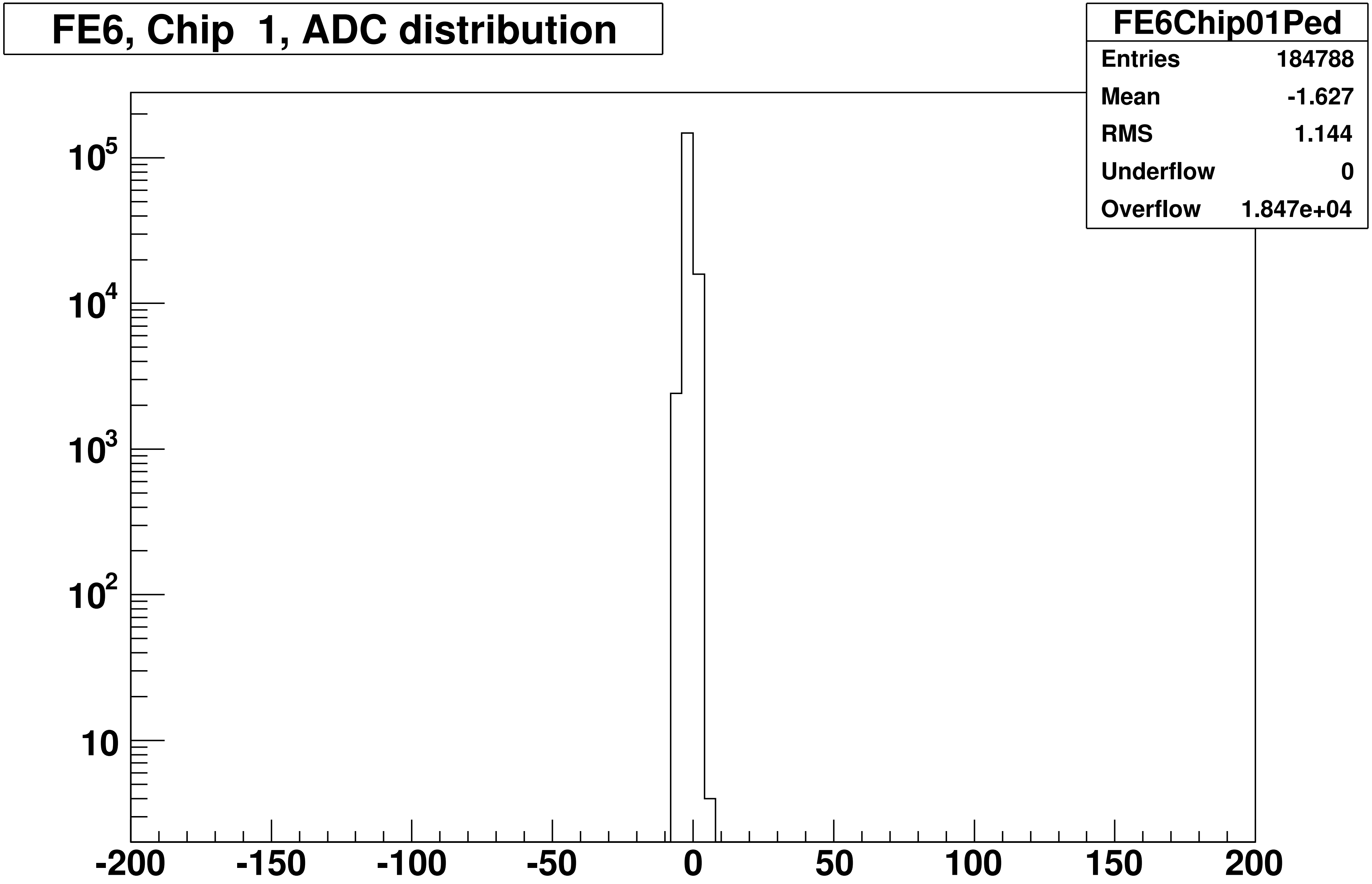
25000



FE6, Chip 1, ADC distribution
FE6Chip01Ped
Entries 184788
Mean -1.627
RMS 1.144
Underflow 0
Overflow 1.847e+04
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10^4
10^3
10^2
10
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150
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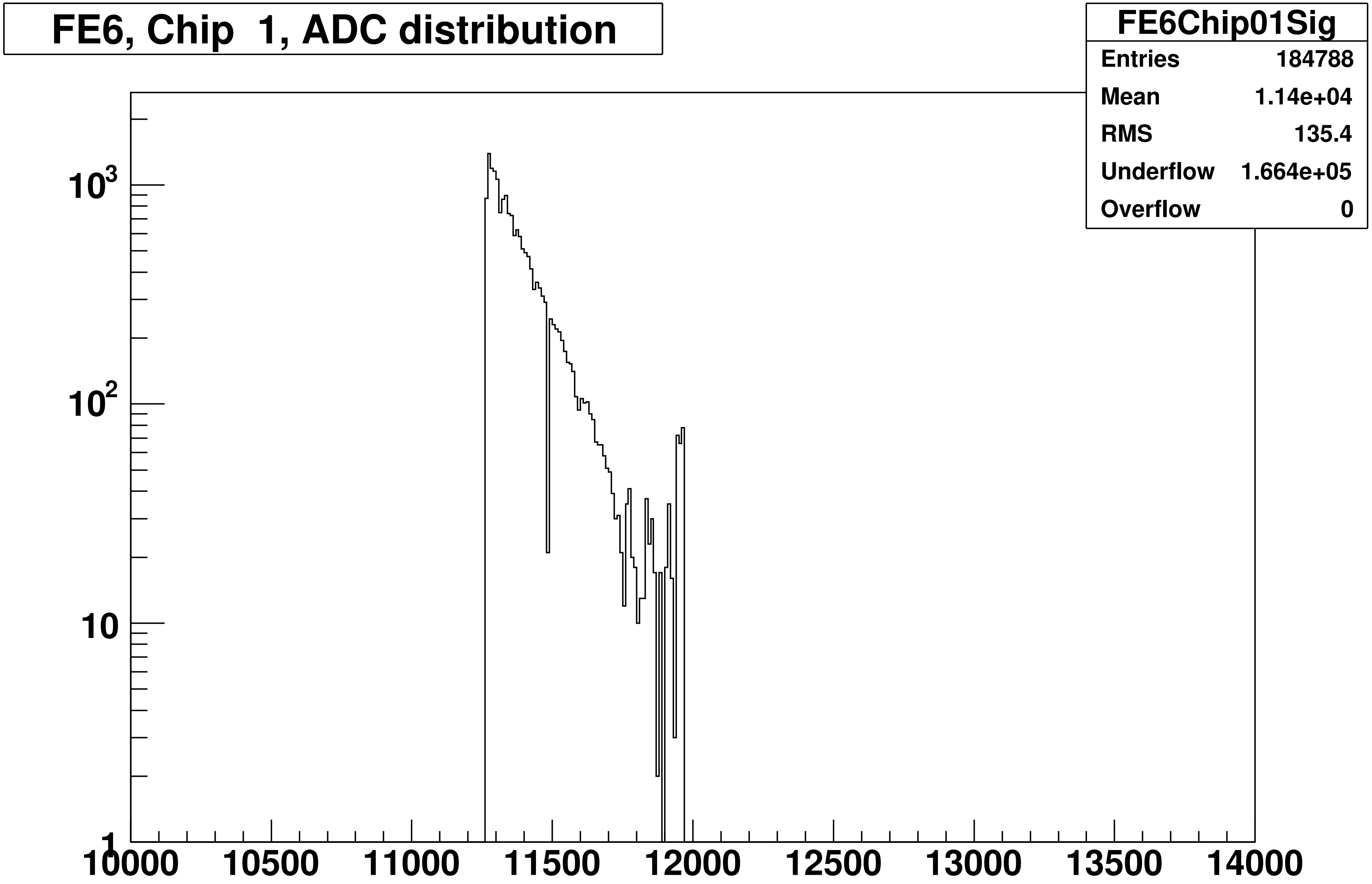
FE6, Chip 1, ADC distribution
FE6Chip01Sig
Entries 184788
Mean 1.14e+04
RMS 135.4
Underflow 1.664e+05
Overflow 0
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10^2
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1
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11500
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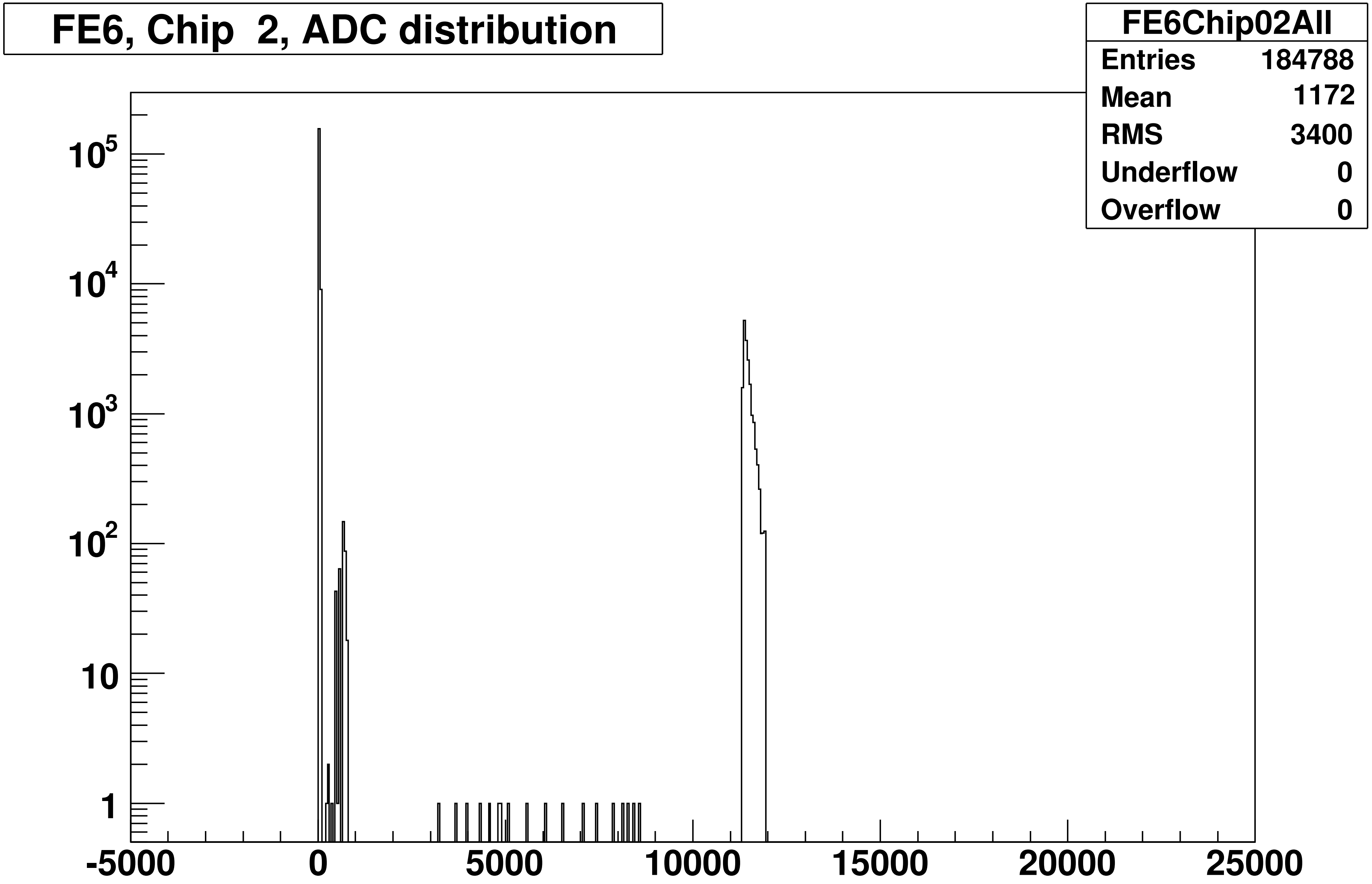

FE6, Chip 2, ADC distribution
FE6Chip02All
Entries 184788
Mean 1172
RMS 3400
Underflow 0
Overflow 0
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10^4
10^3
10^2
10
1
-5000
0
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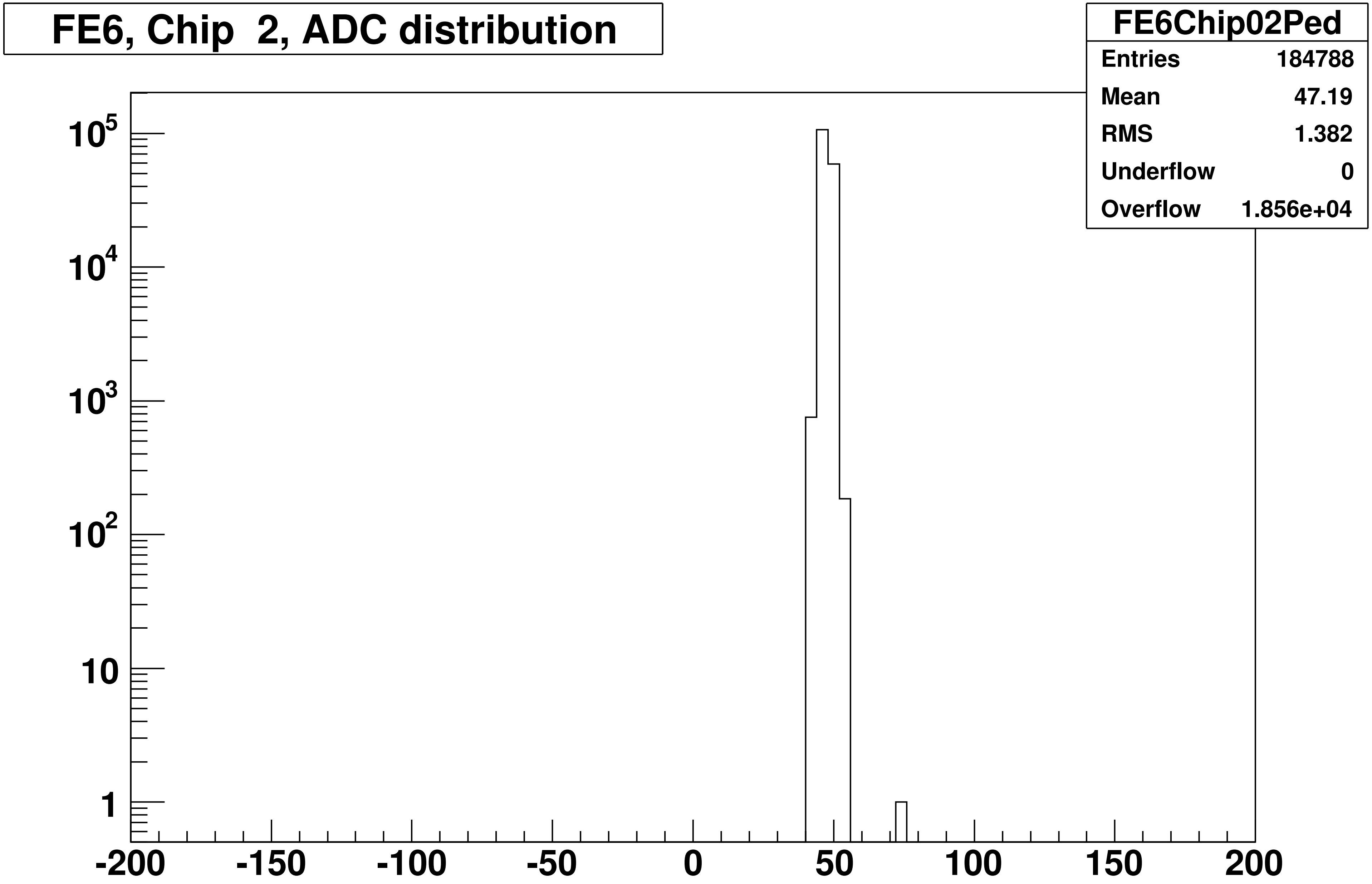
10000
15000
20000
25000


FE6, Chip 2, ADC distribution
FE6Chip02Ped
Entries 184788
Mean 47.19
RMS 1.382
Underflow 0
Overflow 1.856e+04
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10^3
10^2
10
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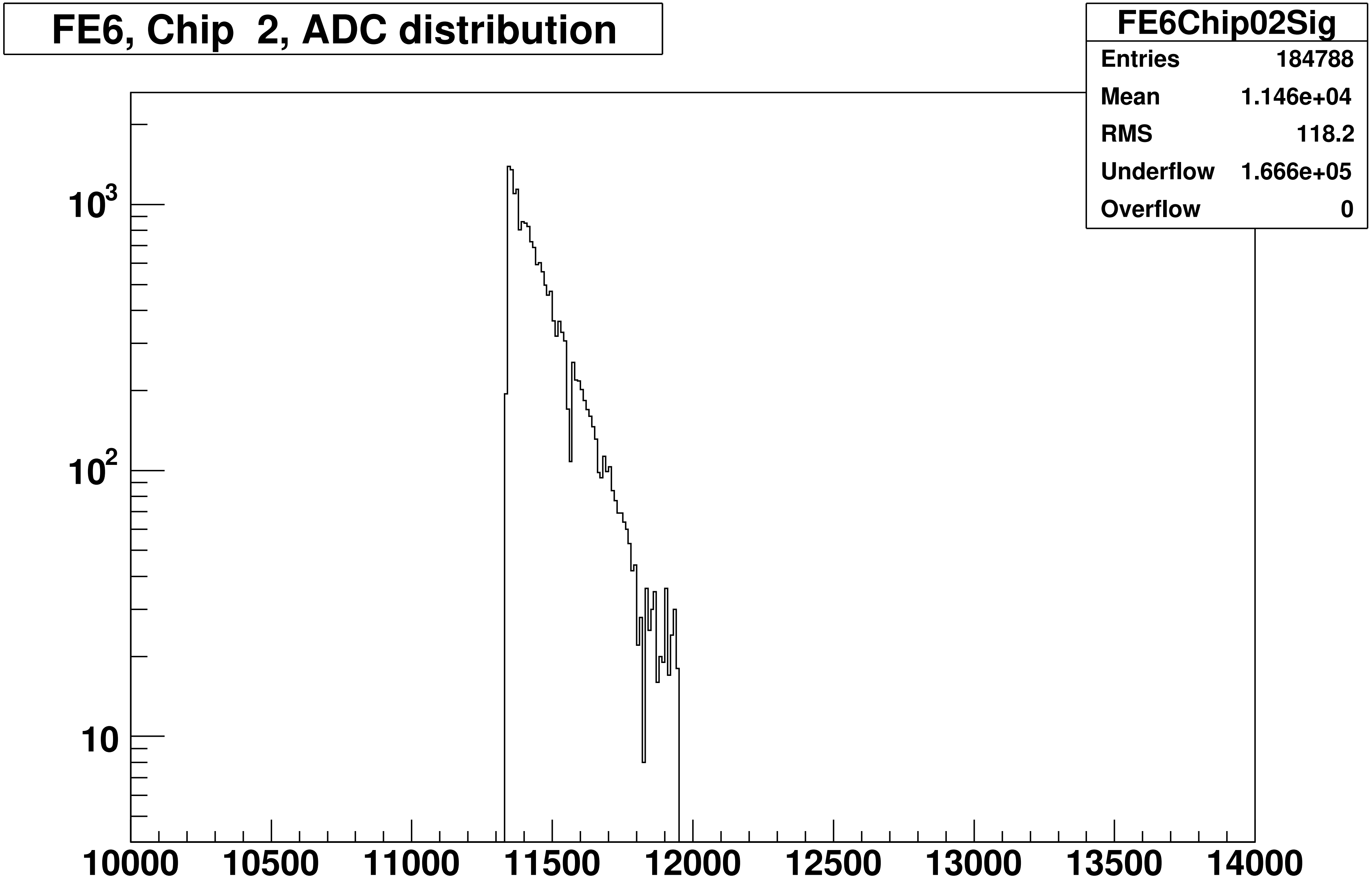
FE6, Chip 2, ADC distribution
FE6Chip02Sig
Entries 184788
Mean 1.146e+04
RMS 118.2
Underflow 1.666e+05
Overflow 0
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10^2
10
10000
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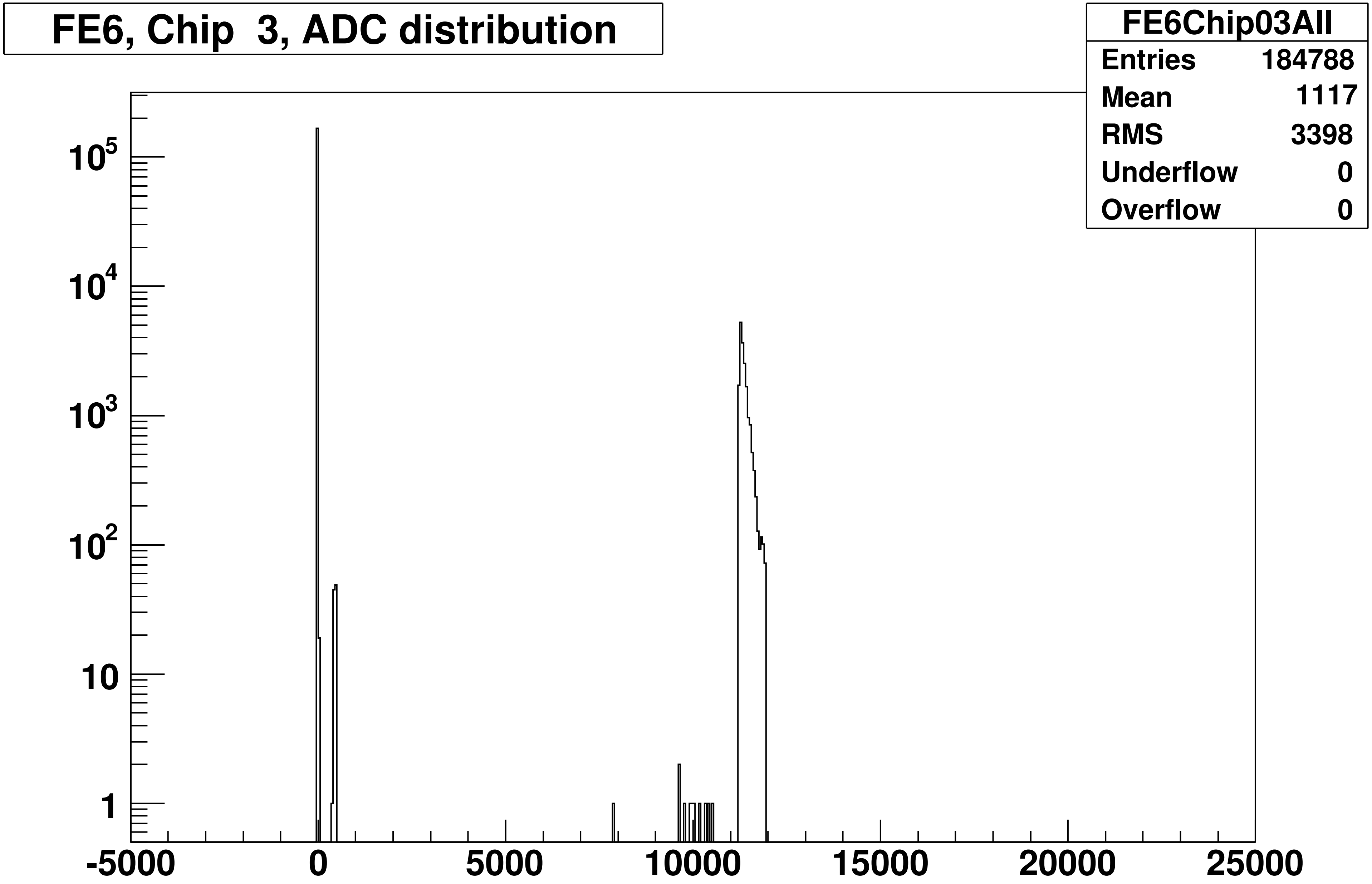
FE6, Chip 3, ADC distribution
FE6Chip03All
Entries 184788
Mean 1117
RMS 3398
Underflow 0
Overflow 0
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10^4
10^3
10^2
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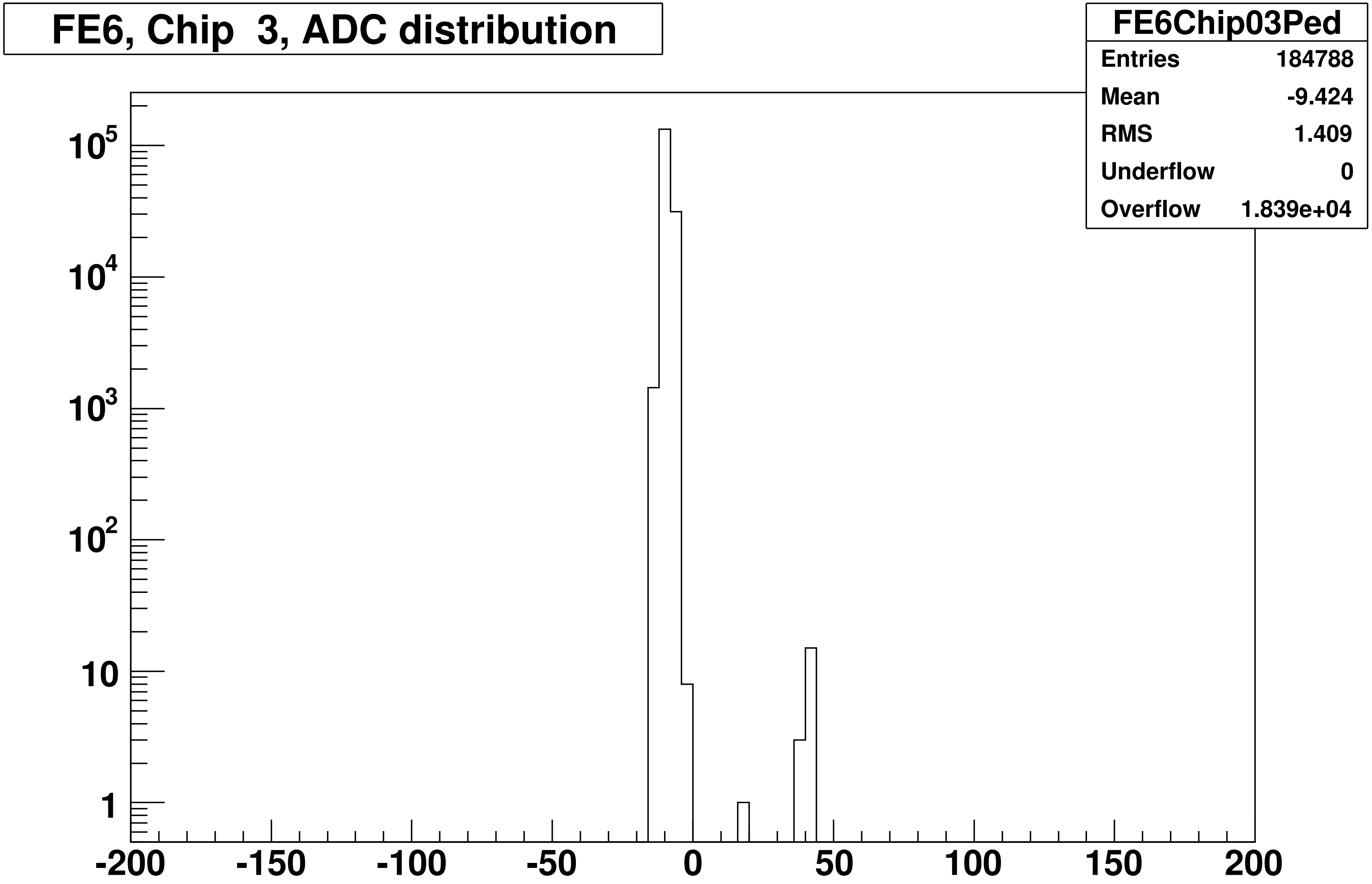
FE6, Chip 3, ADC distribution
FE6Chip03Ped
Entries 184788
Mean -9.424
RMS 1.409
Underflow 0
Overflow 1.839e+04
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10^4
10^3
10^2
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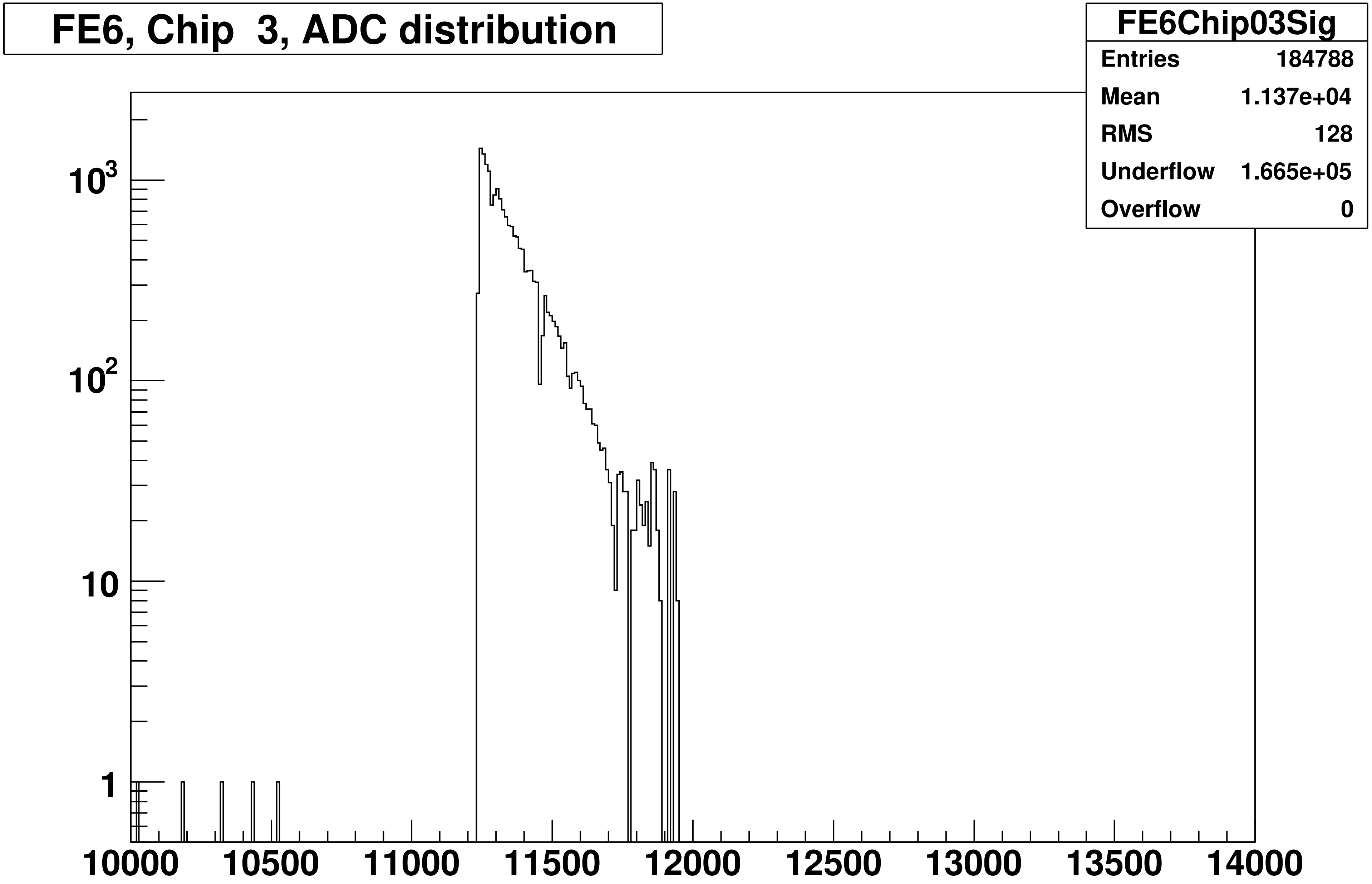
FE6, Chip 3, ADC distribution
FE6Chip03Sig
Entries 184788
Mean 1.137e+04
RMS 128
Underflow 1.665e+05
Overflow 0
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10^2
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1
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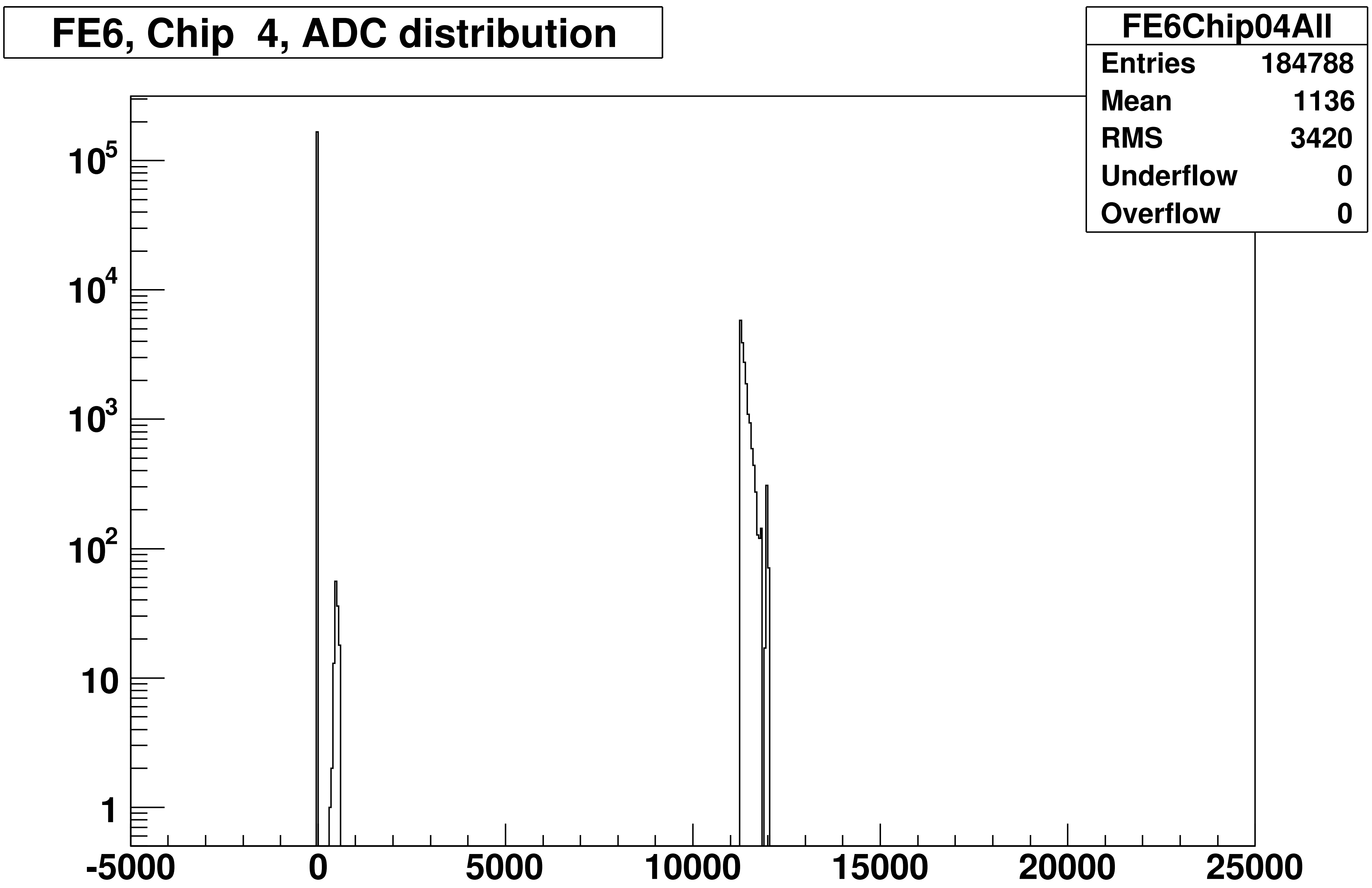
FE6, Chip 4, ADC distribution
FE6Chip04All
Entries 184788
Mean 1136
RMS 3420
Underflow 0
Overflow 0
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10^4
10^3
10^2
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0
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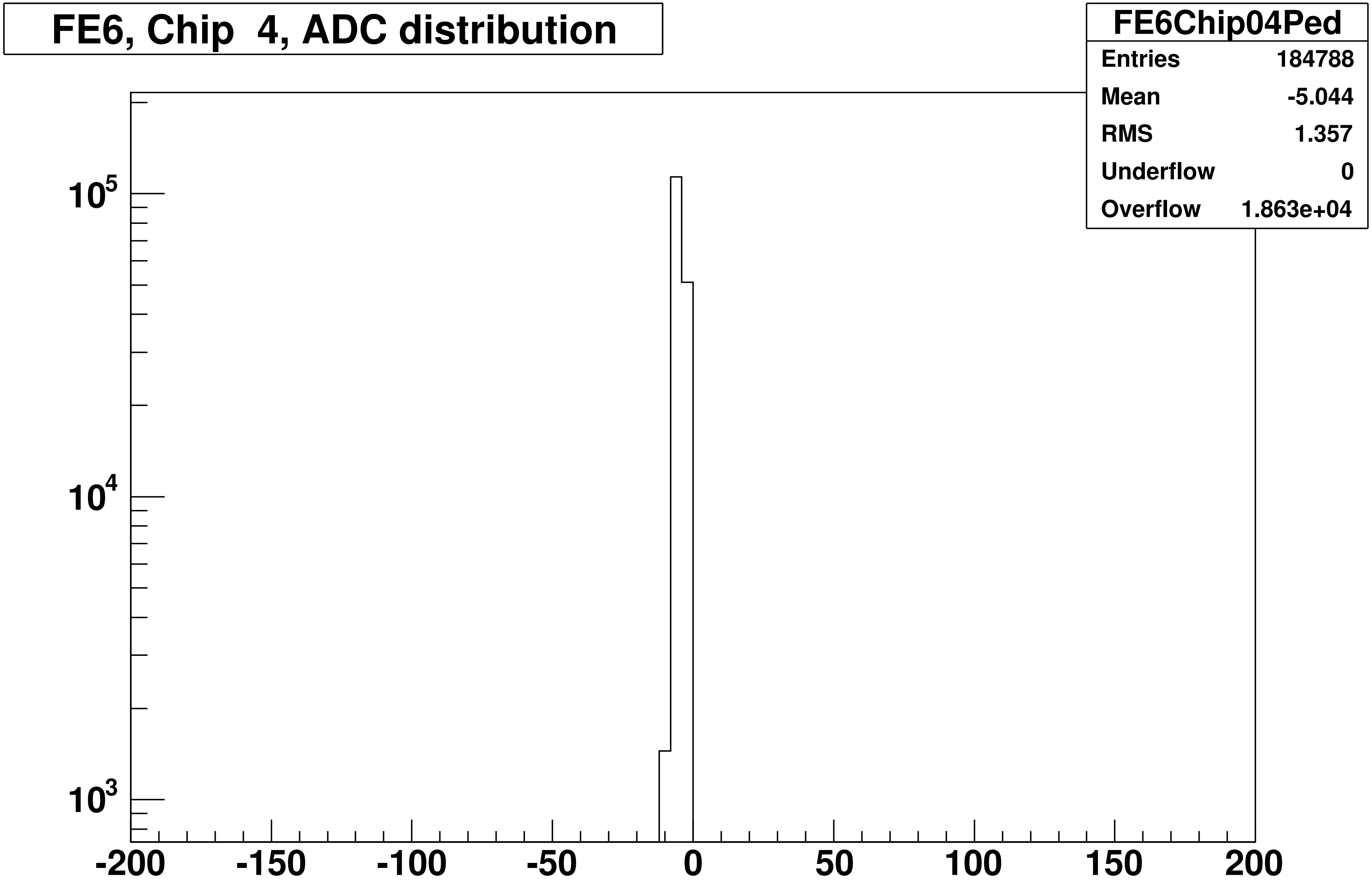
FE6, Chip 4, ADC distribution
FE6Chip04Ped
Entries 184788
Mean -5.044
RMS 1.357
Underflow 0
Overflow 1.863e+04
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10^4
10^3
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150
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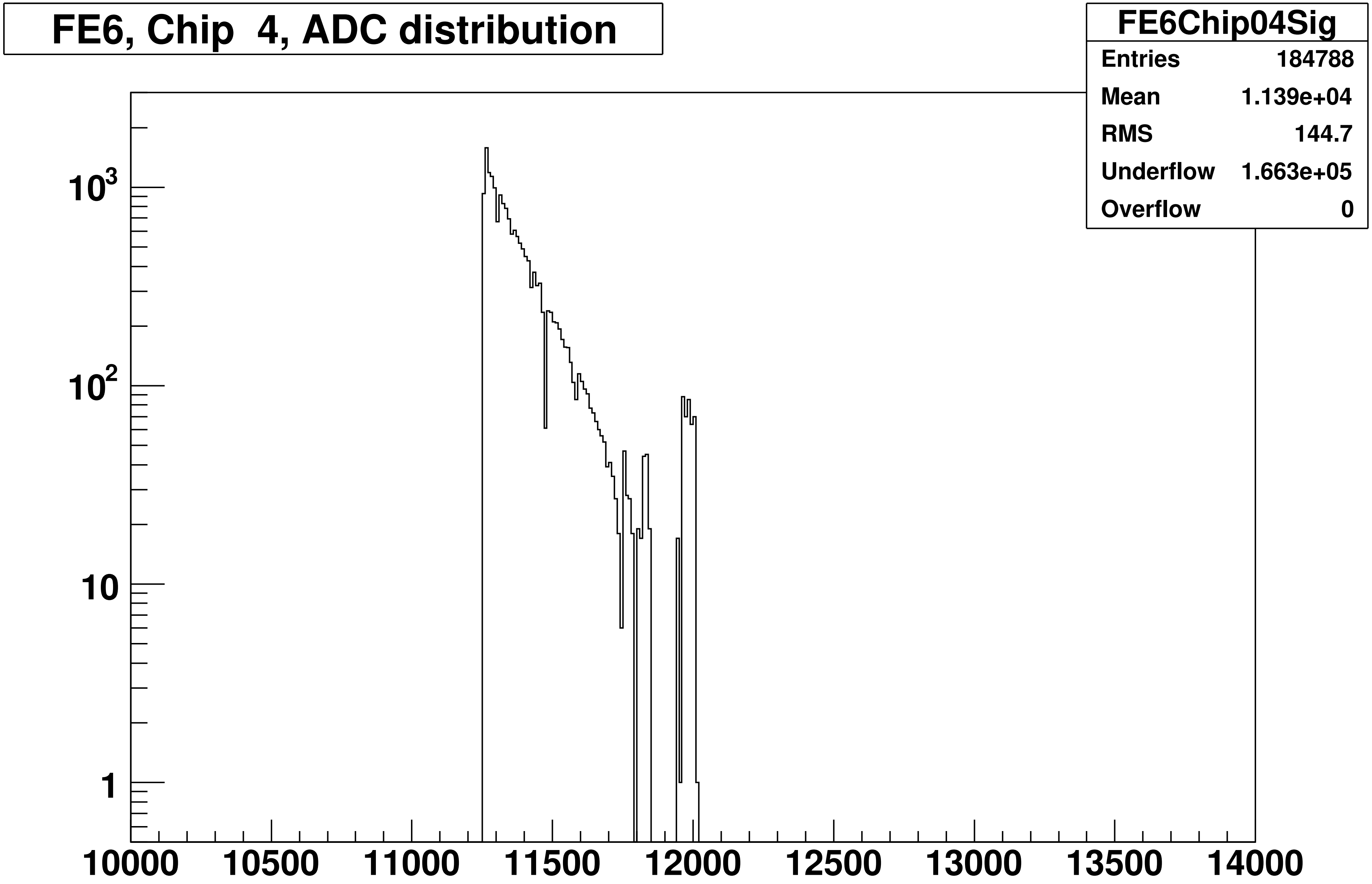
FE6, Chip 4, ADC distribution
FE6Chip04Sig
Entries 184788
Mean 1.139e+04
RMS 144.7
Underflow 1.663e+05
Overflow 0
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10^2
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1
10000
10500
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11500
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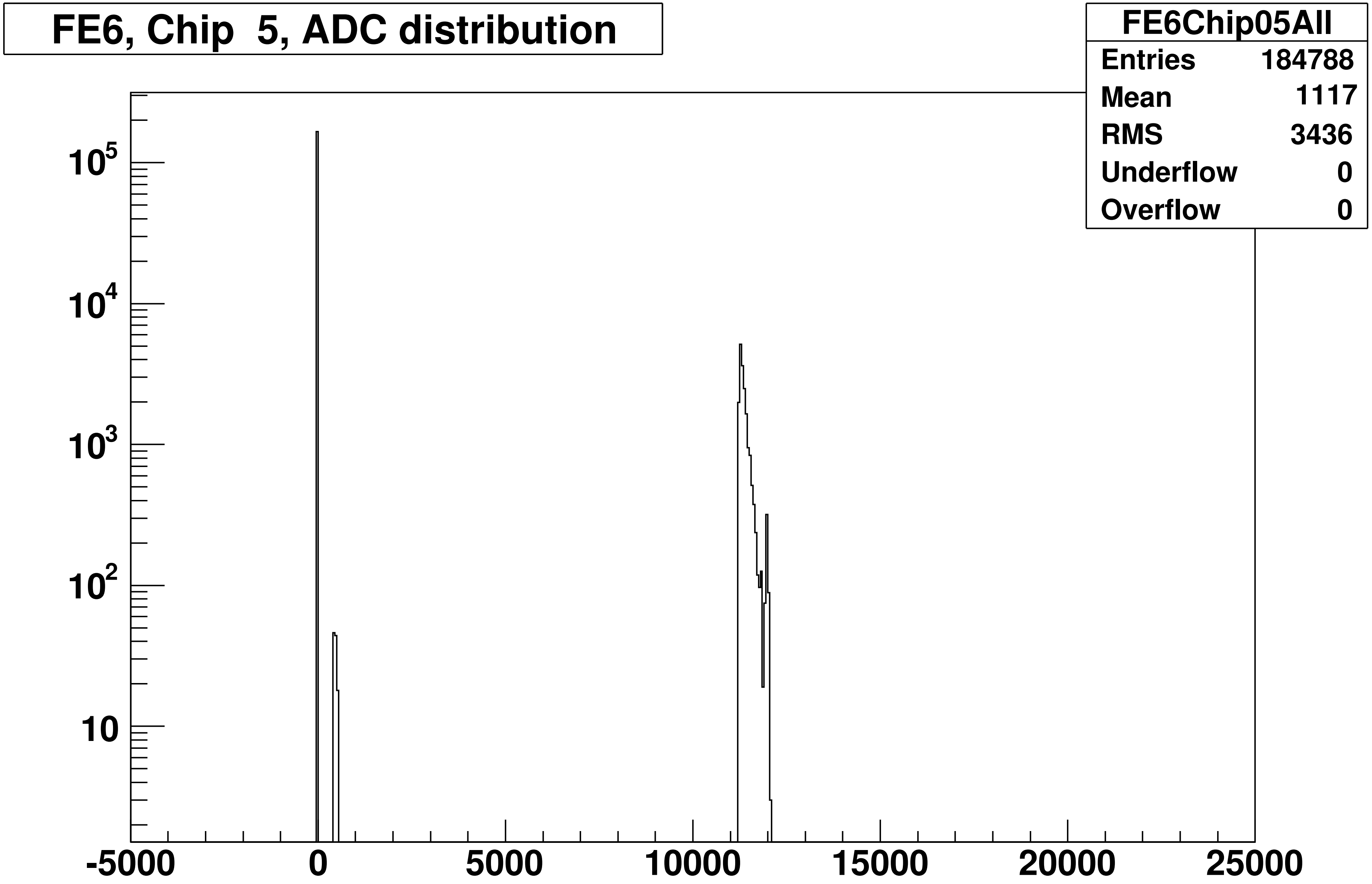
FE6, Chip 5, ADC distribution
FE6Chip05All
Entries 184788
Mean 1117
RMS 3436
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
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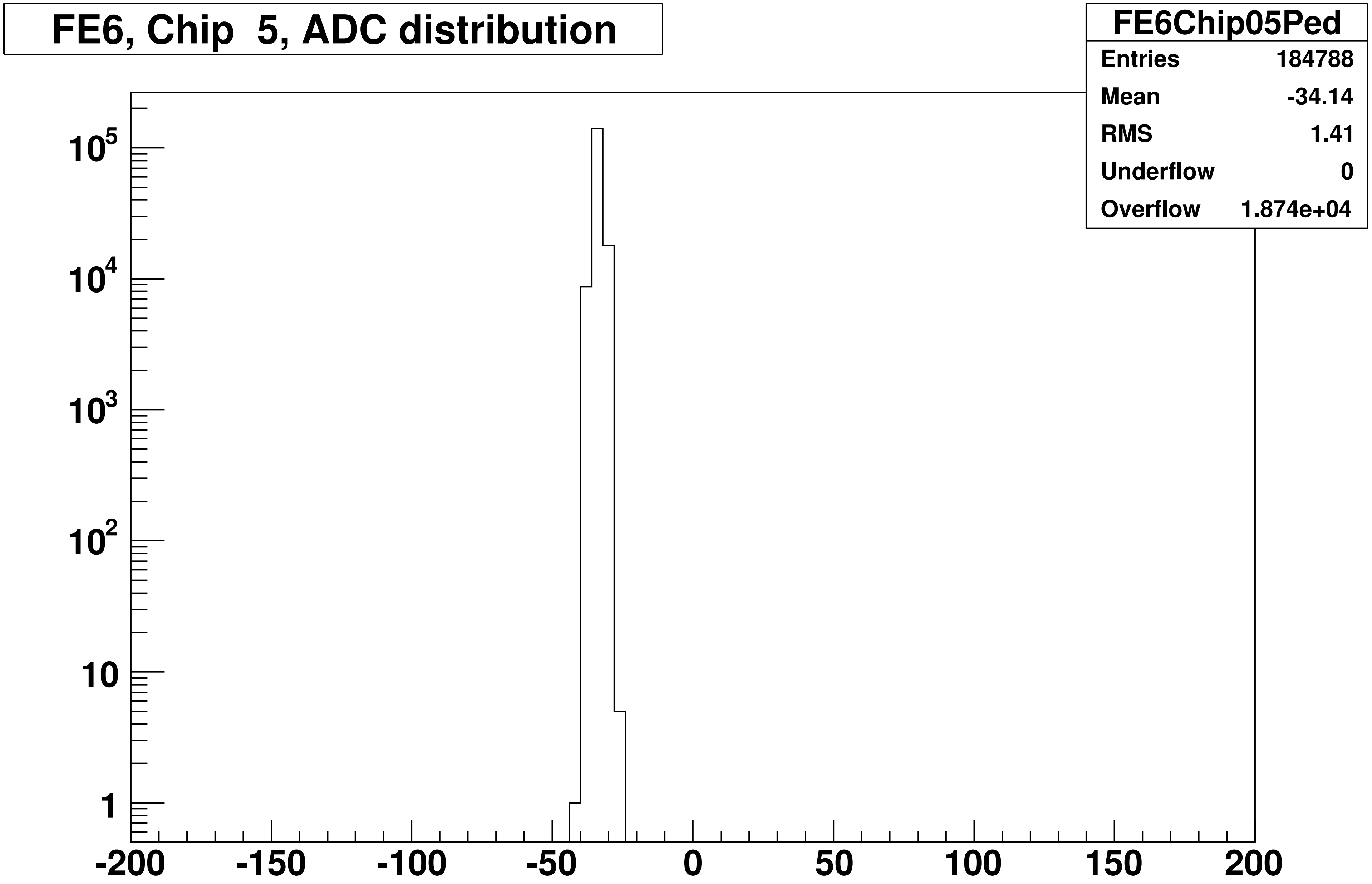
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 5, ADC distribution
FE6Chip05Ped
Entries 184788
Mean -34.14
RMS 1.41
Underflow 0
Overflow 1.874e+04
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10^3
10^2
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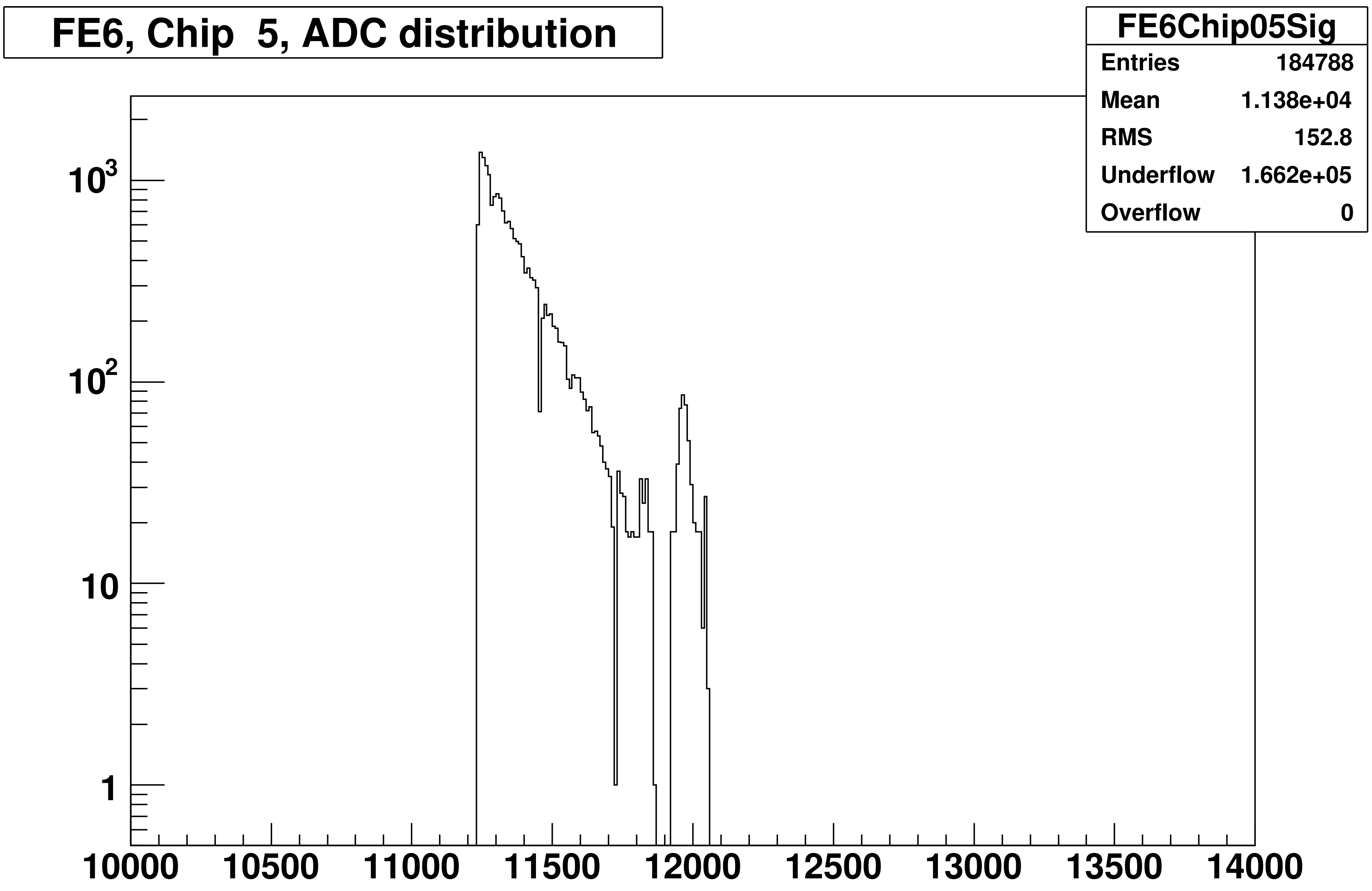
150
200


FE6, Chip 5, ADC distribution
FE6Chip05Sig
Entries 184788
Mean 1.138e+04
RMS 152.8
Underflow 1.662e+05
Overflow 0
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10^2
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1
10000
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11500
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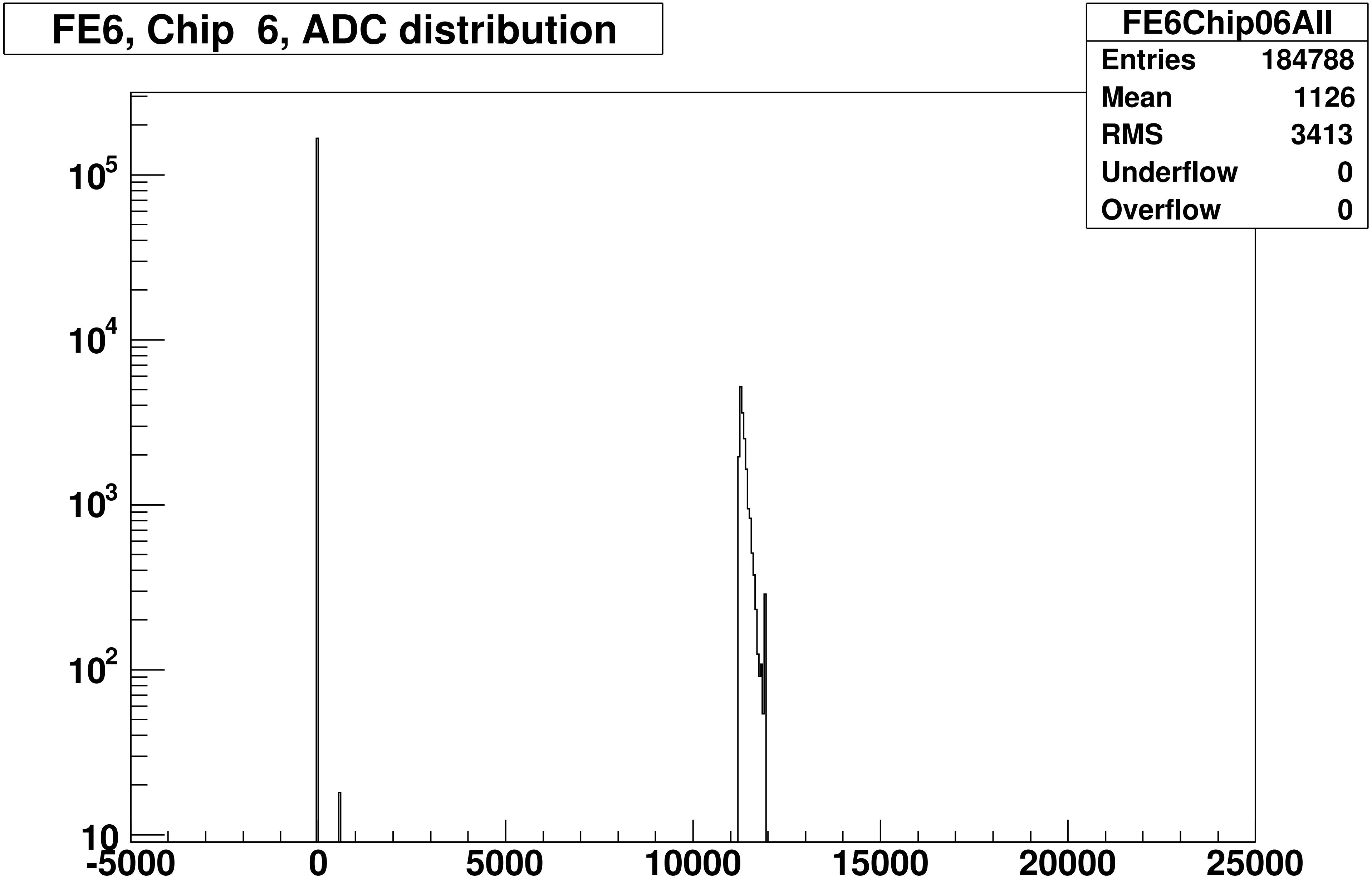
FE6, Chip 6, ADC distribution
FE6Chip06All
Entries 184788
Mean 1126
RMS 3413
Underflow 0
Overflow 0
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10^4
10^3
10^2
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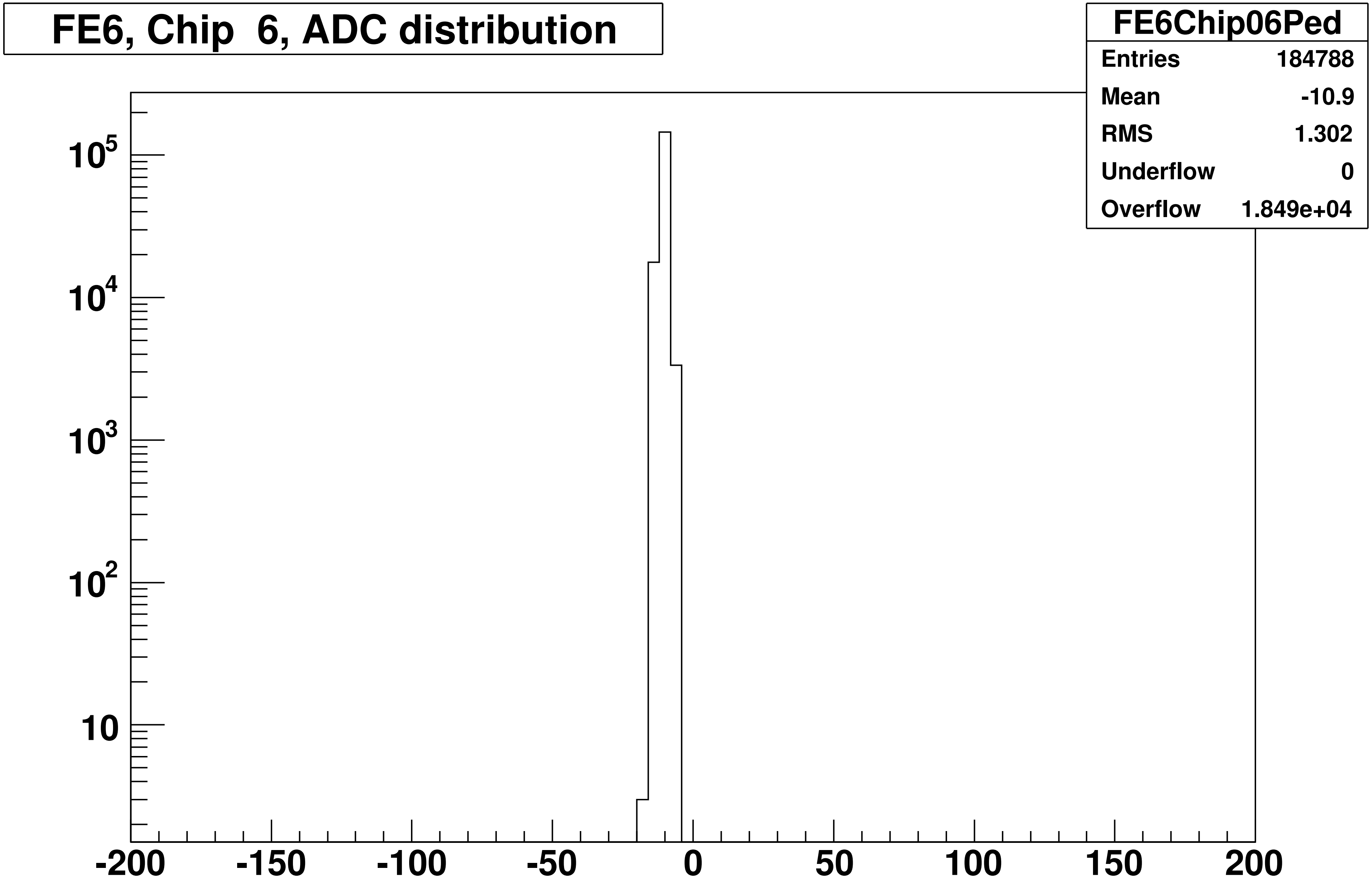
25000



FE6, Chip 6, ADC distribution
FE6Chip06Ped
Entries 184788
Mean -10.9
RMS 1.302
Underflow 0
Overflow 1.849e+04
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10^4
10^3
10^2
10
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-100
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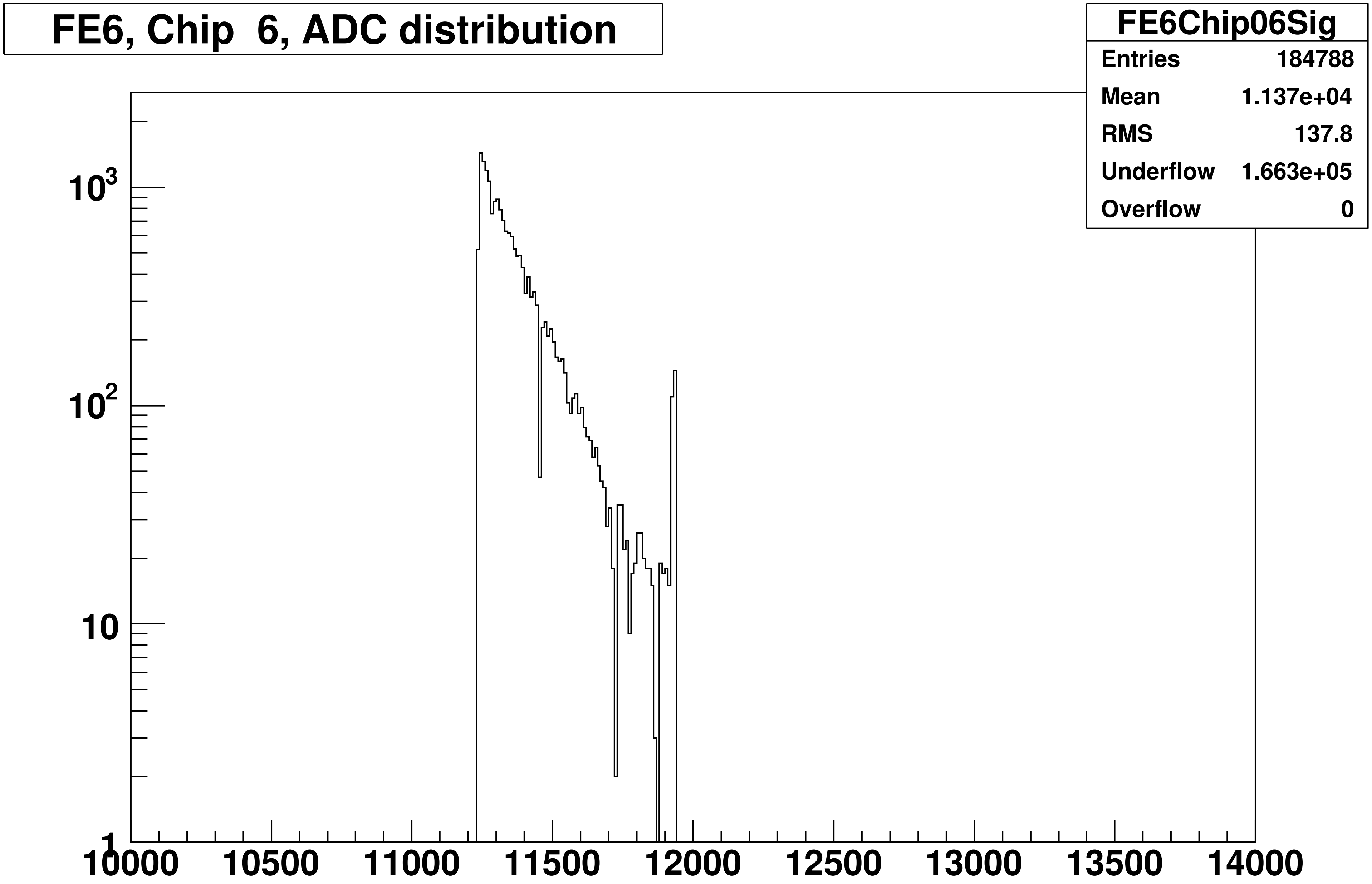
50
100
150
200


FE6, Chip 6, ADC distribution
FE6Chip06Sig
Entries 184788
Mean 1.137e+04
RMS 137.8
Underflow 1.663e+05
Overflow 0
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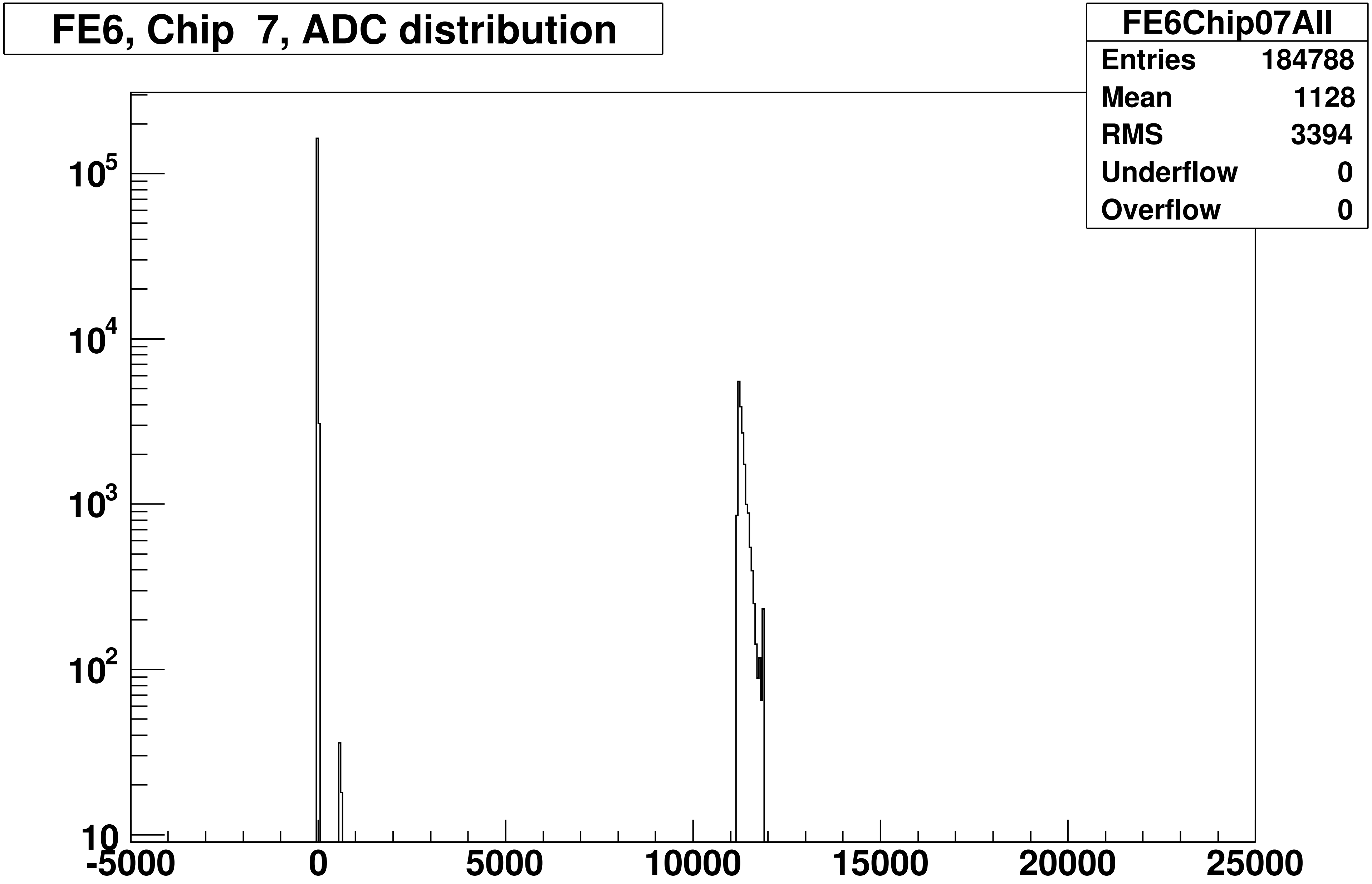
FE6, Chip 7, ADC distribution
FE6Chip07All
Entries 184788
Mean 1128
RMS 3394
Underflow 0
Overflow 0
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10^2
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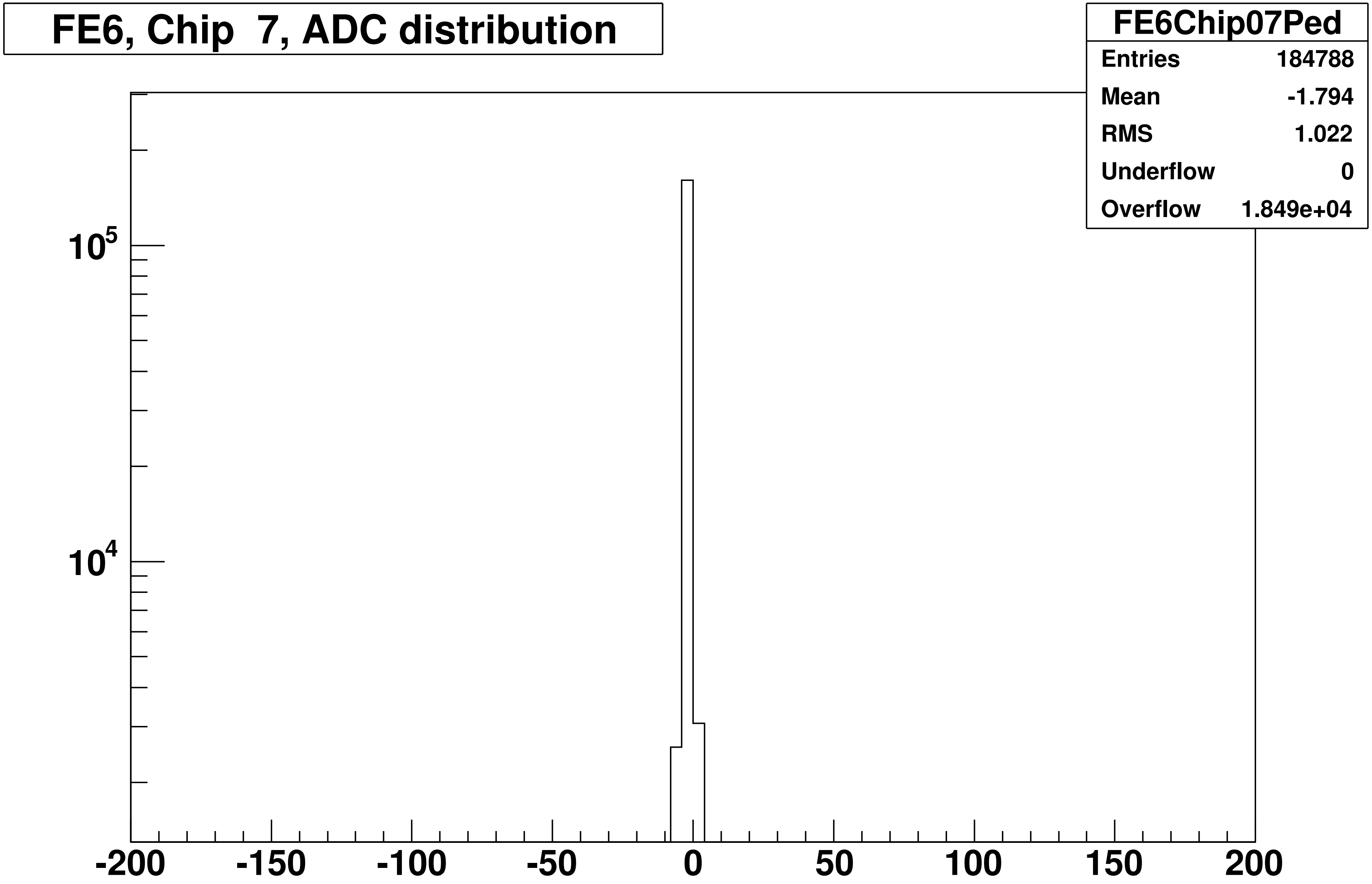
FE6, Chip 7, ADC distribution
FE6Chip07Ped
Entries 184788
Mean -1.794
RMS 1.022
Underflow 0
Overflow 1.849e+04
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10^4
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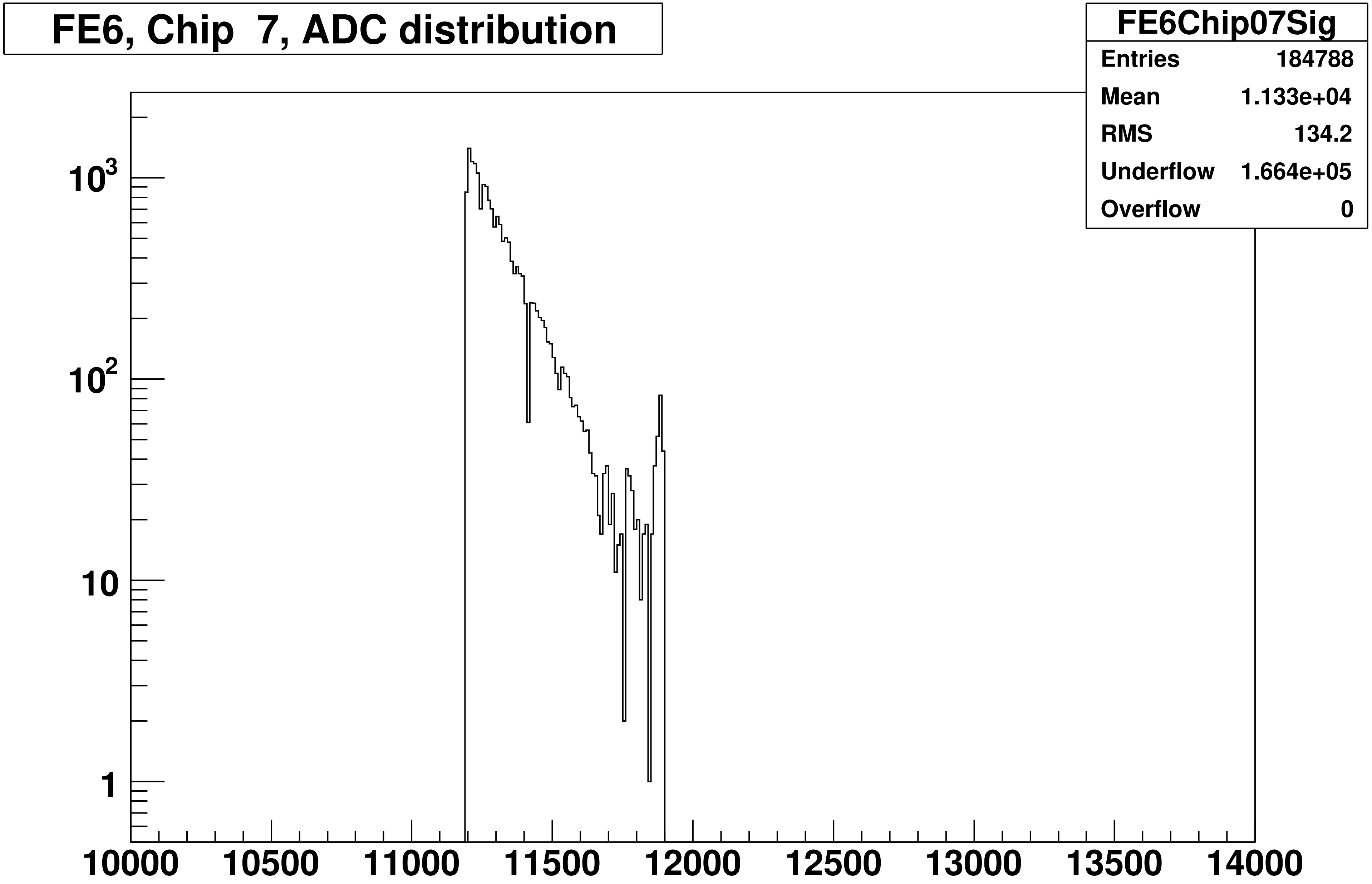
150
200


FE6, Chip 7, ADC distribution
FE6Chip07Sig
Entries 184788
Mean 1.133e+04
RMS 134.2
Underflow 1.664e+05
Overflow 0
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10^2
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10000
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11500
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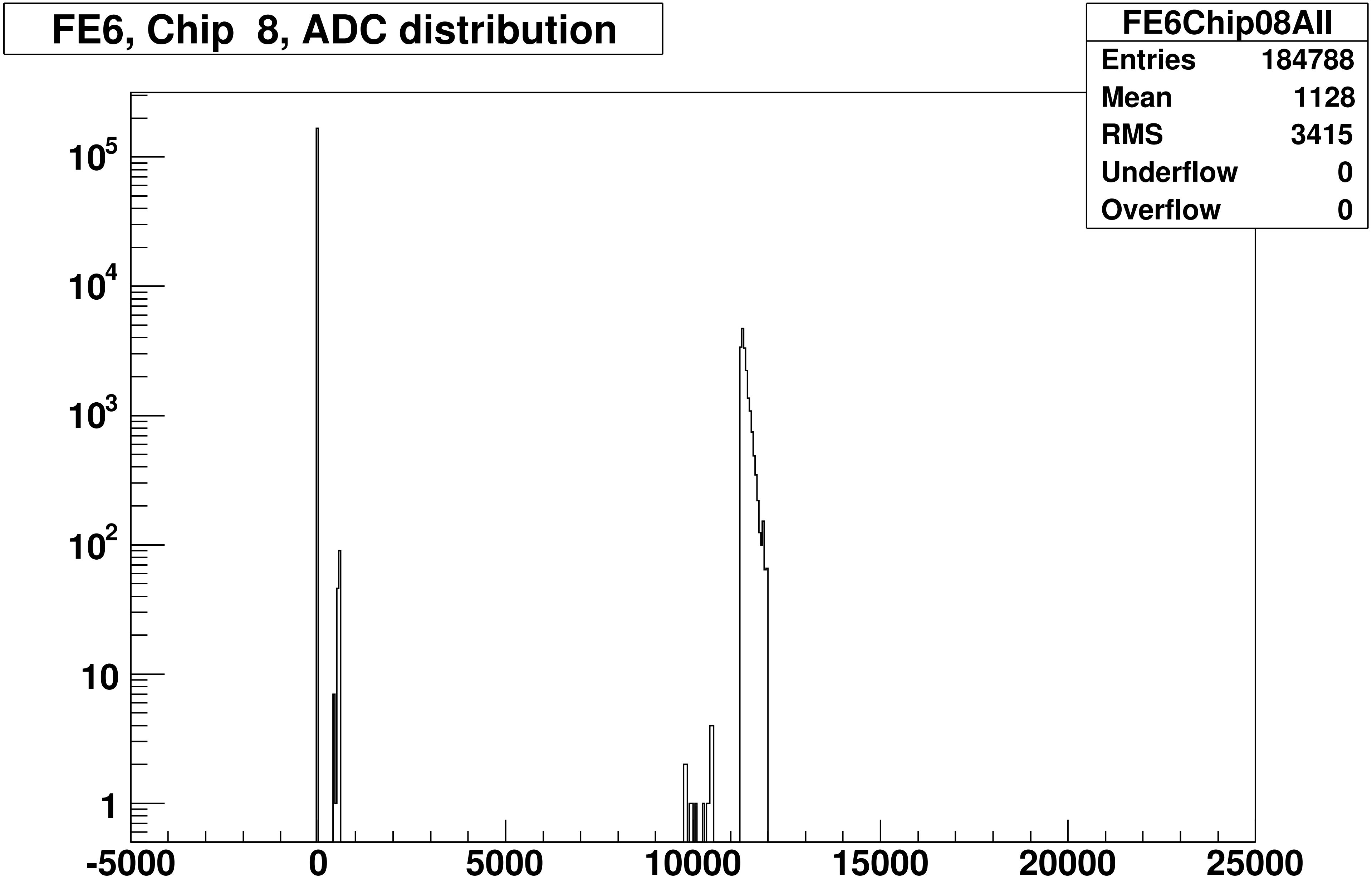
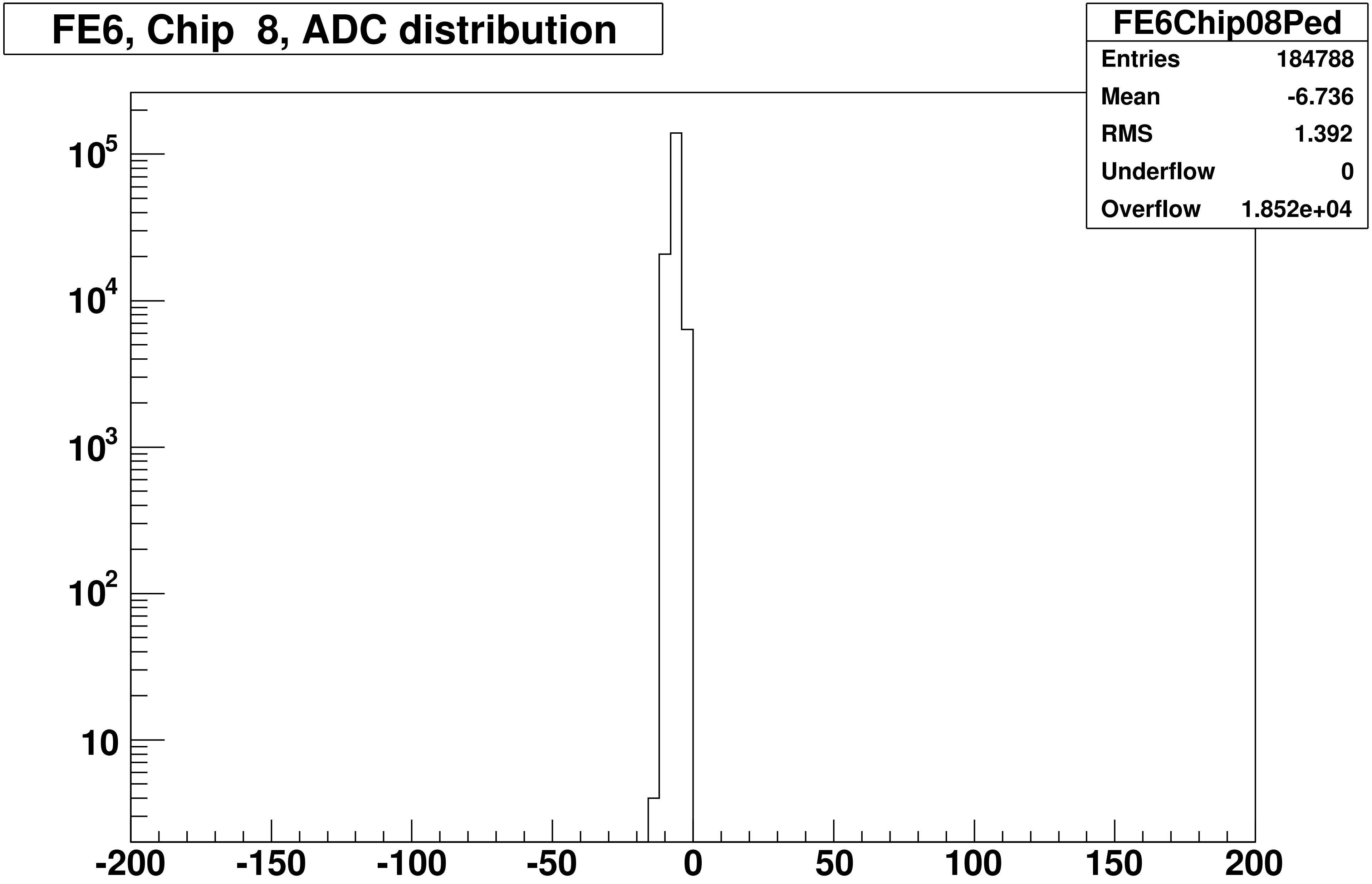


FE6, Chip 8, ADC distribution
FE6Chip08All
Entries 184788
Mean 1128
RMS 3415
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 8, ADC distribution
FE6Chip08Ped
Entries 184788
Mean -6.736
RMS 1.392
Underflow 0
Overflow 1.852e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
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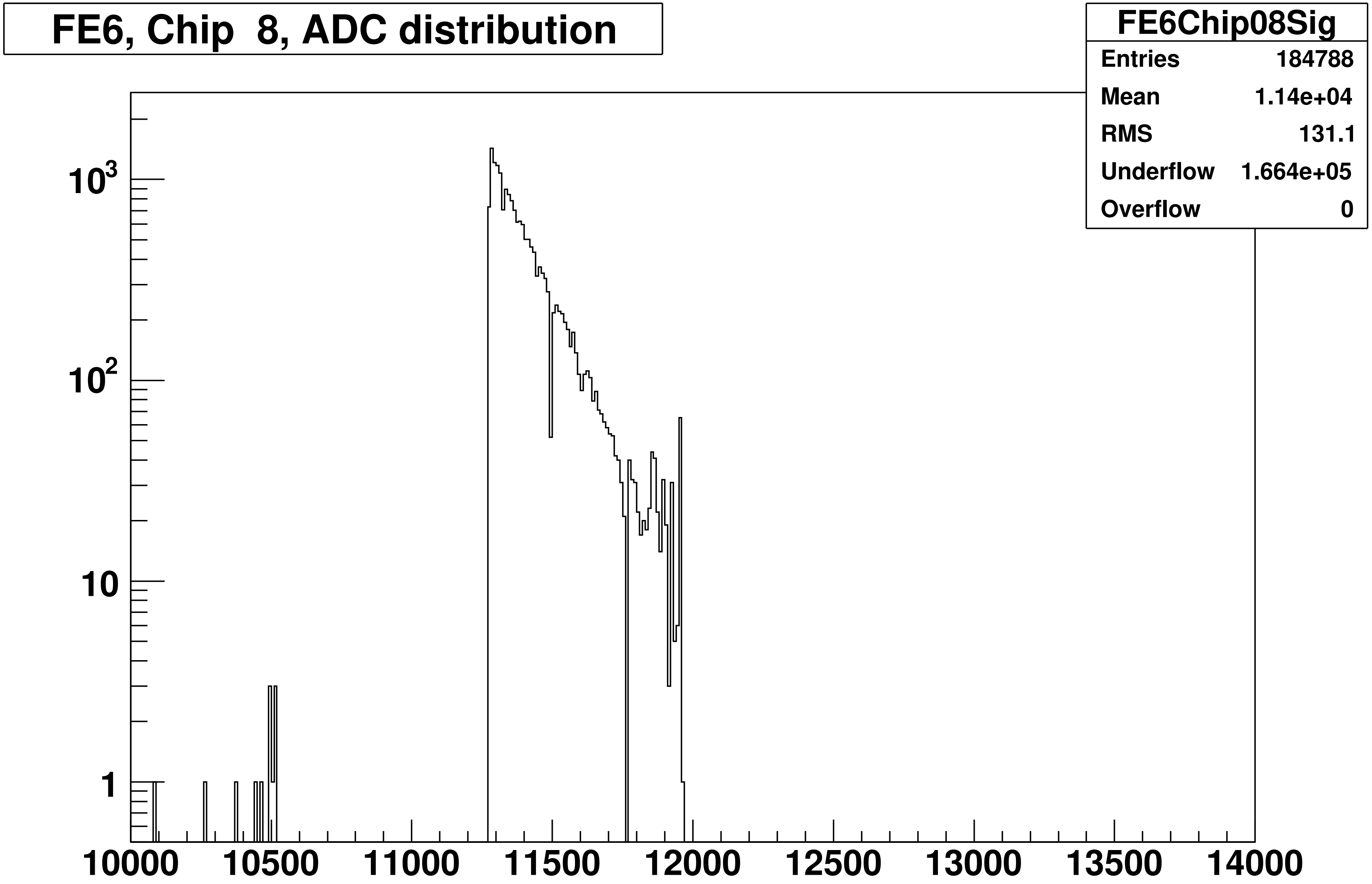
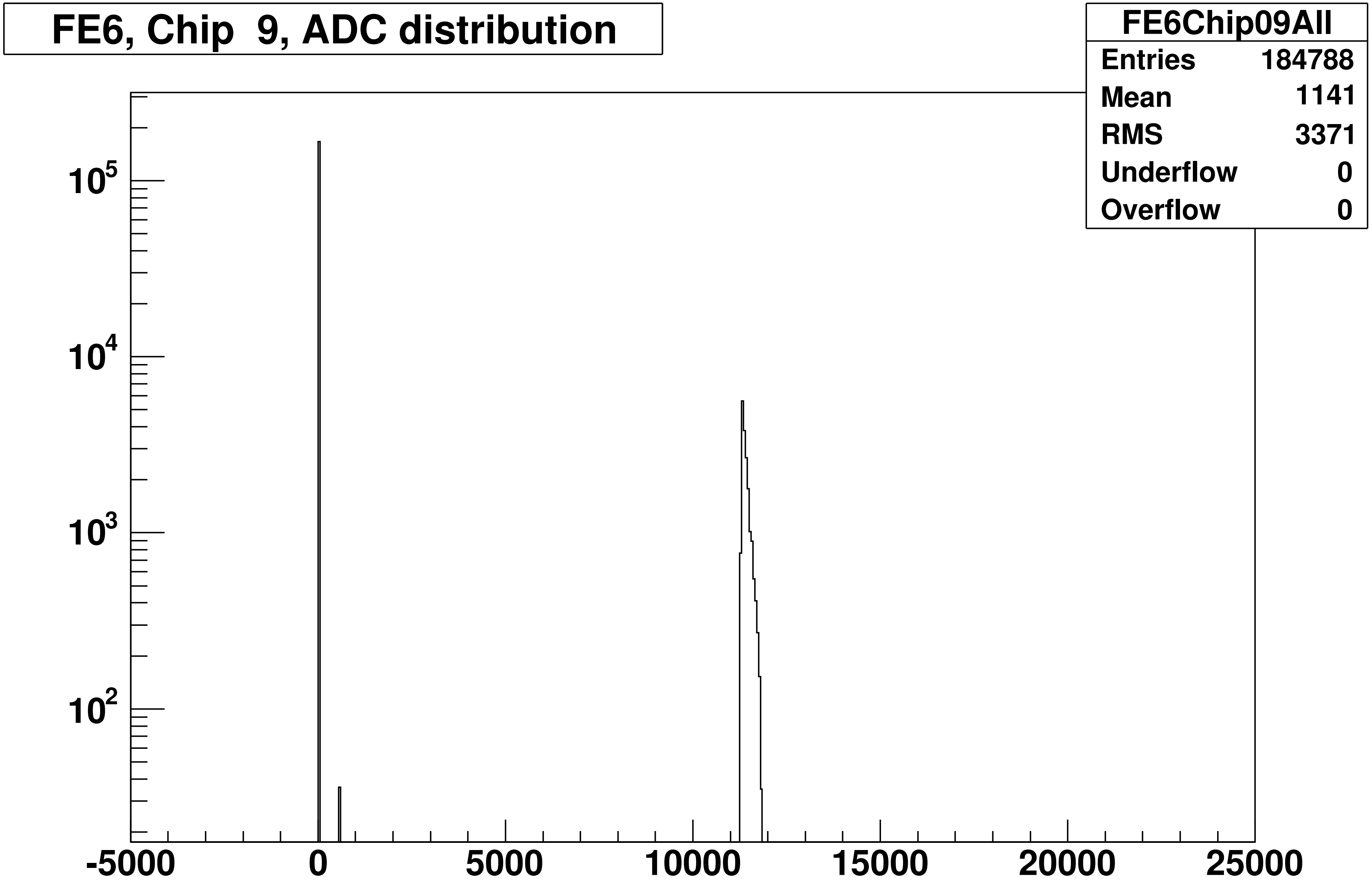
100
150
200



FE6, Chip 8, ADC distribution
FE6Chip08Sig
Entries 184788
Mean 1.14e+04
RMS 131.1
Underflow 1.664e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE6, Chip 9, ADC distribution
FE6Chip09All
Entries 184788
Mean 1141
RMS 3371
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
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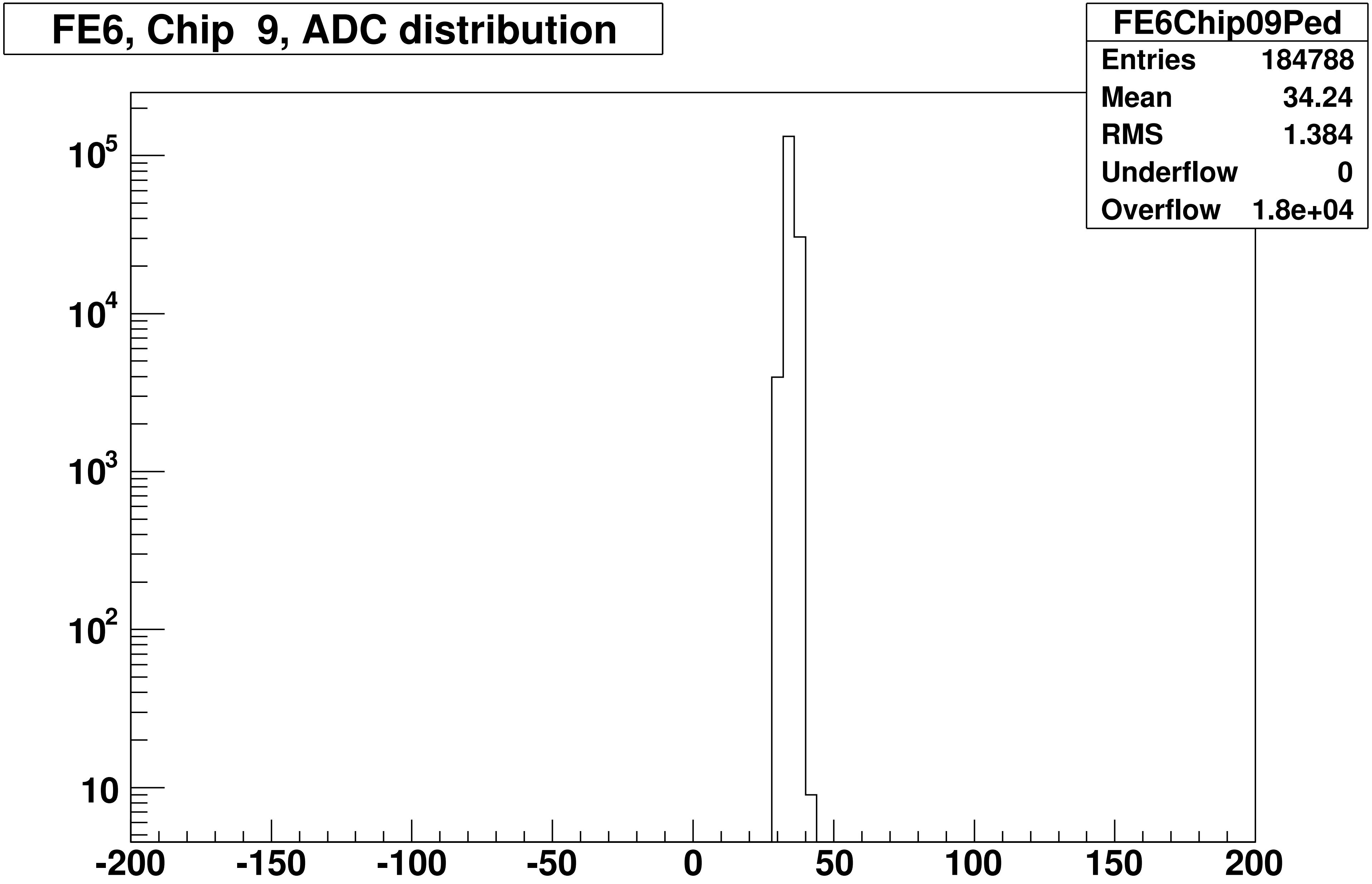
FE6, Chip 9, ADC distribution
FE6Chip09Ped
Entries 184788
Mean 34.24
RMS 1.384
Underflow 0
Overflow 1.8e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
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100
150
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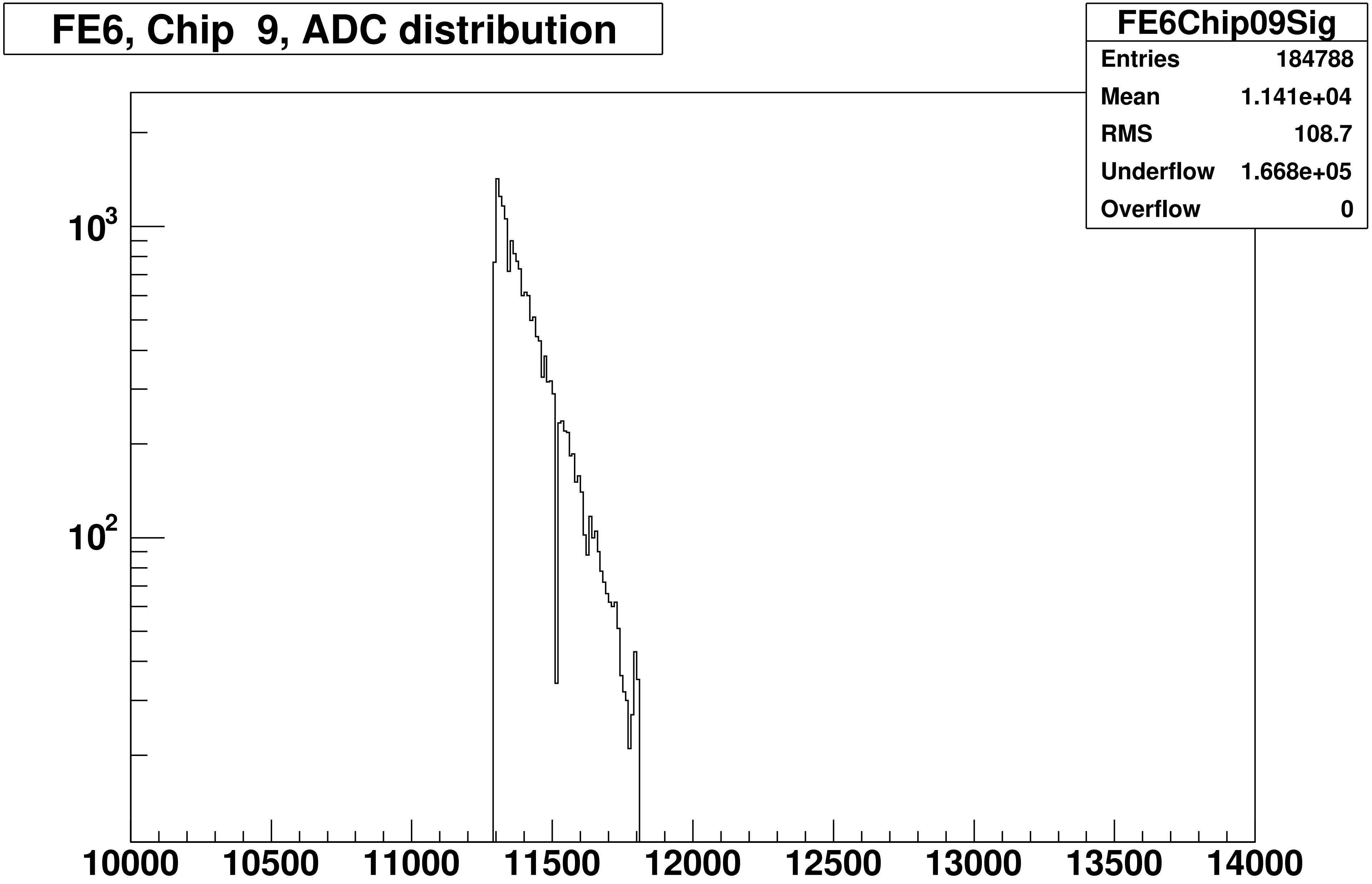
FE6, Chip 9, ADC distribution
FE6Chip09Sig
Entries 184788
Mean 1.141e+04
RMS 108.7
Underflow 1.668e+05
Overflow 0
10^3
10^2
10000
10500
11000
11500
12000
12500
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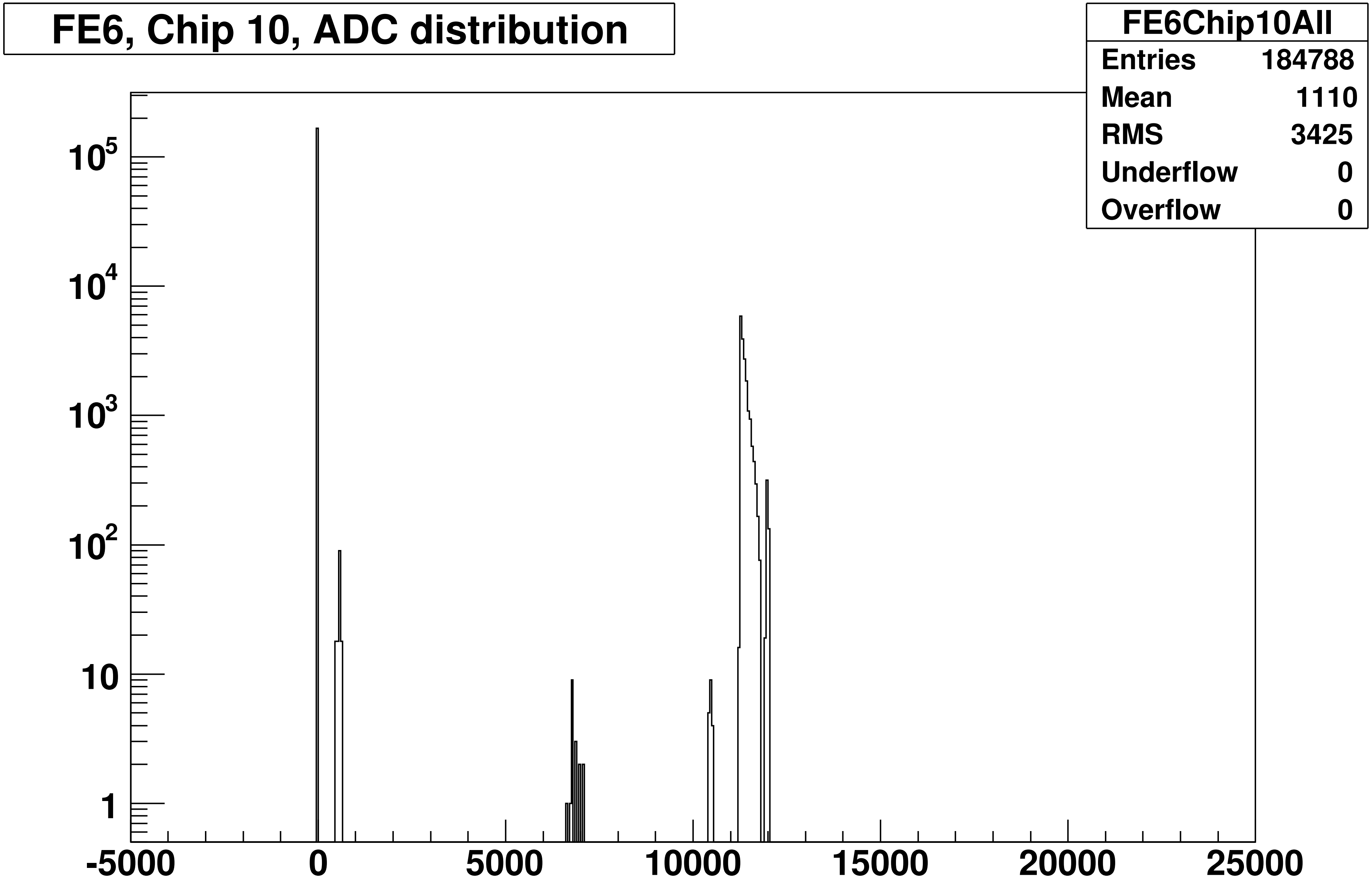
13500
14000


FE6, Chip 10, ADC distribution
FE6Chip10All
Entries 184788
Mean 1110
RMS 3425
Underflow 0
Overflow 0
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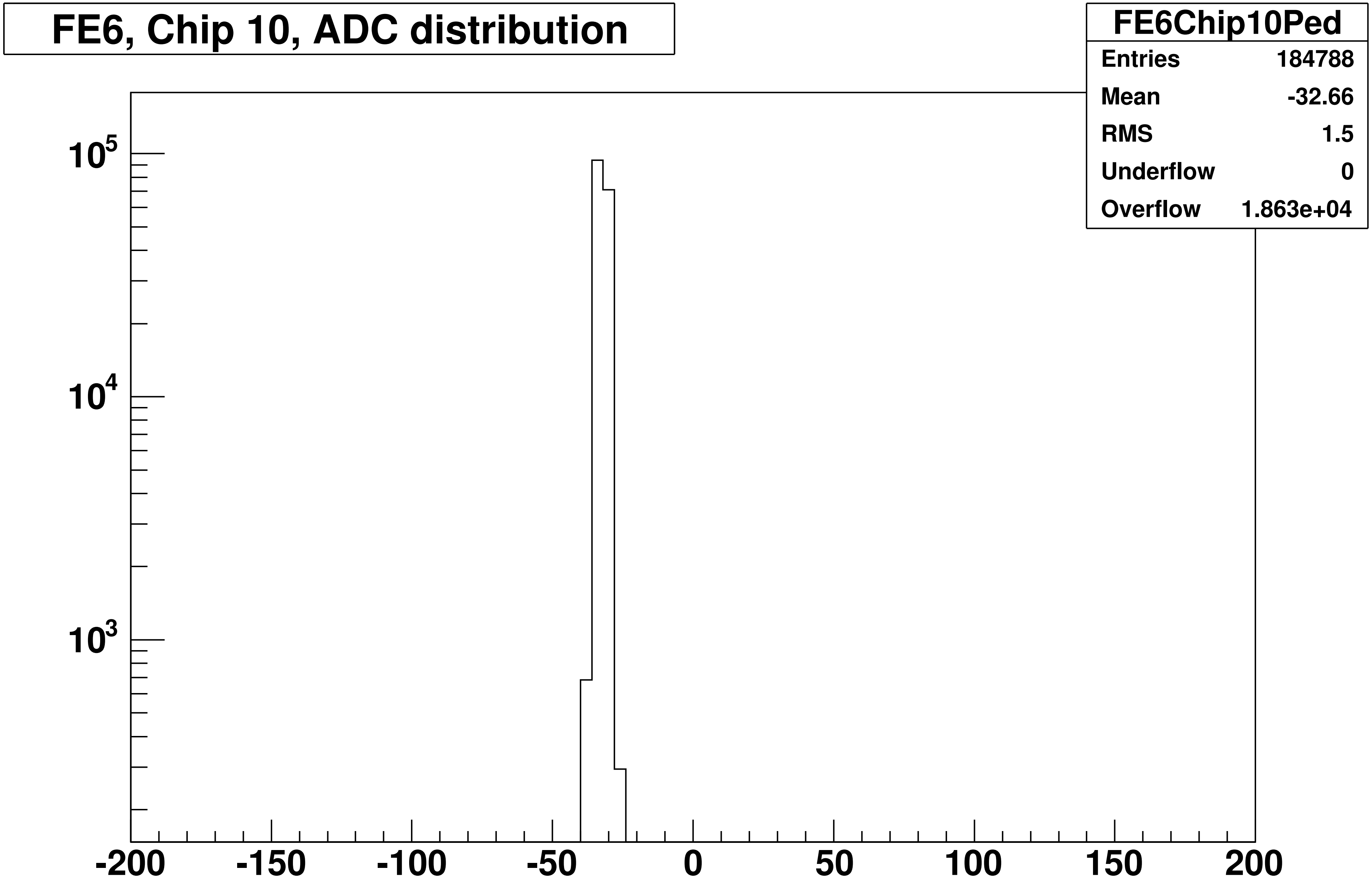
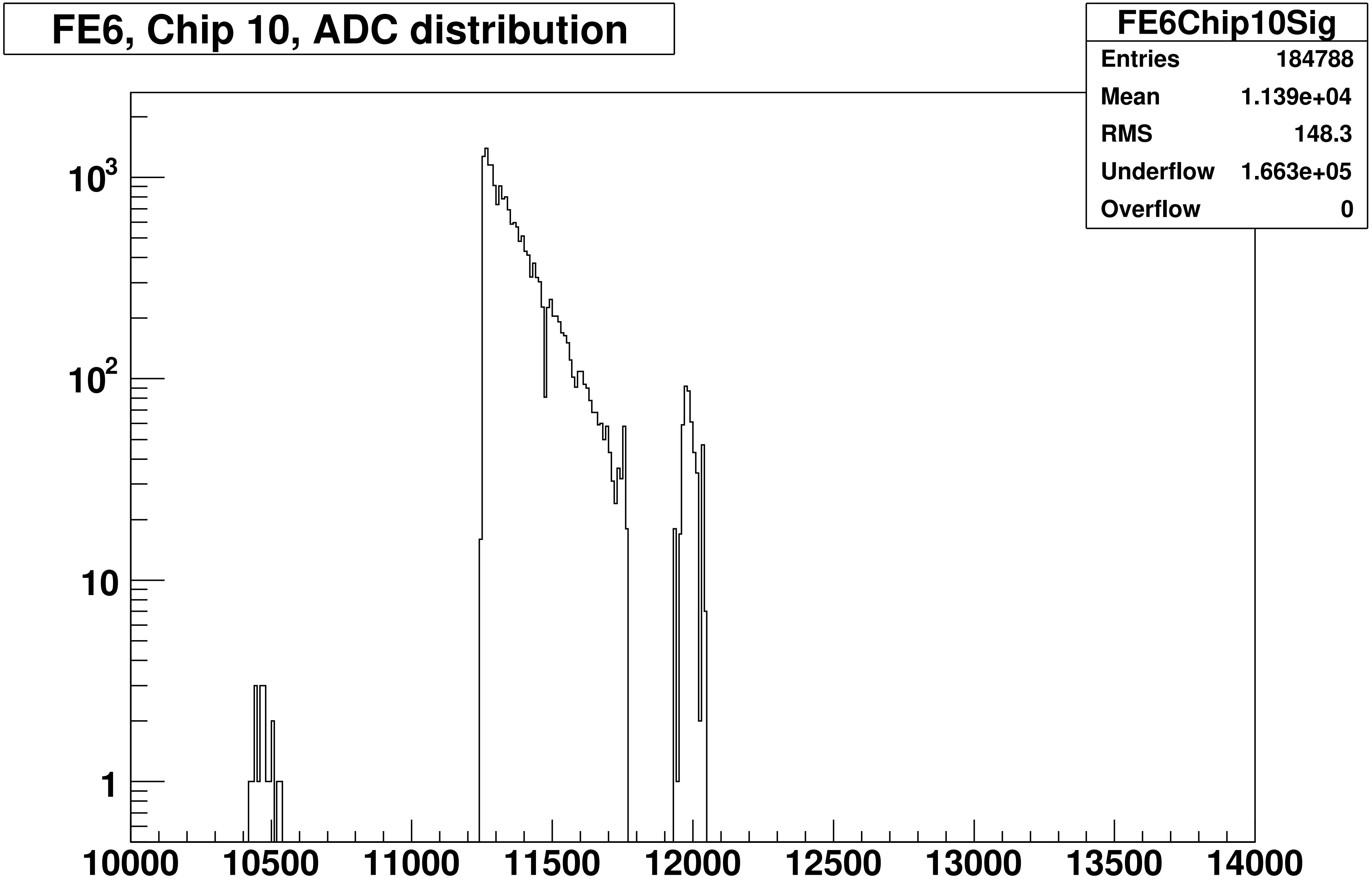
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 10, ADC distribution
FE6Chip10Ped
Entries 184788
Mean -32.66
RMS 1.5
Underflow 0
Overflow 1.863e+04
10^5
10^4
10^3
-200
-150
-100
-50
0
50
100
150
200



FE6, Chip 10, ADC distribution
FE6Chip10Sig
Entries 184788
Mean 1.139e+04
RMS 148.3
Underflow 1.663e+05
Overflow 0
10^3
10^2
10
1
10000
10500
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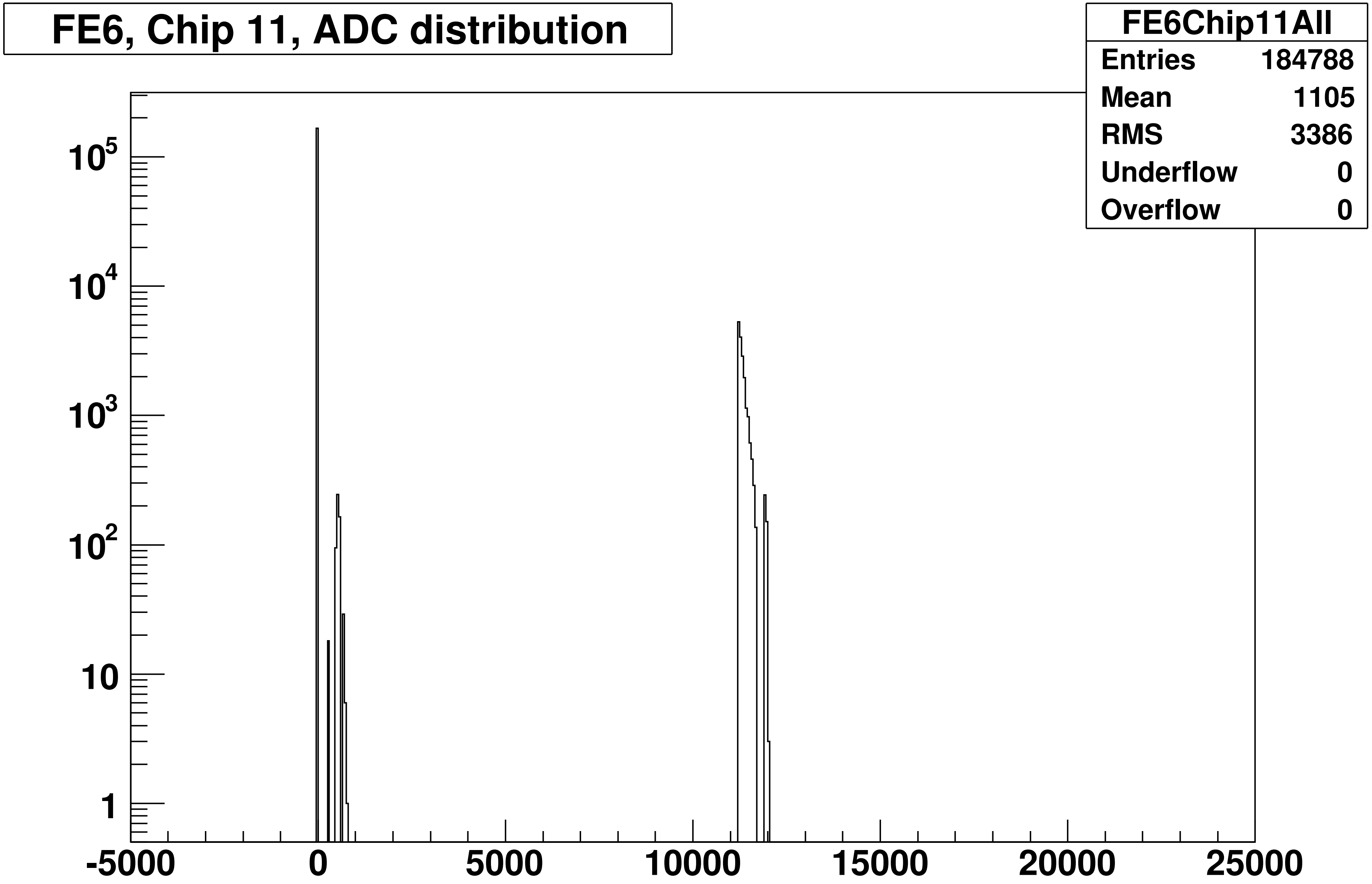
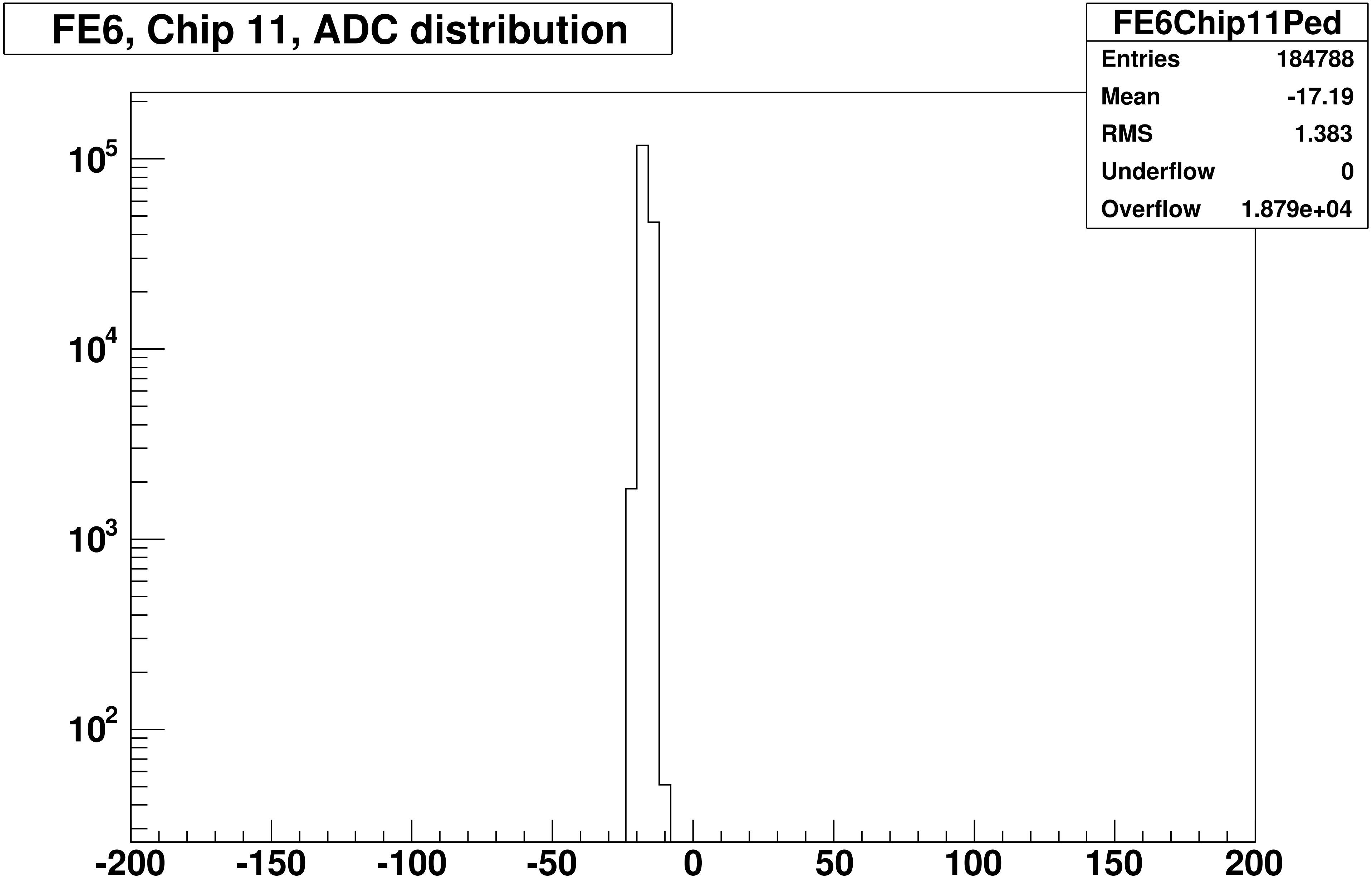
11500
12000
12500
13000
13500
14000



FE6, Chip 11, ADC distribution
FE6Chip11All
Entries 184788
Mean 1105
RMS 3386
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE6, Chip 11, ADC distribution
FE6Chip11Ped
Entries 184788
Mean -17.19
RMS 1.383
Underflow 0
Overflow 1.879e+04
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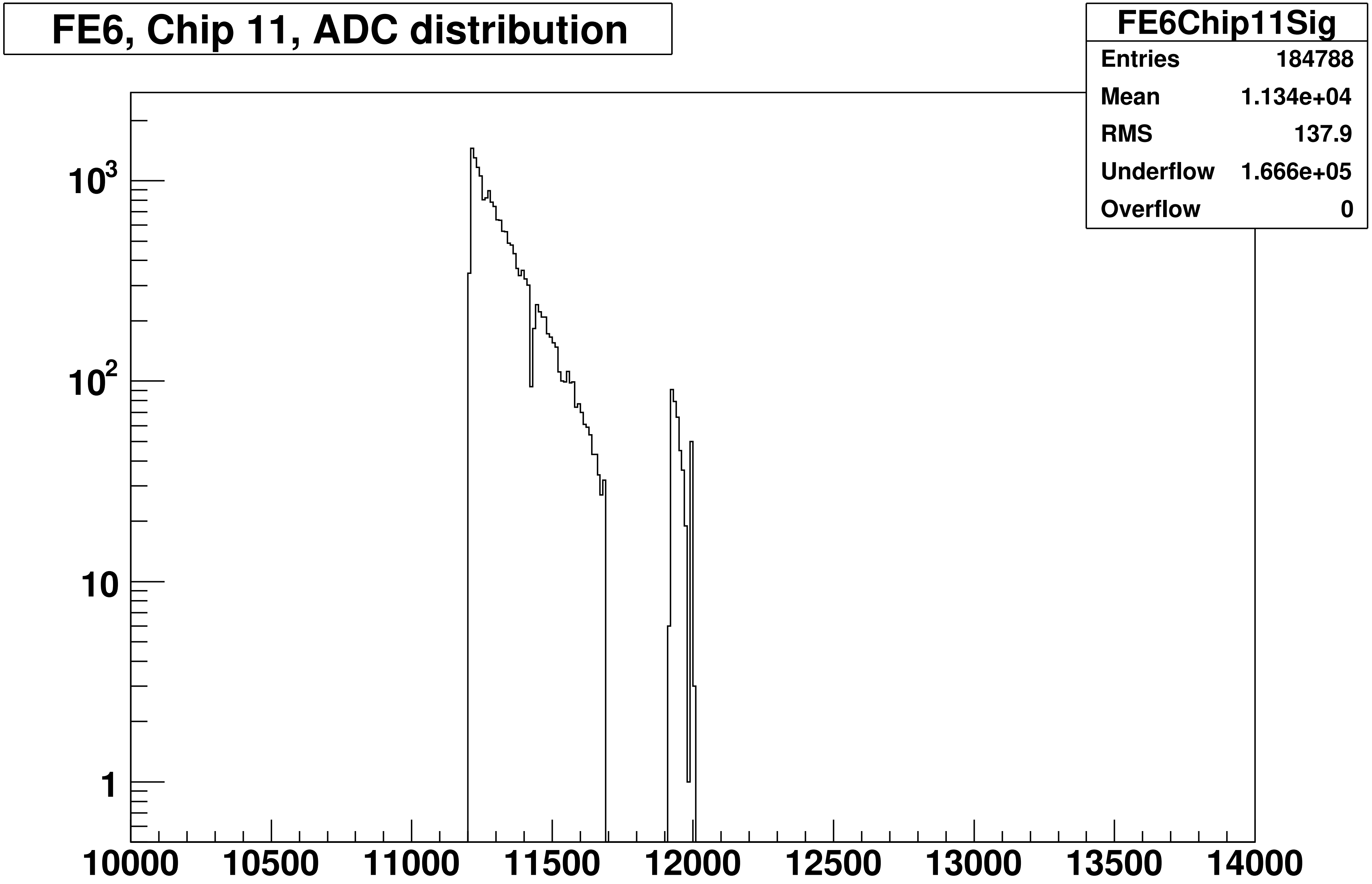
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE6, Chip 11, ADC distribution
FE6Chip11Sig
Entries 184788
Mean 1.134e+04
RMS 137.9
Underflow 1.666e+05
Overflow 0
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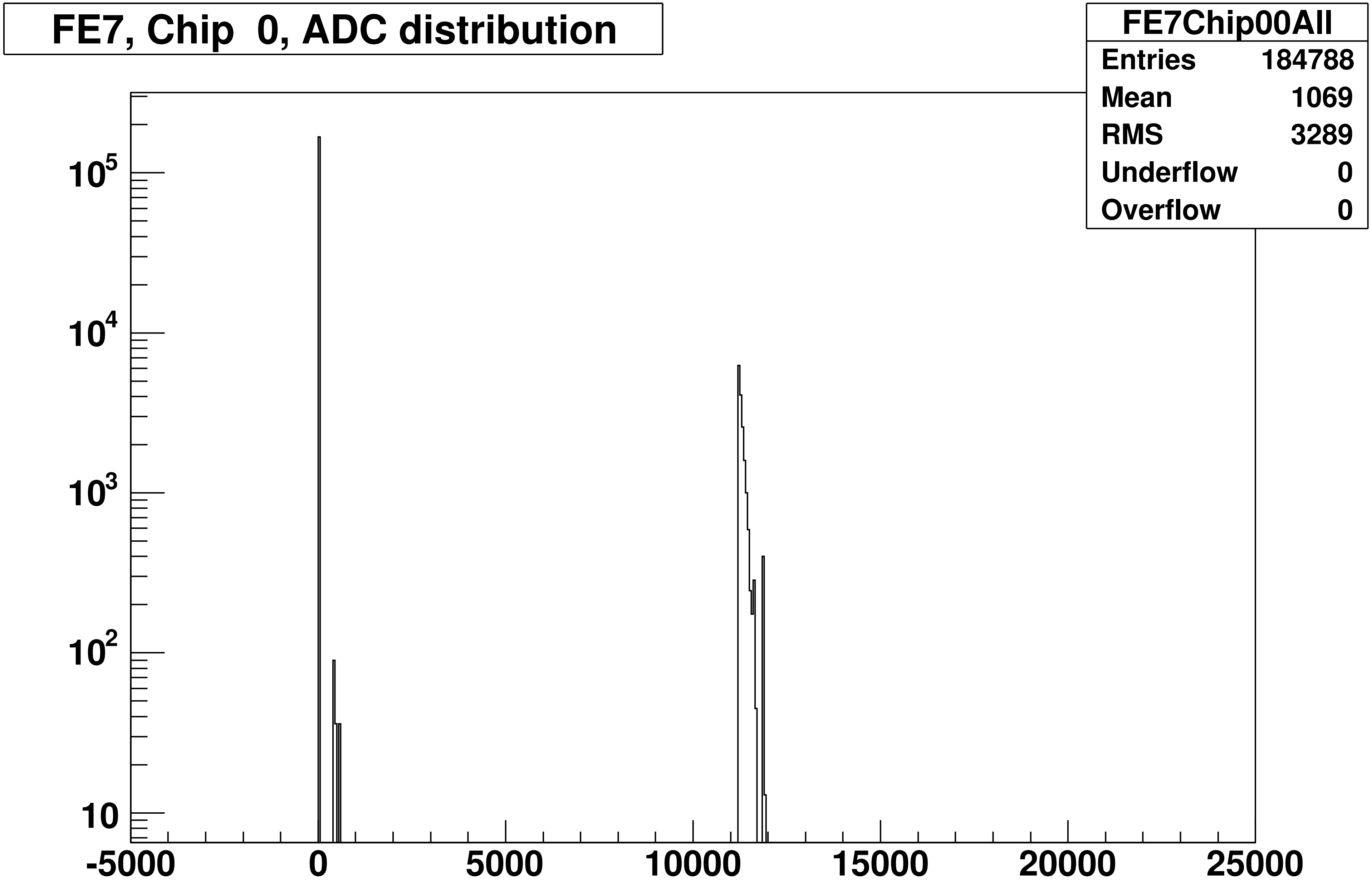
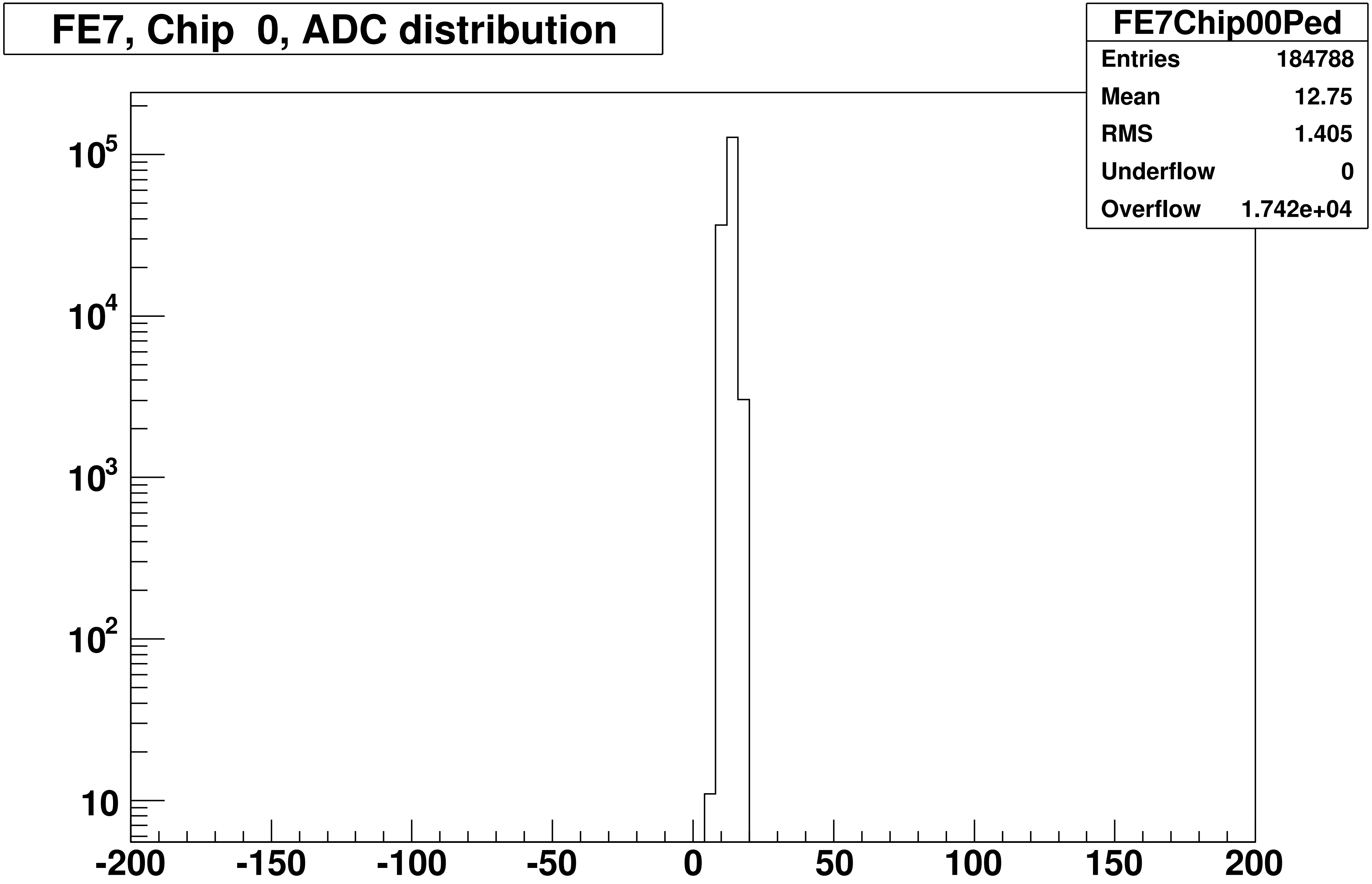
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 0, ADC distribution
FE7Chip00All
Entries 184788
Mean 1069
RMS 3289
Underflow 0
Overflow 0
10
10^2
10^3
10^4
10^5
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 0, ADC distribution
FE7Chip00Ped
Entries 184788
Mean 12.75
RMS 1.405
Underflow 0
Overflow 1.742e+04
10
10^2
10^3
10^4
10^5
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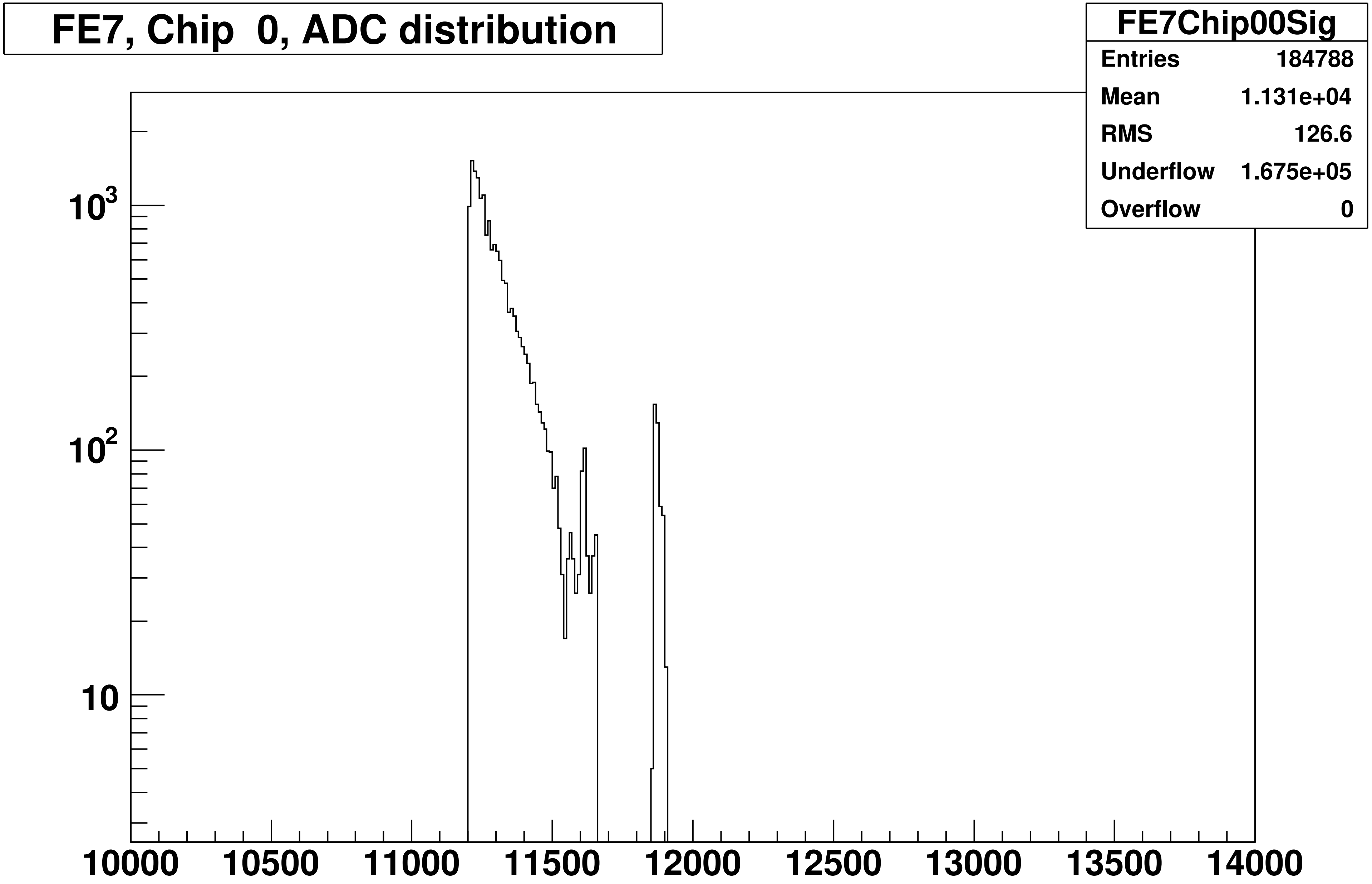
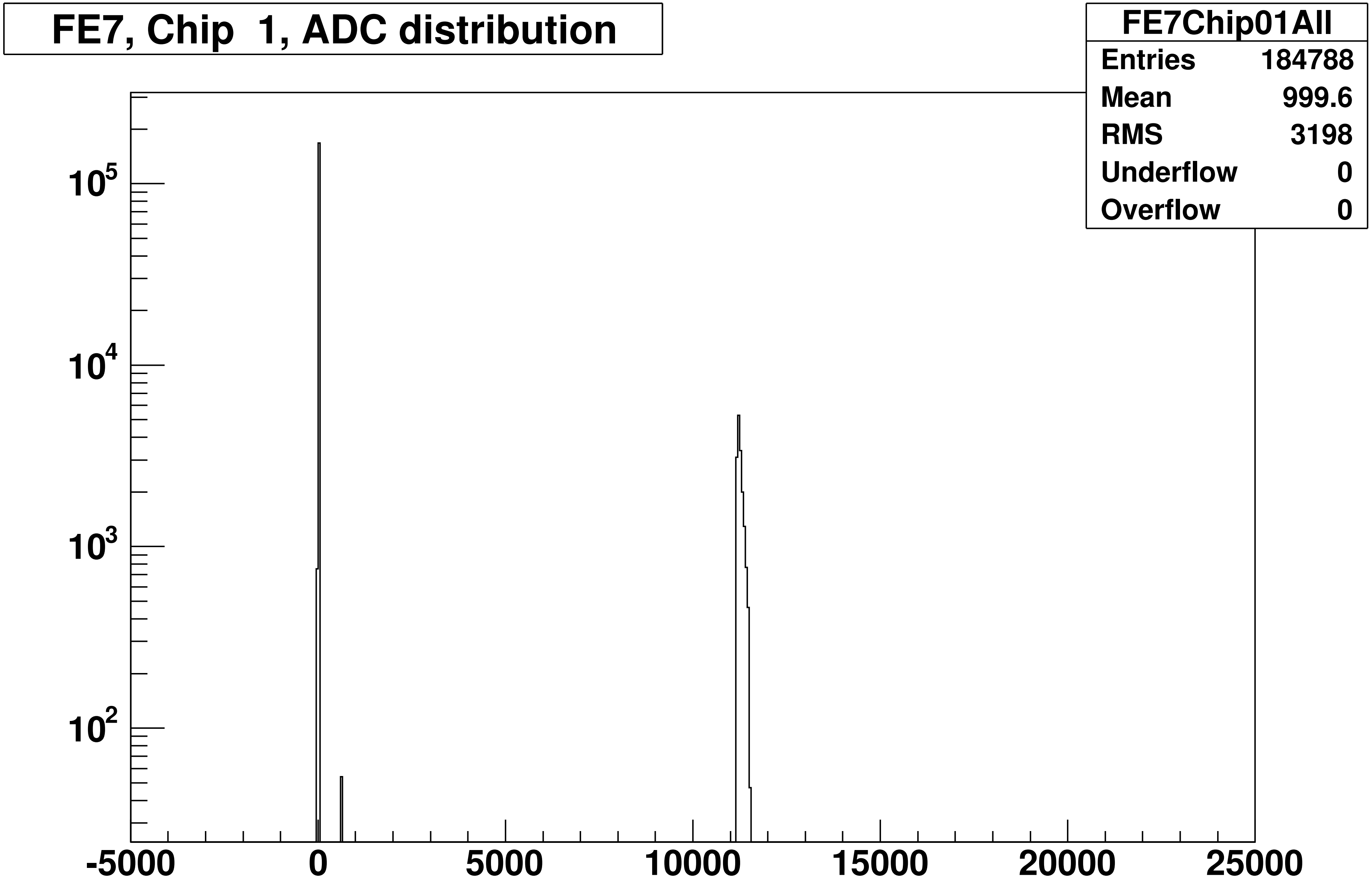
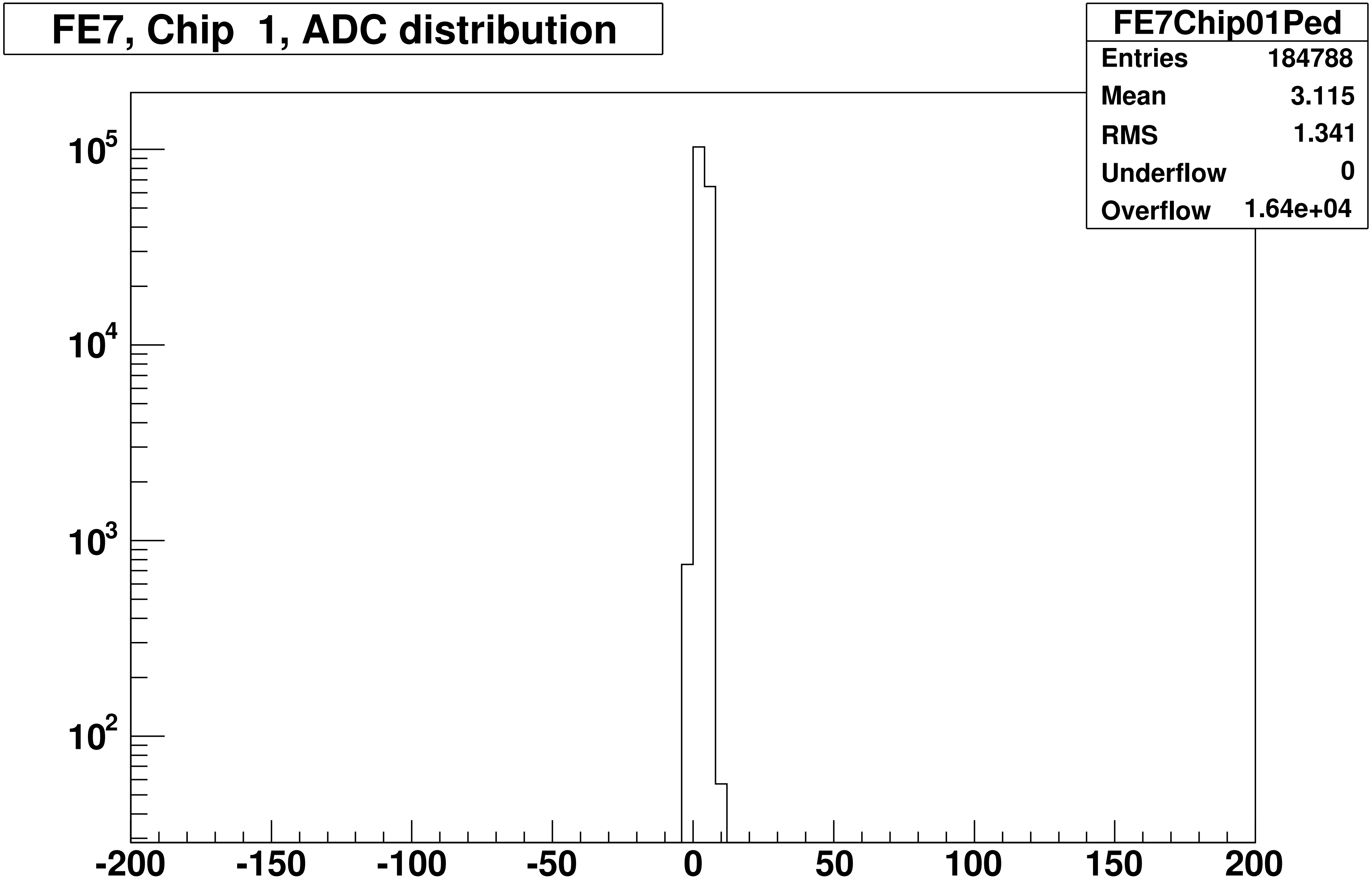
-150
-100
-50
0
50
100
150
200



FE7, Chip 0, ADC distribution
FE7Chip00Sig
Entries 184788
Mean 1.131e+04
RMS 126.6
Underflow 1.675e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 1, ADC distribution
FE7Chip01All
Entries 184788
Mean 999.6
RMS 3198
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 1, ADC distribution
FE7Chip01Ped
Entries 184788
Mean 3.115
RMS 1.341
Underflow 0
Overflow 1.64e+04
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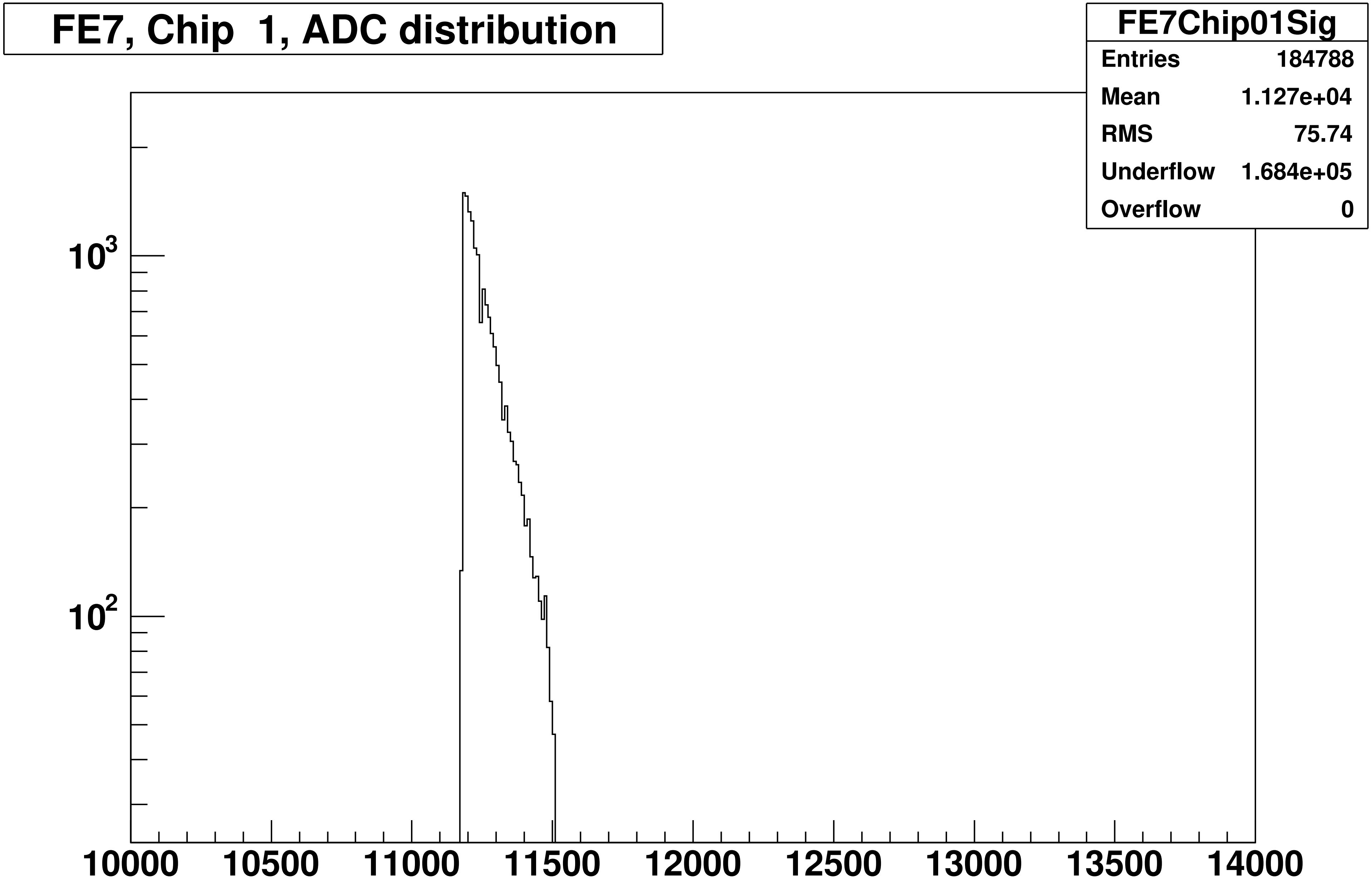
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200


FE7, Chip 1, ADC distribution
FE7Chip01Sig
Entries 184788
Mean 1.127e+04
RMS 75.74
Underflow 1.684e+05
Overflow 0
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10^2
10000
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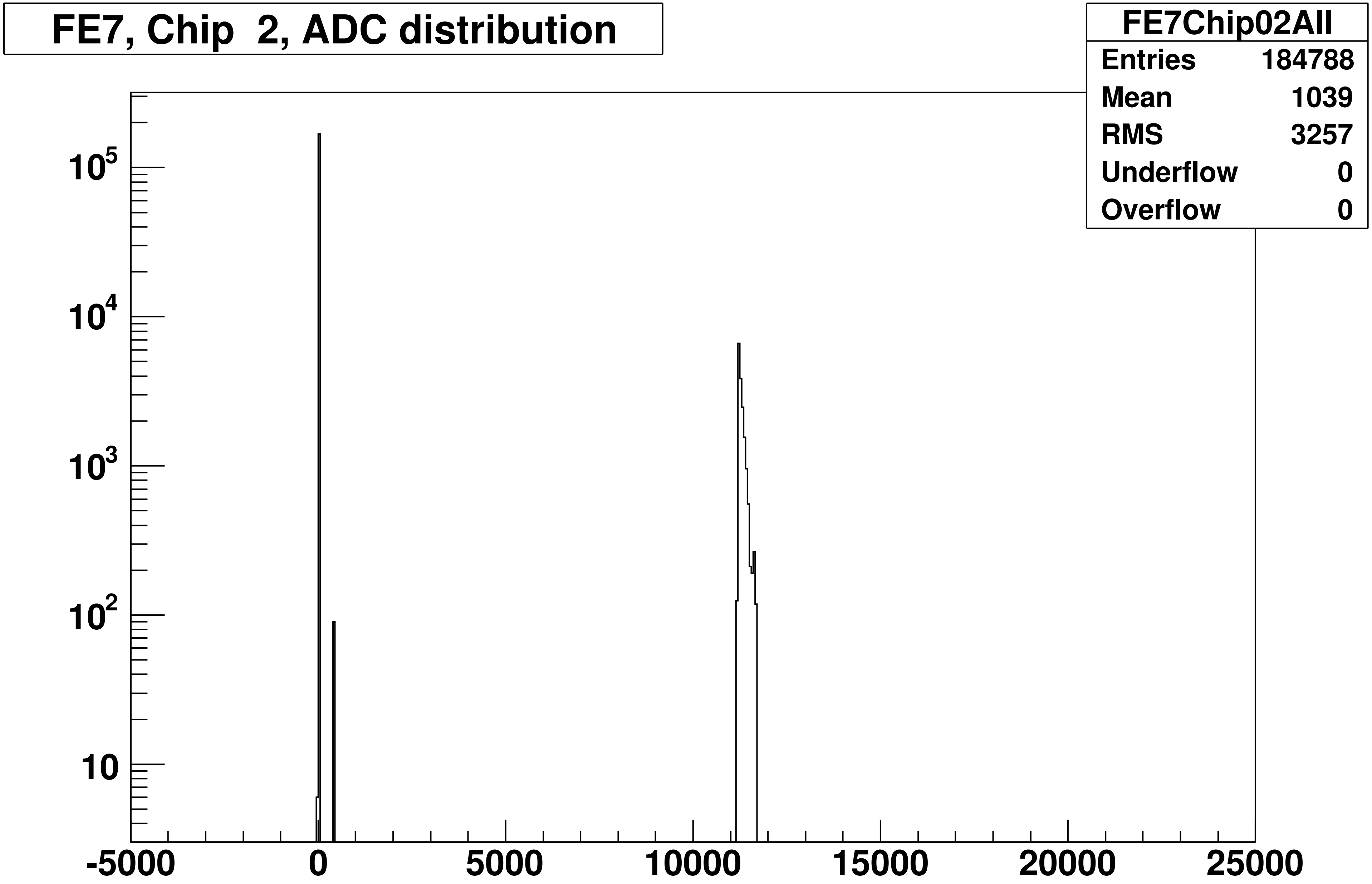
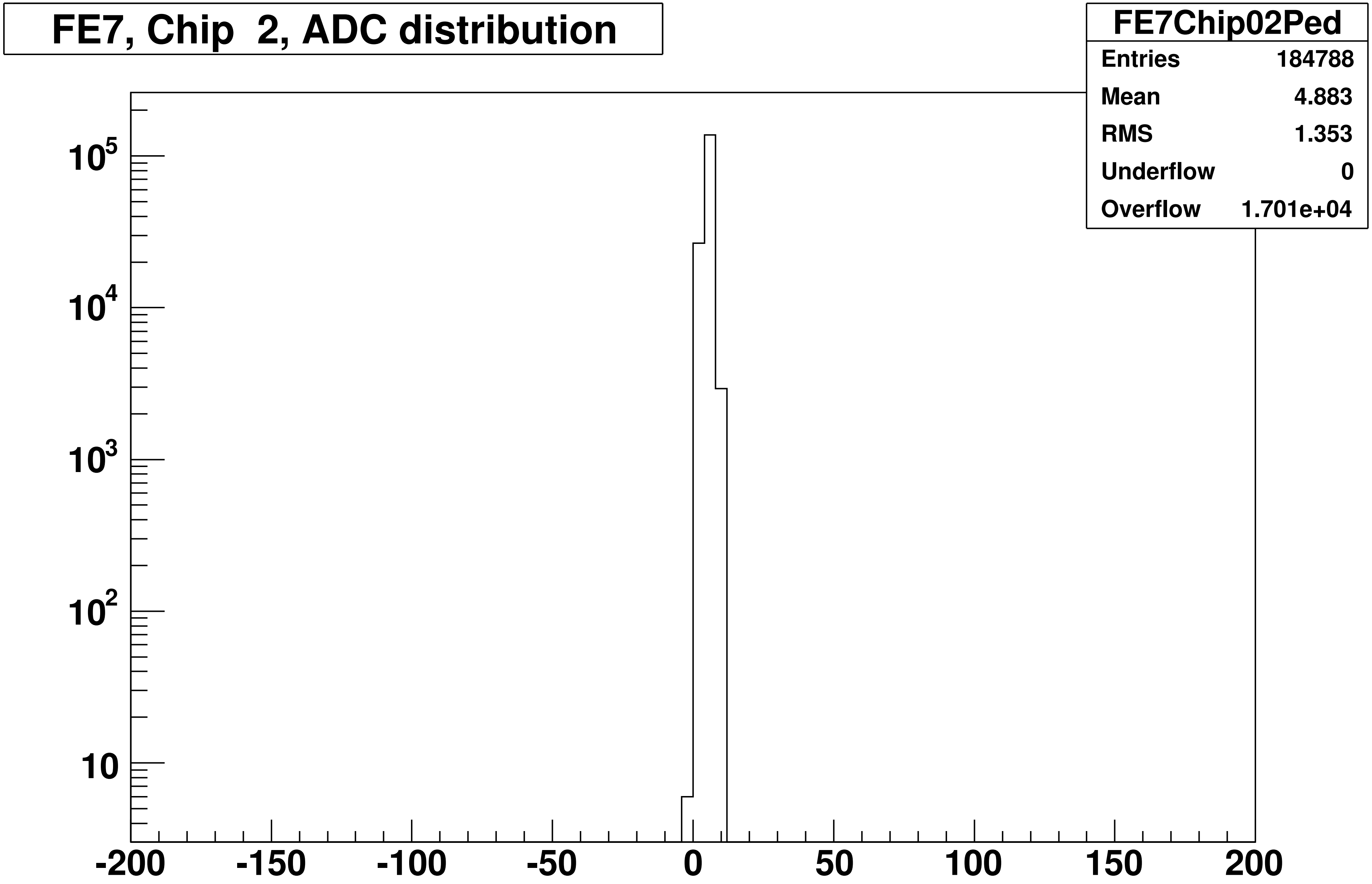
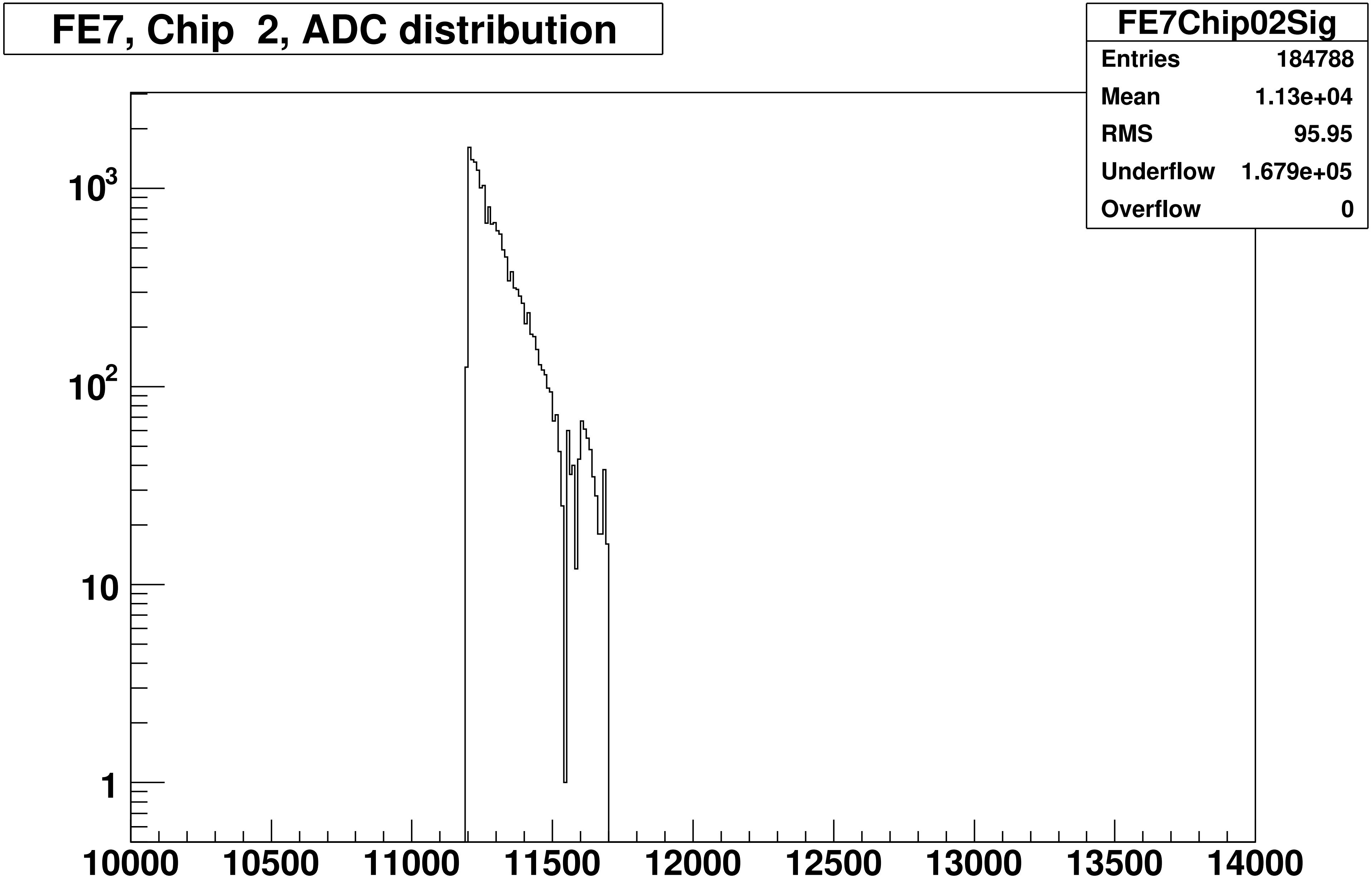
11500
12000
12500
13000
13500
14000


FE7, Chip 2, ADC distribution
FE7Chip02All
Entries 184788
Mean 1039
RMS 3257
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 2, ADC distribution
FE7Chip02Ped
Entries 184788
Mean 4.883
RMS 1.353
Underflow 0
Overflow 1.701e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200



FE7, Chip 2, ADC distribution
FE7Chip02Sig
Entries 184788
Mean 1.13e+04
RMS 95.95
Underflow 1.679e+05
Overflow 0
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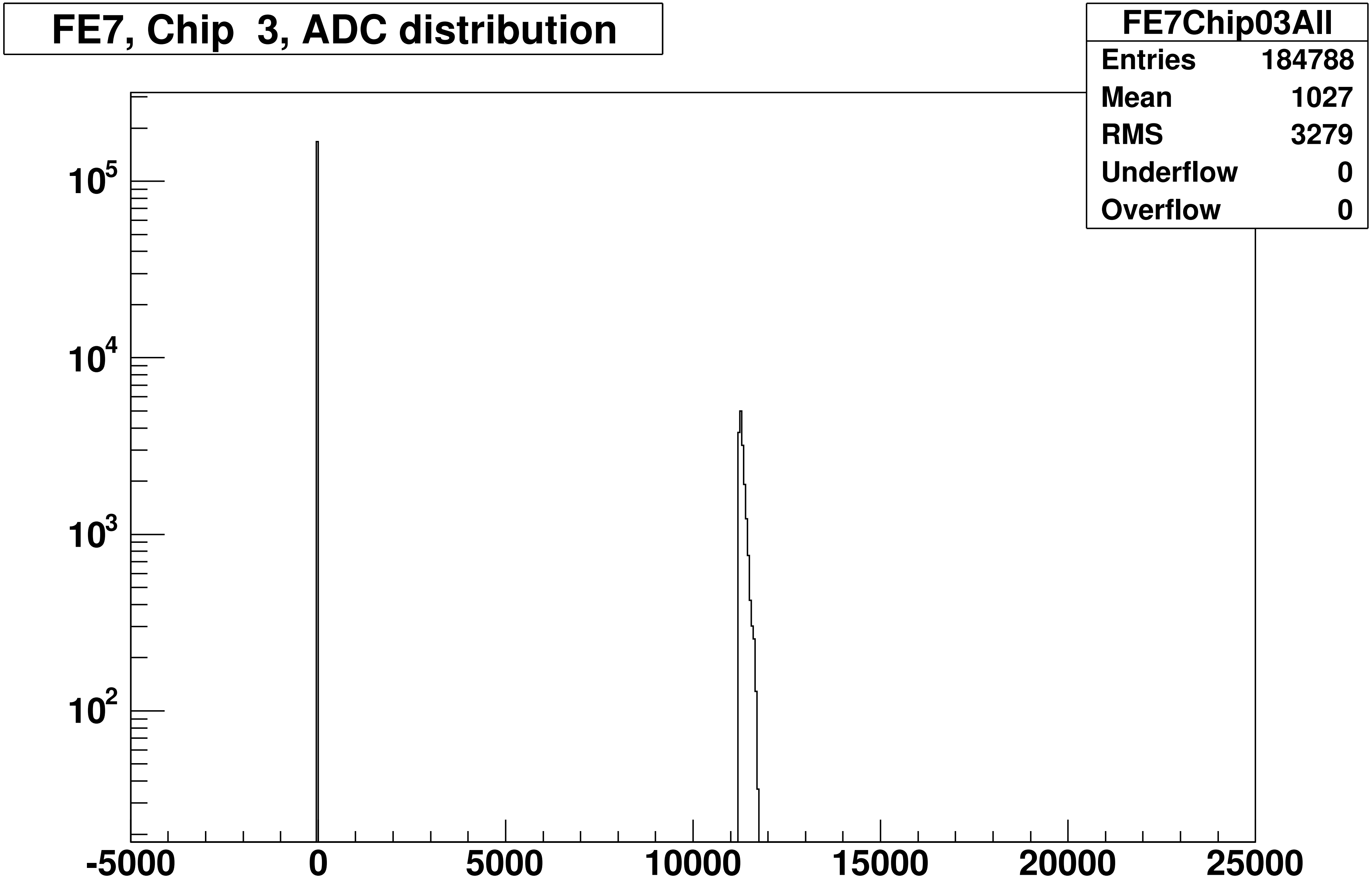
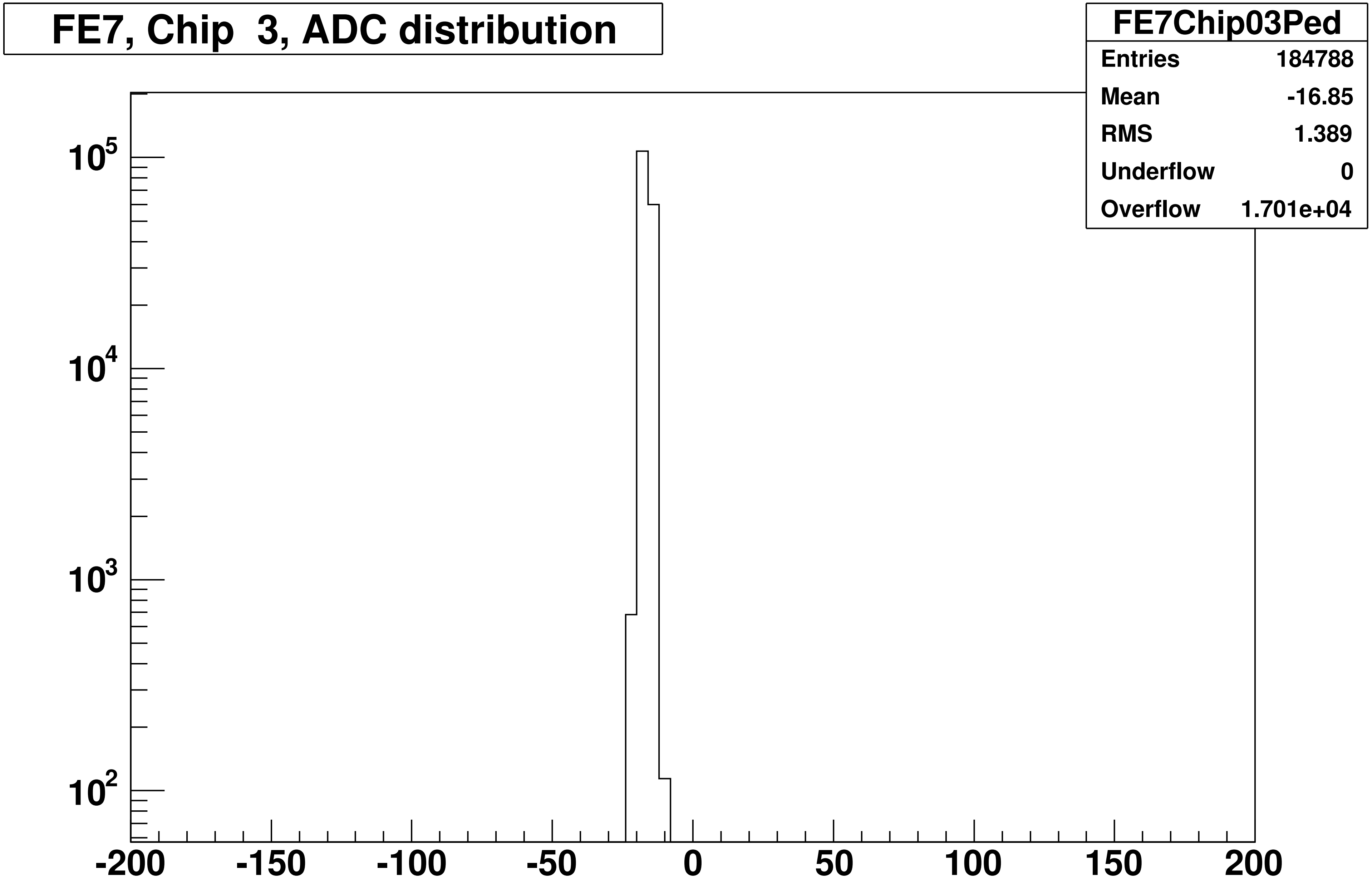
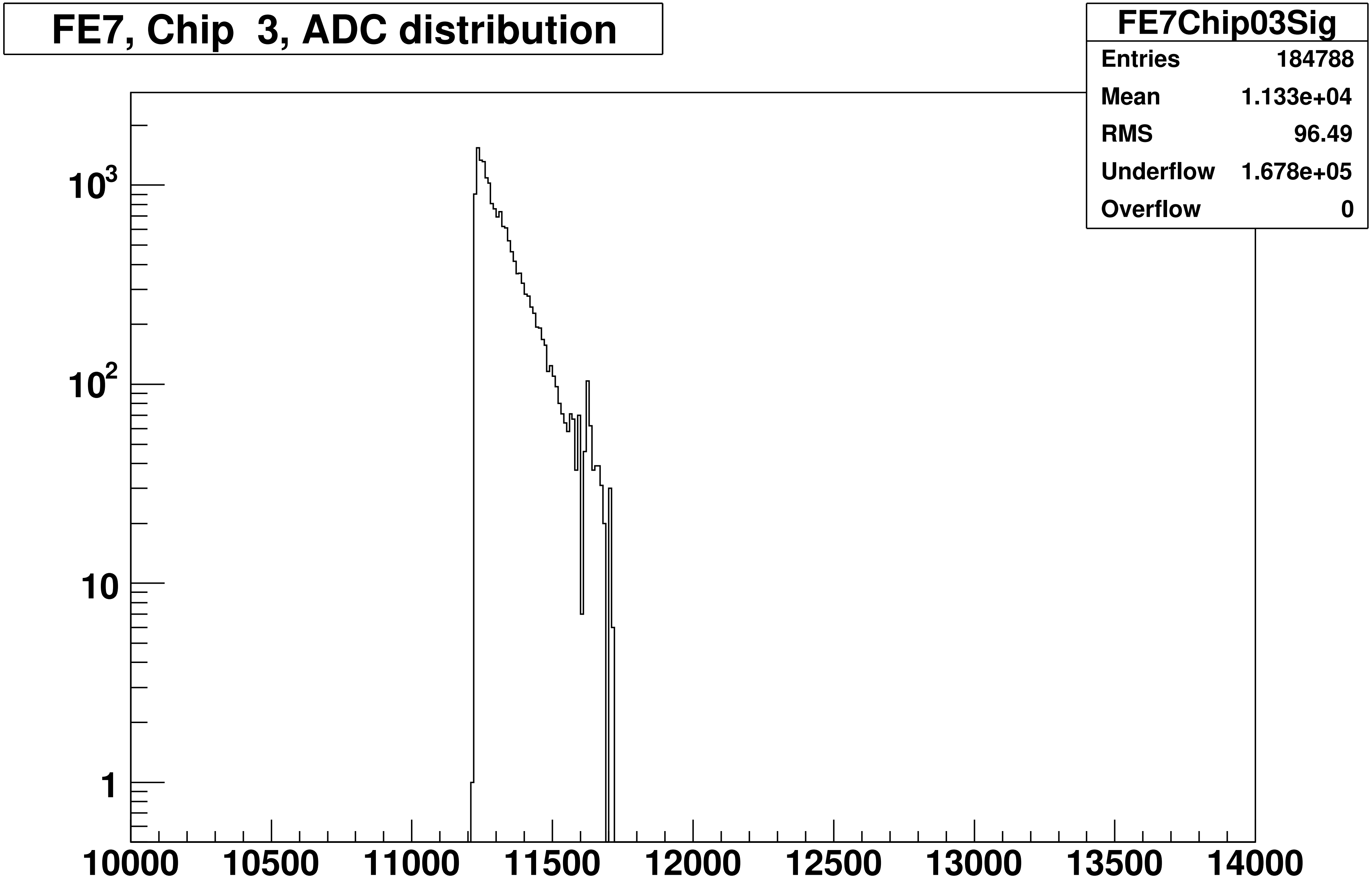
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 3, ADC distribution
FE7Chip03All
Entries 184788
Mean 1027
RMS 3279
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 3, ADC distribution
FE7Chip03Ped
Entries 184788
Mean -16.85
RMS 1.389
Underflow 0
Overflow 1.701e+04
10^5
10^4
10^3
10^2
-200 -150 -100 -50 0 50 100 150 200



FE7, Chip 3, ADC distribution
FE7Chip03Sig
Entries 184788
Mean 1.133e+04
RMS 96.49
Underflow 1.678e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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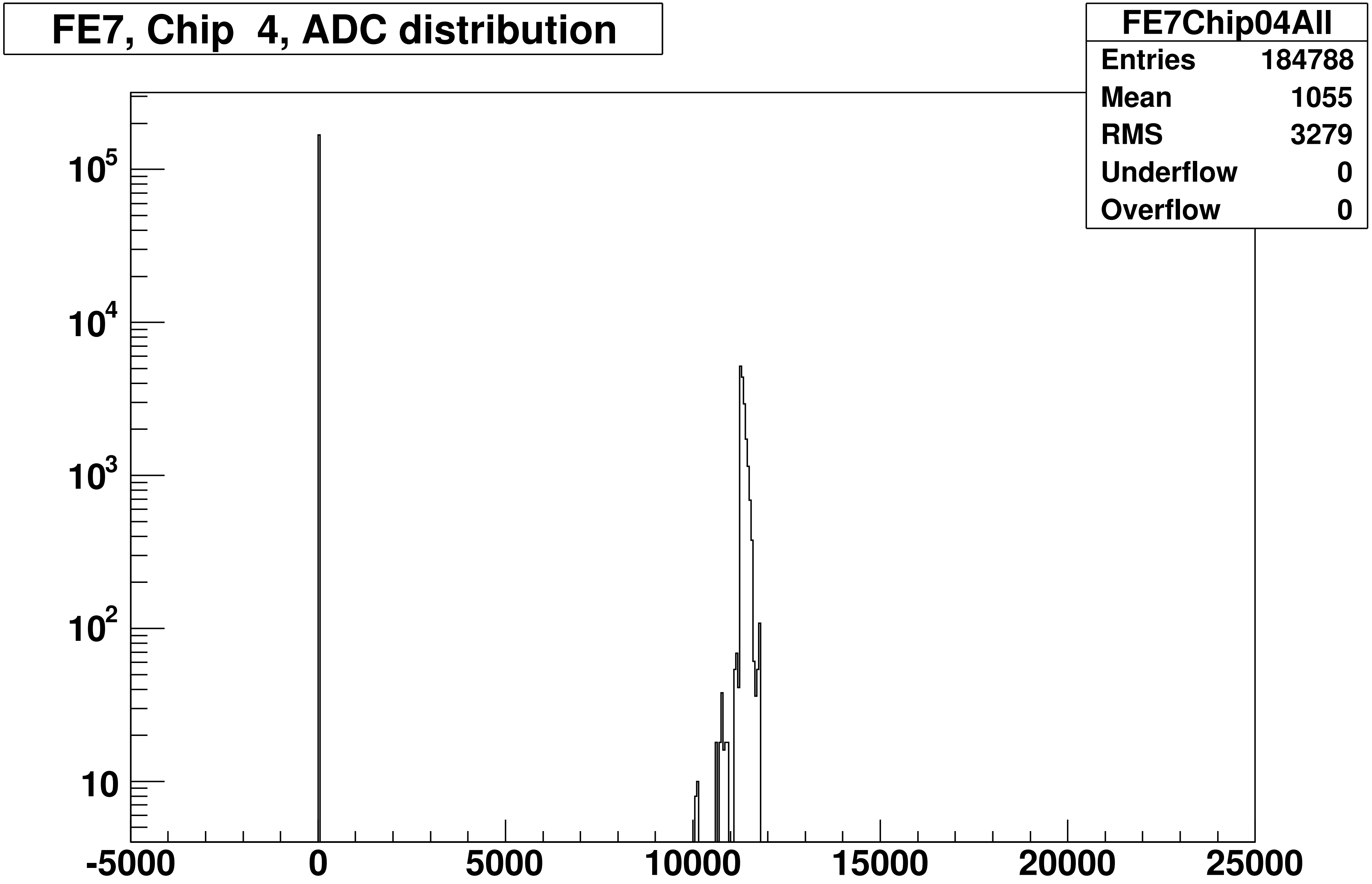
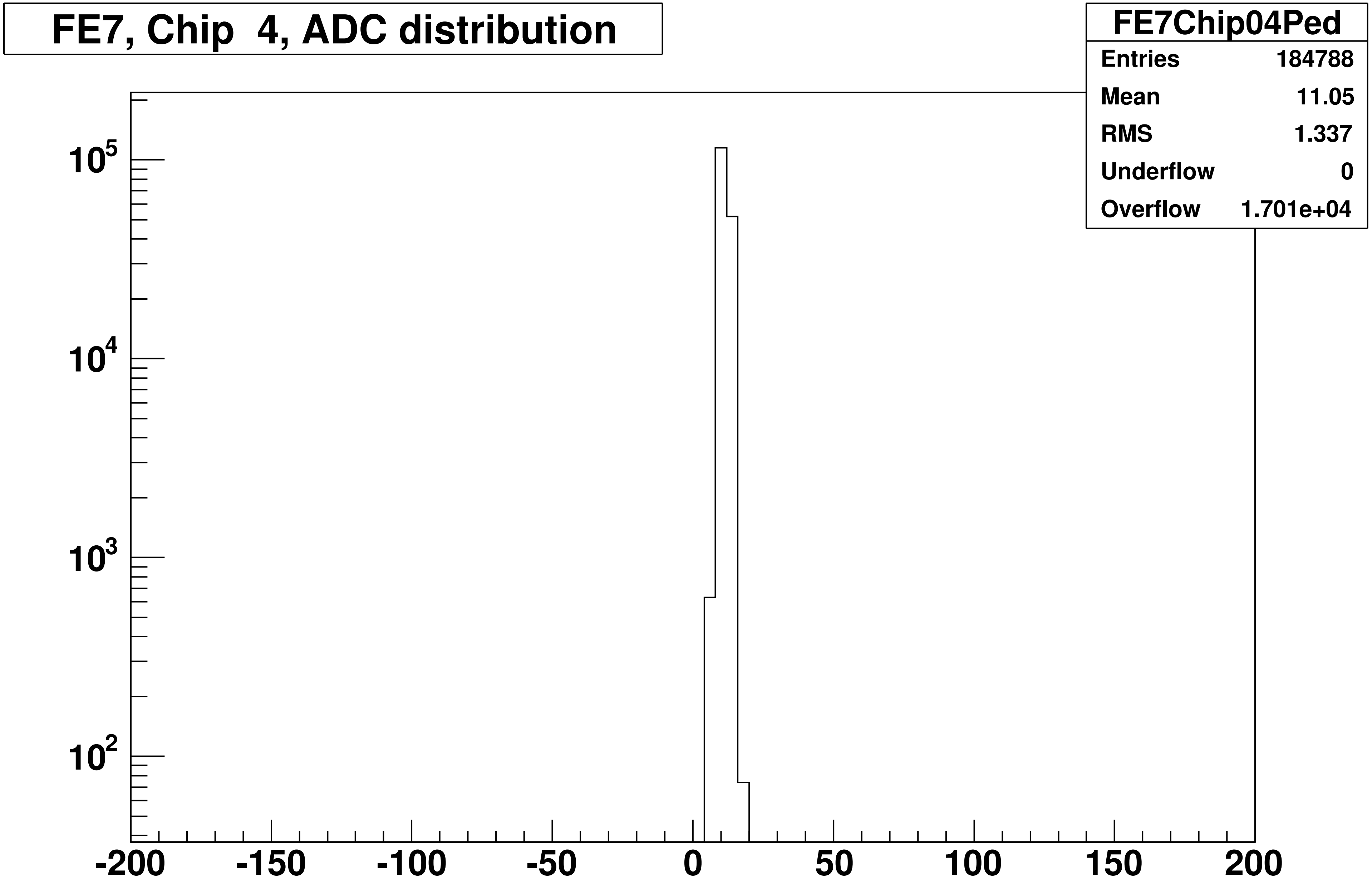
13500
14000



FE7, Chip 4, ADC distribution
FE7Chip04All
Entries 184788
Mean 1055
RMS 3279
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 4, ADC distribution
FE7Chip04Ped
Entries 184788
Mean 11.05
RMS 1.337
Underflow 0
Overflow 1.701e+04
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10^4
10^3
10^2
-200
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-100
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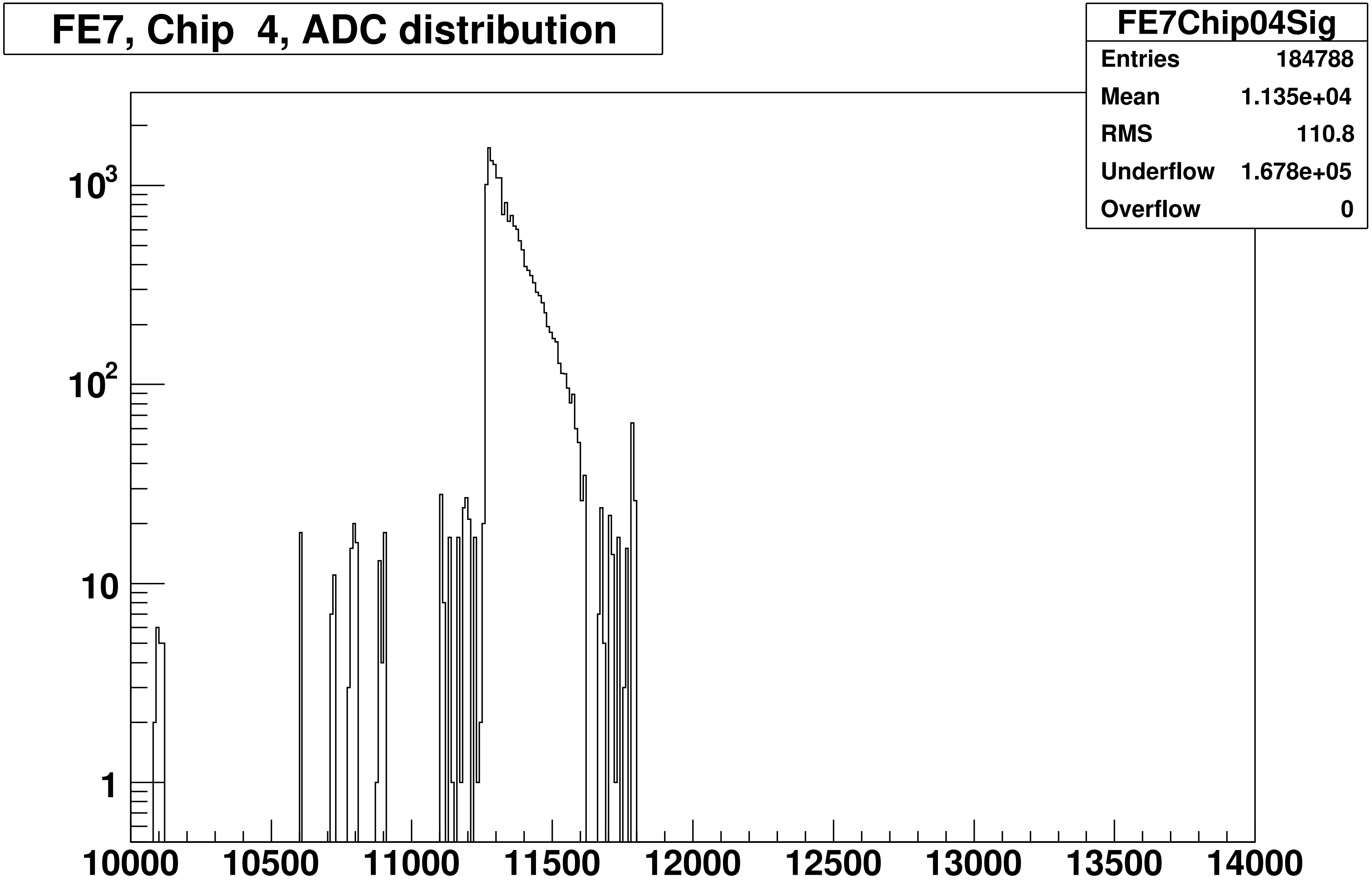
150
200


FE7, Chip 4, ADC distribution
FE7Chip04Sig
Entries 184788
Mean 1.135e+04
RMS 110.8
Underflow 1.678e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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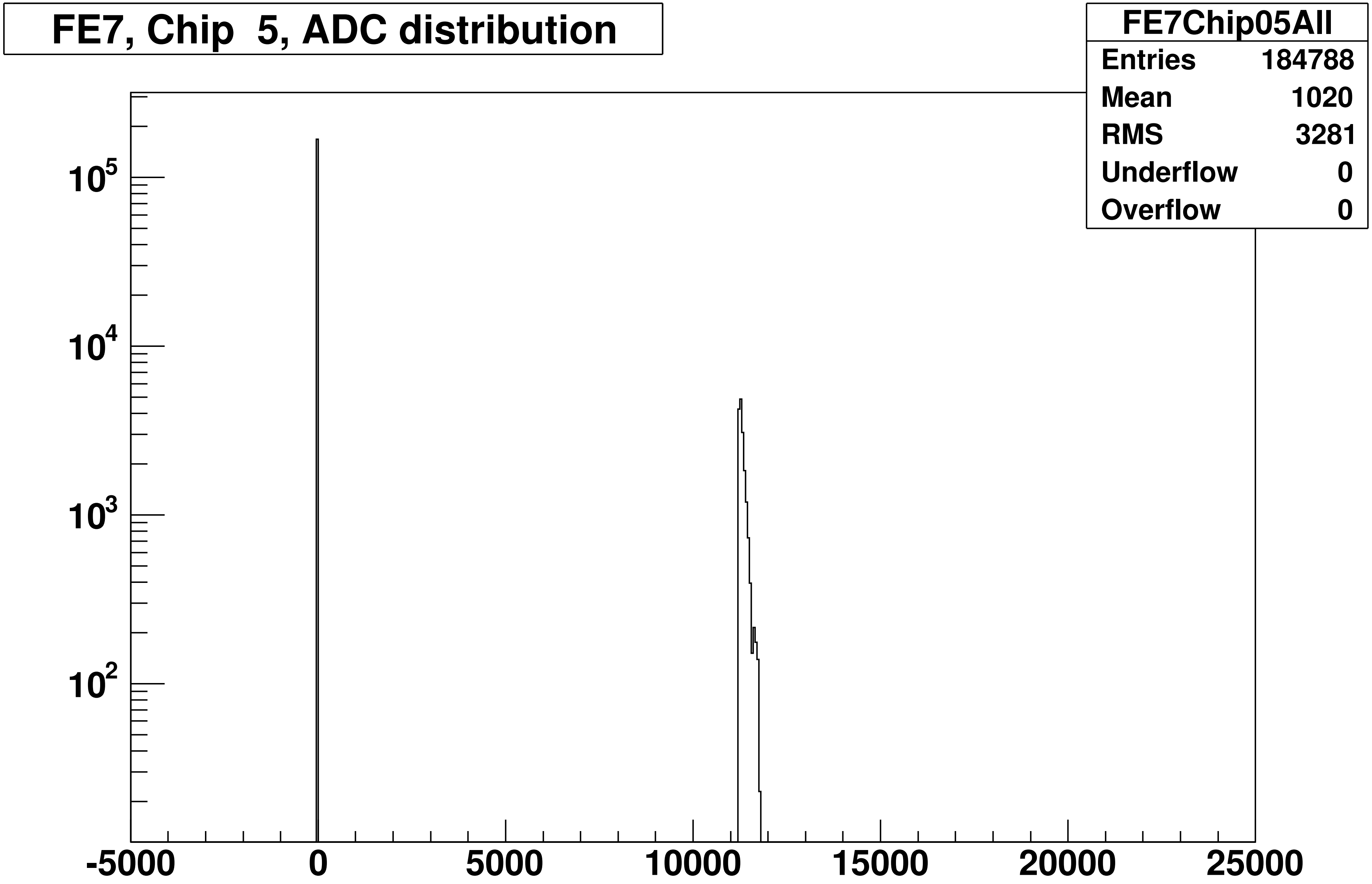
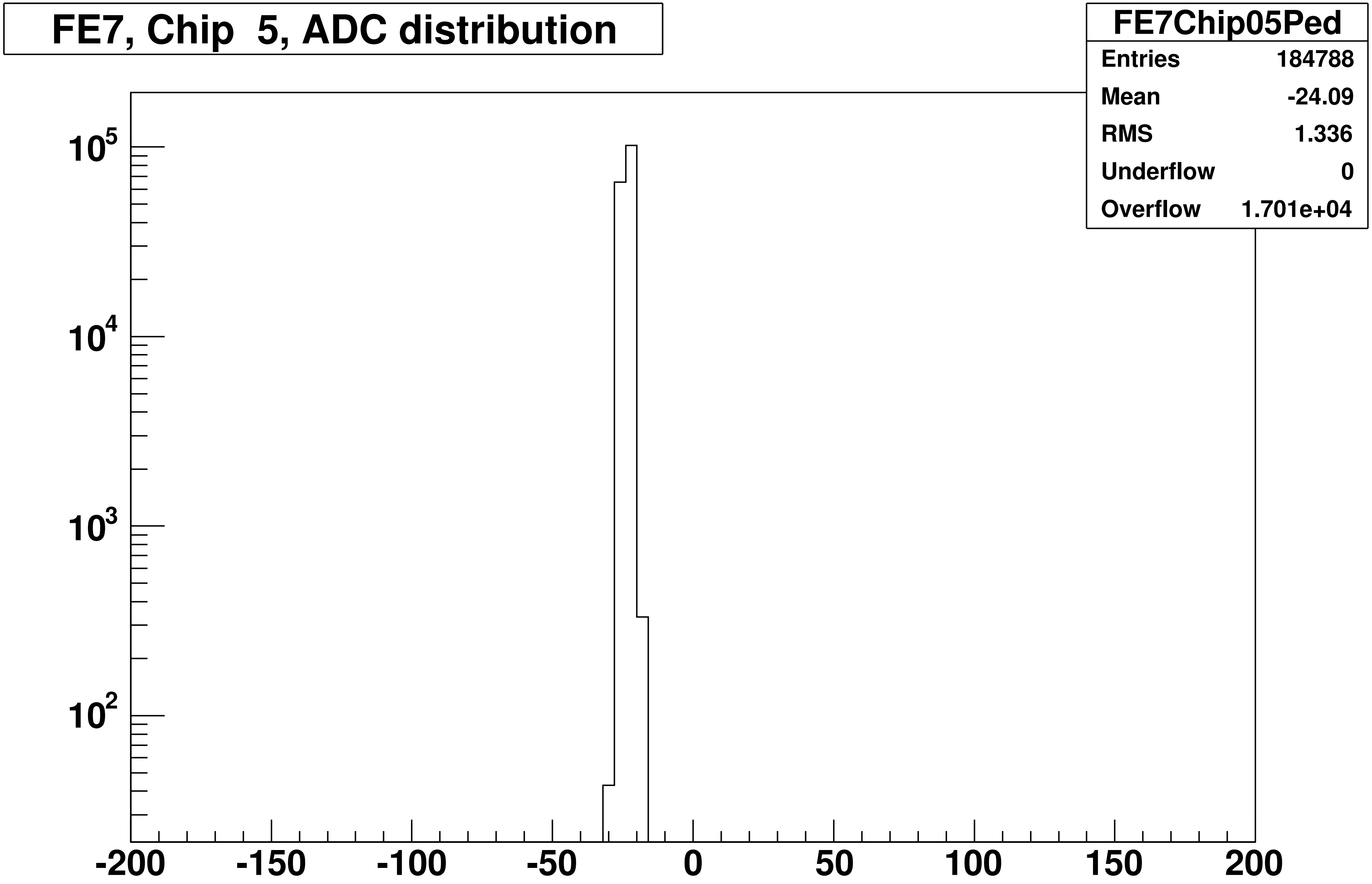

FE7, Chip 5, ADC distribution
FE7Chip05All
Entries 184788
Mean 1020
RMS 3281
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000



FE7, Chip 5, ADC distribution
FE7Chip05Ped
Entries 184788
Mean -24.09
RMS 1.336
Underflow 0
Overflow 1.701e+04
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10^4
10^3
10^2
-200
-150
-100
-50
0
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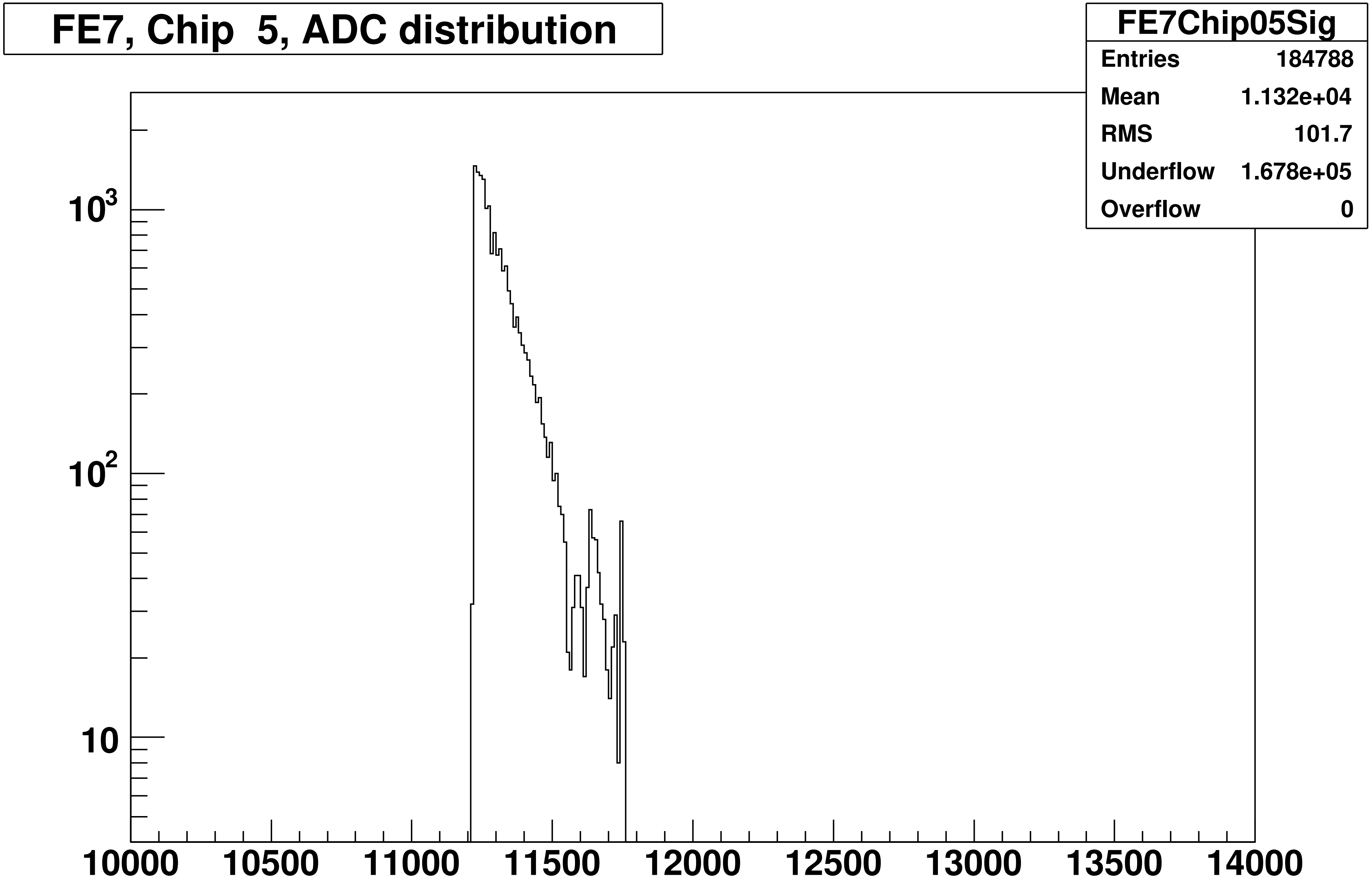
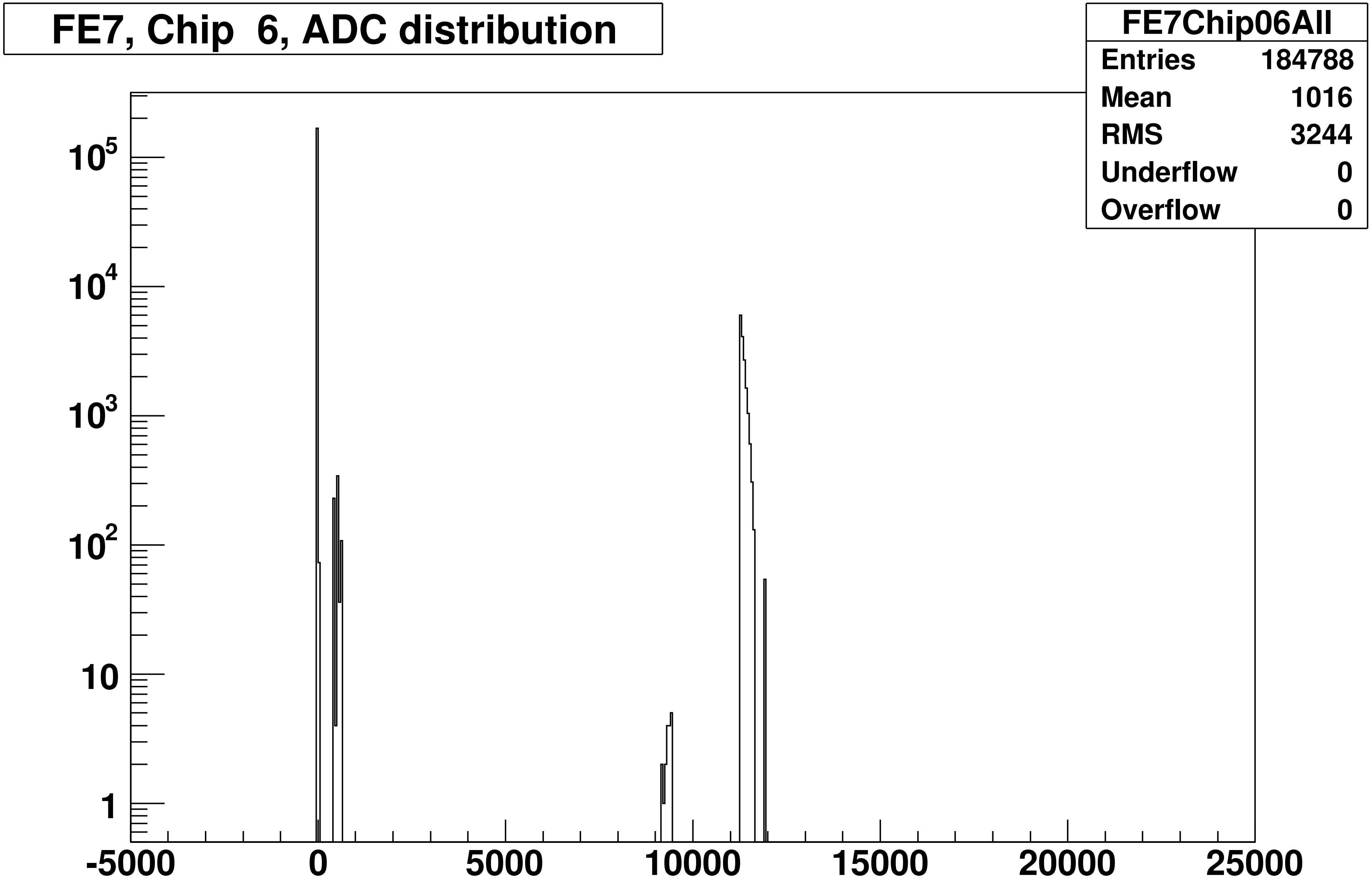
100
150
200



FE7, Chip 5, ADC distribution
FE7Chip05Sig
Entries 184788
Mean 1.132e+04
RMS 101.7
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000


FE7, Chip 6, ADC distribution
FE7Chip06All
Entries 184788
Mean 1016
RMS 3244
Underflow 0
Overflow 0
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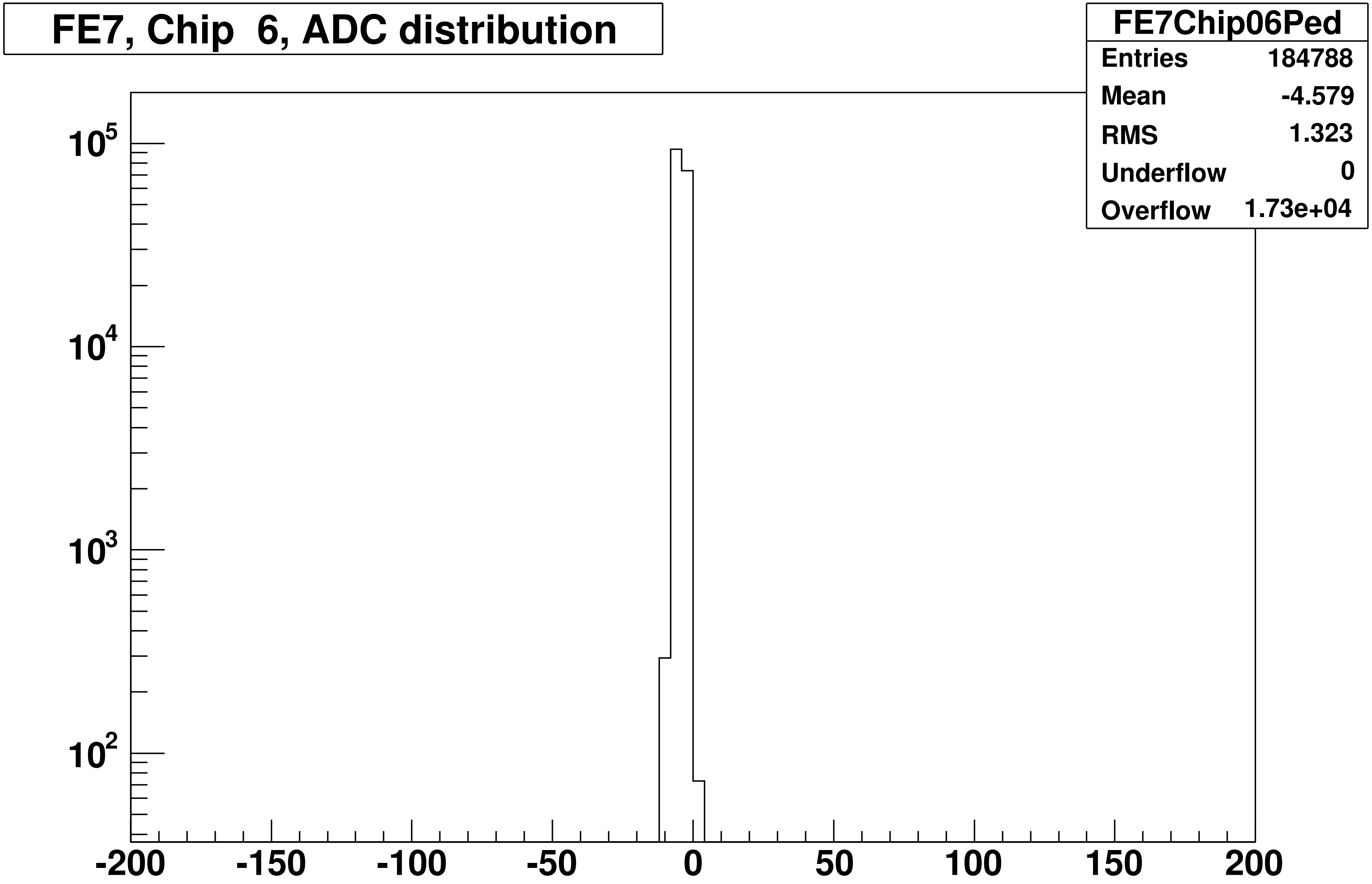
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 6, ADC distribution
FE7Chip06Ped
Entries 184788
Mean -4.579
RMS 1.323
Underflow 0
Overflow 1.73e+04
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10^4
10^3
10^2
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-100
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0
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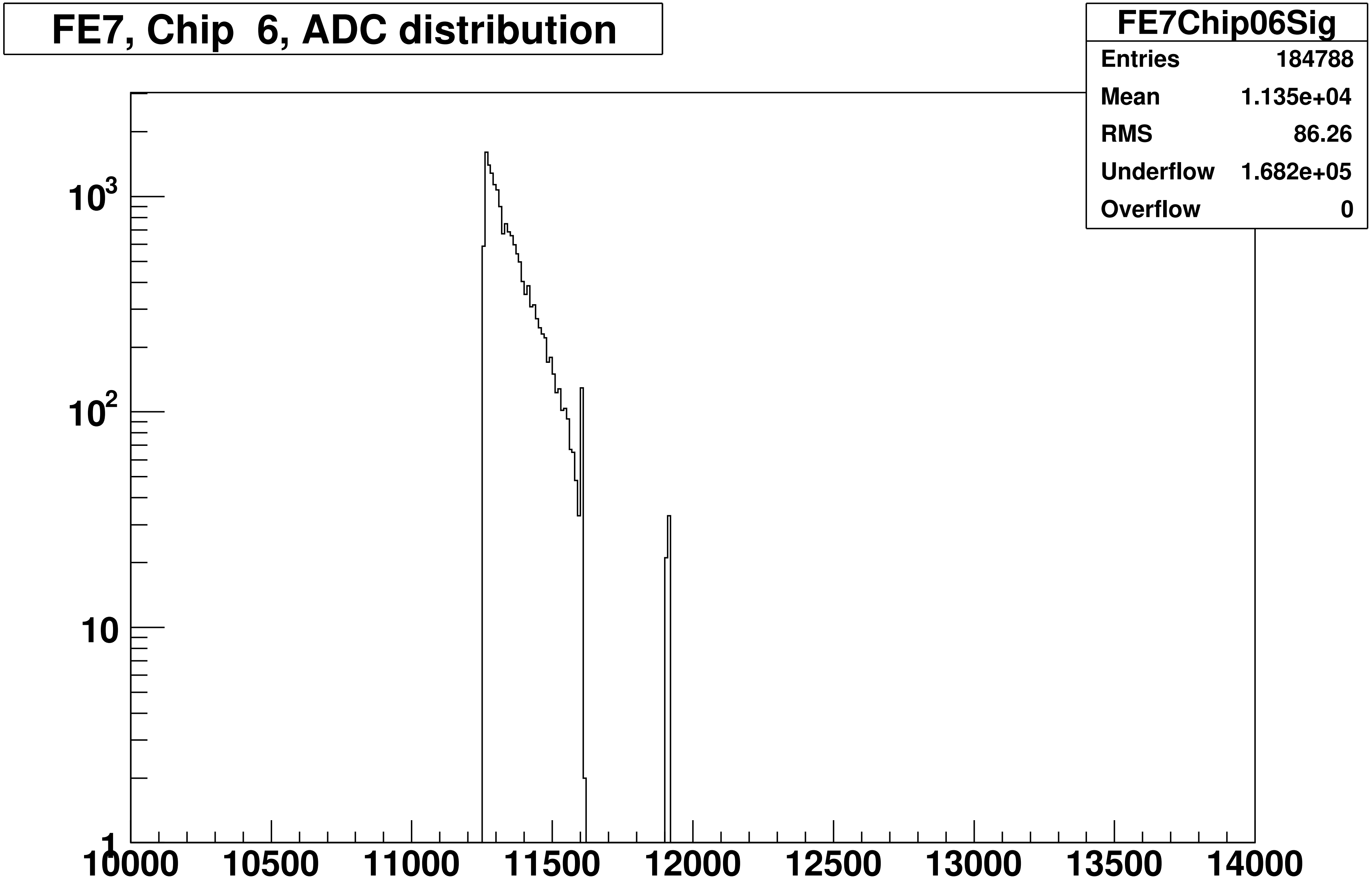
100
150
200


FE7, Chip 6, ADC distribution
FE7Chip06Sig
Entries 184788
Mean 1.135e+04
RMS 86.26
Underflow 1.682e+05
Overflow 0
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10^2
10
1
10000
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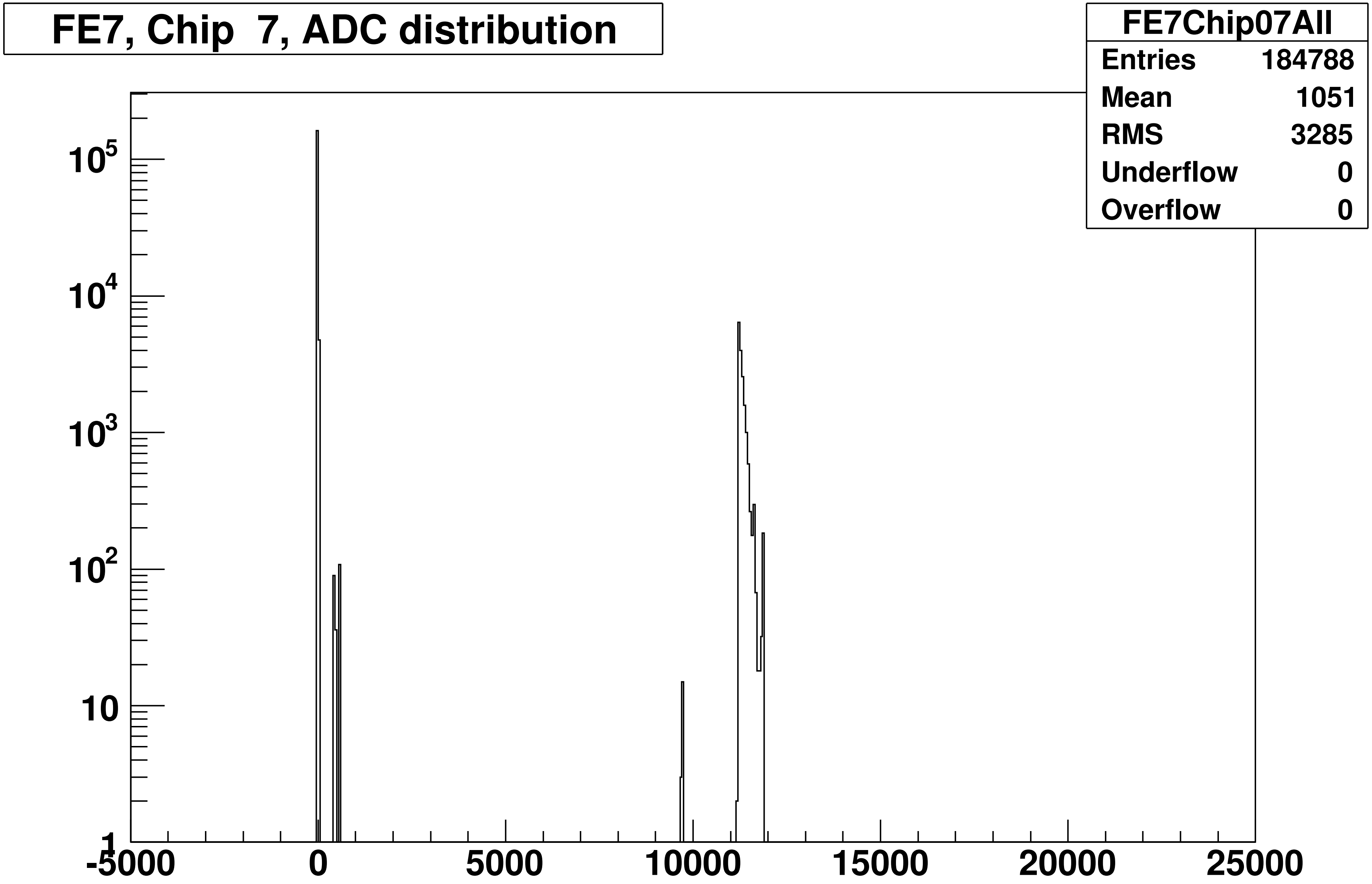
14000


FE7, Chip 7, ADC distribution
FE7Chip07All
Entries 184788
Mean 1051
RMS 3285
Underflow 0
Overflow 0
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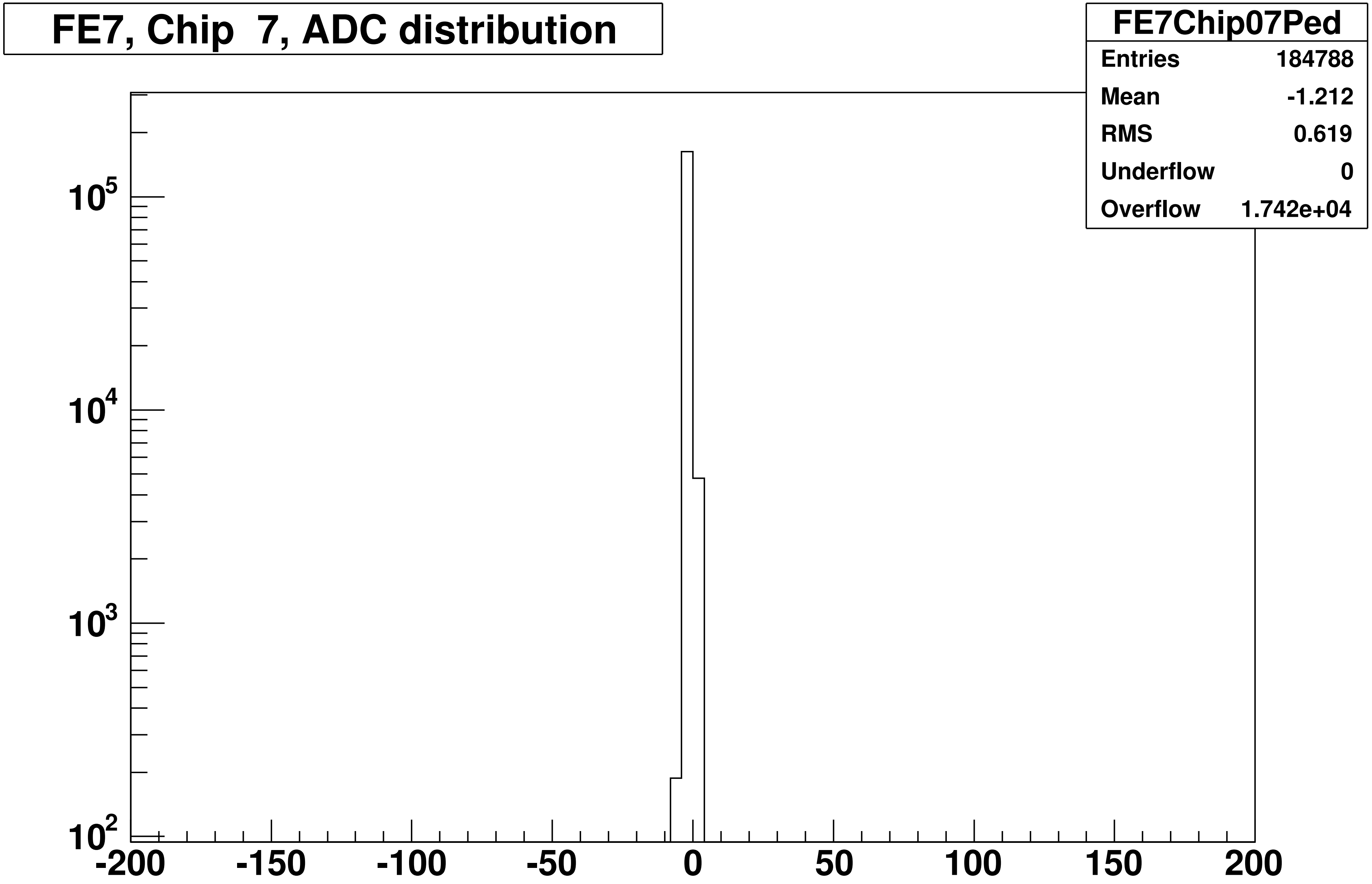
10^4
10^3
10^2
10
1
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 7, ADC distribution
FE7Chip07Ped
Entries 184788
Mean -1.212
RMS 0.619
Underflow 0
Overflow 1.742e+04
10^5
10^4
10^3
10^2
-200
-150
-100
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0
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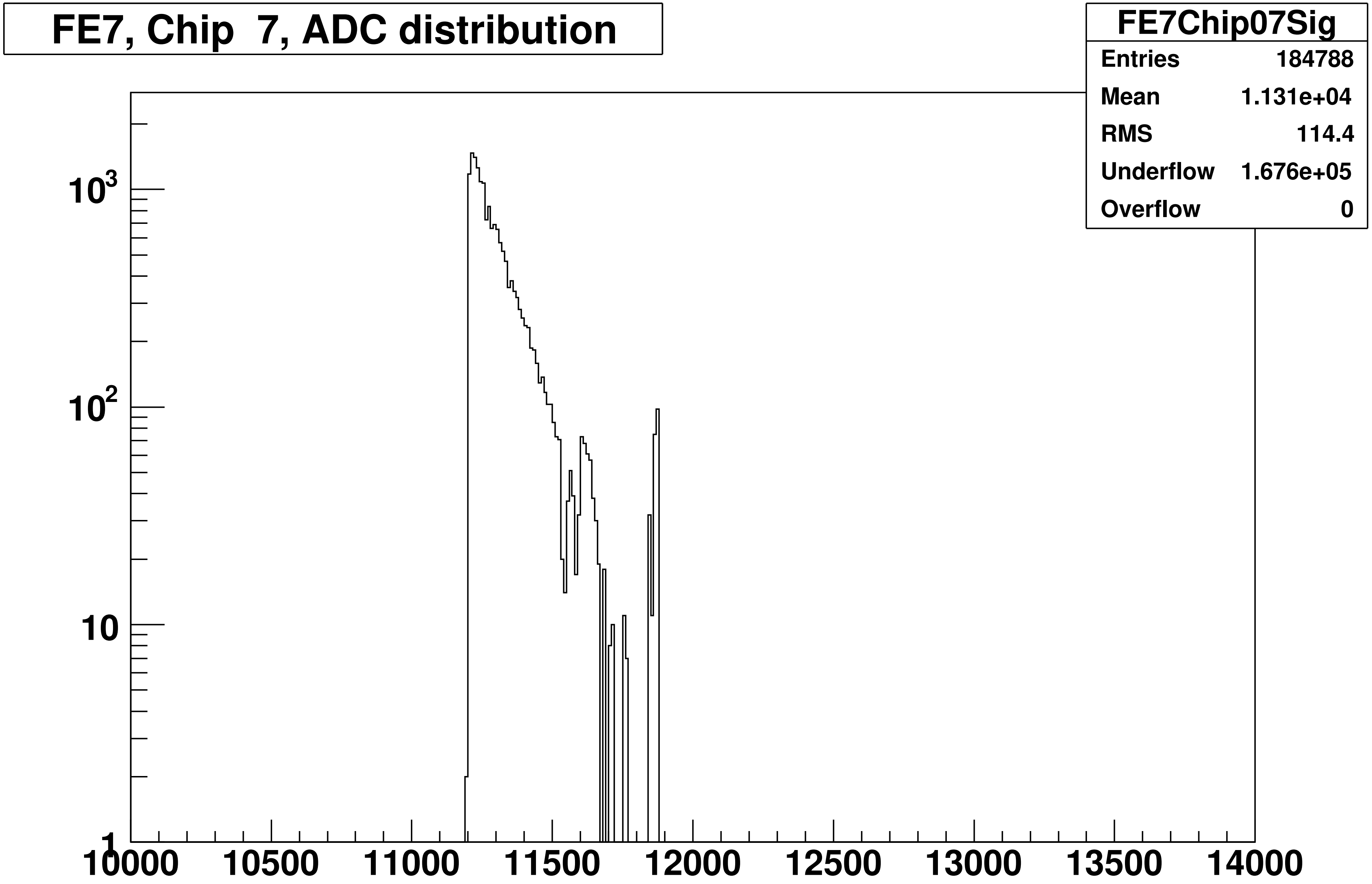
100
150
200


FE7, Chip 7, ADC distribution
FE7Chip07Sig
Entries 184788
Mean 1.131e+04
RMS 114.4
Underflow 1.676e+05
Overflow 0
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10^2
10
1
10000
10500
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11500
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12500
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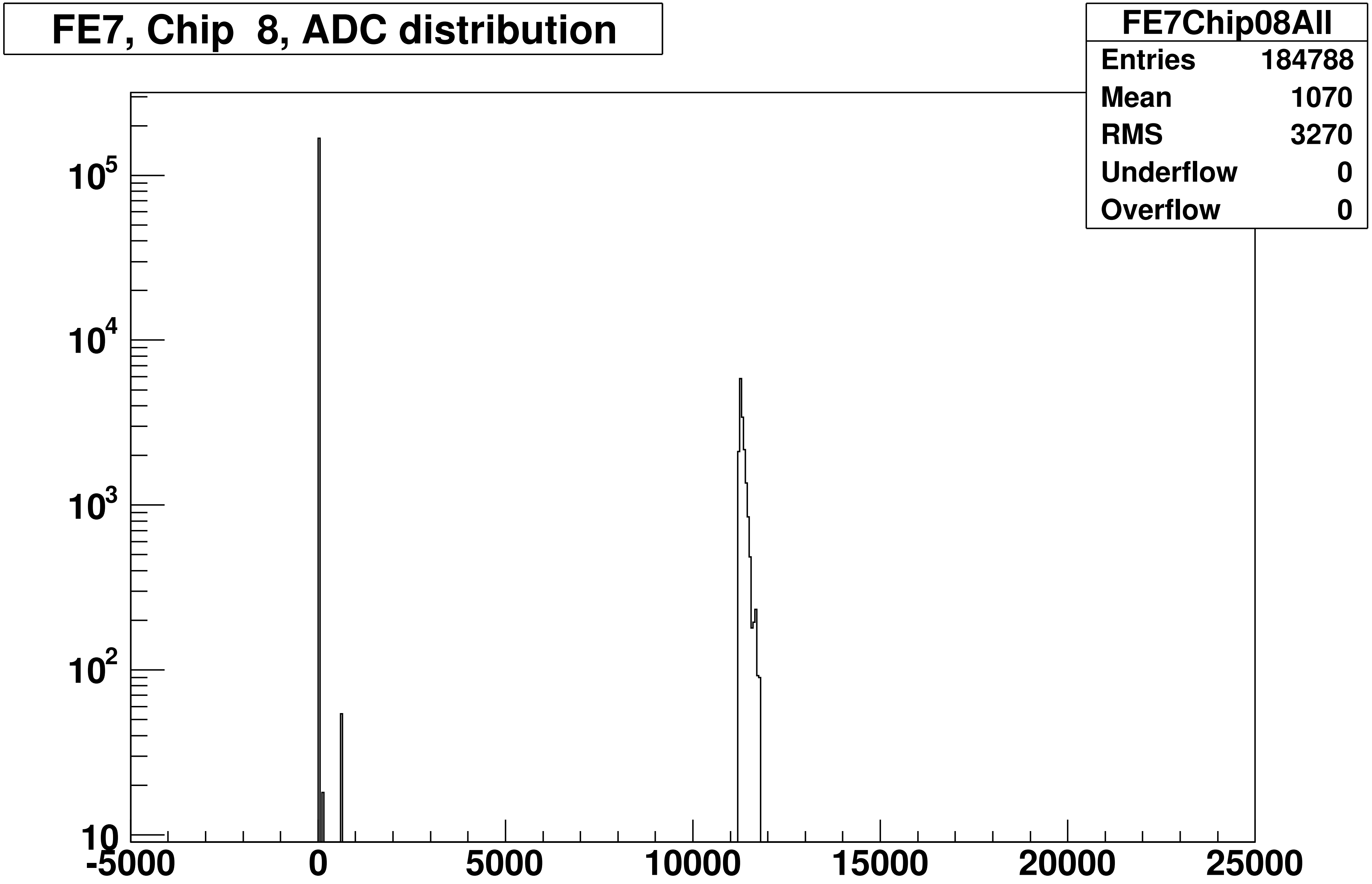
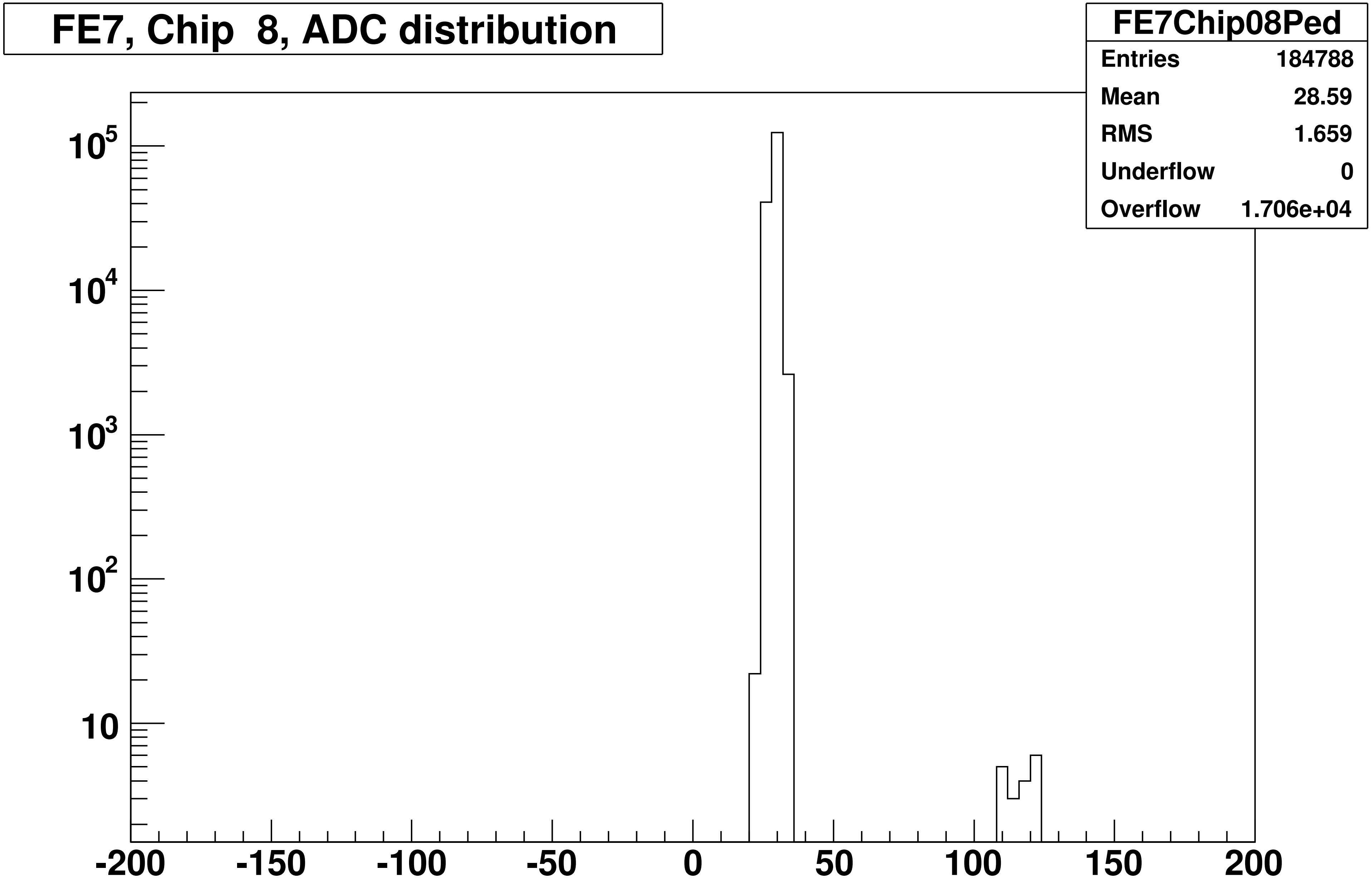
14000


FE7, Chip 8, ADC distribution
FE7Chip08All
Entries 184788
Mean 1070
RMS 3270
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
10
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 8, ADC distribution
FE7Chip08Ped
Entries 184788
Mean 28.59
RMS 1.659
Underflow 0
Overflow 1.706e+04
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10^4
10^3
10^2
10
-200
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-100
-50
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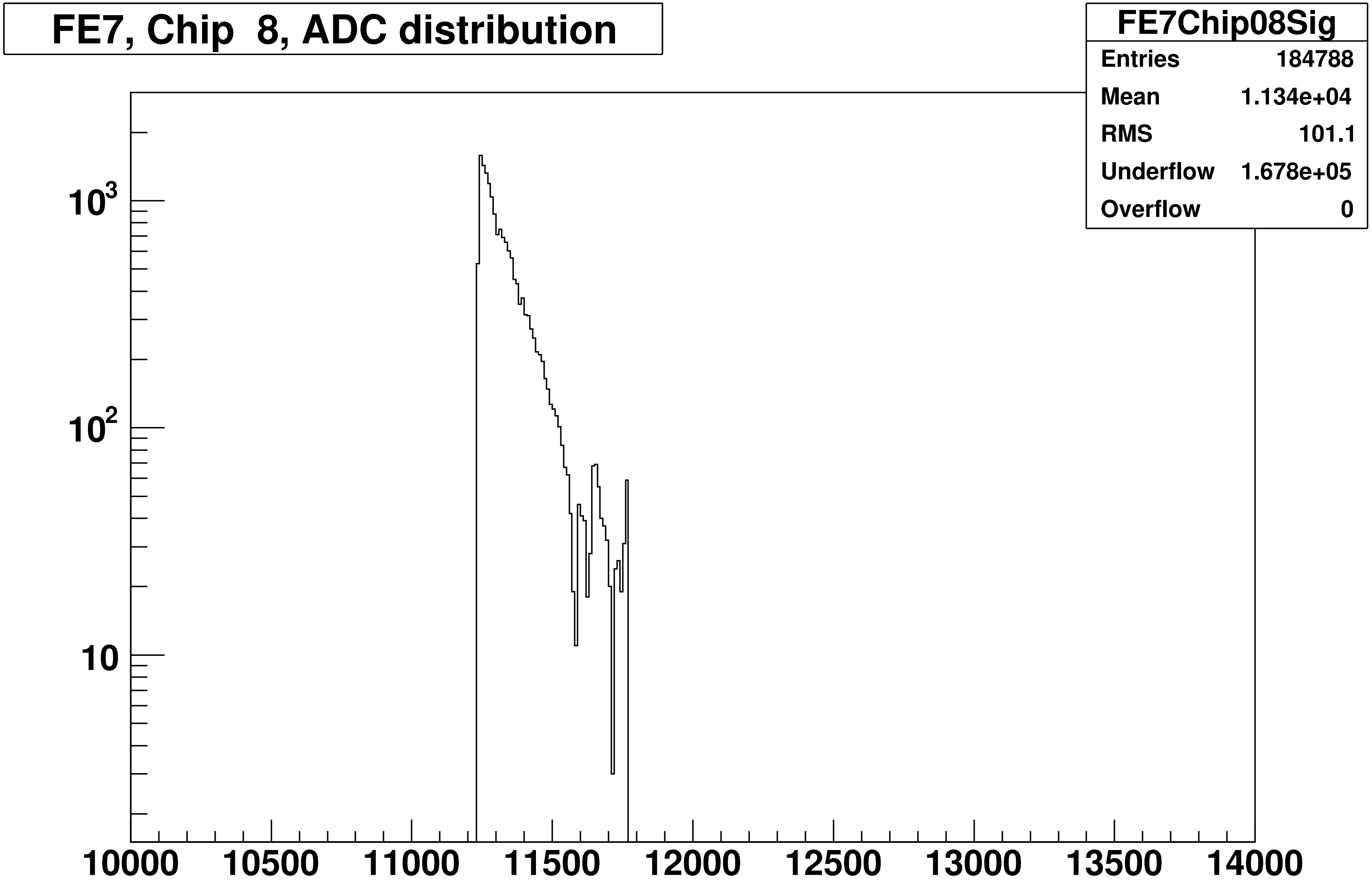
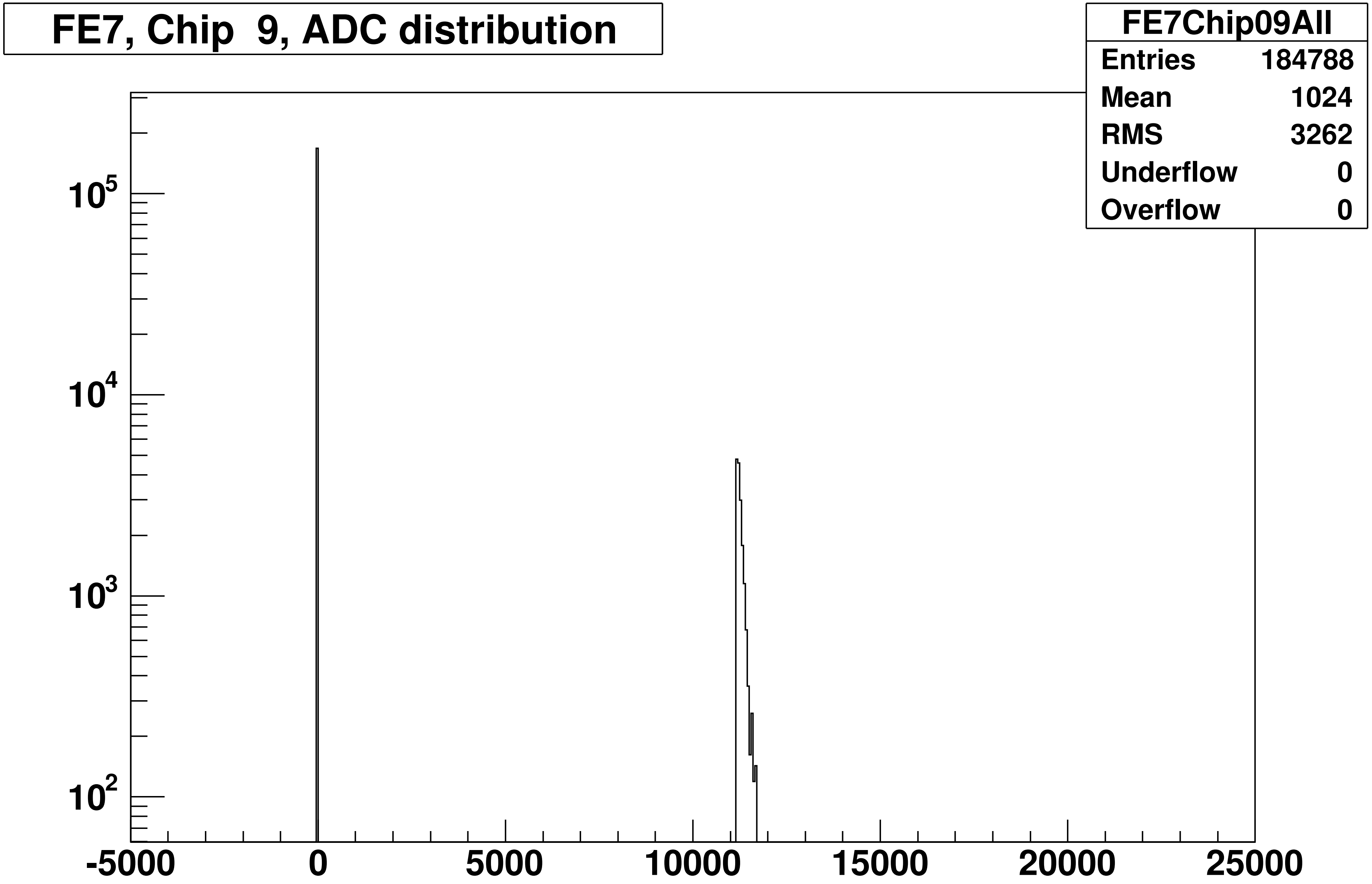
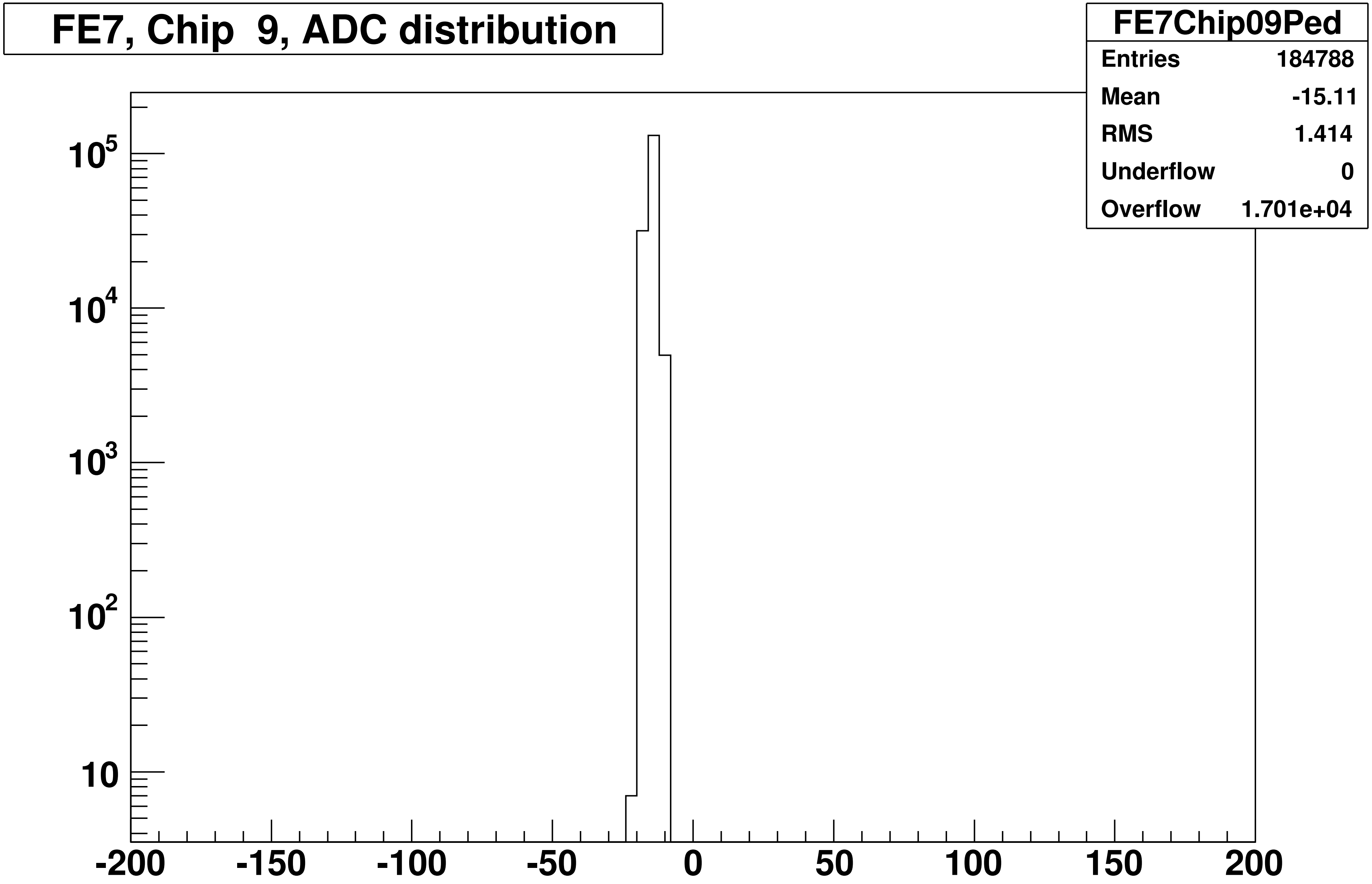
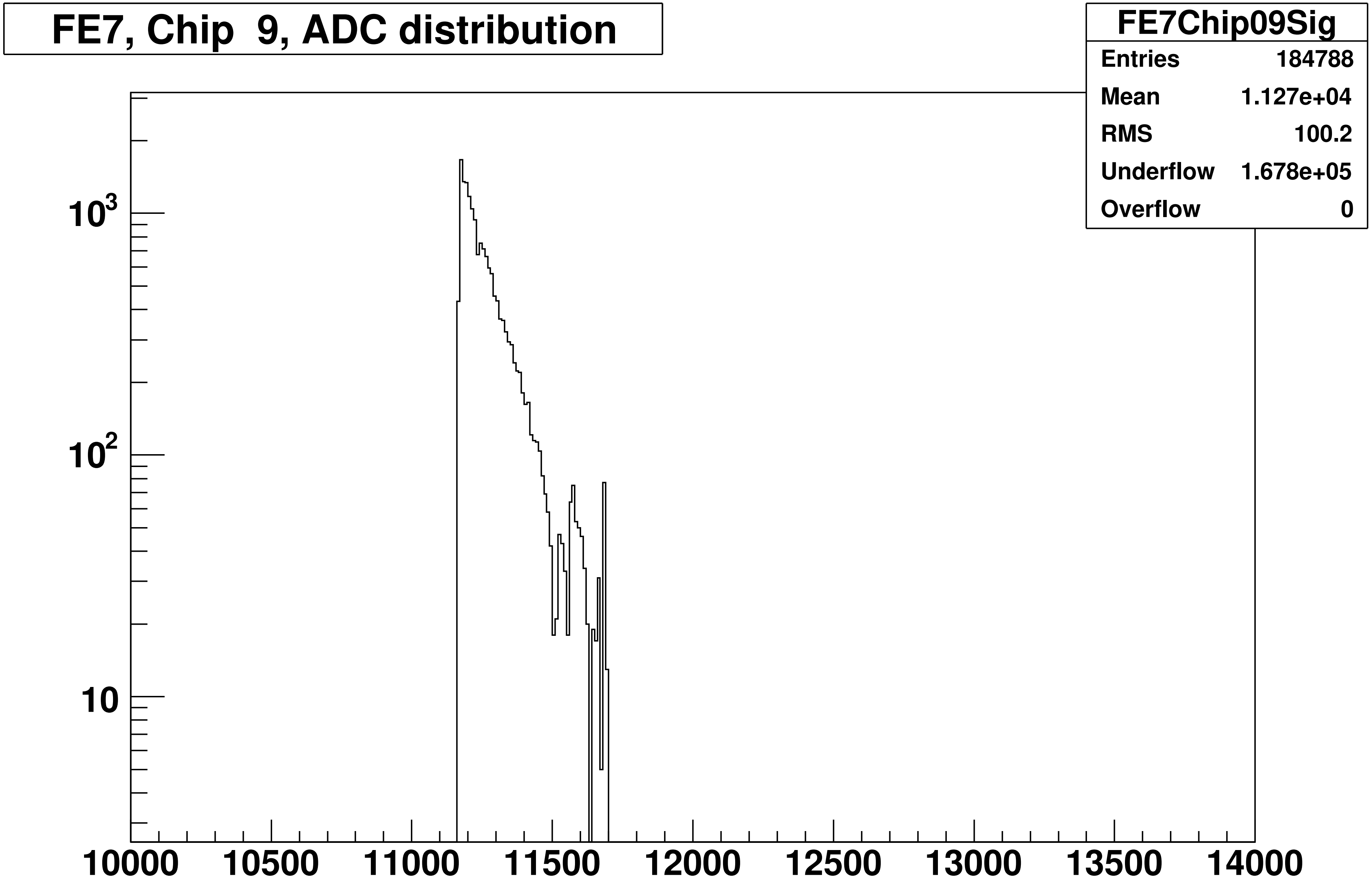
50
100
150
200

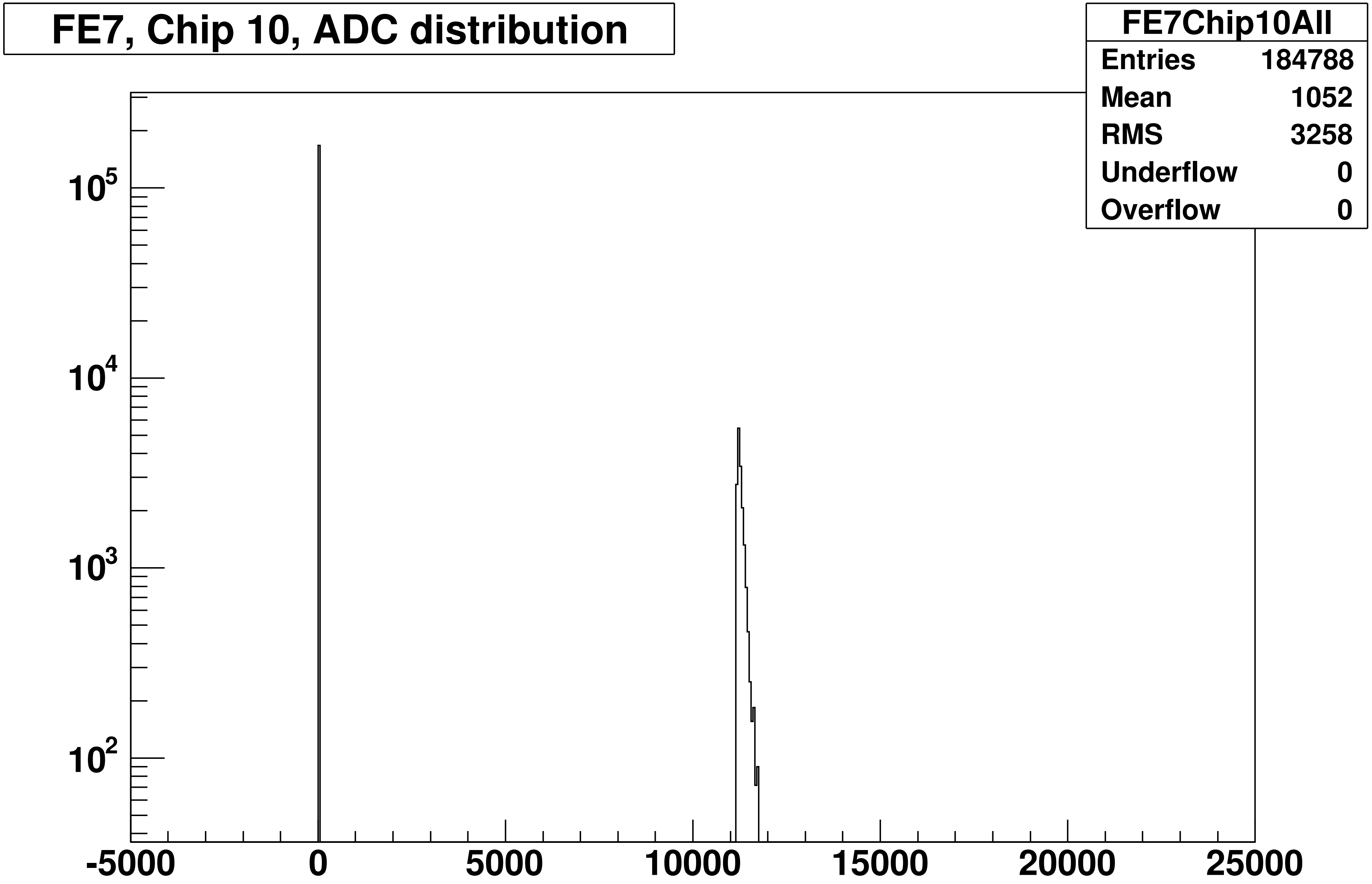

FE7, Chip 8, ADC distribution
FE7Chip08Sig
Entries 184788
Mean 1.134e+04
RMS 101.1
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000



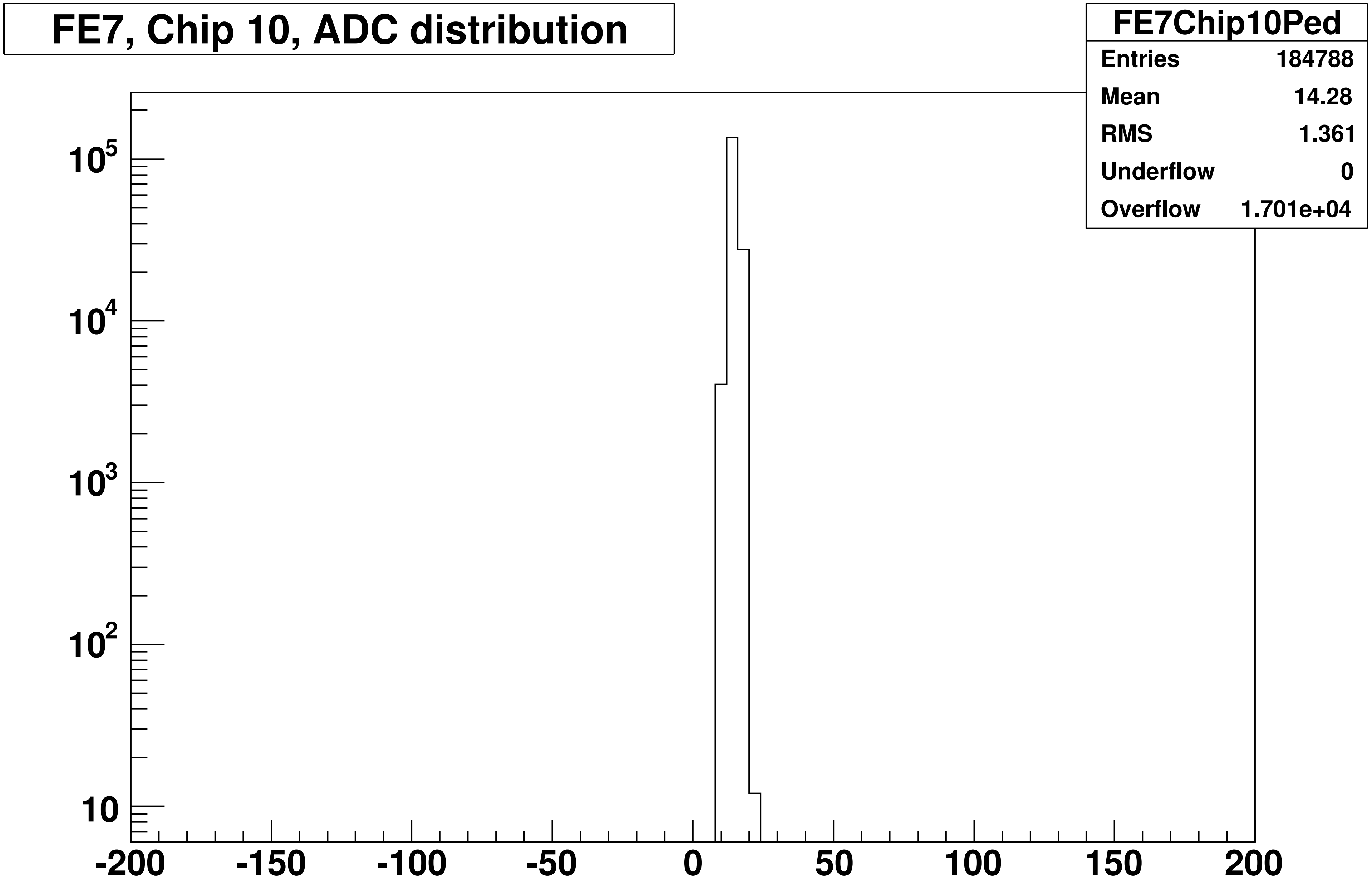
FE7, Chip 9, ADC distribution
FE7Chip09All
Entries 184788
Mean 1024
RMS 3262
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000


FE7, Chip 9, ADC distribution
FE7Chip09Ped
Entries 184788
Mean -15.11
RMS 1.414
Underflow 0
Overflow 1.701e+04
10^5
10^4
10^3
10^2
10
-200
-150
-100
-50
0
50
100
150
200

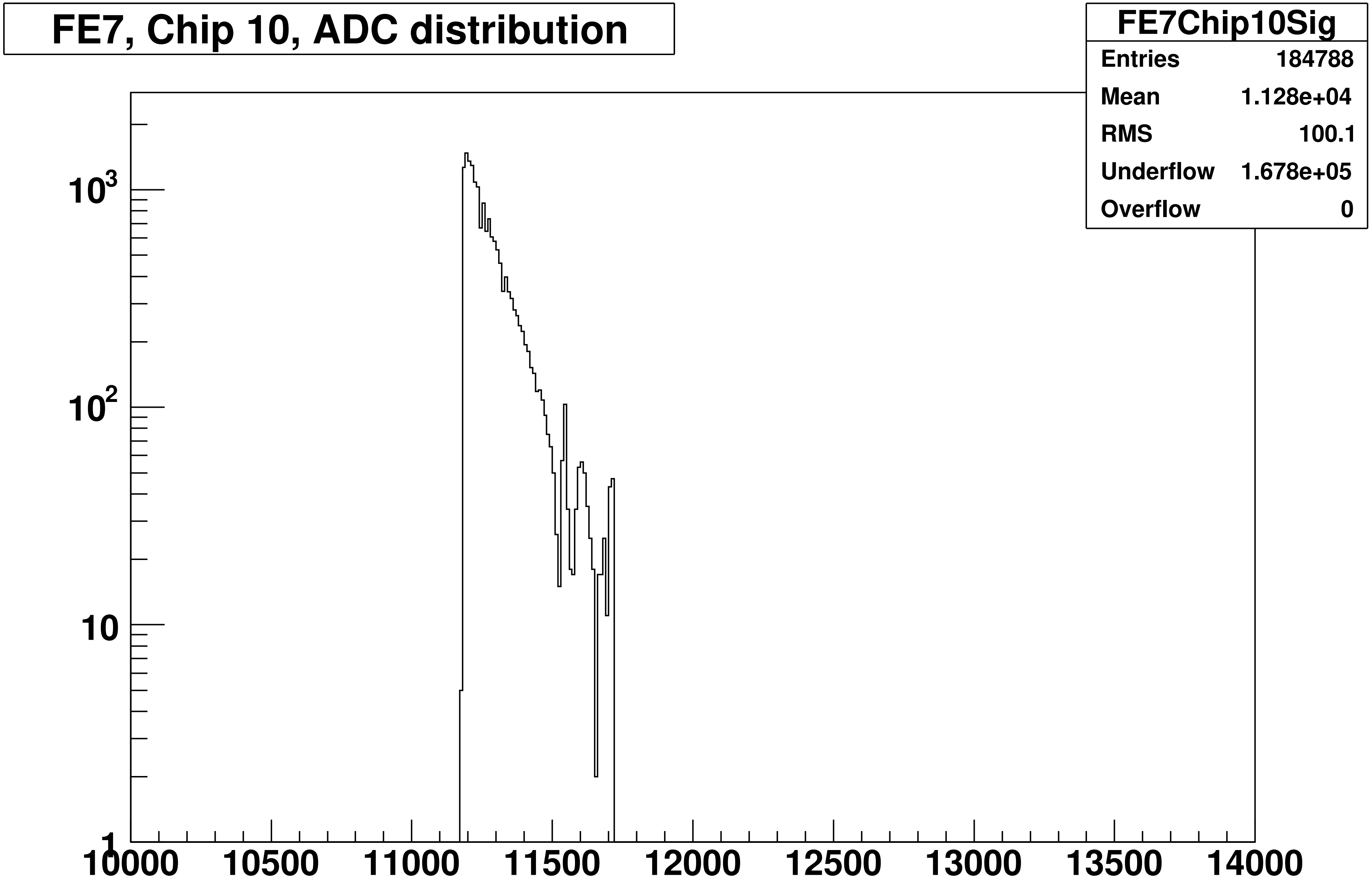

FE7, Chip 9, ADC distribution
FE7Chip09Sig
Entries 184788
Mean 1.127e+04
RMS 100.2
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
10000
10500
11000
11500
12000
12500
13000
13500
14000

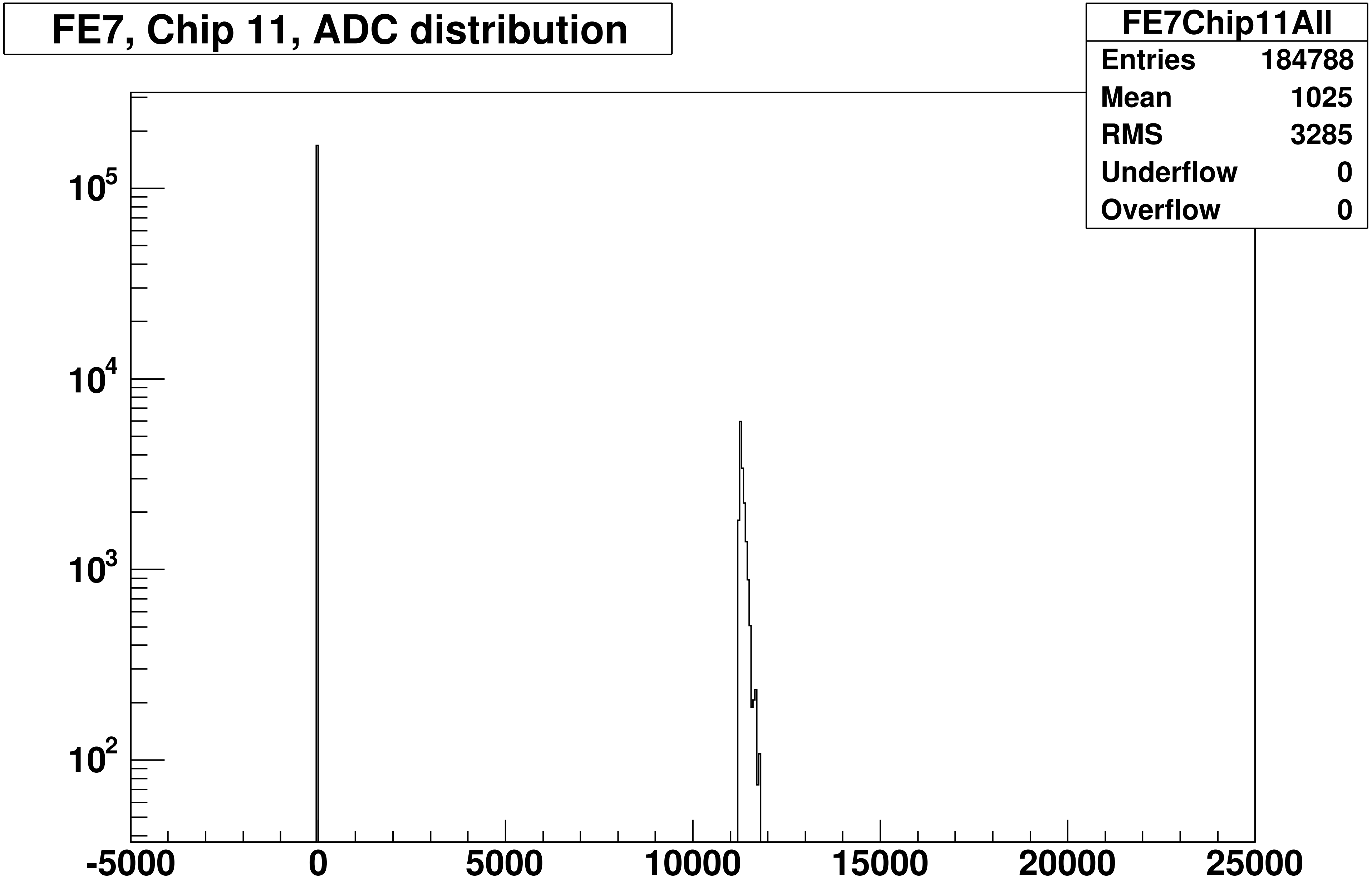


FE7, Chip 10, ADC distribution
FE7Chip10All
Entries 184788
Mean 1052
RMS 3258
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

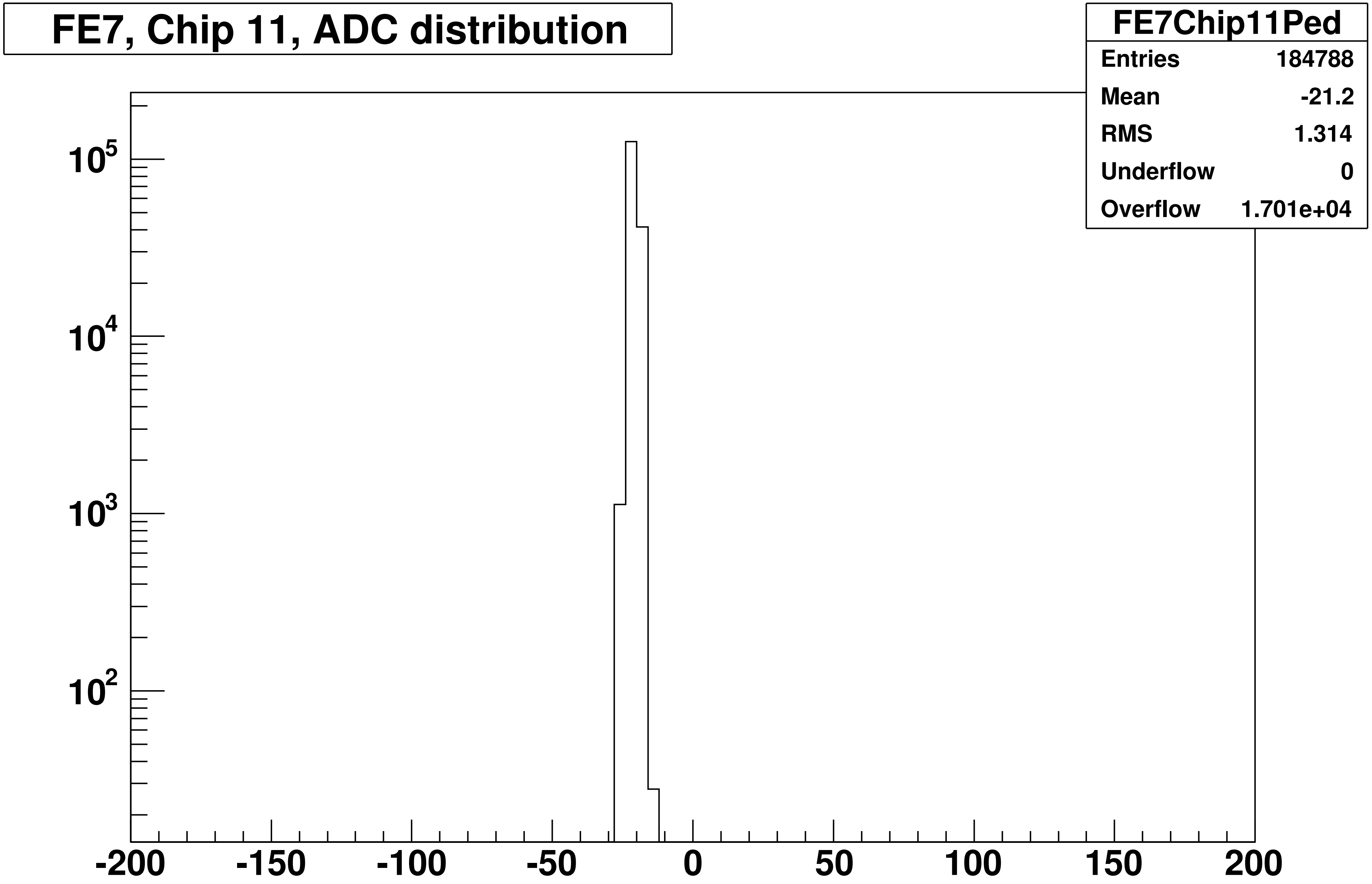


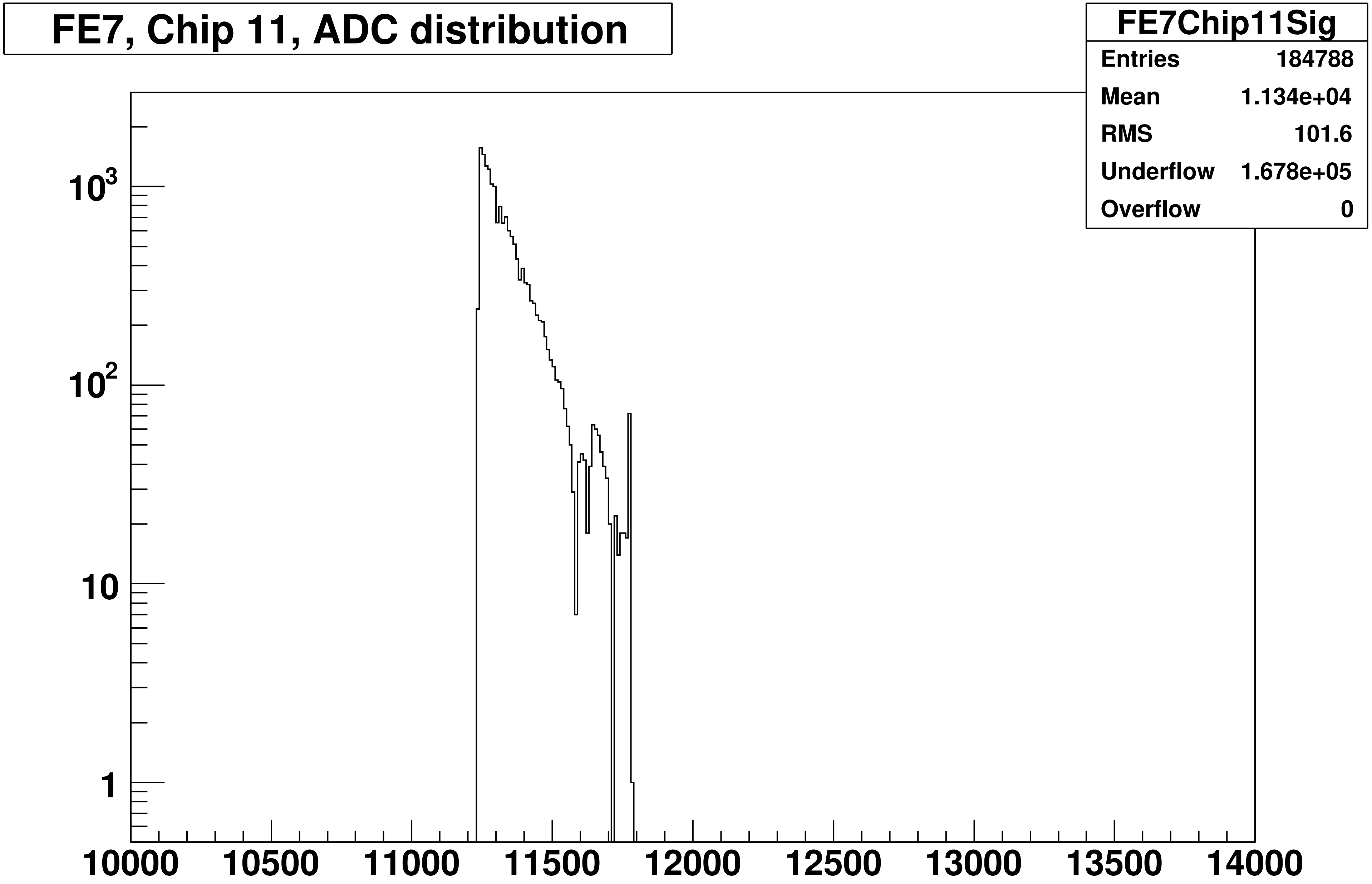
FE7, Chip 10, ADC distribution
FE7Chip10Ped
Entries 184788
Mean 14.28
RMS 1.361
Underflow 0
Overflow 1.701e+04
10
10^2
10^3
10^4
10^5
-200
-150
-100
-50
0
50
100
150
200

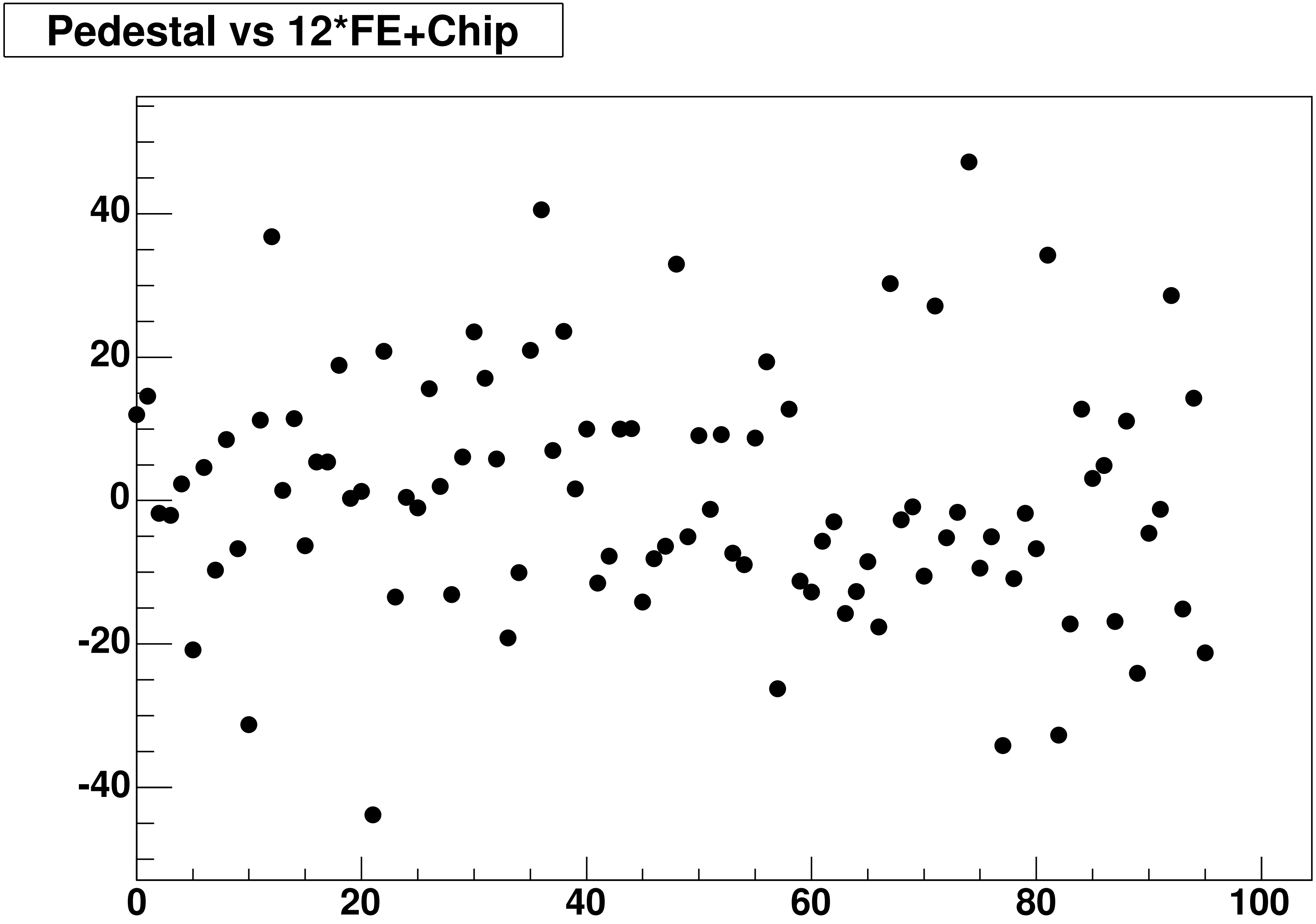

FE7, Chip 10, ADC distribution
FE7Chip10Sig
Entries 184788
Mean 1.128e+04
RMS 100.1
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

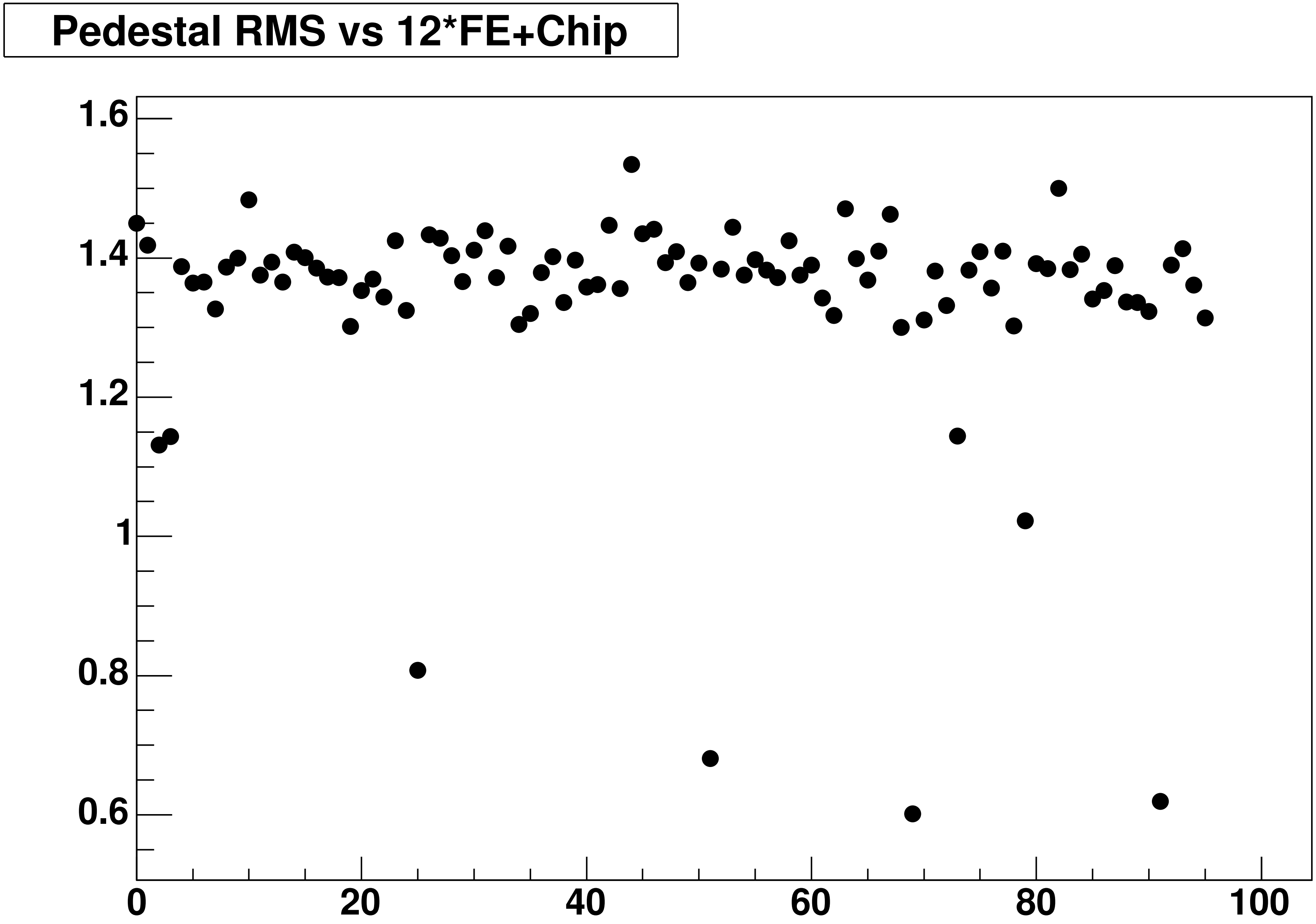


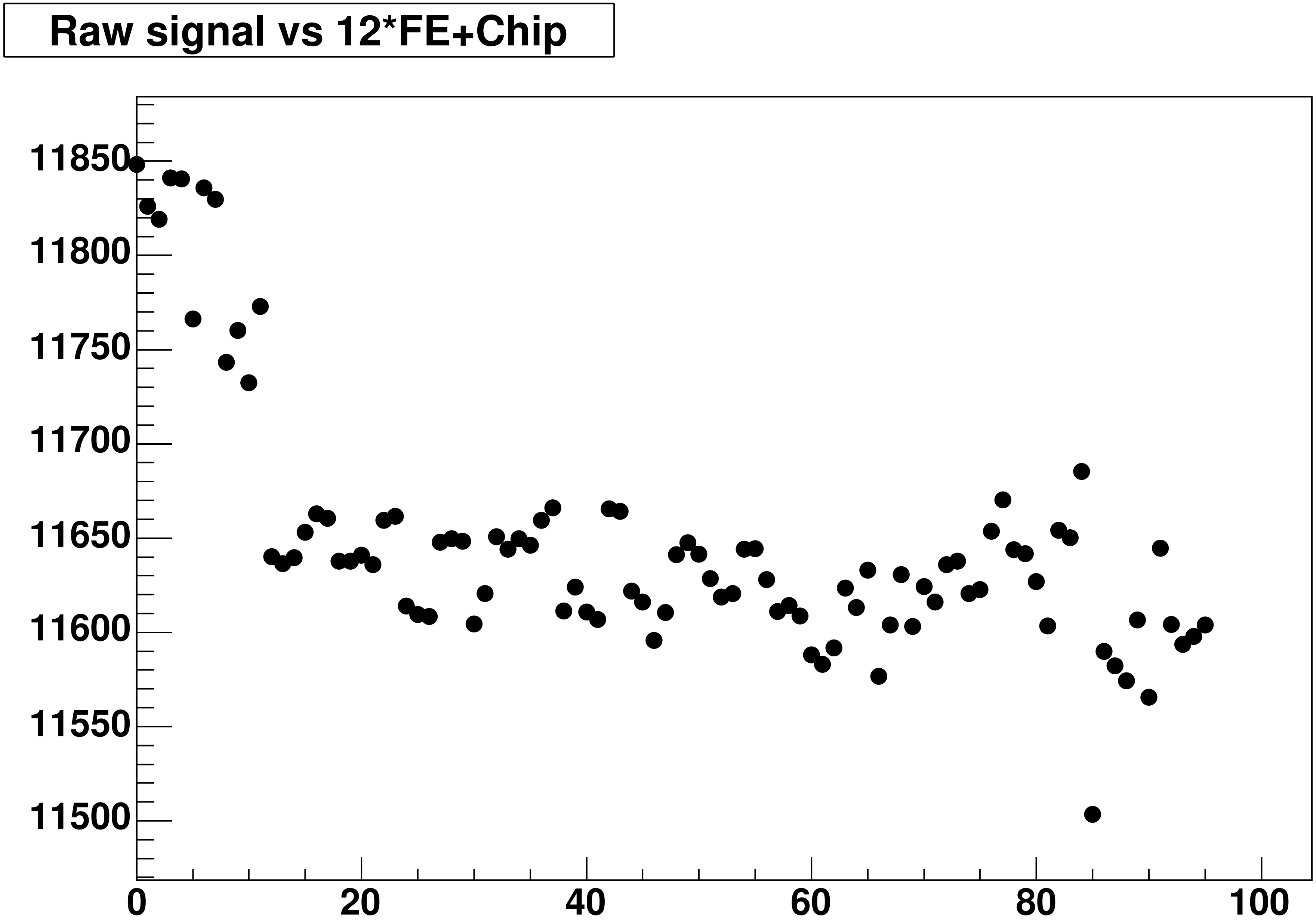
FE7, Chip 11, ADC distribution
FE7Chip11All
Entries 184788
Mean 1025
RMS 3285
Underflow 0
Overflow 0
10^5
10^4
10^3
10^2
-5000
0
5000
10000
15000
20000
25000

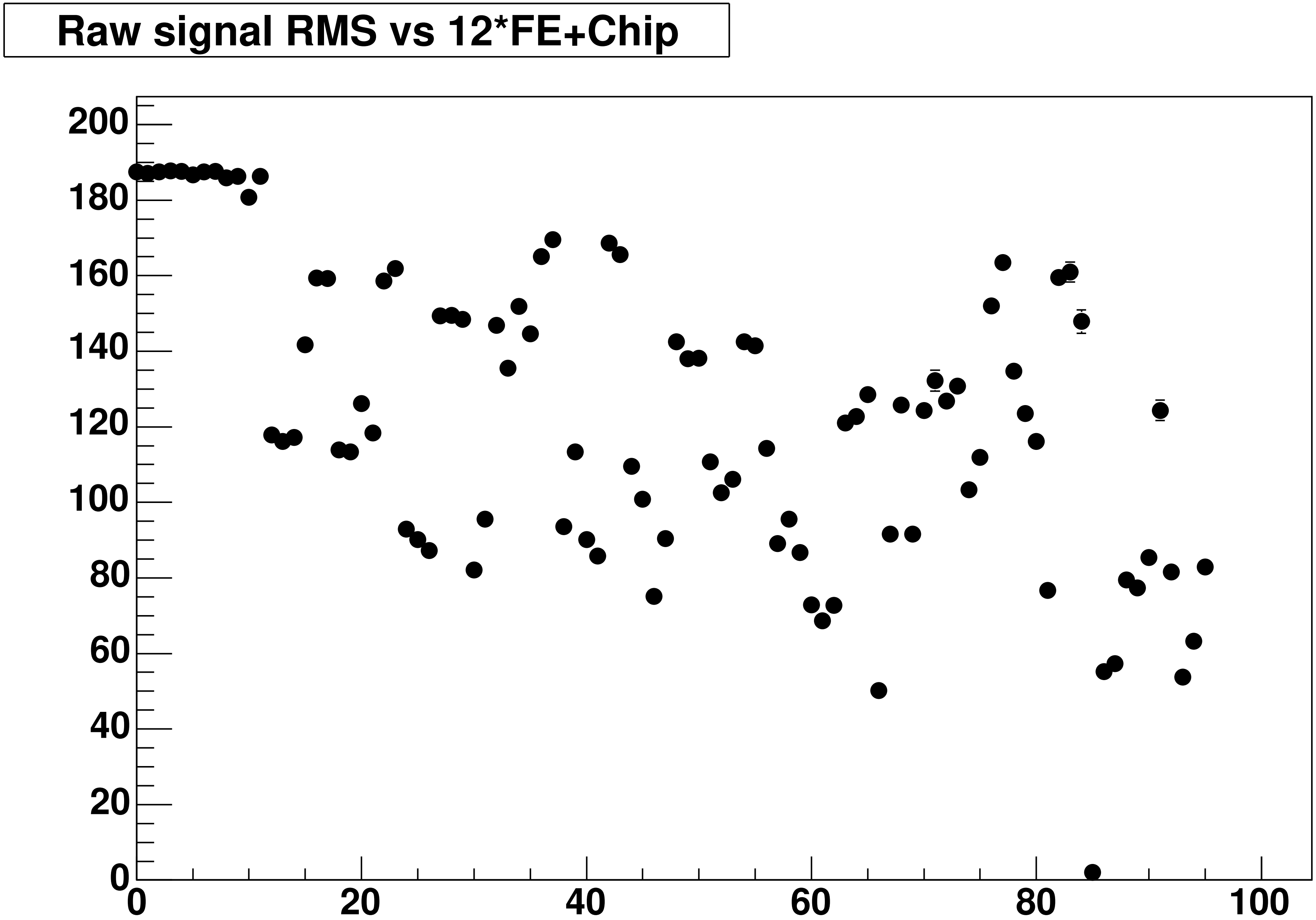

FE7, Chip 11, ADC distribution
FE7Chip11Ped
Entries 184788
Mean -21.2
RMS 1.314
Underflow 0
Overflow 1.701e+04
10^5
10^4
10^3
10^2
-200
-150
-100
-50
0
50
100
150
200

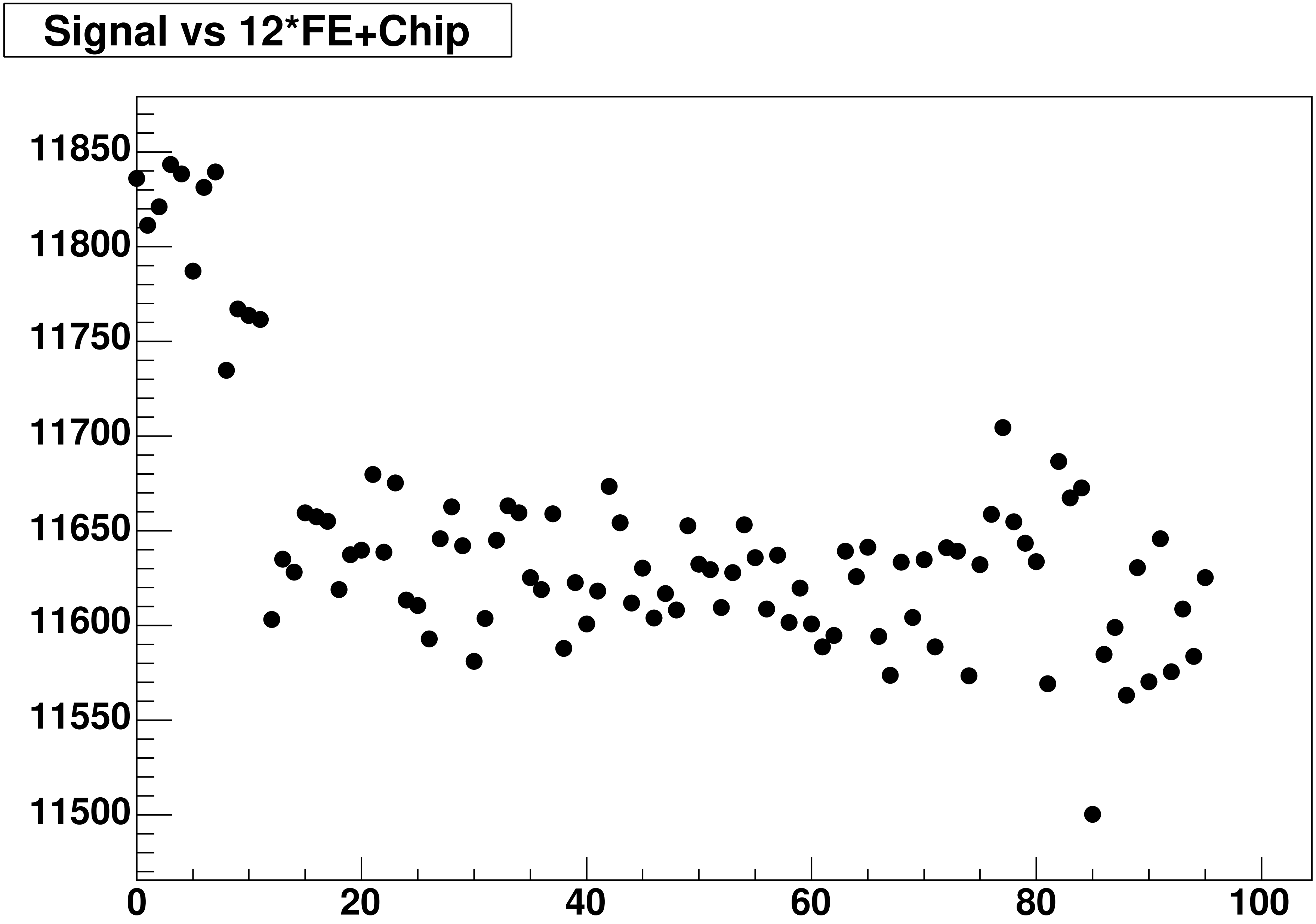

FE7, Chip 11, ADC distribution
FE7Chip11Sig
Entries 184788
Mean 1.134e+04
RMS 101.6
Underflow 1.678e+05
Overflow 0
10^3
10^2
10
1
10000
10500
11000
11500
12000
12500
13000
13500
14000

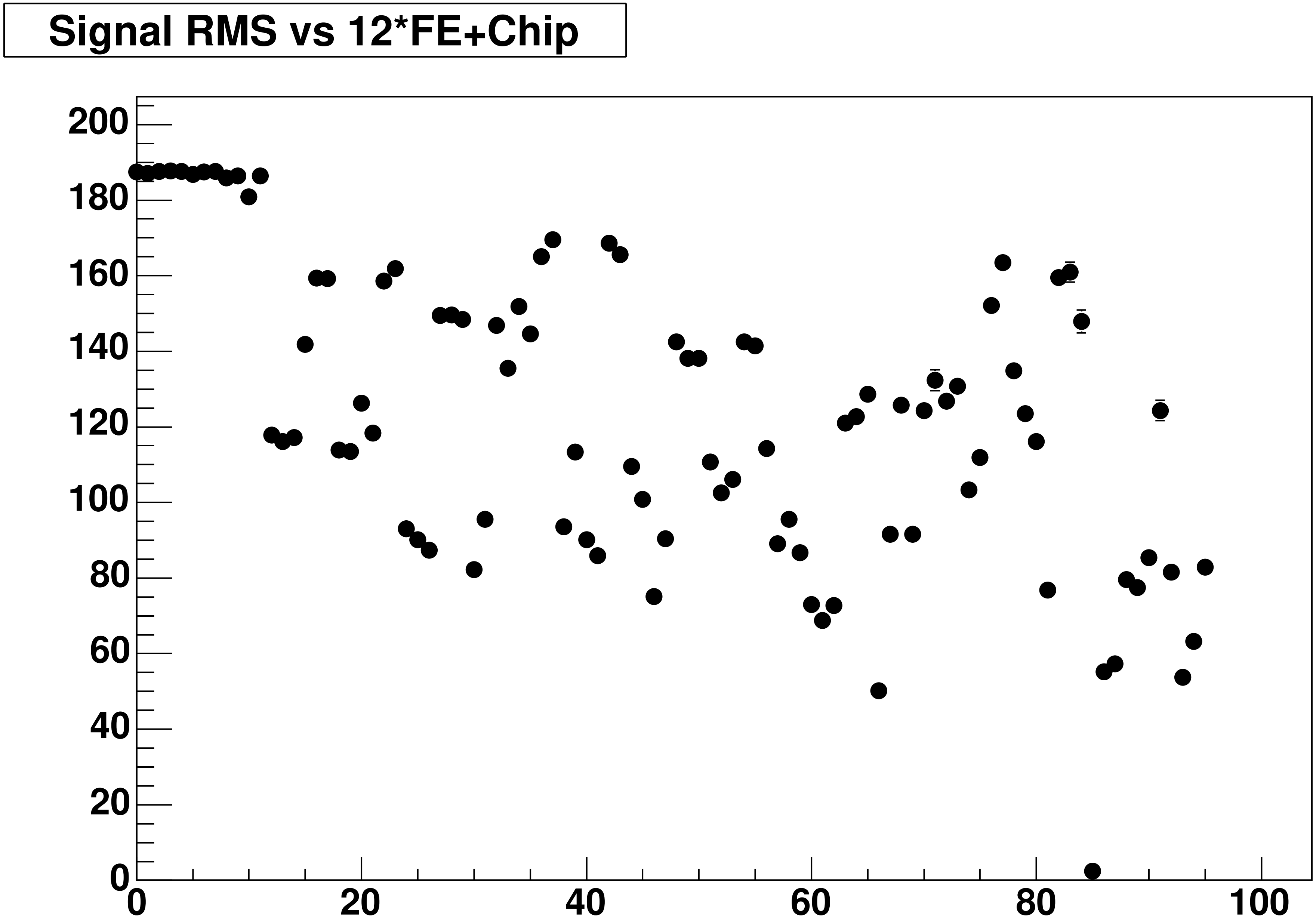

Pedestal vs 12*FE+Chip
40
20
0
-20
-40
0
20
40
60
80
100


Pedestal RMS vs 12*FE+Chip
1.6
1.4
1.2
1
0.8
0.6
0
20
40
60
80
100


Raw signal vs 12*FE+Chip
11850
11800
11750
11700
11650
11600
11550
11500
0
20
40
60
80
100


Raw signal RMS vs 12*FE+Chip
0
20
40
60
80
100
120
140
160
180
200
0
20
40
60
80
100


Signal vs 12*FE+Chip
11850
11800
11750
11700
11650
11600
11550
11500
0
20
40
60
80
100


Signal RMS vs 12*FE+Chip
200
180
160
140
120
100
80
60
40
20
0
0
20
40
60
80
100