Monolithic Active Pixel Sensors

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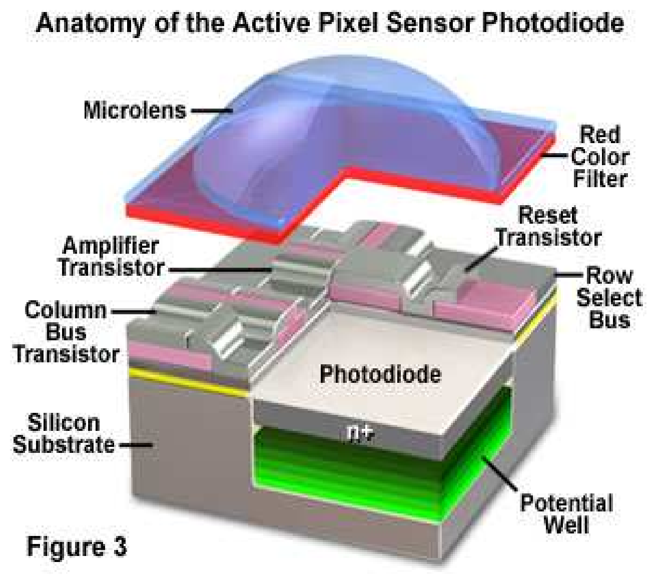
Workpackage 3: MAPS

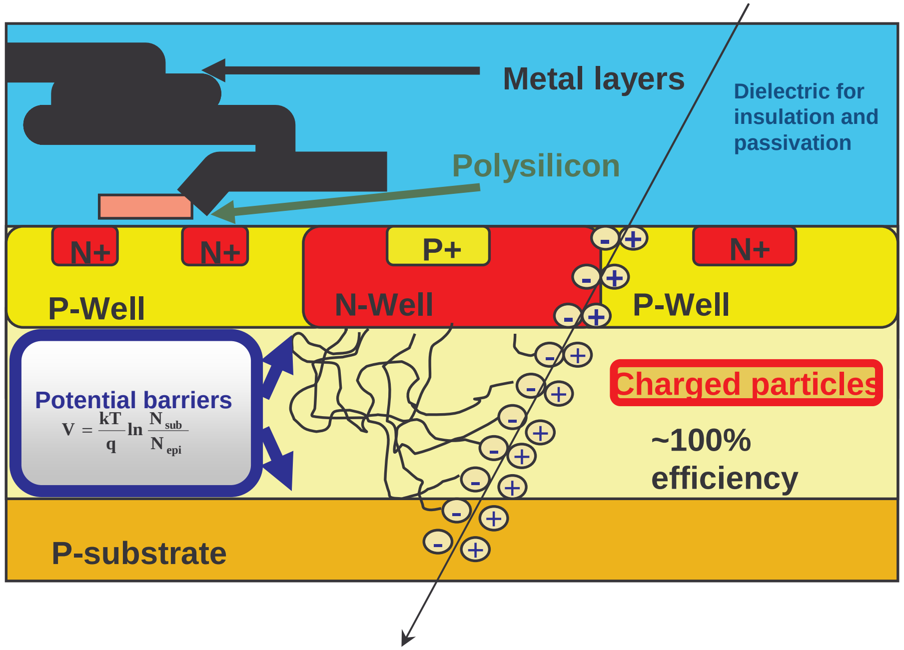
- Who?
  - Birmingham, Imperial, RAL ID, RAL PPD
- Why?
  - Alternative to standard silicon diode pad detectors in ECAL
  - Potential to be cheaper and/or better
- What?
  - Attempt to prove or disprove "MAPS-for-ECAL" concept over next 3 years

- Two-pronged approach: hardware…
  - Two rounds of sensor fabrication and testing, including cosmics and sources
  - Electron beam test, to check response in showers and single event upsets
- …and simulation
  - Model detailed sensor response to EM showers and validate against hardware
  - Simulate effect on full detector performance in terms of PFLOW

MAPS history

- Developed over the last decade
  - Integrates sensitive silicon detector and readout electronics into one device
  - "Camera on a chip"; all-in-one device for light detection
  - Standard CMOS technology

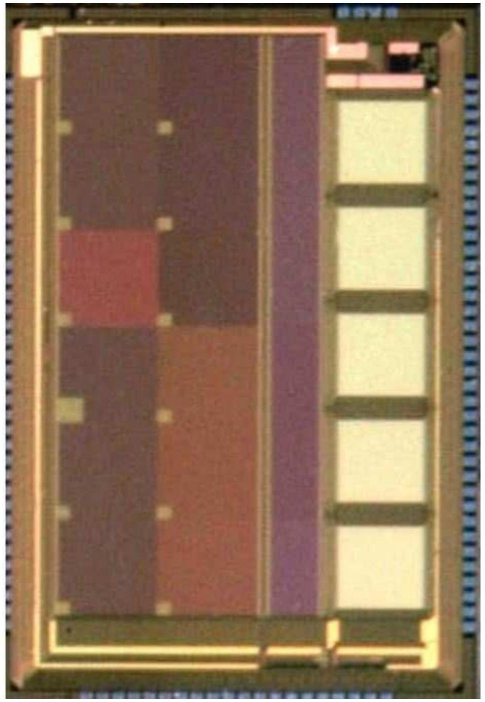


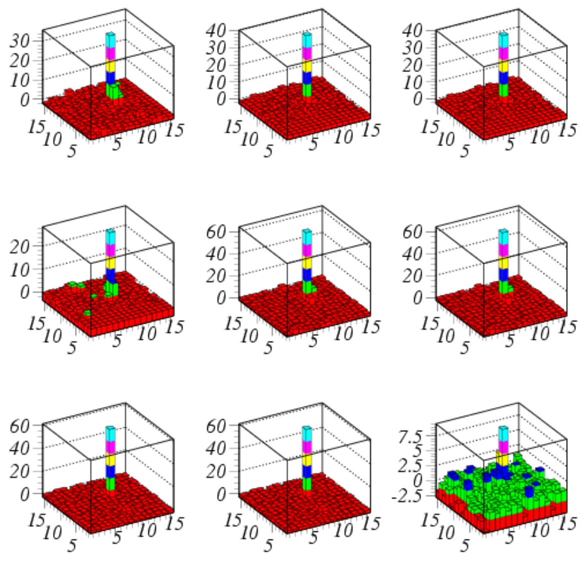


- HEP and space applications more recent
  - Detector for higher energy X/gamma-rays or charged particles
  - Basic principle; collection of liberated charge in thin epitaxial layer just below surface readout electronics

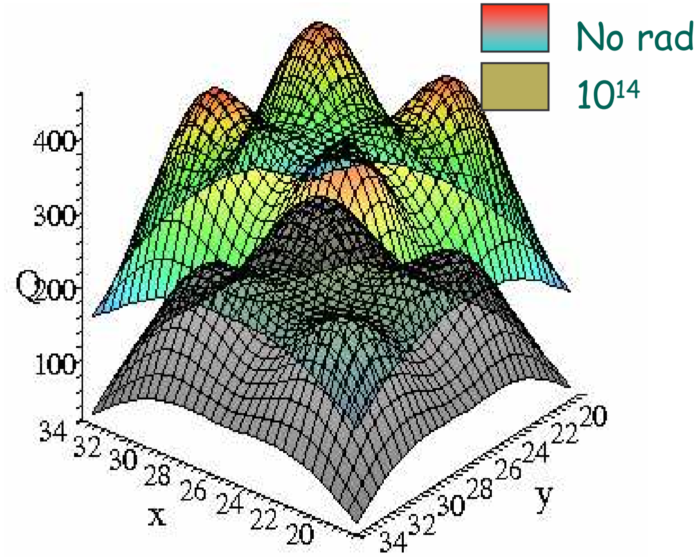
“MAPS for PP&SS” collaboration

- Birmingham, Glasgow, Leicester (→Brunel), Liverpool, RAL
- Two year programme; June 2003 – May 2005
- Simulated and real devices studied
- A lot of experience at RAL in areas directly relevant to us



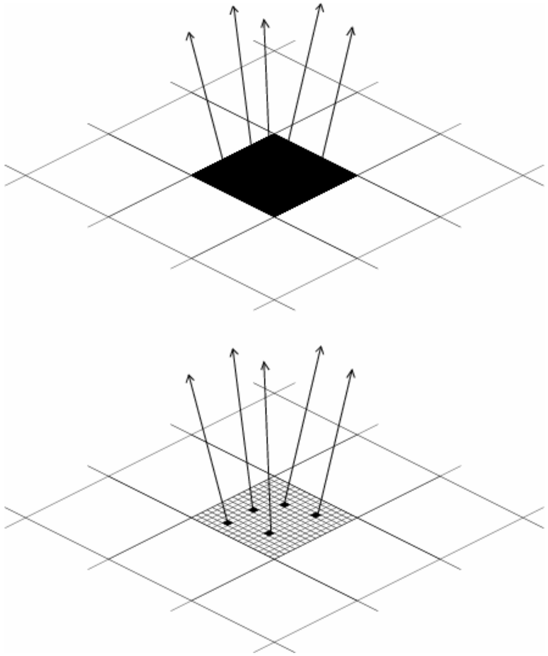


Measurements of S/N with ^{106}Ru

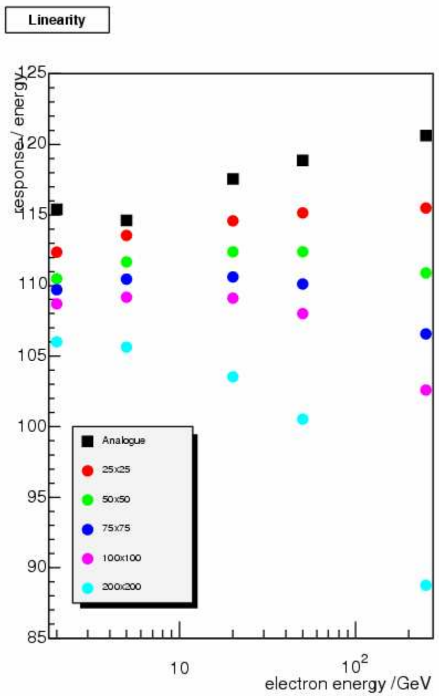


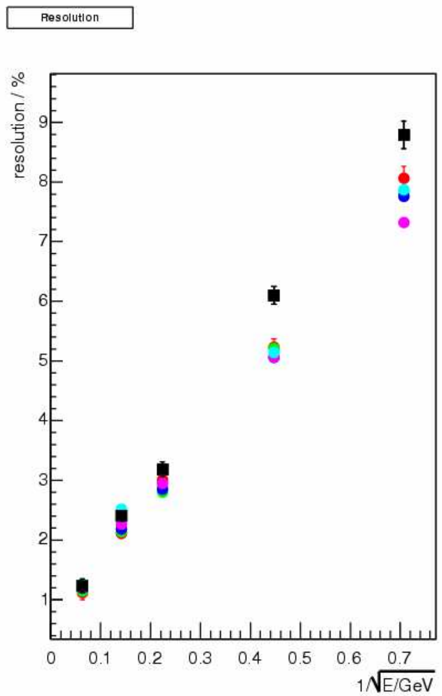
Simulation of charge collection with 4-diode structure before/after irradiation

Basic concept for ECAL



- Replace 1×1 cm^2 diode pads with much smaller pixels
  - Make pixels small enough that at most one particle goes through each
  - Then only need threshold to say if pixel hit or not; "binary" readout, i.e. DECAL

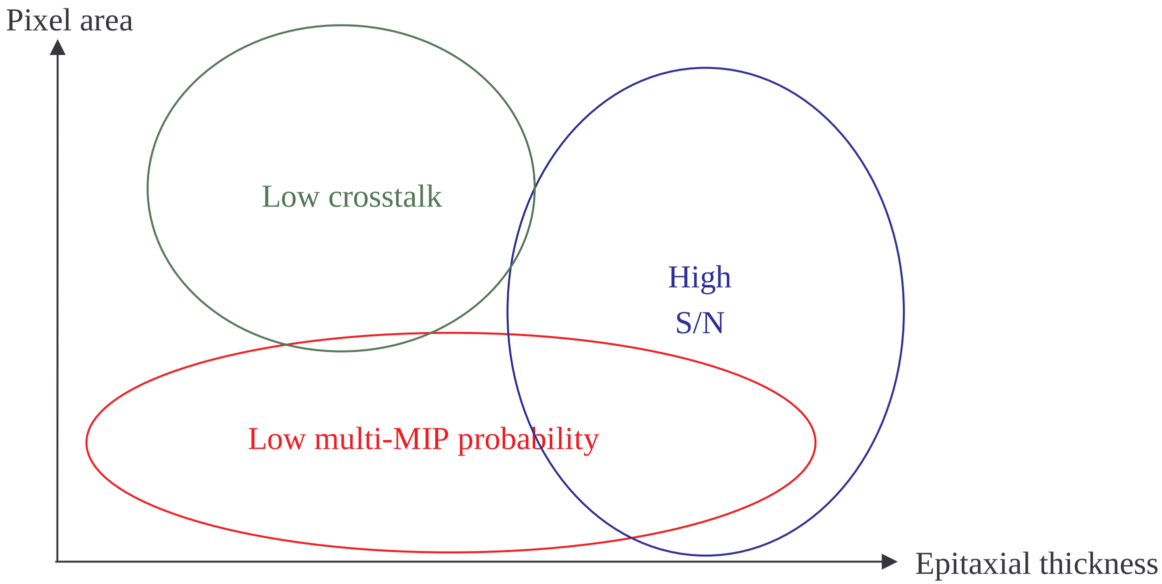




- How small is small?
  - EM shower core density at 500GeV is ~100/mm^2
  - Pixels must be < 100×100μm^2; working number is 50×50μm^2
  - Gives ~10^{12} pixels for ECAL!

Pixel analogue optimisation

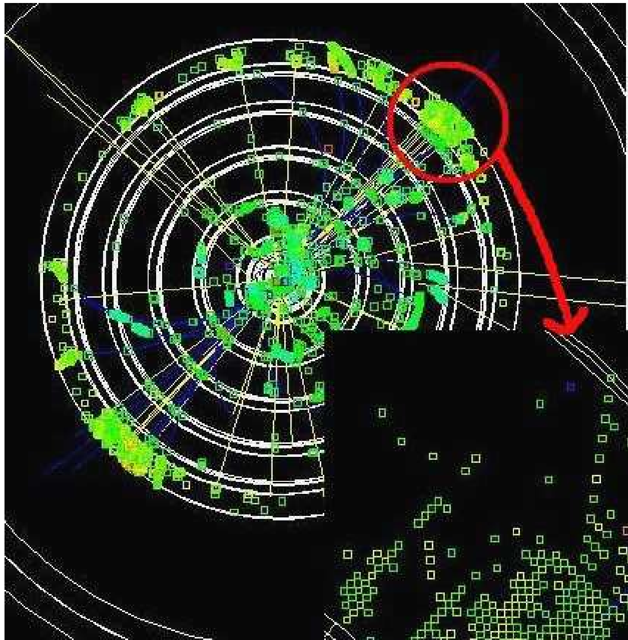
- Studies are needed on
  - Charge sharing (crosstalk), MIP S/N, MIP multiple hits/pixel
  - Dependent on pixel area, epitaxial thickness, threshold, diode geometry, etc



- Noise rate target < 10^{-6} (~5σ); DAQ could handle (at least) ~10^{-5}
- Large parameter space; need to find best combination
  - Sensor-level simulation to interpolate between sensor measurements
  - Physics-level simulation needed to guide choices

Physics MC studies in progress

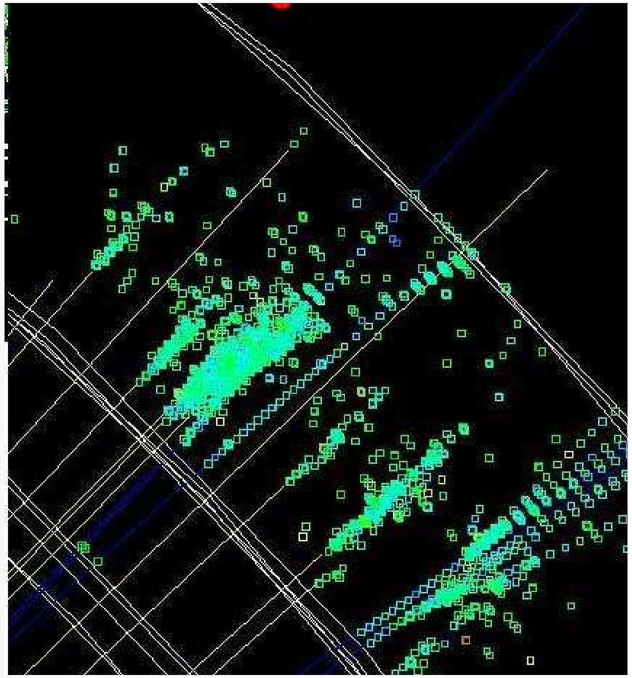
- By eye, pixels look very good compared with diodes
  - But can be deceptive as analogue information not easily apparent in diode picture
  - Quantitative comparison needed



Same event

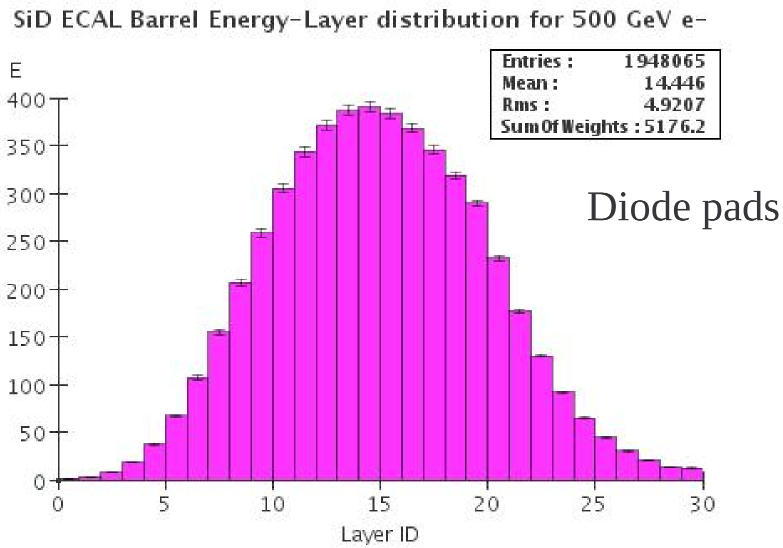
Diode pads

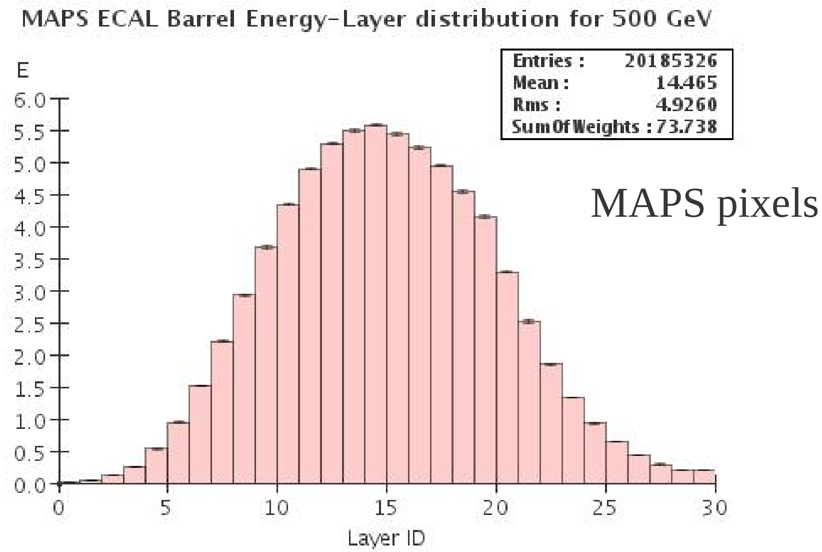
MAPS pixels



MC studies (cont)

- Compare electron resolution up to 500 GeV
  - Resolutions very similar for diode and MAPS
  - Mainly dominated by fundamental EM shower fluctuations?





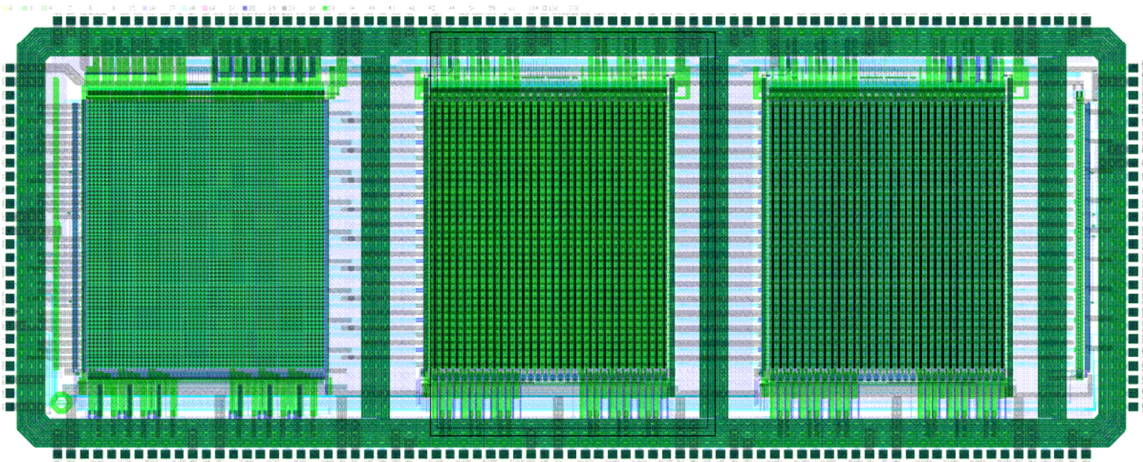
- Need to build up to comparison of ECALs using hadronic jets with realistic PFLOW algorithm
  - Need very flexible PFLOW code to handle both ECALs
  - Much work to be done before this study can be completed

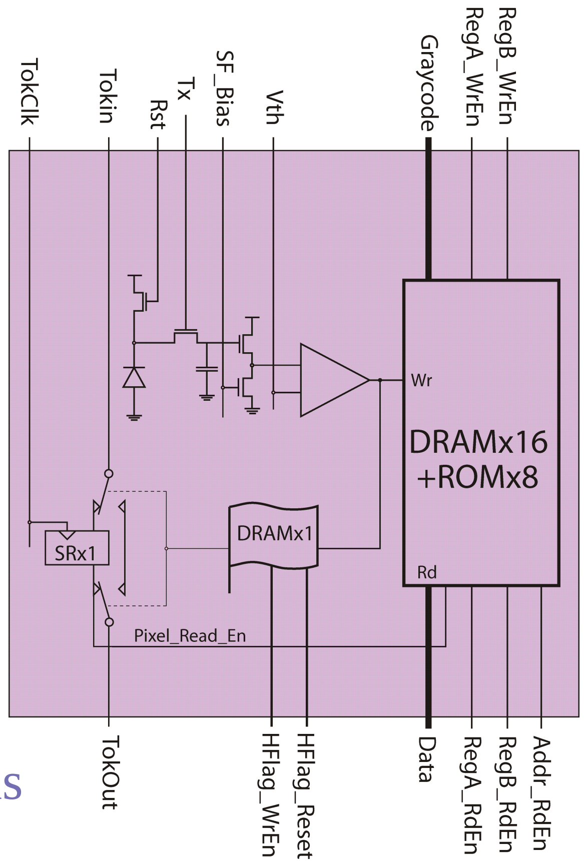
Readout concept

- In reality, will not have single event at a time
  - ILC will have multiple beam crossings per train
- Buffer results within bunch train, readout between trains
  - Must do threshold discrimination for each beam crossing in train
  - Store results in on-pixel memory until end of train and then flush out
- Could be up to 5000 beam crossings per train
  - Not feasible to build 5kbits of memory into a $50\times50\mu m^2$ pixel
  - Assume rate is low and only store beam crossing numbers when hit
  - Memory is then 2 bytes $\times$ maximum number of crossings allowed
- Must know hit rate to determine maximum memory needed
  - Presumably dominated by one or more of: beam-induced background, Bhabhas, mini-jets, pixel noise
  - Need good estimates of rates of each of these; overlap with WP5

MI^3 Collaboration

- Wide ranging (not just PPARC), Basic Technology development
- RAL ID a major contributor
  - Design centre for CMOS sensors and leading group in DAQ

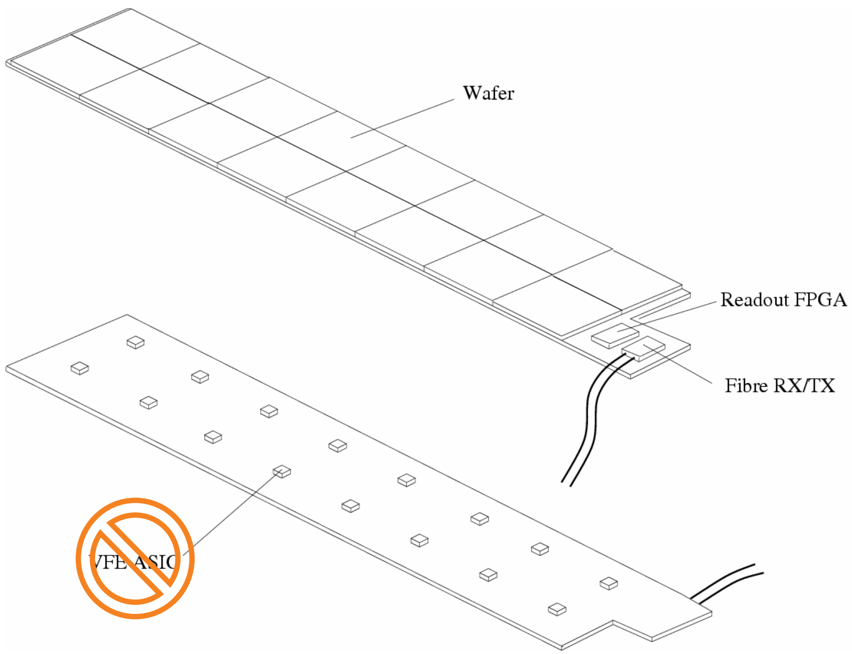




- Current design (by J.Crooks, also on CALICE)
  - Many similar features to ILC ECAL requirements…
  - …but several differences also
  - Sensors fabricated and under test over next few months
  - Valuable experience before starting CALICE design

ECAL as a system

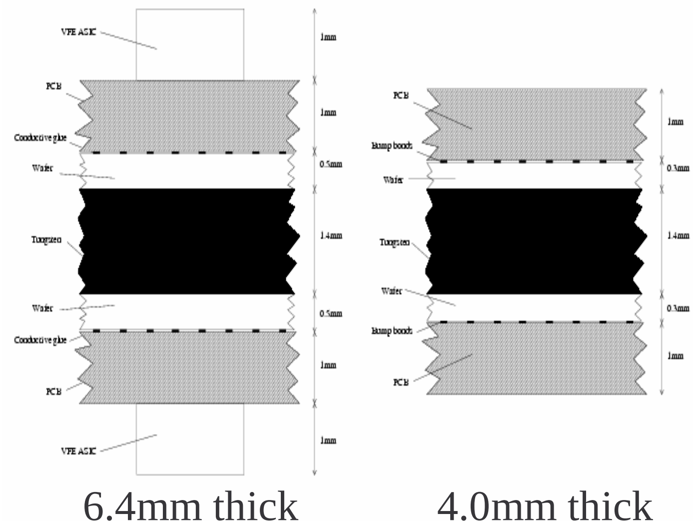
- Replace diode pad wafers and VFE ASICs with MAPS wafers
  - Mechanically very similar; overall design of structure identical
  - DAQ very similar; FE talks to MAPS not VFE ASICs
    - Both purely digital I/O, data rates within order of magnitude

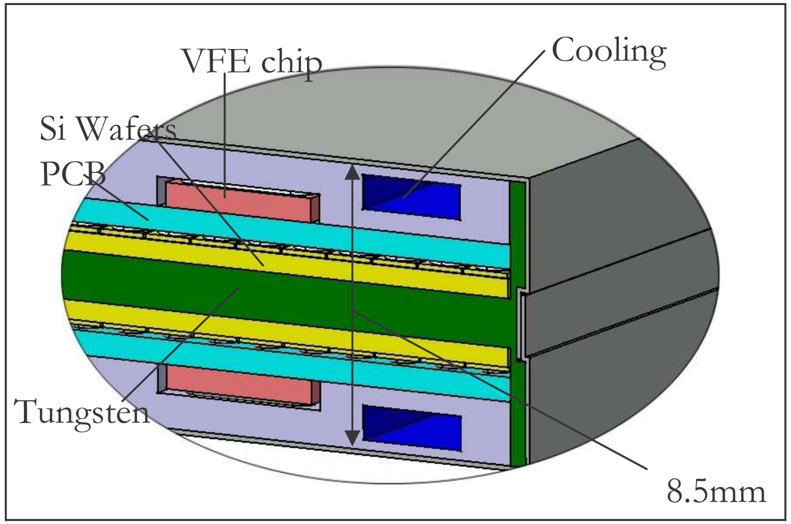


- Aim for MAPS to be a “swap-in” option without impacting too much on most other ECAL design work
- Requires sensors to be glued/solder-pasted to PCB directly
  - No wirebonds; connections must be routed on sensor to pads above pixels
  - New technique needed which is part of our study

Potential advantages

- Slab thinner due to missing VFE ASICs
  - Improved effective Moliere radius (shower spread)
  - Reduced size (=cost) of detector magnet and outer subdetectors





- Thermal coupling to tungsten easier
  - Most heat generated in VFE ASIC or MAPS comparators
  - Surface area to slab tungsten sheet ~1cm^2 for VFE ASIC, ~100cm^2 for final MAPS

- **COST!** Standard CMOS should be cheaper than high resistivity silicon
  - No crystal ball for 2012 but roughly a factor of two different now
  - TESLA ECAL wafer cost was 90M euros; 70% of ECAL total of 133M euros
  - That assumed 3euros/cm^2 for 3000m^2 of processed silicon wafers

Other requirements

- Also need to consider power, uniformity and stability
  - Power must be similar (or better) that VFE ASICs to be considered
    - Main load from comparator; ~2.5μW/pixel when powered on
    - Investigate switching comparator; may only be needed for ~10ns
    - Would give averaged power of ~1nW/pixel, or 0.2W/slab
    - There will be other components in addition
    - VFE ASIC aiming for 100μW/channel, or 0.4W/slab
  - Unfeasible for threshold to be set per pixel
    - Prefer single DAC to set a comparator level for whole sensor
    - Requires sensor to be uniform enough in response of each pixel
    - Possible fallback; divide sensor into e.g. four regions
  - Sensor will also be temperature cycled, like VFE ASICs
    - Efficiency and noise rate must be reasonably insensitive to temperature fluctuations
    - More difficult to correct binary readout downstream

Planned programme

- Two rounds of sensor fabrication
  - First with several pixel designs, try out various ideas
  - Second with uniform pixels, iterating on best design from first round
- Testing needs to be thorough
  - Device-level simulation to guide the design and understand the results
  - “Sensor” bench tests to study electrical aspects of design
  - Sensor-level simulation to check understanding of performance
  - “System” bench tests to study noise vs. threshold, response to sources and cosmics, temperature stability, uniformity, magnetic field effects, etc.
  - Physics-level simulation to determine effects on ECAL performance
- Verification in a beam test
  - Build at least one PCB of MAPS to be inserted into pre-prototype ECAL
  - Replace existing diode pad layer with MAPS layer
  - Direct comparison of performance of diode pads and MAPS

First draft of schedule

		FY	5/6			FY	6/7			FY	7/8			FY	8/9	
	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Feasibility study	=	=	=													
Design 1				=	=	=	=									
Fabrication 1								=	=							
Basic tests 1									=							
Detailed tests 1									=	=	=	=				
Design 2										=	=					
Fabrication 2												=	=			
Basic tests 2													=			
Detailed tests 2													=	=	=	=
Beam test PCB											=	=	=	=		
Beam test															=	=

Schedule implications

- Design starting 6 months later than originally planned
  - Limit on RAL ID staff effort in FY05/06
- First fabrication and testing starting 6-9 months later
  - Limit on equipment funds in FY06/07
- Second fabrication and testing starting 9 months later
  - Knock-on effects from above
- Beam test starting 9 months later also
  - Would be ready from Oct 2008
  - Misses scheduled CALICE beam tests at CERN and FNAL
  - Have to arrange for specific ECAL+MAPS beam test (at DESY?)

Conclusions

- Basic idea of MAPS seems feasible so far
  - No showstoppers identified (yet!)
- Will continue conceptual study until end of year
  - Had first meeting last week
- Design and fabrication of real sensors will follow
  - RAL/ID effort funded from Jan 2006
- Simulation studies are needed in parallel
  - RAL/PPD will do sensor simulation
  - Good start at Birmingham already on physics studies
  - New RAs at Birmingham and Imperial should contribute soon