

# Off-Detector Receiver

- Receives data from front end
- Buffer data
- Makes data available to DAQ software

# Features of input

- High input data rate
  - Greater than 100MB/s
- Low average data rate
  - ~10MB/s

# Consequences of input data rates & size

- Off detector receiver needs to be able to buffer the whole of the data on the link for each spill (to avoid upstream buffering)
- Is 128MB per link enough

# Input Technologies

- Input rate achievable with existing technologies
  - Single or multiple Gigabit ethernet
  - 10 Gigabit ethernet

# Input data Format

- Header containing
  - Event ID
  - Source ID (for debugging and if source likely to change)
  - Beginning of data
  - End of data or Length of data

# Data processing

- Data processing (compression) can be inserted into data stream in the FPGA
- This reduces output data rates and allows more channels to be written to single storage system

# Output data presentation

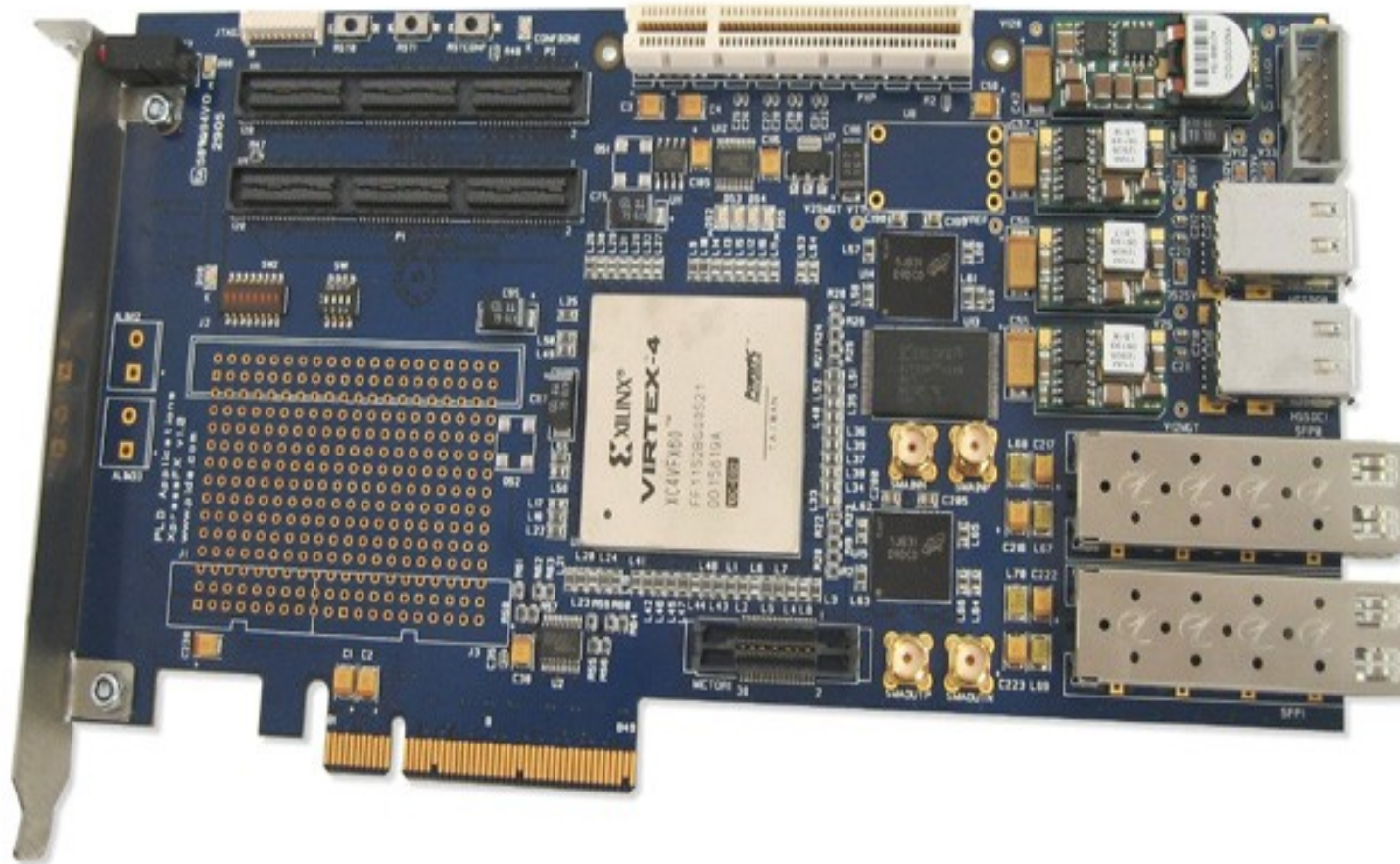
- Data written to hard disk array
- Data written to memory disk
- Data written to custom memory array
- Data written to remote disk or system

# Output data format

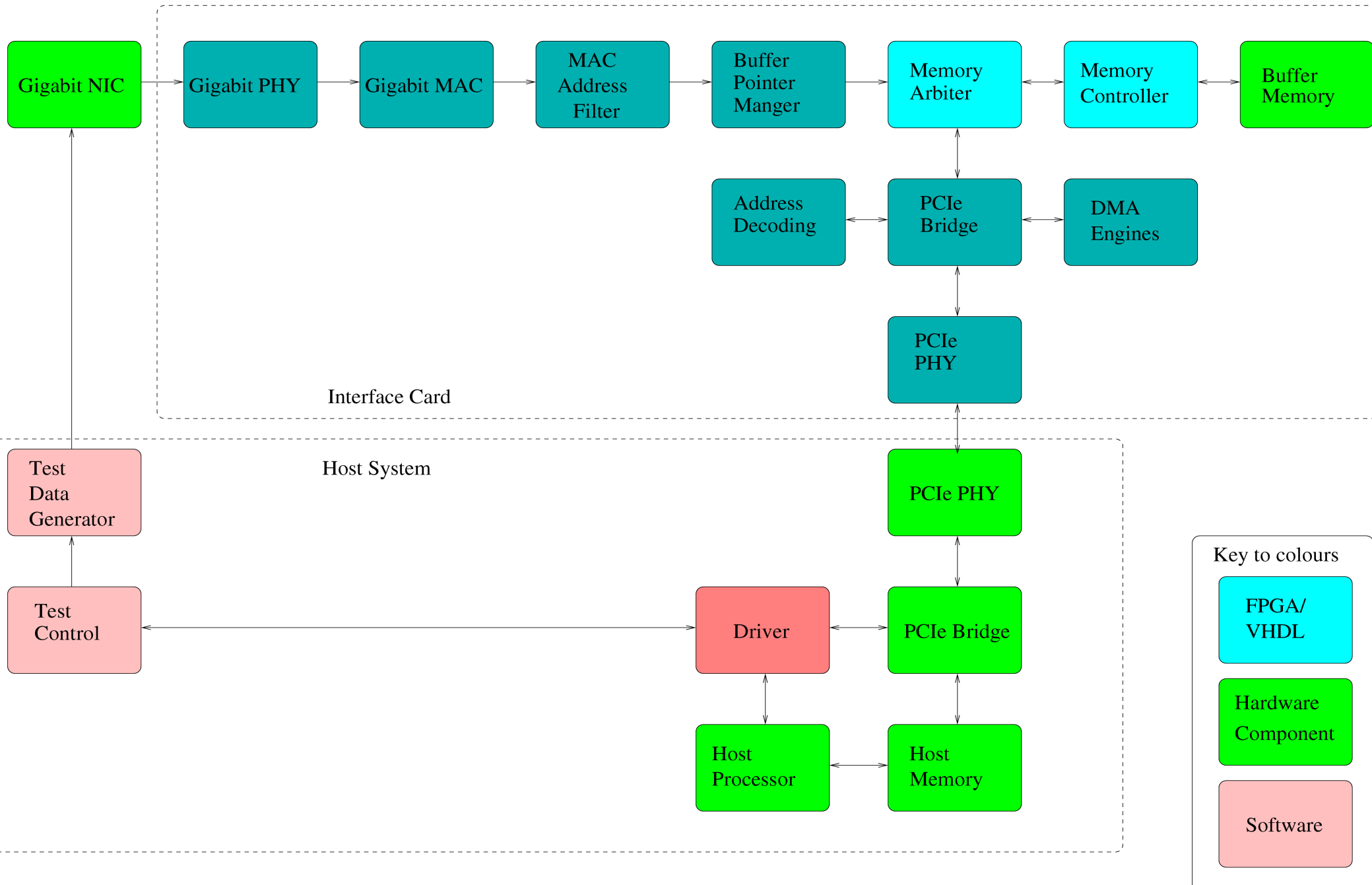
- Data stored on disk index by event ID
- Directory entry = event ID
- Alternative



# Off-Detector Receiver Prototype platform



# Off-Detector Receiver



# Off Detector Receiver Status

- Prototype cards received
- Gigabit MAC core implemented
- PCI express core implemented
- DMA engine implemented
- Memory controller being worked on
- Basic linux driver implemented
- Other logic is straight forward