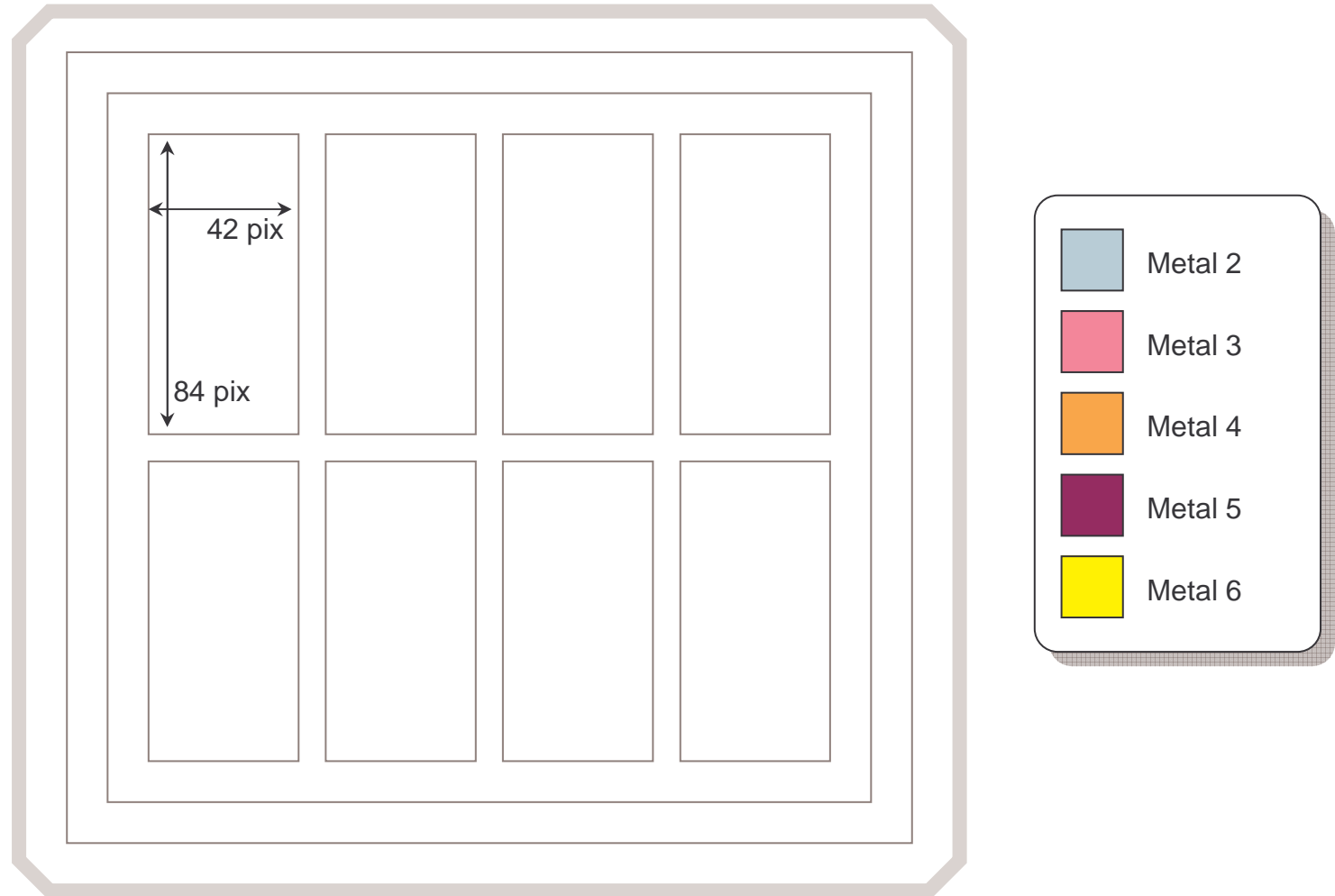
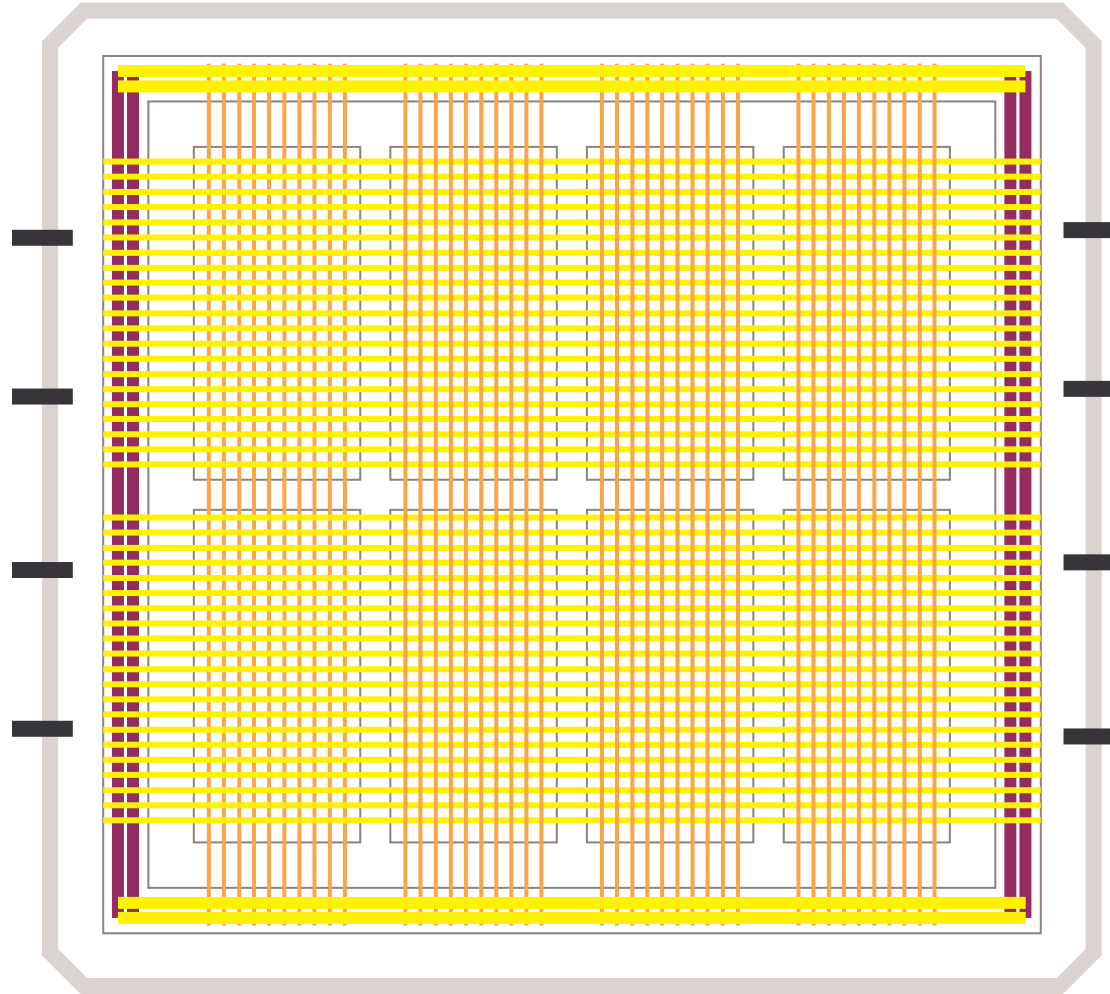


CALICE ASIC1: Power Plan

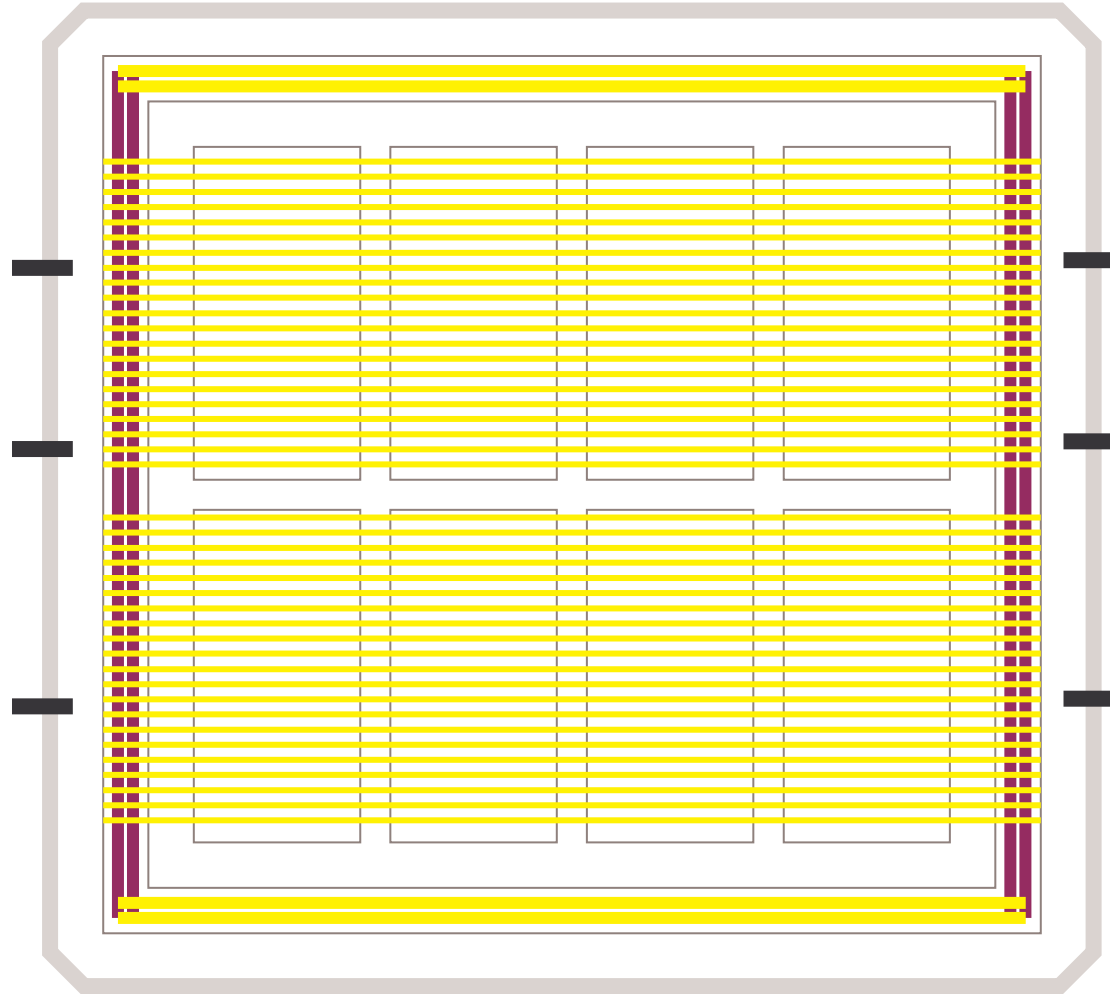


(Top Level)

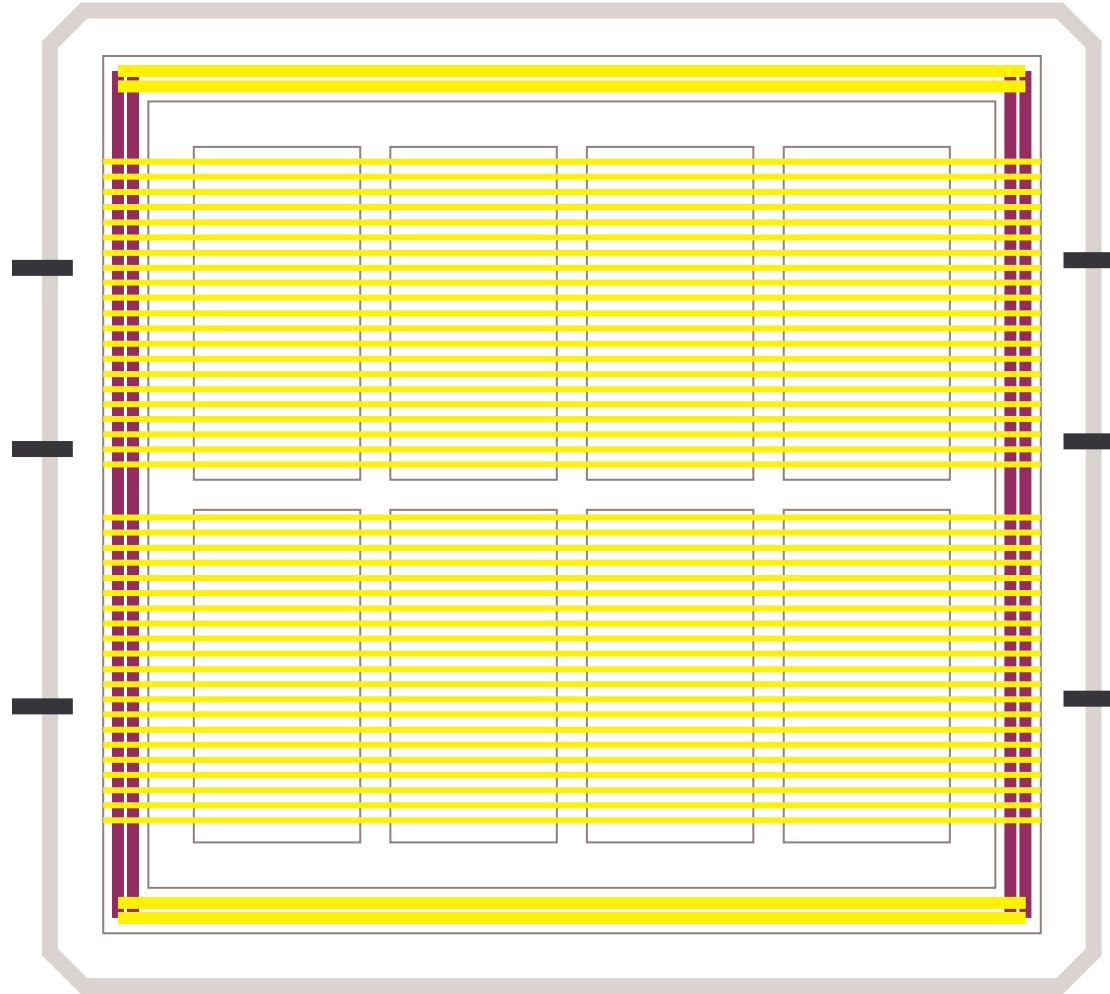
VDD1V8pix & VSS:Gpix



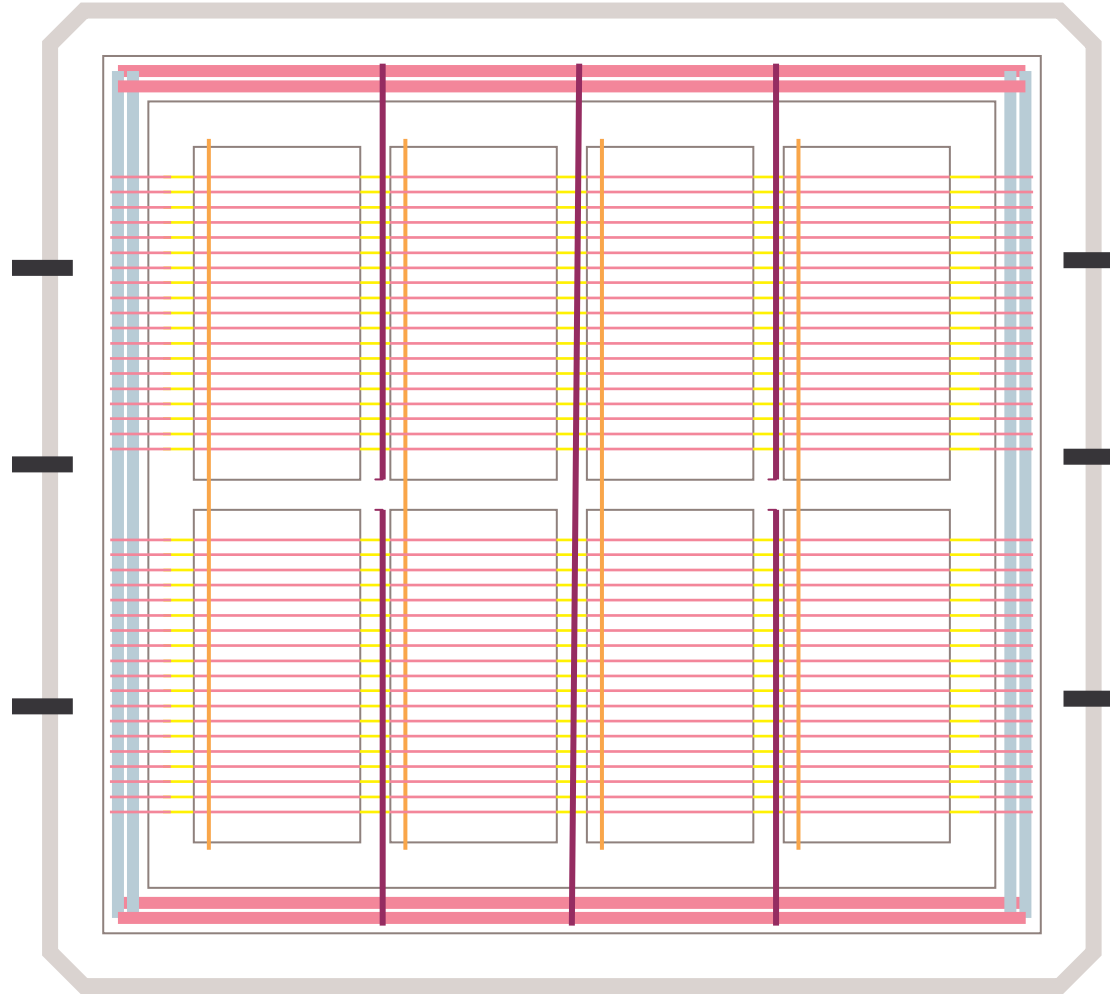
VDD1V8aco & VSS:Gaco



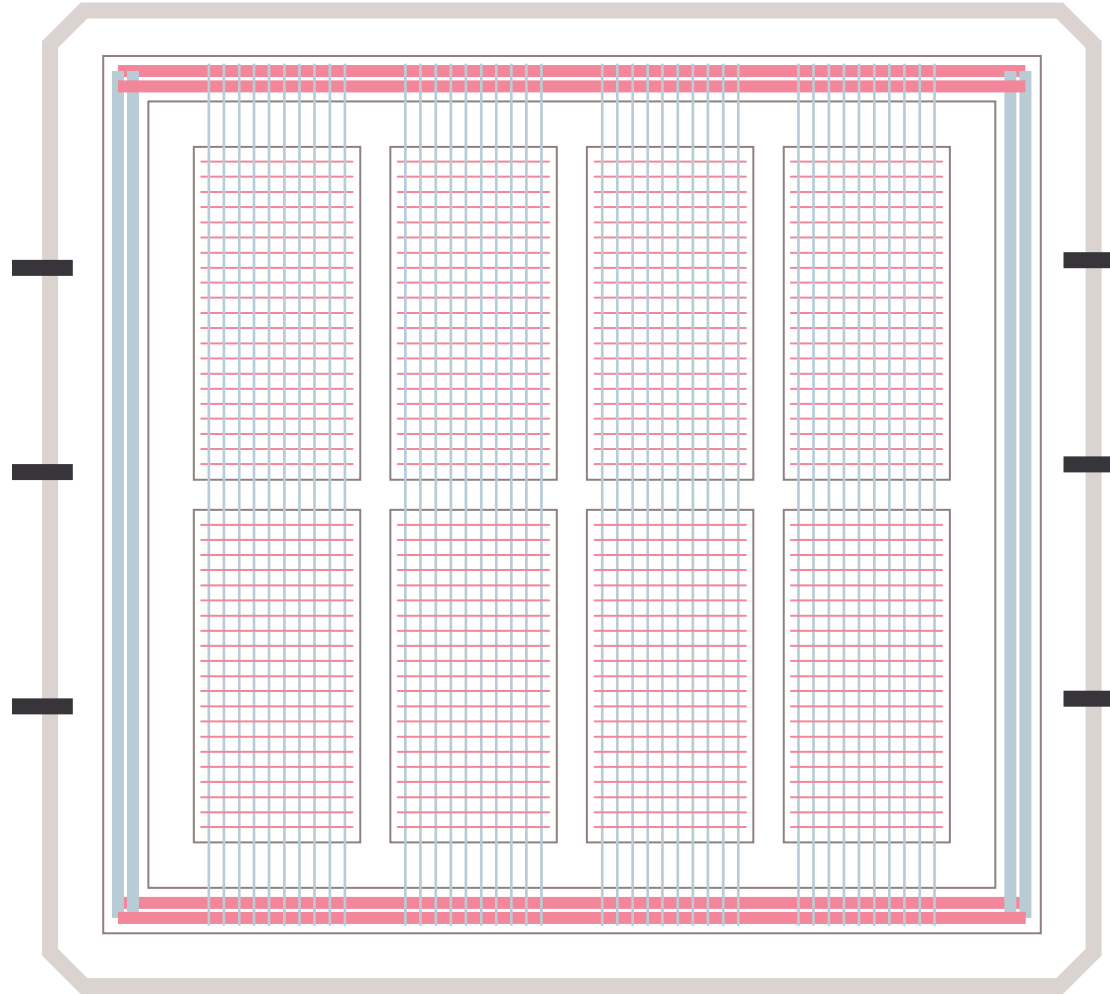
VDD1V8dco & VSS:Gdco



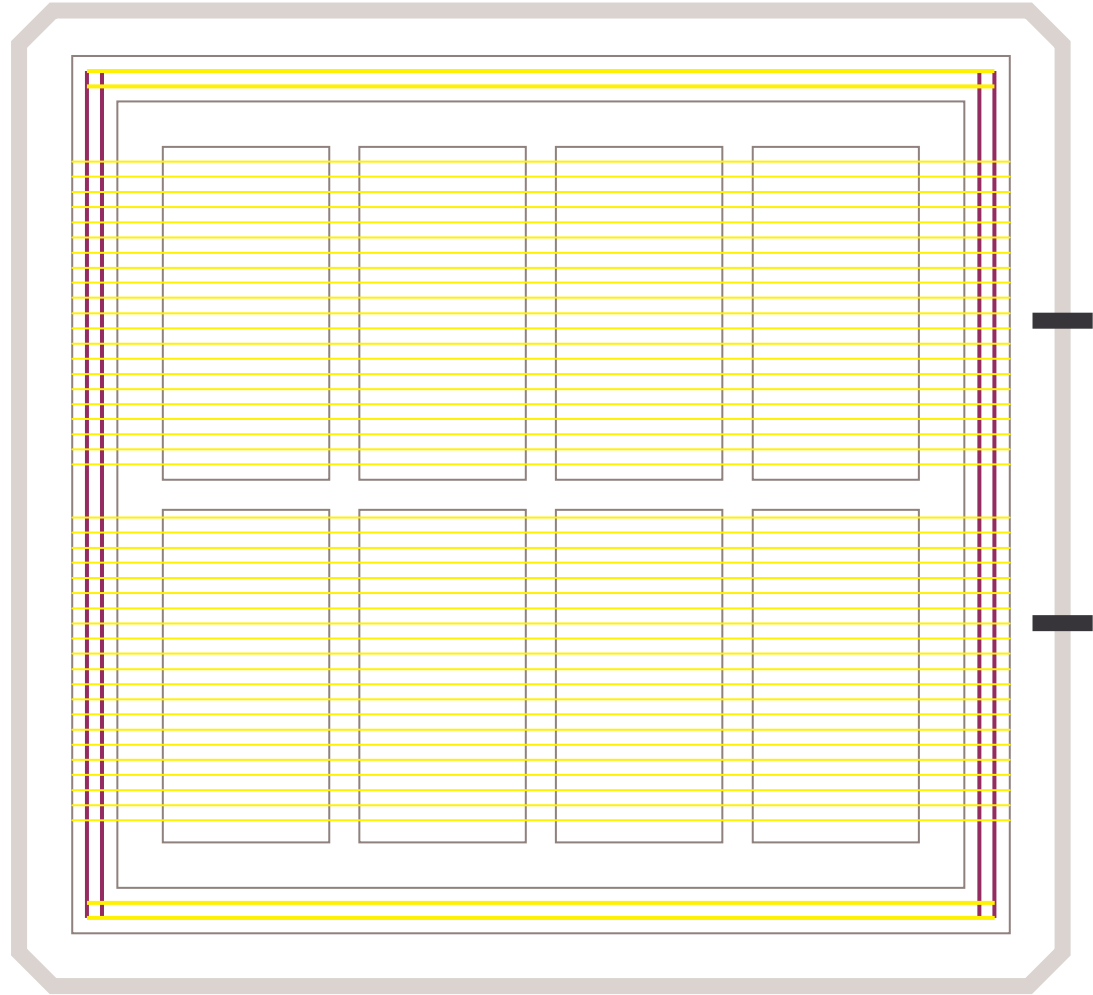
VDD1V8mso & VSS:Gmso



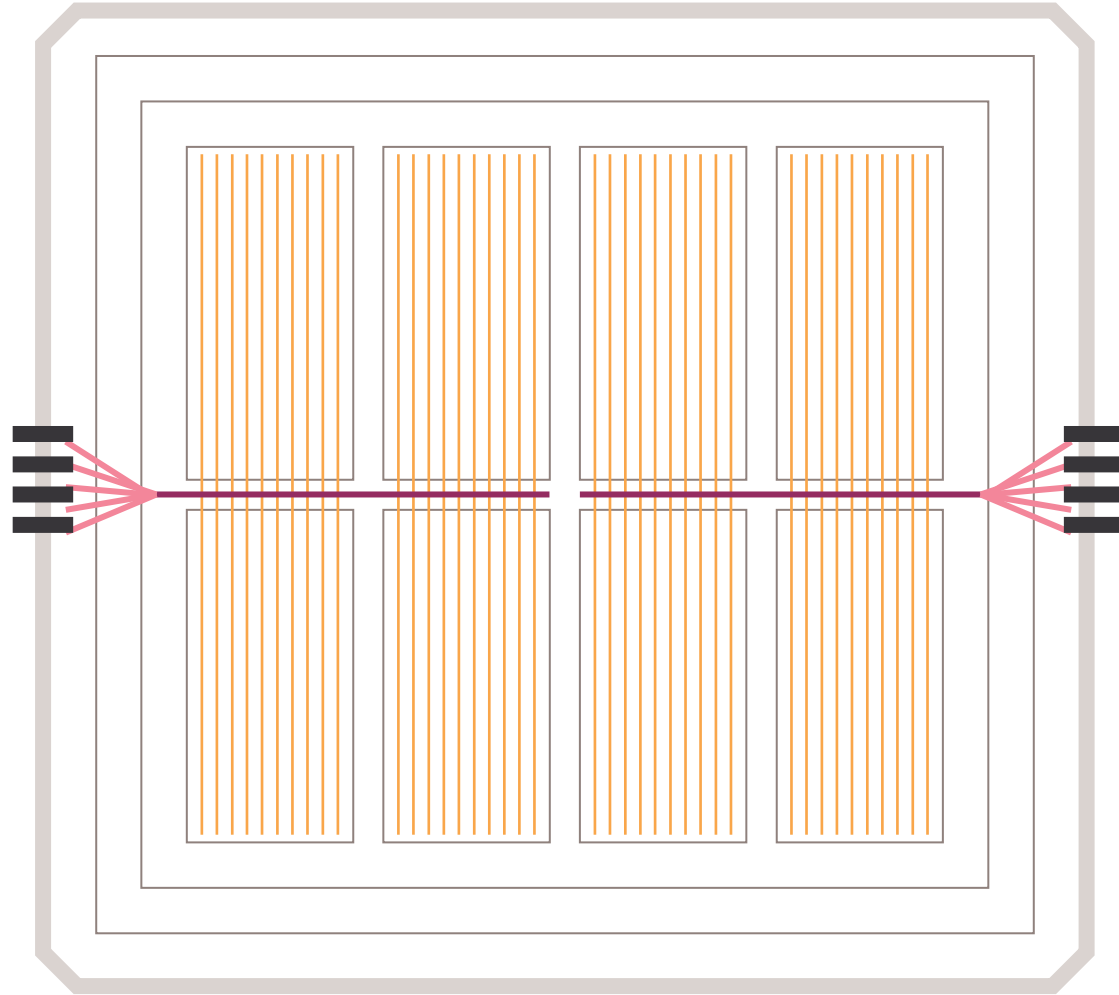
VDD1V8sram & VSS:Gsram



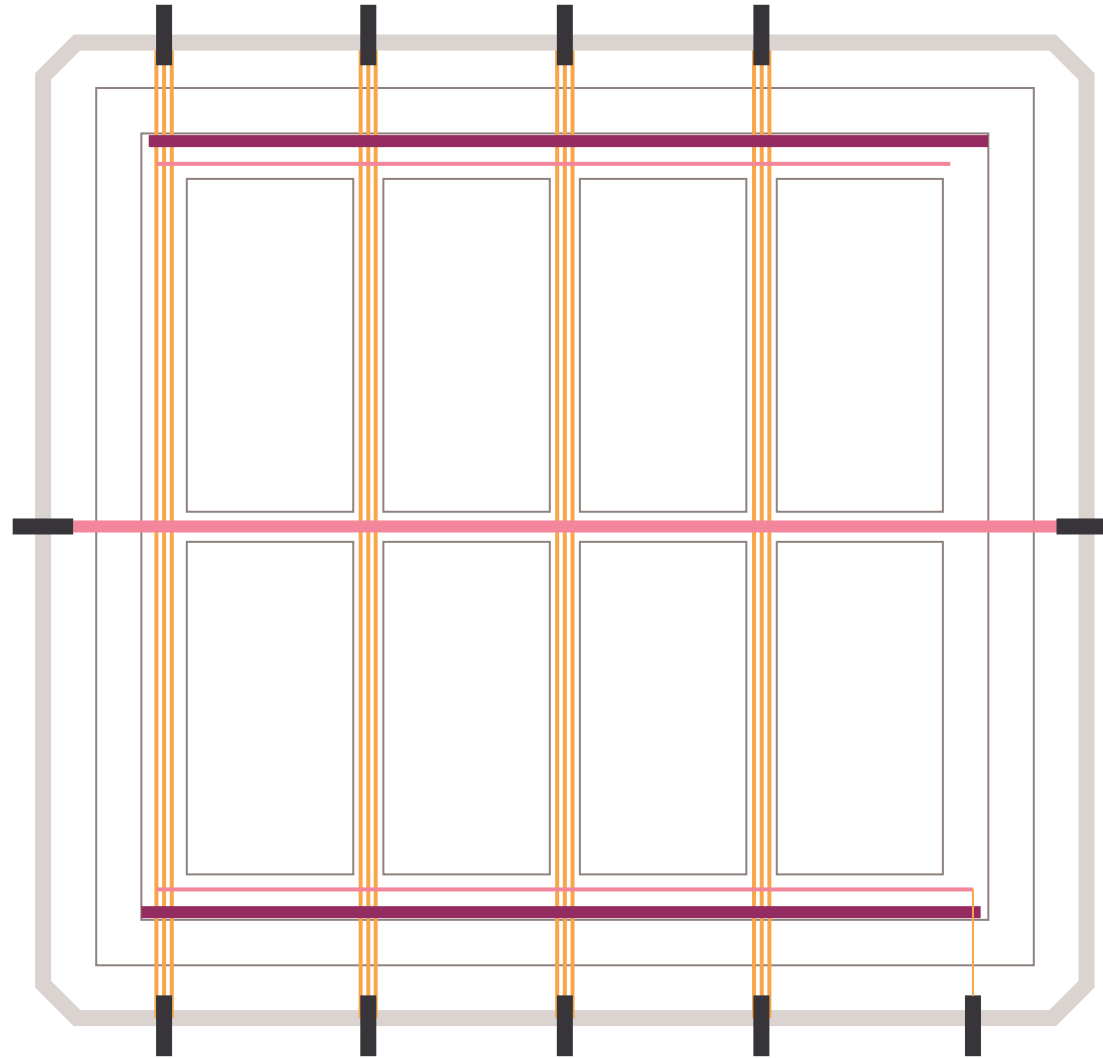
vrst



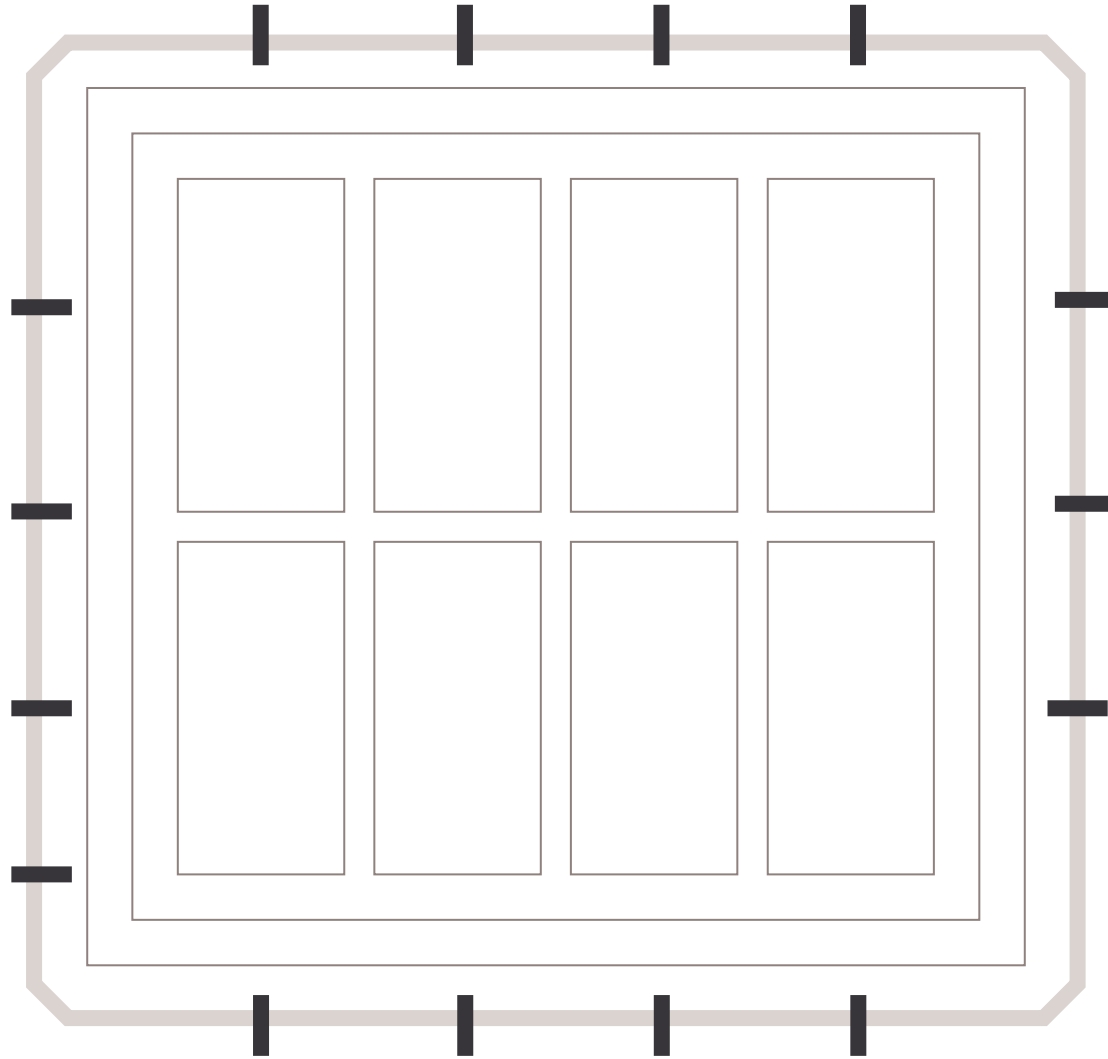
$V_{th}(+/-)$ & $V_{casc}(s)$



VDD1V8dig & VSS:Gdig



VDDO & VSSO (3.3v max)



Pixel Identification

