Problem Report

Report Number: 4

Project Name: TeraPixel APS for CALICE

Item: HiPoly resistors in preShape pixel





Originator (Sign/Date) Project Manager (Sign/Date) \leftarrow Monte-Carlo simulations of mismatch don't show much spread, although it is unclear whether they assume the recommended width rule was applied.

Manual simulations of resistor values $\pm 10\%$ show similar spread in circuit gain.

A long resistor of minimum width will be most susceptible to variation in track width

Remedial Action

Summary of options

Width	Length	Approx area	PCELL value	Actual value	Comment
0.18	486	343	3.9MΩ	2.7MΩ	Original design
0.18	595	416	4.8MΩ	3.3MΩ	Possible in new design, maximising length
2	5500	11000	3.9MΩ	2.7MΩ	Recommended width, target $2.7M\Omega$
0.21	570	417	3.9 MΩ	2.7MΩ	Maximised width for 2.7M Ω , possible in new design

Green trace in previous plot shows the 3.3M case, which is an improvement on original design, but not full designed performance. No larger resistor can fit in the pixel with all other changes implemented.

Clearly the recommended resistor width is impractical in the pixel – in fact keeping the original 2.7M resistance value and boosting width to improve matching can only fit an additional .03um width before using the full available area in the new pixel design – hence improvement to matching from this option will be negligible so recommend increase to length as most appropriate course of action.

Actual gain mismatch have not yet been fully evaluated in sensors – if significant this is a likely cause.

Note there is no facility to trim for gain mismatch.

Project Manager (Sign/Date)