Review Approval Form

Type of Review: FDR

Project Name: TeraPixel APS for CALICE: (TPAC1.1)

Documents Reviewed
Problem reports 1,2,3,4,5 Supporting documentation (pdf) Power distribution summary ASIC1.1 Design GANNT chart, updated status Schematics and layouts (cadence viewer) Printed layout of pixels, original and new designs. Copies of all review documents, agenda and minutes are held on PDR web site: http://www.hep.ph.ic.ac.uk/calice/maps/fdr2/fdr2.html

Comments

Top level/general changes

- Bulk pixels should be uniform, ie no capacitor variant. The chosen variant was (2), as located in the diagonally opposite corner to the test pixels.
- Hi-res wafers are a possibility, funded primarily by RT's CFi programme, but will implement the TPAC1.1 design for proof-of-principal.
- Pads, already enlarged to 80x80 should be lengthened if feasible (low priority) to further reduce risks with bonding future sensors, and push the foundry-added seal ring further out.

preShape pixel design:

- Poly resistor running under diode node M1 is not good – move linking section to M3 with M2 guard plate to avoid coupling to diode node.
- Link from comparator to monostable could be moved further over the sram config registers to avoid coupling to diode node
- M1 link to diodes in corners could be moved away from guard ring slightly, extra kink unnecessary
- Optimise layout of 4MR resistor for maximum resistance:
  - minimum space between strips
  - Bend corners as resistor, no need to come up to m1
  - Add extra length at beginning where connecting link is m1
- Parasitic extraction and simulation should be checked once layout changes are compete
- Review origins of the different contributory parasitics

Test devices (proposed in change req 2)

- Considered to be a good idea, should be done if possible
- 4M Resistor should be included (as finally implemented in the pixel
- Capacitors could be tested at IC, therefore include if feasible
- Diodes could also be useful (RT)

Test pixels

- Should implement one new pixel layout, and the old preShape pixel layout as the two test pixels now that the capacitor variants have been eliminated.
- Implement each as a 3x3 block of the same pixel type
- Two 3x3 blocks must be separated from the array, and each other, as the two pixel layouts won't tessellate correctly.

Hi Res Epi related changes

- deep p-well must be added under all circuits, such as logic, sram between pixels, and array edge circuits such as biases, shift registers, sense amplifiers, pads etc.
- Guard ring should be added around bulk array (not around logic columns). Connect to VRST pads for external bias.
- Guard ring should also be added around the test pixel arrays.
- Check with foundry extent of necessary DPW extension under bond pads
- Phone meeting with foundry scheduled in following week to discuss whether any other mitigating changes should be made for likely success with the hi-res wafers.

Wafer splits

- 6x(12um epi, DPW)
- 3x(12um epi, no DPW)
- 3x(5um epi, DPW)
- 3x(12um hi-res epi, DPW)

Due to lead time in hi-res epi procurement, the hi-res epi and 3 of the 6 (12um epi, DPW) parts will be manufactured at a later date using masks from the shuttle. Other parts will be processed as standard shuttle.

Approval: emails indicating approval are an adequate substitute for hardcopy signatures

Review Report agreed
Group Leader (sign/date) as required by the Project Management Plan

Customer (sign/date) as required by the Project Management Plan

Others – as stated in the Project Management Plan

Review Report agreed and any changes incorporated
Project Manager (sign/date) always required