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Summary/Dialogue

The improved pixel design incorporates a passive RC filter before the comparator. The resistor is made with an NMOS transistor biased such that it is 'on'. The noise is reduced by this filtration, but this also slows down the operation.

This document characterises the new pixel where it differs from the original, and presents some graphs in different units (generally equivalent electrons for noise) to aid comparison and understanding.

This pixel has a large input capacity of $\sim 64,000$ electrons which offers uncompromised performance after very large charge deposits. The pixel is inactive for a well-defined 600ns reset sequence following a hit. This may be reduced but at the cost of errors in the reset sample (and therefore the differential signal).

A key disadvantages to this pixel design is the integrating nature of the shaper circuit during bunch-train operation: Stray charge from nearby hits & noise will integrate on the shaper output and will not disperse. This will effectively reduce the threshold of these pixels towards the noise floor.

These pixels also require complex timing logic to trigger and sequence the reset lines for pixels who have been hit.

This pixel is very sensitive to additional capacitance at the input, which degrades the signal height – full parasitic extraction will be important to check the final layout and predict how it will function.

PreSample Pixel Overview



Brief Operating Instructions

- The pixel diodes are reset prior to a bunch train. (The diodes are then not reset during the bunch train.)
- Immediately before the bunch train commences, or after a hit is detected the following 600ns reset/sampling sequence occurs:
 - The preamplifier is reset for 200ns
 - The preamplifier output settles
 - The reset sample is taken after 600ns
 - The pixel is now active
 - Reducing this reset to 300ns introduces errors in the reset sample
- The diode source follower buffers the pixel signal from transients during preamp reset.
- The diode node collects charge and is read in voltage mode, therefore additional capacitance on the diode node will decrease the voltage (and therefore signal) that is seen by the circuit.
- Decreasing Cpre would increase the signal magnitude (gain of charge amplifier is ratio of Cpre to Cin)
- Increasing Cin further would improve gain in the preamplifier but requires more current in Buffer and Preamp stages to reset correctly in 150ns.
- The comparator takes signal and threshold in differential form and outputs a low voltage differential hit signal that must be sensed with a secondary PMOS comparator at the input to the logic blocks, where it is converted to 1.8v logic.

PreSample Pixel simulation: Example Operation

Circuit stimulus/scenario

Basic operation of the pixel circuits is demonstrated during start-up and typical operation.

Current (excluding comparator) 6 480 470 È460 45 44(430 1.7 1.6 150ns (rst) 1.25 § 1.0 .75 600ns (prerst) lus (smpl-rst) .25 2.0 1.75 13 Enable (power-up) .25 0.0-10.25 time (us) 9.75 10.5 10.75 11.0 9.5 10.0

Results waveforms

Above: Initial power-on (enable) conditions; timing and current consumption. This simulation show the circuit is operational and ready for a hit within 1us of enable.



Above: Pixel waveforms after a 400e- MIP. The reset cycle is initiated 300ns after the hit occurs, which means the shaper output does not have time to develop its full magnitude before the hit is reset.

PreSample Pixel simulation: Small Signals around threshold

The threshold is set at 60mV, which is the signal magnitude seen for 200 electrons, which corresponds to numele=50 in the plots below. The input signal (per diode) is swept from 20 to 150 electrons. The signal magnitude is plotted to check linearity and variation between corners. Where the circuit registers a "hit" the length of time the "hit" signal is active is plotted



Above: All five process corners are checked. The "numele" variable represents the charge on each diode. Only the FF corner exhibits significant variation from the other cases – since the signal magnitude does not display this variation this most likely arises in the comparator, which may be optimised further in final analysis.

PreSample Pixel simulation: Typical Signals (400 → 8000e-)

The threshold is set at 40mV, which is the signal magnitude seen for 130 electrons. The input signal (per diode) is swept from 400 to 8000 electrons. The signal magnitude is plotted to check linearity and variation between corners.



Above: Signal magnitude, reset error and time-to-threshold for typical input signals. Signal magnitude is presented at 150ns and 300ns delay from hit time where the reset has been omitted – in normal operation the channel reset would be applied thus preventing the full signal magnitude to develop. Note that the linear range of operation extends only as far as ~1200e- beyond this point the recently added filter starts to attenuate large signals, but this is of little concern to the CALICE application.

PreSample Pixel simulation: Typical Reset Sampling Errors



Given the relaxed timing constraints, the full preamp and reset re-sampling can be achieved in 600ns achieving low errors after large or small signals, and allowing good full-well capacity of order 65,000e-.

Below: Errors in reset sample after hits of various sizes (3 process corners checked)



PreSample Pixel simulation: Large Signals (→100,000e-)

Pixel operation is evaluated for very large signals (>10 MIPS). Hit and reset performance must be evaluated.

Results Waveforms



Above: Time-to-threshold for very large hits & reset sampling error following a very large hit. Note that the x axis 'numeleBIG' should be multiplied by 4 to determine the total input charge.

In this circuit topology, larger hits simply yield faster rise times; for such large signals the rise time is limited by the slew rate of the amplifier stage, hence there is little difference for such large signals.

Observing the diode node and the output from the first source follower indicates that the **maximum input charge is ~64,000 electrons**. Beyond this point (whether as a single hit or integrated from several hits) the diode nears saturation and non-linear behaviour is expected. This limit is also reflected in the reset errors above.

PreSample Pixel simulation: Power consumption

Pixel Source follower	Charge (Pre)amplifier	Output Source Follower	Comparator (in-pixel)	Comparator (off-pixel)
1.8v	1.8v	1.8v	1.8v	1.8v
0.9uA	1.3uA	1.2uA	1uA	750nA
1.6uW	2.4uW	2.2uW	1.8uW	1.3uW

Total power consumption = 9.3uW

PreSample Pixel simulation: Noise Analysis

Circuit stimulus/scenario

Standard noise analysis is shown to illustrate the dominant noise sources in the circuit. Noise is measured at the shaper output / input to comparator. The pixel circuit is modified for noise analysis as follows

- a) The reset transistor is disconnected from the diode, which is biased to 1v with an ideal voltage source
- b) The preamplifier reset switch is replaced with a 1Tohm resistor to correctly set the DC operating point.

Results

/I470/M1	fn	0.003012	28.34			
/I470/M3	id	0.00284252	25.24			
/I470/M1	id	0.00262834	21.58			
/I470/M3	fn	0.00180591	10.19			
/I470/M2	id	0.00145969	6.66			
/I470/R0	rn	0.000804504	2.02			
/I470/M5	id	0.000637879	1.27			
/I470/M5	fn	0.000630638	1.24			
/I461/M110	id	0.000487317	0.74			
/I461/M33	id	0.000438274	0.60			
/I470/M2	fn	0.000407097	0.52			
/I470/M8	id	0.000197127	0.12			
/I461/M110	fn	0.000167859	0.09			
Integrated Noise Summary (in V) Sorted By Noise						
Contributors						
Total Output Noise = 0.00565762						
Total Input Referred Noise = 0.0670668						
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The dominant noise sources are found to be the input devices in the diode source follower (M1) and the amplifier (M3). Contribution from R0 can be ignored.

Due to the sampling nature of this pixel architecture the noise seen at the output of the pixel circuitry must be considered twice, since it will be sampled on the reset-storage capacitor, and will be considered again at the other input to the comparator, thus a factor of $\sqrt{2}$ should be applied when evaluating signal/noise.

Applying the $\sqrt{2}$ factor and referring to the input assuming 300μ V/e- gives: <u>26.7e- equivalent noise charge.</u>

PreSample Pixel simulation: Noise Vs Input Capacitance

Circuit stimulus/scenario

Noise in pixel circuits is independent of the capacitance at the input node but signal magnitude is. Referring the simulated noise back to the output takes account of the signal gain, hence it is possible to express equivalent noise in electrons as a function of the parasitic capacitance at the input.

Results waveforms



Above: Equivalent noise at input as varies with the capacitance at the input node:

- The charge-voltage gain is calculated for a 250 electron hit.
- Noise is multiplied by the $\sqrt{2}$ factor to account for the sampling action
- Square diodes of sizes 0.9, 1.8 and 3.6 micron are simulated.

All other simulations in this document have been produced using value of Cextra=8fF and diodes measuring 1.8x1.8um.

PreSample Pixel simulation: Noise Filtering

Circuit stimulus/scenario

The cut-off frequency of the noise filtering is adjusted by varying Cfilt. Key circuit performance criteria are checked.

Results waveforms

The filtering effect can be seen to slow the edge of the step pulse at the shaper output

The signal magnitude is barely affected but the noise reduces if longer time-to-threshold is acceptable.

Below: Noise in electrons, timeto-threshold for 250 & 500esignal sizes, and signal magnitude are plotted





PreShape Pixel simulation: Performance vs Bias Current

Circuit stimulus/scenario

The current in the diode source follower is adjusted; key performance parameters are plotted. The input signal is 400 electrons.



The parameter isfbias is mirrored into the source follower circuit by a factor of 0.01, hence the point at 90 is the chosen operating point (0.9uA) for the simulations & results in this document.

Circuit stimulus/scenario

The current in the shaper amplifier is adjusted; key performance parameters are plotted. The input signal is 400 electrons.



The parameter iprebias 1 is mirrored into the shaper amplifier circuit by a factor of 0.01, hence the point at 130 is the chosen operating point (1.3uA) for the simulations & results in this document.

Circuit stimulus/scenario

The current in the output source follower is adjusted; key performance parameters are plotted. The input signal is 400 electrons.



The parameter iouts $f_{0.01}$ is mirrored into the source follower circuit by a factor of 0.01, hence the point at 120 is the chosen operating point (1.2uA) for the simulations & results in this document.

PreSample Pixel simulation: Matching/Manufacturing Risks

Circuit stimulus/scenario

Each passive component in the circuit is varied individually to check the dominance of their value on the signal pulse, noise and reset sample error (after small 400e- and large 10,000e- inputs). Those components that have the largest effect will contribute most to mismatch between pixels and should be most carefully considered during layout.

<u>Shaper</u> Cin	3.6fF	Small area capacitance will be most prone to mismatch. Consider enlarging this device (within spec) once final numbers for signal (#electrons) are better defined.
		<u>High risk</u>
Shaper	250fF	Large size should allow good matching
C.A.		
Cfb		Low risk



Above: the capacitor "cin" is adjusted to show the relationship between signal magnitude and noise. The reset sample errors introduced for larger Cin are due to the increased signal gain which pushes the circuit beyond its intended operating region. The selected operating point is indicated.



Above: the capacitor "cfb" is adjusted to show the relationship between signal magnitude and noise. The selected operating point is indicated.

PreSample Pixel simulation: Mismatch

Circuit stimulus/scenario

Monte-Carlo simulation varies component parameters according to statistical models: Typical process corner; 1MIP (400e) input signal. Reset sample error is checked after a small 400e- hit and a large 10,000e- hit.

Results waveforms



	Gain (V/e-)	Noise (e-)	Rst Err 400	Rst Err 10000	Hit Delay 400
mu	307u	25.9	-86u	-426u	200n
stddev	1u	0.2	87u	96u	38n

These preliminary results from 27 runs show good matching between mismatch cases.

 \rightarrow LONGER MONTE-CARLO AND CORNERS TO FOLLOW (lengthy simulation results unavailable at time of writing)

Pixel Layout Placement

The plot below is a quick placement of all the pixel components in a 50 micron pixel boundary to check that they will fit. The large capacitors will dominate the pixel area, but there is sufficient space for careful placement. The central NWELL consists of a single PMOS transistor and well contact, which should fit into a 3.5x3.5 micron square: At present the transistor is long and thin, instead of a square, requiring an nwell measuring 1.3x6.3um – perhaps the diode placement could be optimised for this shape NWELL rather than using additional NWELL area to split the transistor into parallel fingers? Additional blocks (pmos comparator, masking) could be incorporated into the pixel if the deep p-implant is available.

