Review Approval Form

Type of Review: IDR (logic & top-level schematics)

Project Name: TeraPixel APS for CALICE

Documents Reviewed
Latest top level schematic (design open in cadence for interactive viewing) Logic and top-level simulation results document v1.0. Attendees: JC, RT, Paul Dauncey, Andy Clark, Marcel Stanitzki, Matt Noy, Konstantin Stefanov

Comments
Full minutes taken by Paul Dauncey, available on web at http://www.hep.ph.ic.ac.uk/calice/maps/idr1/idr1.html Requested that logic layout should occupy 50 micron units (ie interger number of dead pixels) for simplified physics simulations. The preference would be to spread the dead logic areas across the array of pixels, rather than grouping them together “back-to-back” ie 4 col logic, 42 cols pixels; 4 cols logic; 42 cols pixels etc… (P.11) Add monitoring pad to the monostable output from this circuit. Power supply separation for the monostable should be completely isolated from substrate – ie do not connect monostable-VSS to the substrate, use another local digital VSS to make these substrate ties. (Ensures high return-currents do not flow in the substrate). SRAM write will be driven at 3.3v as demonstrated in the simulation doc is required to avoid bit errors (noted as some other parts of docs reference 2.5v which *is* sufficient in all but extreme process corners). (P.30-31) SRAM cells for shift-reg control. Decision to avoid possible race hazards completely by supplying third clock phase externally: Place pad for phi3b adjacent to phi2 so can be bonded to same if it works. Check phi3 and phi2 loads are the same so edges consistent at other end of chip. Look for glitch in the “Done” signal (logic NOR of the shift-register) – check these cannot propagate to next cell and implement mitigation strategy if necessary Look for glitches in the hold circuit & check implications of. Add pull up/power-down mechanism to hold circuit so it is safe and doesn’t require constant clocking to avoid high-power drain state. Re-simulate hold circuit at 50C to check charge leakage from gate does not prevent operation at 5Mhz! Re-run key mixed-mode simulations at 50C Propagation/loading delays of MUX_ADDR signals should be checked (must synchronise with 50Mhz phi2) Row encoder must be made suitable for 168 lines, not 84 as present (otherwise would see repeating addresses in full sensor readout!) P.50 Dummy logic column simulation: Check edges and delays on all control signals that must operate with the phi1 and phi2 clocks at the 50Mhz rate – 1ns delays on such fast signals ARE significant and should be double-checked! P53 full logic simulation output does not include row info – add if re-running this sim. Test structures will be added to the schematic as the design nears completion and it is clear what room and pads are available.

Approval: emails indicating approval are an adequate substitute for hardcopy signatures

Review Report agreed
Group Leader (sign/date) as required by the Project Management Plan

Customer (sign/date) as required by the Project Management Plan

Others – as stated in the Project Management Plan

Review Report agreed and any changes incorporated
Project Manager (sign/date) always required