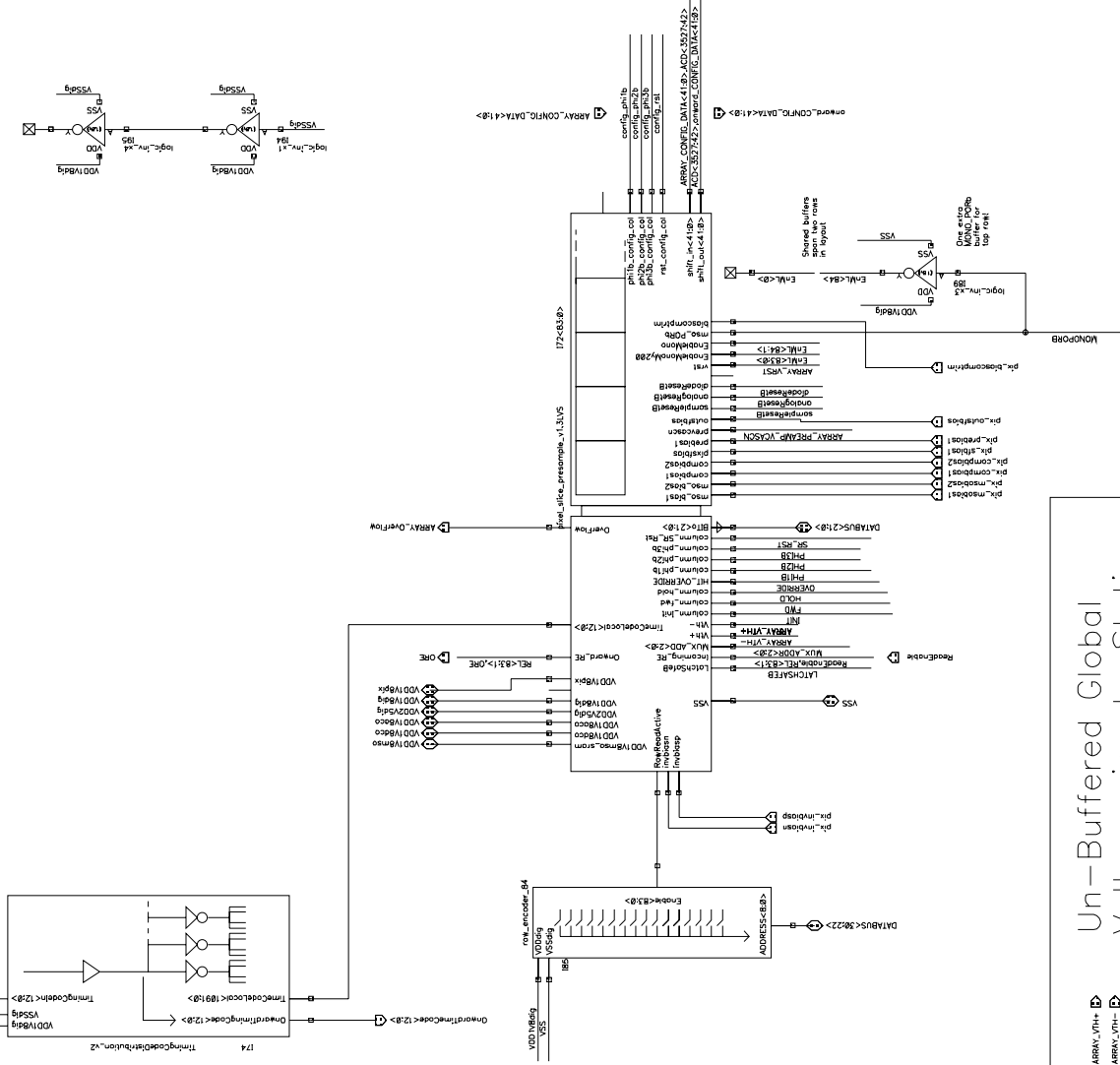


# Pre-Sample Pixel Half-Array 84rows x 42cols

Spare inverter in layout, tied off to gnd

- ARRAY\_VH1
- ARRAY\_VH2
- ARRAY\_VH3
- ARRAY\_VH4
- ARRAY\_VH5
- ARRAY\_VH6
- ARRAY\_VH7
- ARRAY\_VH8
- ARRAY\_VH9
- ARRAY\_VH10
- ARRAY\_VH11
- ARRAY\_VH12
- ARRAY\_VH13
- ARRAY\_VH14
- ARRAY\_VH15
- ARRAY\_VH16
- ARRAY\_VH17
- ARRAY\_VH18
- ARRAY\_VH19
- ARRAY\_VH20
- ARRAY\_VH21
- ARRAY\_VH22
- ARRAY\_VH23
- ARRAY\_VH24
- ARRAY\_VH25
- ARRAY\_VH26
- ARRAY\_VH27
- ARRAY\_VH28
- ARRAY\_VH29
- ARRAY\_VH30
- ARRAY\_VH31
- ARRAY\_VH32
- ARRAY\_VH33
- ARRAY\_VH34
- ARRAY\_VH35
- ARRAY\_VH36
- ARRAY\_VH37
- ARRAY\_VH38
- ARRAY\_VH39
- ARRAY\_VH40
- ARRAY\_VH41
- ARRAY\_VH42
- ARRAY\_VH43
- ARRAY\_VH44
- ARRAY\_VH45
- ARRAY\_VH46
- ARRAY\_VH47
- ARRAY\_VH48
- ARRAY\_VH49
- ARRAY\_VH50
- ARRAY\_VH51
- ARRAY\_VH52
- ARRAY\_VH53
- ARRAY\_VH54
- ARRAY\_VH55
- ARRAY\_VH56
- ARRAY\_VH57
- ARRAY\_VH58
- ARRAY\_VH59
- ARRAY\_VH60
- ARRAY\_VH61
- ARRAY\_VH62
- ARRAY\_VH63
- ARRAY\_VH64
- ARRAY\_VH65
- ARRAY\_VH66
- ARRAY\_VH67
- ARRAY\_VH68
- ARRAY\_VH69
- ARRAY\_VH70
- ARRAY\_VH71
- ARRAY\_VH72
- ARRAY\_VH73
- ARRAY\_VH74
- ARRAY\_VH75
- ARRAY\_VH76
- ARRAY\_VH77
- ARRAY\_VH78
- ARRAY\_VH79
- ARRAY\_VH80
- ARRAY\_VH81
- ARRAY\_VH82
- ARRAY\_VH83
- ARRAY\_VH84
- ARRAY\_VH85
- ARRAY\_VH86
- ARRAY\_VH87
- ARRAY\_VH88
- ARRAY\_VH89
- ARRAY\_VH90
- ARRAY\_VH91
- ARRAY\_VH92
- ARRAY\_VH93
- ARRAY\_VH94
- ARRAY\_VH95
- ARRAY\_VH96
- ARRAY\_VH97
- ARRAY\_VH98
- ARRAY\_VH99
- ARRAY\_VH100



Un-Buffered Global Voltage signals: Static during operation

Project	Terc-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array_presample_v1.4
Last OA Review	
Last Changed	Feb 27, 18:43:10 2007

- ARRAY\_VH1
- ARRAY\_VH2
- ARRAY\_VH3
- ARRAY\_VH4
- ARRAY\_VH5
- ARRAY\_VH6
- ARRAY\_VH7
- ARRAY\_VH8
- ARRAY\_VH9
- ARRAY\_VH10
- ARRAY\_VH11
- ARRAY\_VH12
- ARRAY\_VH13
- ARRAY\_VH14
- ARRAY\_VH15
- ARRAY\_VH16
- ARRAY\_VH17
- ARRAY\_VH18
- ARRAY\_VH19
- ARRAY\_VH20
- ARRAY\_VH21
- ARRAY\_VH22
- ARRAY\_VH23
- ARRAY\_VH24
- ARRAY\_VH25
- ARRAY\_VH26
- ARRAY\_VH27
- ARRAY\_VH28
- ARRAY\_VH29
- ARRAY\_VH30
- ARRAY\_VH31
- ARRAY\_VH32
- ARRAY\_VH33
- ARRAY\_VH34
- ARRAY\_VH35
- ARRAY\_VH36
- ARRAY\_VH37
- ARRAY\_VH38
- ARRAY\_VH39
- ARRAY\_VH40
- ARRAY\_VH41
- ARRAY\_VH42
- ARRAY\_VH43
- ARRAY\_VH44
- ARRAY\_VH45
- ARRAY\_VH46
- ARRAY\_VH47
- ARRAY\_VH48
- ARRAY\_VH49
- ARRAY\_VH50
- ARRAY\_VH51
- ARRAY\_VH52
- ARRAY\_VH53
- ARRAY\_VH54
- ARRAY\_VH55
- ARRAY\_VH56
- ARRAY\_VH57
- ARRAY\_VH58
- ARRAY\_VH59
- ARRAY\_VH60
- ARRAY\_VH61
- ARRAY\_VH62
- ARRAY\_VH63
- ARRAY\_VH64
- ARRAY\_VH65
- ARRAY\_VH66
- ARRAY\_VH67
- ARRAY\_VH68
- ARRAY\_VH69
- ARRAY\_VH70
- ARRAY\_VH71
- ARRAY\_VH72
- ARRAY\_VH73
- ARRAY\_VH74
- ARRAY\_VH75
- ARRAY\_VH76
- ARRAY\_VH77
- ARRAY\_VH78
- ARRAY\_VH79
- ARRAY\_VH80
- ARRAY\_VH81
- ARRAY\_VH82
- ARRAY\_VH83
- ARRAY\_VH84
- ARRAY\_VH85
- ARRAY\_VH86
- ARRAY\_VH87
- ARRAY\_VH88
- ARRAY\_VH89
- ARRAY\_VH90
- ARRAY\_VH91
- ARRAY\_VH92
- ARRAY\_VH93
- ARRAY\_VH94
- ARRAY\_VH95
- ARRAY\_VH96
- ARRAY\_VH97
- ARRAY\_VH98
- ARRAY\_VH99
- ARRAY\_VH100

VDD1V8  
 VDD1V5

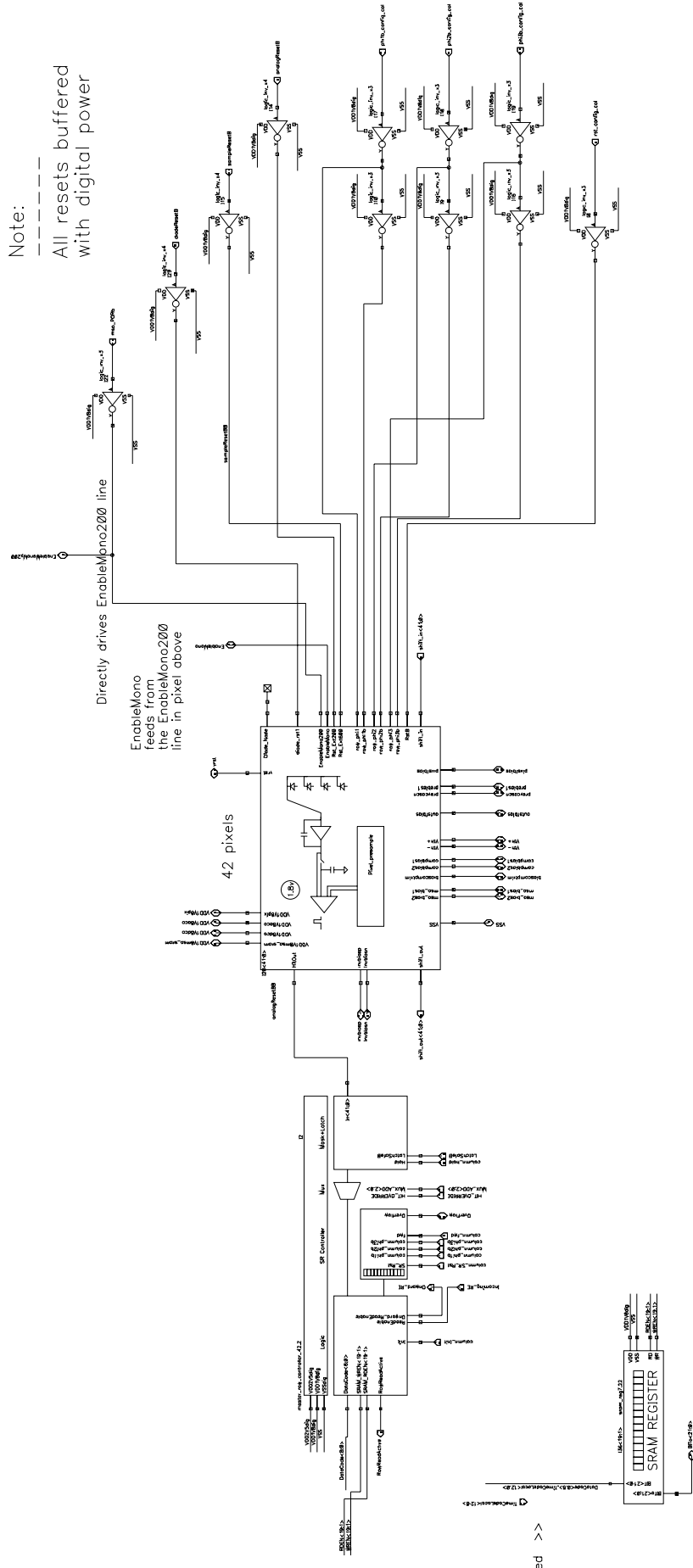
Note: ---

All resets buffered with digital power

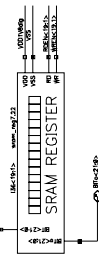
Directly drives EnableMono200 line

EnableMono feeds from the EnableMono200 line in pixel above

42 pixels

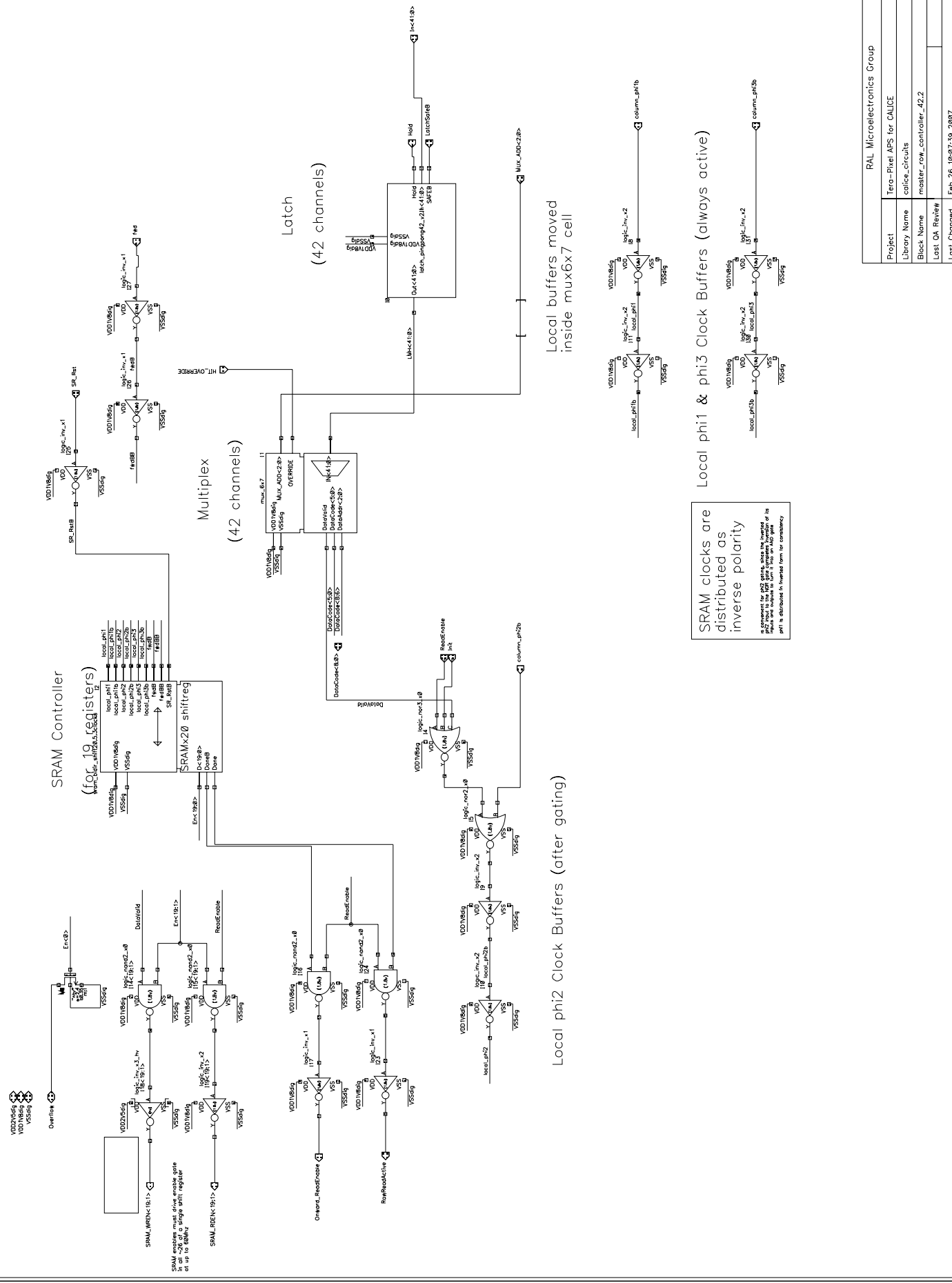


Note: bus order changed >>

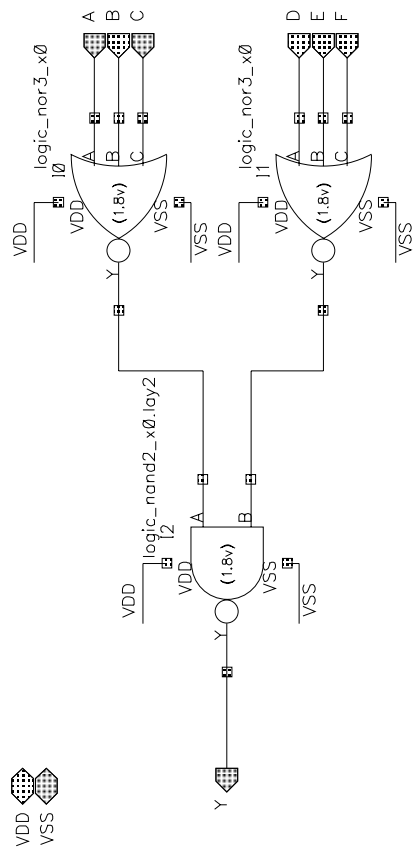


RAL Microelectronics Group	
Project	Zero-Power APIS for CALICE
Library Name	calice_circuits
Block Name	pixel_array_resetbuffer_1_1_1_V15
Last CA Review	
Last Changed	Feb 26 16:56:30 2017

# 42-CHANNEL 3-CLOCKS VERSION

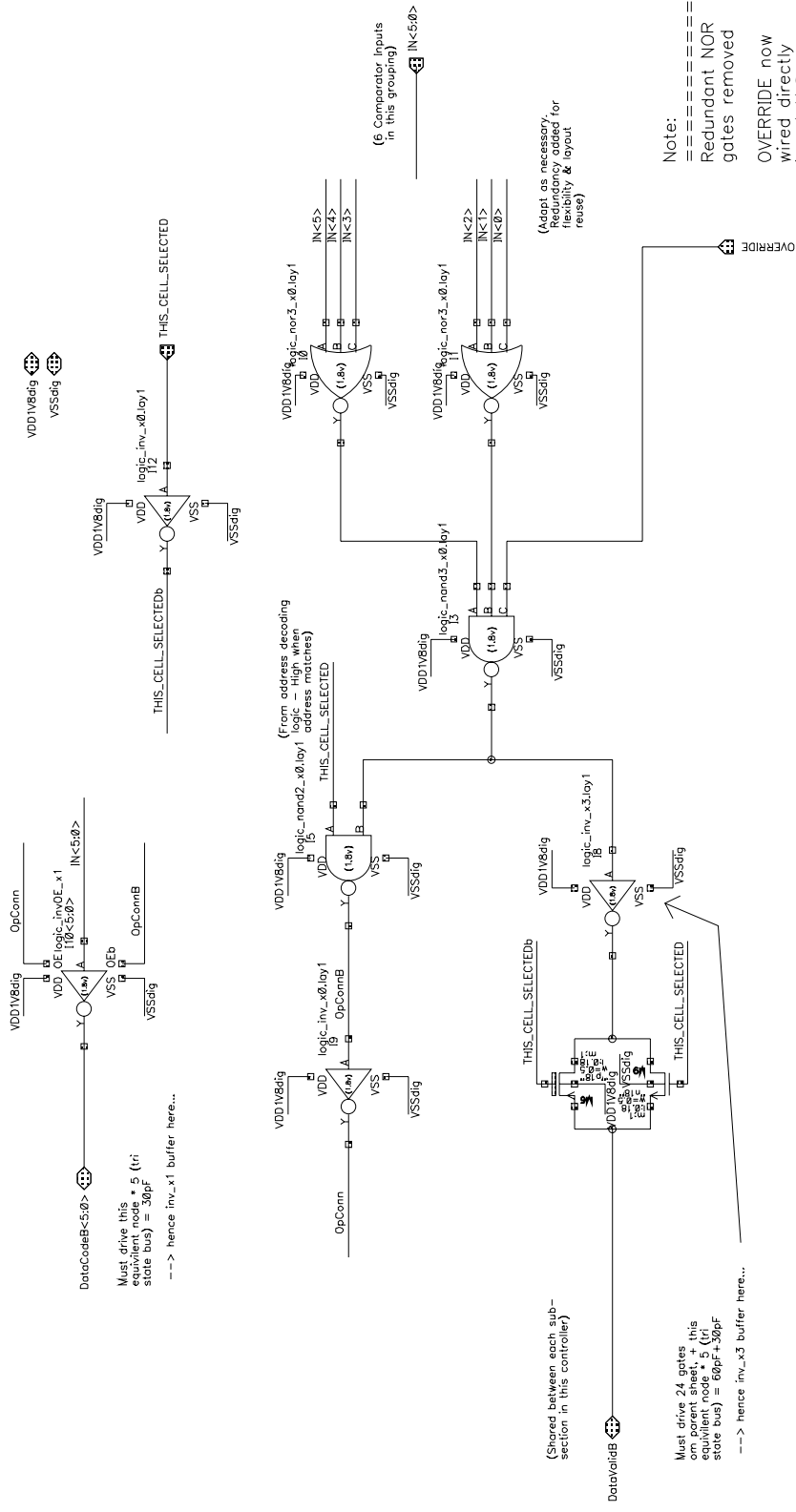


Project	Tero-Flex APS for CALICE
Library Name	calice_circuits
Block Name	master_row_controller_422
Last OA Review	
Last Changed	Feb 26 16:07:39 2007



RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_or6
Last QA Review	
Last Changed	Feb 15 11:02:18 2007

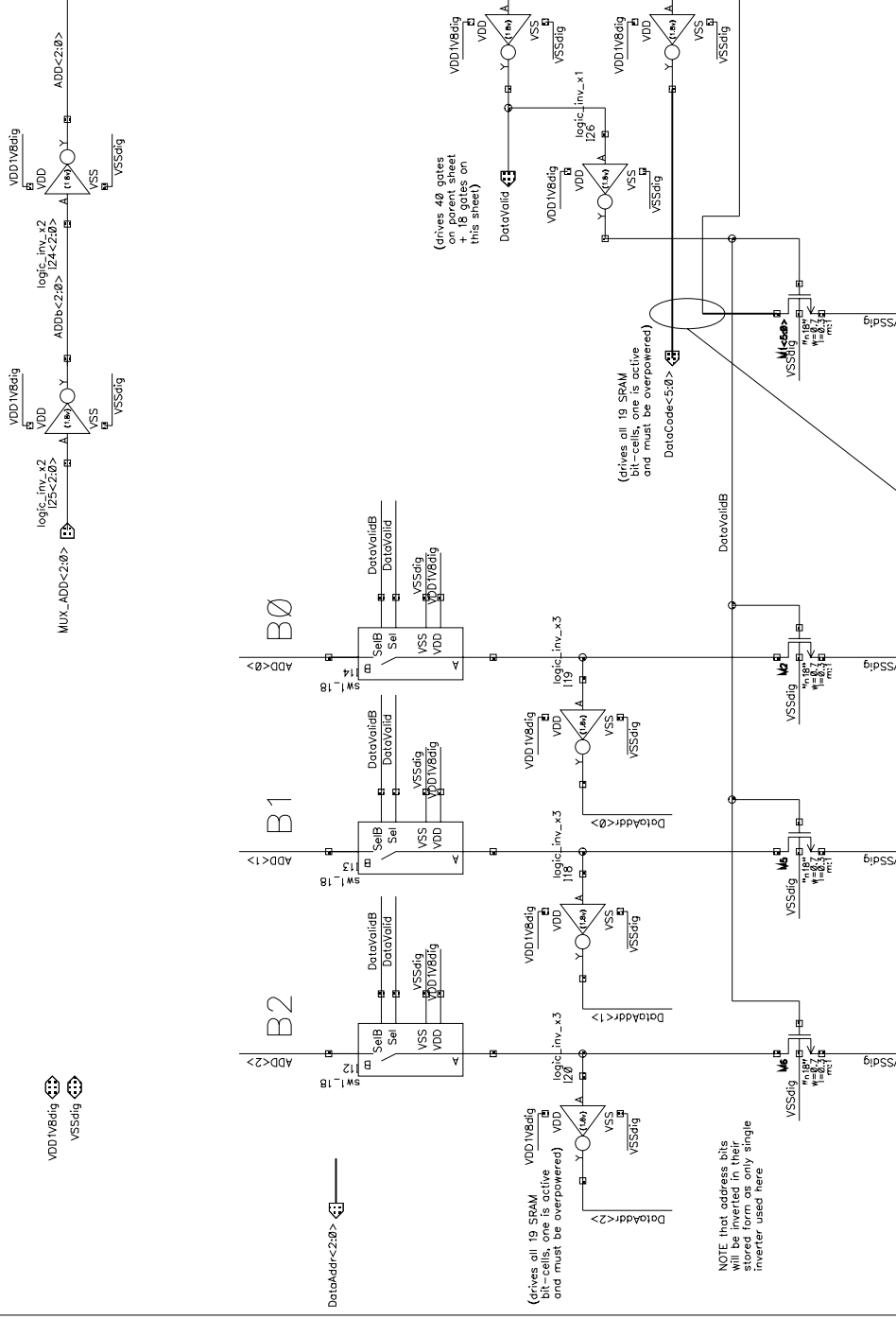


RAL Microelectronics Group	
Project	Tero-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6
Last QA Review	
Last Changed	Jan 11 15:41:42 2007

# Address Decoding

ADD<2, 1, 0>	111	*new* SEL<6>
	110	SEL<5>
	101	SEL<4>
	100	SEL<3>
	011	SEL<2>
	010	SEL<1>
	001	SEL<0>
	000	Reserved (below)

0000111  
1100001  
1001100

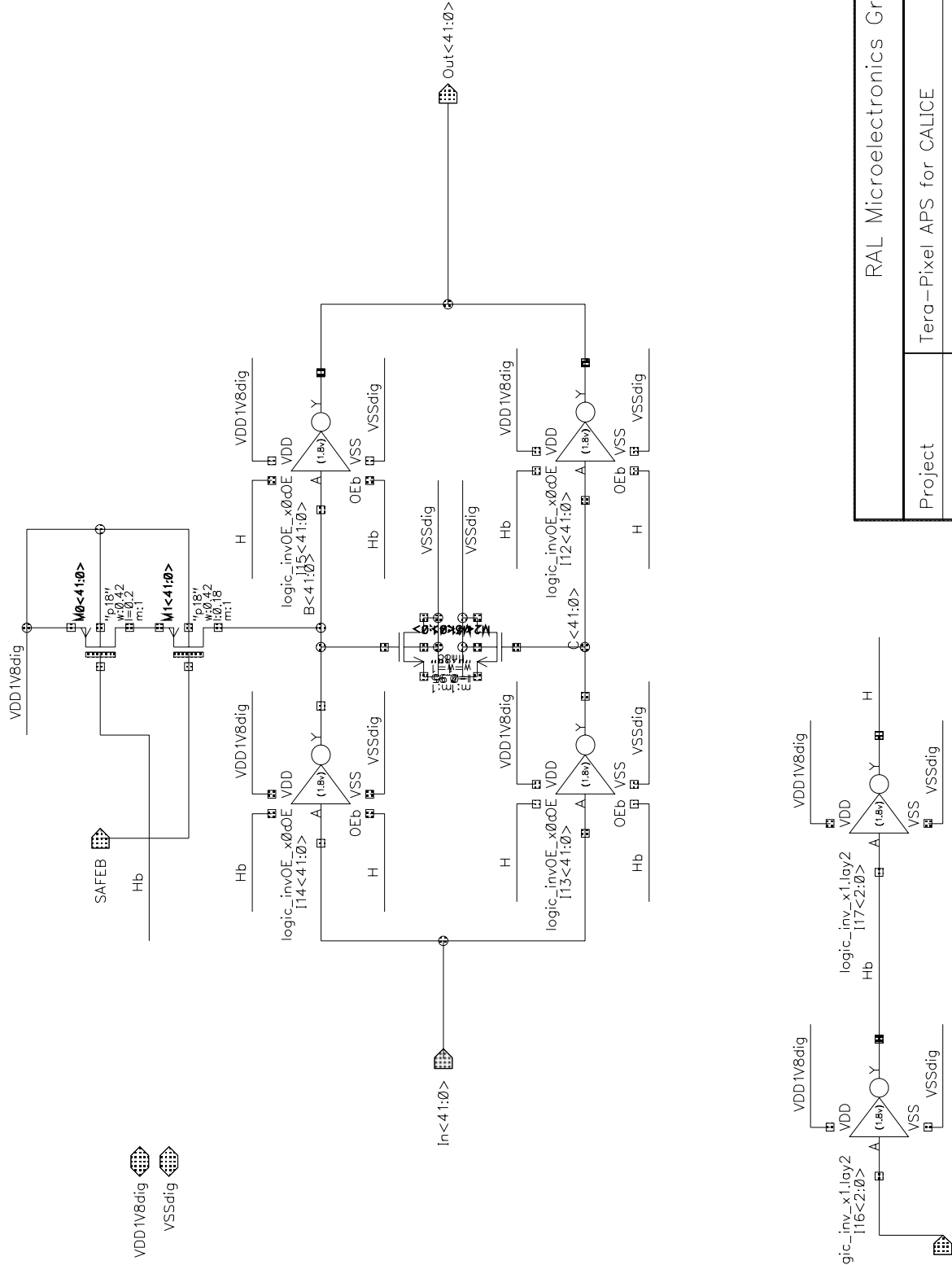


ERROR CORRECTED:

Note new buffer for local DataValid  
 Modifications in progress – CONFIRM!

DataCode should be pulled down  
 BEFORE the inverter not after  
 ReSim to confirm.

RAL Microelectronics Group	
Project	Tero-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6x7
Last QA Review	
Last Changed	Feb 16 10:35:10 2007

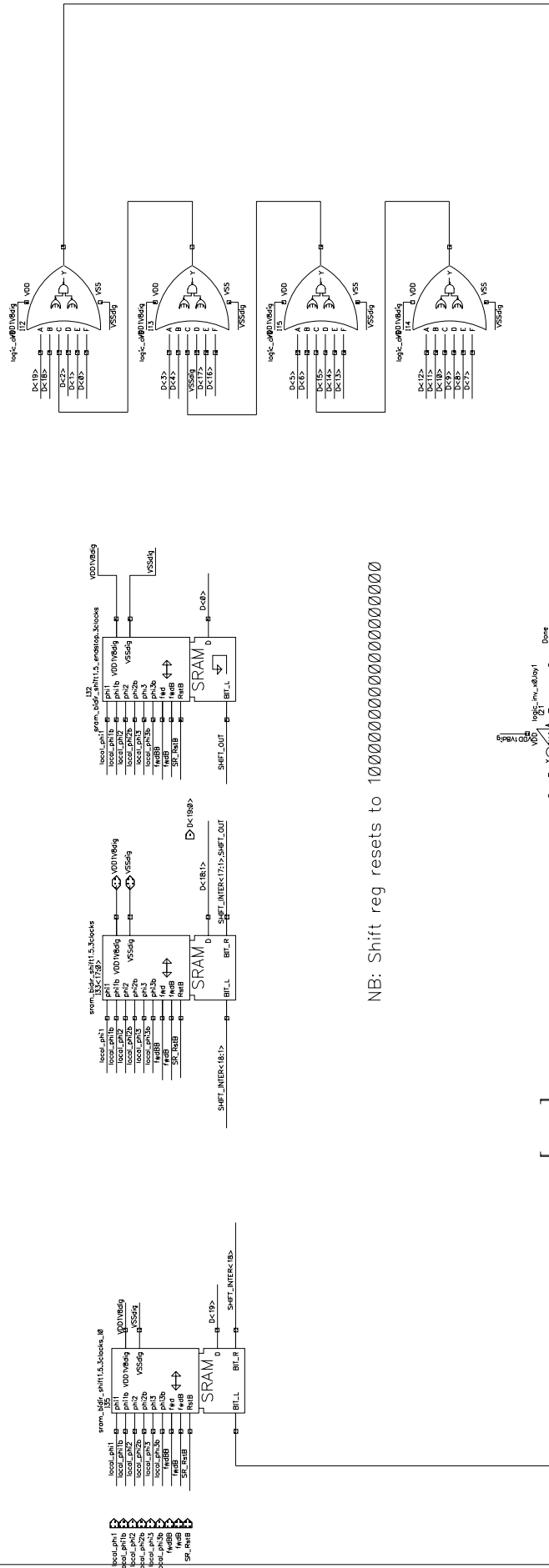


VDD1V8dig  
VSSdig

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	latch_pingpong42_v2.1
Last QA Review	
Last Changed	Feb 12 18:50:02 2007

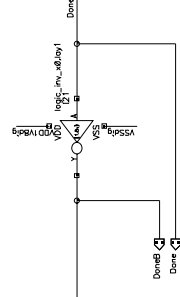
Hold  
logic\_inv\_x1\_lay2  
116<2:0>  
Hb  
VDD  
VSSdig

VDD1V8dig  
VDD  
VSSdig  
logic\_inv\_x1\_lay2  
117<2:0>  
Hb  
H  
VSSdig



NB: Shift reg resets to 10000000000000000000

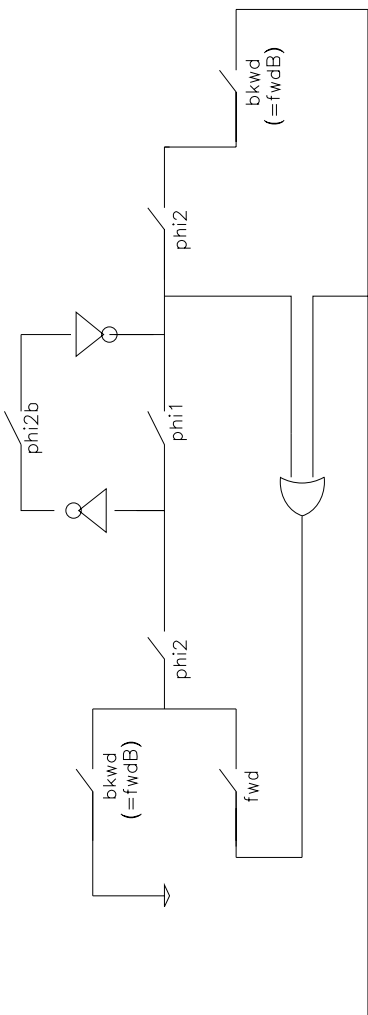
TG removed since special I0 part in SR is now used



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	srnm_bdf_sh1105.5_blocks
Last QA Review	
Last Changed	Feb 15 16:27:03 2007

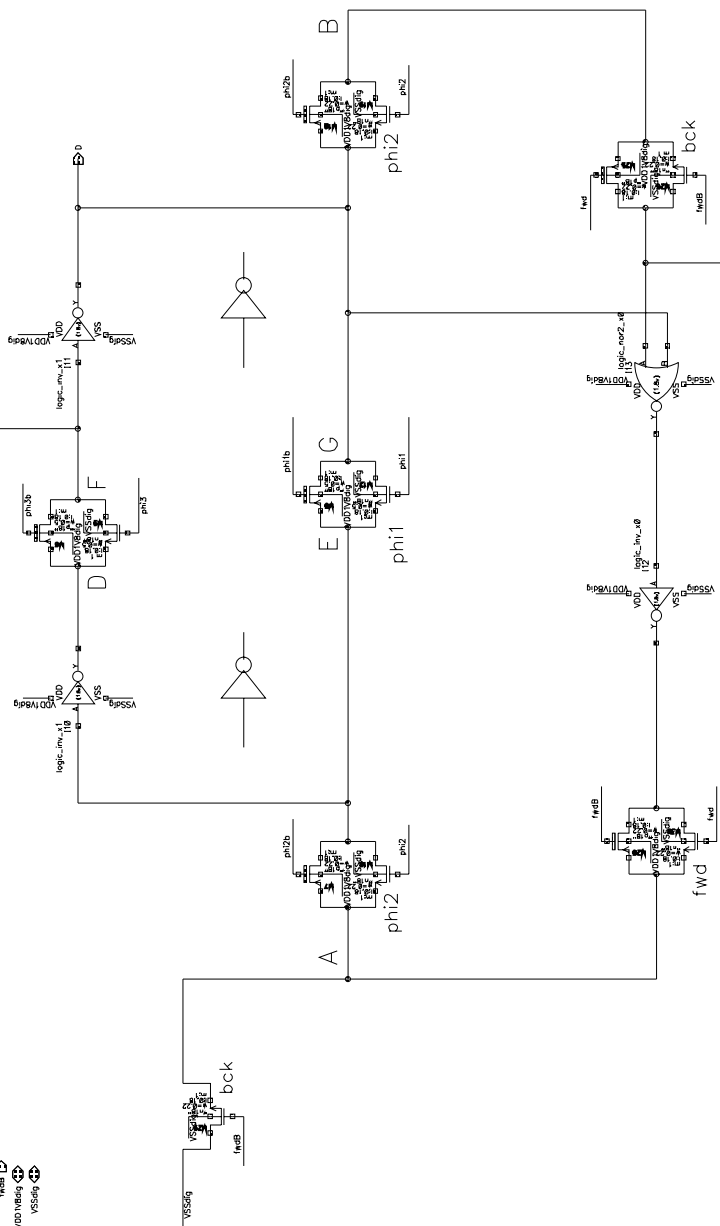


<b>POWER UP</b> phi1 off phi2 on RstB on (low)
<b>IN-SERVICE RESET</b> phi1 off phi2 on RstB pulsed on (low) during phi2
<b>INVALID STATE</b> phi1 X phi2 off (low) RstB on (low)



phi1 : Data Hold State  
 phi2 : Data transfer L>R (fwd=1)  
 phi2 : Data transfer R>L (fwd=0)

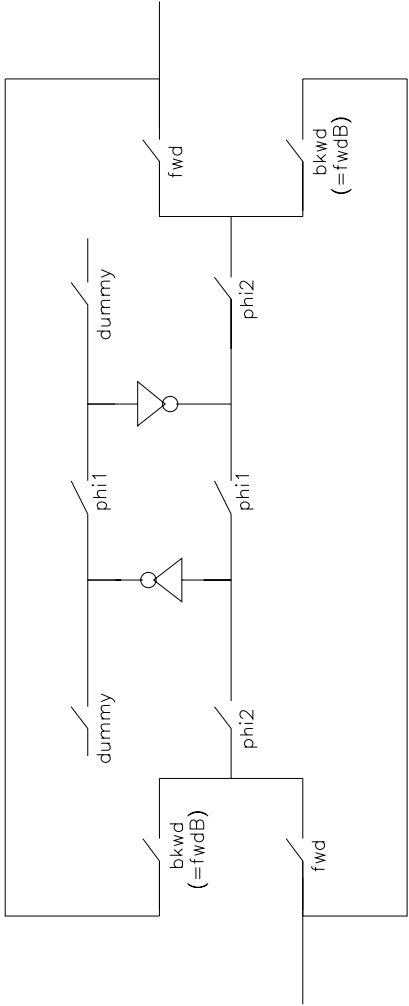
- phi1
- phi2
- phi2b
- phi1b
- fwd
- fwdB
- VDDVBSig
- VSSSig



RAL Microelectronics Group	
Project	Tera-Fixer APS for CALICE
Library Name	calice_circuits
Block Name	stom_bufr_sifn1.5_endstop_blocks
Last QA Review	
Last Changed	Feb 5 18:18:07 2007

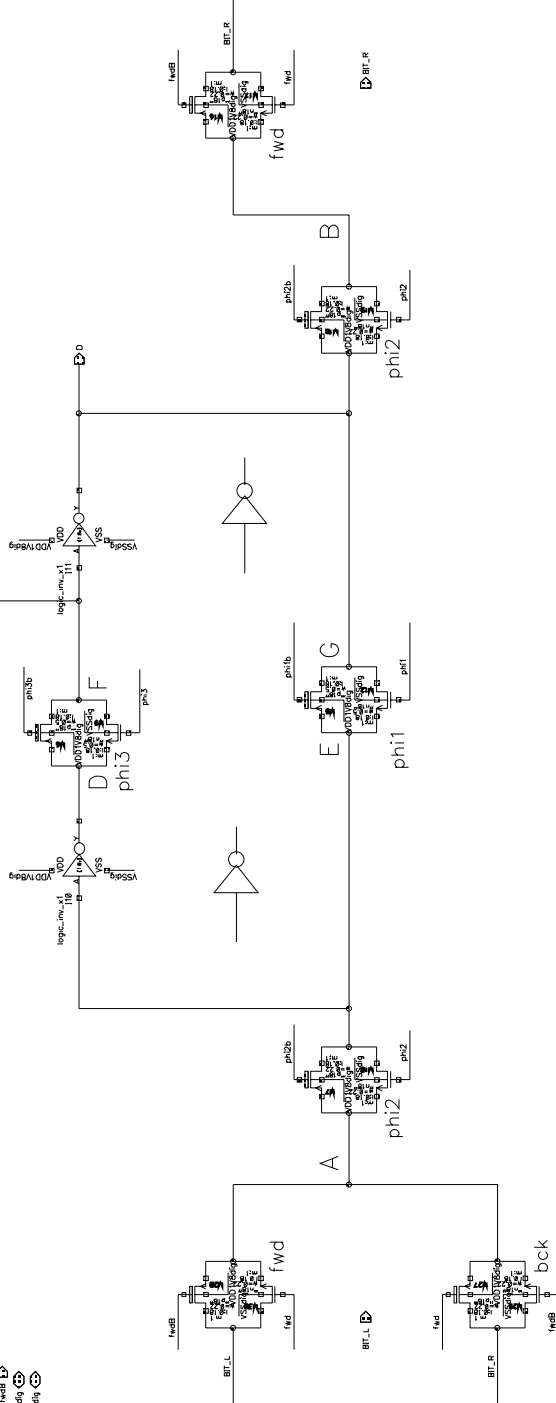


POWER UP	phi1 off phi2 on RstB on (low)
IN-SERVICE RESET	phi1 off phi2 on RstB pulsed on (low) during phi2
INVALID STATE	phi1 X phi2 off (low) RstB on (low)

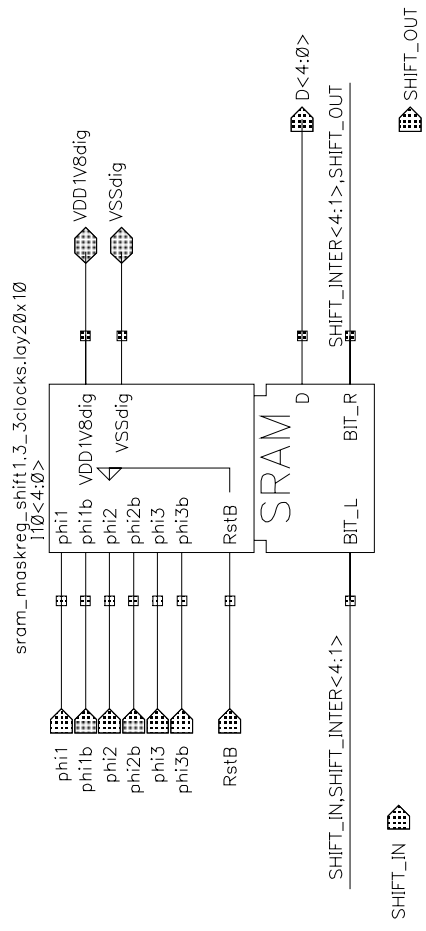


phi1 : Data Hold State  
 phi2 : Data transfer L>R (fwd=1)  
 phi3 : Data transfer R>L (fwd=0)

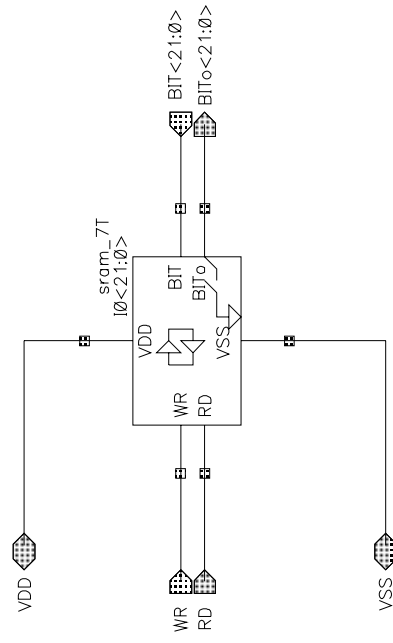
phi1  
 phi2  
 phi3  
 phi2b  
 phi1b  
 phi3b  
 fwd  
 bkwd  
 VDD  
 VSS



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	stamu_bkwd_shift1.5_blocks_10
Last QA Review	
Last Changed	Feb 2 14:07:46 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sram_maskreg_shift5_lay20x10
Last QA Review	
Last Changed	Feb 9 11:11:15 2007

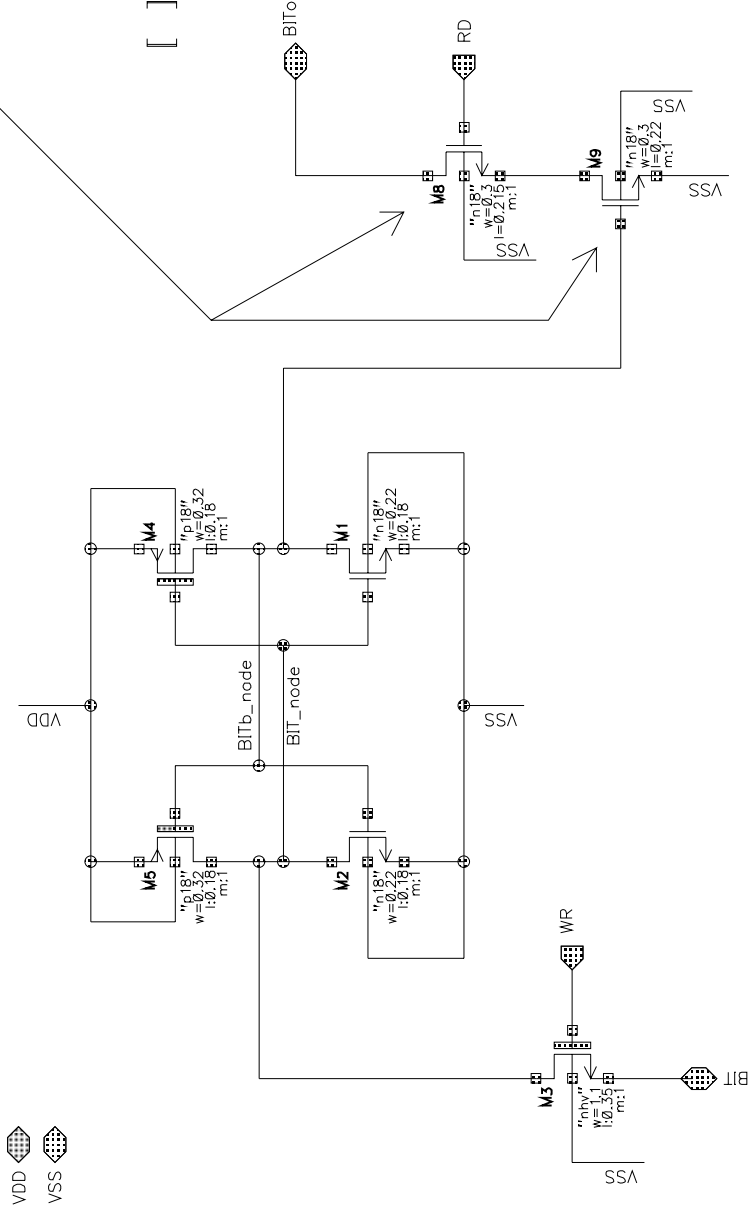


## RAL Microelectronics Group

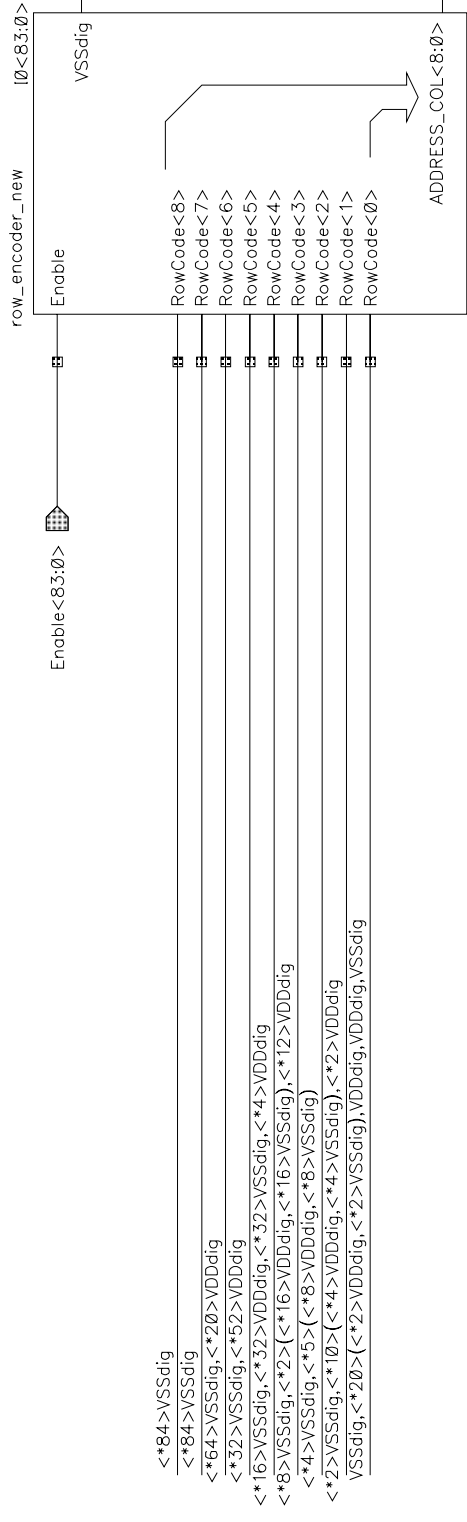
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_reg7.22
Last QA Review	
Last Changed	Jan 2 16:08:03 2007

NB: TRANSISTOR LENGTH REDUCED TO 0.22um FOR BETTER LAYOUT

[ ] RE-SIM CORNERS

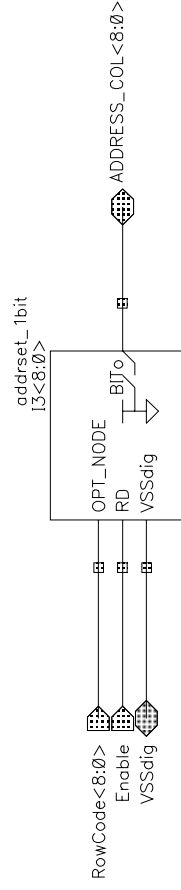


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_7T
Last QA Review	
Last Changed	Feb 19 18:38:06 2007



### RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	row_encoder_84
Last QA Review	
Last Changed	Jan 15 09:52:29 2007



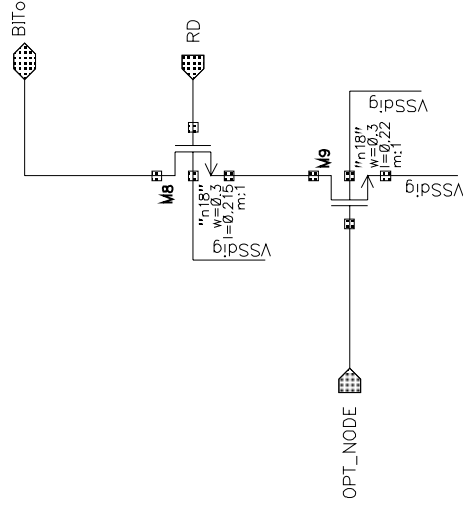
Set Row Code input to the unique row address: with net names in schematics; with repeated tie up/down cells in layout.

GRAY CODE should be used

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	row_encoder_new
Last QA Review	
Last Changed	Jan 15 09:39:09 2007



VSSd1g



Tie OPT\_NODE to either vdd or gnd to effectively set the address code that will be read when RD is asserted

### RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	addrset_1bit
Last QA Review	
Last Changed	Jan 15 09:35:52 2007

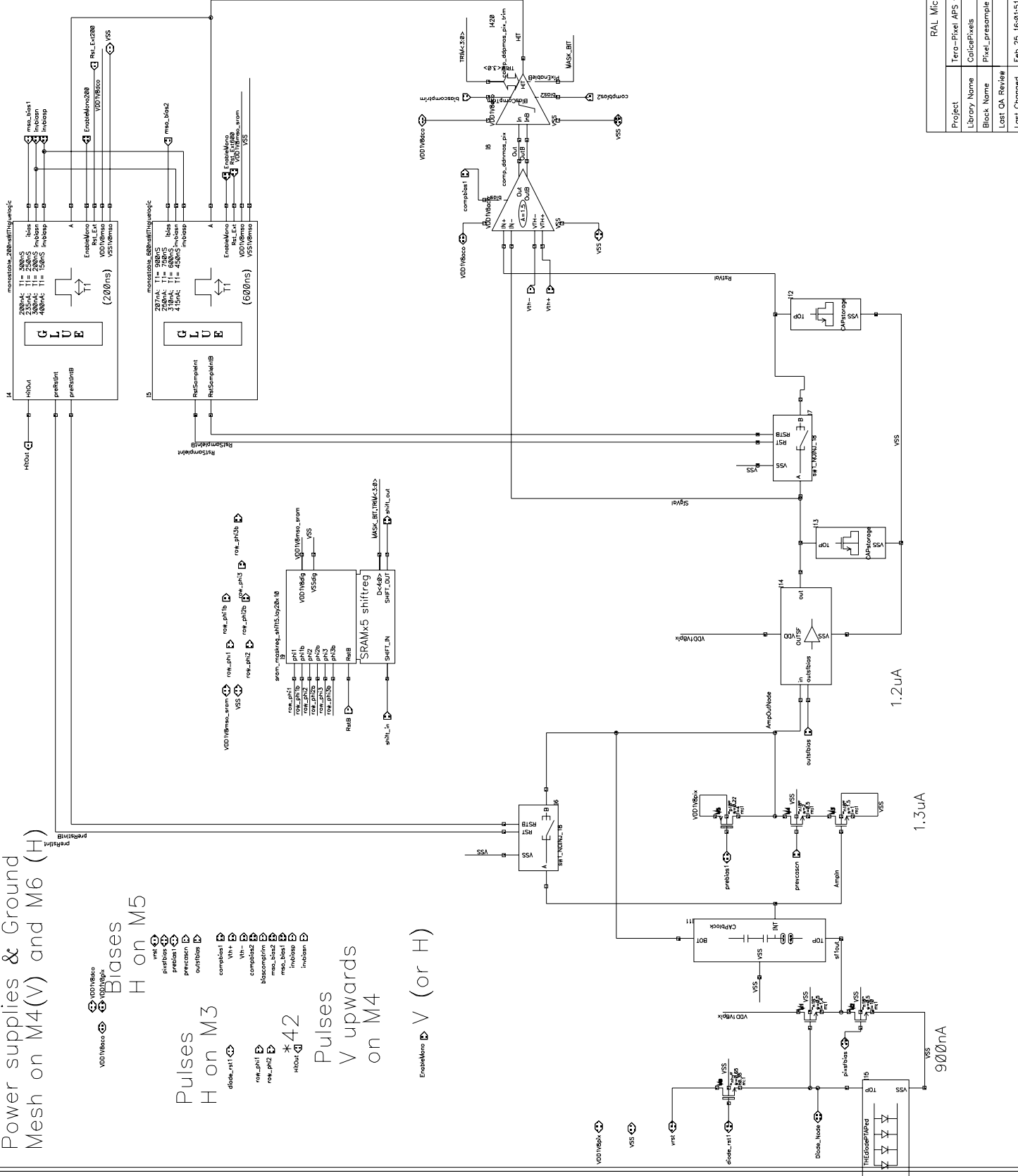
# Power supplies & Ground Mesh on M4(V) and M6 (H)

Biases  
H on M5

Pulses  
H on M3

\*42  
Pulses  
V upwards  
on M4

EnableM6 V (or H)

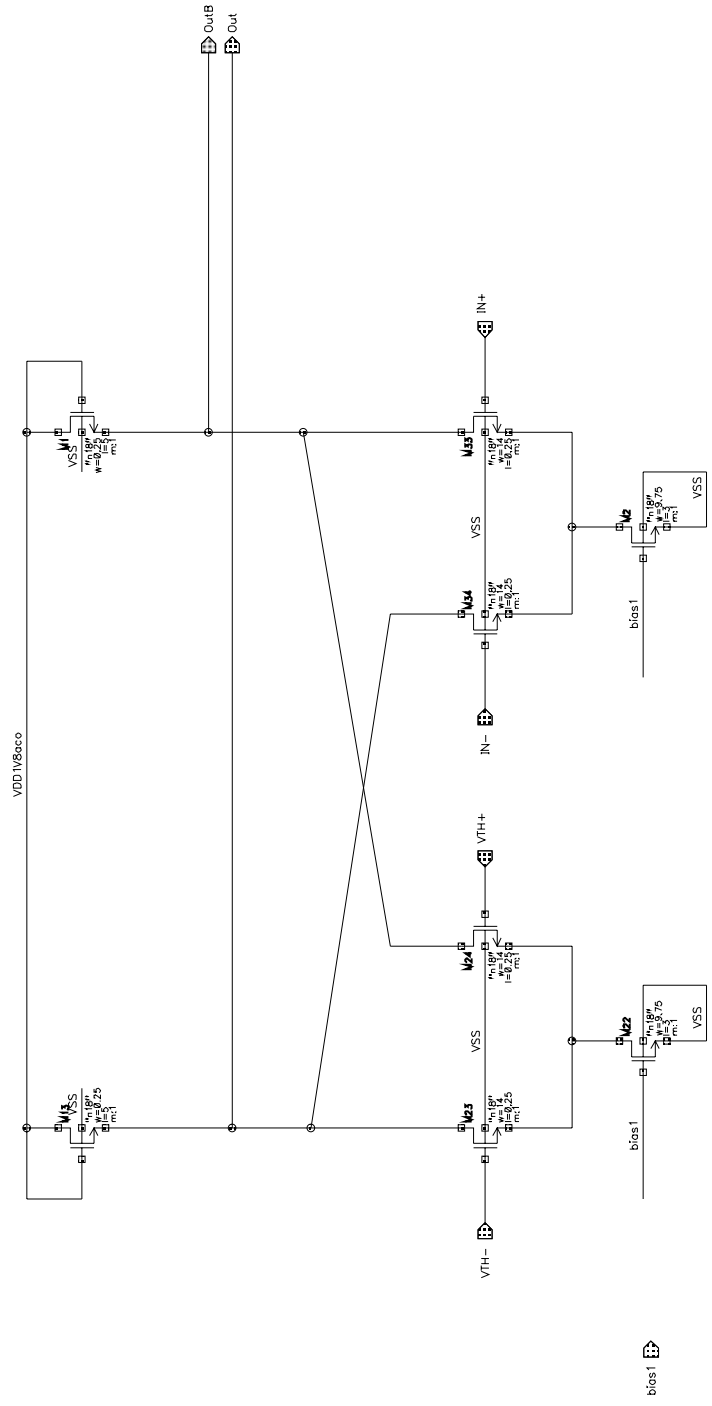


Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_presample
Last QA Review	
Last Changed	Feb 25 16:01:51 2007

RAL Microelectronics Group

VSS

VDD1V8acc



differential (10s of mV)  
 hit signal wired across  
 to pmos comparator at ro  
 logic

330nA

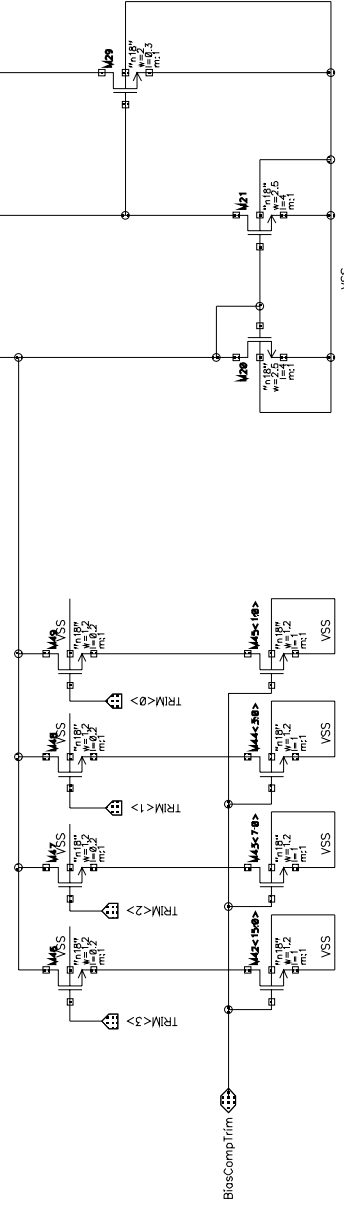
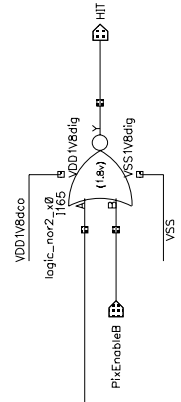
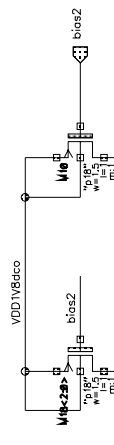
330nA

RAL Microelectronics Group	
Project	Tero-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	comp_dnrmos_pix
Last QA Review	
Last Changed	Feb 25 17:02:52 2007

VDD1V8dco

1uA 330nA

VSS



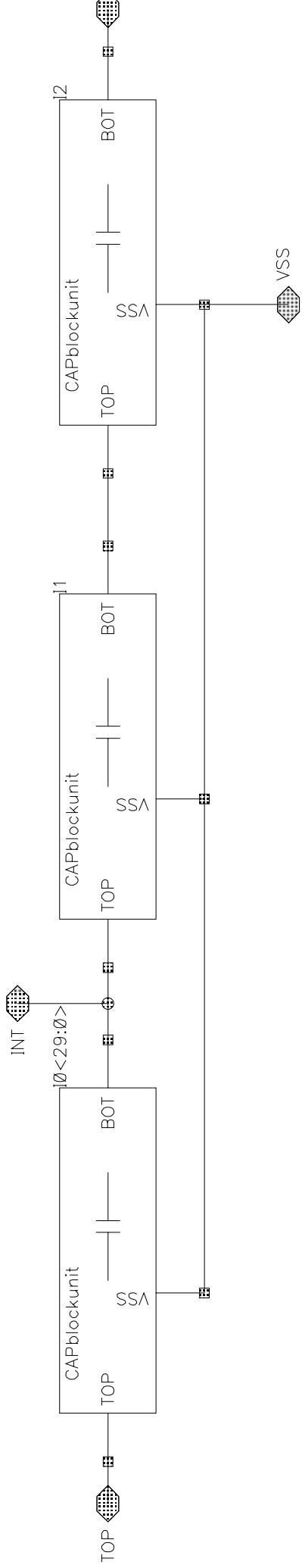
Hit\_Int

Hit\_Int = not Hit\_Int

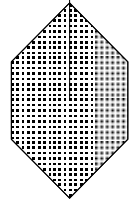
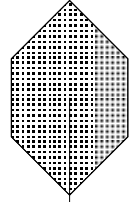
Hit\_Int = 0

Hit\_Int = 1

RAL Microelectronics Group	
Project	Tero-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	comp_dapmos_pix_trim
Last QA Review	
Last Changed	Feb 17 16:53:26 2007



BOT



TOP

$m:1$

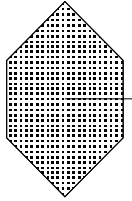
$l=1$

$w_{Total}=1$

$w=1$

$n_{wcap3t}$

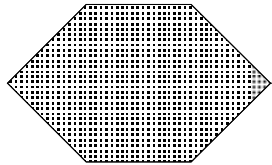
$V_S$



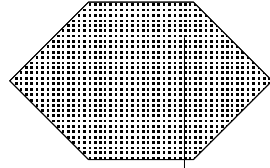
$c_{nwmmos\_thn3t}$

$C_0$

VSS



TOP



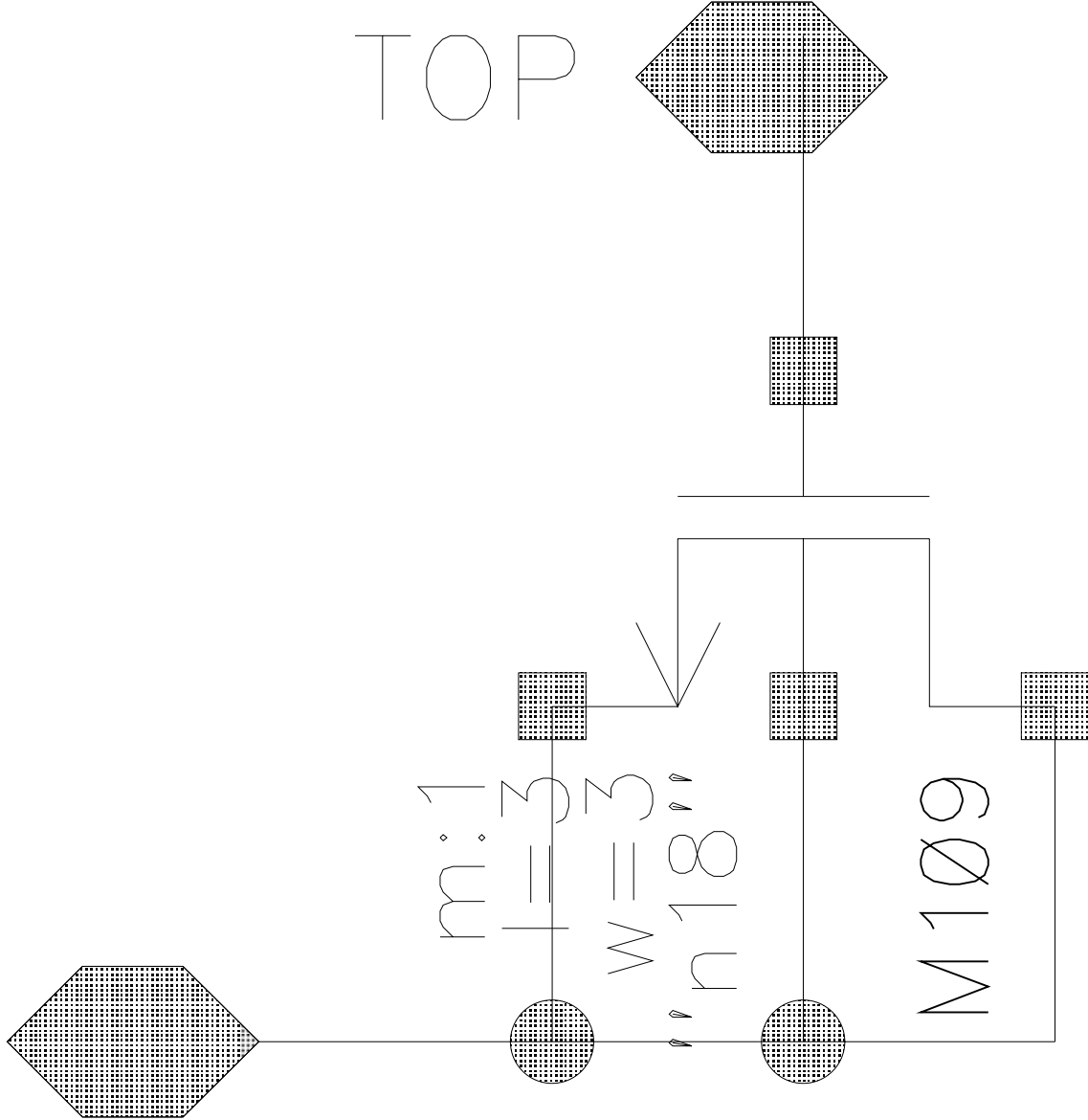
m:1

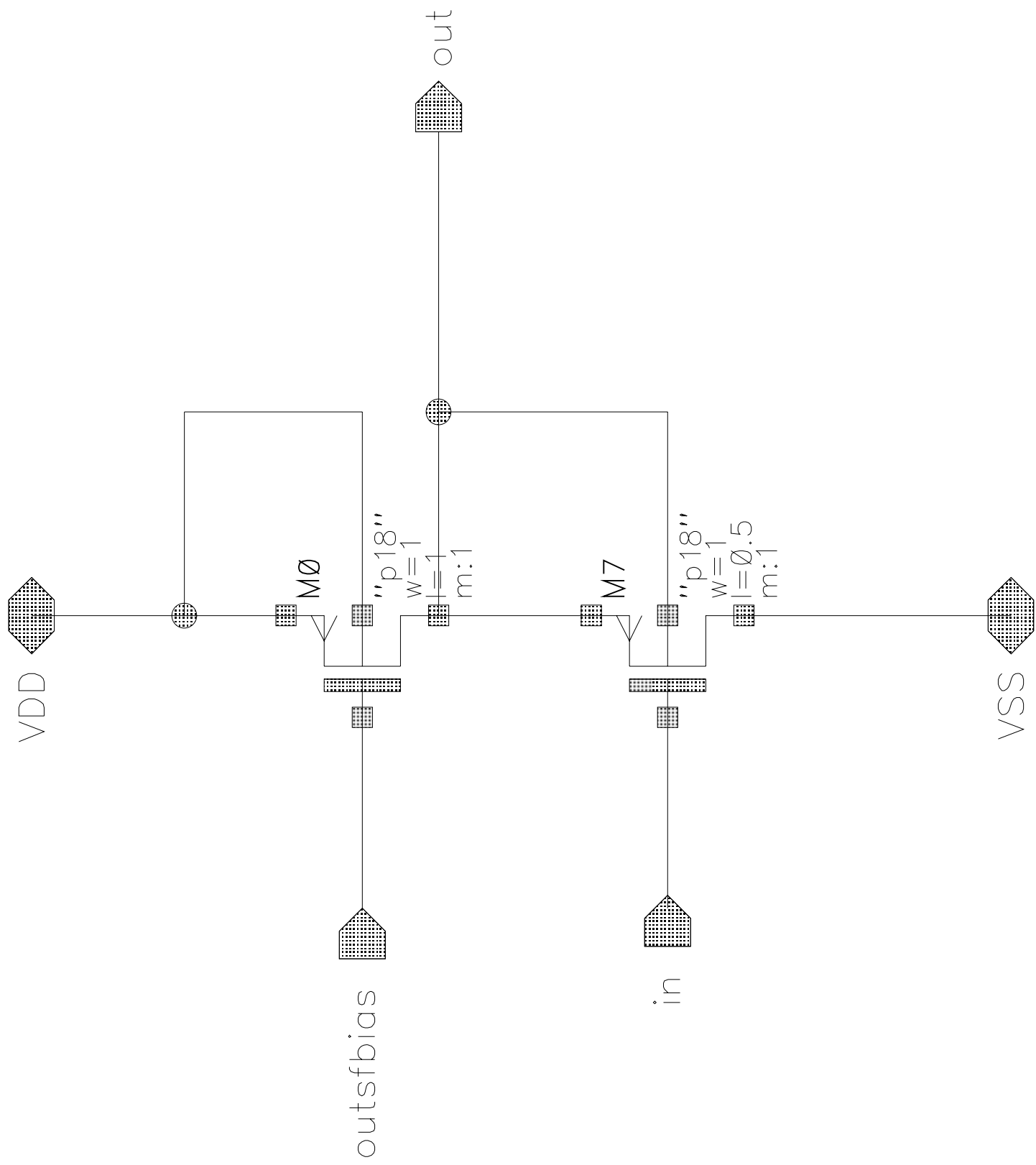
l=3

w=3

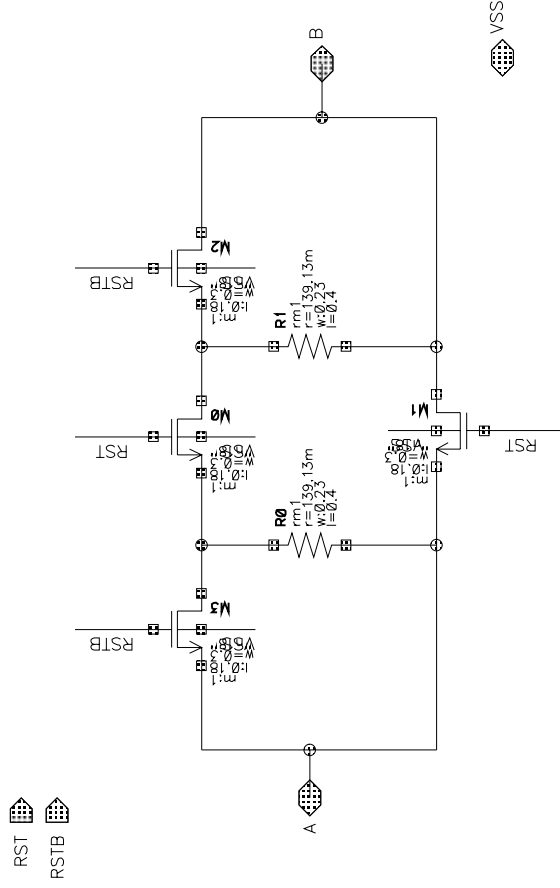
n18

M109



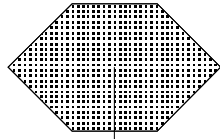






RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sw1_NOINUJ_18
Last QA Review	
Last Changed	Feb 17 18:13:08 2007

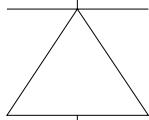
TOP



m:1

area = 11.73

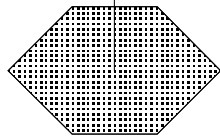
''dnwell''



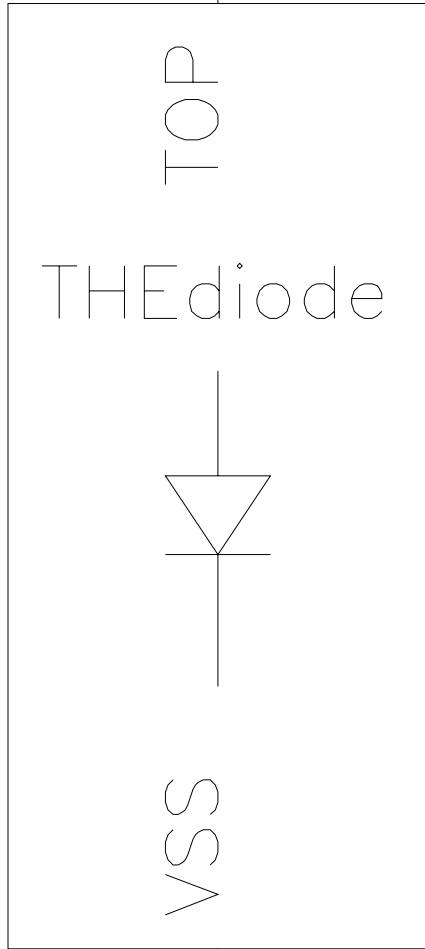
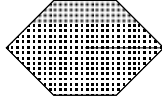
D1



VSS

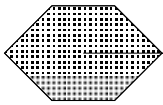


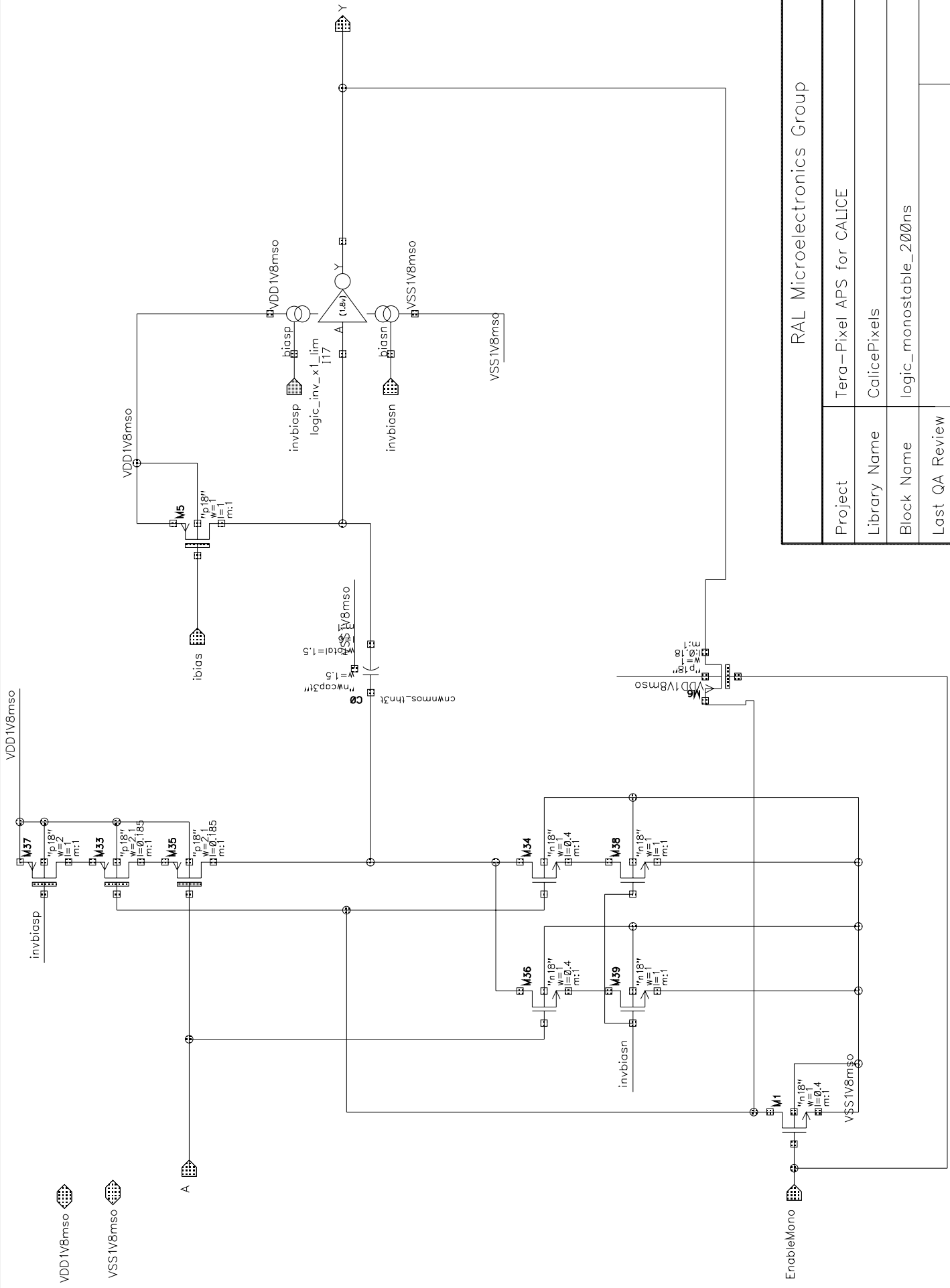
TOP



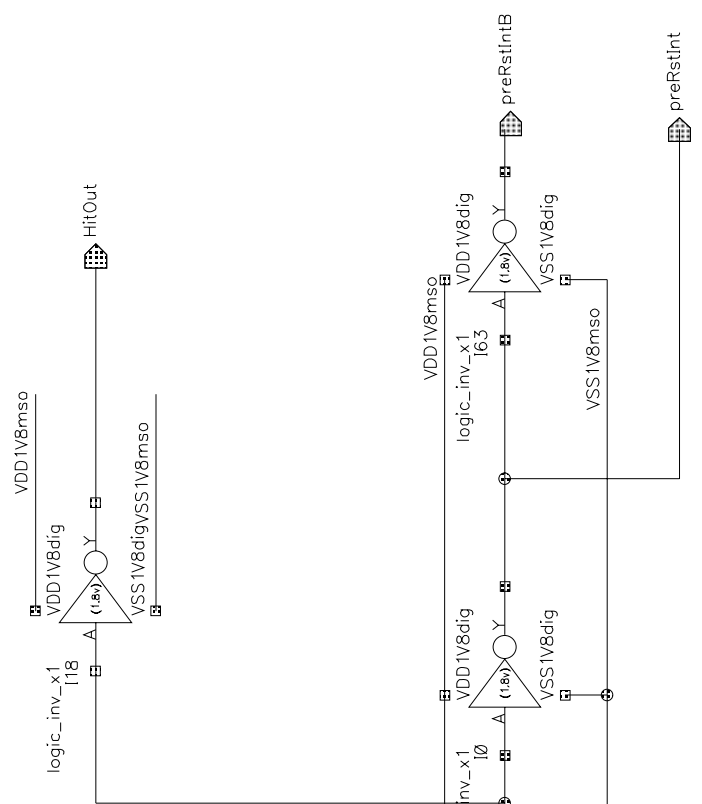
I0 < 3:0 >

VSS





RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_monostable_200ns
Last QA Review	
Last Changed	Feb 14 10:50:33 2007



**logic\_monostable\_200ns** I5

200ns: T1= 300ns  
 235ns: T1= 250ns  
 300ns: T1= 200ns  
 400ns: T1= 150ns

ibias  
 invbiasn  
 invbiasp

A

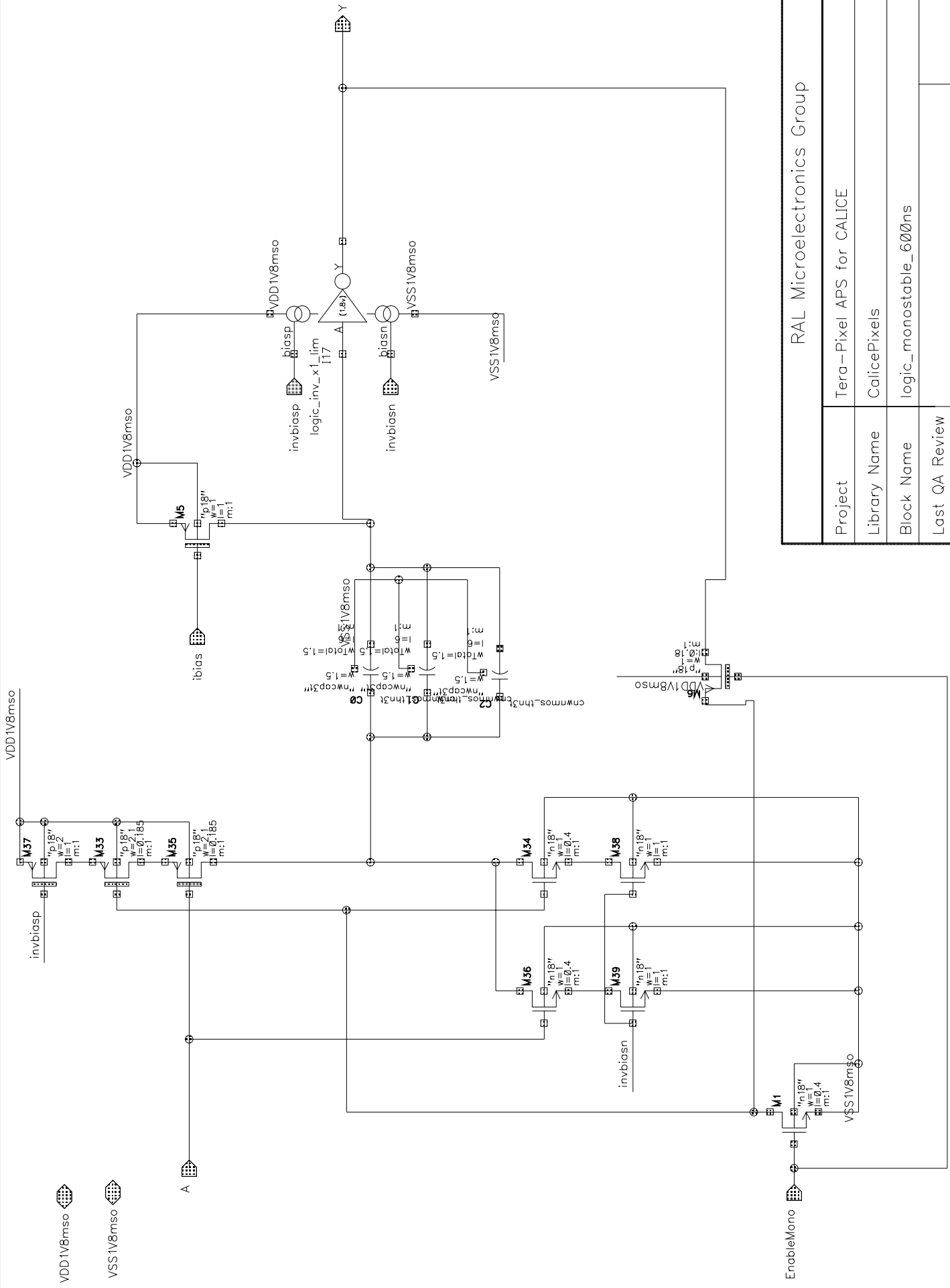
EnableMono

VDD1V8mso  
 VSS1V8mso

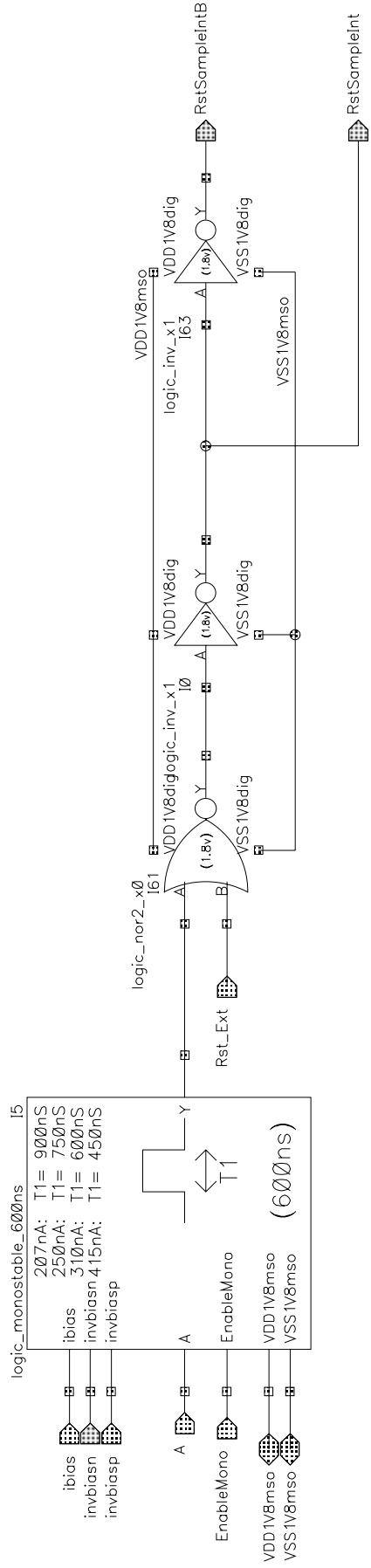
(200ns)

RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable_200nsWITHgluelogic
Last QA Review	
Last Changed	Feb 13 11:47:56 2007

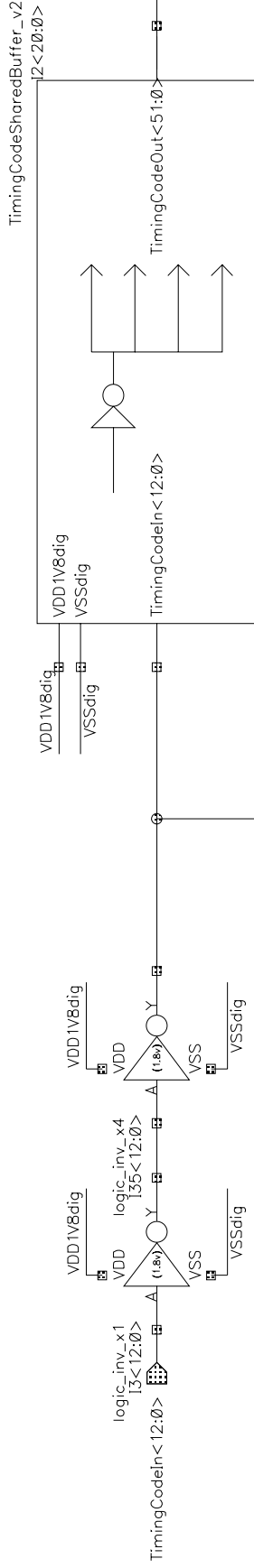


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_monostable_600ns
Last QA Review	
Last Changed	Feb 14 10:48:02 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable_600nsWITHgluelogic
Last QA Review	
Last Changed	Feb 14 10:52:08 2007

VDD1V8dig  
VSSdig



x4 buffers drive the full column length (84 pix)

Timing Code in the column is in inverted format

Correct polarity output to next column (this cell again)

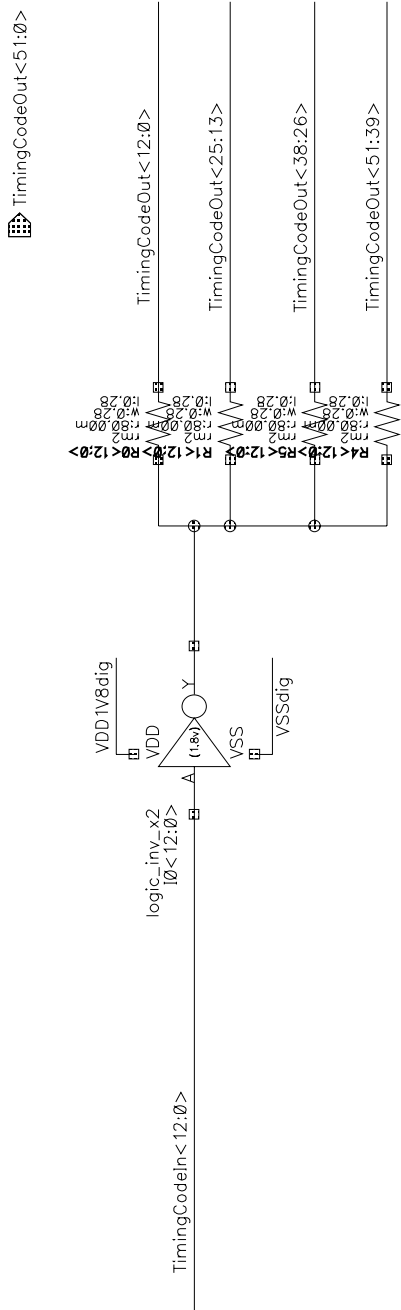
a local buffer drives 4 rows worth of SRAM cells buffers are distributed between the four rows to save space.

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	TimingCodeDistribution_v2
Last QA Review	
Last Changed	Feb 27 17:50:55 2007

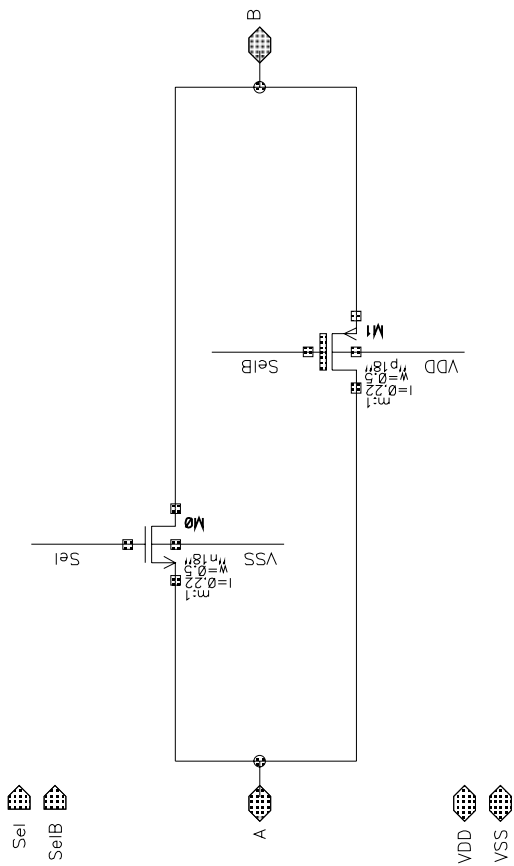


VDD1V8dig  
VSSdig

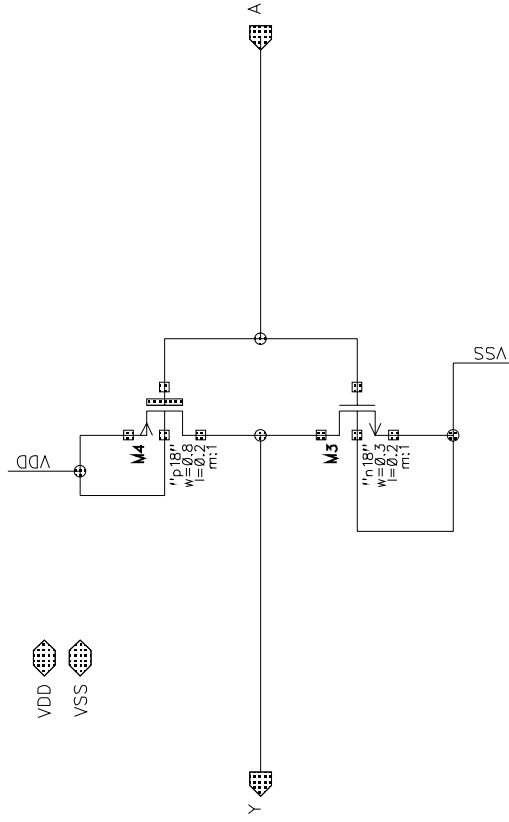
TimingCodeIn < 12:0 >



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	TimingCodeSharedBuffer_v2
Last QA Review	
Last Changed	Feb 20 09:23:44 2007

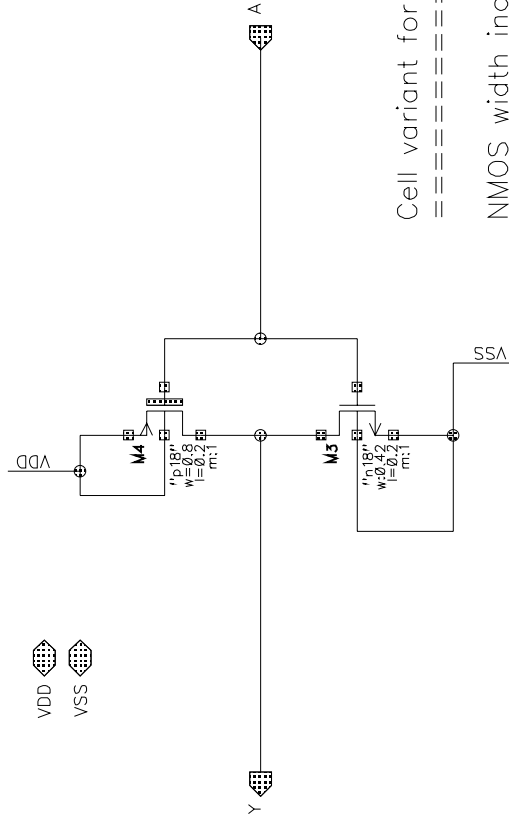


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sw1_18
Last QA Review	
Last Changed	Sep 28 11:41:21 2006



RAL Microelectronics Group

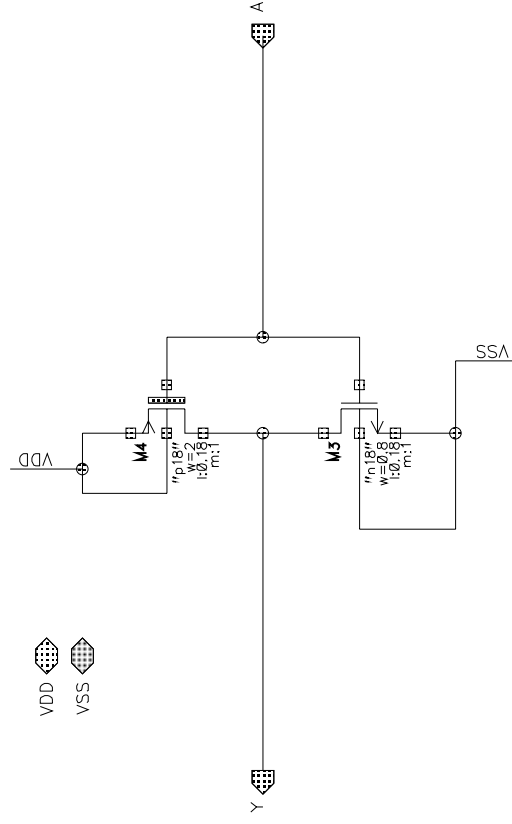
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x0
Last QA Review	
Last Changed	Sep 28 11:41:11 2006



Cell variant for layout ".lay1"

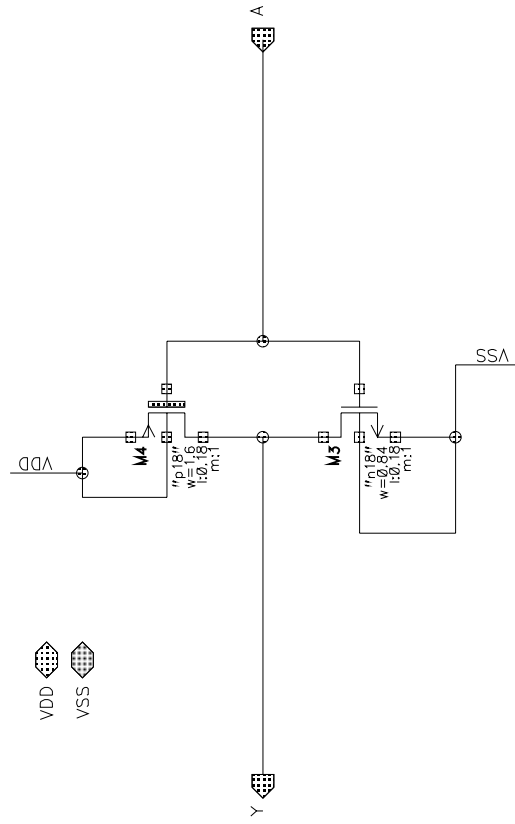
NMOS width increased from 0.3 to 0.42um

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x0.lay1
Last QA Review	
Last Changed	Jan 11 15:41:07 2007



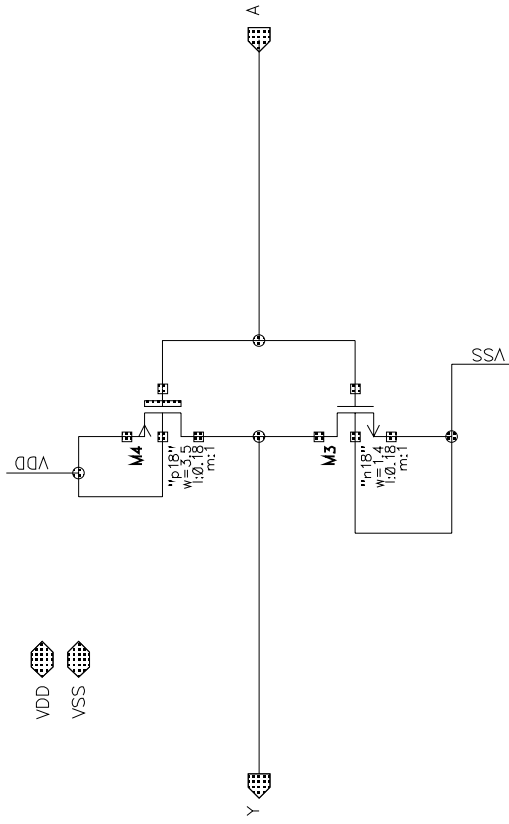
## RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006



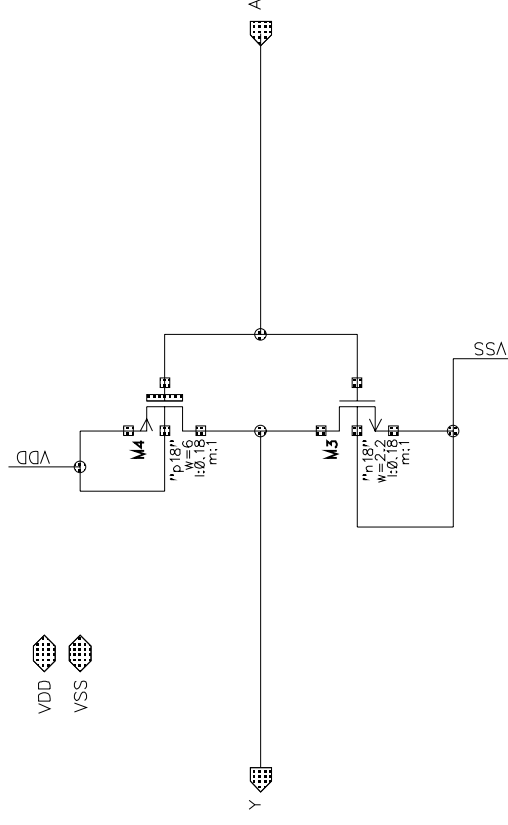
RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1.lay2
Last QA Review	
Last Changed	Feb 12 18:45:22 2007



## RAL Microelectronics Group

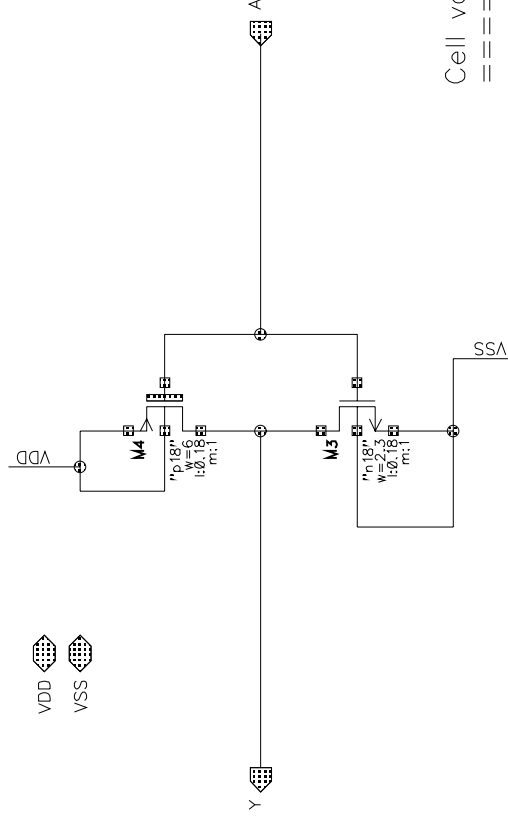
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x2
Last QA Review	
Last Changed	Sep 28 11:45:54 2006



RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3
Last QA Review	
Last Changed	Sep 28 11:42:15 2006

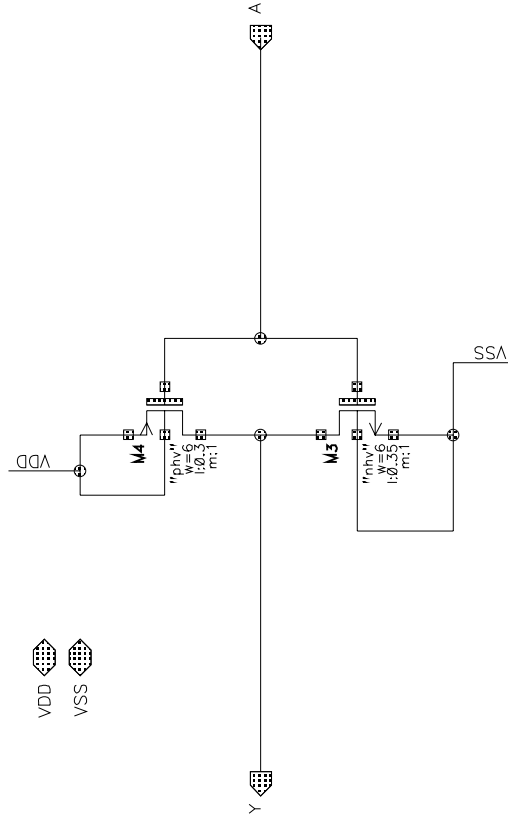




Cell variant for layout ".lay1"

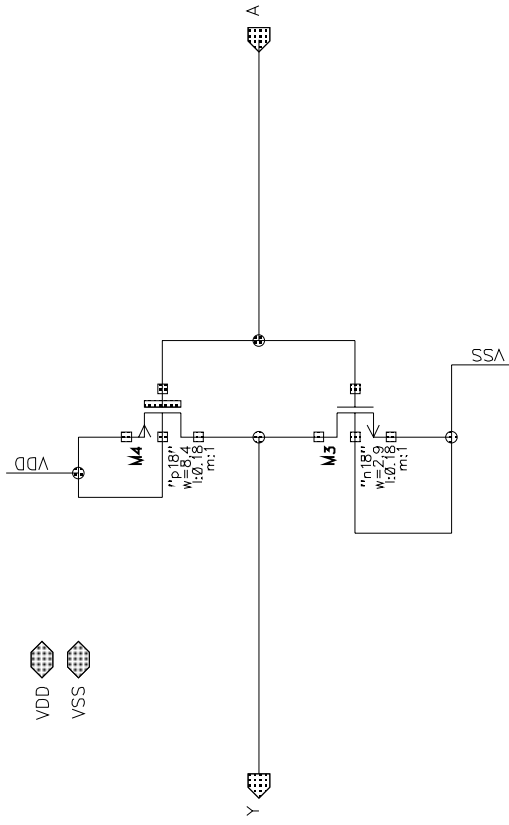
=====  
 NMOS width increased from 2.2 to 2.3

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3.lay1
Last QA Review	
Last Changed	Jan 10 14:27:47 2007



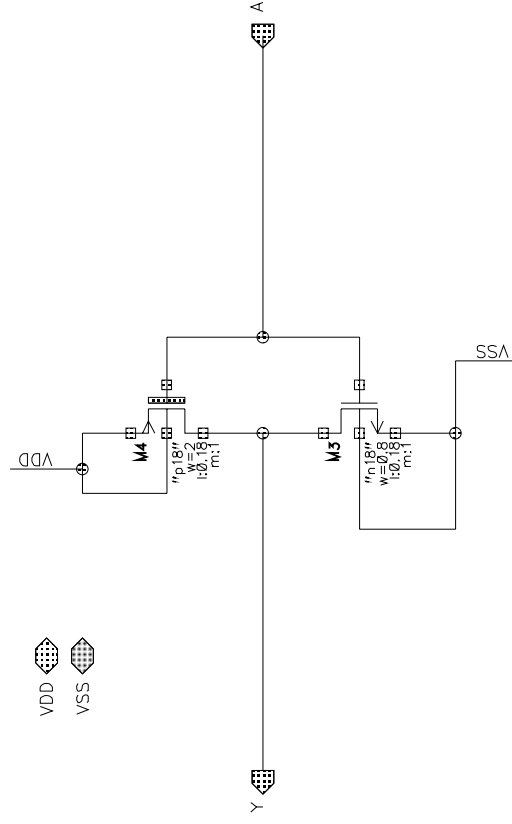
### RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3_hv
Last QA Review	
Last Changed	Sep 29 15:18:48 2006



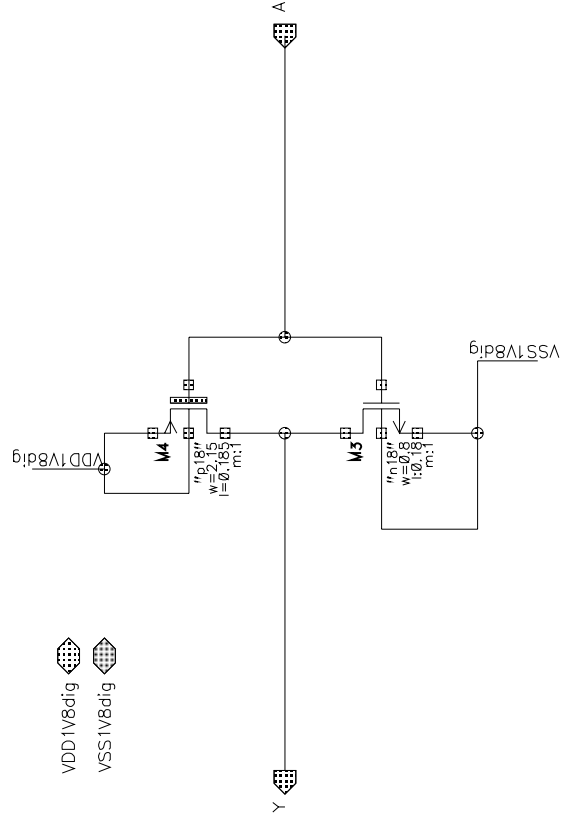
RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x4
Last QA Review	
Last Changed	Sep 28 11:42:24 2006



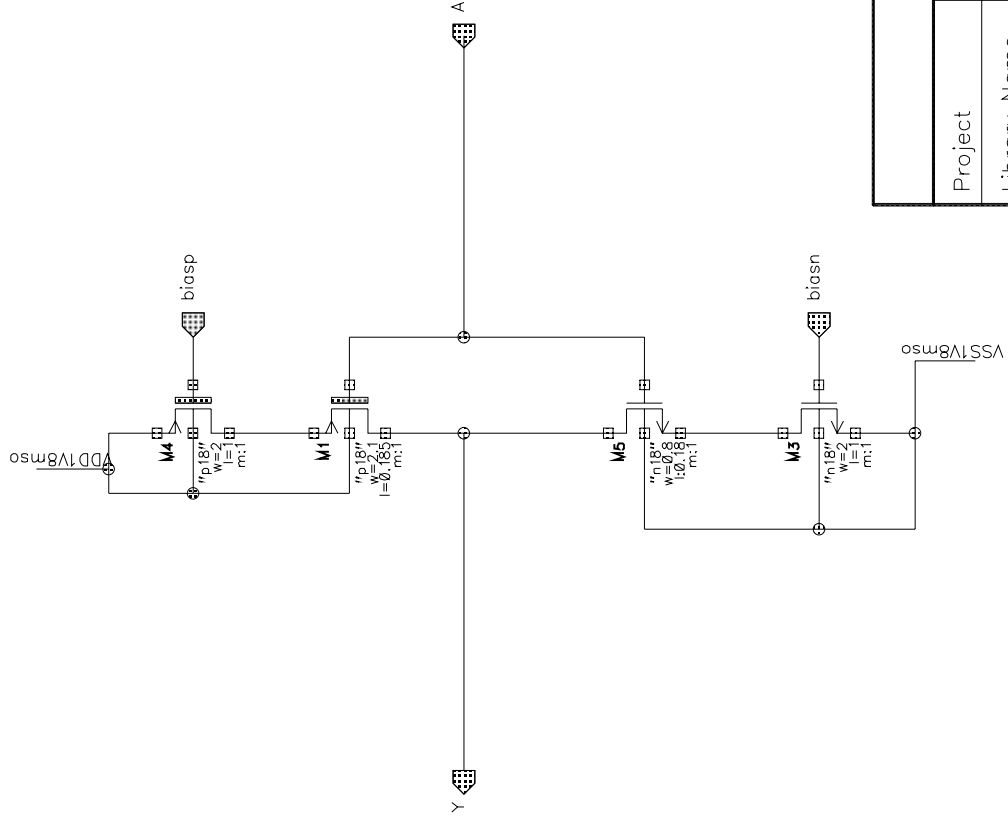
### RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006



RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Feb 5 17:55:09 2007

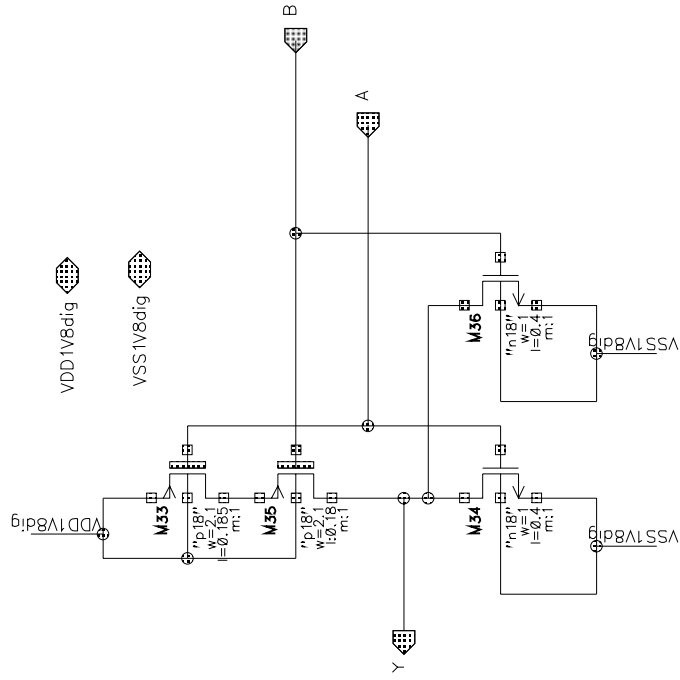


VDD1V8mso

VSS1V8mso

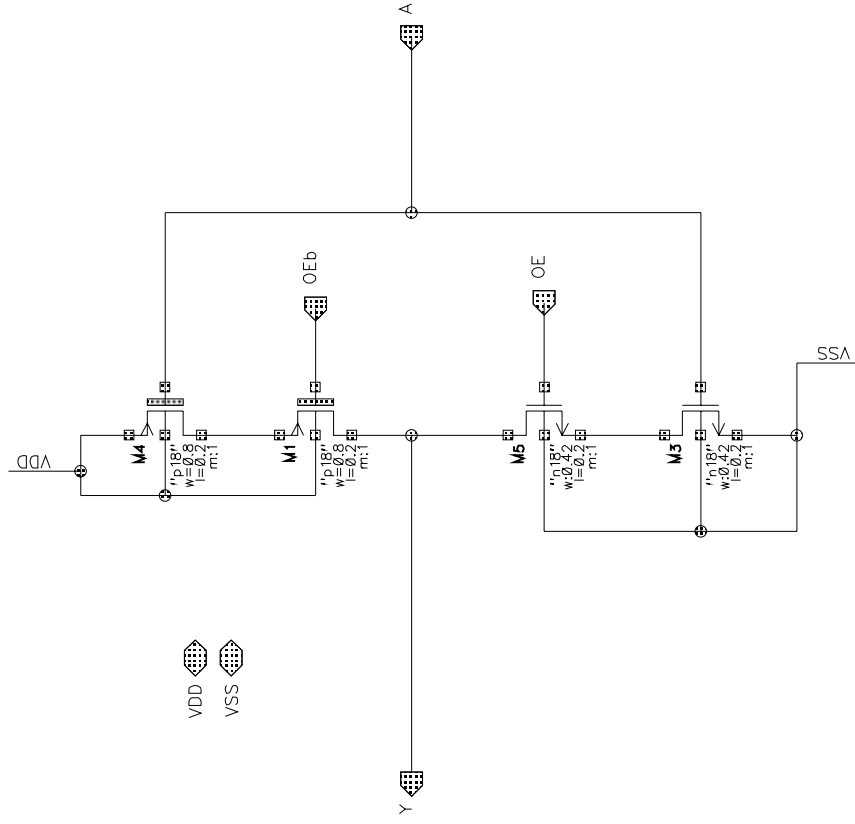
RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1_lim
Last QA Review	
Last Changed	Jan 24 17:38:39 2007



RAL Microelectronics Group

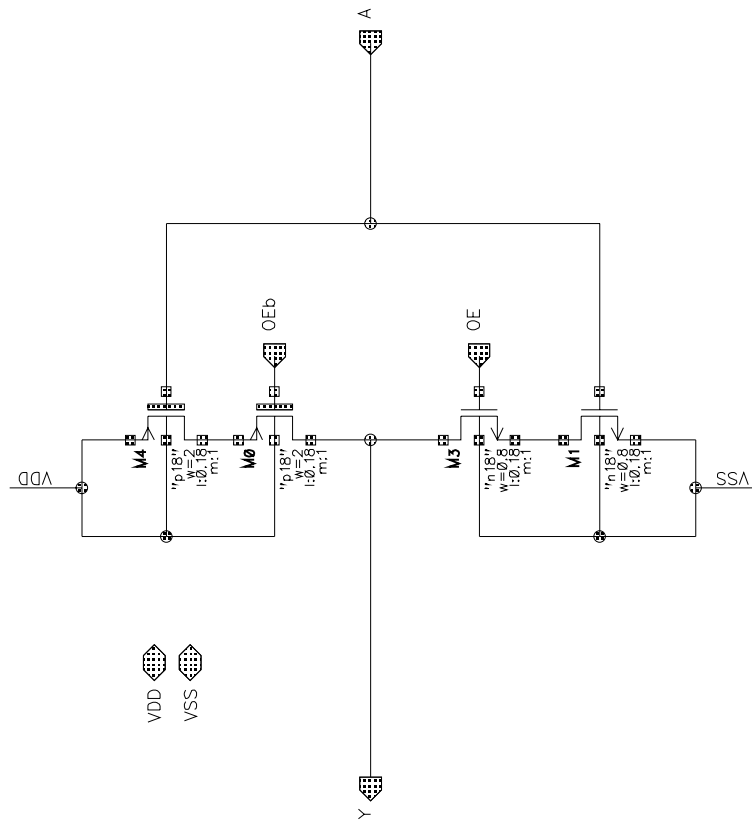
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_nor2_x0
Last QA Review	
Last Changed	Feb 5 18:38:32 2007



RAL Microelectronics Group

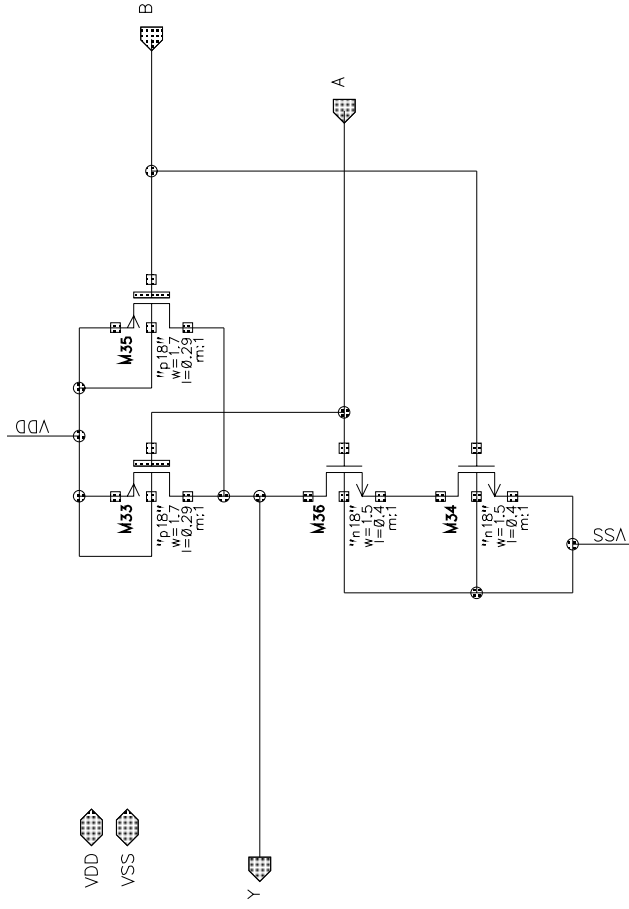
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x0c
Last QA Review	
Last Changed	Feb 12 18:49:59 2007





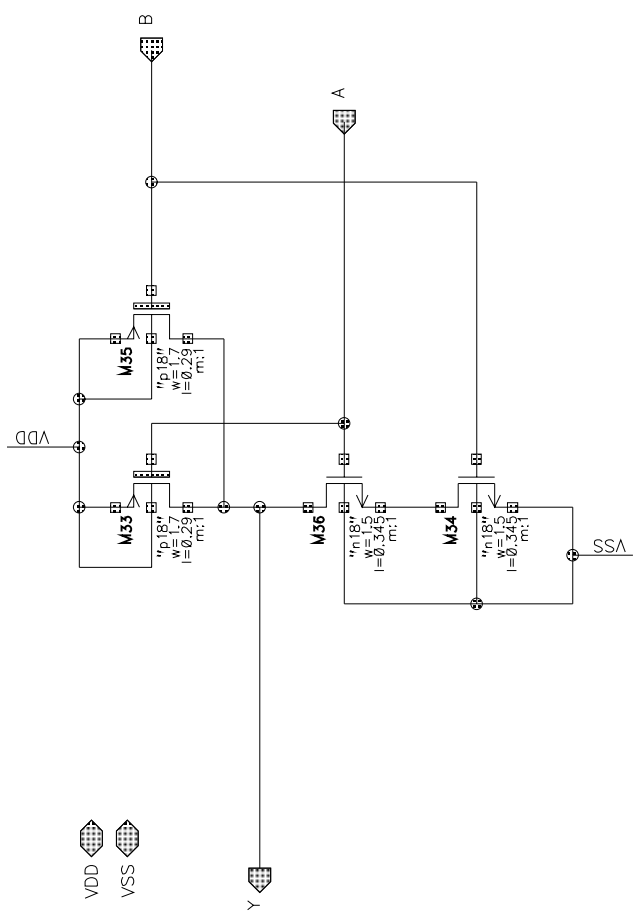
RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x1
Last QA Review	
Last Changed	Sep 28 11:42:37 2006



RAL Microelectronics Group

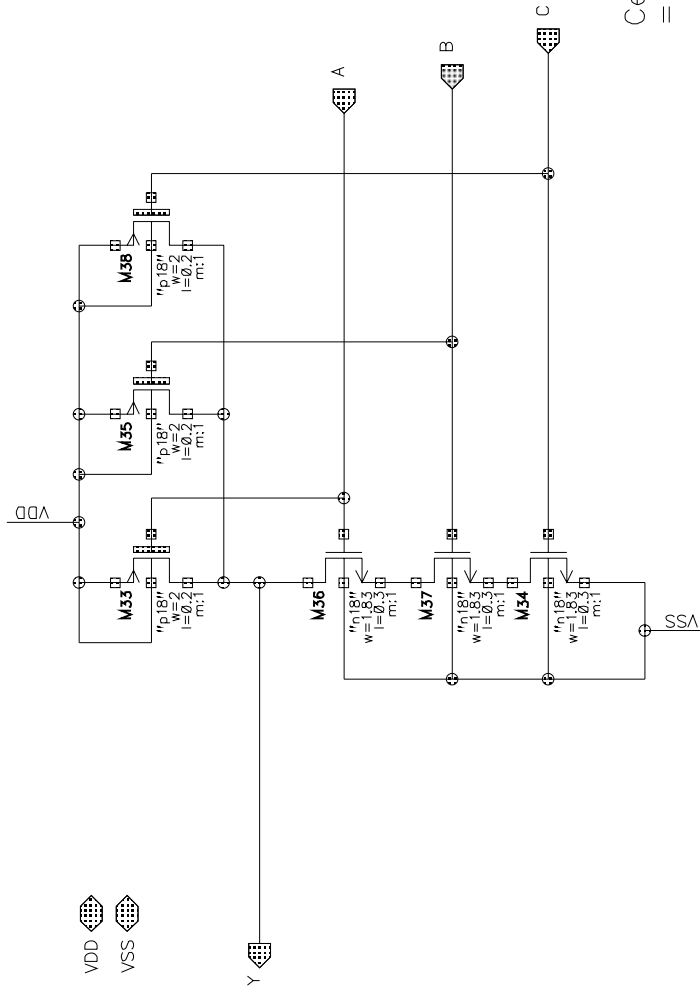
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand2_x0
Last QA Review	
Last Changed	Jan 4 09:07:25 2007



Cell variant for layout ".lay1"

NMOS lengths reduced from 0.4 to 0.345

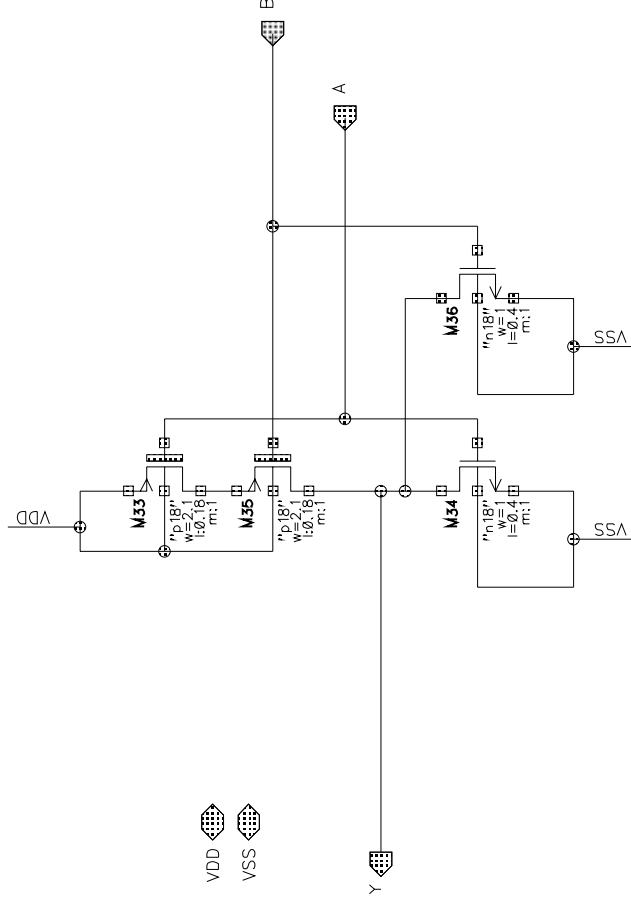
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand2_x0.lay2
Last QA Review	
Last Changed	Feb 5 16:11:45 2007



Cell variant for layout ".lay1"

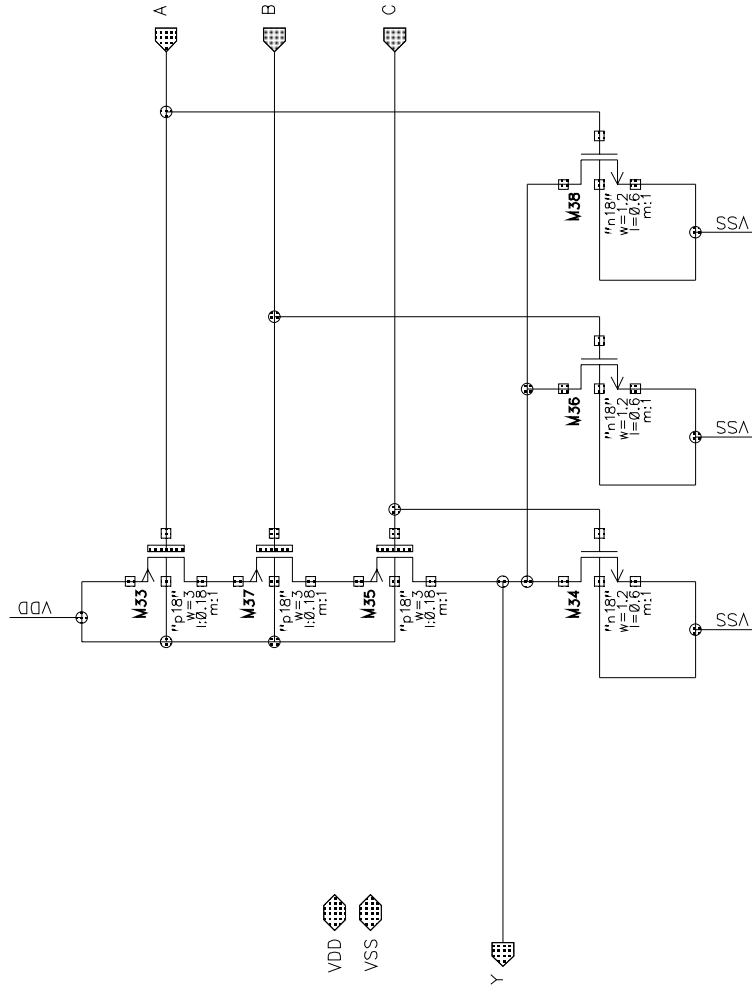
NMOS width reduced from 1.9 to 1.83

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand3_x0.lay1
Last QA Review	
Last Changed	Jan 10 14:24:41 2007



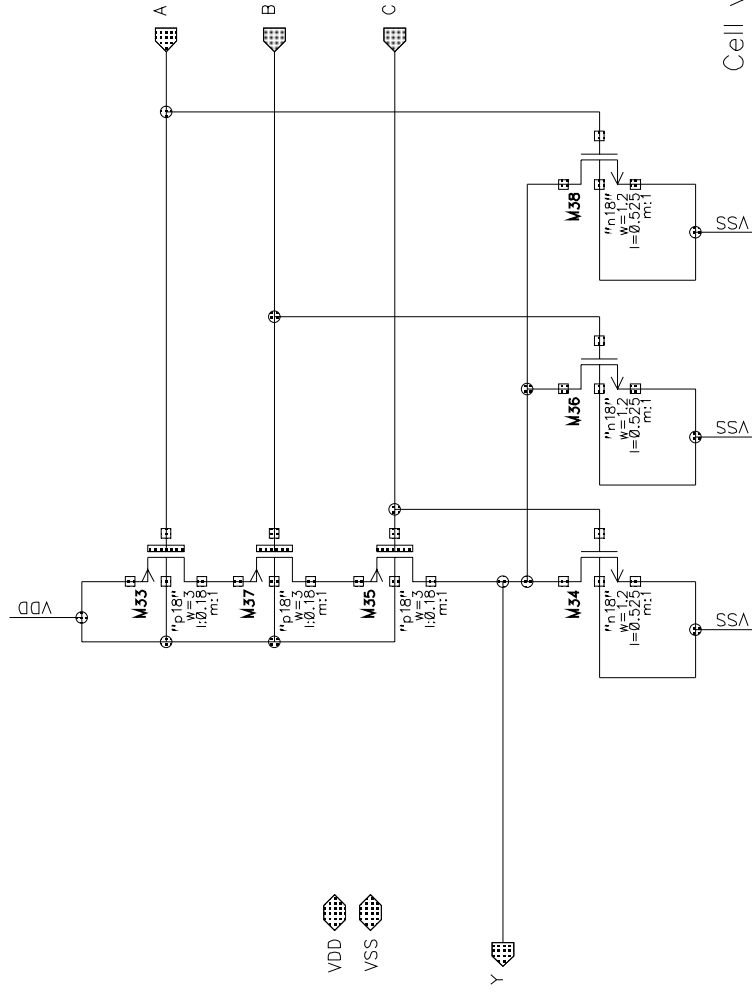
RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor2_x0
Last QA Review	
Last Changed	Sep 28 11:45:21 2006



RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_x0
Last QA Review	
Last Changed	Jan 10 14:06:59 2007



VDD   
 VSS 

=====  
 Cell variant for layout: ".lay1"  
 =====

NMOS length reduced from 0.6 to 0.525

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_x0.lay1
Last QA Review	
Last Changed	Jan 10 14:20:51 2007