

VDD0  
 NORTH: 3+3  
 EAST: 3+3  
 SOUTH: 4+4  
 WEST: 3+2

VDD1/6defg  
 NORTH: 4+4  
 EAST: 4+4  
 SOUTH: 5+5  
 WEST: 1+1

VDD2/4defg  
 NORTH: 3+3  
 EAST: 3+3  
 SOUTH: 3+3  
 WEST: 3+3

VDD2/5defg  
 NORTH: 2  
 EAST: 2  
 SOUTH: 1  
 WEST: 1

VDD1/8defg  
 NORTH: 3+3  
 EAST: 3+3  
 SOUTH: 3+3  
 WEST: 3+3

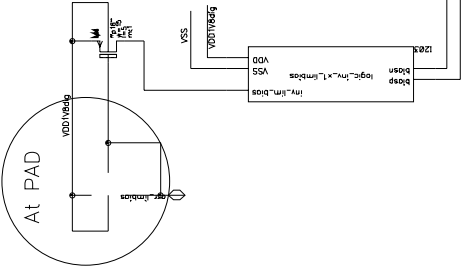
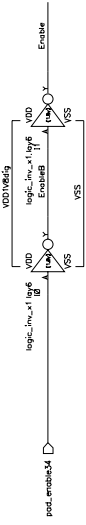
VDD1/8defg  
 NORTH: 4+4  
 EAST: 4+4  
 SOUTH: 4+4  
 WEST: 4+4

VDD1/8defg  
 NORTH: 3+3  
 EAST: 3+3  
 SOUTH: 3+3  
 WEST: 3+3

VDD1/8defg  
 NORTH: 3+3  
 EAST: 3+3  
 SOUTH: 3+3  
 WEST: 3+3

VRS1  
 NORTH: 2  
 EAST: 2  
 SOUTH: 2  
 WEST: 2

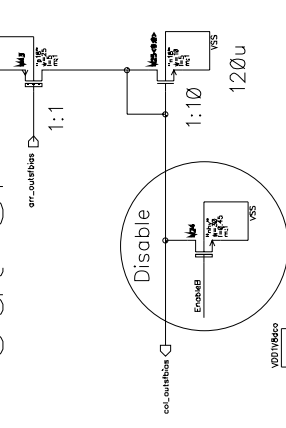
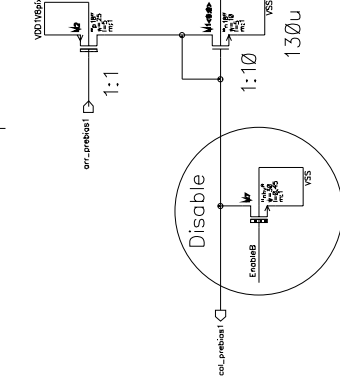
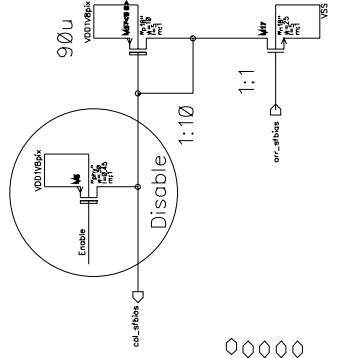
Rev. Management Form	
DATE:	1997/04/22 02:00:00
DESIGNER:	WANG, JIN
CHK'D BY:	WANG, JIN
DATE:	1997/04/22 02:00:00



## Pixel SF

## Preamp Bias

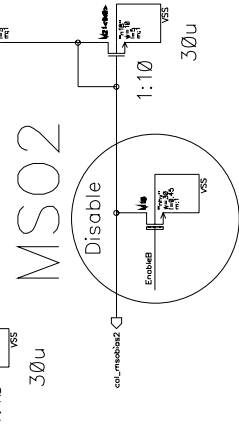
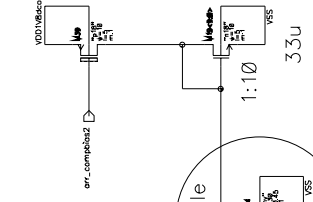
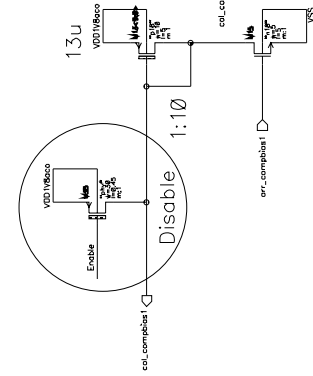
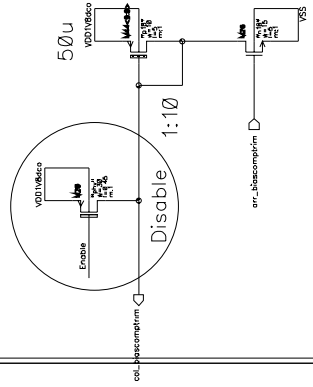
## Out SF



- VDD1V8B0 <
- VDD1V8B0 <
- VDD1V8B0 <
- VDD1V8B0 <
- VSS <

## MSO1

## Comparator

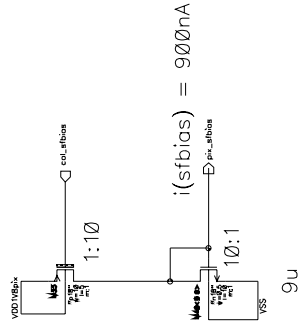


# ARRAY CIRCUITS

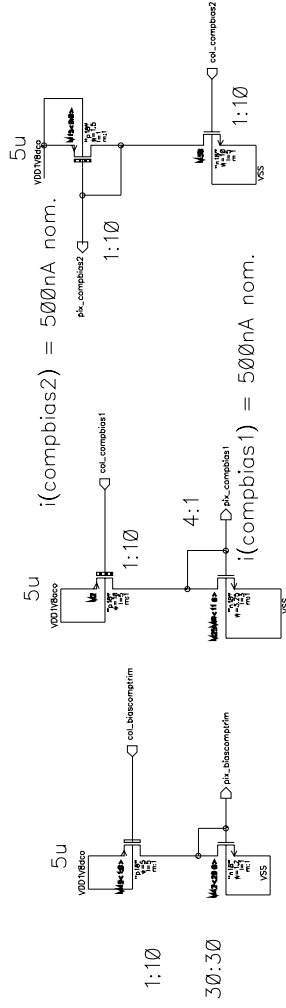
RAL Microelectronics Group	
Project	Tera-Pixel MPS for CALICE
Library Name	calice_circuits
Block Name	Pixel_preamp_bias_0rr_v1.3
Last CA Review	
Last Changed	Apr. 30 09:07:20 2007

VDD1V8p0  
 VDD1V8p0  
 VDD1V8p0  
 VDD1V8p0  
 VSS

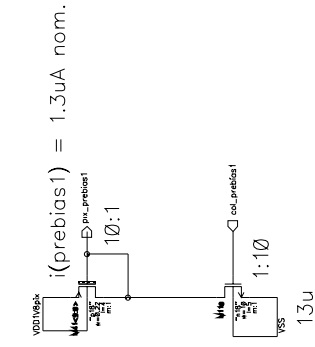
# Pixel SF



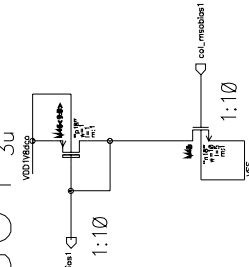
# Comparator Bias



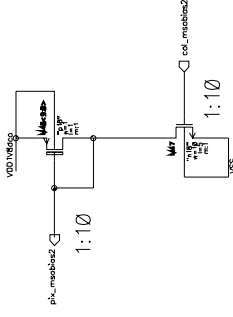
# Preamp Bias



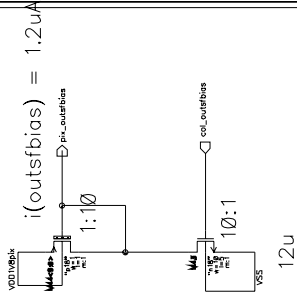
# MSO1



# MSO2

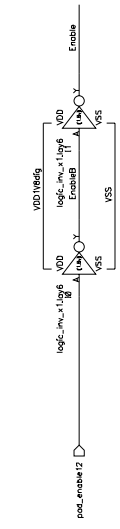


# Out SF

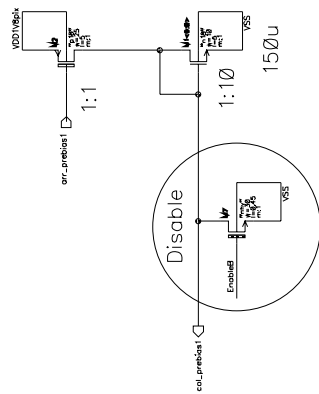
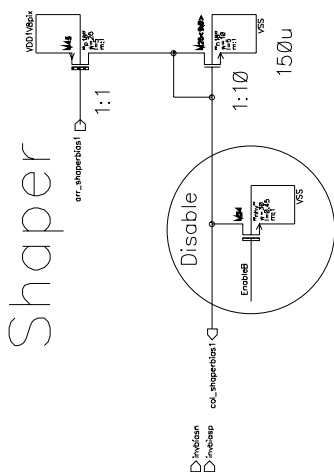
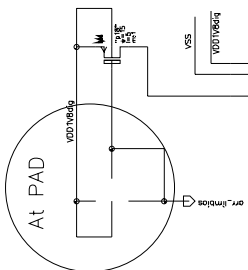


# COLUMN CIRCUITS

Project	RAL Microelectronics Group
Library Name	Tera-Pixel APS for CALICE
Block Name	CollicaPixels
Last QA Review	phobias_promptRT_col_v1.2
Last Changed	Mar 8 14:21:08 2007

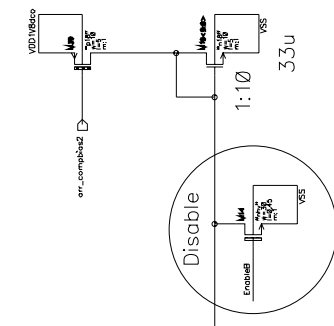
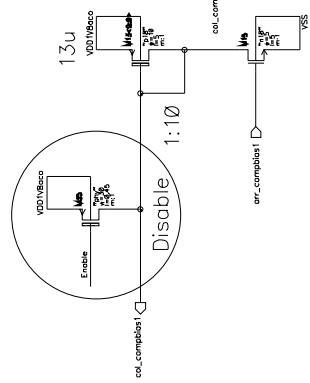
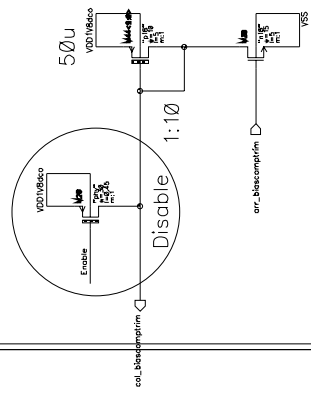


# Preamp Bias

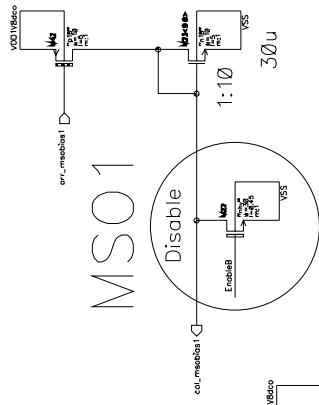


- VDD1V850
- VDD1V850
- VDD1V850
- VDD1V850
- VSS

# Comparator



# MISO1

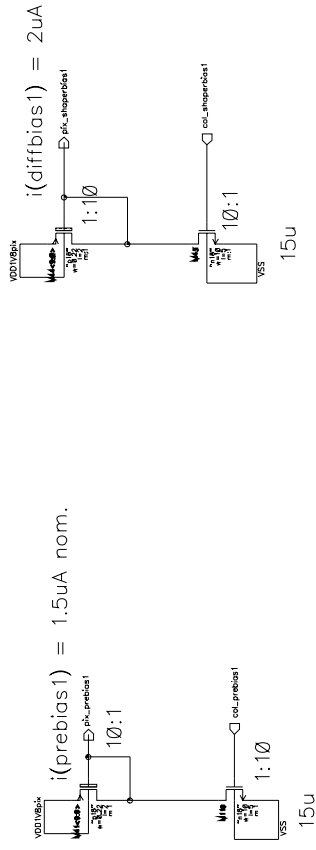


# ARRAY CIRCUITS

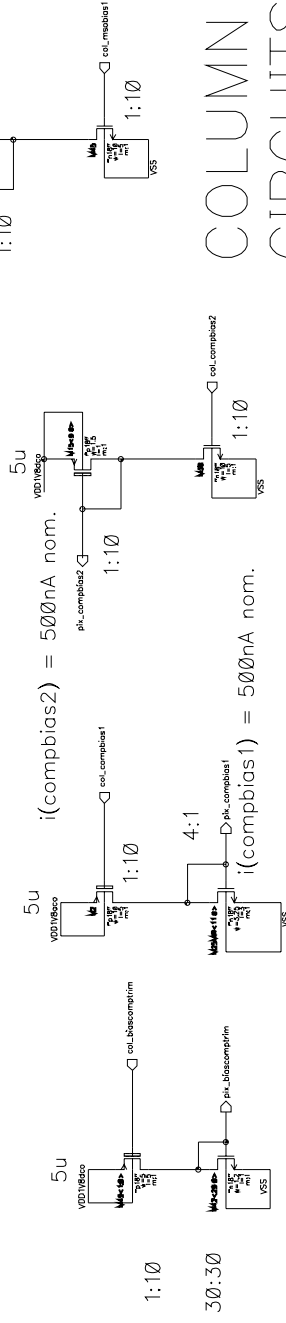
RAL Microelectronics Group	
Project	Tera-Fixel APS for CALICE
Library Name	calice_circuits
Block Name	Fixed_preshape_bias_arr_v1.3
Last QA Review	
Last Changed	Mar 26 16:12:09 2007

VDD/VBico  
 VDD/VBico  
 VDD/VBino  
 VDD/VBico  
 VSS

# Preamp Bias Shaper



# Comparator Bias



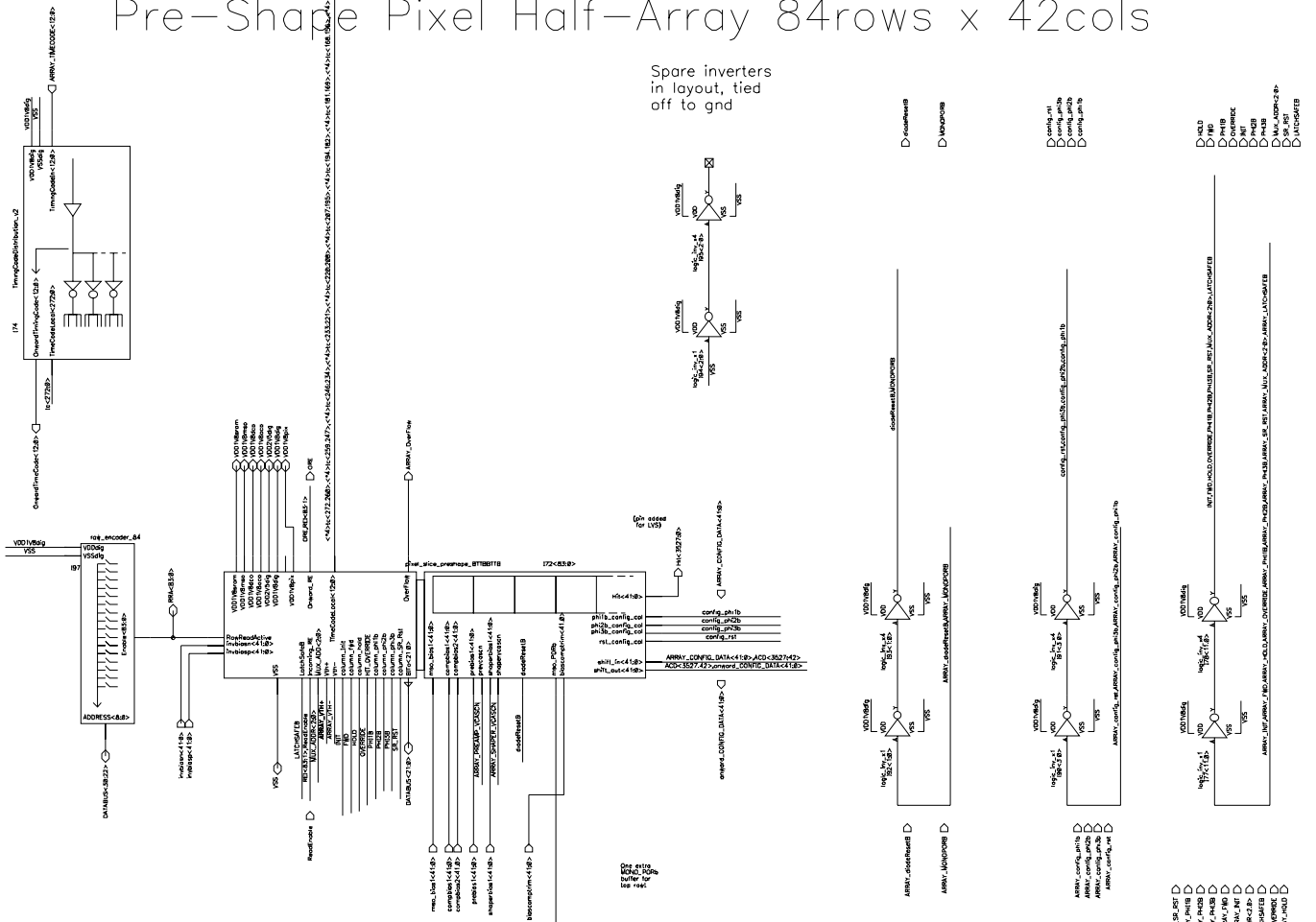
M501 3u

# COLUMN CIRCUITS

Project	RAL Microelectronics Group
Library Name	Tera-Pixel APS for CALICE
Block Name	ColCircPhets
Last OA Review	phabos_pr@ph_col
Last Changed	Mar 22 18:15:00 2007

# Pre-Shape Pixel Half-Array 84rows x 42cols

Spare inverters in layout, tied off to gnd



Un-Buffered Global Voltage signals: Static during operation

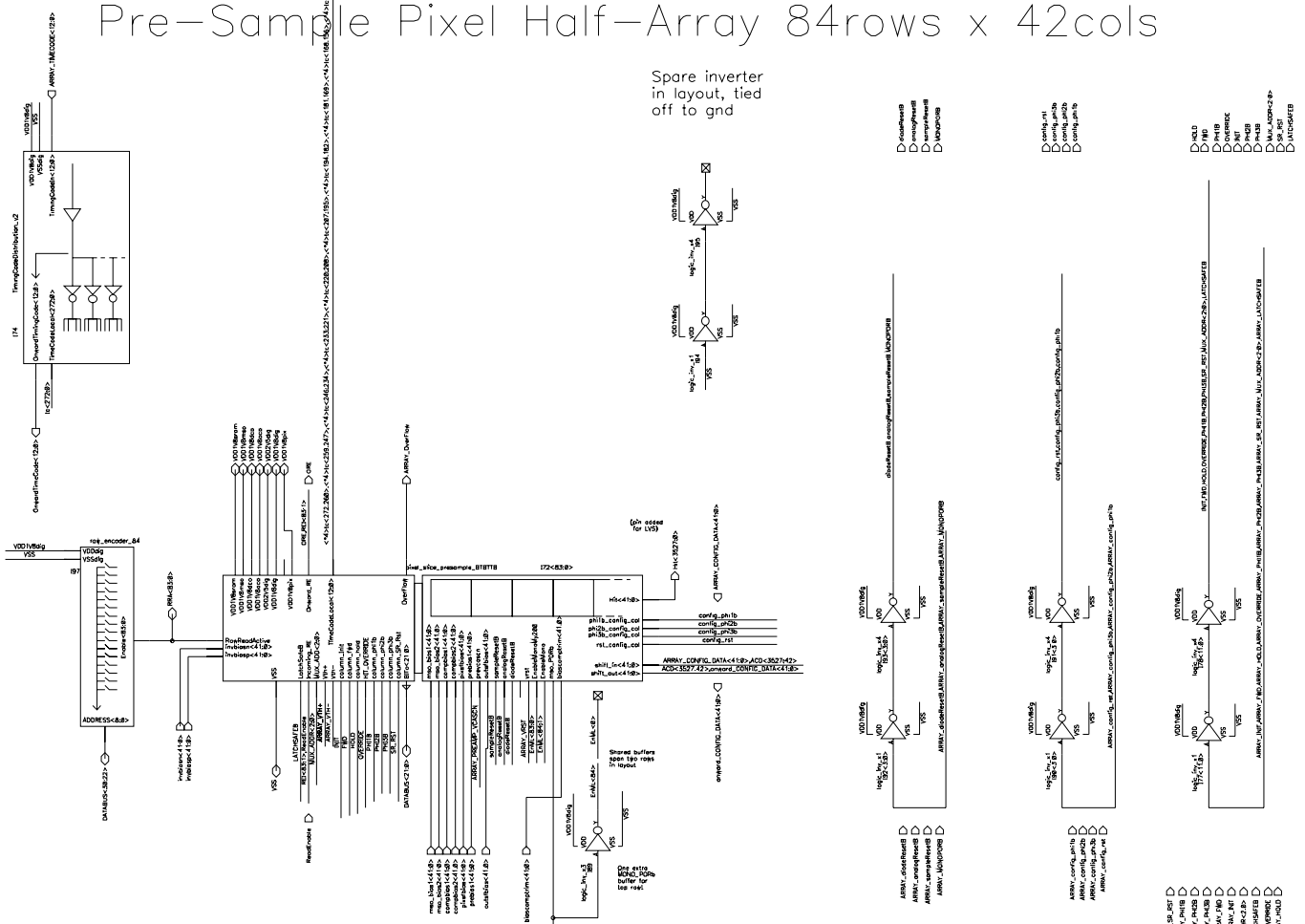
- ARRAY\_VTH1
- ARRAY\_VTH2
- ARRAY\_PREAMP\_VGAIN0
- ARRAY\_SHAPER\_VGAIN0

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array1_preshape_BT9BTTB
Lost QA Rev#	
Lost Changed	Apr 17 10:16:21 2007



# Pre-Sample Pixel Half-Array 84rows x 42cols

Spore inverter  
in layout, tied  
off to gnd



Un-Buffered Global  
Voltage signals: Static  
during operation

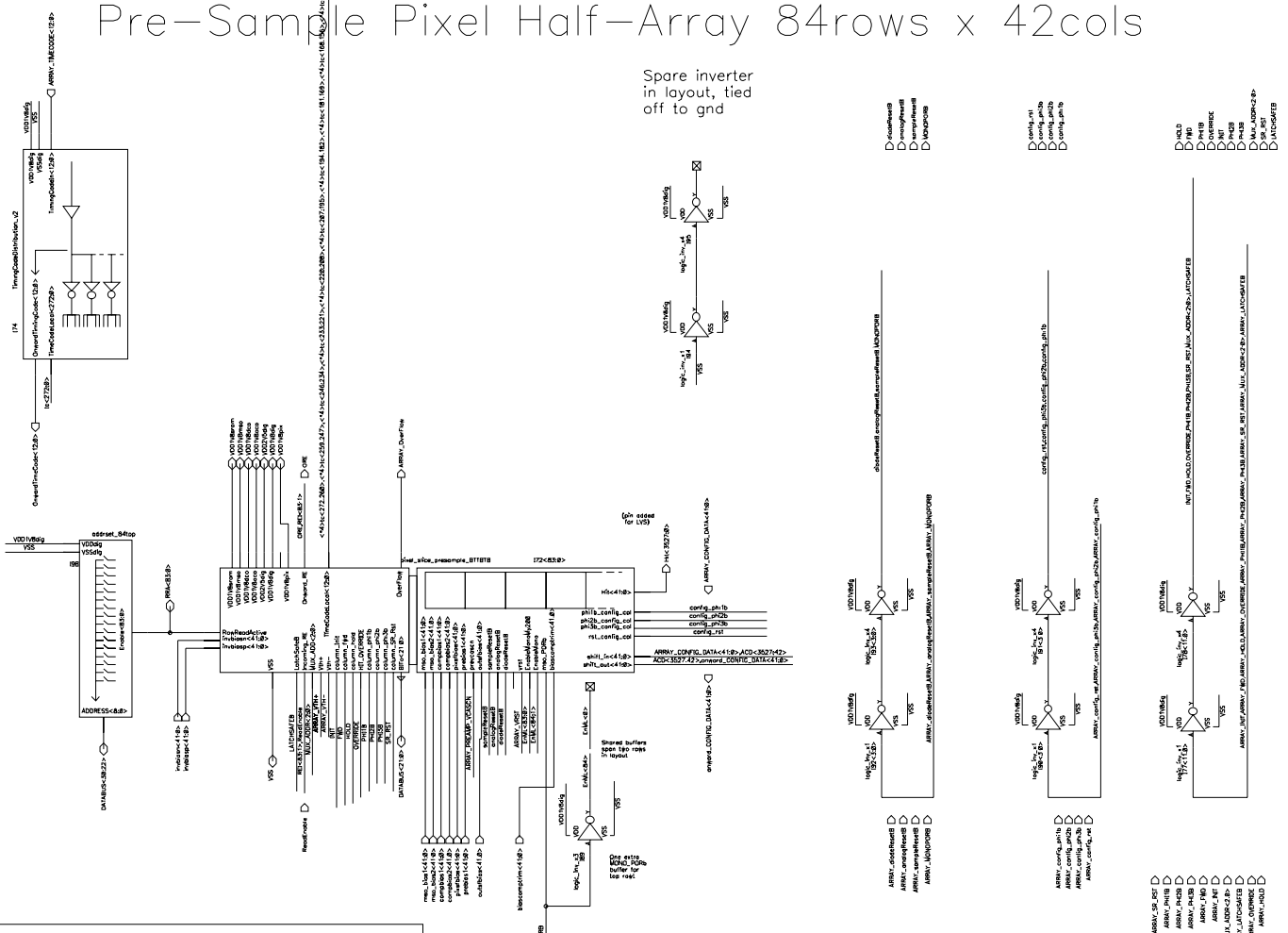
- ARRAY\_VTH1 ⊠
- ARRAY\_VTH2 ⊠
- ARRAY\_PREMIP\_CAS0N ⊠
- ARRAY\_VSG ⊠

- ⊠ node\_mip0n0
- ⊠ node\_mip0n1
- ⊠ node\_mip0n2
- ⊠ node\_mip0n3
- ⊠ node\_mip0n4
- ⊠ node\_mip0n5
- ⊠ node\_mip0n6
- ⊠ node\_mip0n7
- ⊠ node\_mip0n8
- ⊠ node\_mip0n9
- ⊠ node\_mip0n10
- ⊠ node\_mip0n11
- ⊠ node\_mip0n12
- ⊠ node\_mip0n13
- ⊠ node\_mip0n14
- ⊠ node\_mip0n15
- ⊠ node\_mip0n16
- ⊠ node\_mip0n17
- ⊠ node\_mip0n18
- ⊠ node\_mip0n19
- ⊠ node\_mip0n20
- ⊠ node\_mip0n21
- ⊠ node\_mip0n22
- ⊠ node\_mip0n23
- ⊠ node\_mip0n24
- ⊠ node\_mip0n25
- ⊠ node\_mip0n26
- ⊠ node\_mip0n27
- ⊠ node\_mip0n28
- ⊠ node\_mip0n29
- ⊠ node\_mip0n30
- ⊠ node\_mip0n31
- ⊠ node\_mip0n32
- ⊠ node\_mip0n33
- ⊠ node\_mip0n34
- ⊠ node\_mip0n35
- ⊠ node\_mip0n36
- ⊠ node\_mip0n37
- ⊠ node\_mip0n38
- ⊠ node\_mip0n39
- ⊠ node\_mip0n40
- ⊠ node\_mip0n41
- ⊠ node\_mip0n42
- ⊠ node\_mip0n43
- ⊠ node\_mip0n44
- ⊠ node\_mip0n45
- ⊠ node\_mip0n46
- ⊠ node\_mip0n47
- ⊠ node\_mip0n48
- ⊠ node\_mip0n49
- ⊠ node\_mip0n50
- ⊠ node\_mip0n51
- ⊠ node\_mip0n52
- ⊠ node\_mip0n53
- ⊠ node\_mip0n54
- ⊠ node\_mip0n55
- ⊠ node\_mip0n56
- ⊠ node\_mip0n57
- ⊠ node\_mip0n58
- ⊠ node\_mip0n59
- ⊠ node\_mip0n60
- ⊠ node\_mip0n61
- ⊠ node\_mip0n62
- ⊠ node\_mip0n63
- ⊠ node\_mip0n64
- ⊠ node\_mip0n65
- ⊠ node\_mip0n66
- ⊠ node\_mip0n67
- ⊠ node\_mip0n68
- ⊠ node\_mip0n69
- ⊠ node\_mip0n70
- ⊠ node\_mip0n71
- ⊠ node\_mip0n72
- ⊠ node\_mip0n73
- ⊠ node\_mip0n74
- ⊠ node\_mip0n75
- ⊠ node\_mip0n76
- ⊠ node\_mip0n77
- ⊠ node\_mip0n78
- ⊠ node\_mip0n79
- ⊠ node\_mip0n80
- ⊠ node\_mip0n81
- ⊠ node\_mip0n82
- ⊠ node\_mip0n83
- ⊠ node\_mip0n84
- ⊠ node\_mip0n85
- ⊠ node\_mip0n86
- ⊠ node\_mip0n87
- ⊠ node\_mip0n88
- ⊠ node\_mip0n89
- ⊠ node\_mip0n90
- ⊠ node\_mip0n91
- ⊠ node\_mip0n92
- ⊠ node\_mip0n93
- ⊠ node\_mip0n94
- ⊠ node\_mip0n95
- ⊠ node\_mip0n96
- ⊠ node\_mip0n97
- ⊠ node\_mip0n98
- ⊠ node\_mip0n99

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array3_presample_BTBTB
Lost QA Rev#	
Lost Changed	Apr 17 10:14:43 2007



# Pre-Sample Pixel Half-Array 84rows x 42cols

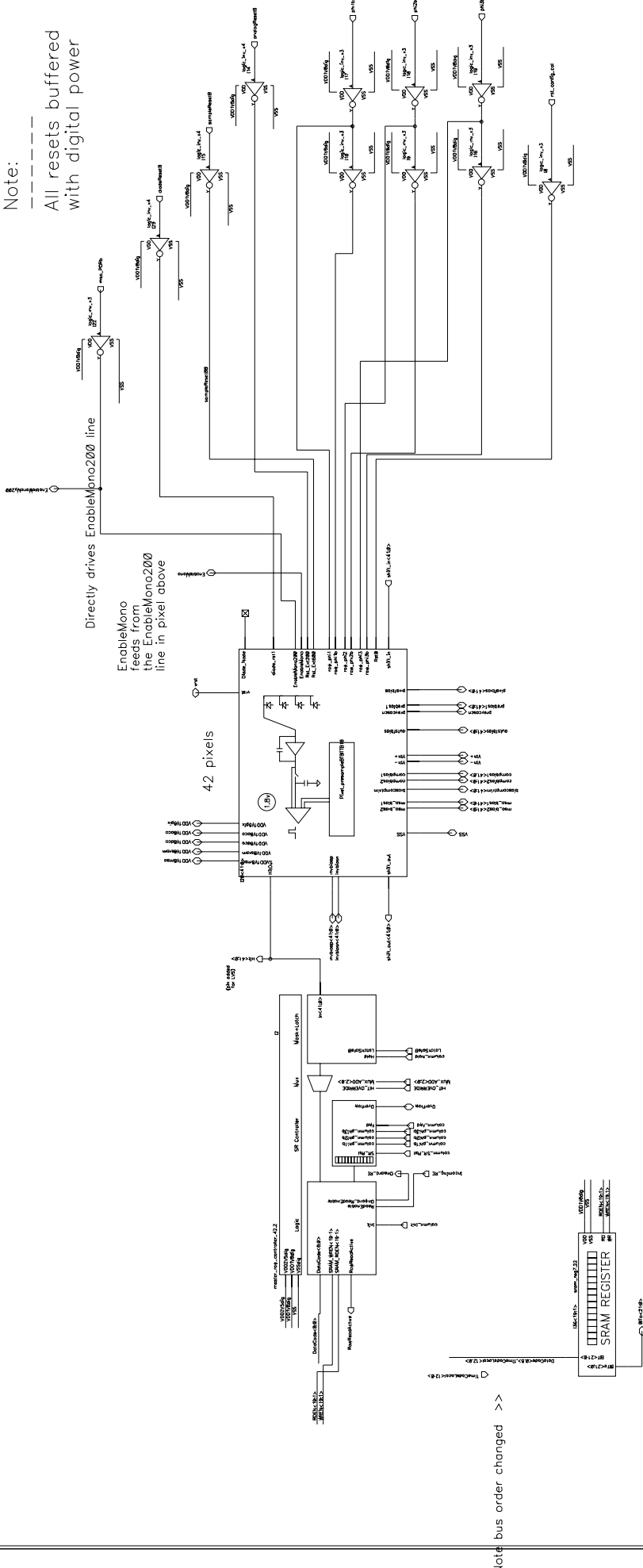


Un-Buffered Global Voltage signals: Static during operation

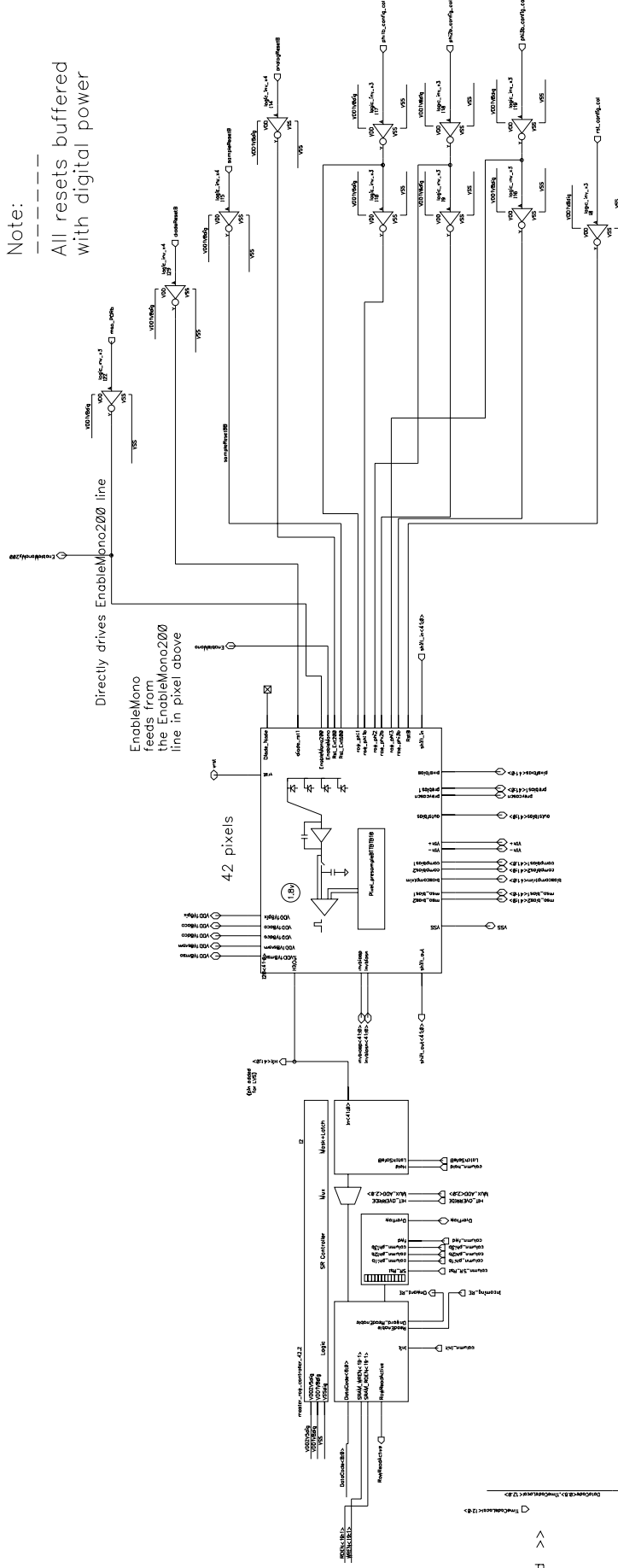
- ARRAY\_VTH1
- ARRAY\_VTH2
- ARRAY\_PREAMP\_CASIN
- ARRAY\_VDD1

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array4_presample_BT1B1B
Lost QA Rev#	
Lost Changed	Apr 17 13:19:19 2007

RAL Microelectronics Group		
Project	Inno-Phase AFS for DALI2E	
Library Name	c642c.c642c0b	
Block Name	panel_block_ferromagnetic_BFTFB	
Unit Cell Name	panel_block_ferromagnetic_BFTFB	
Unit Cell Version	Apr 17 09:24:37 2007	



Note bus order changed >>



Note: ---  
All resets buffered  
with digital power

EnableMono feeds from the EnableMono200 line in pixel above

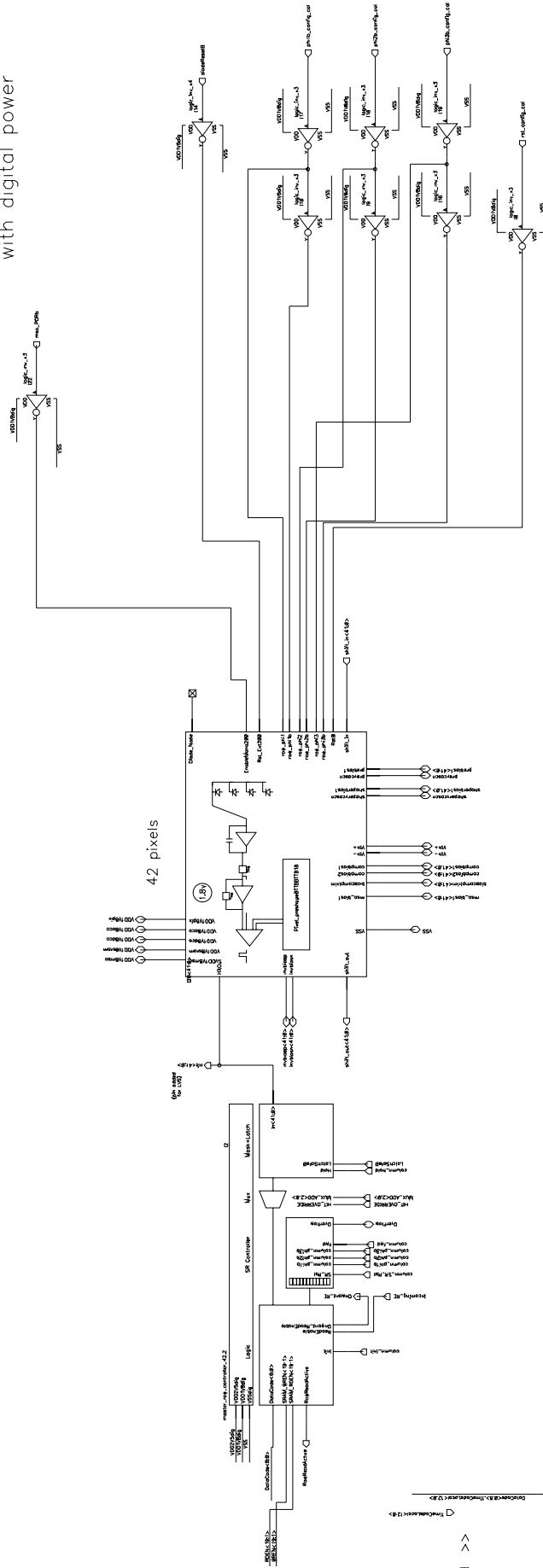
Directly drives EnableMono200 line

Note bus order changed >>

RAL Microelectronics Group	
Project	Imo-Pixel-AFS for DAU2E
Library Name	celic_circuits
Block Name	pixel_array_monochrome_BTBIB
Unit On Version	
Unit Changed	Apr 17 2025 24:28:07



Note:  
 --- All resets buffered  
 with digital power

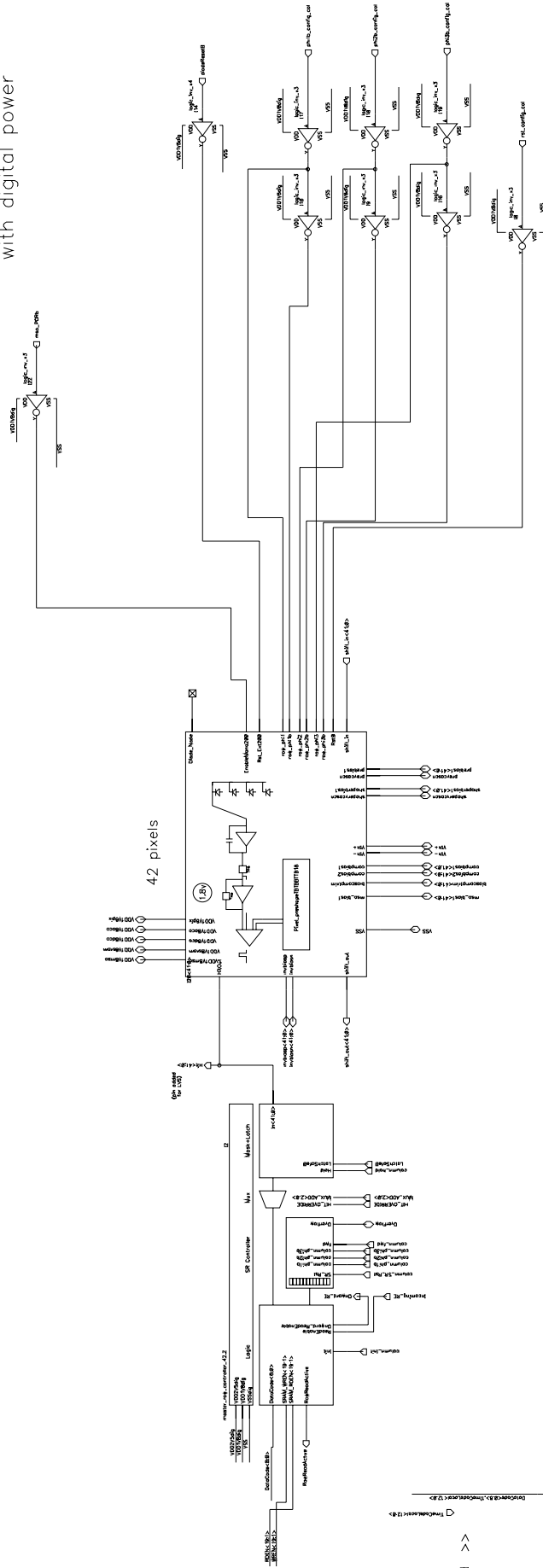


Note bus order changed >>

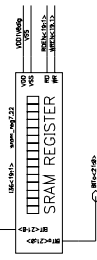
RAL Microelectronics Group	
Project	Imo-Pixel-APS for DAU2E
Library Name	cell2_circuits
Block Name	pixel_array_preproc_2T18M0T18
Unit On Version	
Unit Changed	Apr 17 2025 17:28:07



Note:  
 --- All resets buffered  
 with digital power



Note bus order changed >>



RAL Microelectronics Group	
Project	Imo-Pixel-APS for DAU2E
Library Name	cell2_circuits
Block Name	pixel_array_preproc_1818181818
Unit On Version	
Unit Changed	Apr 17 09:46:38 2007

Power supplies & Ground Mesh on M4(V) and M6 (H)

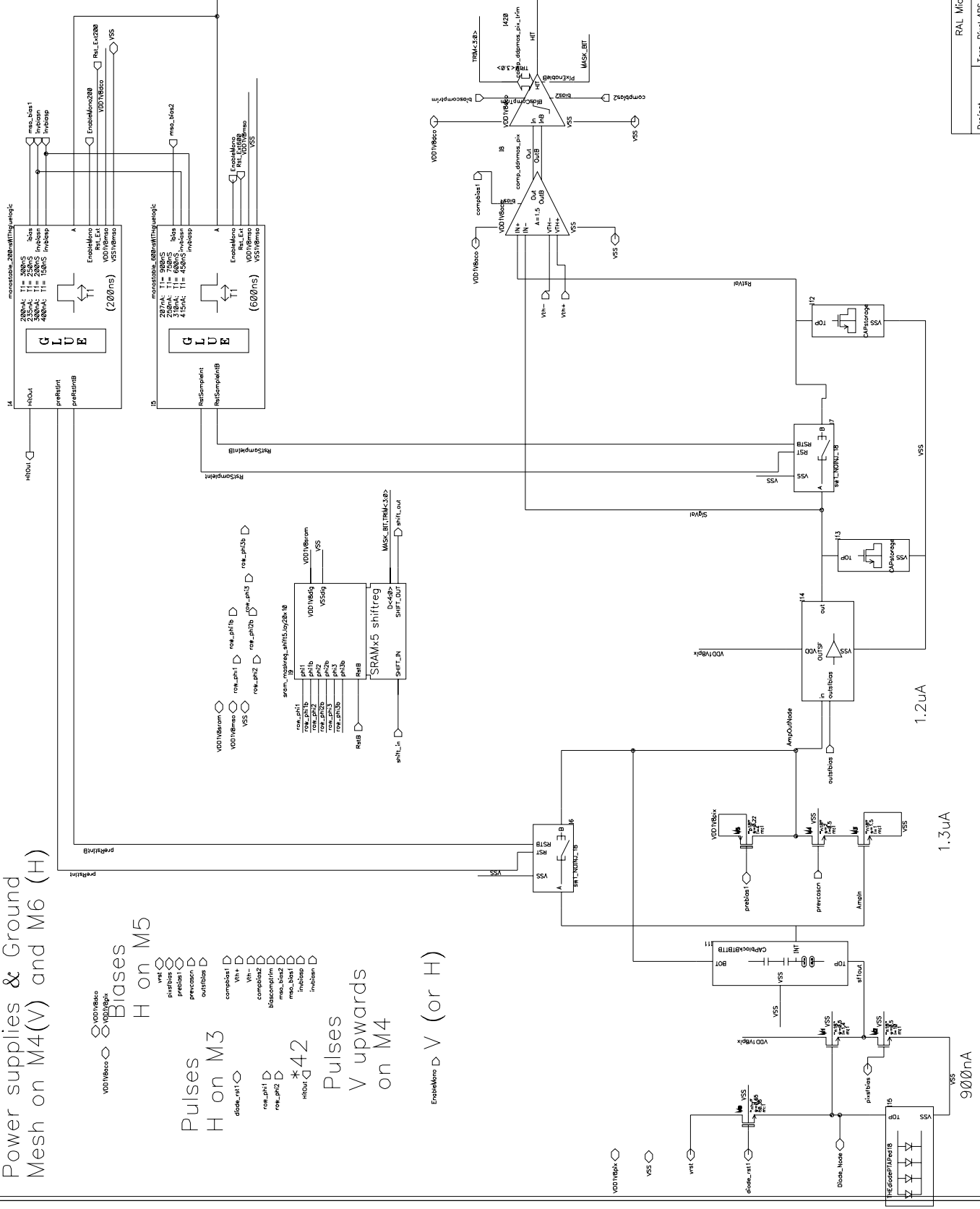
Biases  
H on M5

Pulses  
H on M3

\*42

Pulses  
V upwards  
on M4

EnableM6 V (or H)



Project	Tero-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_presampleBTBT1B
Last OA Review	
Last Changed	Apr. 16. 16:35:45 2007

RAL Microelectronics Group

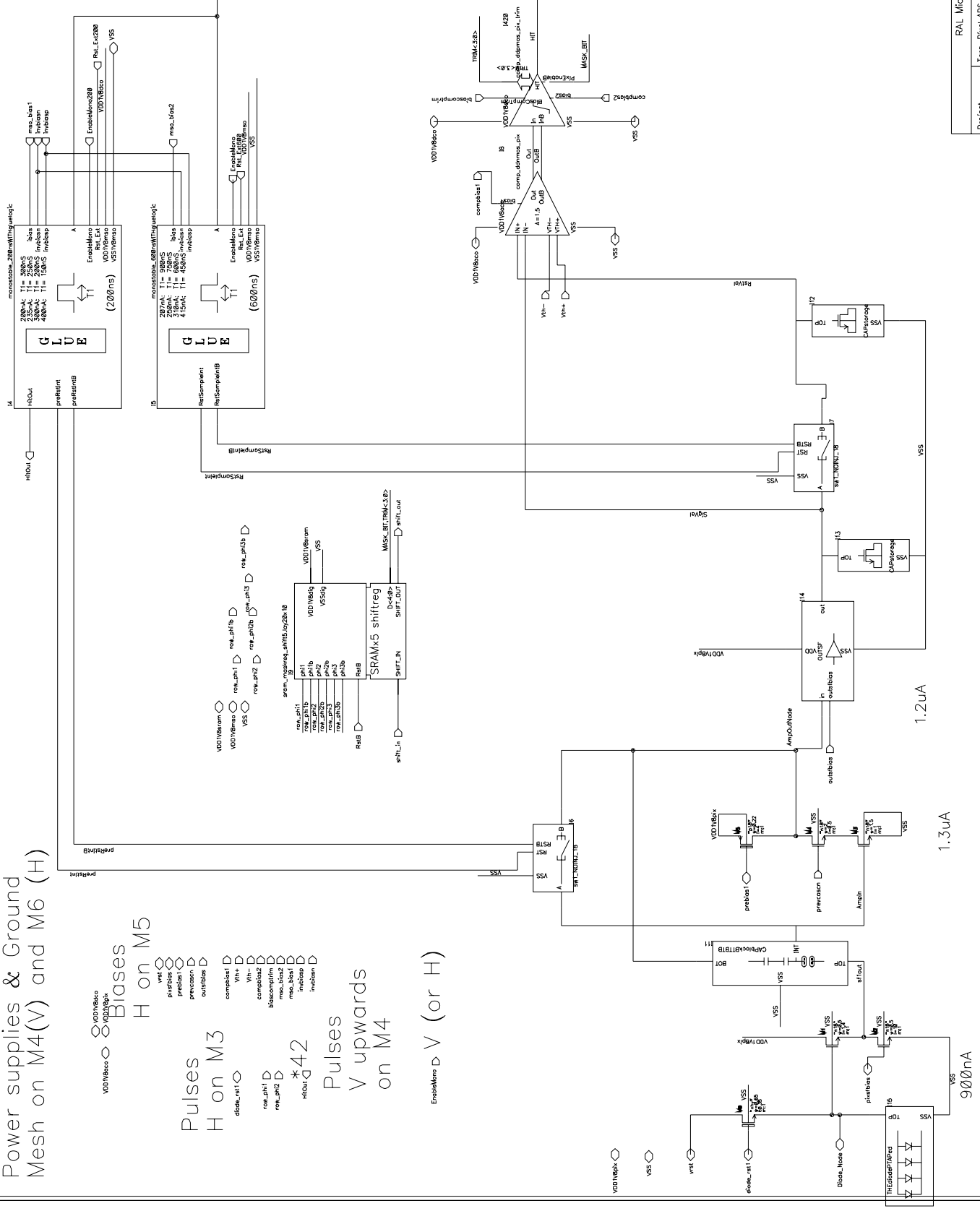
Power supplies & Ground Mesh on M4(V) and M6 (H)

Biases  
H on M5

Pulses  
H on M3

\*42  
Pulses  
V upwards  
on M4

EnableM6  
V (or H)



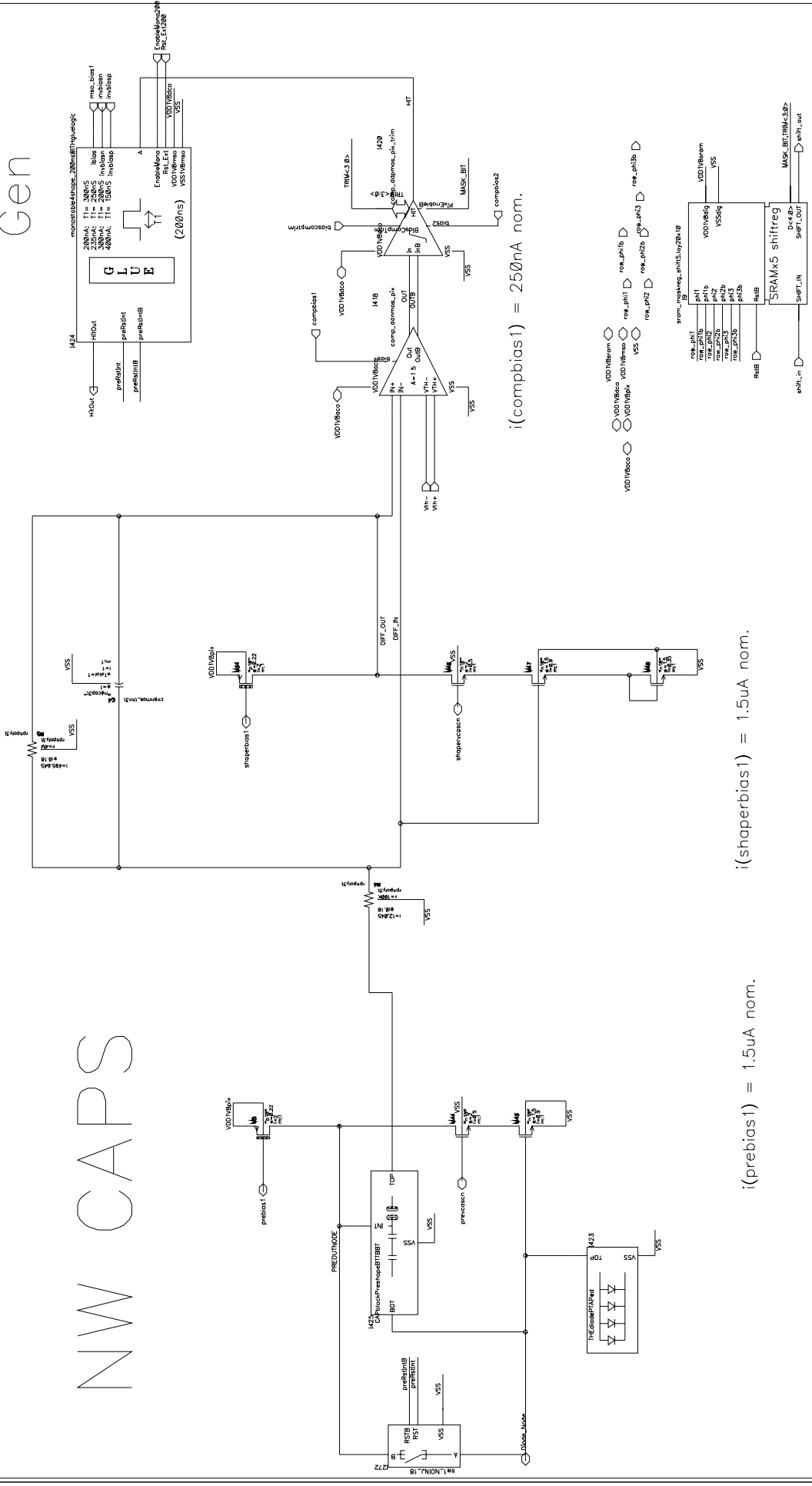
Project	Tero-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_presampleBTBTB1B
Last OA Review	
Last Changed	Mar-15 17:45:39 2007

RAL Microelectronics Group

Charge Preamp

NW CAPS

Shaper Comparators Pulse Gen



$i(\text{compbias1}) = 250\text{nA nom.}$

$i(\text{shaperbias1}) = 1.5\mu\text{A nom.}$

$i(\text{prebias1}) = 1.5\mu\text{A nom.}$

$\text{shapercascn} = 1.5\text{v}$

$\text{prebiascn} = 1.5\text{v}$

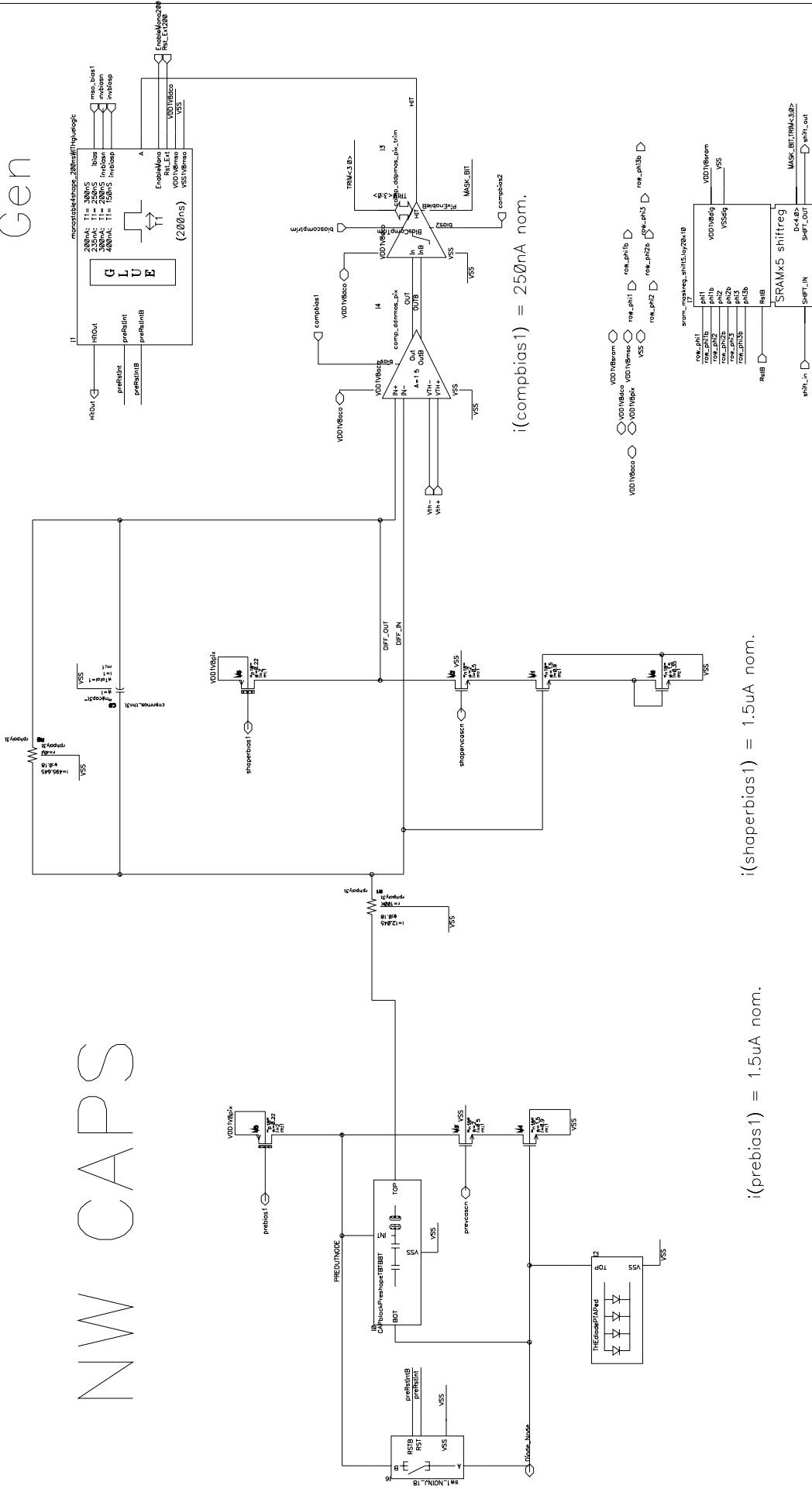
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_preshaperBITBTB1B
Last OA Review	
Last Changed	May 1 16:45:08 2007



Charge  
Preamp

Shaper  
Comparators  
Pulse  
Gen

NW CAPS



$i(\text{compbias1}) = 250\text{nA nom.}$



$i(\text{shaperbias1}) = 1.5\mu\text{A nom.}$

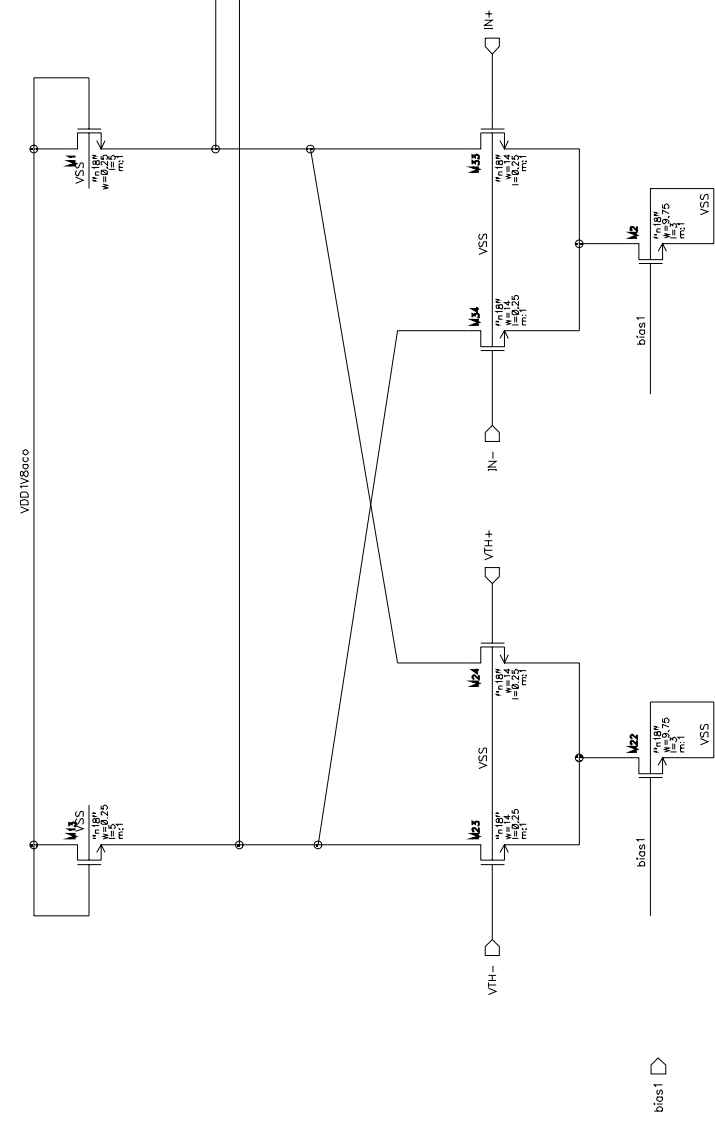
$i(\text{prebias1}) = 1.5\mu\text{A nom.}$

shapercasen = 1.5v

precasen = 1.5v

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pulse_preshapeTB1B1B1B
Lost OA Review	
Lost Changed	May 3 05:42:12 2007

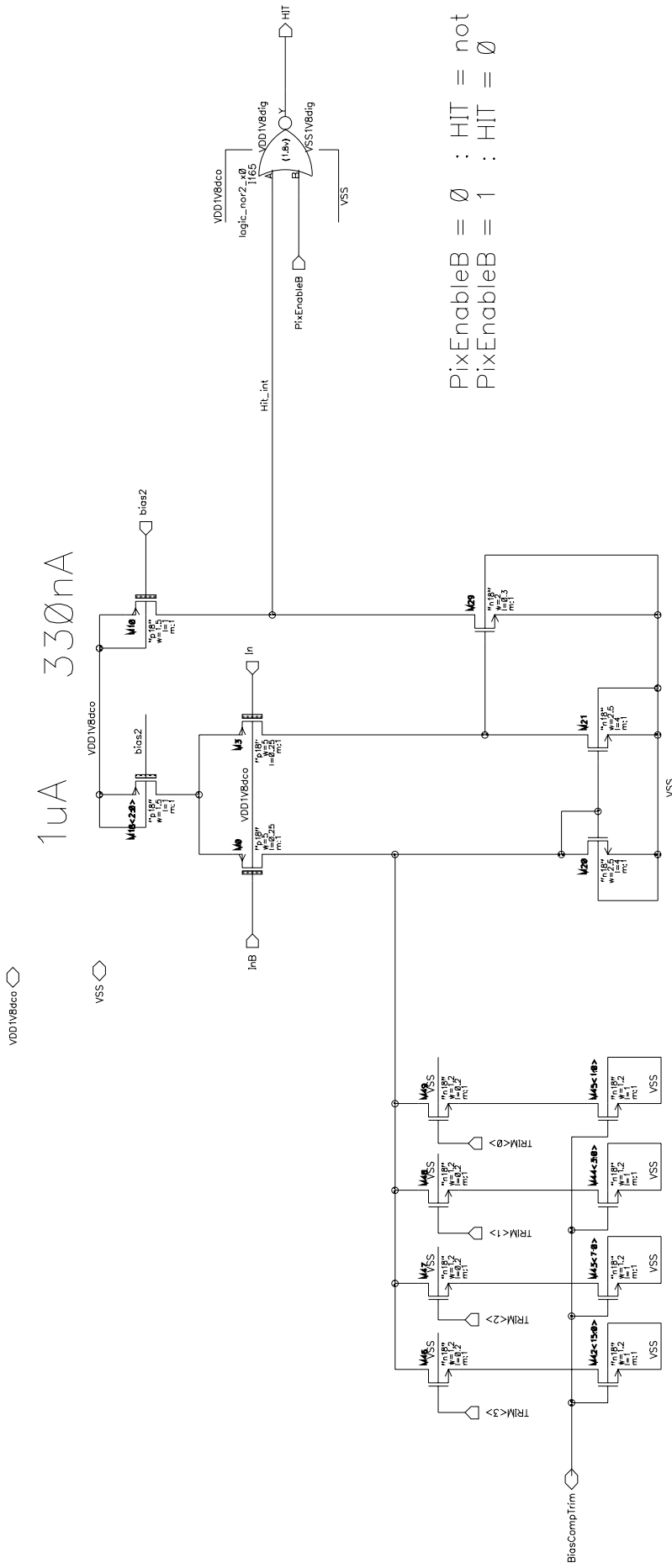
VSS   
 VDD1V8cc0 



differential (10s of mV)  
 hit signal wired across  
 to pmos comparator at row  
 logic

330nA 330nA

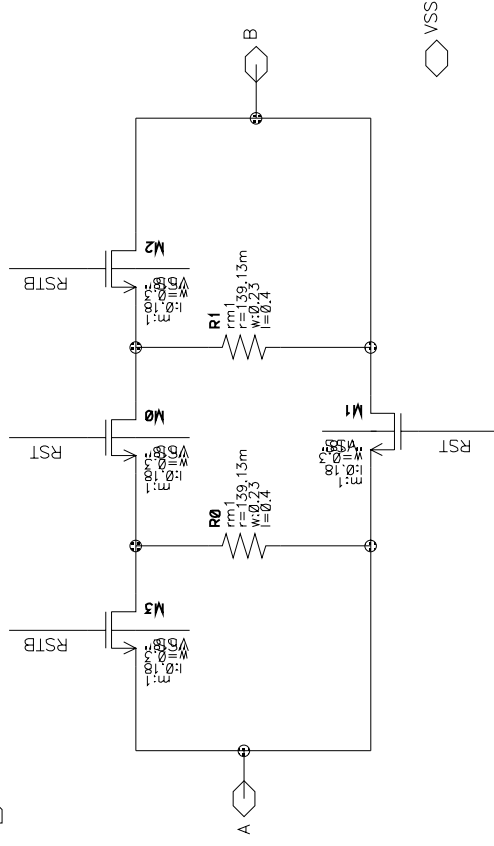
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	comp_ddnmos_pix
Last QA Review	
Last Changed	Feb 25 17:02:52 2007



PixEnableB = 0 : HIT = not Hit\_Int  
 PixEnableB = 1 : HIT = 0

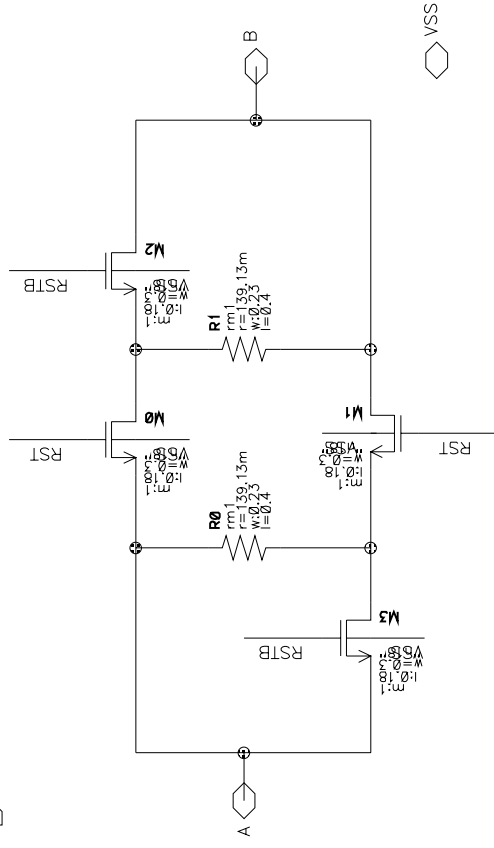
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	comp_ddpmos_pix_trim
Last QA Review	
Last Changed	Feb 17 16:53:26 2007

RST   
 RSTB 

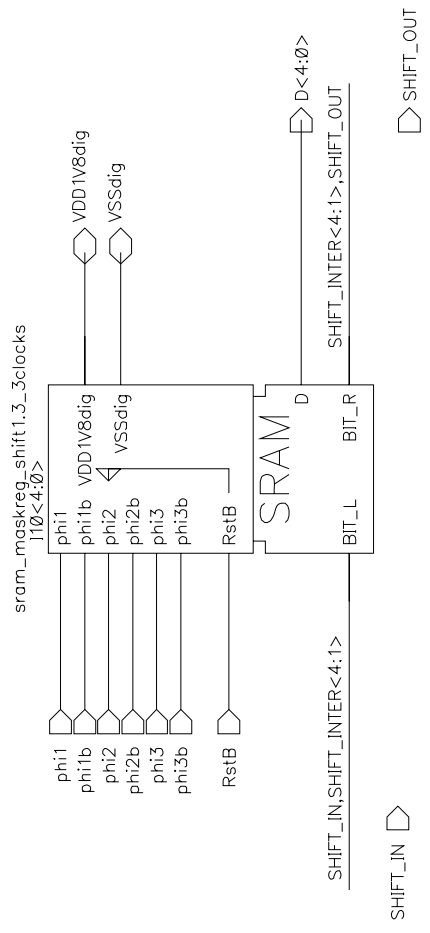


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sw1_NOINUJ_18
Last QA Review	
Last Changed	Feb 17 18:13:08 2007

RST   
 RSTB 



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sw1_NOINUJ_18sh
Last QA Review	
Last Changed	Mar 20 19:34:26 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sram_maskreg_shift5.lay20x10
Last QA Review	
Last Changed	Mar 8 17:41:45 2007

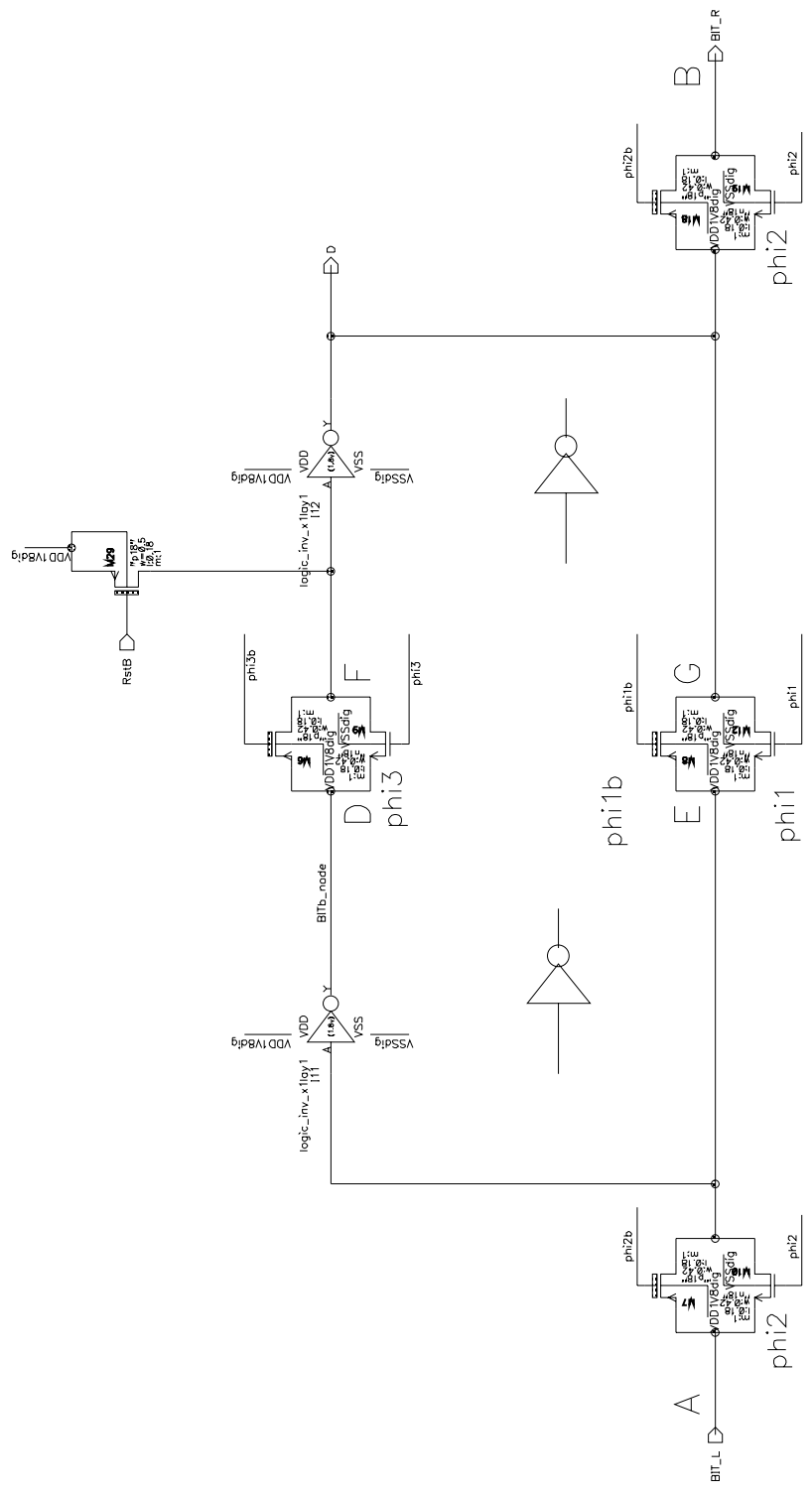
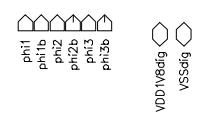
New Shiftreg Revision 1.3 3CLOCKSKS!

> Added third clock for slow edge immunity

Layout inspired changes:

Reset transistor modified wider shorter  
All TGs made width 0.42

Resim & Check [ ]



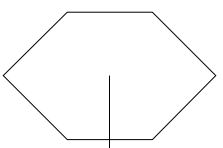
POWER UP  
phi1 off  
phi2 on  
RstB on (low)

IN-SERVICE RESET  
phi1 off  
phi2 on  
RstB pulsed on (low) during phi2

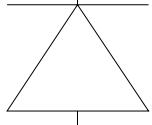
INVALID STATE  
phi1 X  
phi2 off (low)  
RstB on (low)

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sram_maskreg_shift1.3_3clocks
Last QA Review	
Last Changed	Jun 27 11:55:45 2007

TOP



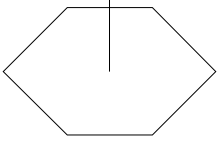
m:1  
area=11.73  
"dnwell"



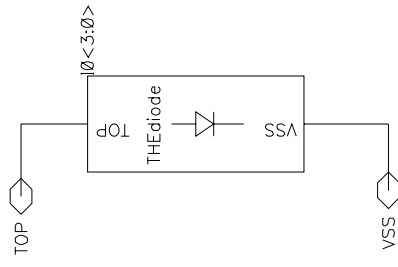
D1



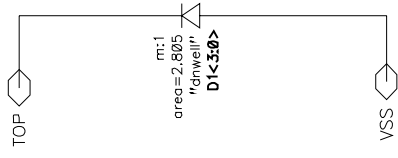
VSS



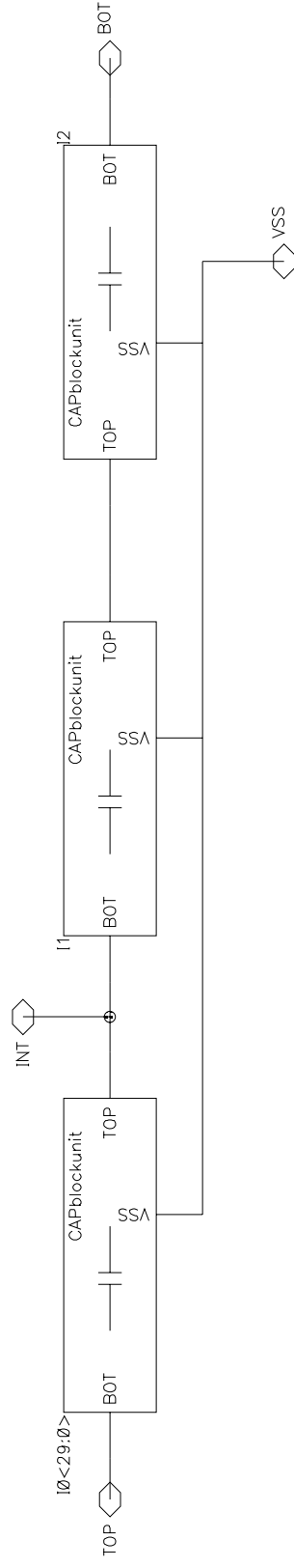




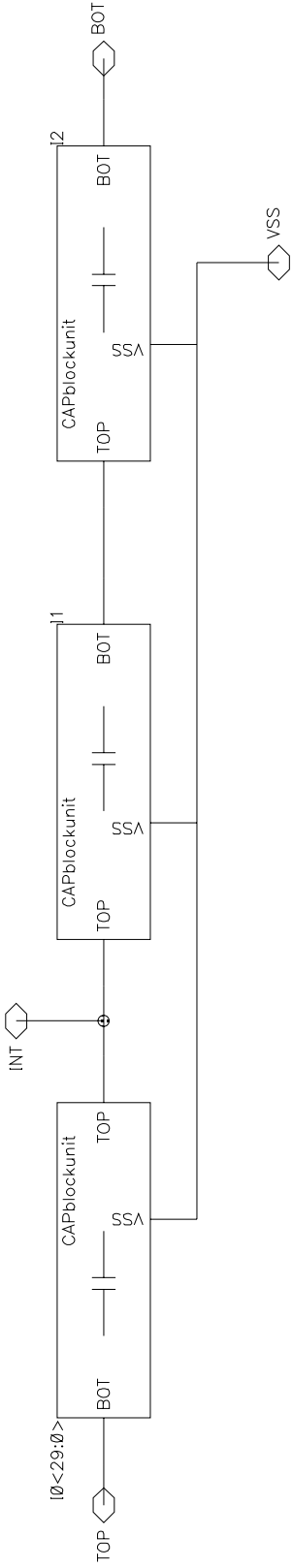
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	THEdiodePTAPed
Last QA Review	
Last Changed	Jun 27 11:57:01 2007



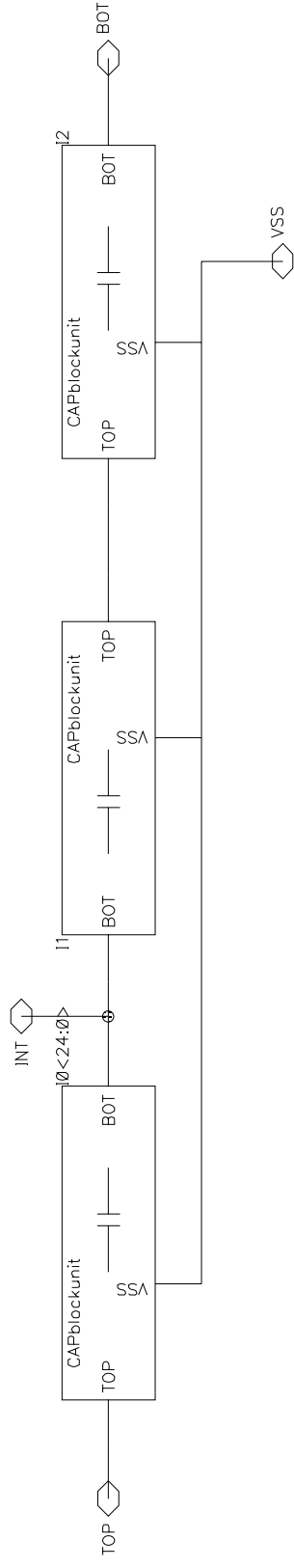
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	THEdiodePTAPed18
Last QA Review	
Last Changed	Jun 27 11:54:18 2007



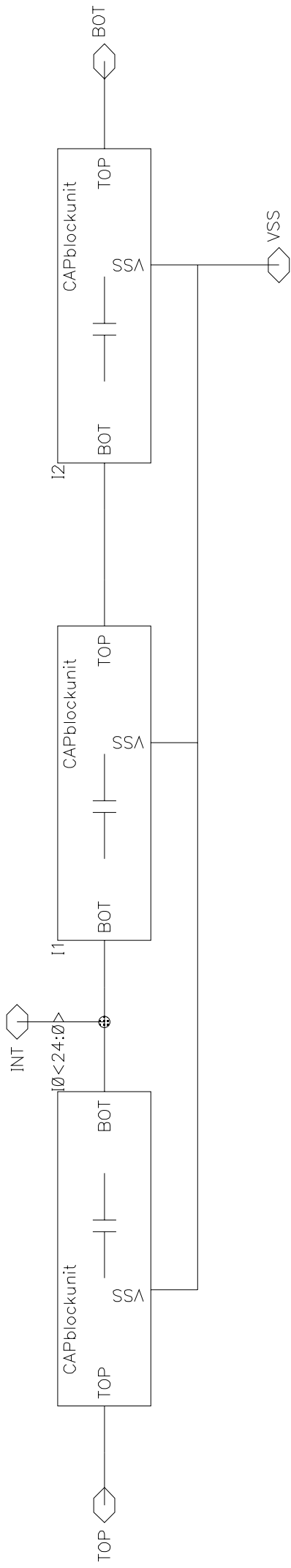
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockBTBTB
Last QA Review	
Last Changed	Jun 27 11:53:27 2007

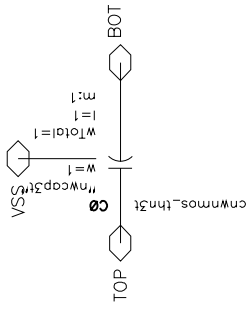


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockBTTTB
Last QA Review	
Last Changed	Jun 27 11:57:11 2007

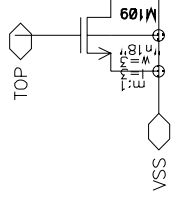


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockPreshapeBTBBT
Last QA Review	
Last Changed	Jun 27 11:58:37 2007



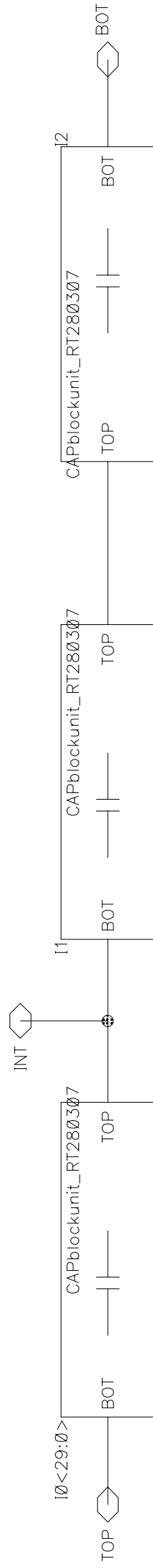


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockunit
Last QA Review	
Last Changed	Jun 27 11:53:47 2007

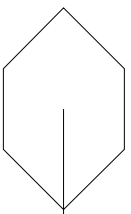


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPstorage
Last QA Review	
Last Changed	Jun 27 11:54:52 2007



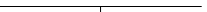
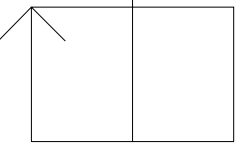


BOT

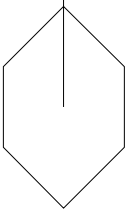


$w_{Total} = 1$   
 $w = 1$

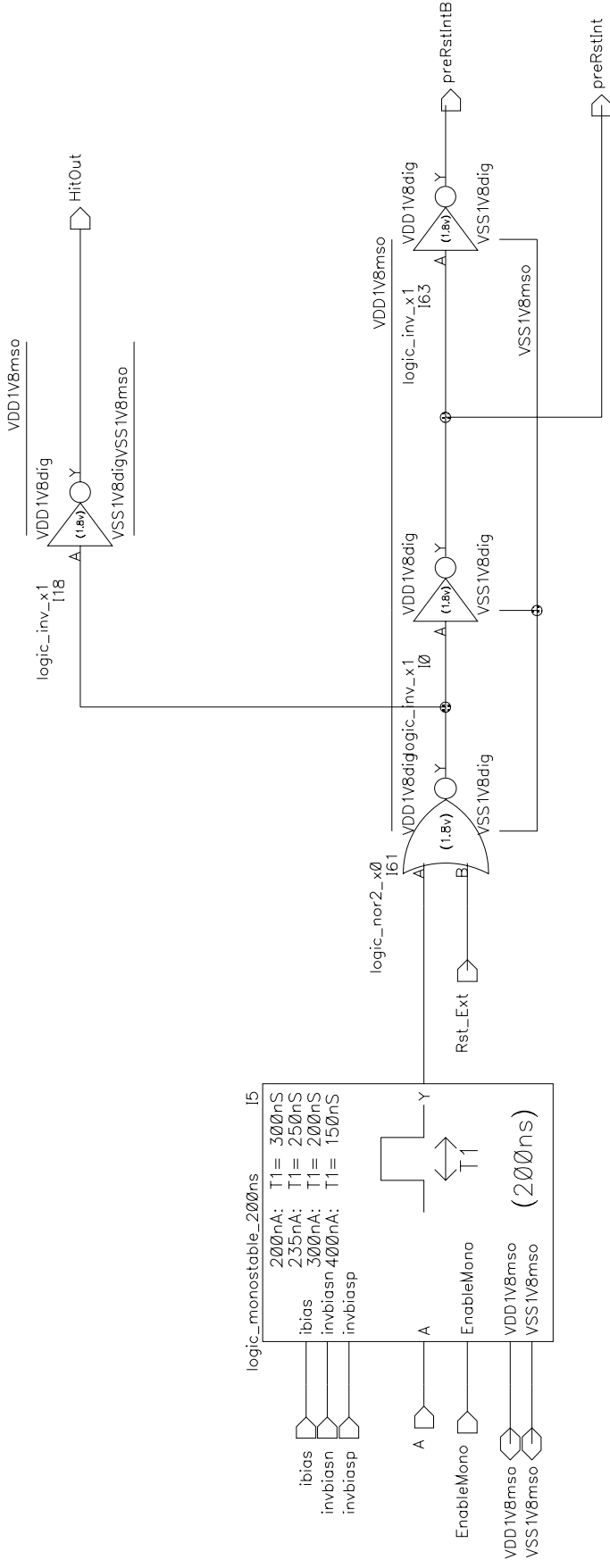
“nwcap2f”



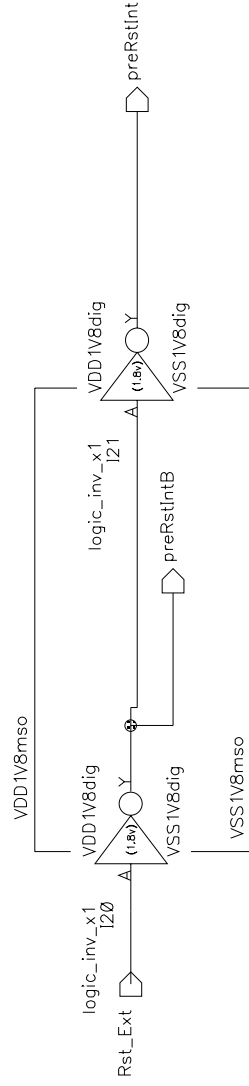
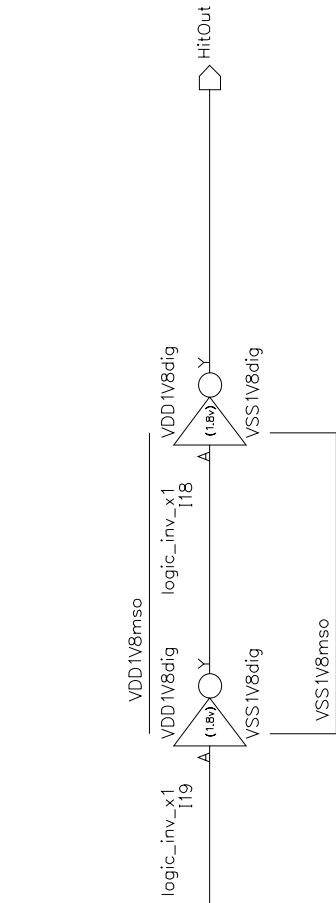
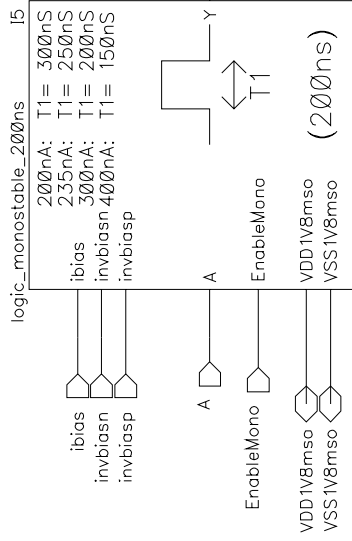
$\emptyset$



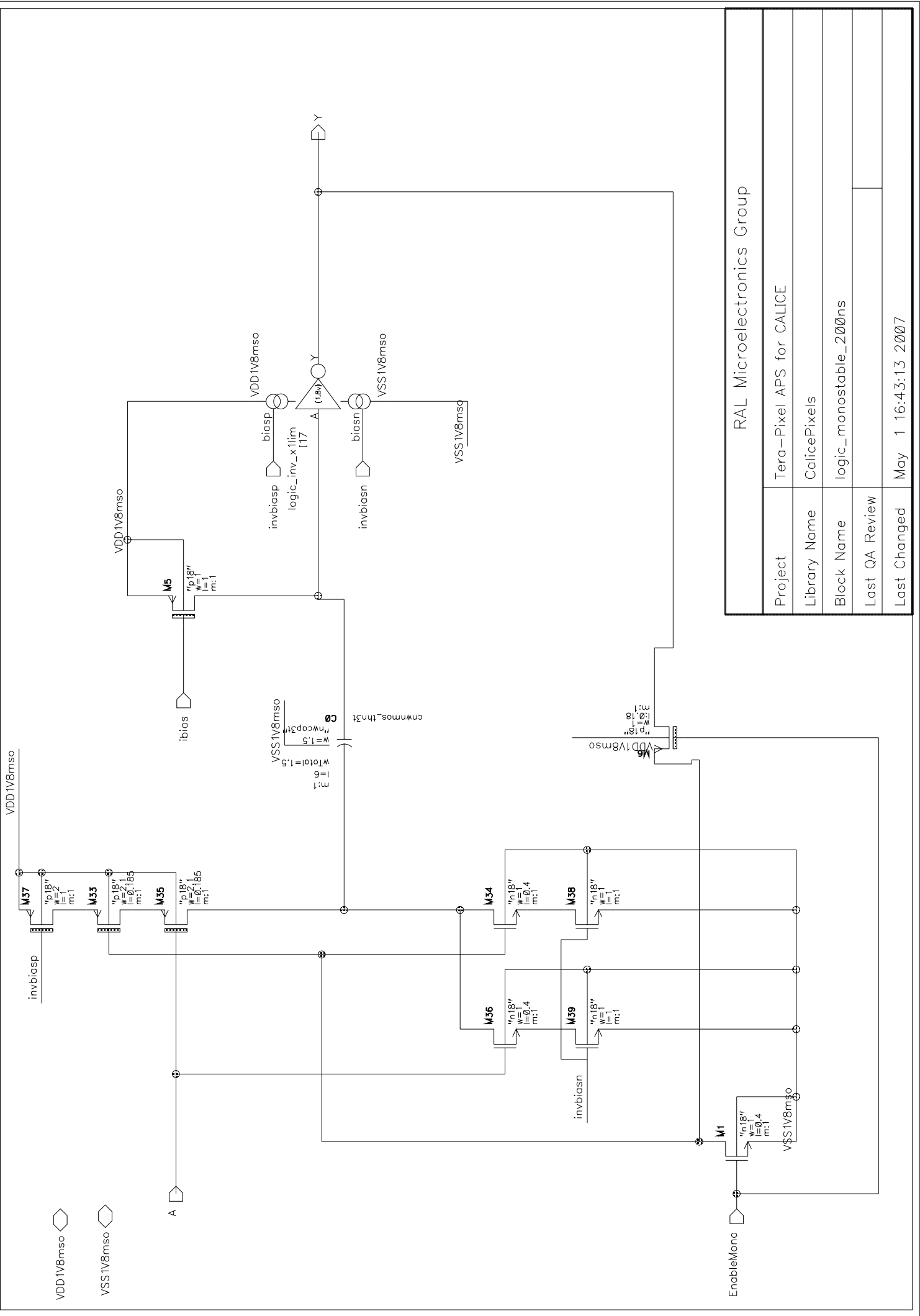
TOP

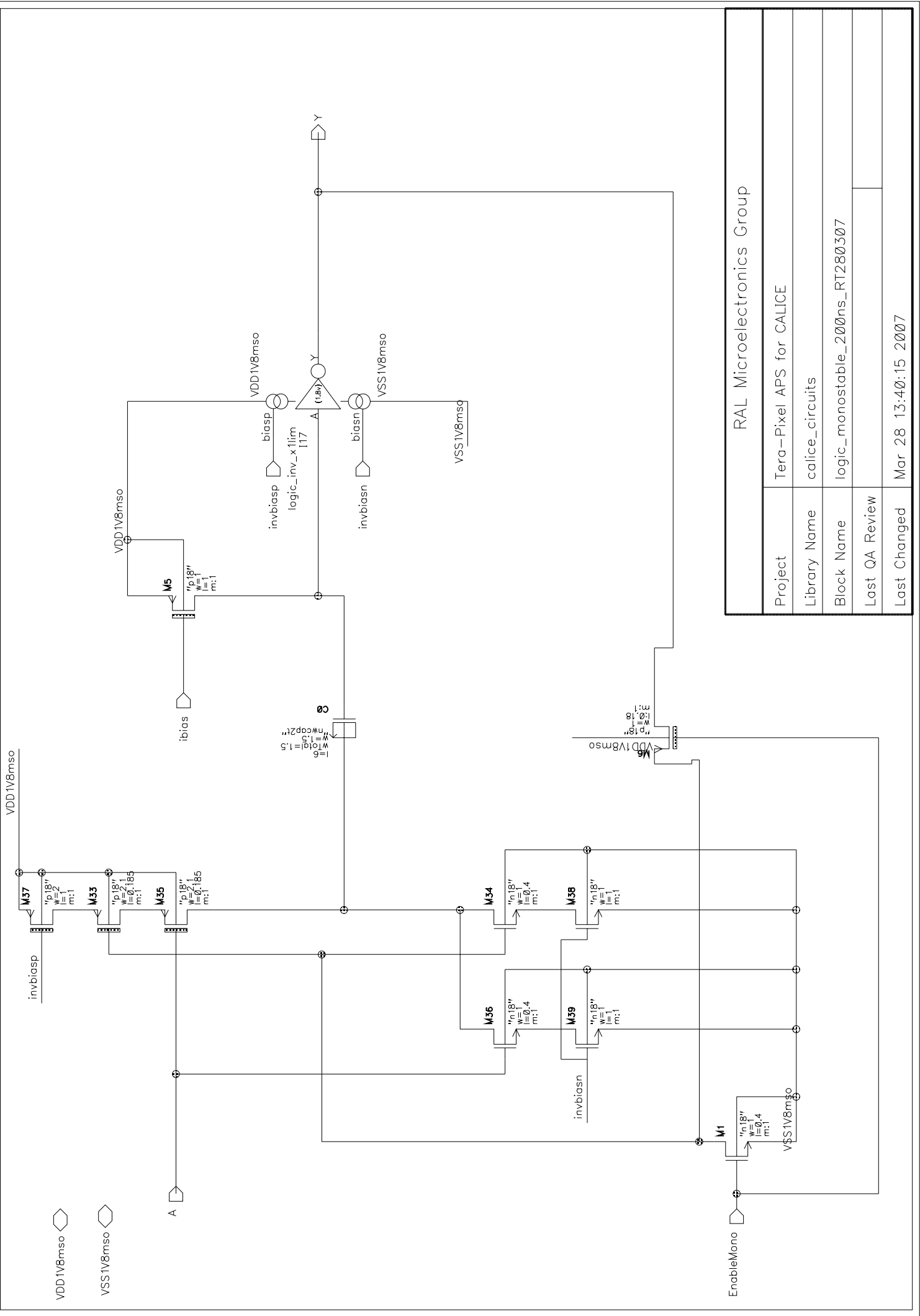


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable_200nsWITHgluelogic
Last QA Review	
Last Changed	Feb 13 11:47:56 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable4shape_200nsWITHgluelogic
Last QA Review	
Last Changed	May 1 16:43:18 2007



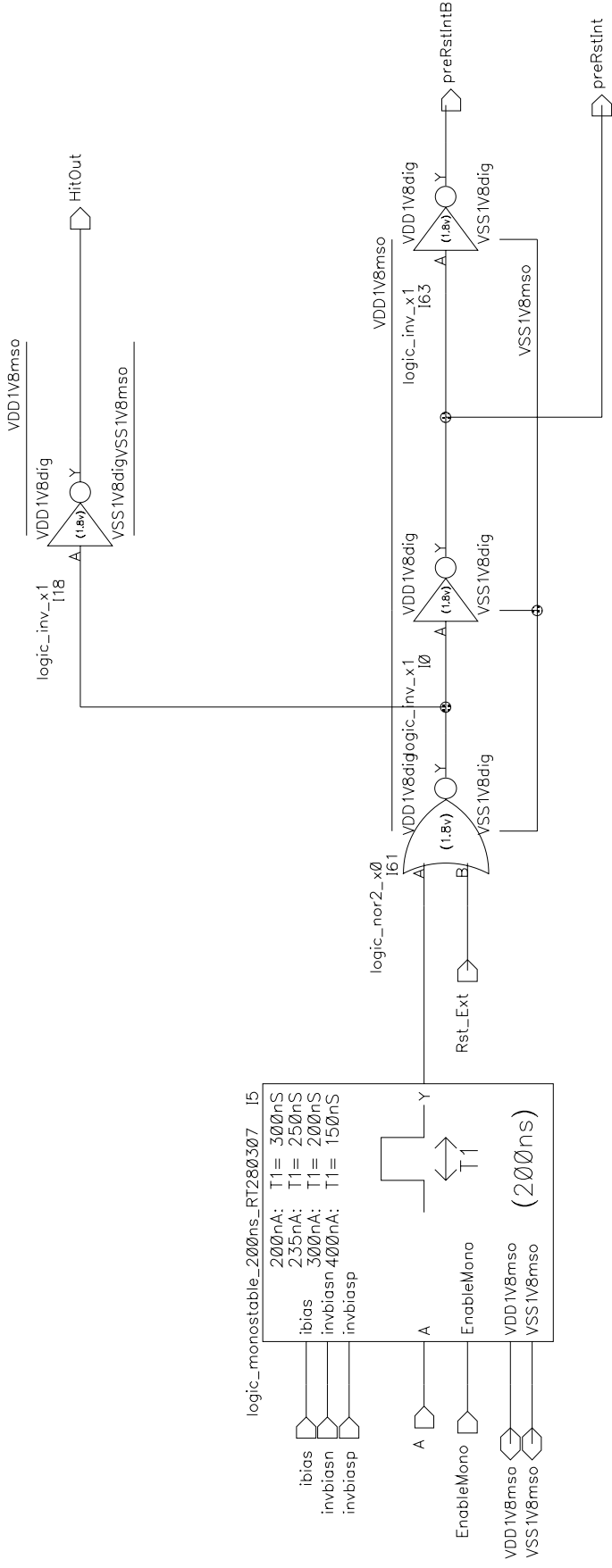


VDD1V8mso

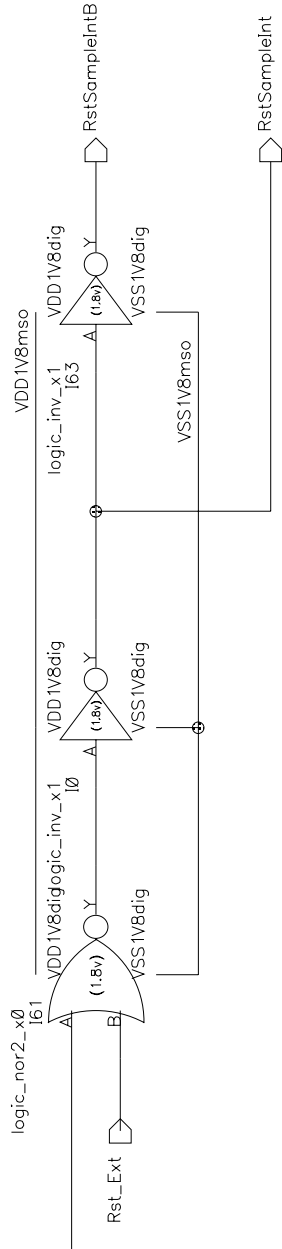
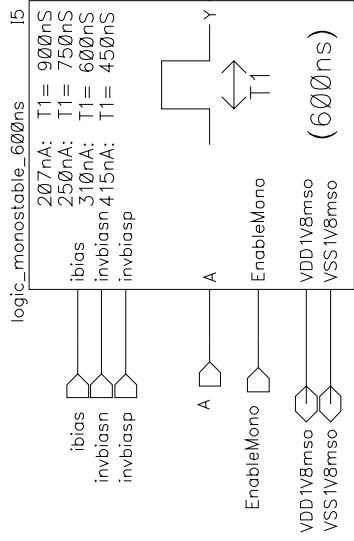
VSS1V8mso

EnableMono

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_monostable_200ns_RT280307
Last QA Review	
Last Changed	Mar 28 13:40:15 2007

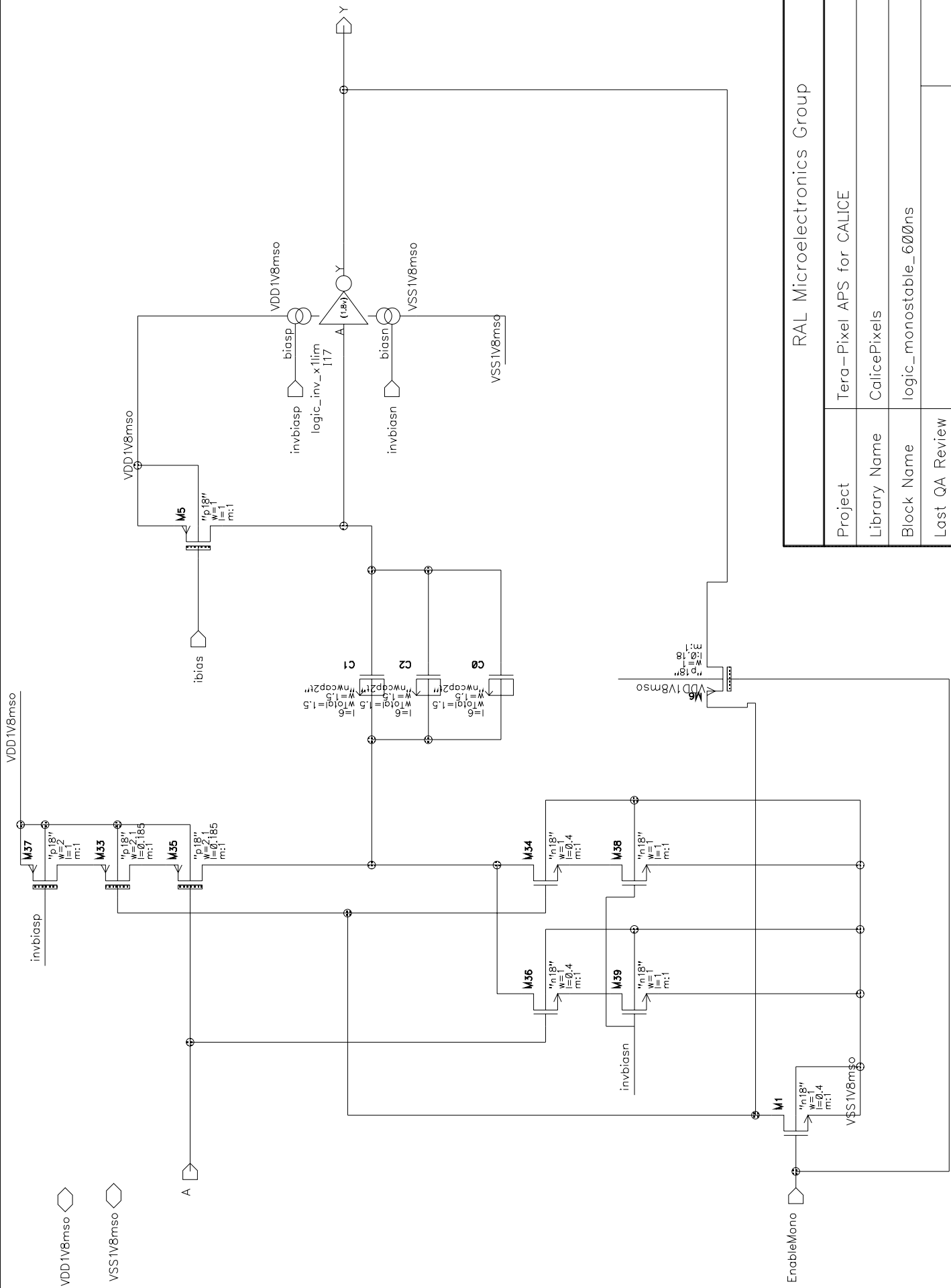


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	monostable_200nsWITHgluelogic_RT280307
Last QA Review	
Last Changed	Mar 28 13:40:20 2007

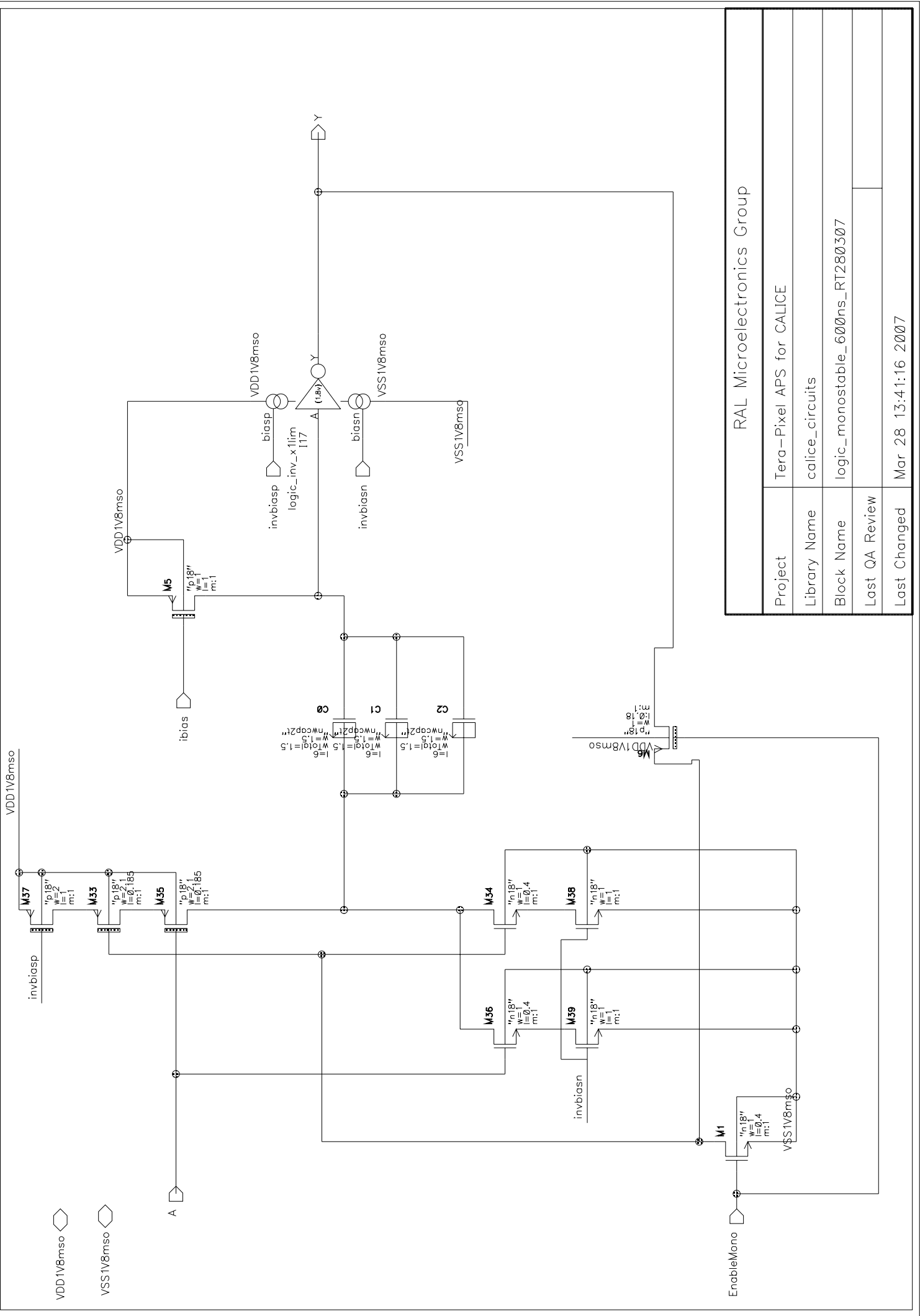


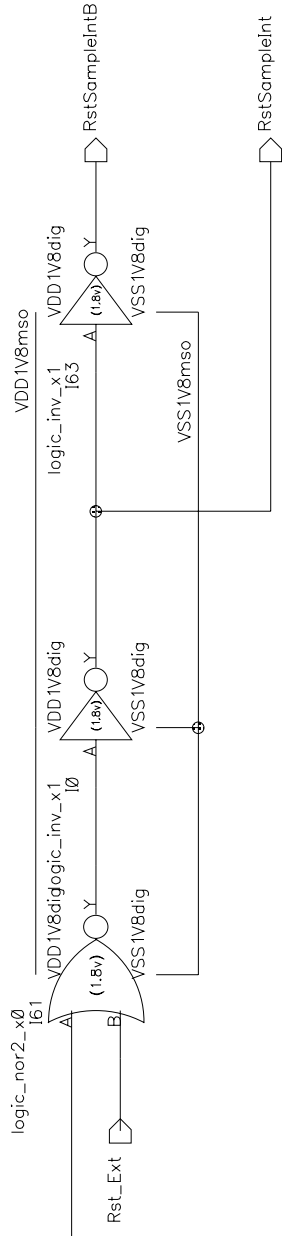
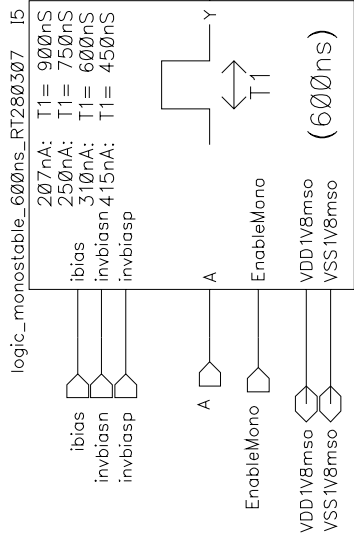
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable_600nsWITHgluelogic
Last QA Review	
Last Changed	Mar 15 16:42:09 2007





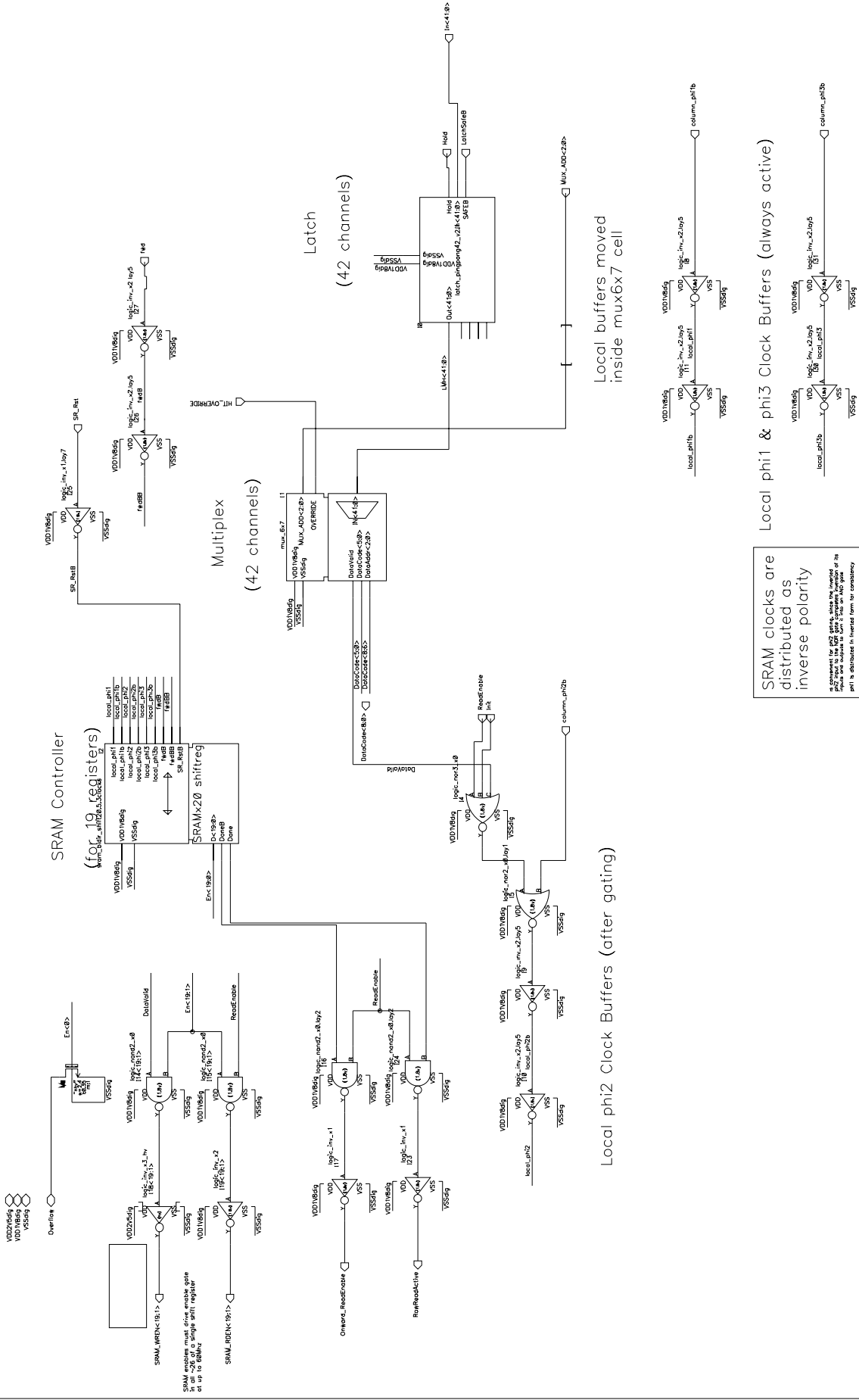
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_monostable_600ns
Last QA Review	
Last Changed	Apr 16 16:39:18 2007



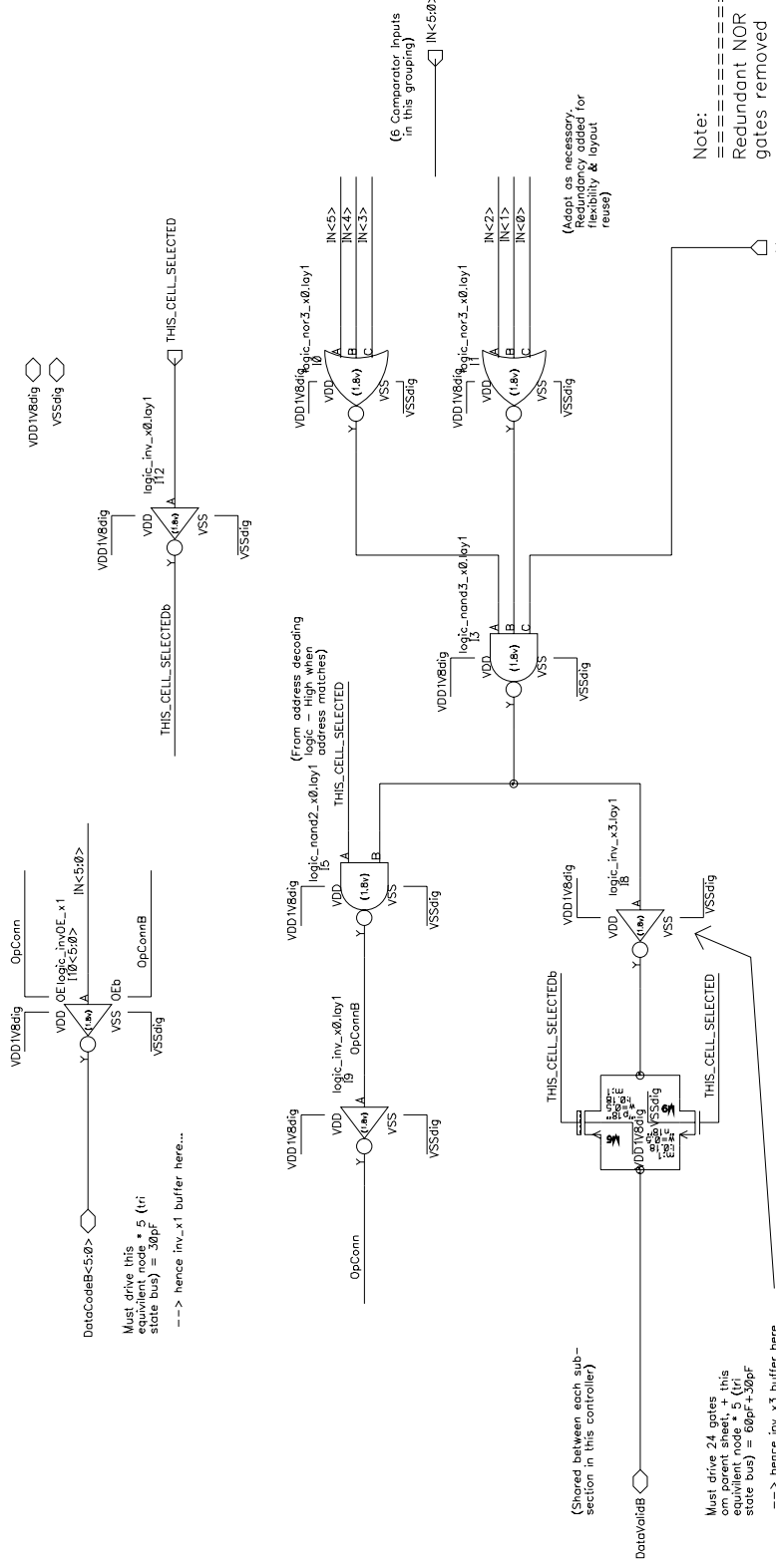


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	monostable_600nsWITHgluelogic_RT280307
Last QA Review	
Last Changed	Mar 28 13:41:19 2007

# 42-CHANNEL 3-CLOCKS VERSION



RAL Microelectronics Group	
Project	Tera-Phi1 APS for CALICE
Library Name	calice_circuits
Block Name	master_row_controller_42.2
Last OA Review	
Last Changed	Apr 19 11:33:28 2007

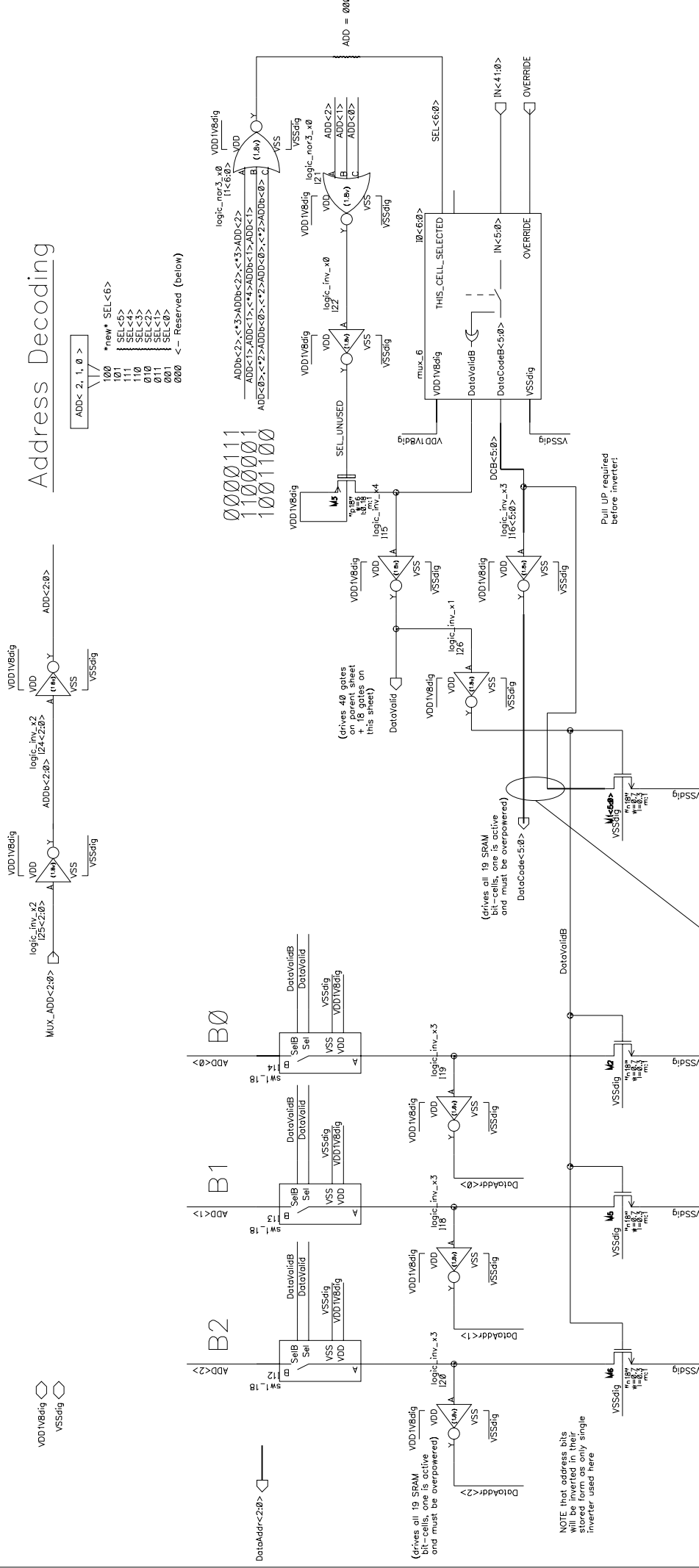


Note:  
 =====  
 Redundant NOR  
 gates removed

Override now  
 wired directly  
 into NAND so  
 polarity is  
 opposite:

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6
Last QA Review	
Last Changed	Jan 11 15:41:42 2007

# Address Decoding



ERROR CORRECTED:

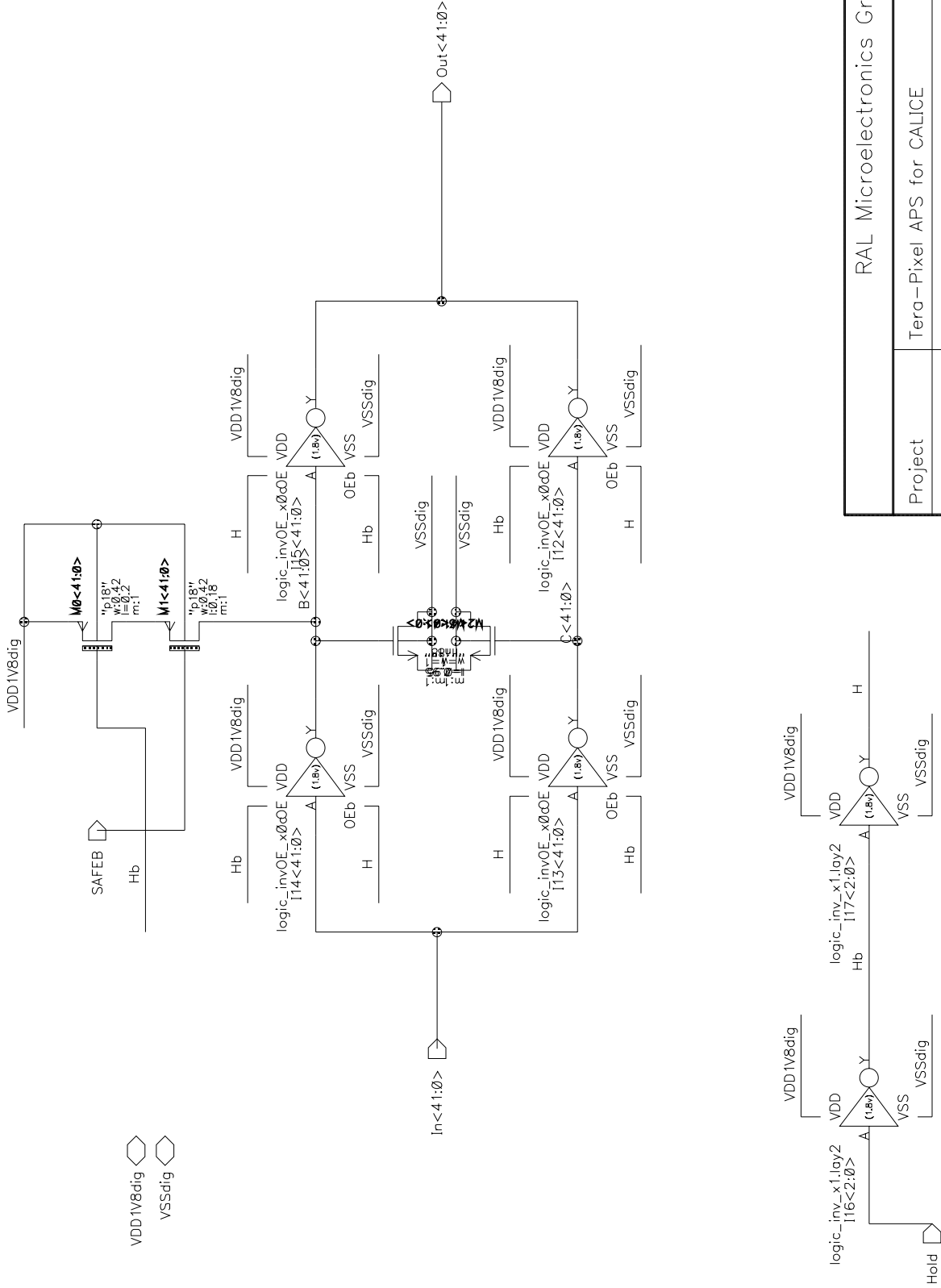
Note new buffer for local DataValid

DataCode should be pulled down BEFORE the inverter not after

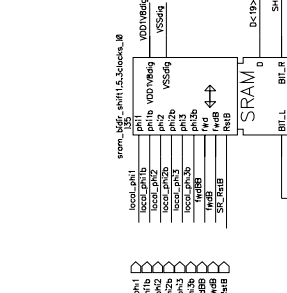
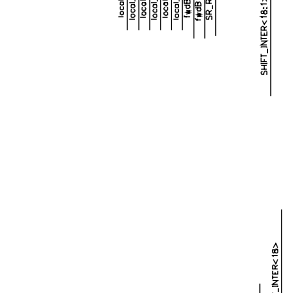
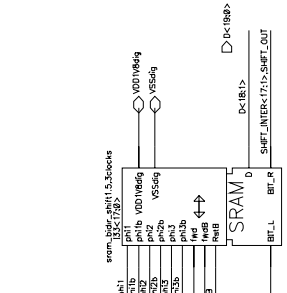
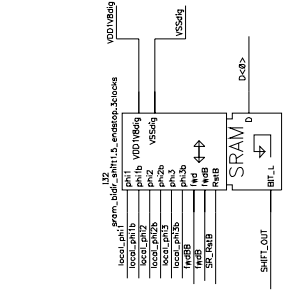
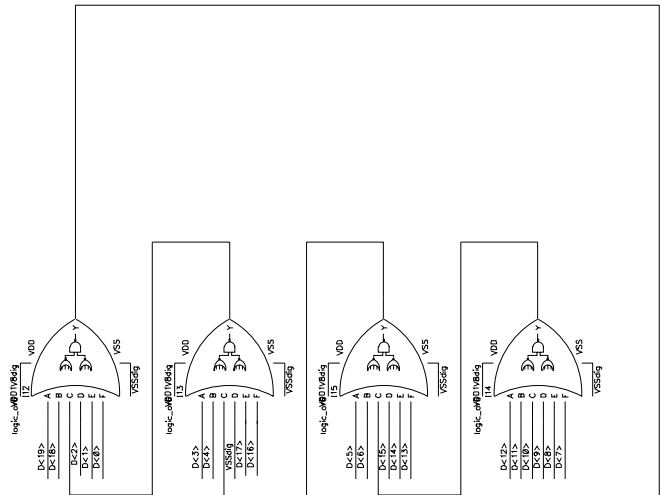
ReSim to confirm.

RAL Microelectronics Group

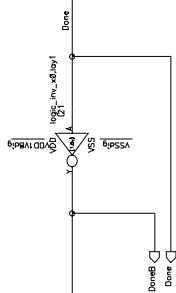
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6x7
Last QA Review	
Last Changed	Feb 16 10:35:10 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	latch_pingpong42_v2.1
Last QA Review	
Last Changed	Mar 27 19:20:29 2007



NB: Shift reg resets to 100000000000000000000000

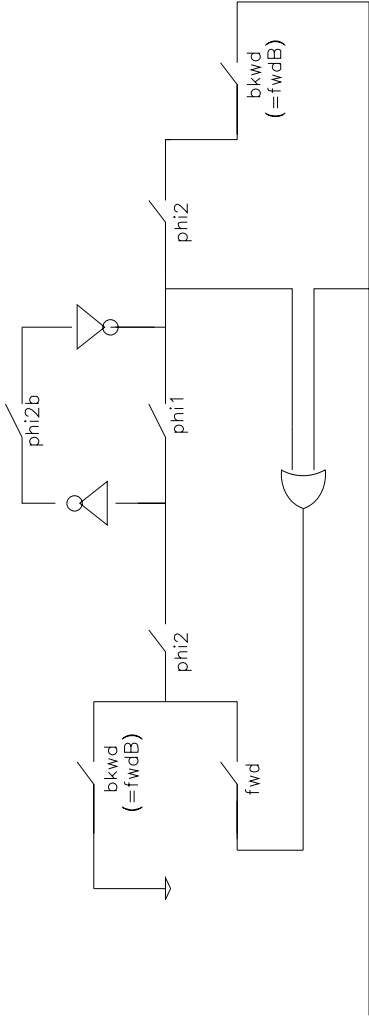


TG removed since special I0 part in SR is now used

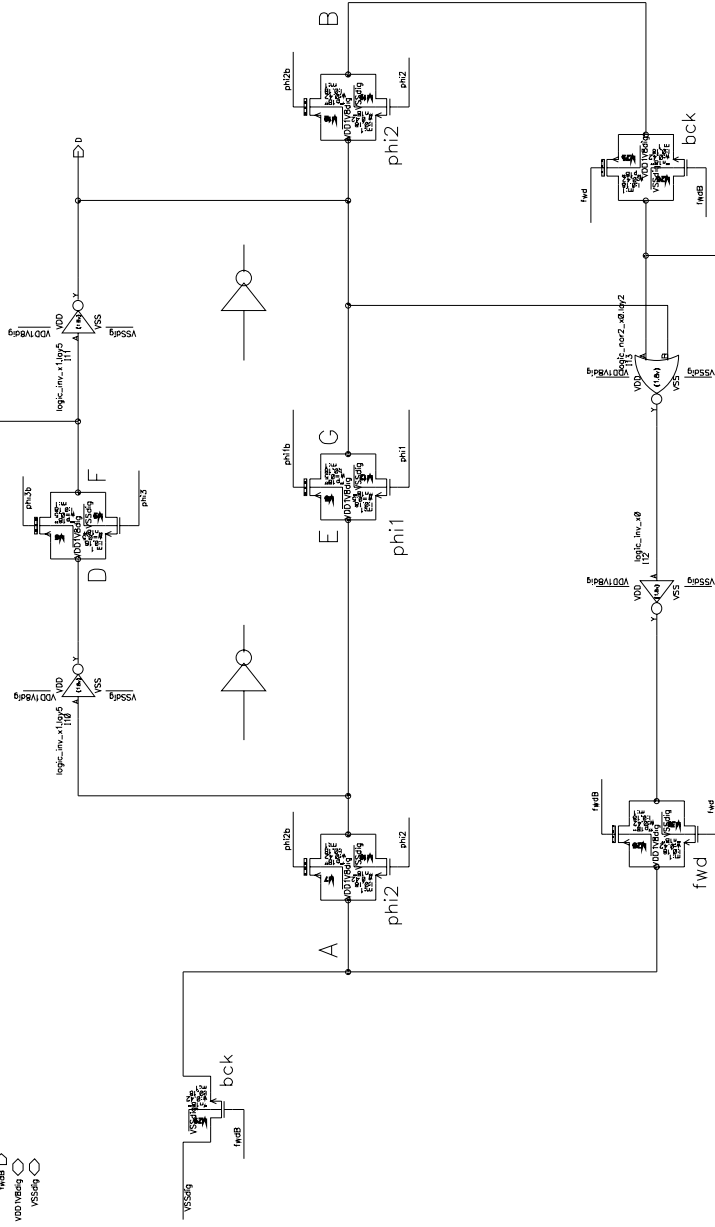
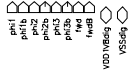
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_bldr_shift20.5_3clocks
Last QA Review	
Last Changed	Apr 19 11:33:26 2007



POWER UP phi1 off phi2 on RstB on (low)
IN-SERVICE RESET phi1 off phi2 on RstB pulsed on (low) during phi2
INVALID STATE phi1 X phi2 off (low) RstB on (low)

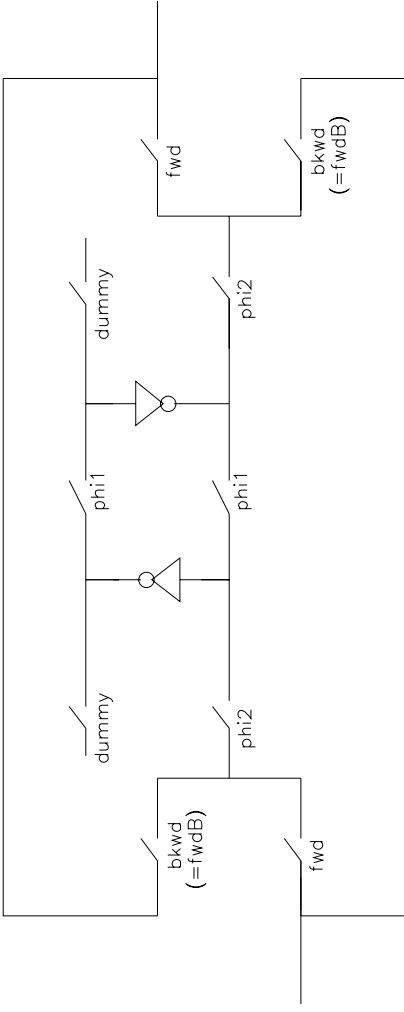


phi1 : Data Hold State  
 phi2 : Data transfer L>R (fwd=1)  
 phi2 : Data transfer R>L (fwd=0)

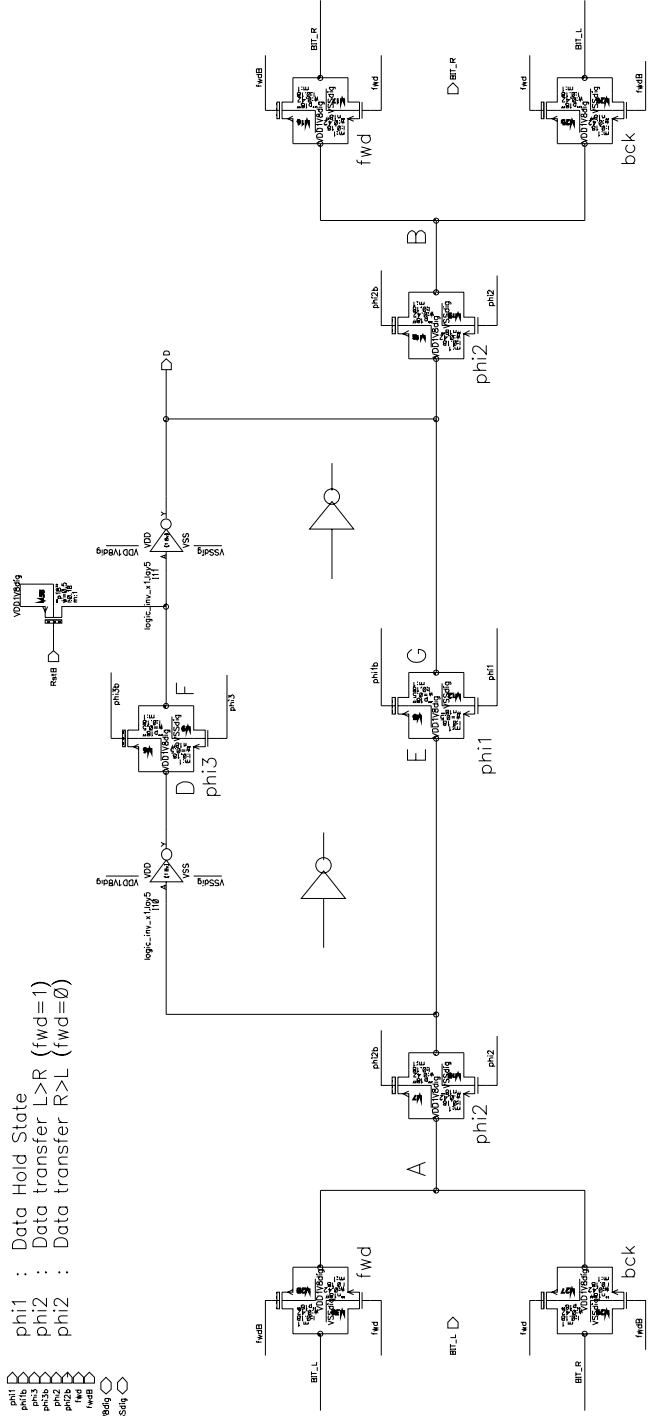
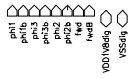


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	scrm_bidir_shift1.5_endstop_3clocks
Last OA Review	
Last Changed	Apr 19 10:55:08 2007

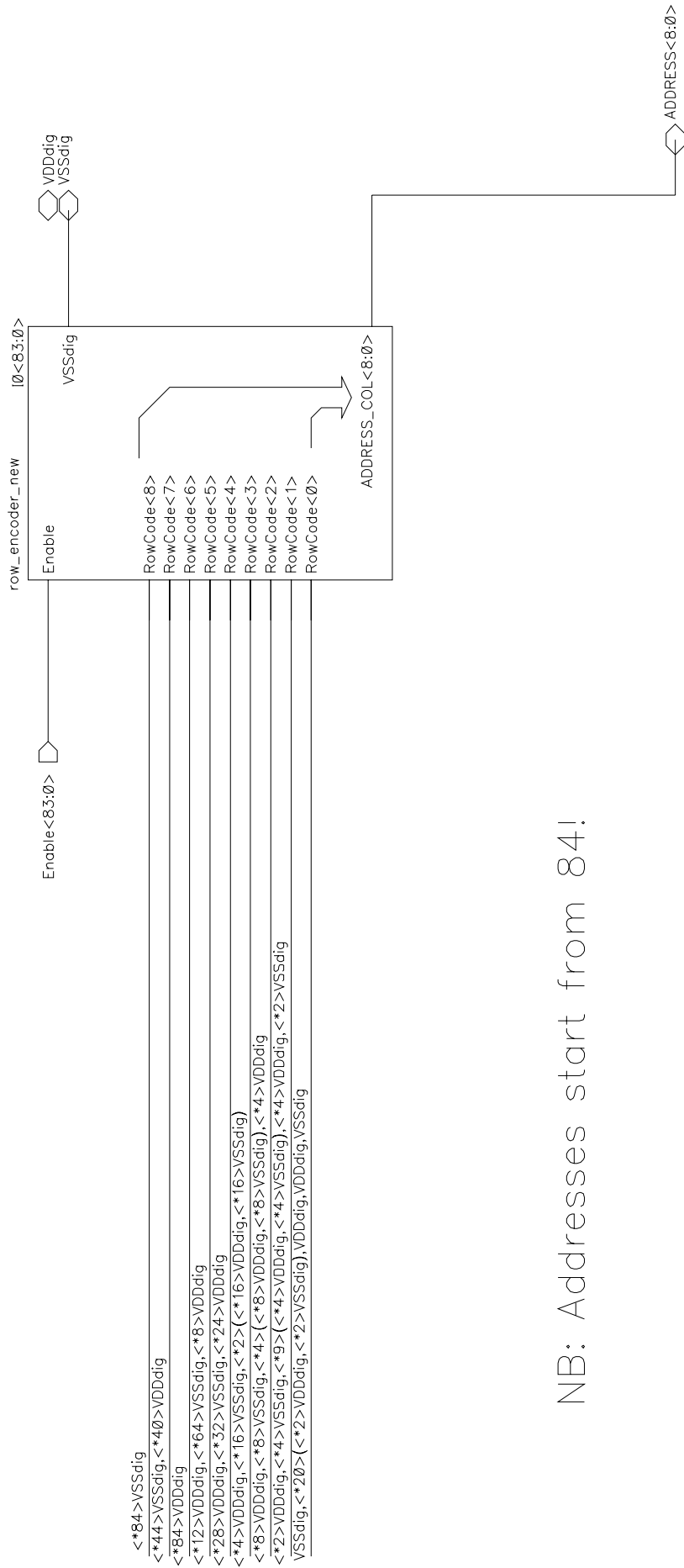
POWER UP phi1 off phi2 on RstB on (low)
IN-SERVICE RESET phi1 off phi2 on RstB pulsed on (low) during phi2
INVALID STATE phi1 X phi2 off (low) RstB on (low)



phi1 : Data Hold State  
 phi2 : Data transfer L>R (fwd=1)  
 phi3 : Data transfer R>L (fwd=0)

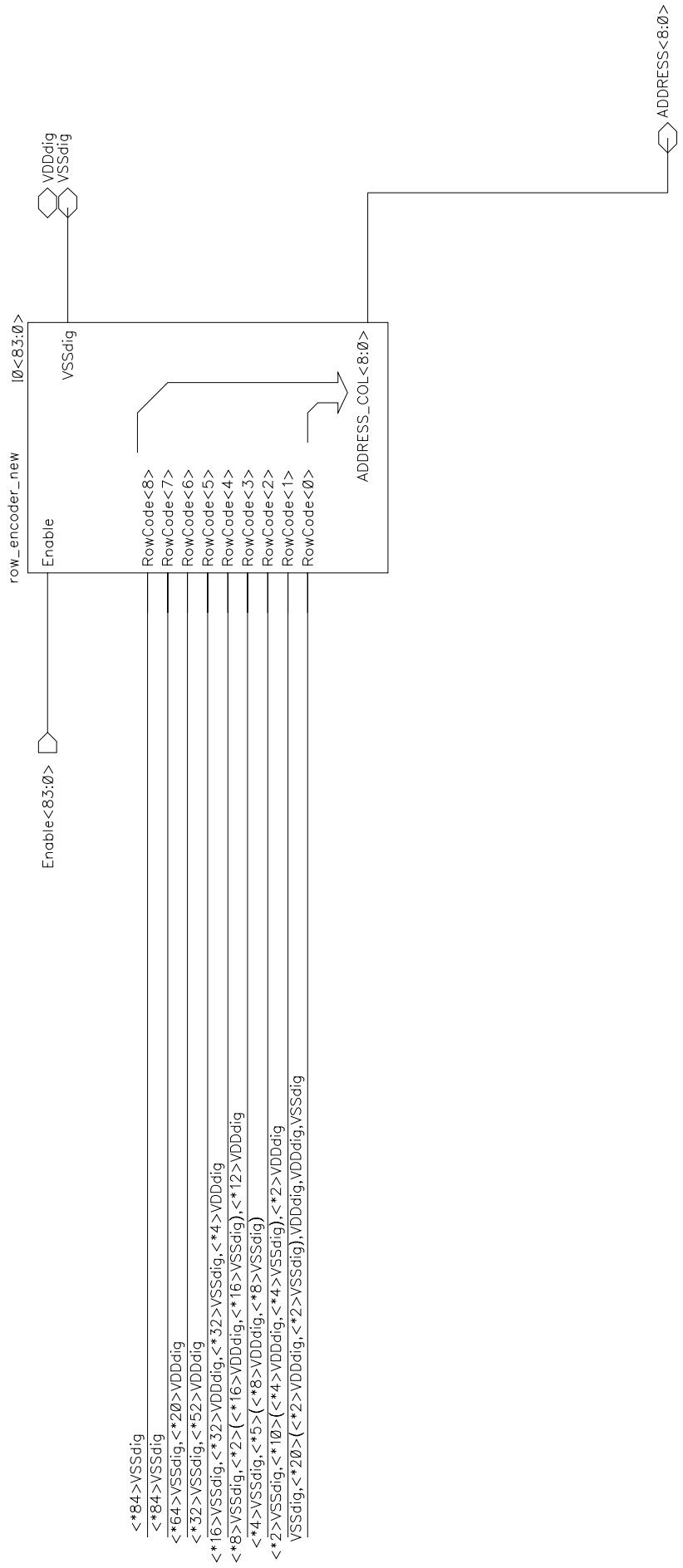


RAL Microelectronics Group	
Project	Tera-Phiel APS for CALICE
Library Name	calice_circuits
Block Name	scrm_bldr_shift1.5.3locks
Last QA Review	
Last Changed	Apr 19 11:06:51 2007

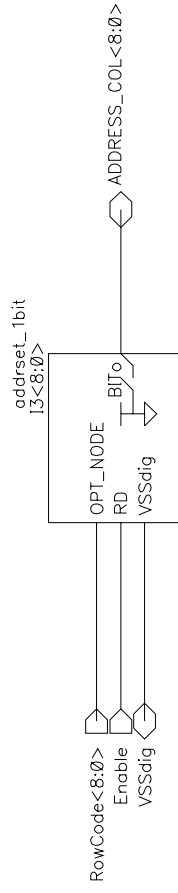


NB: Addresses start from 84!

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	addrset_84top
Last QA Review	
Last Changed	Mar 15 17:05:41 2007




RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	row_encoder_84
Last QA Review	
Last Changed	Jan 15 09:52:29 2007

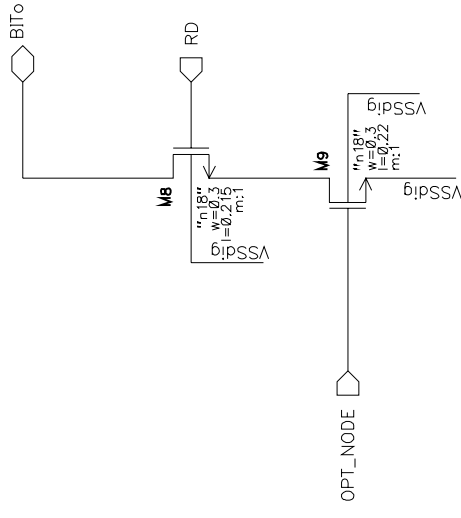


Set Row Code input to the unique row address: with net names in schematics; with repeated tie up/down cells in layout.

GRAY CODE should be used

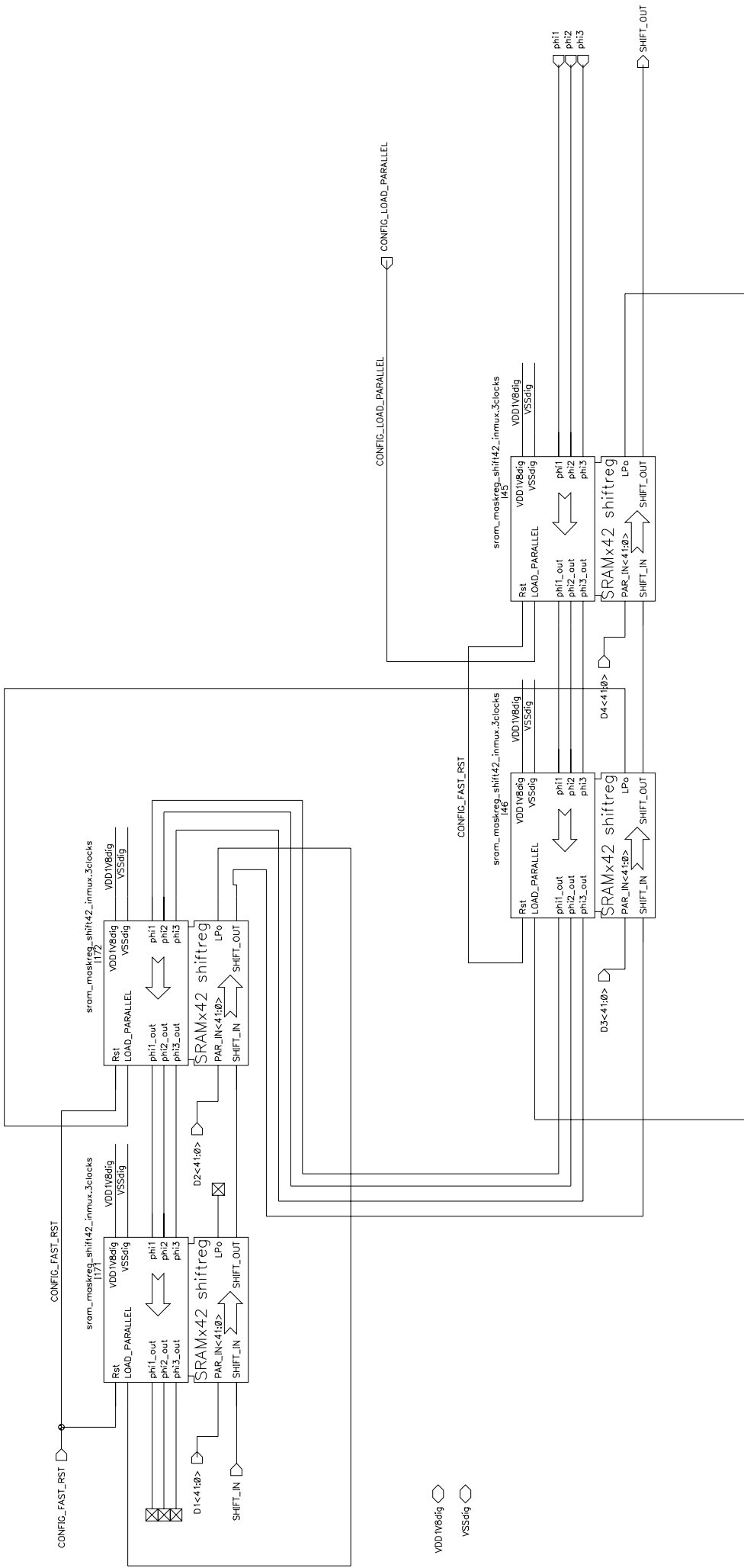
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	row_encoder_new
Last QA Review	
Last Changed	Jan 15 09:39:09 2007

VSSd1g 



The OPT\_NODE is to either vdd or gnd to effectively set the address code that will be read when RD is asserted

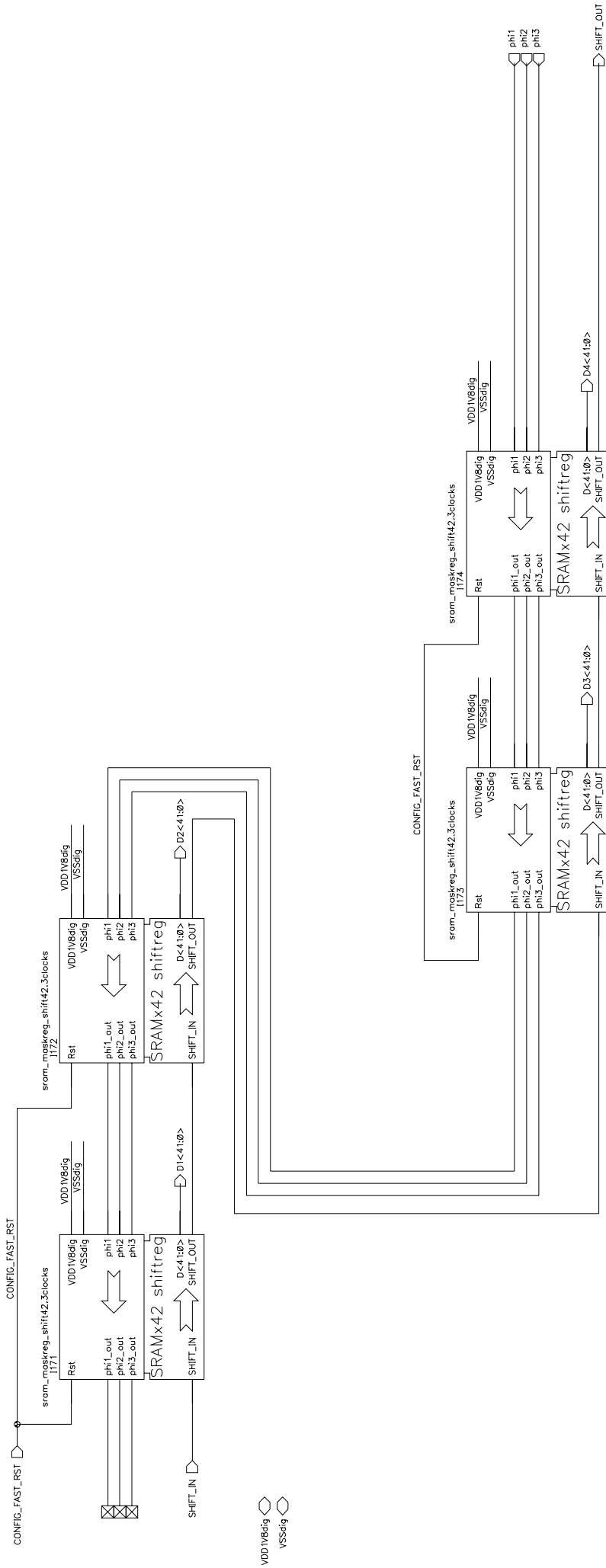
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	addrset_1bit
Last QA Review	
Last Changed	Jan 15 09:35:52 2007



VDD1V8dig ◊  
VSSdig ◊

RAL Microelectronics Group

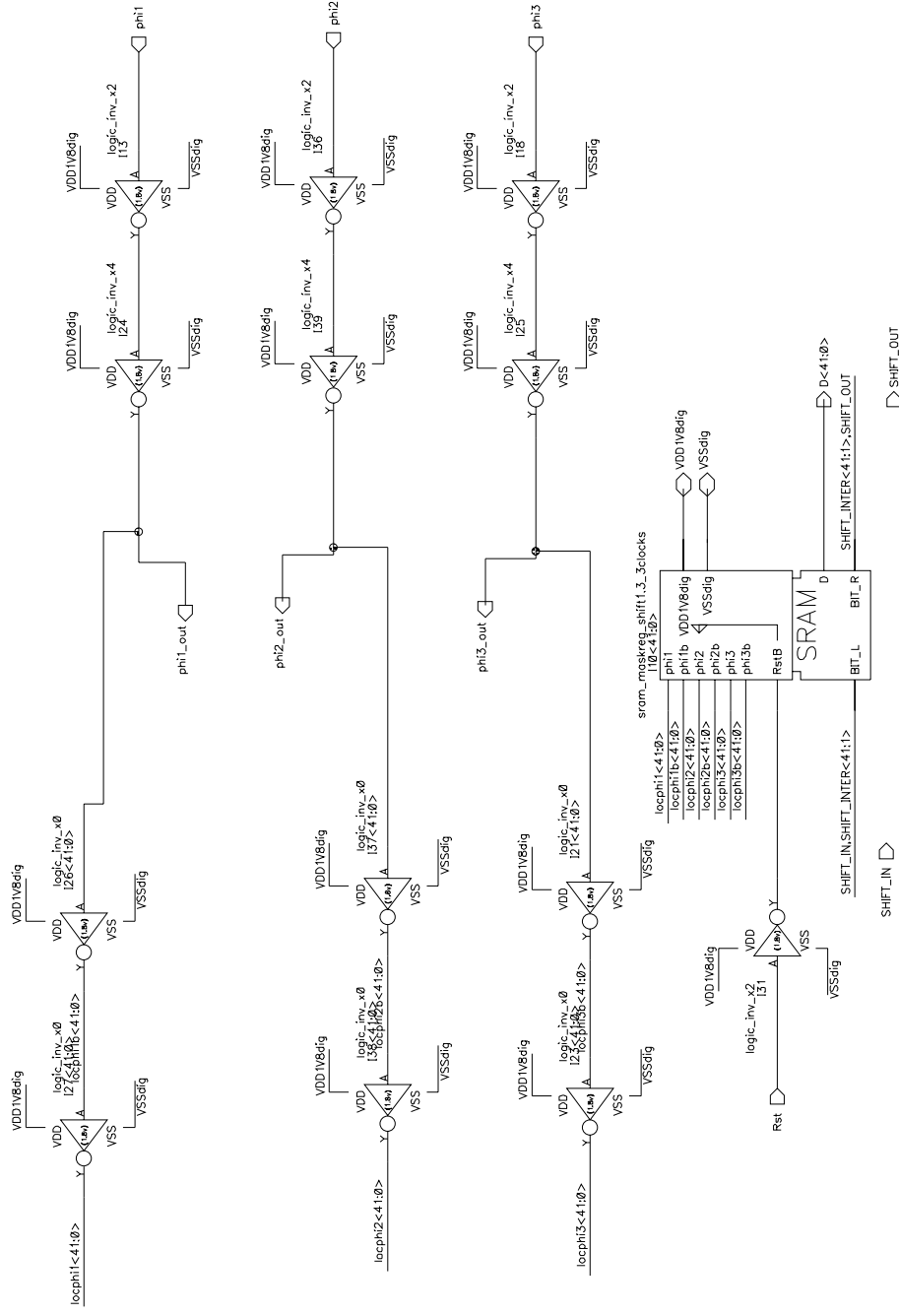
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	config_sr_bot_v1.1
Last QA Review	
Last Changed	Mar 19 13:07:17 2007



VDD1V8dig  
VSSdig

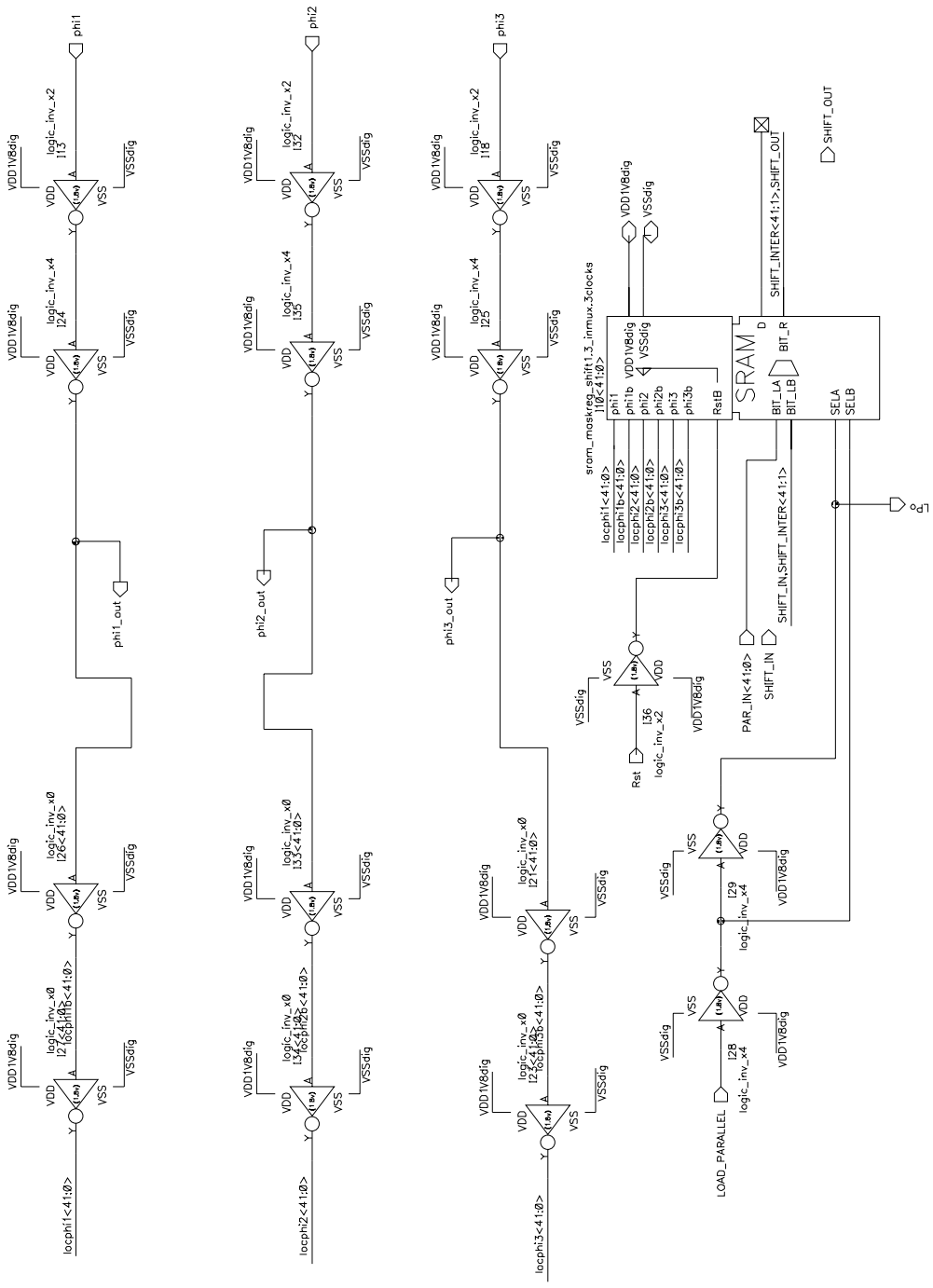
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	config_sr_top_v1.1
Last QA Review	
Last Changed	Mar 19 13:05:52 2007





Each cell has minimum size clock buffers to ensure clock integrity. 4x buffers drive the global clock signal for the length of the full 42 cells

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift42_3clocks
Last QA Review	
Last Changed	Jan 30 13:41:34 2007



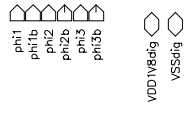
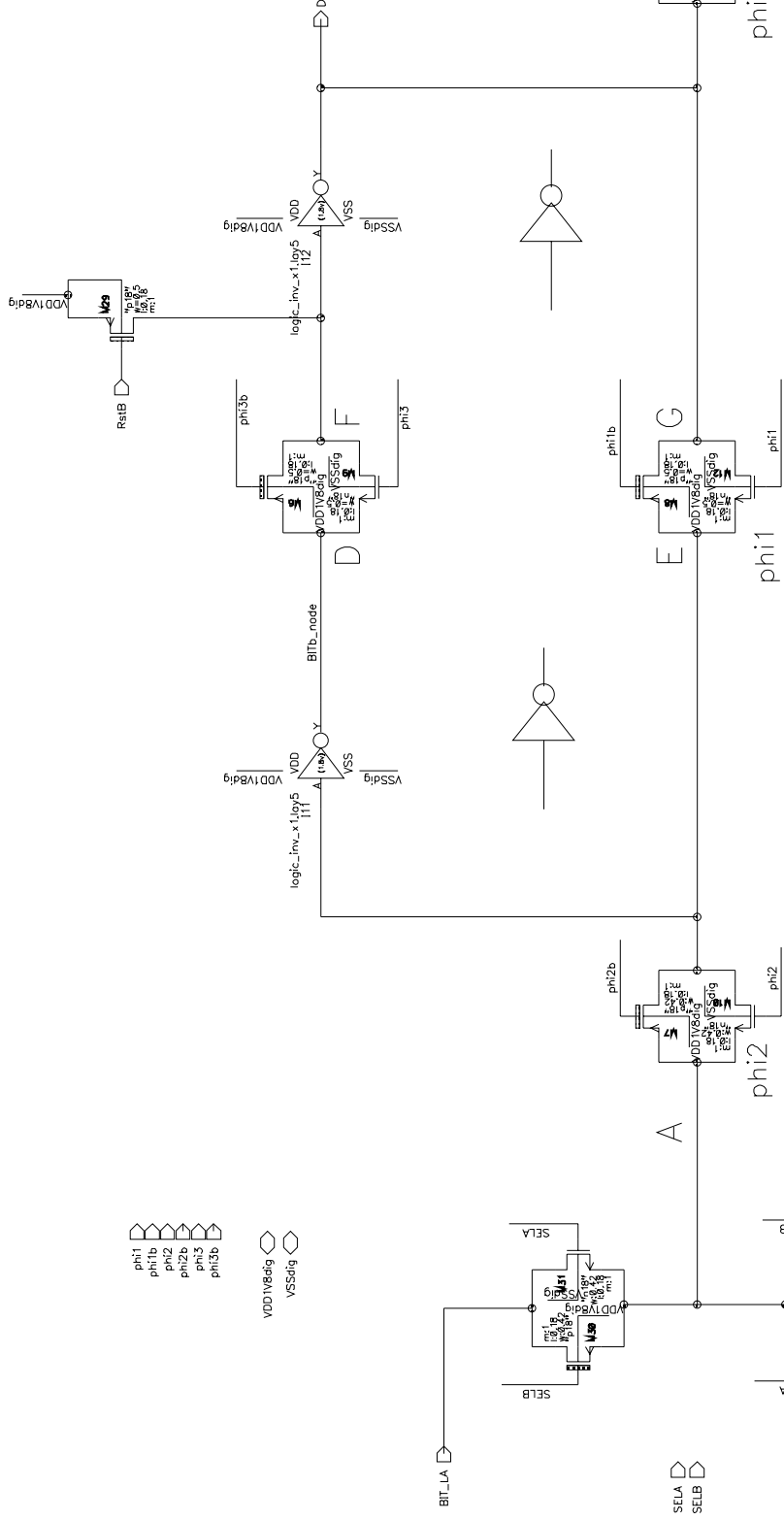
LOAD\_PARALLEL = 1 sets shift register inputs to point to the PAR\_IN<4:1:0> inputs

LOAD\_PARALLEL = 0 sets the shift register to internal serial mode (will shift its own data out)

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift42_inmux_3clocks
Last QA Review	
Last Changed	Mar 13 10:47:23 2007

### Shiftreg Revision 1.3 with input multiplexing

> Two inputs can be selected for use as either serial/parallel input



<p><b>POWER UP</b></p> <ul style="list-style-type: none"> <li>phi1 off</li> <li>phi2 on</li> <li>RstB on (low)</li> </ul>
<p><b>IN-SERVICE RESET</b></p> <ul style="list-style-type: none"> <li>phi1 off</li> <li>phi2 on</li> <li>RstB pulsed on (low) during phi2</li> </ul>
<p><b>INVALID STATE</b></p> <ul style="list-style-type: none"> <li>phi1 X</li> <li>phi2 off (low)</li> <li>RstB on (low)</li> </ul>

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift1.3_inmux.3locks
Last QA Review	
Last Changed	Mar 12 17:32:36 2007

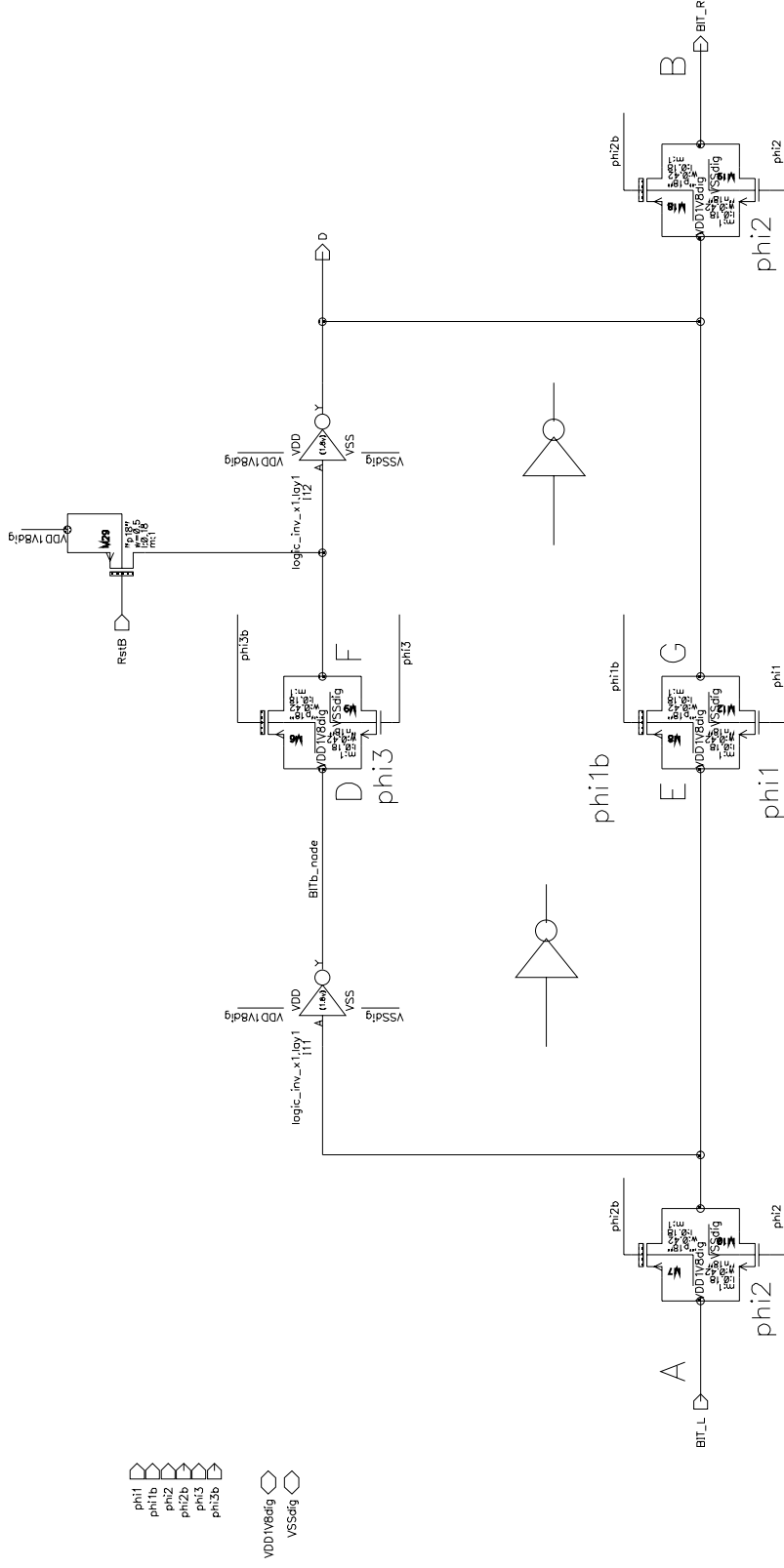
Layout inspired changes:

Reset transistor modified wider shorter  
 All TGs made width 0.42

> Added third clock for slow edge immunity

Resim & Check [ ]

New Shiftreg Revision 1.3 3CLOCKS!

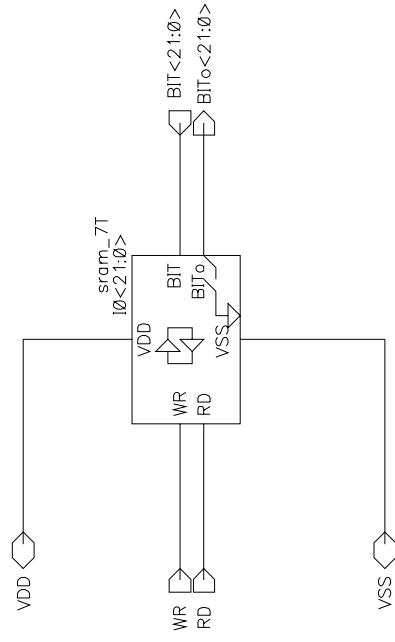


POWER UP  
 phi1 off  
 phi2 on  
 RstB on (low)

IN-SERVICE RESET  
 phi1 off  
 phi2 on  
 RstB pulsed on (low) during phi2

INVALID STATE  
 phi1 X  
 phi2 off (low)  
 RstB on (low)

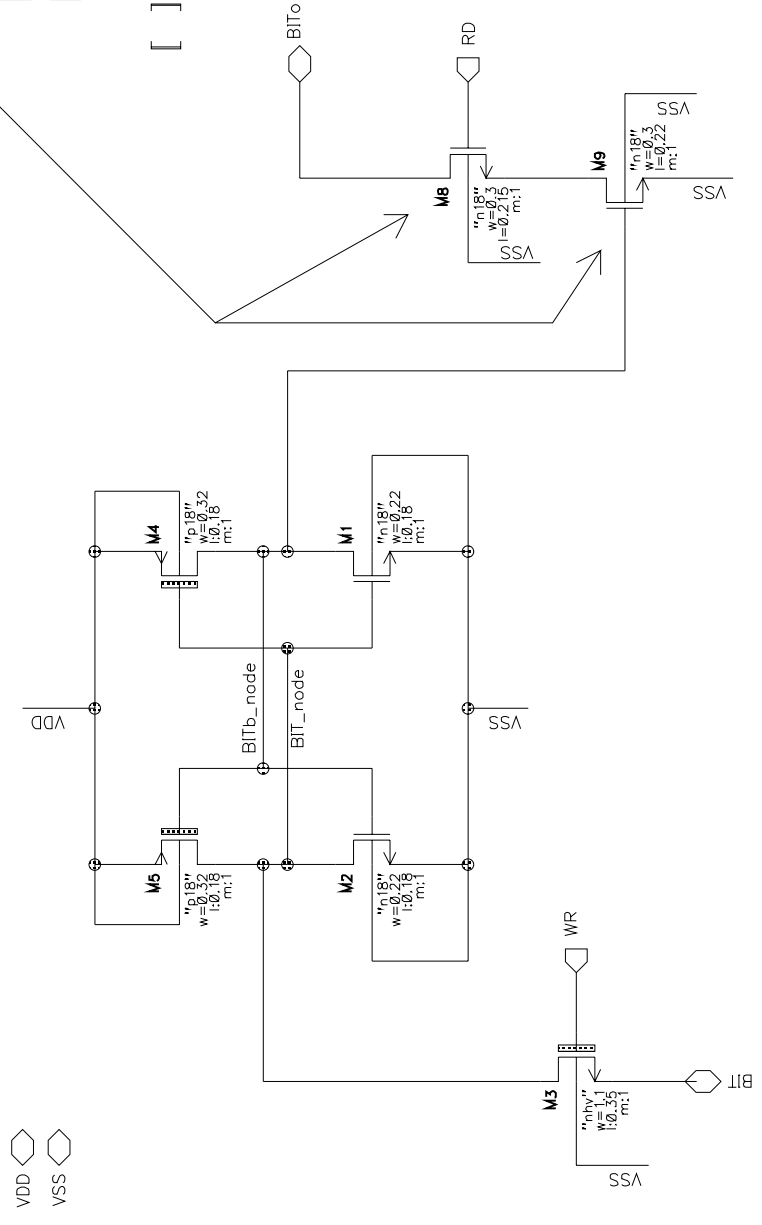
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift1.3_3clocks
Last QA Review	
Last Changed	Mar 12 11:20:58 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_reg7.22
Last QA Review	
Last Changed	Jan 2 16:08:03 2007

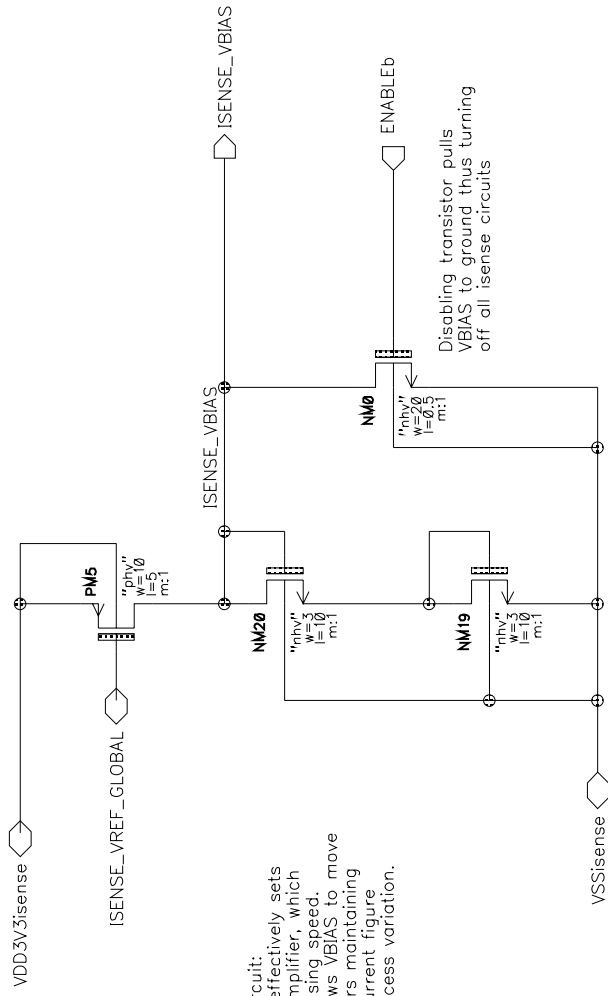
NB: TRANSISTOR LENGTH REDUCED TO 0.22um FOR BETTER LAYOUT

[ ] RE-SIM CORNERS



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_7T
Last QA Review	
Last Changed	Feb 19 18:38:06 2007

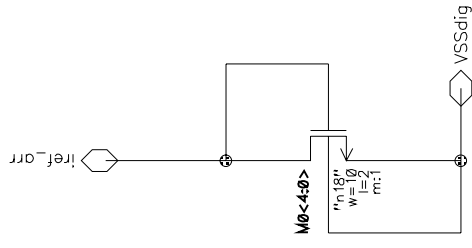
NOTE VDD MUST BE 3v3, hence hv transistors used



VBIAS generator circuit:  
 Current reference effectively sets current in sense amplifier, which effectively sets sensing speed.  
 Bias generator allows VBIAS to move with process corners maintaining approx constant current figure independent of process variation.

Disabling transistor pulls VBIAS to ground thus turning off all isense circuits

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_bias_v1.2
Last QA Review	
Last Changed	Mar 2 17:52:37 2007



5:1

500uA typ

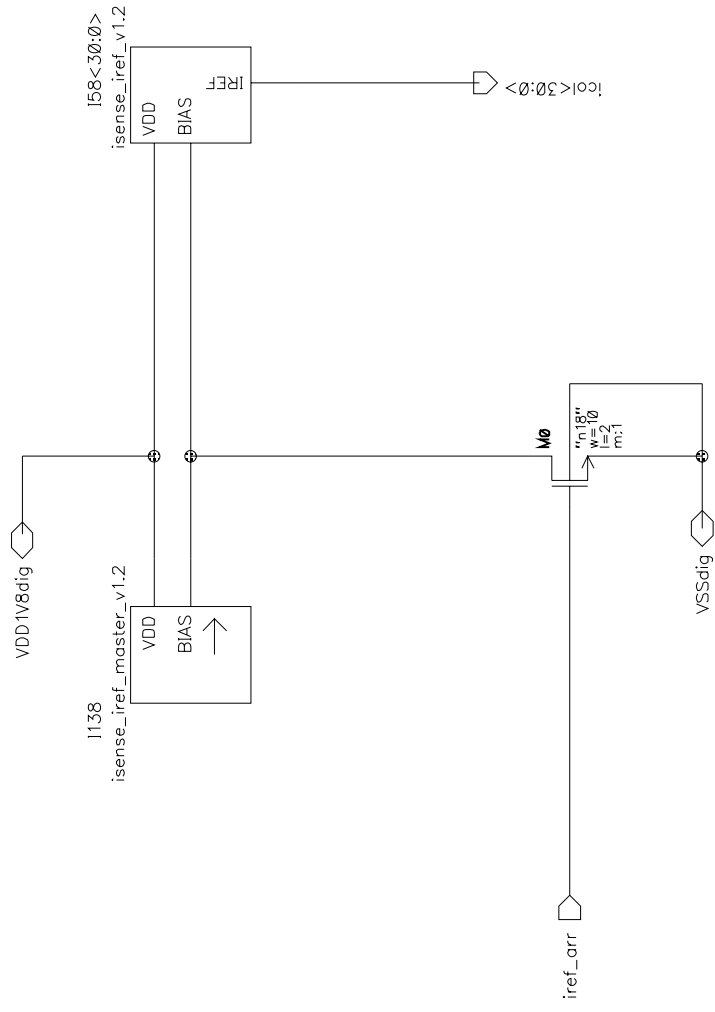
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_0rr
Last QA Review	
Last Changed	Apr 10 09:08:45 2007



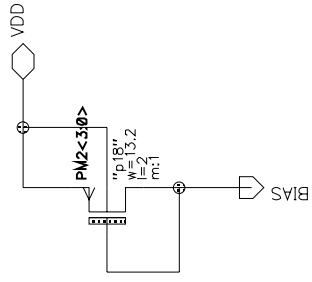
10uA typ

2.5uA typ

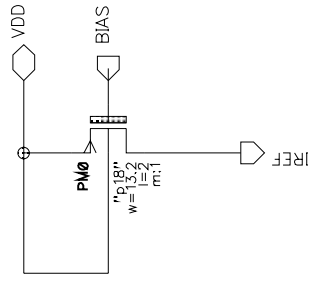
4:1



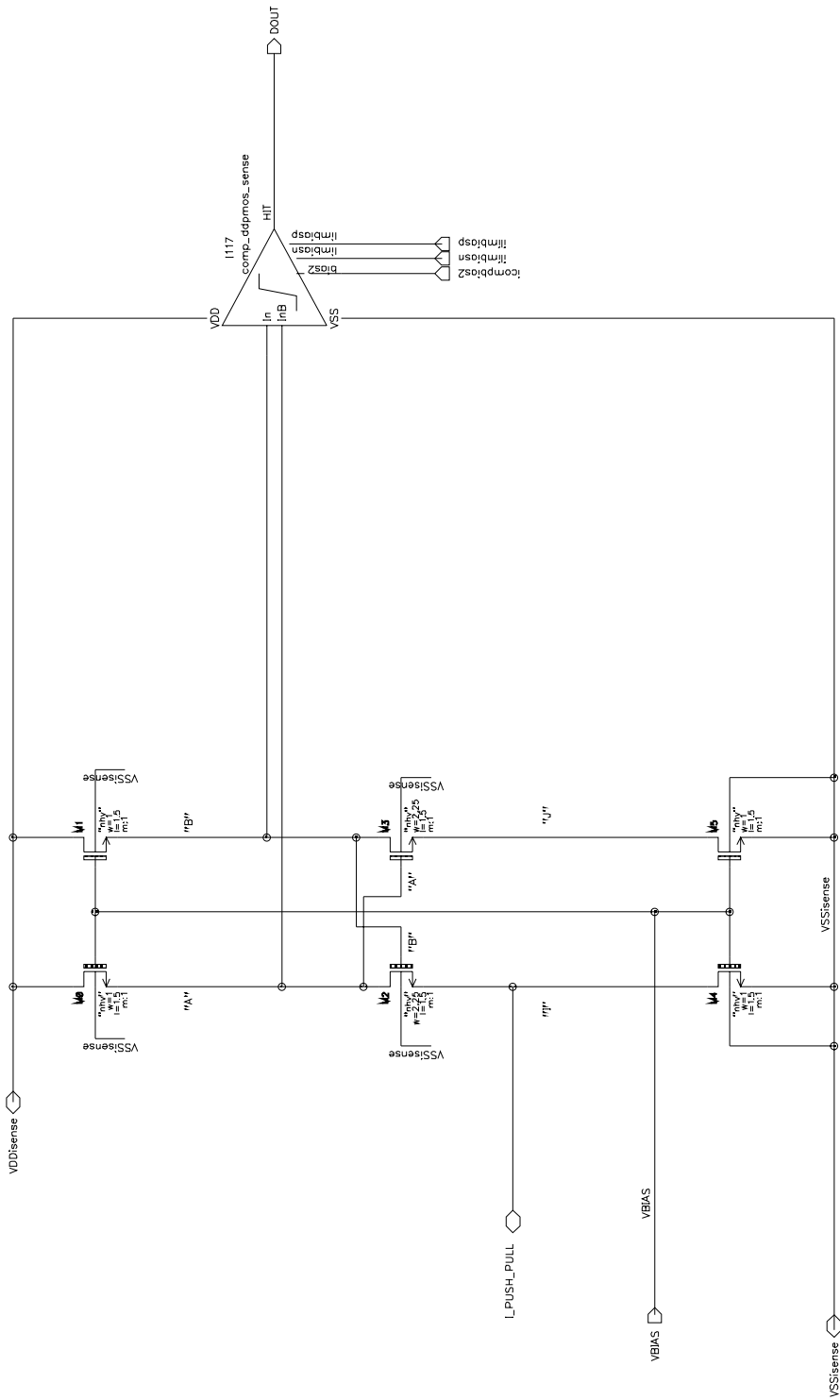
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_col
Last QA Review	
Last Changed	Mar 14 13:29:16 2007



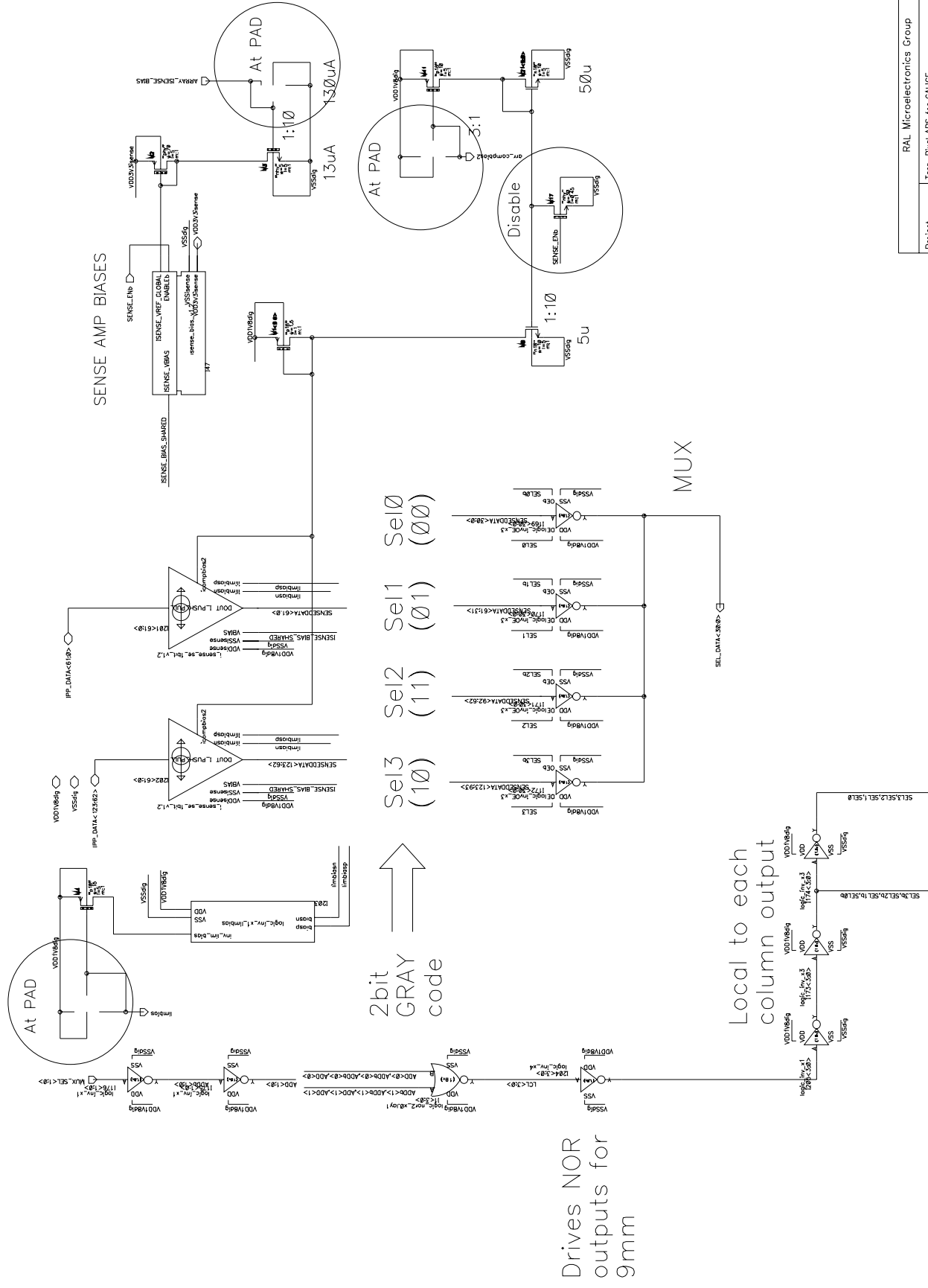
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_master_v1.2
Last QA Review	
Last Changed	Dec 14 11:49:02 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_v1.2
Last QA Review	
Last Changed	Sep 29 10:33:57 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	i_sense_se_1bit_v1.2
Last QA Review	
Last Changed	Mar 1 17:58:05 2007

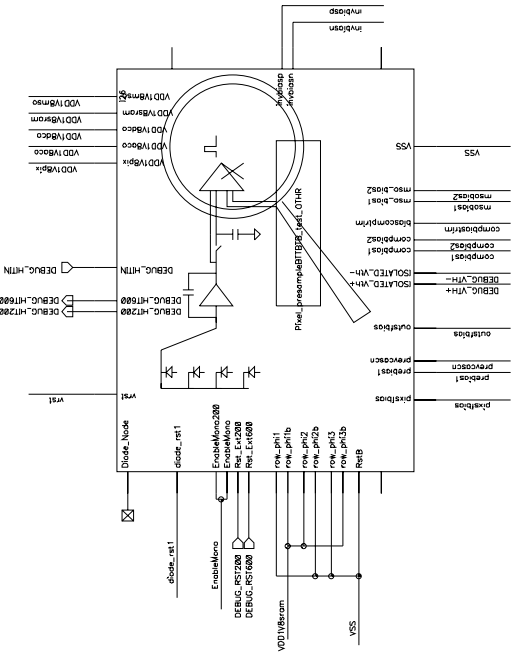


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sense_mux_v1.2
Last OA Review	
Last Changed	Mar 29 10:56:11 2007



- VH
- VDDVb1+
- VDDVb1-
- VDDVb2+
- VDDVb2-
- VDDVb3+
- VDDVb3-
- VDDVb4+
- VDDVb4-
- VDDVb5+
- VDDVb5-
- VSS

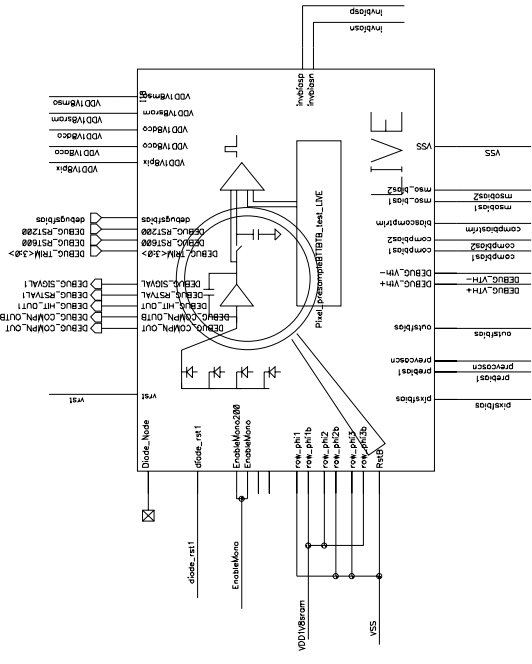
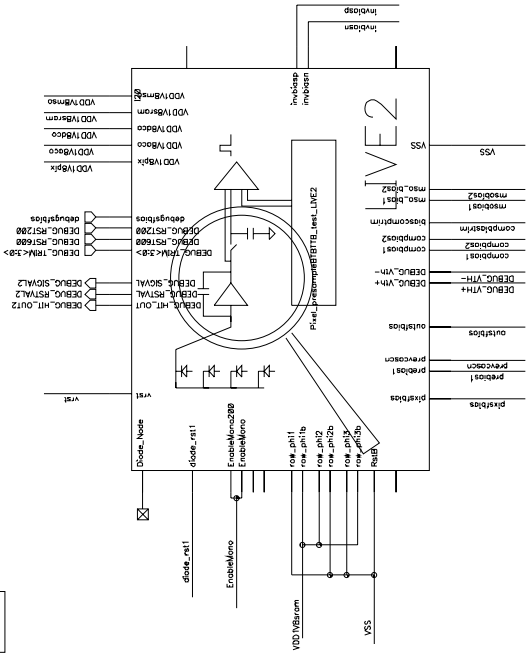
- EnableMono
- diode\_rst1
- DEBUC\_VH+
- DEBUC\_VH-
- DEBUC\_VH+
- DEBUC\_VH-
- prebias1
- prebias2
- prebias3
- prebias4
- prebias5
- compbias1
- compbias2
- compbias3
- compbias4
- compbias5
- mso\_bias2
- mso\_bias1
- Invb2p
- Invb2n



LIVE1

LIVE2

OTHR



Project	RAL Microelectronics Group
Library Name	Tera-Pixel APS for CALICE
Block Name	calice_circuits
Last OA Review	Pixel_presampleBITTB1B_test_setof3
Last Changed	Apr 21 14:45:44 2007

# TEST STRUCTURE PIXEL 2

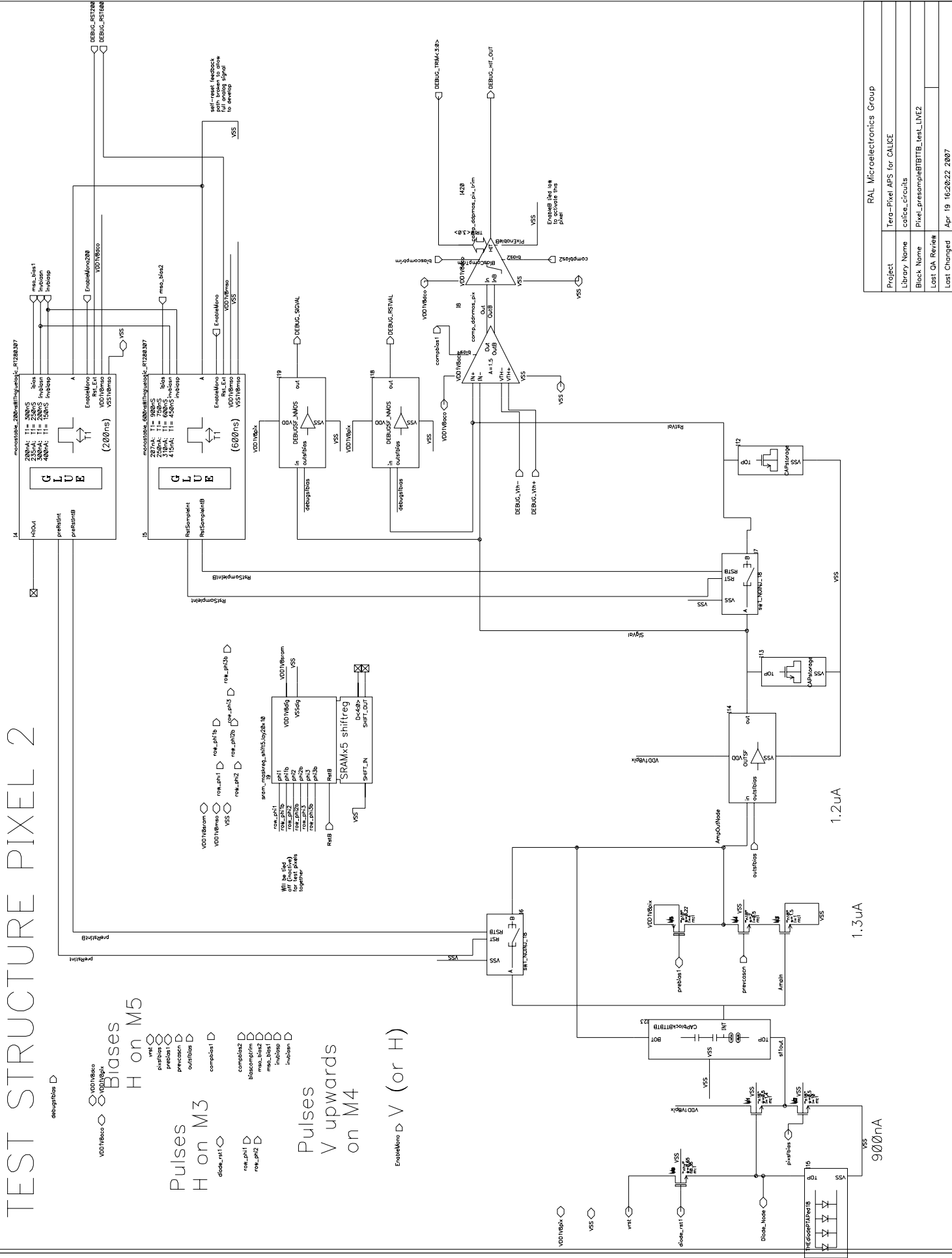
debugsignals D

VDD1V8eoc  
VDD1V8gk  
Biases  
H on M5

Pulses  
H on M3

Pulses  
V upwards  
on M4

EnableM5  
V (or H)



RAL Microelectronics Group



# TEST STRUCTURE PIXEL

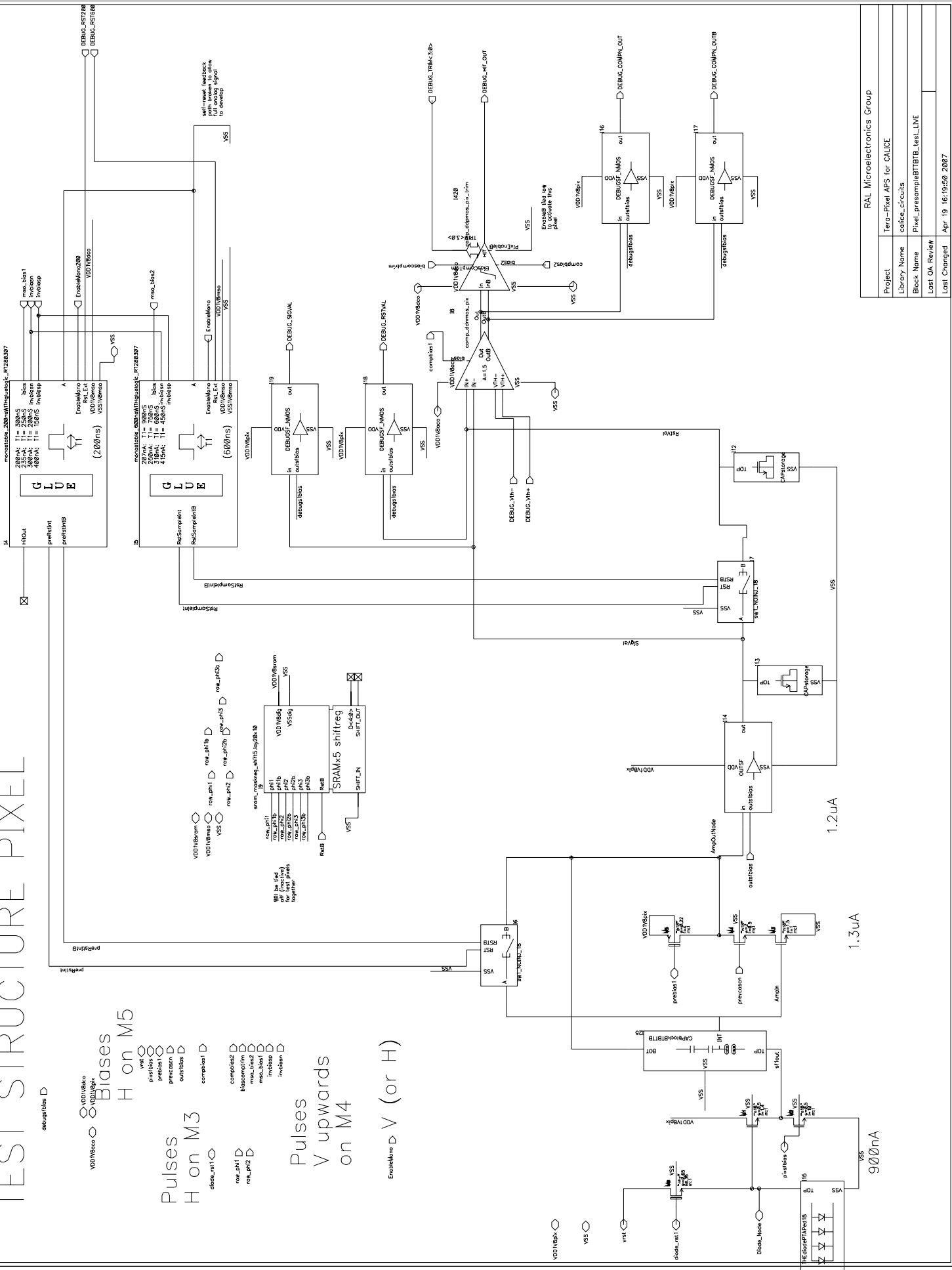
debugsignals D

VDD1V8eoc VDD1V8eok  
Biases  
H on M5

Pulses  
H on M3

Pulses  
V upwards  
on M4

EnableLens V (or H)



Project	Tero-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presampleBTBTIB_test_LIVE
Last OA Review	Apr 19 16:19:56 2007
RAL Microelectronics Group	

# TEST STRUCTURE NEIGHBOURS

VDD/VBico  $\odot$  VDD/VBco  
 VDD/VBco  $\odot$  VDD/VBco  
 Biases

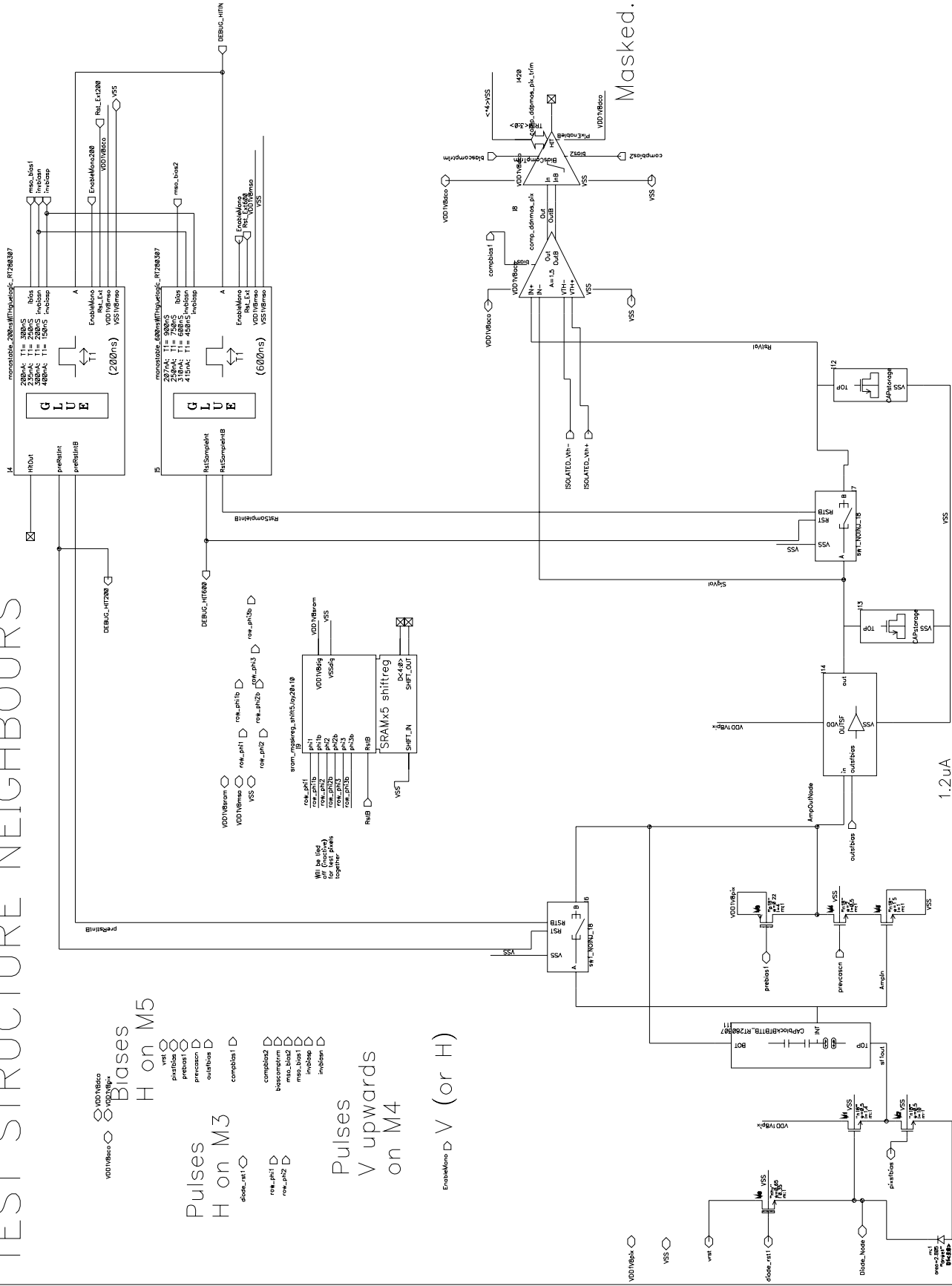
H on M5

Pulses  
 H on M3

done\_rst1  $\square$   
 row\_ph11  $\square$   
 row\_ph12  $\square$

Pulses  
 V upwards  
 on M4

enable\_k0  $\square$  V (or H)

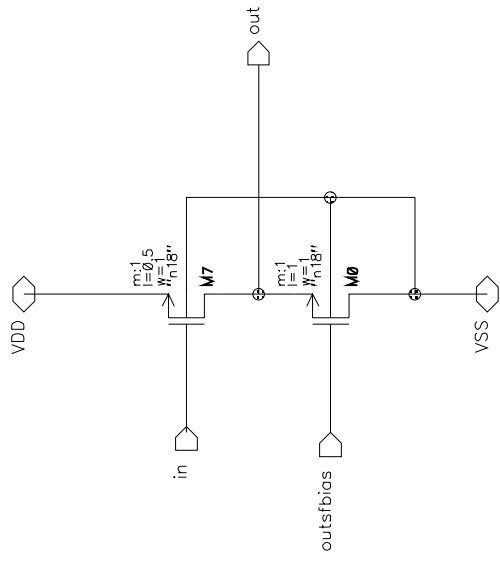


900nA

1.3uA

1.2uA

Project	RAL Microelectronics Group
Library Name	Tera-Pixel APS for CALICE
Block Name	calice_circuits
Last OA Review	Pixel_presampleBITTB_test_OTHR
Last Changed	Apr 20 16:03:16 2007

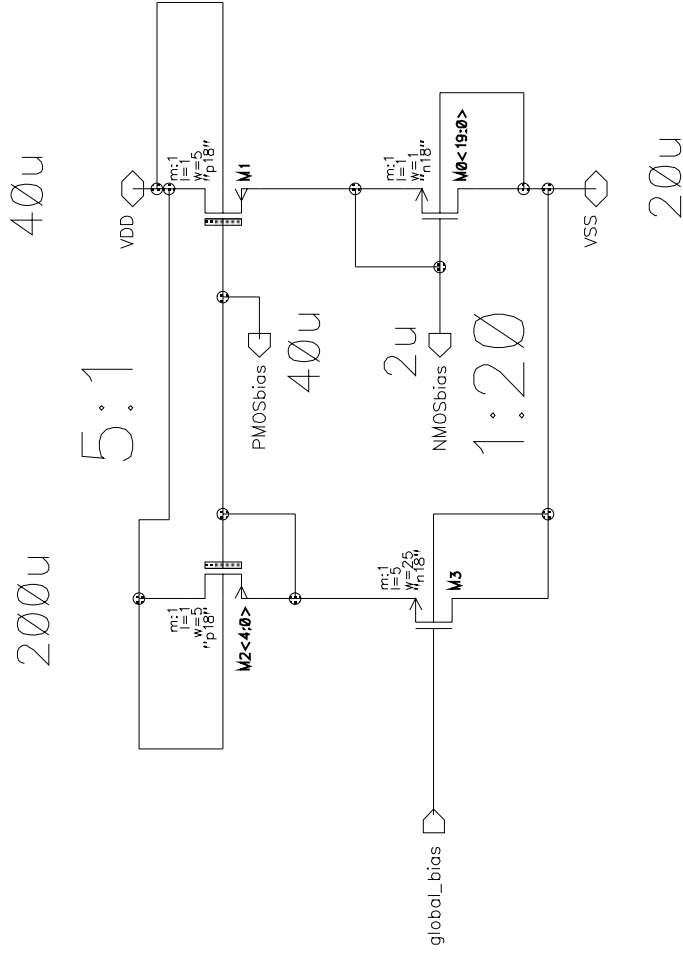


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	DEBUGSF_NMOS
Last QA Review	
Last Changed	Jul 3 13:42:33 2007

Note: 28-6-07

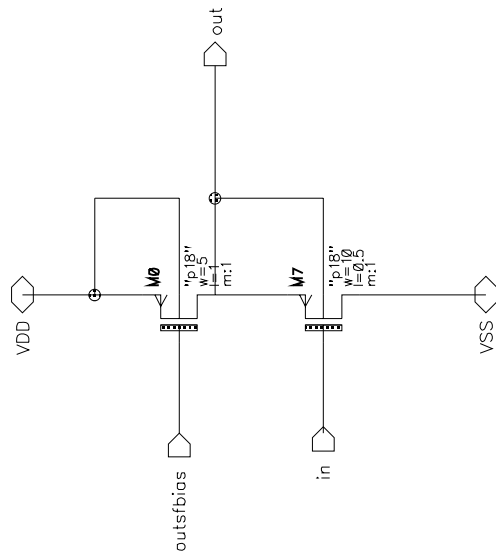
Transistor symbols upside-down (noticed post-submission, hence not changed in this version of schematic)

No effect to operation, but should be corrected if this cell is used in ASIC2.

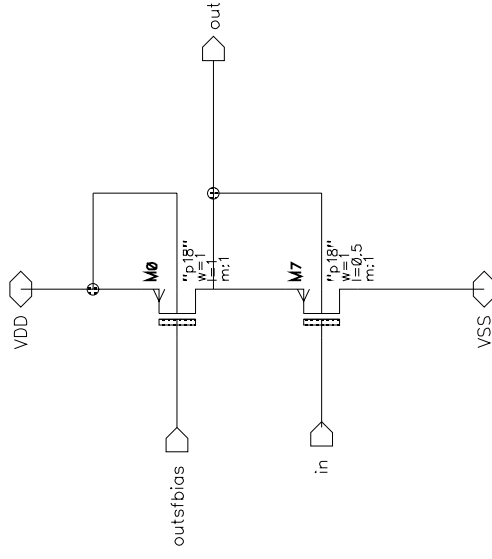


PMOS bias is 20x NMOS bias

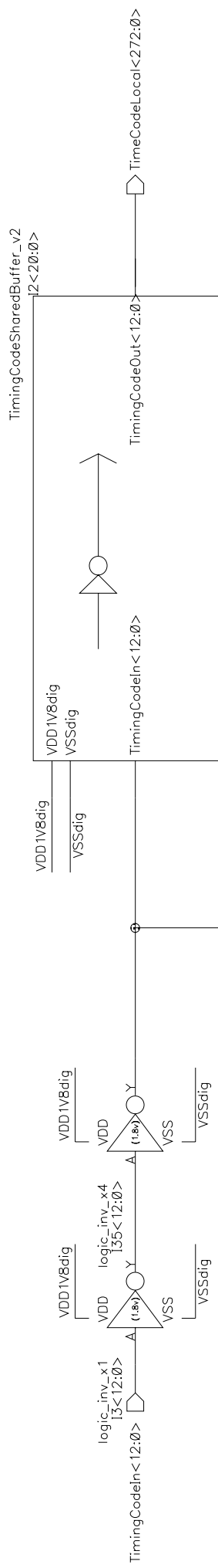
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	DEBUGSF_NMOS_BIAS
Last QA Review	
Last Changed	Jun 28 09:06:56 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	DEBUGSF_PMOS
Last QA Review	
Last Changed	Jul 3 13:42:59 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	OUTSF
Last QA Review	
Last Changed	Jun 27 11:54:06 2007



x4 buffers drive the full column length (84 pix)

Timing Code in the column is in inverted format

Correct polarity output to next column (this cell again)

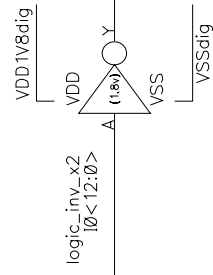
a local buffer drives 4 rows worth of SRAM cells the four rows to save space.

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	TimingCodeDistribution_v2
Last QA Review	
Last Changed	Mar 5 16:22:47 2007

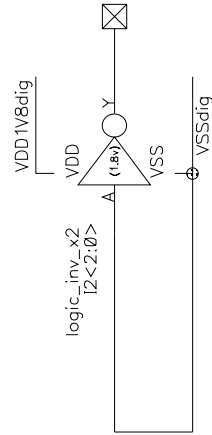
VDD1V8dig  
VSSdig

TimingCodeIn<12:0>

TimingCodeOut<12:0>



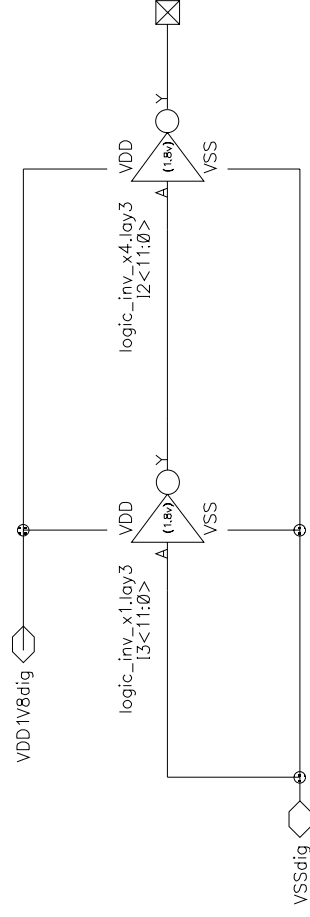
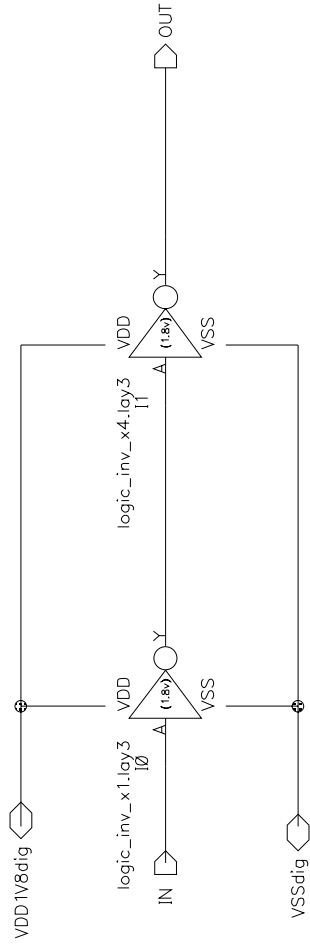
TimingCodeIn<12:0>



Spare inverters  
tied off (not  
used in repeated  
layout cell)

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	TimingCodeSharedBuffer_v2
Last QA Review	
Last Changed	Mar 5 11:36:51 2007

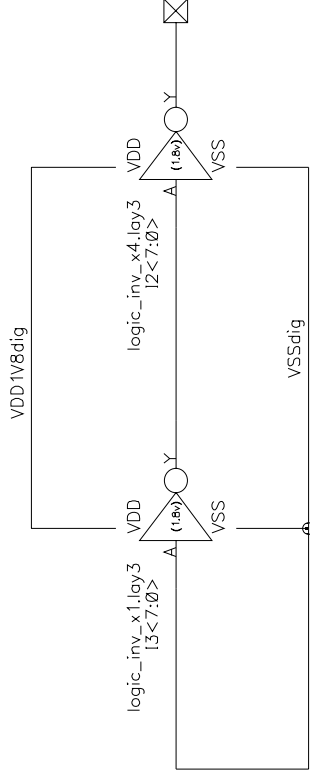




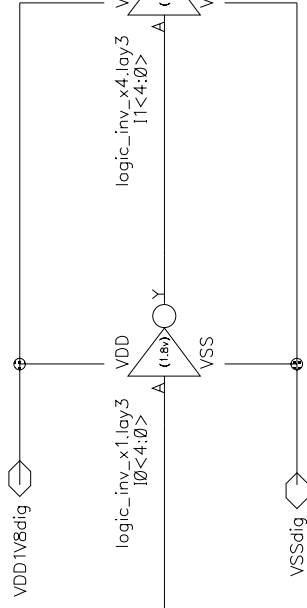
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_rpt_buffers_DN_debug
Last QA Review	
Last Changed	Jul 3 13:43:19 2007

Inactive buffers tied off (same layout cell can be used with only minor changes)

- MA<5:0>
- P1<1:0>
- P2<1:0>
- P3<1:0>
- RST<1:0>



VDD1V8dig



MA<3>,P1<1>,P2<1>,P3<1>,RST<1>

DEBUG\_MA,DEBUG\_P1,DEBUG\_P2,DEBUG\_P3,DEBUG\_RST

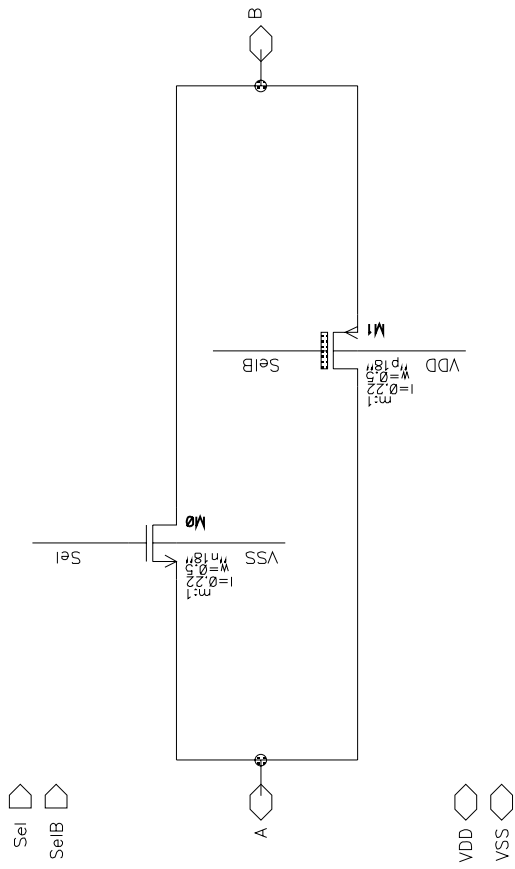
- DEBUG\_MA
- DEBUG\_P1
- DEBUG\_P2
- DEBUG\_P3
- DEBUG\_RST

Spare lines

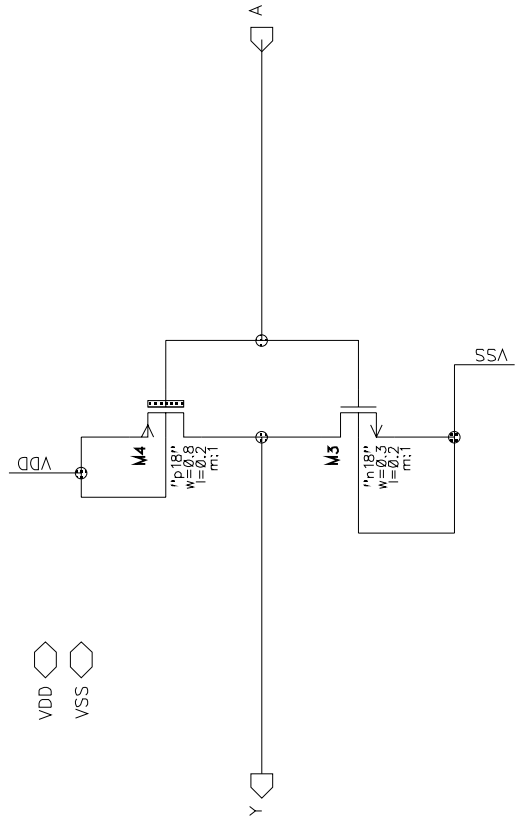
MA<5:4>,MA<2:0>,P1<0>,P2<0>,P3<0>,RST<0>



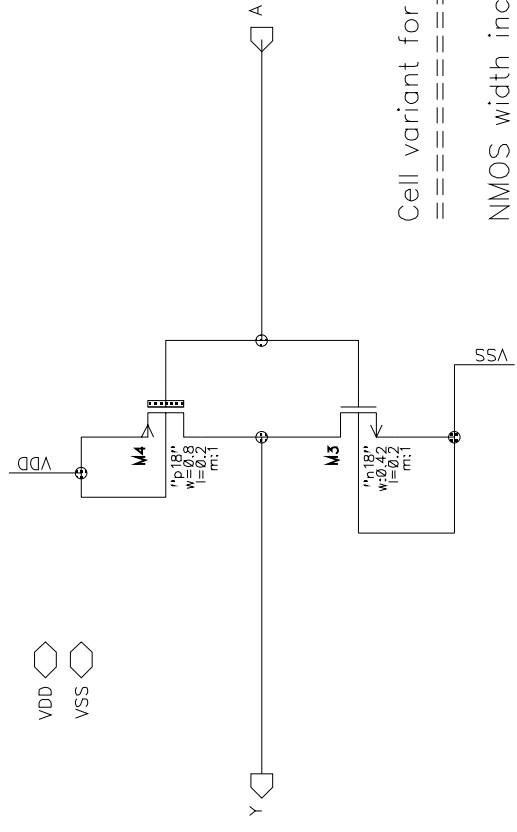
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_rpt_buffers_debug
Last QA Review	
Last Changed	Jul 3 13:37:44 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sw1_18
Last QA Review	
Last Changed	Sep 28 11:41:21 2006



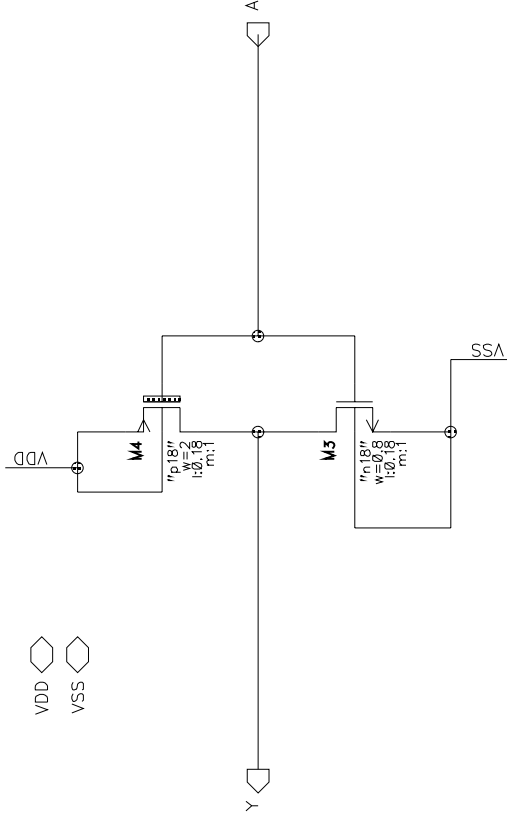
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x0
Last QA Review	
Last Changed	Sep 28 11:41:11 2006



Cell variant for layout ".lay1"

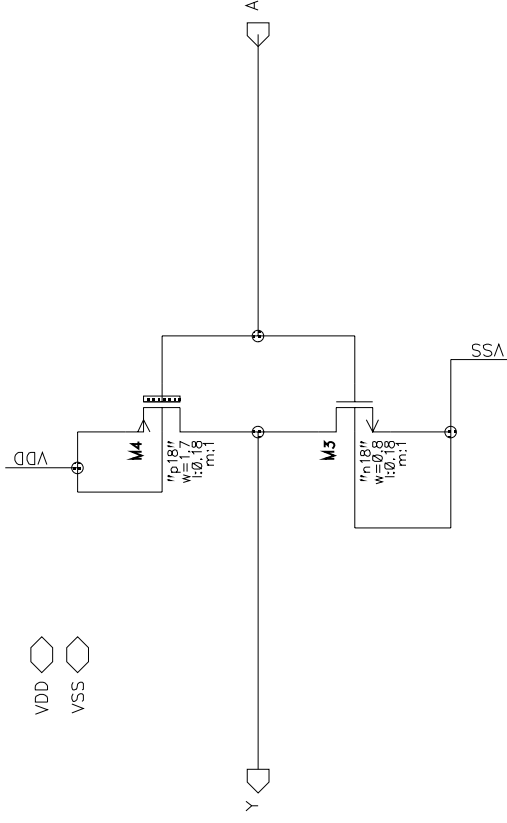
NMOS width increased from 0.3 to 0.42um

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x0.lay1
Last QA Review	
Last Changed	Jan 11 15:41:07 2007

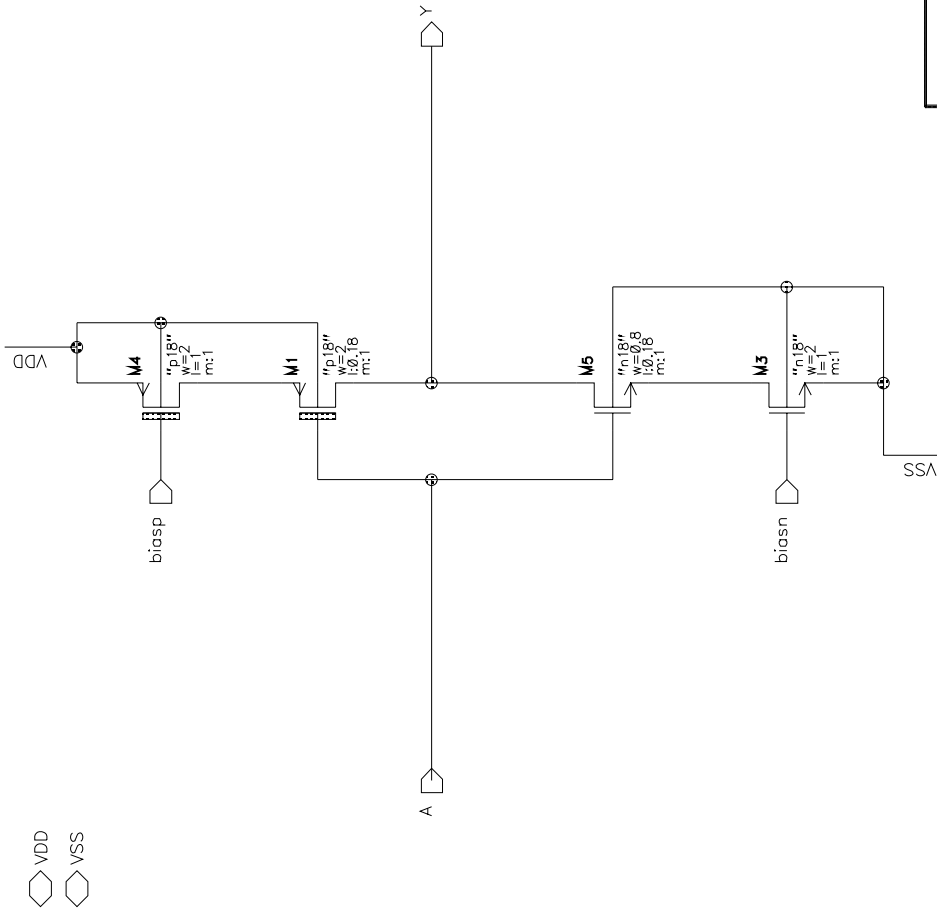


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

PMOS width reduced from 2um to 1.7um  
to aid efficient SRAM layout



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1.lay1
Last QA Review	
Last Changed	Feb 9 10:48:31 2007



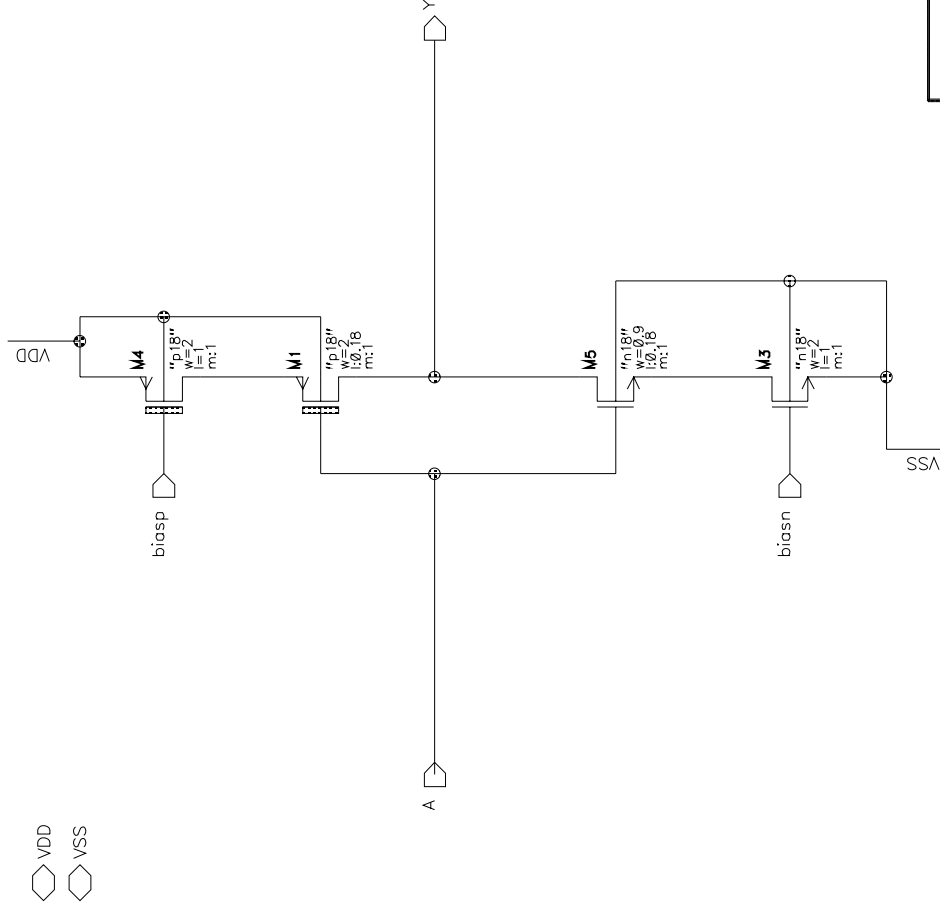
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_lim
Last QA Review	
Last Changed	Jan 22 16:24:31 2007



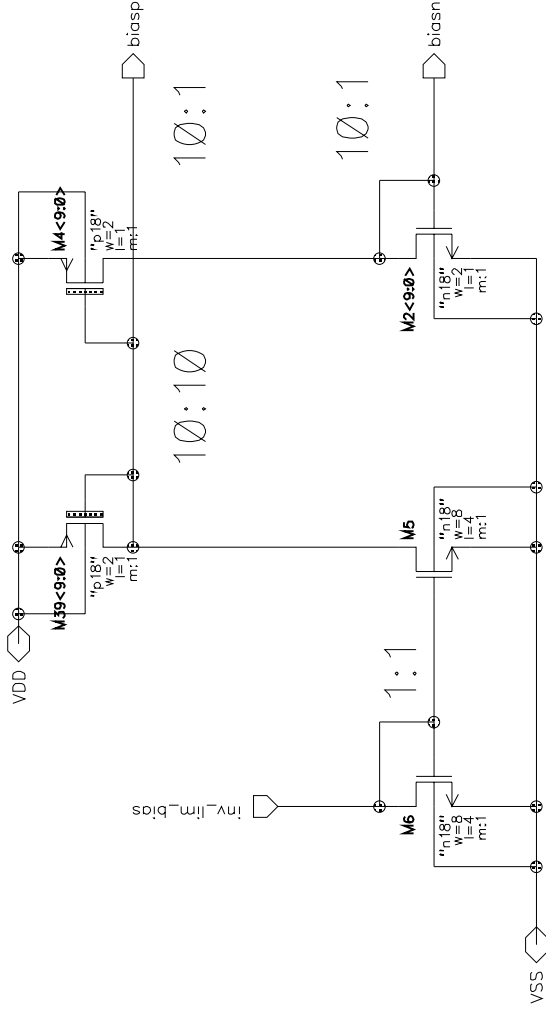
# Layout variant 1

=====

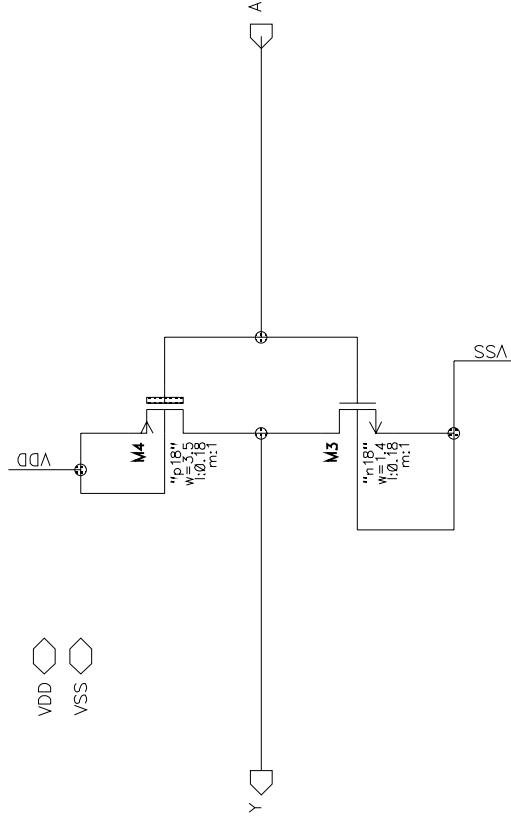
NMOS width increased from 0.8 to 0.9 so there are two contacts in the pcell (preferred for yield)



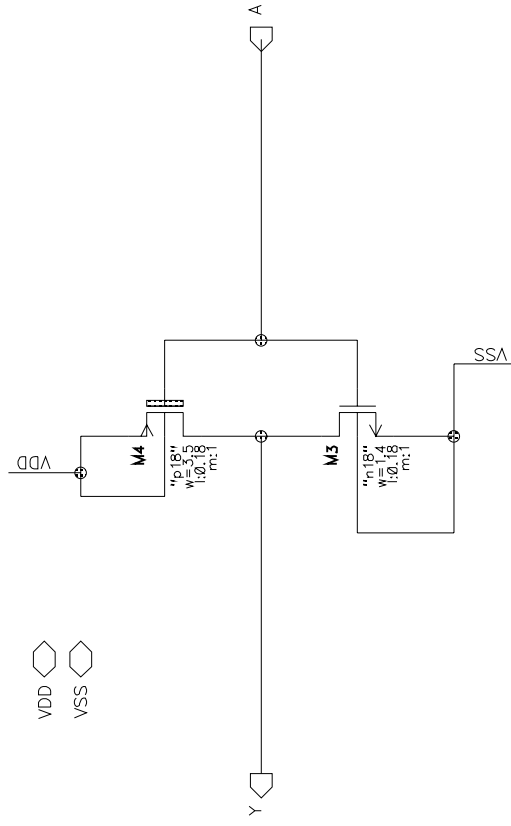
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_lim.lay1
Last QA Review	
Last Changed	Feb 20 17:08:47 2007



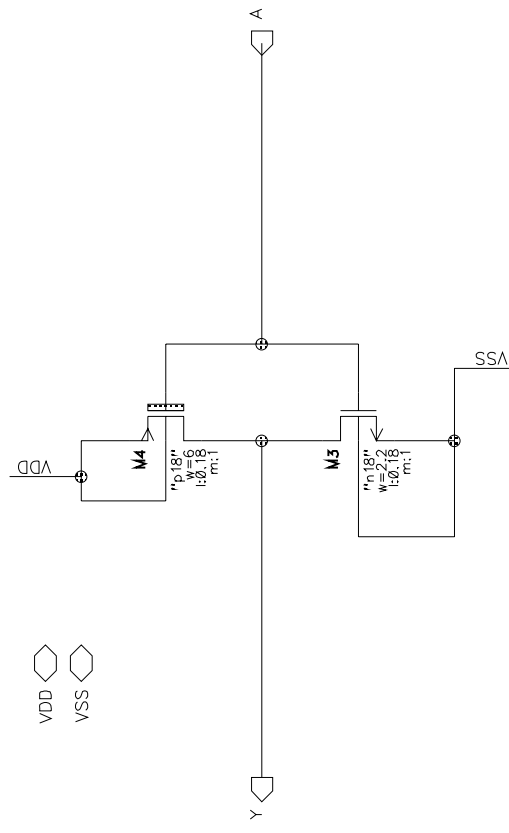
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_limbias
Last QA Review	
Last Changed	Mar 3 13:08:07 2007



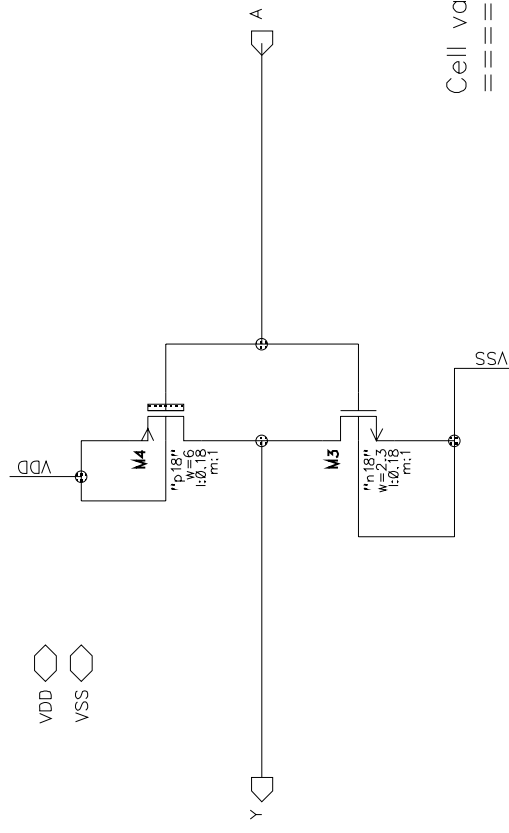
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x2
Last QA Review	
Last Changed	Sep 28 11:45:54 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x2.lay3
Last QA Review	
Last Changed	Sep 28 11:45:54 2006

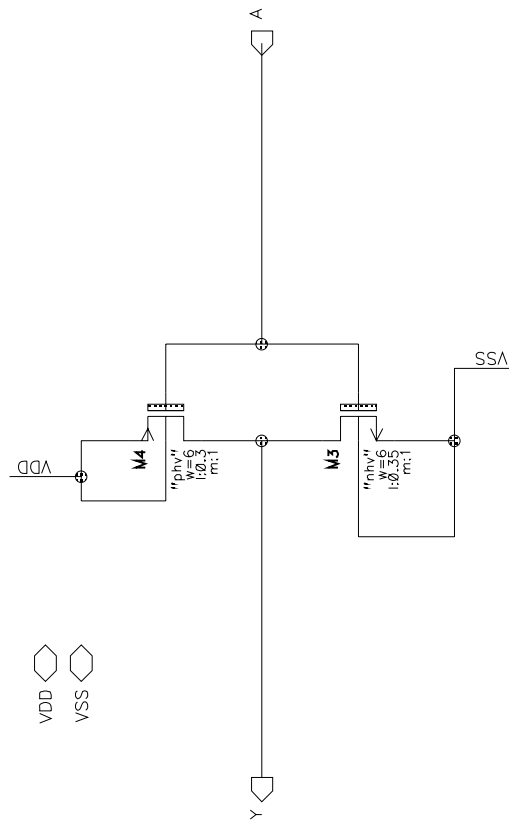


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3
Last QA Review	
Last Changed	Sep 28 11:42:15 2006

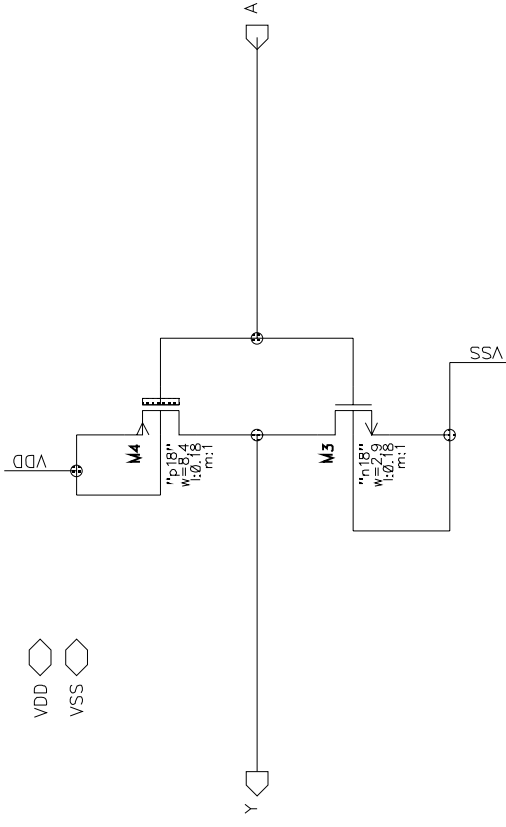


Cell variant for layout ".lay1"  
 =====  
 NMOS width increased from 2.2 to 2.3

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3.lay1
Last QA Review	
Last Changed	Jan 10 14:27:47 2007



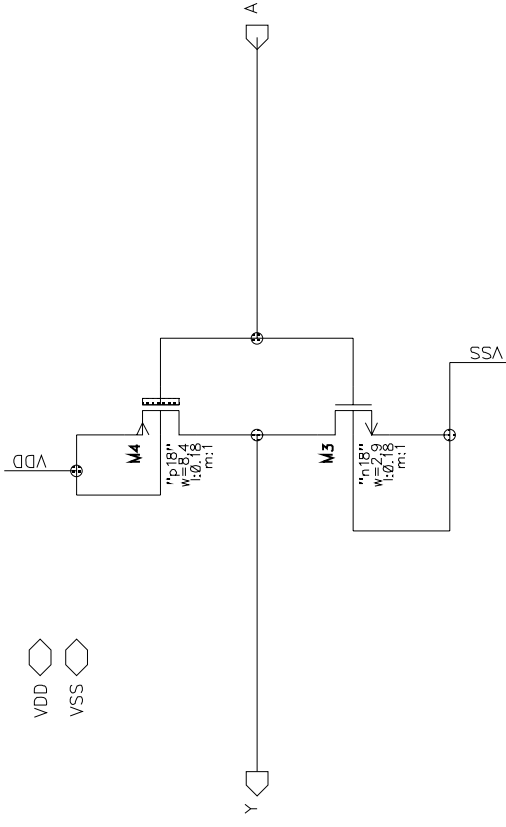
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3_hv
Last QA Review	
Last Changed	Sep 29 15:18:48 2006



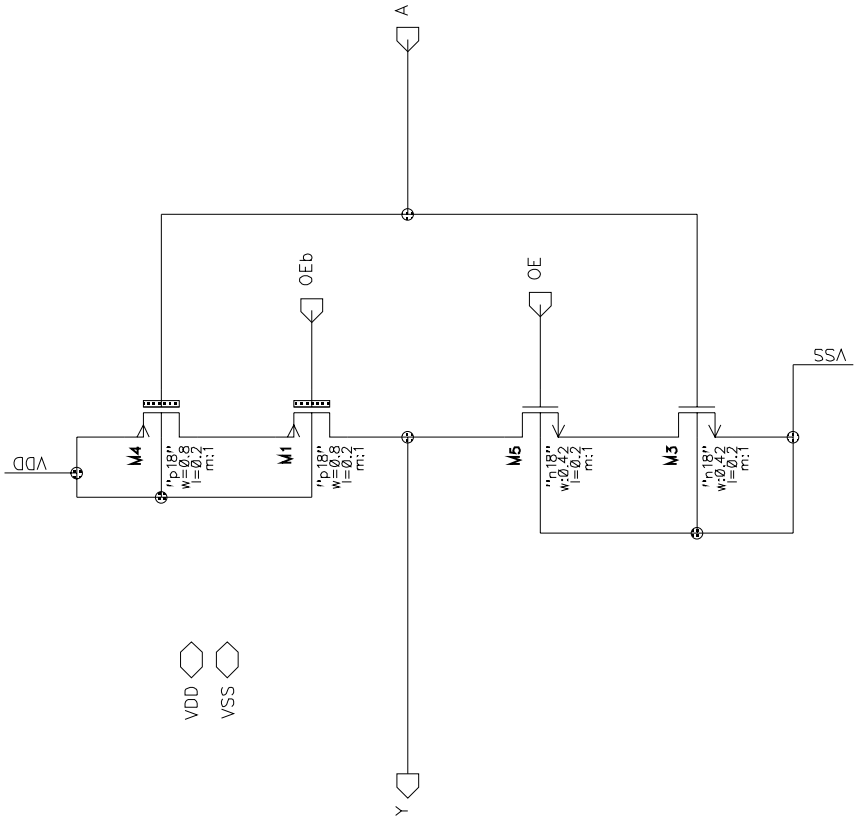
### RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x4
Last QA Review	
Last Changed	Sep 28 11:42:24 2006

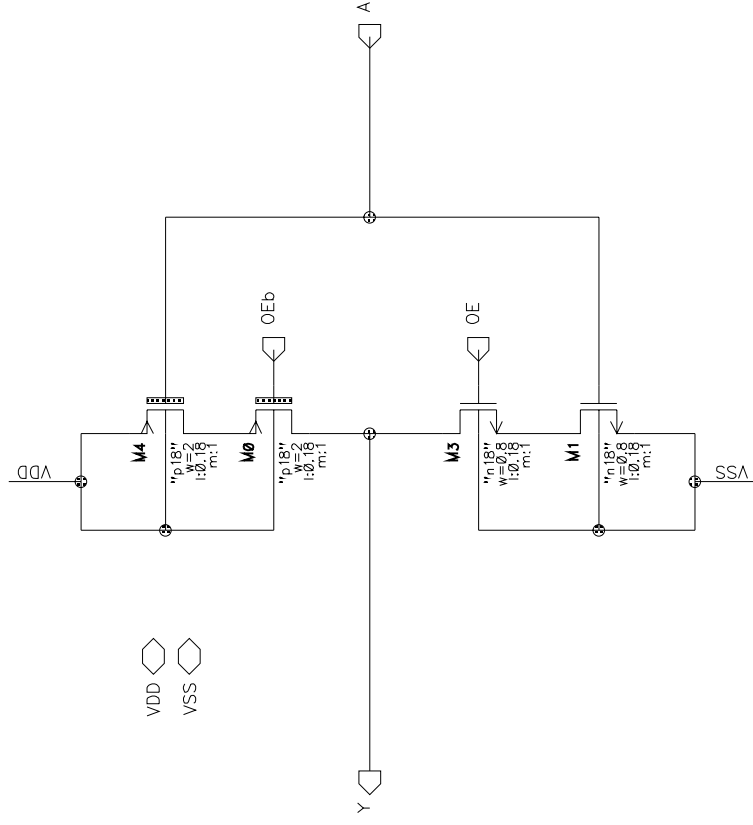




RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x4.lay3
Last QA Review	
Last Changed	Sep 28 11:42:24 2006

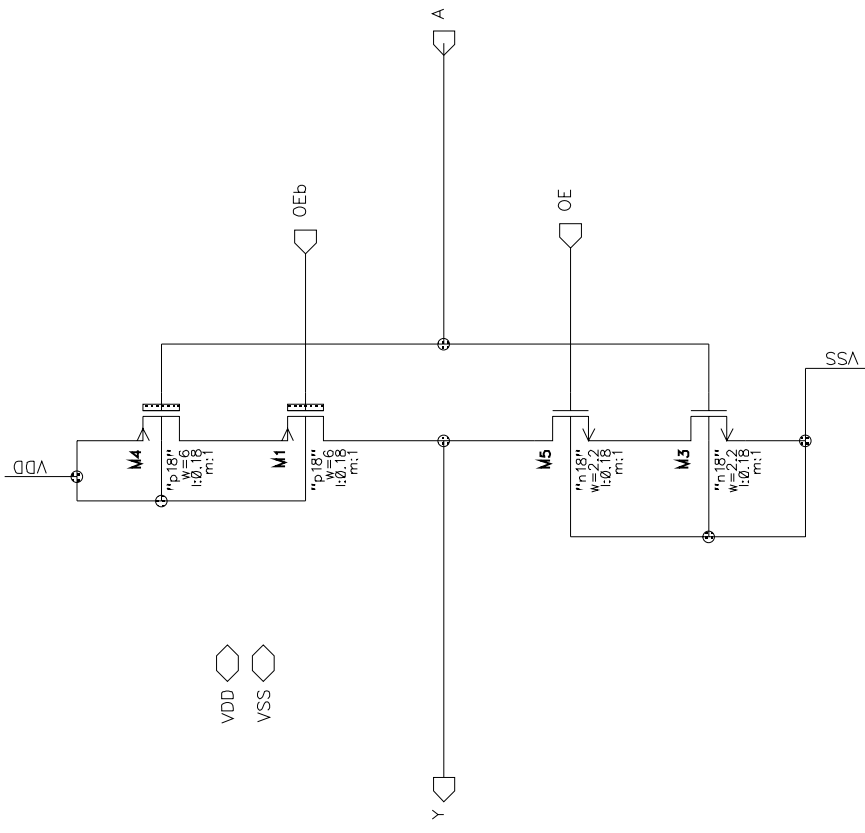


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x0c
Last QA Review	
Last Changed	Feb 12 18:49:59 2007

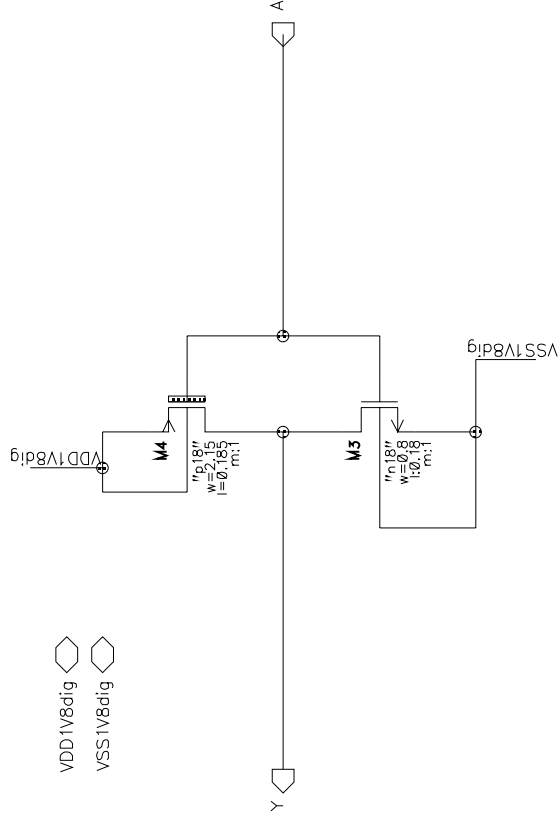


### RAL Microelectronics Group

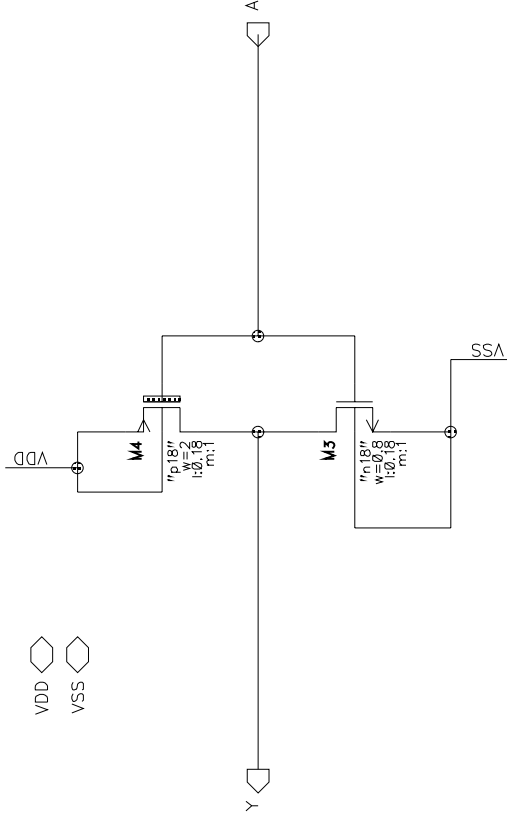
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x1
Last QA Review	
Last Changed	Sep 28 11:42:37 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x3
Last QA Review	
Last Changed	Jan 22 10:54:26 2007

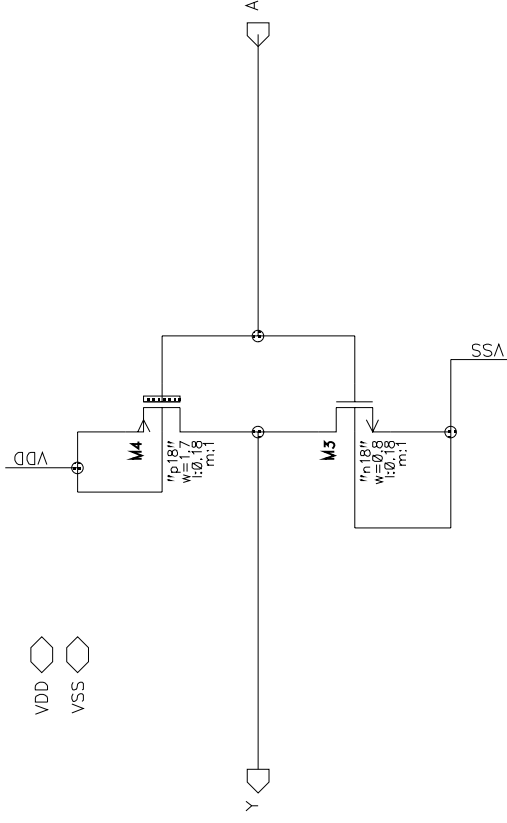


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Feb 5 17:55:09 2007

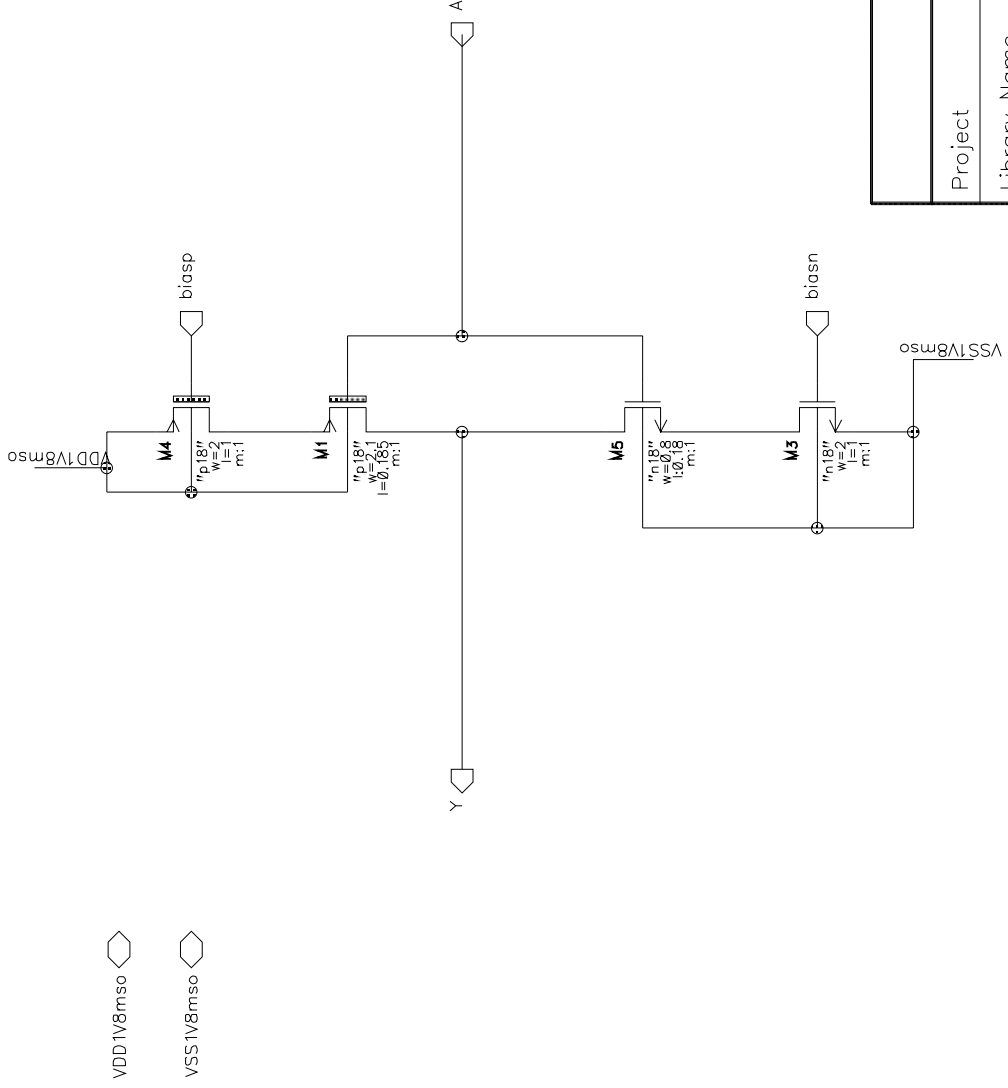


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Mar 12 17:30:10 2007

PMOS width reduced from 2um to 1.7um  
to aid efficient SRAM layout



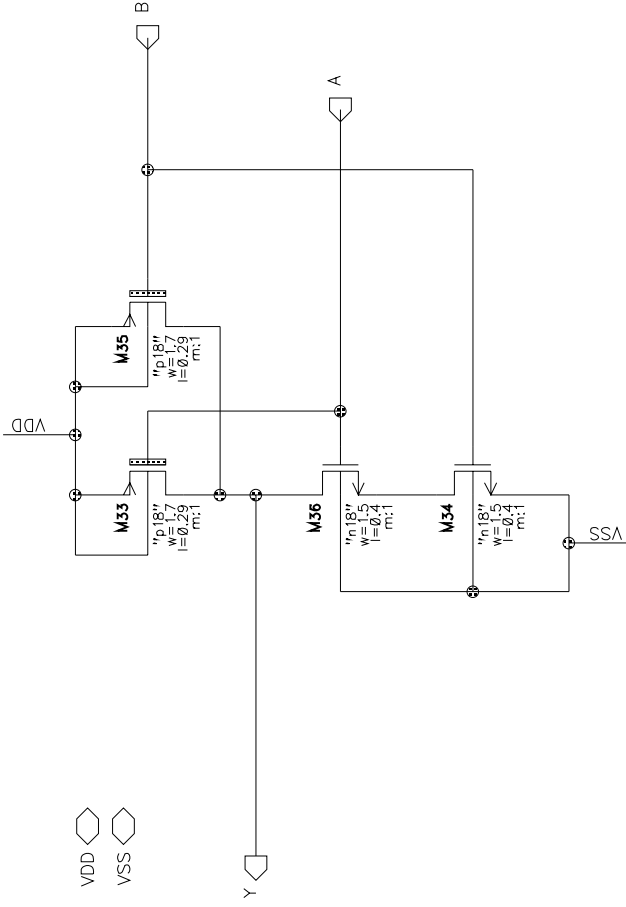
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1lay1
Last QA Review	
Last Changed	Mar 8 17:41:16 2007



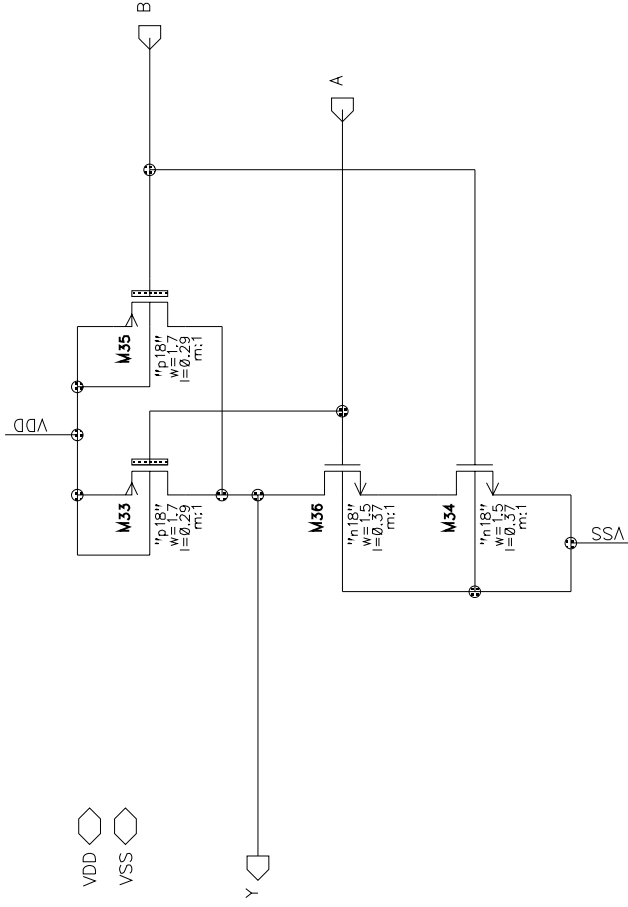
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1lim
Last QA Review	
Last Changed	Mar 8 17:45:02 2007







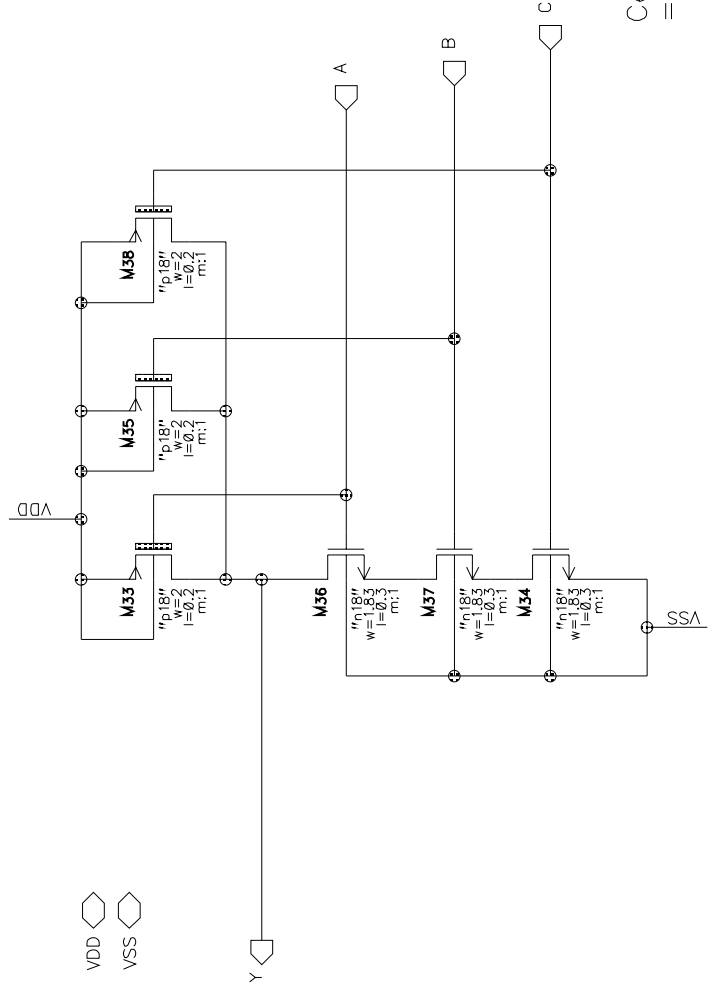
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand2_x0
Last QA Review	
Last Changed	Jan 4 09:07:25 2007



Cell variant for layout ".lay1"

NMOS lengths reduced from 0.4 to 0.37

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand2_x0.lay1
Last QA Review	
Last Changed	Jan 10 14:22:40 2007



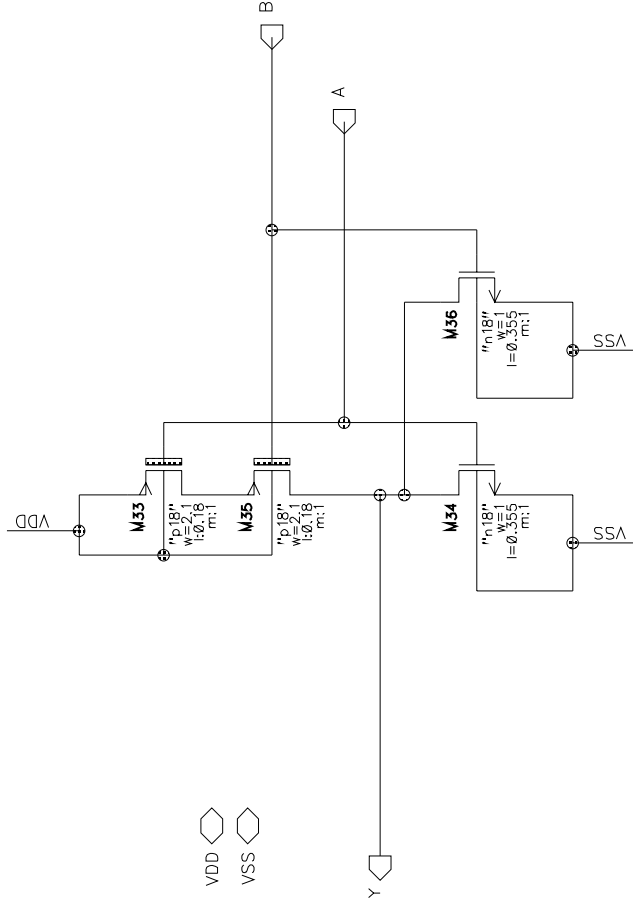
Cell variant for layout ".lay1"  
 =====

NMOS width reduced from 1.9 to 1.83

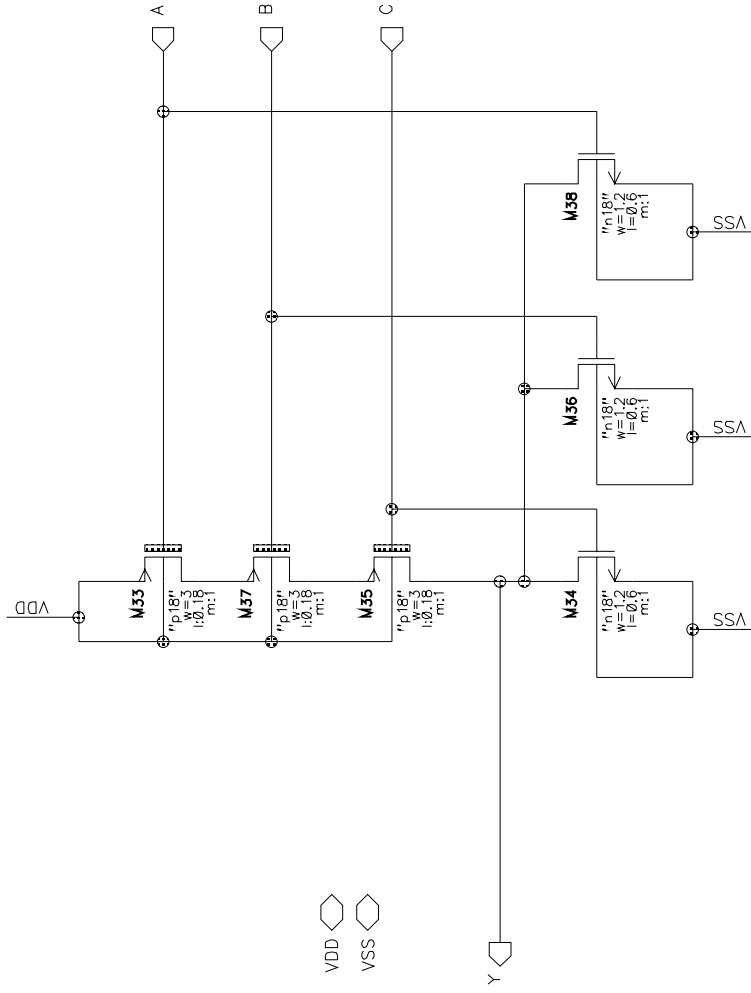
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand3_x0.lay1
Last QA Review	
Last Changed	Jan 10 14:24:41 2007

# Layout variant

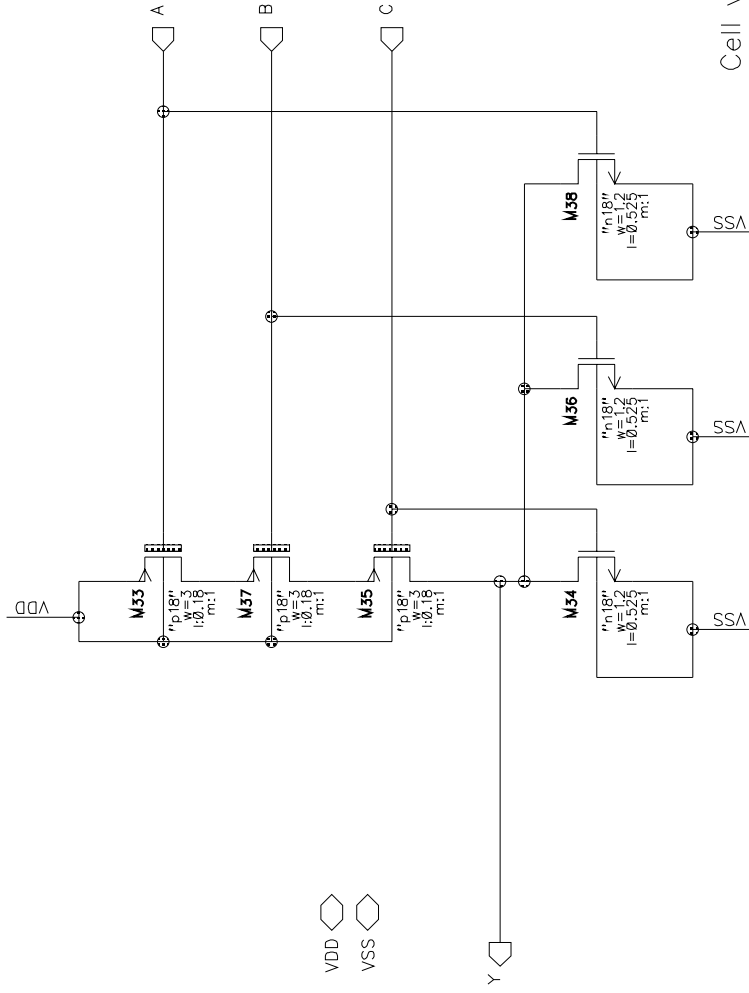
nmos length reduced from 0.4 to 0.355



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor2_x0.lay1
Last QA Review	
Last Changed	Mar 26 11:50:49 2007



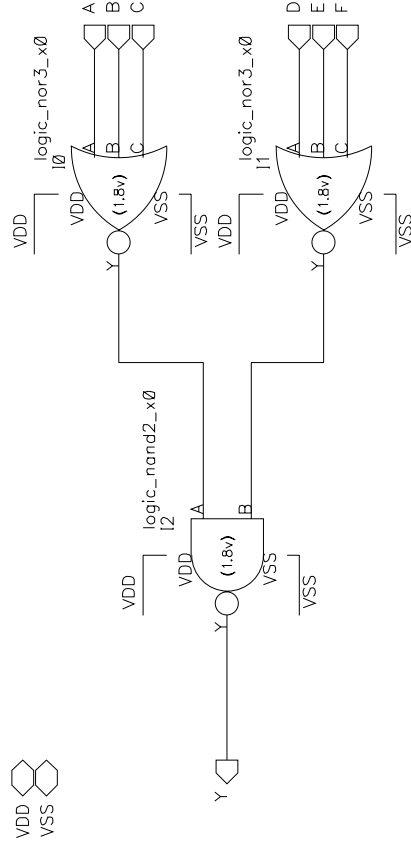
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_x0
Last QA Review	
Last Changed	Jan 10 14:06:59 2007



Cell variant for layout: ".lay1"

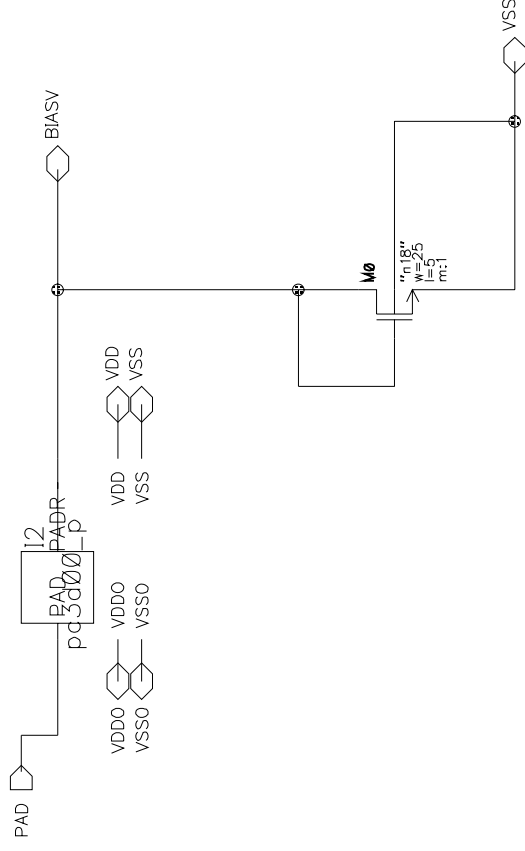
NMOS length reduced from 0.6 to 0.525

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_x0.lay1
Last QA Review	
Last Changed	Jan 10 14:20:51 2007

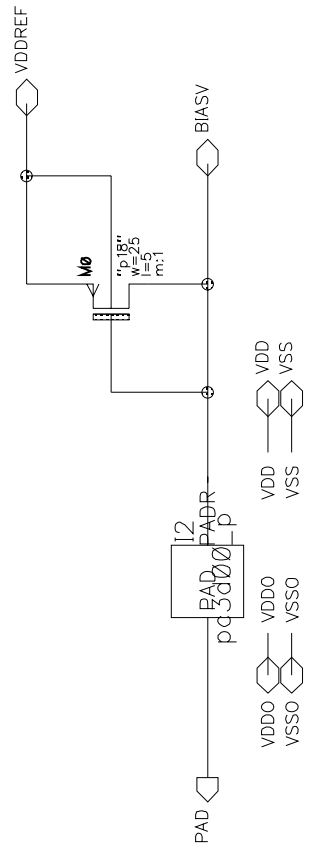


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_or6
Last QA Review	
Last Changed	Apr 19 11:34:27 2007

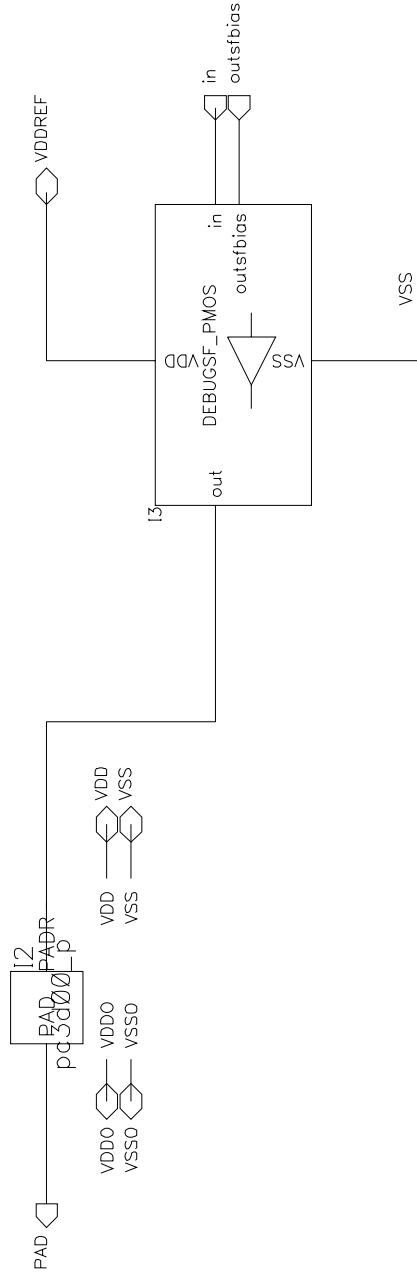




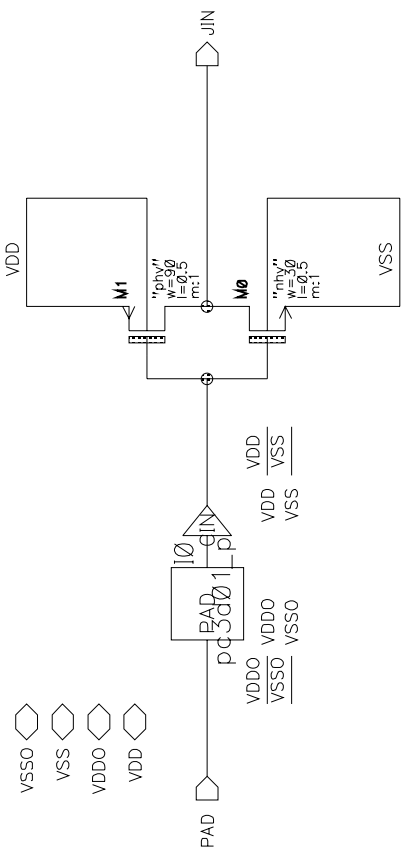
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	ANALG_INPUT_x1_irefNMOS
Last QA Review	
Last Changed	Jun 28 09:07:13 2007



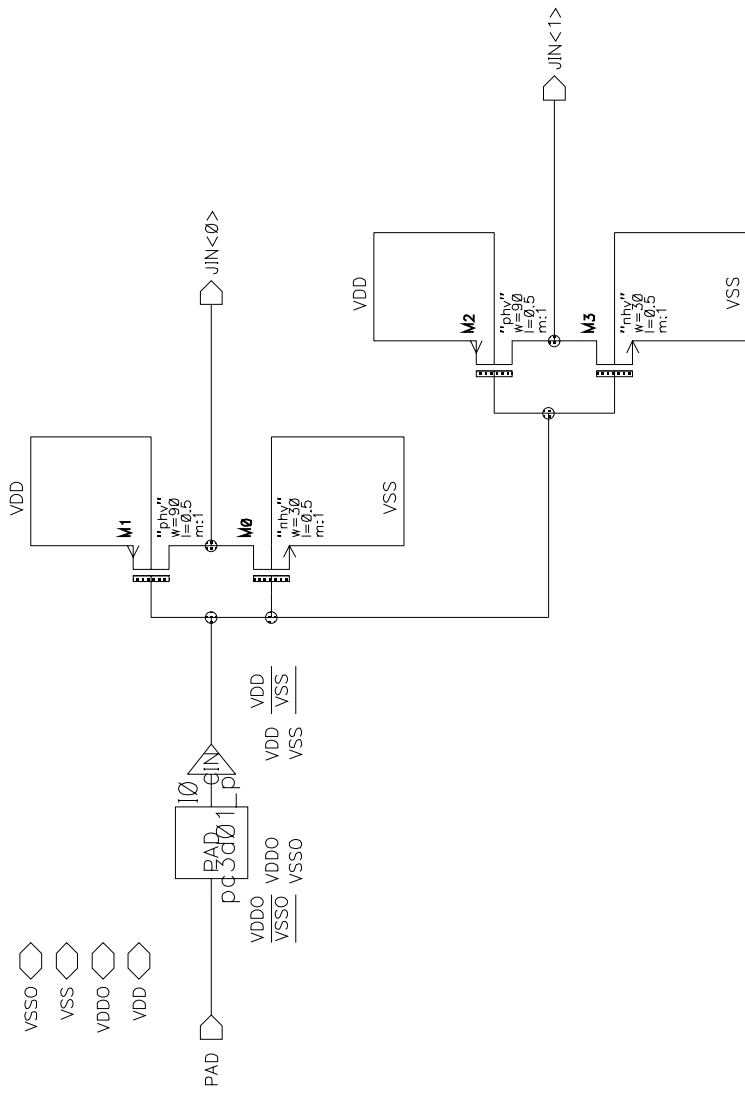
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	ANALG_OUTPUT_x1_irefPMOS
Last QA Review	
Last Changed	Jul 3 13:44:02 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	ANALG_OUTPUT_x1_PMOSsf
Last QA Review	
Last Changed	Jul 3 13:43:00 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	DIGITAL_INPUT_JCbigbuf
Last QA Review	
Last Changed	Jul 3 13:44:55 2007



RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	DIGITAL_INPUT_JCdbibuf
Last QA Review	
Last Changed	Jul 3 13:45:04 2007