Tera-Pixel APS for CALICE

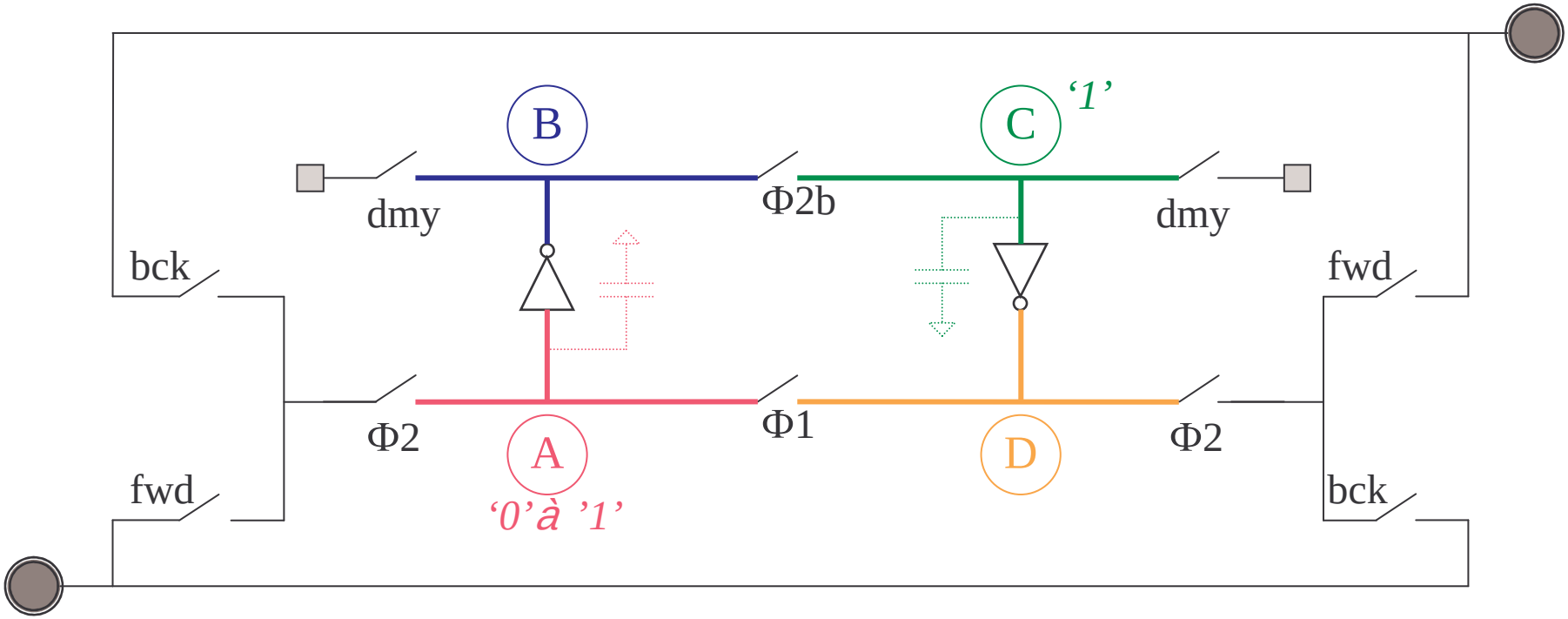
Progress Meeting 6th September 2006

Main Activities

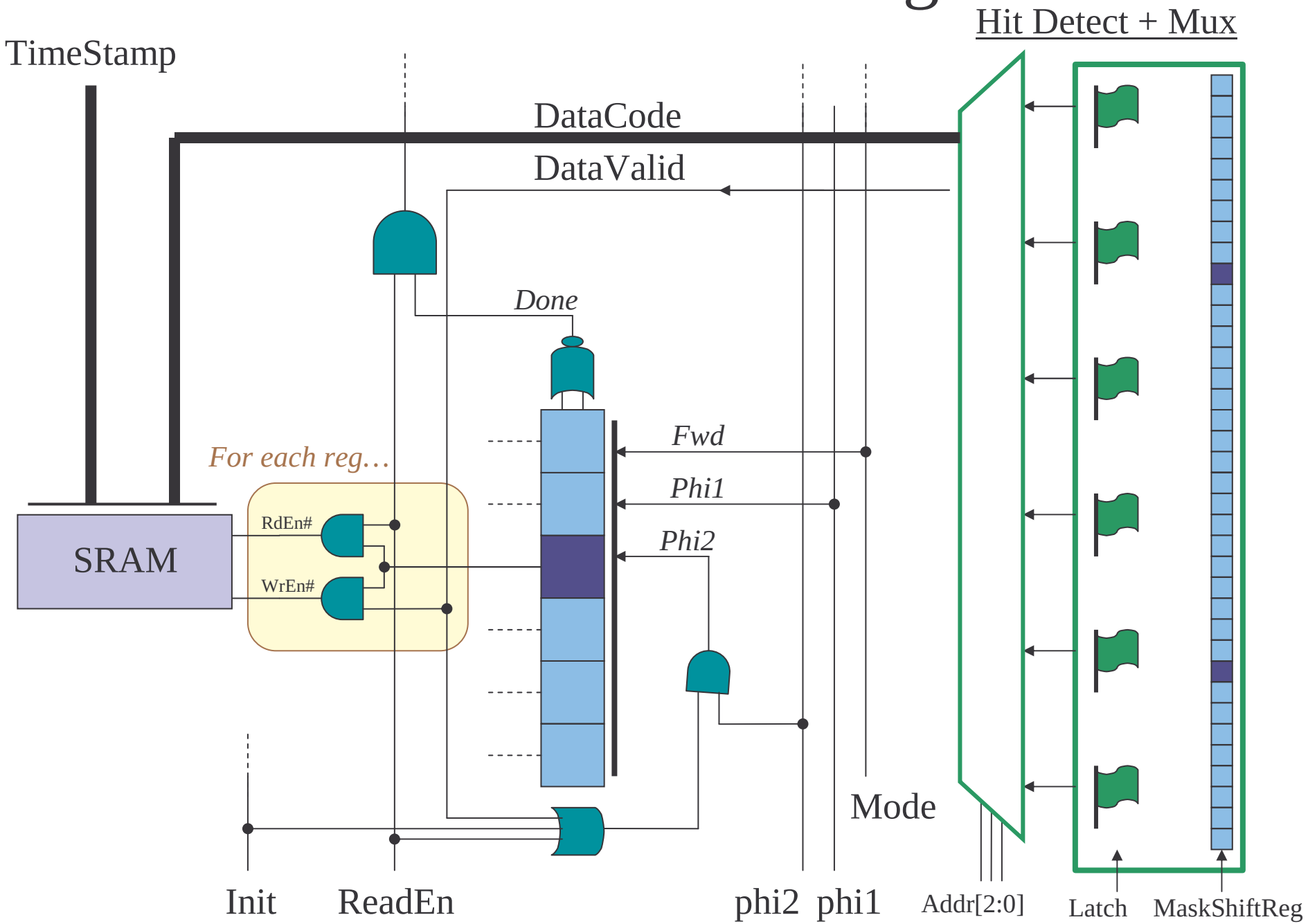
- Meeting with Foundry B
- Tender for 0.18 micron fabrication
- Phone meeting with Foundry D
- [JC] Digital logic design & simulations
- [RT] New analog pixel circuits
- Meeting with Guilio, Mike, Marcel & Konstantin

This presentation

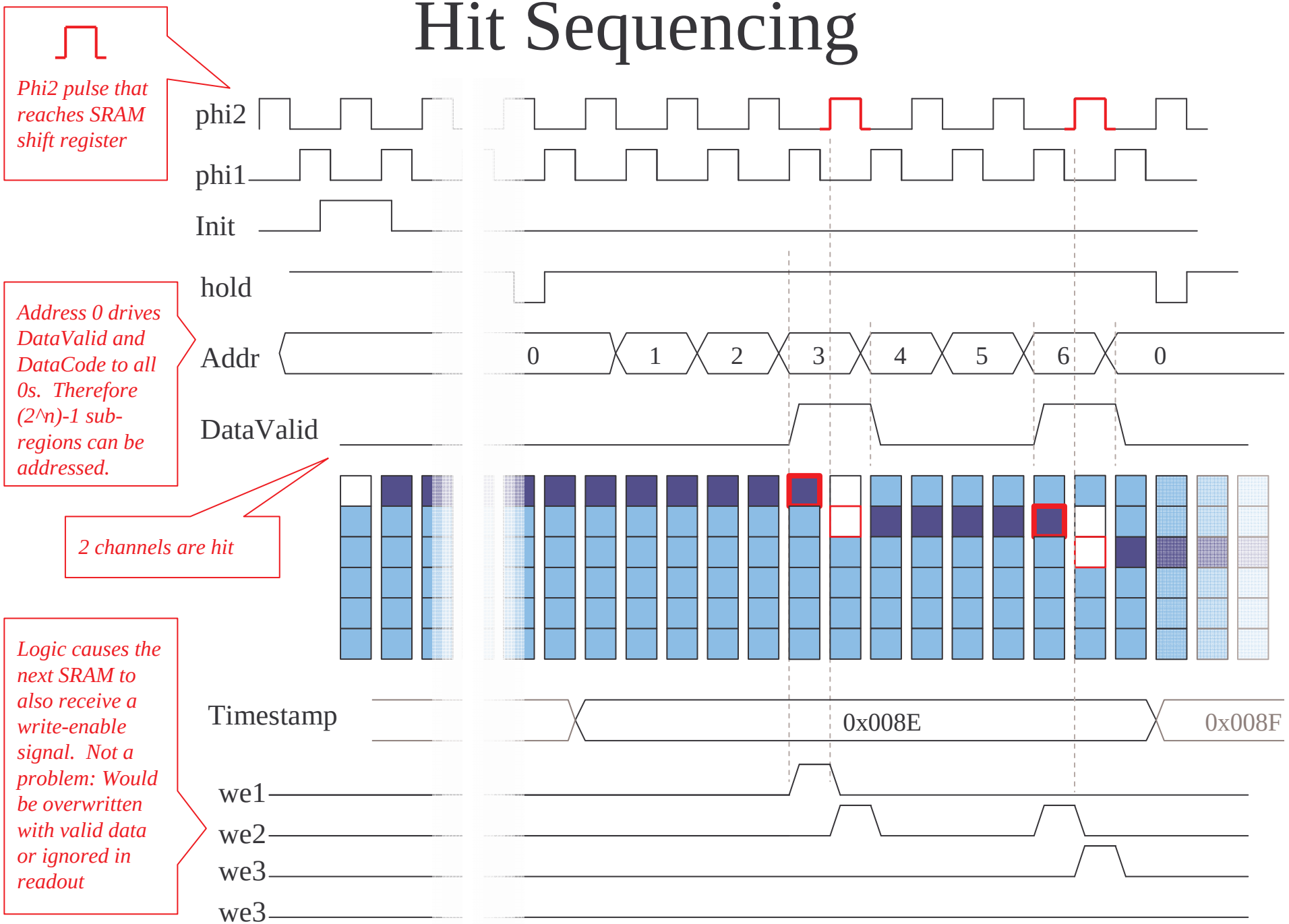
Bidirectional SRAM Shift-Register Cell



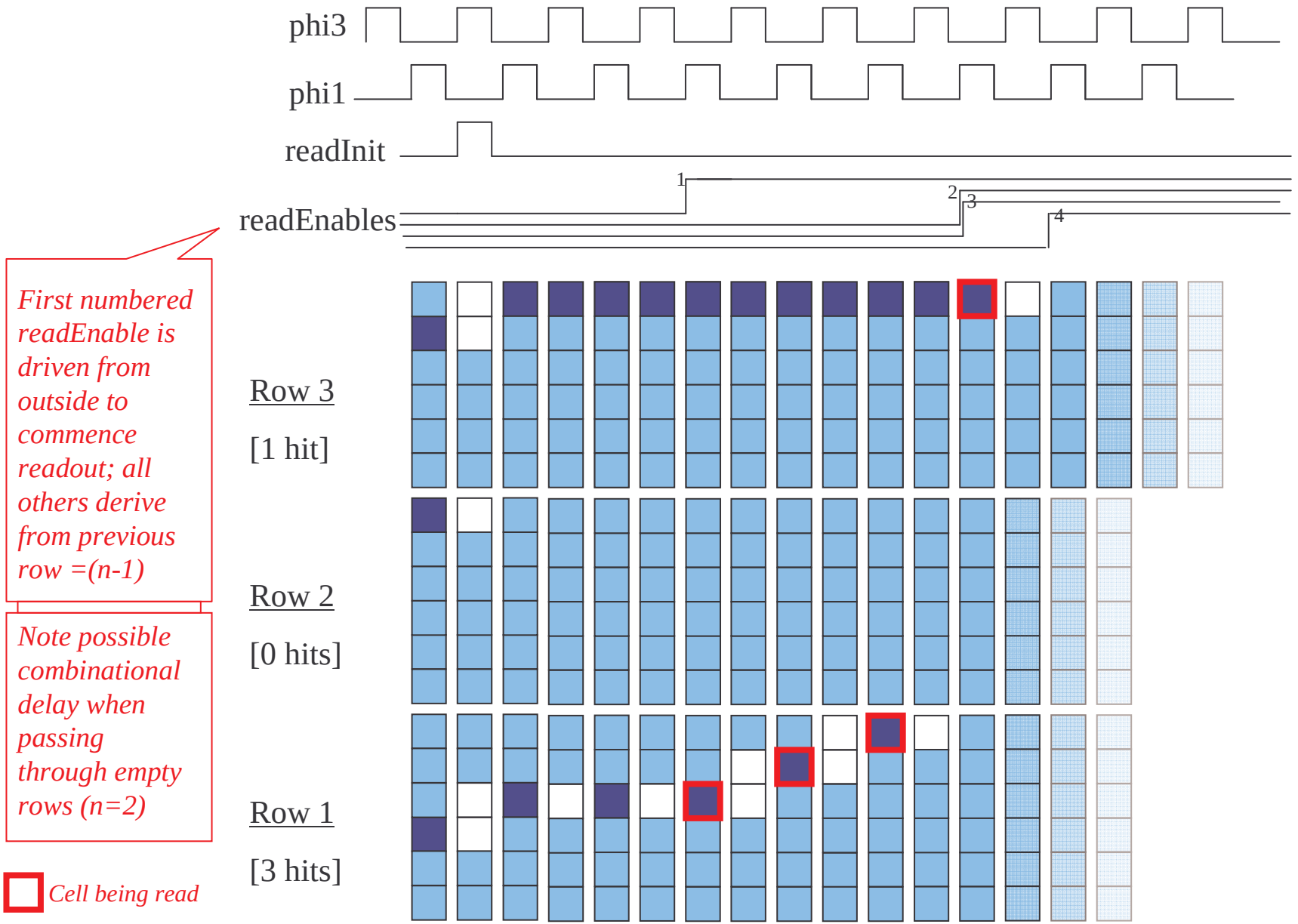
Consolidated Hit Logic



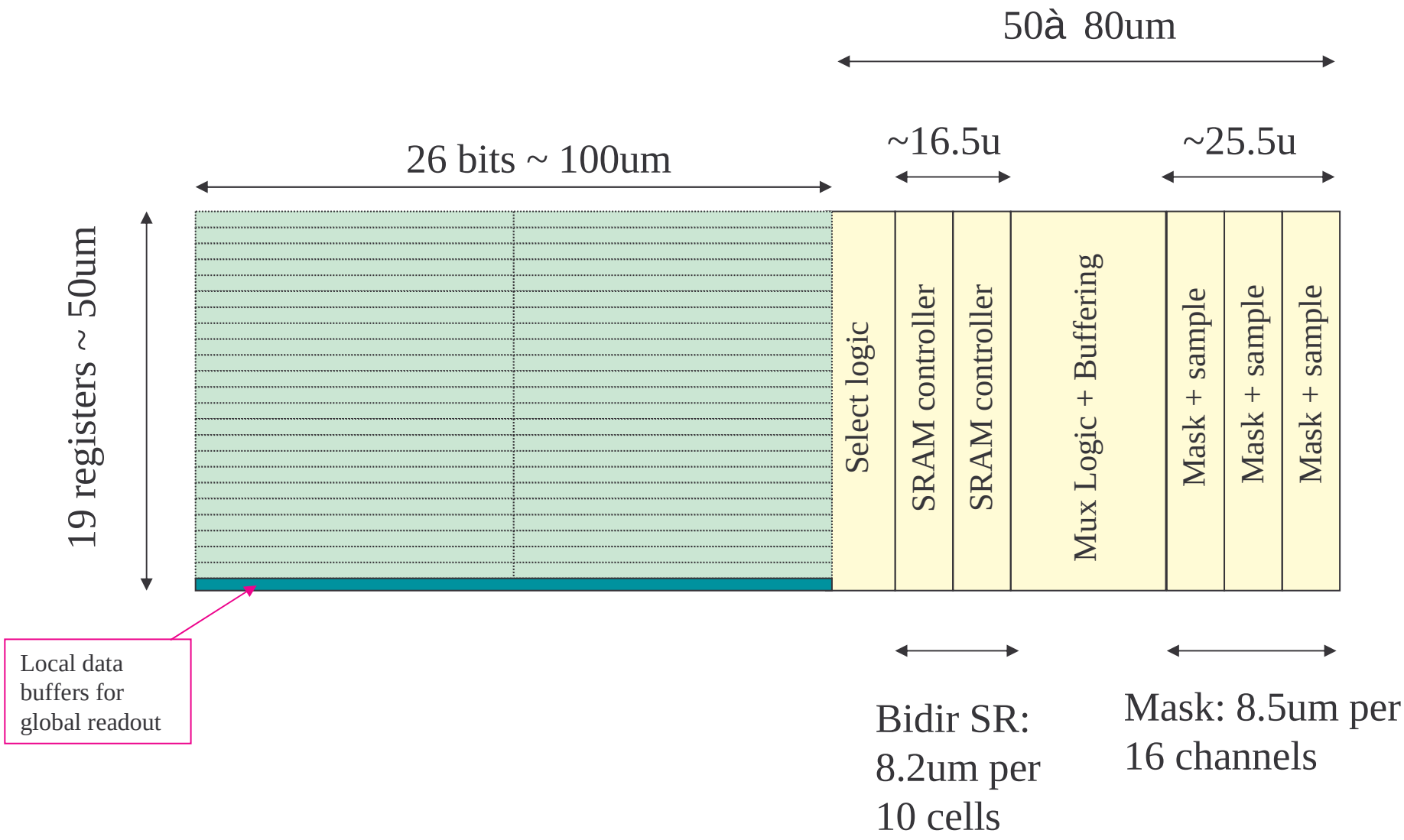
Hit Sequencing



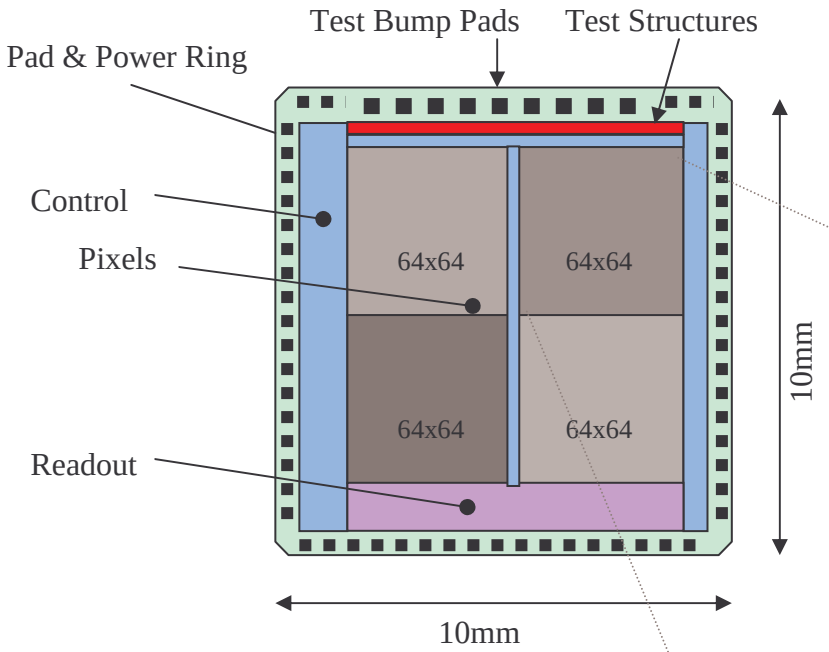
Readout Sequencing

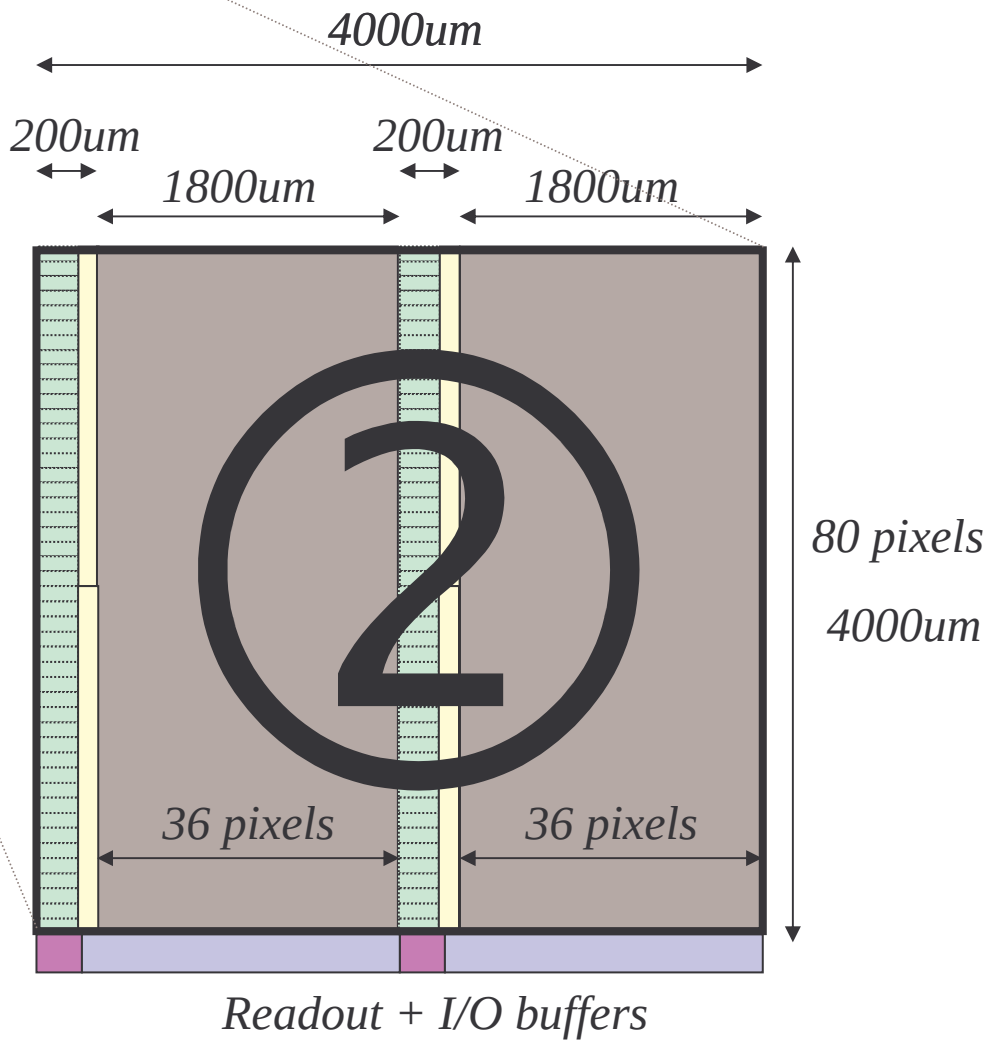


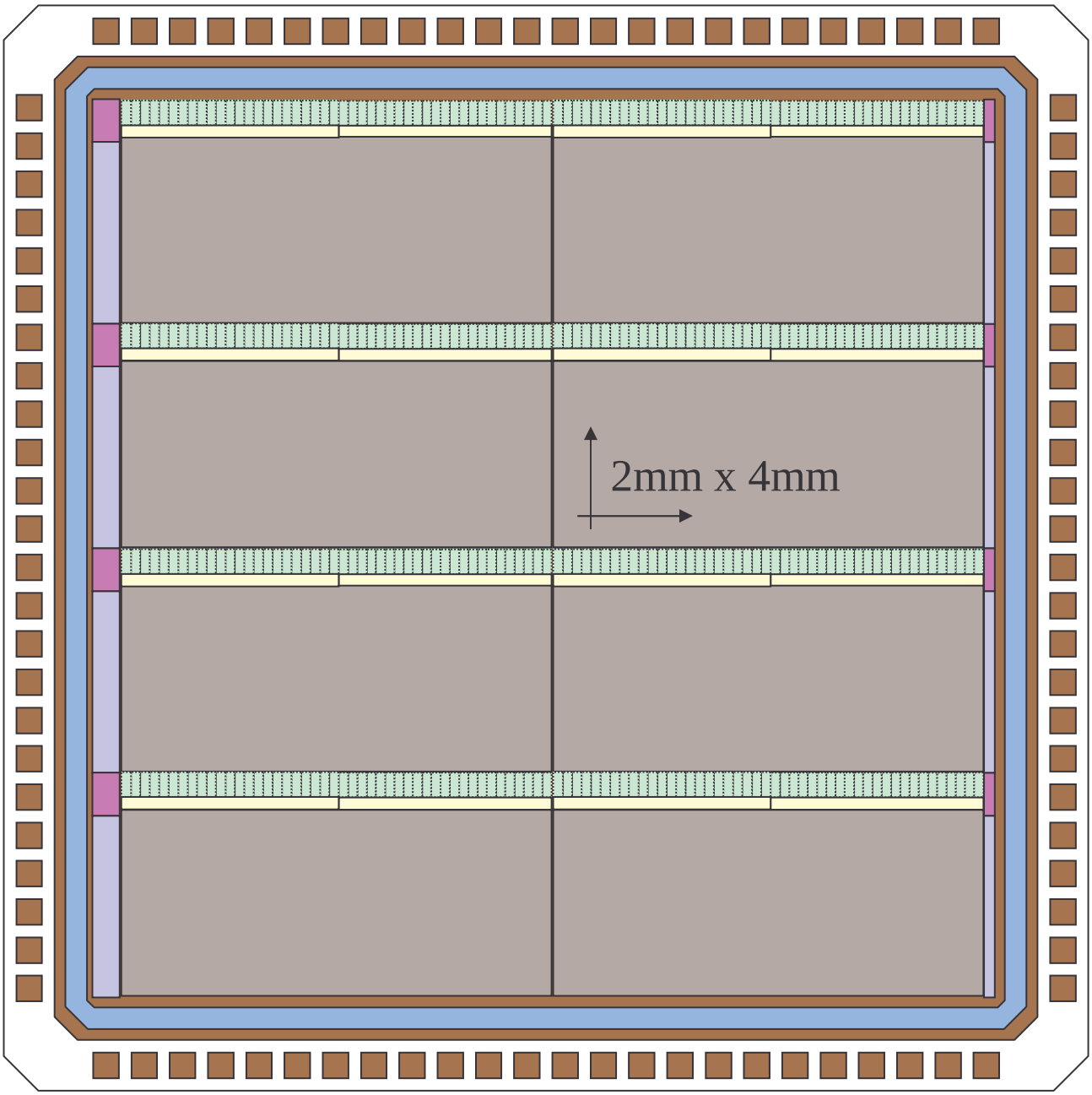
Area Estimates



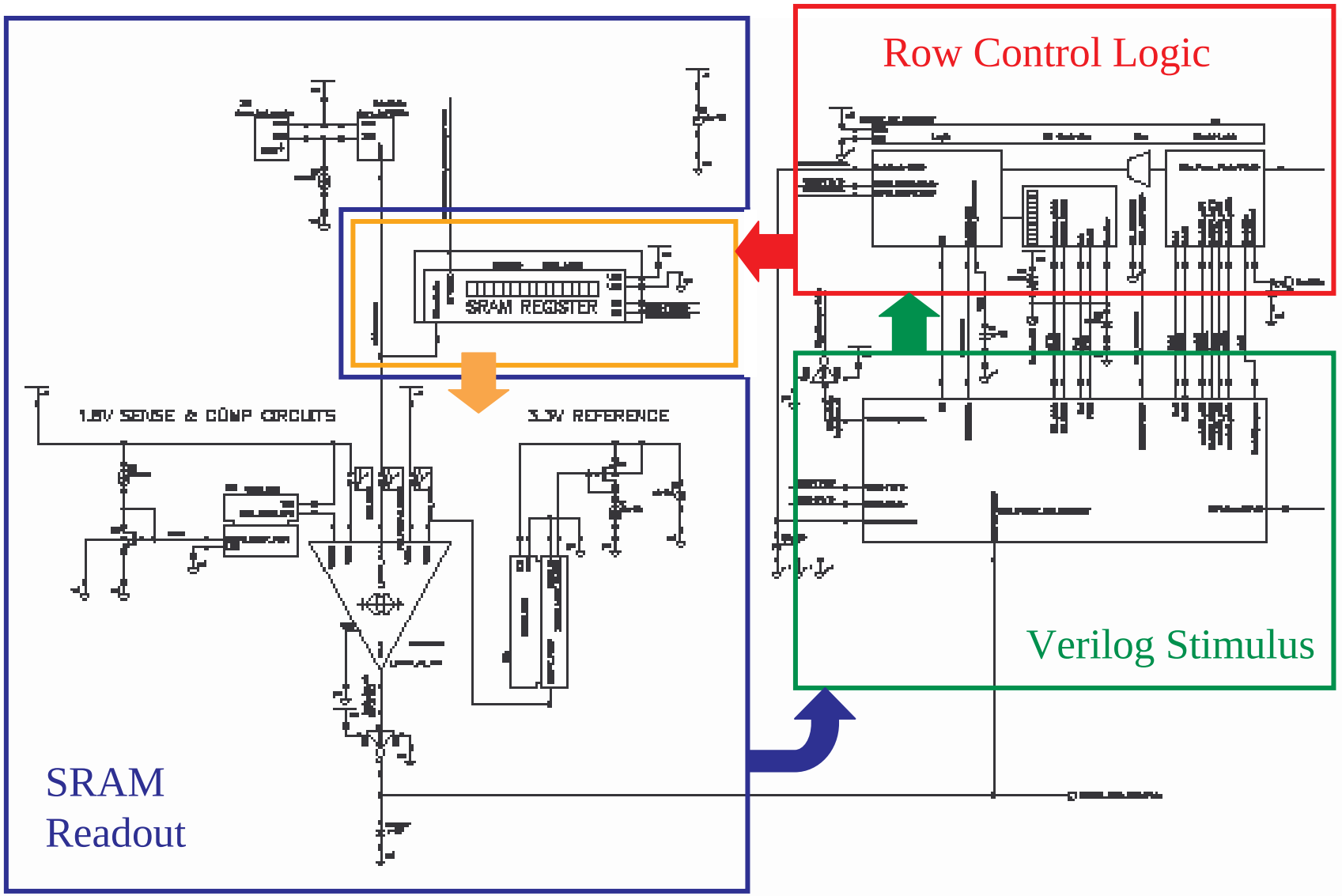
Layout Example

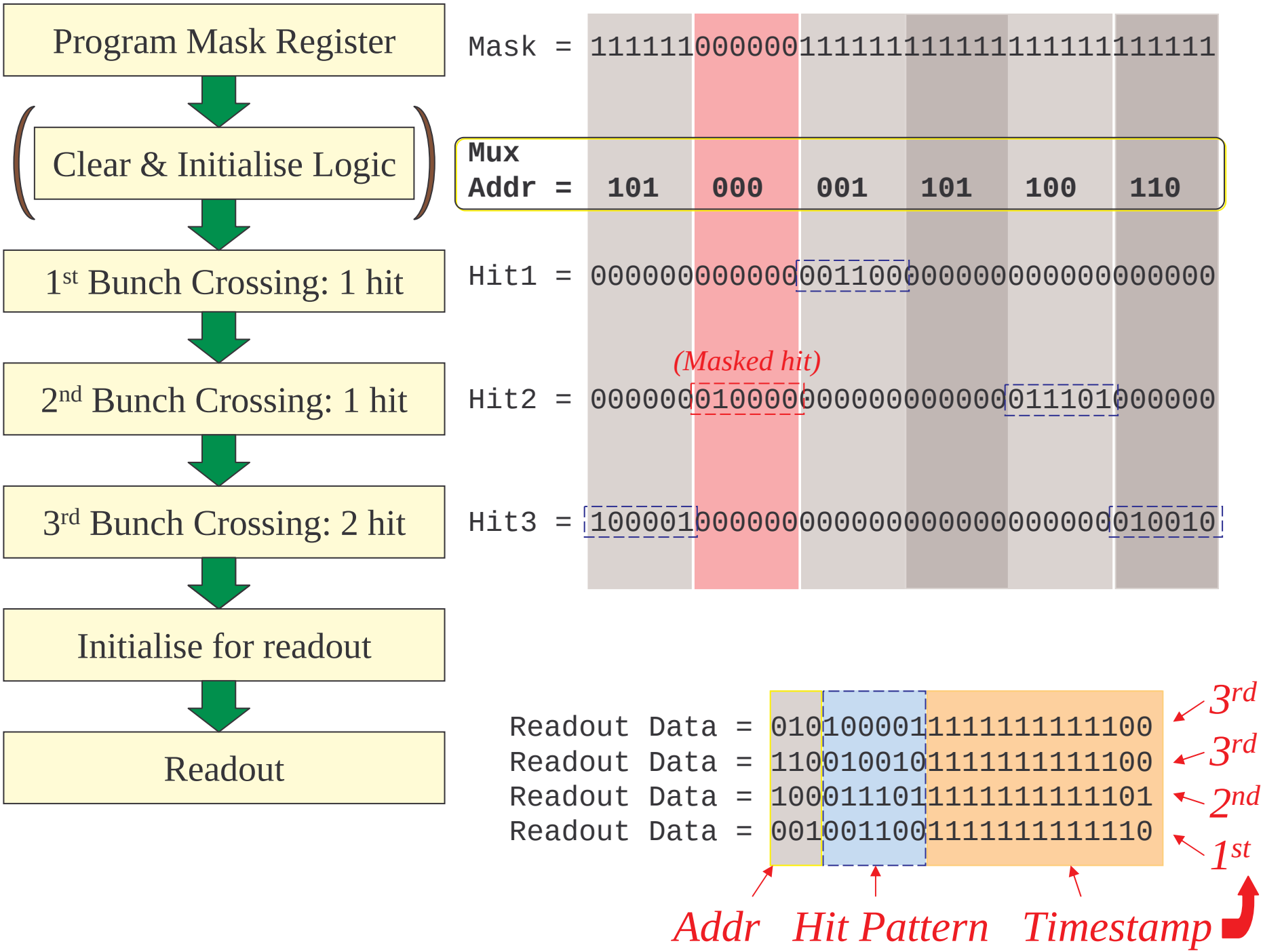


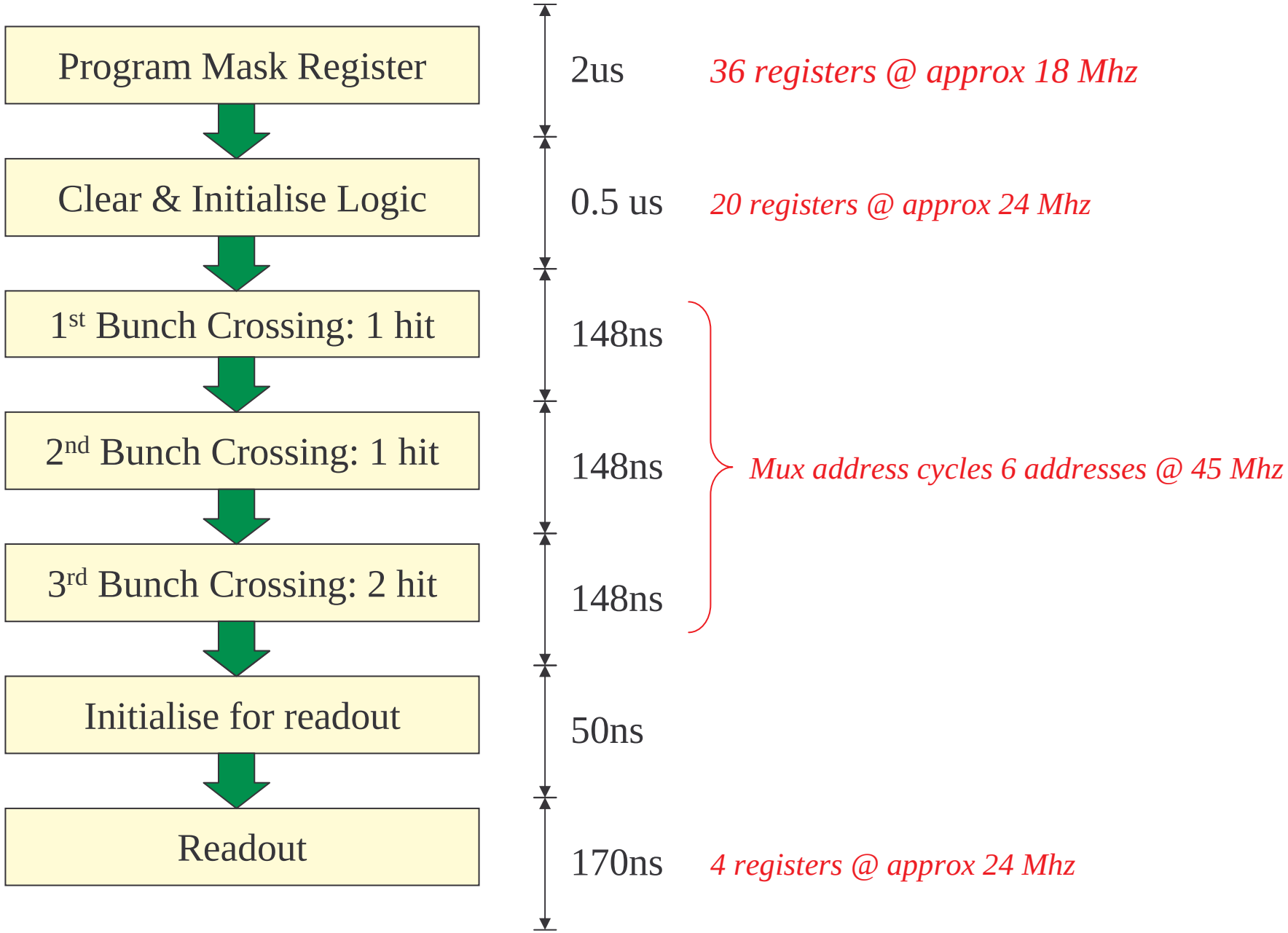



2mm x 4mm

Logic Simulation




Program Mask Register
Clear & Initialise Logic
1st Bunch Crossing: 1 hit
2nd Bunch Crossing: 1 hit
3rd Bunch Crossing: 2 hit
Initialise for readout
Readout
Mask = 111111000000111111111111111111111111
Mux Addr = 101 000 001 101 100 110
Hit1 = 000000000000001100000000000000000000
(Masked hit)
Hit2 = 000000010000000000000000011101000000
Hit3 = 100001000000000000000000000000010010
Readout Data = 010100001111111111100
Readout Data = 110010010111111111100
Readout Data = 100011101111111111101
Readout Data = 001001100111111111110
3rd
3rd
2nd
1st
Addr
Hit Pattern
Timestamp


Program Mask Register
Clear & Initialise Logic
1st Bunch Crossing: 1 hit
2nd Bunch Crossing: 1 hit
3rd Bunch Crossing: 2 hit
Initialise for readout
Readout
2us
36 registers @ approx 18 Mhz
0.5 us
20 registers @ approx 24 Mhz
148ns
148ns
148ns
Mux address cycles 6 addresses @ 45 Mhz
50ns
170ns
4 registers @ approx 24 Mhz

Questions

- Number of sub-sets of pixels?
  - 6 or 7
- Number of pixels in a sub-set?
  - 6 or 7 or 8

Currently Implemented

36 pixels	= 1800	um
Control logic + SRAM *(19 regs)*	= 200	um
Dead Area	= 10 %	

Question

- Assuming a row must be reset after a hit (real or noise)…
  - This reset is likely to occupy the next bunch crossing, ie lasting 150ns, during which time the N pixels in this row will be ‘blind’ to a subsequent hit (real or noise)
  - Is this acceptable?