Summary/Dialogue

Partial results for the Preamplifier-Shaper pixel design are presented in this document.

This design is found to exhibit unsatisfactory signal-to-noise ratio of approximately 5. (Initial figures quoted around 10 were found to be incorrect, due to the simulator improperly biasing the preamplifier during the noise analysis. Further optimisation of the circuit using correct noise analysis did not further improve on S/N ~ 5 for 250 electrons.)

To achieve this noise performance a large current must flow in the input transistor of the preamplifier, pushing the power consumption of this pixel over 10uW.

The circuit is found to be very sensitive to the capacitance on the input node.

The circuit uses 6 PMOS devices, requiring approximately 25 square microns of unrelated NWELL at 1.8v in each pixel. (Physics simulations so far have assumed 9 square microns).

Despite efforts to reduce mismatches, the monte-carlo simulations still show a signal spread of around 30mV (larger PMOS devices and more current would help to improve this).

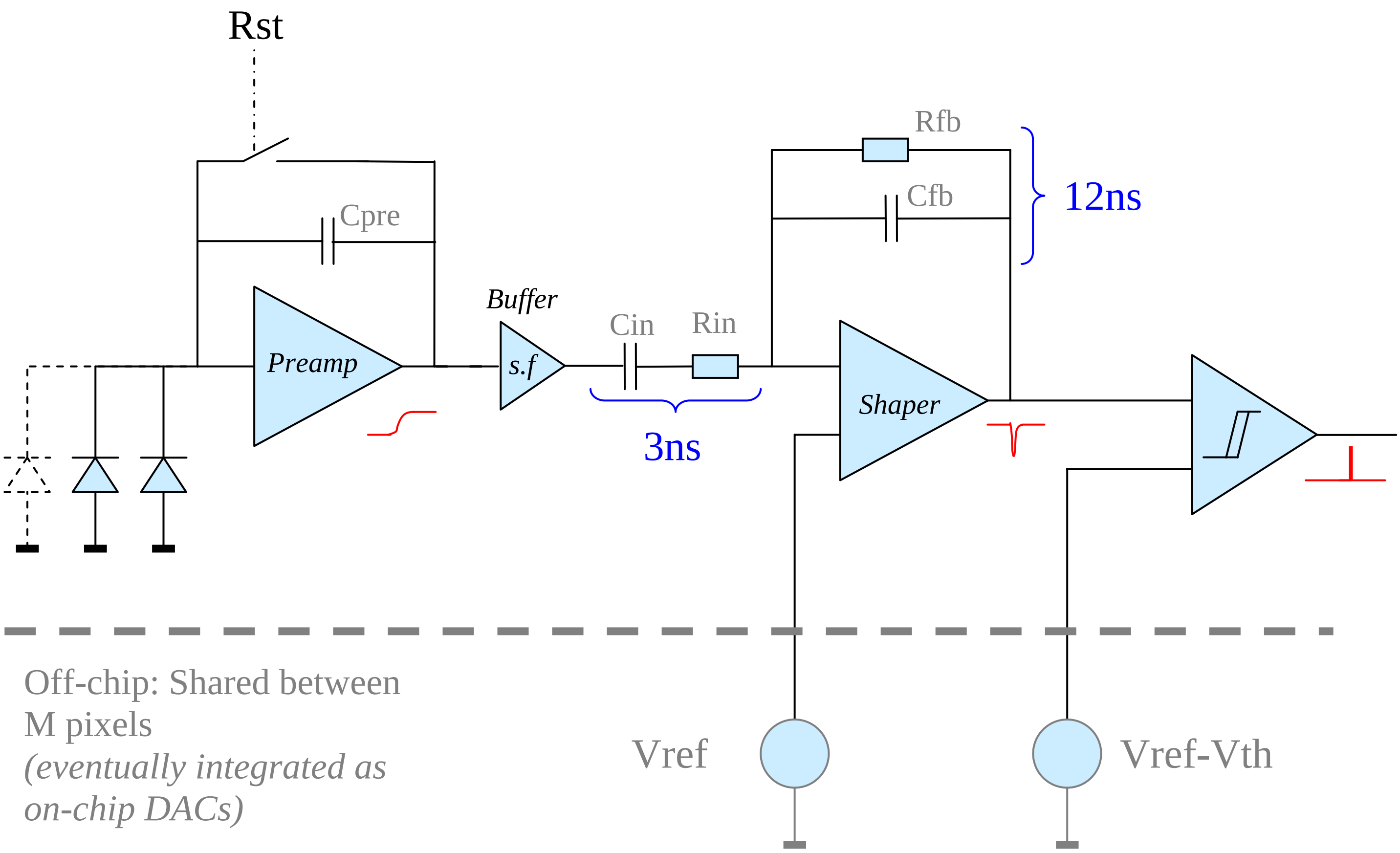
This circuit has been optimised and tweaked to some extent to try to minimise the noise and perform well in process corner and mismatch simulations. Therefore increasing the signal must be considered: The simplest method to increase the signal is to reduce the feedback capacitance of the shaper circuit. At present this capacitor is a metal-metal capacitor of 4fF, already the order of parasitics in the circuit. This could be further reduced by (a) placing two such capacitors in series or (b) drawing metal tracks & spacings to use parasitic/sidewall capacitance alone in the feedback path. Both techniques would increase signal gain, but the matching of such small capacitances is likely to be poor and would require very careful layout.

All results in this document are obtained for 250 electrons (unless otherwise stated), refer to <<<<???>>>>> to estimate the extra signal that would be achieved for greater collected charge.

Note that calculations for signal-to-noise have been based on a signal of 250 electrons, but the diodes used were actually the 1.8 micron size, which should collect more charge. Assuming 400 electrons for these larger diodes, we see the signal-to-noise rise to around 8.7.

- More accurate prediction for parasitic capacitance on the diode node routing would be very useful!

Preshape Pixel Overview



Brief Operating Instructions

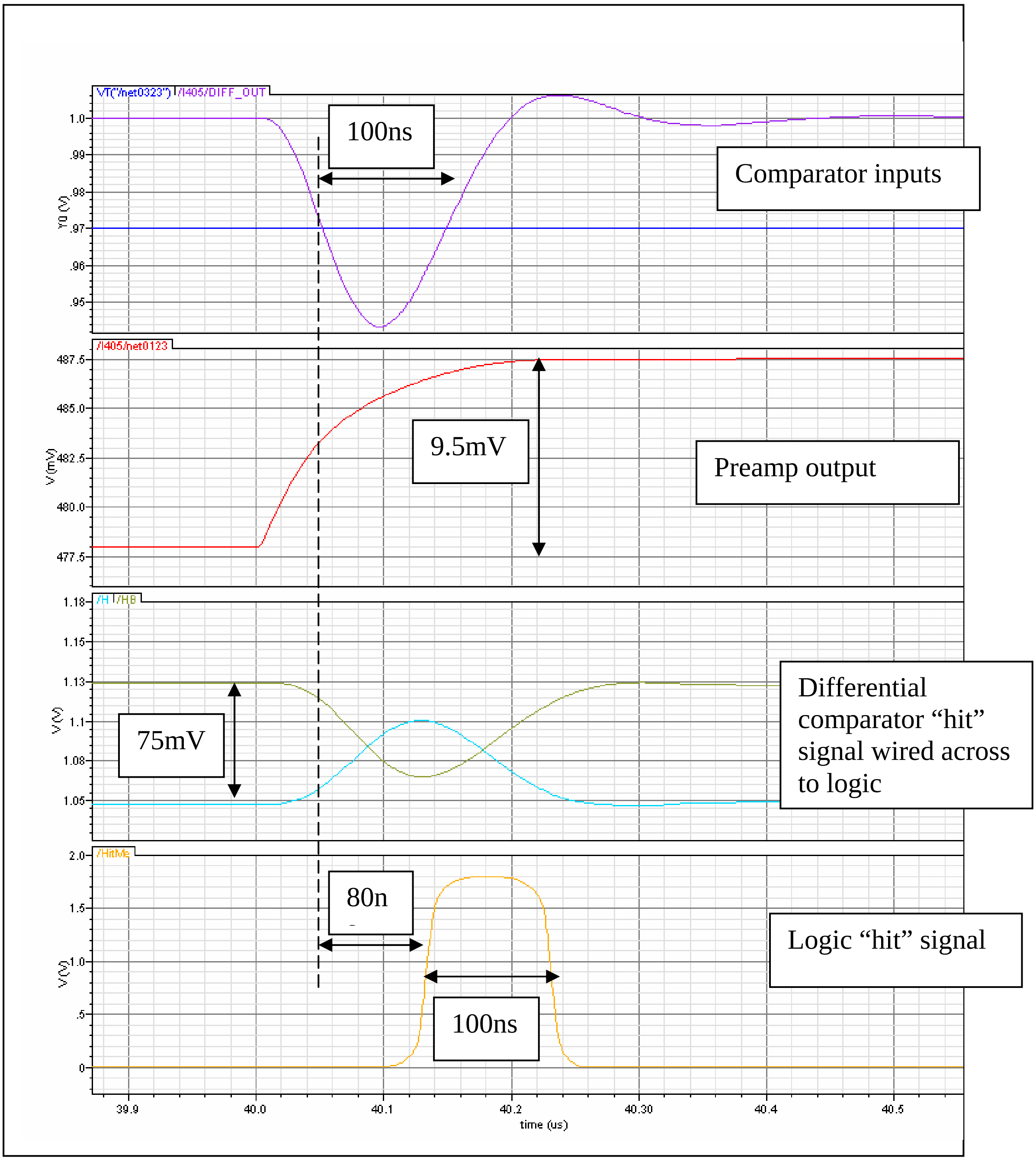
- The preamp must be reset prior to the bunch train. Subsequent hits are seen as steps on the preamplifier output; so there is a maximum charge that can be collected during a bunch train.
- Increasing current in the comparator will reduce the dominant noise source (the input transistor)
- Decreasing Cpre would improve the signal magnitude
- Source-follower current should be adjusted to ensure enough drive-strength is available for the desired speed (pulse width) of the shaper circuit
- More current in the shaper will achieve a faster pulse
- Current in the comparator should be adjusted to achieve the necessary rise/fall time depending on the parasitic capacitance of the “Hit” lines that route from each pixel to the local control logic.

PreShape Pixel simulation: Example Operation

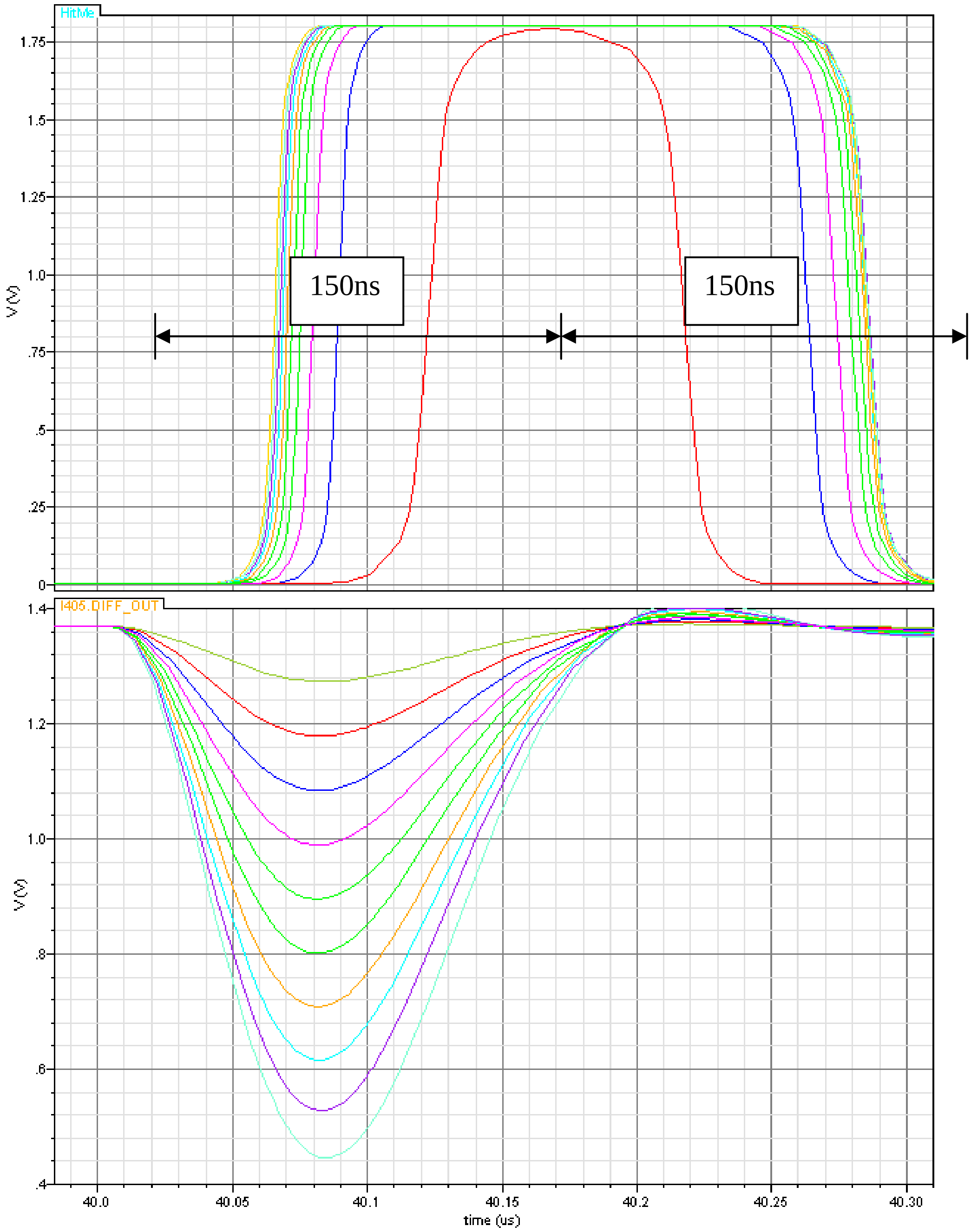
Circuit stimulus/scenario

Basic operation of the pixel circuits is demonstrated:

Results waveforms



Above: Pixel waveforms after the various stages, from MIP hit to logic "hit" decision.



Above: Range of signal sizes (1→10 MIP) for the 180ns case. Sampling every at 150ns intervals it is possible to determine a 10MIP hit followed by a non-hit.

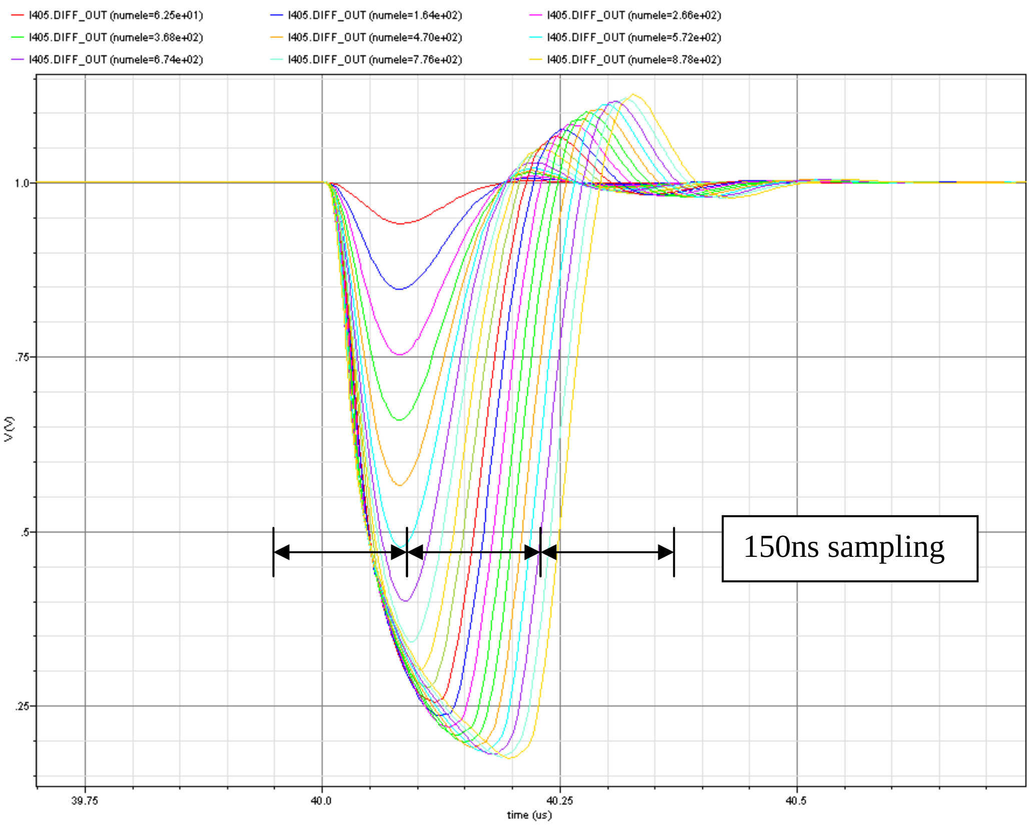
PreShape Pixel simulation: Power consumption

Preamp	Source Follower	Shaper	Comparator (in-pixel)	Comparator (off-pixel)
1.8v	1.8v	1.8v	1.8v	1.8v
3uA	1.1uA	1.7uA	0.5uA	0.3uA
5.4uW	2uW	3uW	0.9uW	0.5uW

Total power consumption = 11.8uW

PreShape Pixel simulation: Maximum signal

Input signals from 250 → 8000 electrons were simulated to check circuit performance in events of larger magnitude. The circuit is linear up to 10 MIPs (625e), after which saturation in the shaper circuit tends to elongate and distort the pulse shape. This ultimately lengthens the time-over-threshold which would cause a double hit.

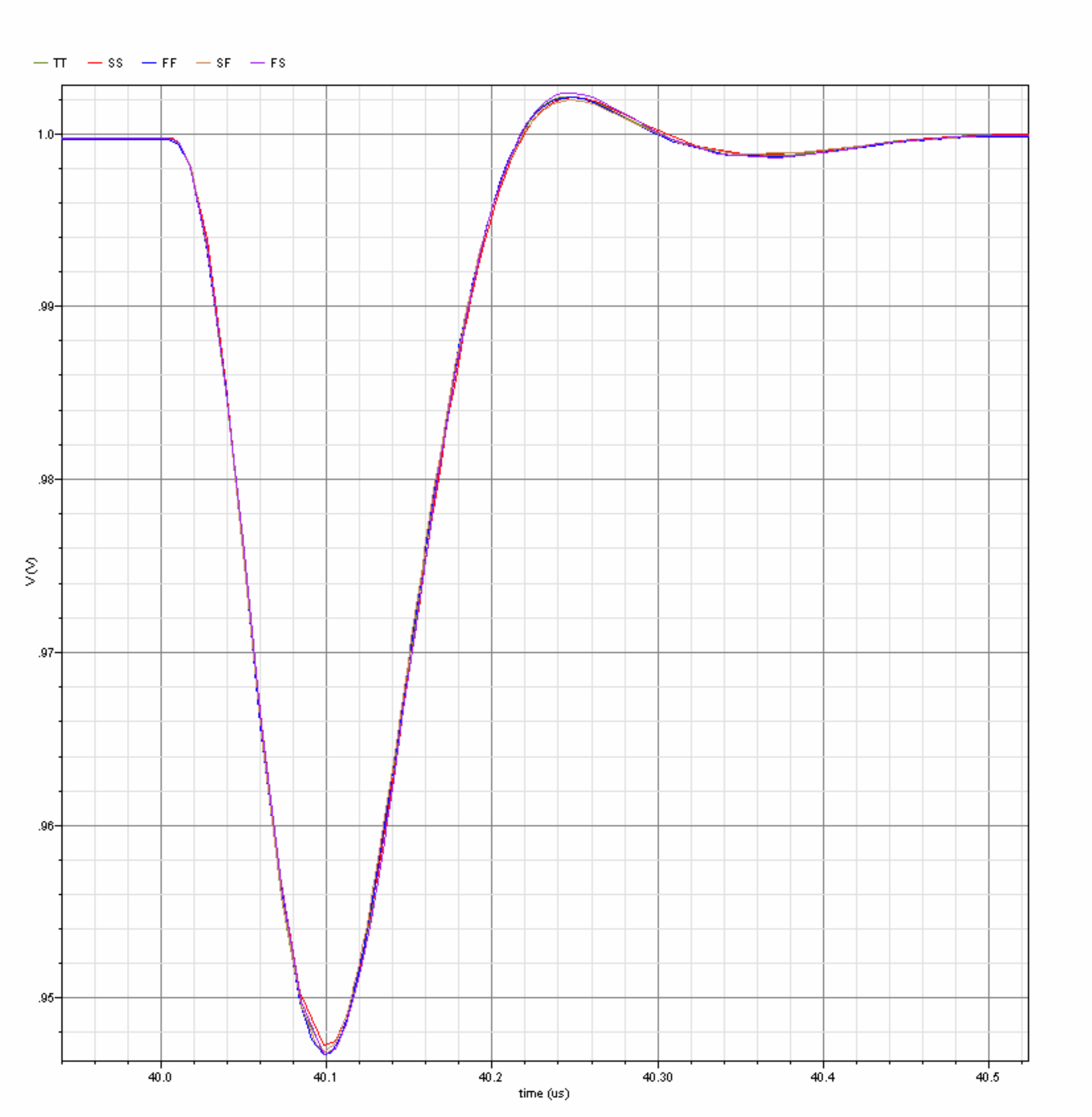


PreShape Pixel simulation: Process corner variations

Circuit stimulus/scenario

Transistor process corners are explored: 1 MIP signal (250 electrons).

Results waveforms



Above: Pulse height for the five process corners is very consistent. (Note that device corners exclude variations to feedback components, ie resistors and capacitors).

	SS	SF	TT	FS	FF
Noise (rms)	11.1mV	11.2mV	11.2mV	11.1mV	11.0mV

Above: Noise at the output of the shaper is consistent in all process corners.

PreShape Pixel simulation: Noise Analysis

Circuit stimulus/scenario

Standard noise analysis is shown to illustrate the dominant noise sources in the circuit. Noise is measured at the shaper output / input to comparator.

Results

```
/I405/M0     id      0.00767987            48.39
/I405/M0     fn      0.00324738            8.65
/I405/M12    id      0.00309899            7.88
/I405/M11    id      0.0030648             7.71
/I405/M10    id      0.00223246            4.09
/I408/M36    id      0.00223143            4.09
/I405/M2     id      0.00206746            3.51
/I405/M4     id      0.00178967            2.63
/I405/M20    id      0.00169626            2.36
/I405/M14    id      0.00159223            2.08
/I405/M19    id      0.00132508            1.44
/I405/M13    id      0.00118306            1.15
/I405/M42    id      0.00117354            1.13

Integrated Noise Summary (in V) Sorted By Noise
Contributors
Total Output Noise = 0.0110402
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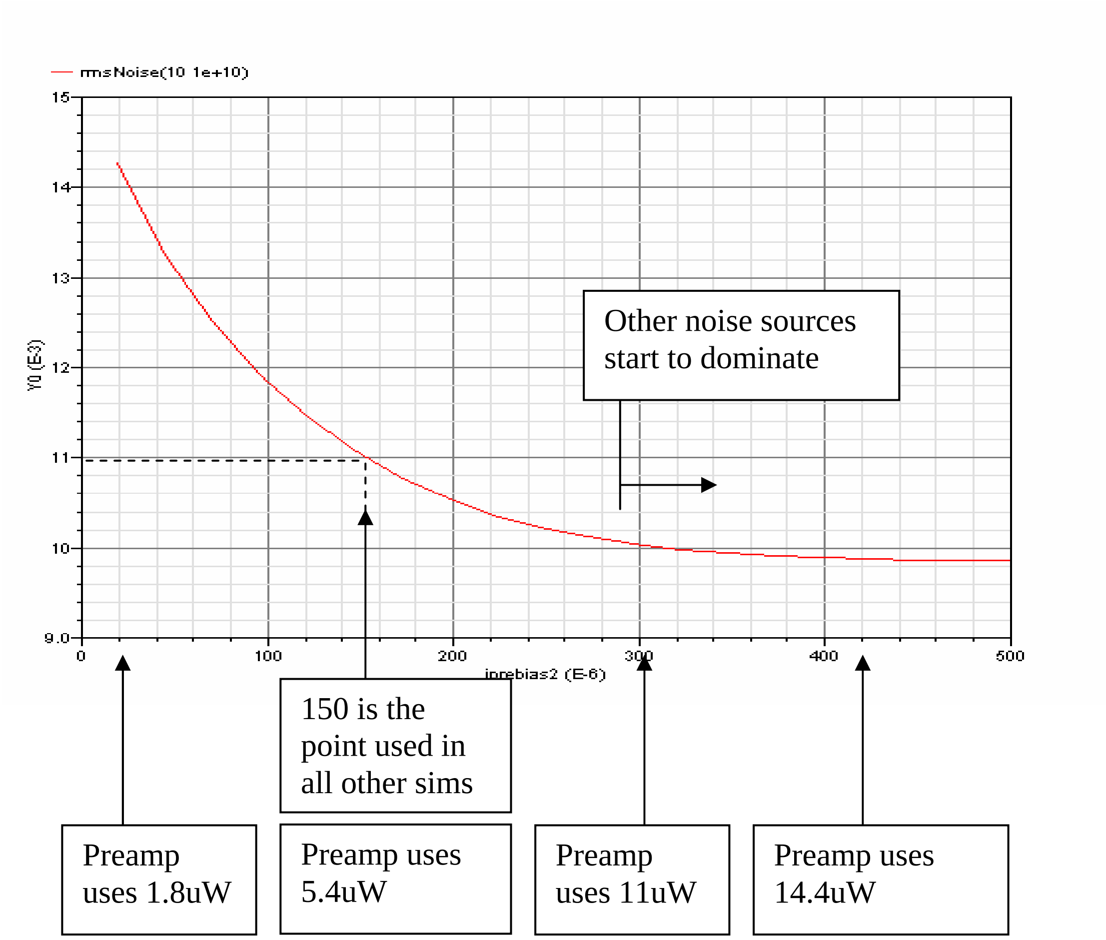
The dominant noise source is the preamplifier input transistor, M0.

The other dominant noise sources are M11 and M12, the pair of input transistors in the differential shaper circuit, and their current source, M10.

Noise in the input transistor can be reduced by increasing the current that flows through the device. The power consumption necessary to reduce noise in this one device is significant. The signal magnitude is independent of this current, since the gain of the charge preamplifier is set by the feedback capacitance.

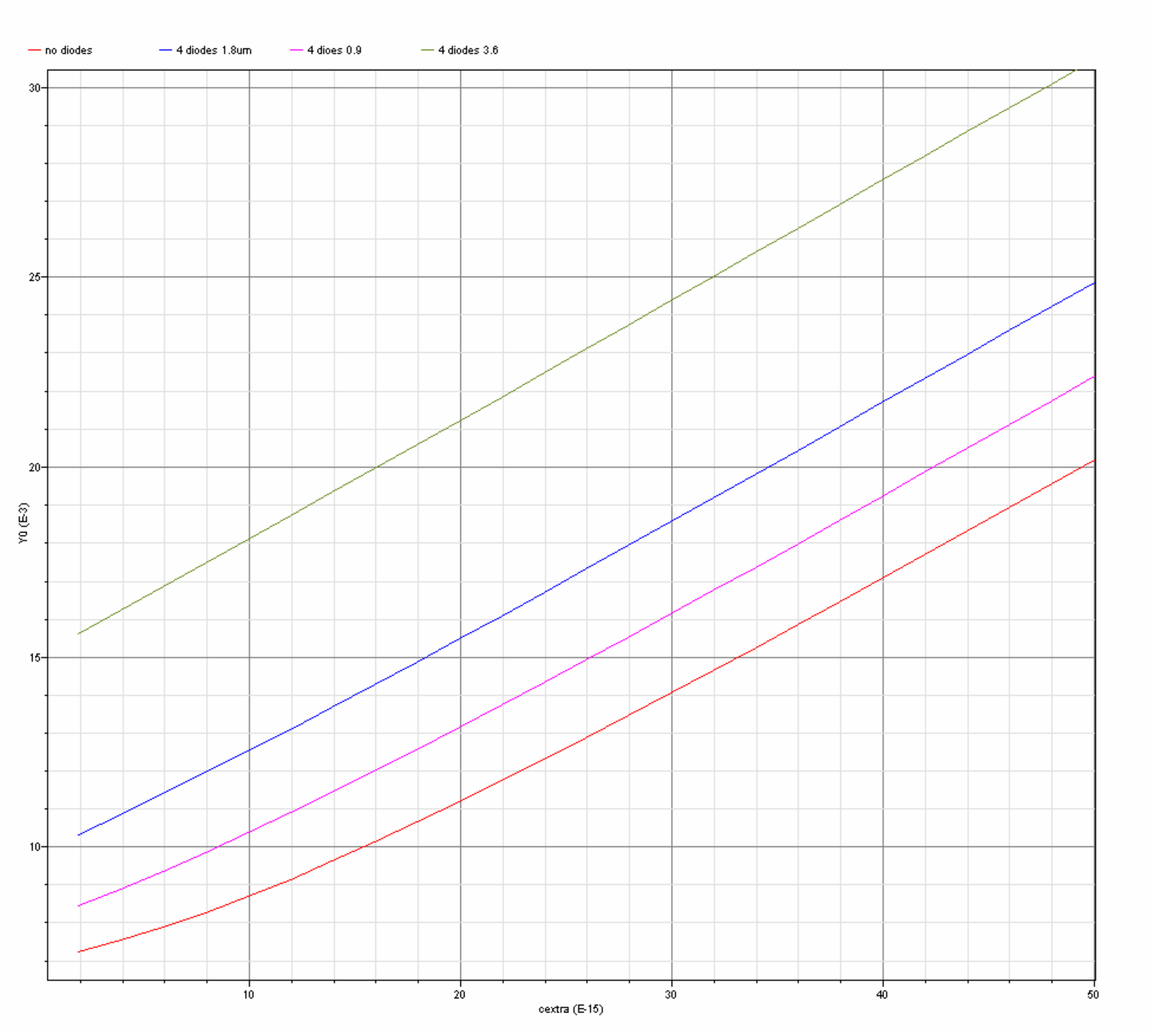


PreShape Pixel simulation: Noise Vs Input Capacitance

Circuit stimulus/scenario

Noise in the charge preamplifier is strongly dependant on the input capacitance. In these simulations, the circuit is first disconnected from the diodes; a single (ideal) capacitor is placed at the input and noise analyses run at a range of values. This is repeated with four diodes connected of sizes 0.9, 1.8 and 3.6 microns dimension to match the sizes selected for the device physics simulations. Noise is measured at the shaper output / input to comparator.

Results waveforms



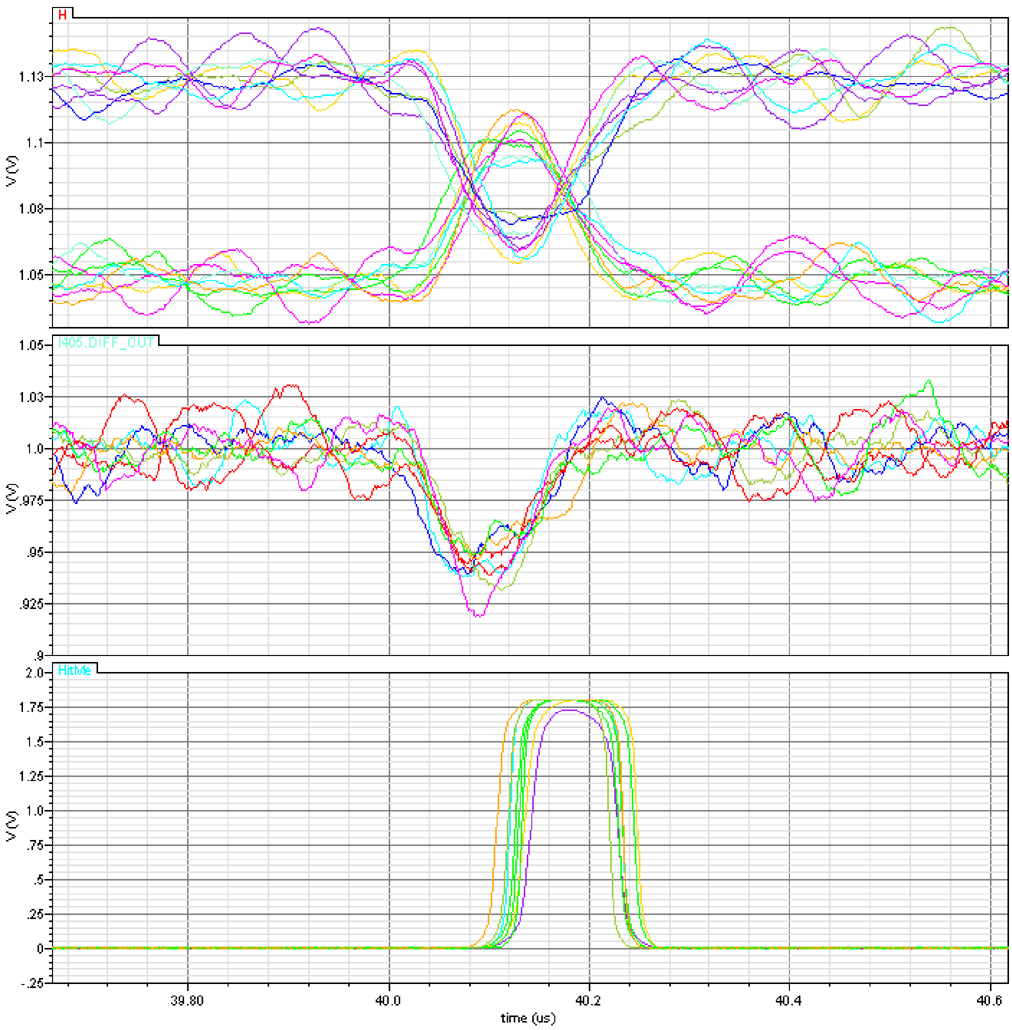
The simulations in this document have been produced assuming 8fF parasitic capacitance on the diode node, and four diodes of 1.8um size.

PreShape Pixel simulation: Transient Noise

Circuit stimulus/scenario

The key circuit nodes are simulated with transient noise to illustrate the likely real operation. 15 runs are superimposed (typical process corner) for a 1MIP hit (250e).

Results waveforms



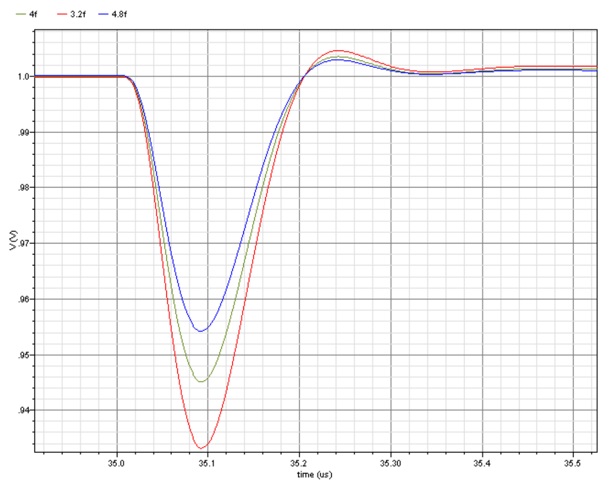
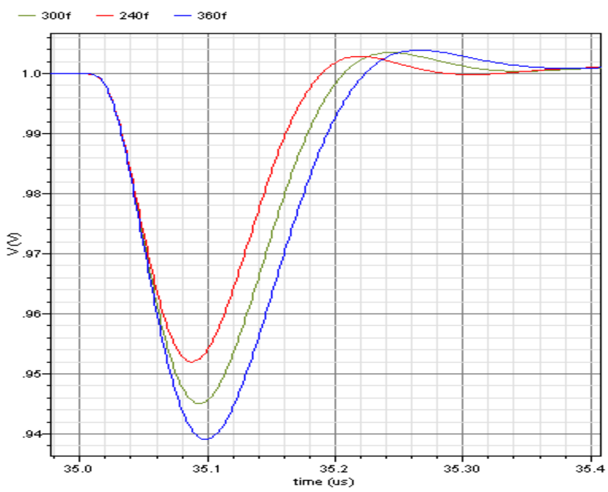
The “hit” signal pulse varies from 85ns to 140ns duration.

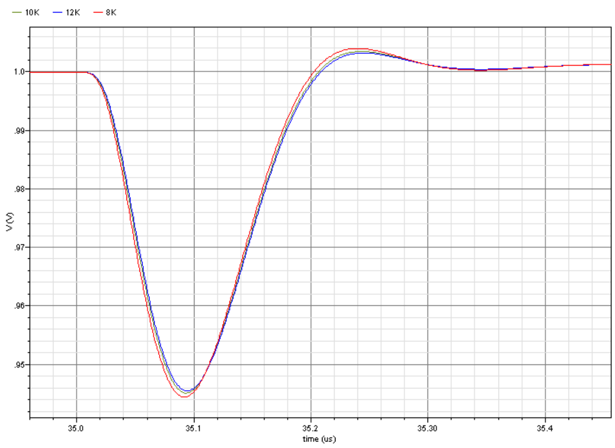
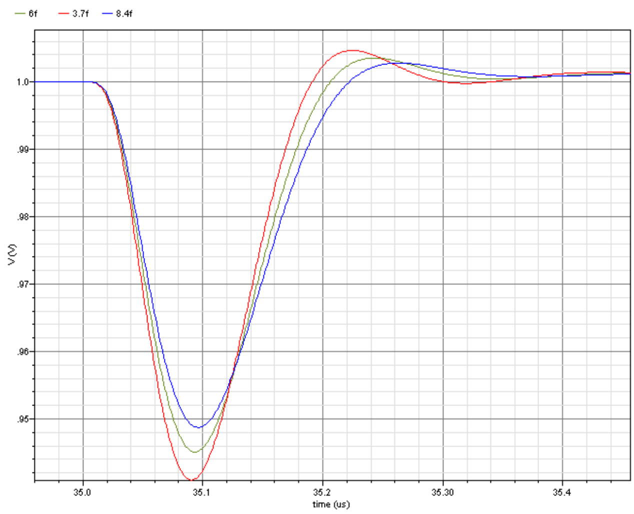
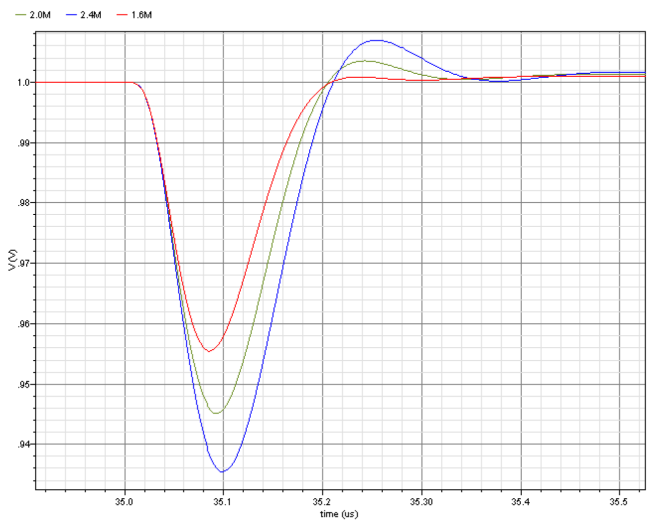
PreShape Pixel simulation: Matching/Manufacturing Risks

Circuit stimulus/scenario

Each passive component in the preamp and shaper circuit is varied individually to check the dominance of their value on the signal pulse. Those components that have the largest effect will contribute most to mismatch between pixels and should be most carefully considered during layout. [Note that simulations in this section are qualitative (from an earlier version of the circuit), and so the absolute values of signal pulses should not be taken as true indication of the final circuit performance.]

Results waveforms

Preamp **Cpre**		4fF +20% -20% Matching of small capacitance will be poor, and effect on signal is significant: <u>High risk</u> Matching may be improved using two 8fF devices in series
Shaper **Cin**		300fF +20% -20% Large area capacitance should match reasonable well <u>Medium risk</u>

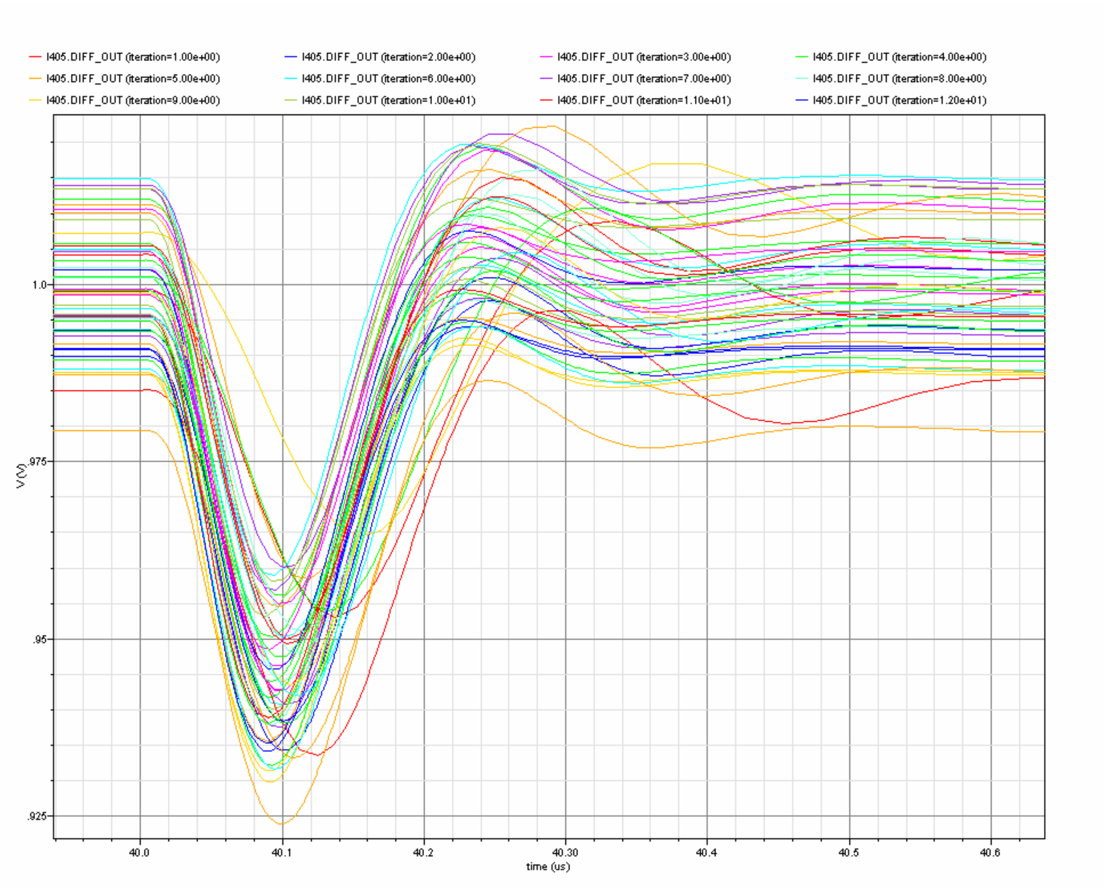
Shaper **Rin**		10K +20% -20% <u>Low risk</u>
Shaper **Cfb**		6fF +40% -40% Small (near minimum) size capacitor even +/- 40% does not impact too much so fairly <u>low risk</u>.
Shaper **Rfb**		2M +20% -20% Large device (long track of high resistance poly) so matching should be reasonable: <u>Moderate risk</u>

PreShape Pixel simulation: Mismatch

Circuit stimulus/scenario

Monte-Carlo simulation varies component parameters according to statistical models: Typical process corner; 1MIP (250e) input signal.

Results waveforms

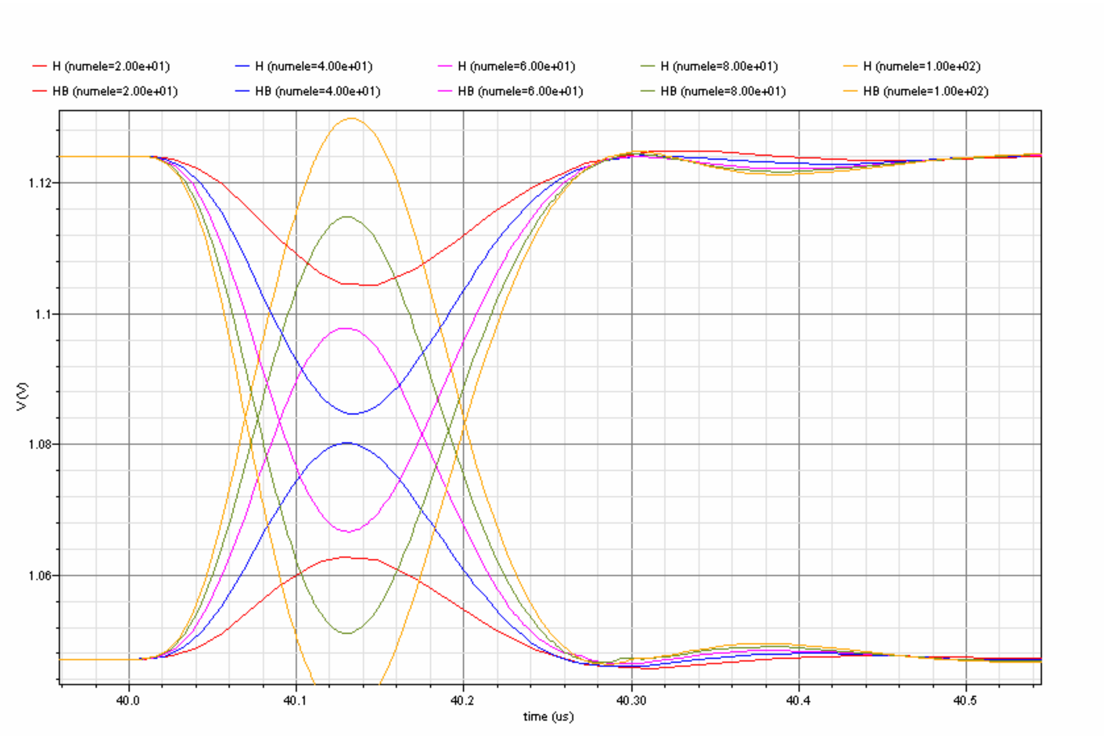


PreShape Pixel simulation: Comparator Noise

Circuit stimulus/scenario

The in-pixel comparator uses only nmos devices, but this yields very low gain, hence the differential signals are effectively the output from a differential amplifier with low gain (approx 3).

Results waveforms



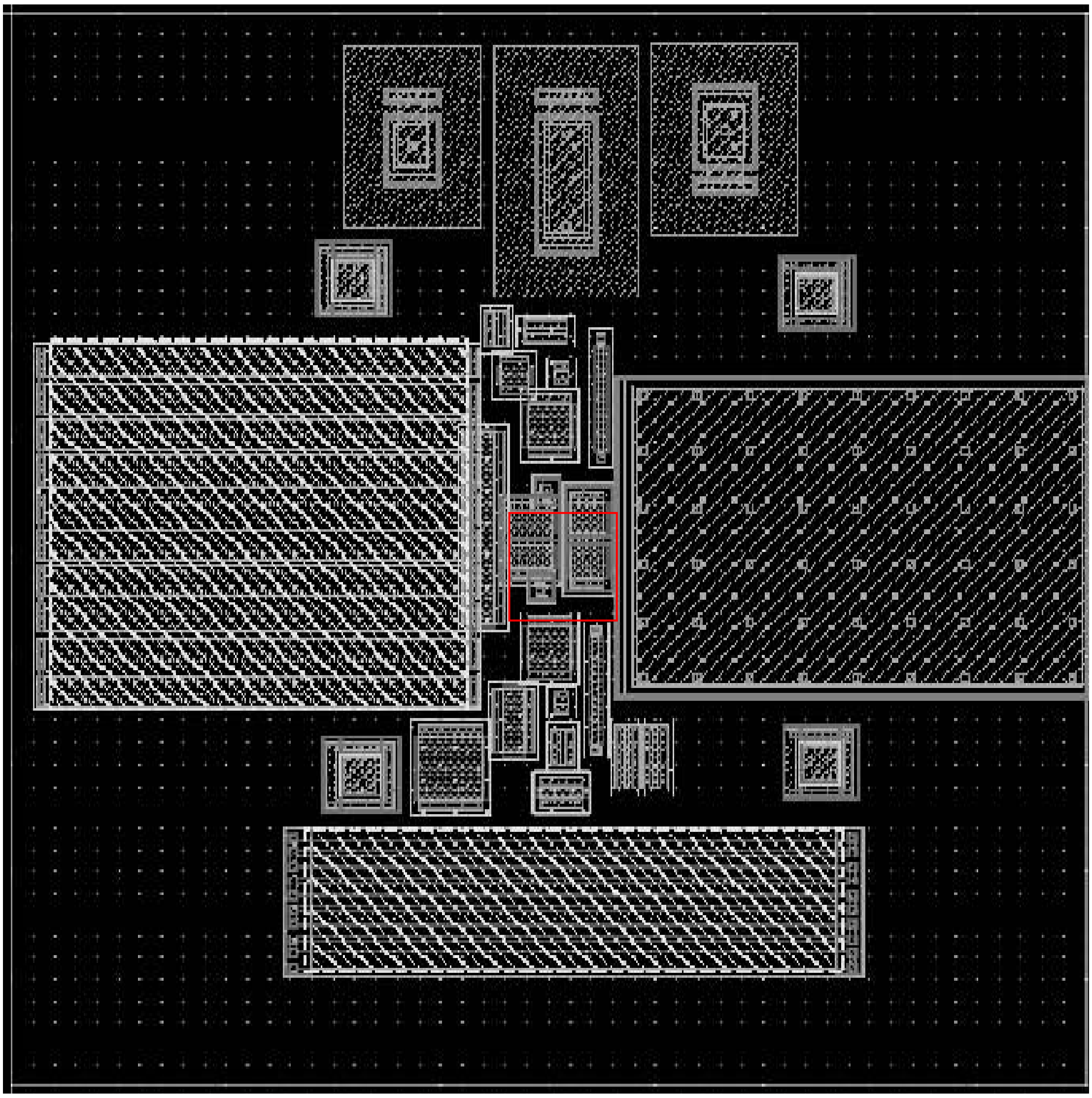
Above: Differential "hit" signal for 80, 160, 240, 320 and 400 electrons input signal; the threshold is set at 125 electrons equivalent level.

Noise on the differential H/HB signals is simulated to be 14mV.

- Consider repeating full noise analysis at this point instead – is actually the two inputs to the high-gain comparator…?

Pixel Layout Placement

The plot below is a quick placement of all the pixel components in a 50 micron pixel boundary to check that they will fit. The large capacitors and resistors will dominate the pixel area, but there is sufficient space for careful placement. The central NWELL measures approx 5um by 5um.



Issues Outstanding

- AC analyses of each circuit block
- Resolve saturation issues for larger signals seen in most recent circuit version
- Comparator analysis (will be considered again for other pixel structure)
- Comparison against signal (collected charge) results to establish true suitability in signal/noise.
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