A MAPS-based readout for Tera-Pixel electromagnetic calorimeter at the ILC

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Outline

• ILC CALICE
• CALICE MAPS Concept, R&D activity
• Conclusions
• Exact ICL beam timing parameters not yet defined
  – Assume close to previous (“TESLA”) design
  – Beams collide rapidly within a quick burst (“train”)
  – Long dead time between trains

• Assume worst case timing as follows
  – Beam collision rate within train = 6.7 MHz, i.e. 150ns between collisions
  – Number of collisions within train = 14000, i.e. train is 2ms long
  – Train rate = 10Hz, i.e. 100ms between trains; 2% duty cycle

• Rate of signals
  – ILC is not like LHC; rate of physics processes is small
  – Most collisions give nothing, but when reaction does happen, many adjacent channels will be hit
  – Expected rate not very well known; needs detailed simulation modeling
  – Assume average ~10–6 hits/pixel/crossing, which is ~0.005 hits/pixel/train
CALICE description

- CALICE has a baseline ECAL design
  - Sampling calorimeter, alternating thick conversion layers (tungsten) and thin measurement layers (silicon)
  - Around 2m radius, 4m long, 30 layers tungsten and silicon, ≈2000m² Si
- Mechanical structure
  - Half of tungsten sheets embedded in carbon fibre structure
  - Other half of tungsten sandwiched between two PCBs each holding one layer of silicon detector wafers
  - Whole sandwich inserted into slots in carbon fibre structure
Baseline ECAL design
- Silicon sensor detectors in baseline are diode pads, pad size between 1.0×1.0 and 0.5×0.5 cm², glued to large PCB
- Pad readout is analogue signal; digitized by Very Front End (VFE) ASIC mounted on the other PCB side
- Si wafers ≈ 10x10cm²
- Si layers on PCB ≈ 1.5m long 30cm wide
- Average dissipated power 1-5 µW/mm²
- Total number of pads around 20-80M
CALICE MAPS design

MAPS ECAL design
Baseline design with diode pads largely unaffected by use of MAPS

Potential benefits include:
- Reduced PCB section for MAPS → Decrease in Moliere radius → Increased resolution
- Increased surface for thermal dissipation
- Less sensitivity to SEU because of spread out logic
- Cost saving (CMOS standard process vs. high resistivity Si for producing 2*10^7 cm^2 and/or overall more compact detector system)
- Simplified assembly (single sides PCB, no need for grounding substrate)

Baseline design with VFE (left) and MAPS without VFE (right)
CALICE MAPS design

- Divide wafer into **small pixels** so as to have small probability of more than one particle going through each pixel
- Binary readout, 1bit ADC
- Improved jet resolution or reduced number of layers (thus cost) for the same resolution

- Around 100 particles/mm$^2$ pixel size of maximum 100 X 100µm$^2$
- Current design with 50 x 50µm$^2$ pixel
- Total number of pixel for ECAL around 8 x 10$^{11}$ pixels **Terapixel** system
- Record collision number each time hit exceeding threshold (timestamp stored in memory on sensor)
- Information read out in between trains

**Effect of pixel size**

- For 50µm pixel, roughly 1 particle/pixel
- For 100µm pixel, >1 particle/pixel

![Graph showing the effect of pixel size on the number of hits per event.](image)
CALICE MAPS design

- First prototype designed in CIS 0.18 µm process submitted early 2007
- Different pixel architectures included in the first prototype
- Target is to reduce noise to the level of physics background (S/N>15)
- Faulty pixels masking and variable threshold to reduce false hits and crosstalk
- Optimization of pixel layout and topology essential
- Minimization of power consumption essential
• Pixel layout optimization:
  Maximization of signal
  Minimization of charge sharing (crosstalk)
  Collection time

Large phase space:

- Pixel size
- Diode size
- Diode layout
- Biasing
- Process
CALICE MAPS design

Full 3D device simulation using TCAD
Sentaurus (Synopsys) for charge collection study

Collected charge on the diodes and central Nwell vs. MIP impact position

Q lost in NWell
Q collected by diodes

MAPS - central NW houses electronics.
Crosstalk is reduced by increasing threshold. This at the expense of S/N. Reduce the charge lost in N-Well housing the readout electronic.

- $\Delta v = 52 \text{ mV} @ 250 \text{ e}^-$
- Noise $= 12 \text{ mV (8 fF)}$
- S/N $= 4.33 \text{ (Sg = Ng)}$
- $\text{e}^-_{\text{in}} \sim 57 \text{ e}^-$
CALICE MAPS design

Optimization MAPS process

- Using Pwell implant to shield N-well housing readout electronic
- Improvement in charge collection
- Optimization of the diode location and size is necessary

![Diagram showing electric potential in epitaxial layer](image)
• Several Deep P W layouts studied
• Optimization of collecting diodes **size and location** given the electronic design constraints

**Cell size: 50 x 50 \( \mu m^2 \)**
CALICE MAPS design - pixel simulation -

Pre-sample Pixel layout

Σ diodes Q (x,y)

S/N

Distance to Diode (µm)

G. Villani

CALICE MAPS

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Pre-Shape:
Pixel reset before start of bunch train
Stand by in readout
Hit event generates one time hit-flag to the logic
CR-RC shaper decays according to input amplitude then is ready to accept next event

Pre-Sample:
Pixel reset before start of bunch train and automatically after local hit during bunch train
Stand by in readout
CA output sampled after Reset and then real-time difference input to comp

Expected similar noise characteristics from both designs
Each digital block serves 42 pixels from one row.
Row split into 7 groups of 6 pixels.
Following a hit, for each row the logic stores in SRAM time stamp (13 bits), pattern number (3 bits), pattern (6 bits).
22 bits/hit + 9 bits row encoding = 31 bits/hit.
Register for masking out noisy pixels.
• 1*1 cm² in total
• 2 capacitor arrangements
• 2 architectures
6 million transistors, 28224 pixels
• Estimated power:
  ≈10 µW/pixel continuous
  ≈40µW/mm² including 1% duty factor
• Dead area ≈200 µm every 2 mm
• Each sensor could be flip-chip bonded to a PCB
CALICE MAPS design – pixel architecture
Laser MIP
• Three wavelength laser: 
  \[ \lambda = 1064, 532, 355 \text{ nm}, \]
  focusing < 2 \, \mu m,
  pulse 4ns, 50 Hz repetition,
• Labview Control software
• MIP Calibration: Si reference detector coupled to low noise CA + differentiator (no shaper)
  A250CF peltier cooled
• Amplifier Gain measured ~ 7mV/MIP
• Amount of stray light and EMP reduced within the laser test setup
A250CF calibration using injected charge through capacitor and pulse generator
CALICE MAPS - RAL test setup -

- A250CF output vs. Laser intensity
- Q injected vs. Laser intensity
- MIP-equivalent vs. Laser intensity
- Sub-MIP resolution AND accuracy capability ($\lambda = 1064$nm, spot size = $2\mu$m)

\[ V = 1.1429 \times \left( \frac{\%}{100} + 1 \right)^2 - 3.4731 \times \left( \frac{\%}{100} + 1 \right) + 14.656 \pm 0.0272 \times \left( \frac{\%}{100} + 1 \right)^2 - 0.0088 \times \left( \frac{\%}{100} + 1 \right) + 0.41 \]
Conclusions

- MAPS-based ECAL can potentially offer a number of advantages in terms of performances and overall cost
- Novel INMAPS process for MAPS might have significant advantages in terms of charge collection efficiency
- Pixel design and readout electronics optimized for charge collection and S/N
- First design aims at demonstrating feasibility of the approach and to achieve significantly high S/N
- Power dissipation still high and needs to be addressed
- Test setup ready
- Chip testing underway now
CALICE MAPS backup slides

- Preamp uses 1.8uW
- Preamp uses 5.4uW
- Preamp uses 11uW
- Preamp uses 14.4uW

150 is the point used in all other sims

Other noise sources start to dominate
Geant4 $E_{\text{init}}$ in 5x5 $\mu m^2$ cells

Apply charge spread $E_{\text{after charge spread}}$

Register the position and the number of hits above threshold

+ noise only hits: proba $10^{-6}$ ~ $10^6$ hits in the whole detector
  BUT in a 1.5*1.5 cm² tower: ~3 hits.

Add noise to signal hits with $\sigma = 100$ eV
(1 e- ~ 3 eV $\times$ 30 e- noise)

Importance of the charge spread:

$$\sum E_{\text{neighbours}} \sim (50\% - 80\%) \times E_{\text{init}}$$

Sum energy in 50x50 $\mu m^2$ cells $E_{\text{sum}}$
CALICE MAPS backup slides

1. Stave structure
2. Lack of hybrids/ASIC allow less complex/thinner PCB
3. Thinner sensors (down to 100 μm)
4. Bump-bond MAPS

![Diagram of CALICE MAPS](image-url)