# TPAC1.0

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## Laser Scans



2um spot 2um steps Analog readout Mean Signal (25 samples)

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### **TPAC1.1 Status**

- Poor device yeild (short circuit)
  - Typ 40% working, from 60 probed devices, but the 12u+DPW split is worst ~20%
- Poor bonding yeild
  - typ 40/250 fails per chip
- Reported problems to foundry
  - Will report back after some investigation
  - Follow-up run (std + hi-res wafers) on hold until these investigations report back

#### • Functionality

- Configuration load
  - Errors under investigation
- Data corruption (override mode)
  - Fixed at RAL, but some low-level problems still reported at IC
  - Will swap boards and investigate further
- Design feature
  - Duplicated row-addresses
- Test structures
  - Monostables ok
  - Laser scans
  - 55Fe
- Threshold Scan

- $\rightarrow$  more details on later slides
- ightarrow more details on later slides
- $\rightarrow$  more details on later slides/Marcel
- → more details on later slides

# **TPAC1.1** Design error

- Row addresses
  - − Should run 0 $\rightarrow$ 167
  - − Actually run  $0 \rightarrow 83, 0 \rightarrow 83$
- Ambiguity in location of a hit
- Caused by copying chosen pixel sub-array to whole sensor
- Matt & Paul's suggested workaround
  - Artificially store one hit per row
    - Trivial to implement, one additional initialisation clock cycle before the bunch train begins
  - All rows participate in (sequential) readout
    - Hence we know where real hits sit in the datastream  $\rightarrow$  array
  - Reduced number of available memories to 18 per row
  - Real-time processing (software?) to strip and correct data so data files stored are back-compatible format with false data removed.

# First look: TPAC1.1 Threshold scan











# **Explanation**?

 PCB hole seen to be misaligned (camera on laser microscope used to check known positions of pixels)





Next: Try another sensor!





### Summary

РСВ	Sensor	Status
37	5u +DPW	At IC (→ RAL today) Problems with config load
40	5u +DPW	At RAL (JC) Ok (apart from config load) Currently being used for debug (soldered probes etc)
32	12u +DPW	At RAL Two dead columns Being used for analog test pixels (laser, 55Fe)
35	5u +DPW	At RAL Severe data corruption – to be investigated
36	5u +DPW	At RAL ( $\rightarrow$ IC today) ok (apart from config load)
31	12u +DPW	Bonding
32	12u +DPW	Bonding
38	N/A	Power-ground short (from first round of bonding) Awaiting rework