# CALICE - Additional Information For The PPRP

February 23, 2005

Prof. G. P. Heath provided us with feedback and specific questions which we answer below.

## 1 General

1. *Can we have a short summary table giving the overall picture of what is requested?*

| | FY05/06 | | FY06/07 | | FY07/08 | | Total | |
|---|---|---|---|---|---|---|---|---|
| | SY | £k | SY | £k | SY | £k | SY | £k |
| Total Non-Staff | | 106 | | 281 | | 300 | | 687 |
| Existing Staff | 2.6 | 153 | 3.9 | 246 | 5.4 | 362 | 11.9 | 762 |
| New Staff | 5.2 | 253 | 7.2 | 375 | 7.2 | 404 | 19.6 | 1033 |
| Non-PPARC Staff | 3.2 | | 3.1 | | 4.0 | | 10.3 | |

Table 1: Request summary table

2. *Can you provide a summary of the work to be done by each of the five new RAs?*

   - Birmingham RA-1: The Birmingham RA-1 is primarily working on the algorithm development and simulation in WP5. The focus for this RA (half of their total time) would be the delivery of the energy flow algorithm and related studies, Task 5.1, with the effort distributed uniformly throughout the three year period. The RA would work closely with N.K.Watson, G.Mavromanolakis and other staff at both Birmingham and Cambridge on this.

     RA-1 would also be responsible for aspects of simulation support of other work packages, for example simulation of the test beam environment for the MAPS beam test, Task 5.3.

     The remaining 25% of the post is devoted to the current test beam programme, Tasks 1.2 and 1.3 (in years 1-2) and MAPS, Task 3.1 (in years 2-3). For the test beam programme, the activity would be data analysis and participation in data taking. In the case of MAPS, the RA would set up a cosmic ray test stand, perform the tests and participate in the beam test. They would also assist the RAL/PPD RA-5 with firmware design for the beam test PCB and benefit from close contact with R.J.Staley who will design this PCB.
   - Imperial RA-2: The Imperial RA-2 is mainly working on the current beam test programme and MAPS. The MAPS work takes roughly half this RA effort throughout the whole period. In the first year, this is concentrated on improving the MAPS physics simulation, Task 5.3, based on results from the device-level simulation produced by E.G.Villani. In addition, they will estimate the improvements or degradation to the

physics of the ILC arising from using MAPS, including studies to indicate the level that sensor characteristics (such as crosstalk) are critical for the physics performance. In the subsequent years, the effort is mainly in preparing the test bench at Imperial and then actually performing the MAPS tests, Task 3.1.

The current beam test work will take the other half of their effort for the first two years and consists of both analysis of the data, Tasks 1.2 and 1.3, and maintanence and upgrades to the DAQ software, Task 1.1.

The final amount of effort, roughly half in the final year, is to do preparations for, and then testing of, the VFE ASIC chips, Task 2.1.

- RHUL RA-3: During the first year, RHUL will work on simulation and analysis of test beam data through part of the effort of F.Salvatore, a rolling grant-funded RA. The new RHUL RA-3, appointed from April 2006, will extend this activity together with F.Salvatore to global detector design and physics studies, Tasks 5.2 and 5.4. Particular issues to be addressed will be the development of physics benchmark analyses and their application to different detector concepts.

  The rest of this RA effort will be devoted to developing a test system for high-rate switching, and to use this system to measure the performance of different elements of the system, Task 2.3. This work will be carried out working with B.J.Green at RHUL in conjunction with the Manchester group, a team that has already worked together on the ATLAS high level trigger.

- UCL RA-4: The UCL RA-4 would work mainly on DAQ hardware and the current test beam programme supporting both with simulation studies. For the first two years, about 1/3 of their time would be dedicated to the test beam data analysis, Tasks 1.2 and 1.3.

  Over the full three years of the project, the RA would spend 60% of their time working with UCL academics and engineers on the DAQ R&D outlined in the proposal. UCL is involved in Tasks 2.3, 2.4 and 2.5 and the RA would contribute to all of these: designing and setting up test benches, programming FPGAs and testing new hardware.

  In addition, for the first two years, the RA would be doing some simulation at a rather low level supporting work for the test beam and DAQ workpackages, Task 5.3. In the final year, when the test-beam data taking has finished, they would spend 40% of their time on simulation. This would be support for the DAQ workpackage on understanding pre-clustering and further understanding of the test beam data, again Task 5.3. We also envisage some participation in global detector design studies, Task 5.2.

- RAL/PPD RA-5: This post starts in January 2006 and would be completely concentrated on the MAPS testing, Task 3.1. They would serve as the direct connection between the design group in RAL/ID and the physicists working on tests at Birmingham and Imperial. This person would play a major role in the MAPS beam test in the third year, including contributing to the beam test PCB firmware.

Note, the current CALICE effort is strongly enhanced by two PPARC Fellows, both of whom finish their Fellowships within the first six months of the proposal period.

3. *For the work to be done by existing staff, what is the currently planned activity for these posts (e.g. in the 2004 RG round)? What happens to this if they move to CALICE?*

   - Birmingham: The RG-funded staff were fully ringfenced in the last round, almost entirely to ATLAS with a small fraction to ALICE. Movement of (non-PPARC funded)

effort within the group compensates for the transfer to CALICE, and the proposal is entirely consistent with the RG submission. There is no infringement of any ringfence.

- Cambridge: The RG-funded staff (M.J.Goodrick, R.Shaw and C.Barham) were all ringfenced in the last RG round, mainly to ATLAS but also for to LC-ABD (R.Shaw and C.Barham) and LHCb (C.Barham). The transfer to CALICE is taking up slack from the ATLAS work which is coming to a successful end. This has been approved by the ATLAS-UK management.
- Imperial: All RG staff involved were listed as ILC effort at the levels proposed in the last RG submission. In particular, there has been no infringement of the CMS or LHCb ringfence.
- Manchester: Only a very small amount of effort was explicitly listed as ILC in the last RG. However, 1.3SY of effort was listed as "Other Developments" and this contributes to the effort in the proposal. The people involved are moving from ATLAS; however, the overall ATLAS ringfence total effort has been preserved. The changes have been approved by the ATLAS-UK management.
- RHUL: The non-ringfenced effort of B.J.Green and G.Boorman were declared as ILC effort in the last RG application. The effort of F.Salvatore will move a little faster from BaBar than was stated in the RG application by about two months in total before April 2007.
- RAL/PPD: The SLA contained 0.5 FTE for CALICE work over the period of this proposal. M.Tyndel and E.G.Villani will transfer some effort to fill this from ATLAS and MI$^3$, respectively.
- UCL: All RG staff involved were listed as either ILC or "Future Neutrino Experiment" effort in the last RG submission at the levels proposed here. Although there has been some movement of people between these two categories, the total effort for each is unchanged and this proposal is consistent with the ILC effort levels of the RG submission. In particular, there has been no infringement of the ATLAS ringfence.

## 2 Workpackage 2

*Issues arose as to whether the work was too early. The revised submission should address what is really needed for the TDR.*

In the seedcorn period, the UK has established itself as the lead country in DAQ for the ILC calorimeter. This brings with it the likelihood of scientific and technical leadership, and important industrial involvement, in this major area of an ILC detector. To maintain such a position, however, we must continue to aggressively develop ideas and push forward our strategy for the DAQ. To this end, we have in the proposal identified a number of tasks where potential bottlenecks exist, where the design of the whole calorimeter could be revolutionised, and where R&D is therefore required to write a TDR. We have taken as a baseline the Si-W pads but have made the majority of the R&D generic enough such that we can read out different designs, e.g. MAPS, or a different number of channels, e.g. including the hadronic calorimeter. This will be achieved by using commercial components where possible and building test systems which are scalable. With the detector TDR expected to be written in 2009, it is essential to solve outstanding problems, and come up with a DAQ system concept by the end of the next three years. This will clearly establish the UK as the lead group in this area and allow us to build the DAQ system for full-scale prototypes and the final detector. Each of the five tasks is discussed below in the context of their necessity to be done before the TDR. We feel that the TDR cannot be written if these questions are not answered.

### Task 2.1: Readout of prototype VFE ASICs

The LAL/Orsay group is currently designing a first realistic version of an ASIC chip which could be used in the CALICE detector. The electronics engineers in that group concentrate mainly on the functionality of the design rather than system-level issues. This is why it was UK people, rather than the LAL/Orsay personnel, who discovered both the temperature dependence of the pedestal (shown on slide 7 of P.D.Dauncey's presentation) and a large crosstalk for the last channel on the ASIC in the previous version of the chip. This information was fed back to the design group who were able to fix the crosstalk problem in the current version being used for the beam test. This method of working has proved very fruitful up until now.

As we propose to do all data transfer immediately after the ASIC up to just before the full data reconstruction, it is essential that we continue this close collaboration with the ASIC development and highlight any problems in their design or its implications for the DAQ during the future developments. The first pre-prototype will be manufactured in 1.5 years at which point we would like to have the basic electronics to be able to read this out and measure the performance of the chip.

### Task 2.2: Study of data paths over 1.5 m slab

Central to the design of the calorimeter is that the boards in the detector are 1.5 m in length. Building boards of such size is a mechanical challenge, but also raises questions for the DAQ and its influence on mechanical and thermal issues. The main issues are crosstalk, bandwidth and number of transmission lines needed. All of these will be investigated by both experiment and simulation. These measurements will also provide useful input to thermal studies. These issues can be tested using a mock board in which we have FPGAs connected together. This will the provide valuable input when a full prototype board and the final detector is built. Should these results show insurmountable issues using 1.5 m boards, this will have a significant impact on the design of the calorimeter and so needs to be identified before the TDR.

### Task 2.3: Connection from to on-detector to off-detector receiver

This task is one which particularly highlights our principle of using commercial components rather than the more traditional bespoke products. The connection from the detector to the receiver will be controlled by a commercial network switch. There are two designs which we consider, both of which need to answer questions of volume, rate and efficiency of switching. As the rates we require are cutting-edge even for industry, these need to be investigated and tested to demonstrate their efficacy within the timing structure of a TESLA accelerator. Test-bench experiments will be built and performed which are assumed to scalable in such things as number of lanes. One of the options proposes to use an optical "layer-1" switch which is very new technology. Here this design also addresses whether optical fibres can be used directly from the ASIC to a PCI card. This results in very high rates and we need to investigate whether optical switches operate within our timing structure. Should we demonstrate this is feasible, we would then be able to feed back information to designers of the ASICs on what needs to be done within the chips to be read out most efficiently by our DAQ system. The possibility of removing the front end electronics could be beneficial financially, mechanically, thermally and for the reconstruction of physics events. However, this is a radical change in design of not just the calorimeter but also has effects on the whole detector. This would have to be decided before any full prototype were built and it therefore needs to be understood for the TDR.

### Task 2.4: Transportation of configuration, clock and control data

This is again a task which is based heavily on the use of commercial equipment and will provide indications as to how the hardware can eventually be incorporated into a dedicated timing structure present at a particle physics accelerator. Different pieces of hardware, probably from different vendors, will have different clocks in them. This self-contained task will develop a solution to being able to synchronising all of these clocks. The solution will use a certain set of hardware to demonstrate a generic principle which can be used for future detectors. Related to this is the possibility of reseting FPGAs which are inaccessible on the detector. A solution here is sought which is 100% efficient, compact and gives out little heat. Such results will ease the building of the final calorimeter but could also be applied or used in other sub-detector systems or the global detector itself. Only by documenting this in the TDR could our ideas be adopted.

### Task 2.5: Prototype off-detector receiver

This task involves using both proprietary and commercial technology. The development of a PCI card is to maximise its flexibility as we will have it plugged into different types of networks, programme the FPGAs and control our clocking and configuration data. This will be based on PCI Express technology which is currently cutting-edge and we assume to be scalable in the number of lanes. As well as answering questions on bottlenecks in the system, the card could be used for future prototypes of both the calorimeter or even other detector systems in other experiments. We will also answer questions of "regional triggering". It is unlikely that we can get all the information from the calorimeter into one PC, so we will investigate how much of a geographical region can be sent to a PC. This will allow us to do some clustering or matching of results from several PCs facilitating some event filtering. This then also has similar ramifications for regional tracking; looking in azimuthal regions for high $p_T$ tracks and even potentially track-calorimeter cluster matching. Each of these studies could have a major impact on the DAQ architecture and so do need to be done before the TDR.

### Summary

CALICE-UK have designed a concept for the DAQ system for the ECAL at a future linear collider. We have identified areas where solutions are required in order to be able to write a techincal design report by 2009. This will then place CALICE-UK in the lead position to build the DAQ system for full-scale prototypes and the final system.

### Specific questions

1. *How do the resources requested map on to the different Tasks?*

   From the total £720k requested for WP2, £170k is for (fractions of) new RA staff for Imperial, RHUL and UCL and a fraction of N.Pezzi's time and £177k is for equipment and travel. Therefore the remainer, £370k (about half of the request) is for staff already funded by PPARC through the RG. There is also a significant amount of academic effort.

   Table 2 shows the breakdown for items which can be allocated to the individual tasks. Travel (£33k) is not included as most trips cannot be sensibly assigned to separate tasks. No indexing has been included.

2. *Comment on whether diode pads and MAPS impose similar requirements on the DAQ. If there are significant differences, how does the DAQ part of the project propose to handle this?*

| | Effort (£k) | Equipment (£k) | Institutes |
|---|---|---|---|
| Task 2.1 | 60 | 9 | Imperial |
| Task 2.2 | 64 | 34 | Cambridge |
| Task 2.3 | 141 | 52 | Manchester/RHUL/UCL |
| Task 2.4 | 84 | 12 | UCL |
| Task 2.5 | 175 | 29 | Cambridge/RHUL/UCL |
| Total | 524 | 136 | |

Table 2: Breakdown of requested resources for Workpackage 2 by task

The diode pads and MAPS options do impose similar requirements on the DAQ. For the MAPS, there is no ADC and the threshold has to be applied on the wafer, by definition. This results in the MAPS data volume within the on-detector PCB being smaller than the diode pads, where each ADC value is read out, by around an order of magnitude. However, the diode pad ADC values will then be threshold suppressed in the front end on-detector FPGA. The level of reduction depends on what threshold cut is applied, but should be around two orders of magnitude. Hence, for the on- to off-detector data transfer, the diode pad option will have a smaller data volume than MAPS, again by around an order of magnitude. These differences are well within the uncertainties for the ECAL overall at this stage. Hence, our DAQ work would also be appropriate for the MAPS option.

3. *To what extent can the work on off-detector DAQ be viewed as generic to different components of an LC detector (vertex detector, tracker, muons)? Does this lead on to a major UK role in provision of central DAQ for some collaboration? On the other hand, if it is calorimeter specific, why are not generic solutions being investigated?*

   The conceptual design presented by us for the calorimeter is the first such report by any of the sub-detectors within linear collider study groups. The UK DAQ concept has been fleshed out in detail for the expected rates and numbers of fibres for the ECAL. However, most of the items discussed for Tasks 2.3, 2.4 and 2.5 are completely generic to any subdetector. In particular, the idea of using a backplaneless DAQ with commercial components makes the concept easily transportable.

   Therefore although not specifically working on the DAQ alone, our DAQ R&D could influence and be used by other detector components and the central DAQ itself. The UK would then be in a very influential position. The idea is to work on generic solutions for ease of integration and to cater for different designs or configurations, e.g. MAPS and the HCAL.

4. *Following on from above: does the calorimeter "drive" the overall DAQ design for an LC detector?*

   Slide 3 from P.D.Dauncey's presentation shows that at the time of the TESLA TDR, the two largest subdetectors in terms of data volume were the TPC and the ECAL. Since that time, the UK has reassessed the data transfer requirements for the ECAL and it is clear the ECAL TESLA numbers were based on very optimistic assumptions, mainly regarding the level of threshold suppression which would be possible. We now believe the rates will be at least an order of magnitude higher than previously assumed.

   No such reassessment has been done (at least publically, i.e. that has been shown in any presentation at an ILC workshop) for the other detectors. Hence, we have to assume

there is a large uncertainty in the other data volumes also and that there may be similar increases for them. However, it is unlikely that any would be orders of magnitude larger than the revised ECAL values.

Therefore, it is clear that the ECAL, if not definitely the largest subdetector in terms of data volume, will certainly be one of the largest and so will push the design of the global DAQ system. If we are the group pushing forward ideas now, we will be in a position to drive the overal DAQ design in the future.

5. *Can you strengthen the justification for working with specific commercial technologies (PCI Express) in 2006/07 for a DAQ system to be implemented in 2013/14?*

   One of the main issues with the DAQ architecture is how fast and how much data can realistically be transported into a single PC. This will clearly improve between now and when the ILC detector is built; over the next decade, we would expect commercial products to increase by 1-2 orders of magnitude. However, this is a wide range and the actual rates could influence the overall architecture. Therefore, rather than relying on Moore's Law guesswork, we proposed to study technologies which are "cutting edge" now and are expected to keep pace with future technology developments over the next ten years. PCI Express is such a technology.

   PCI and PCI-X have survived more than ten years as a standard of the industry. Although it is hard to predict how long PCI Express will last, it is being considered as a viable standard for the next decade. This is because the standard includes room for rate increases through expansion of the number of lanes; this is physically how the Moore's Law increases would be implemented. Hence, it is likely that this technology could take us up to the building of the linear collider and we want to understand it. At this stage no one has even demonstrated that an off-the-shelf PCI solution will work.

   Another aspect of Task 2.5 is that the PCI card itself will be used as a generic data acquisition I/O card, specifically for Tasks 2.3 and 2.4. To do the studies we envisage, a flexible PC interface is needed. We have therefore combined the study of PCI Express itself with the need to make such a card to save costs.

6. *Please provide some more general discussion on ideas for LC DAQ, both technical and managerial.*

   The DAQ concepts are discussed within the EFCA workshops (within Europe) and the international LCWS workshops globally. As shown in slides 3 and 4 of P.D.Dauncey's presentation, the ideas for the general DAQ concept are evolving. Some recent talks from the EFCA DAQ working group convenors give a general overview of the ideas and status [1]. However, it is clear that all concepts being discussed have several common ideas.

   The first is that the DAQ will be triggerless in terms of hardware. All data during a bunch train will be buffered and read out in the relatively long period between bunch trains. These data will then be processed on an event builder PC in a farm to search for the bunch crossings containing interesting events. All data from the whole detector will be available for this and so this software event selection will be based on the maximum information.

   The second is that the DAQ should be "backplaneless", meaning the off-detector elements should be based as far as possible on commercially available components. Clearly, receiving the data off-detector into PCs using a standard I/O stream (such as PCI Express) will be much easier and cheaper to upgrade than through a custom, crate-based system. The hope is that the whole detector can have functionally identical hardware (almost certainly

PCs) to receive the off-detector data, reducing the subdetector-dependent effort needed significantly.

The third common idea is that the movement of data immediately after the off-detector receiver will be much more fluid than in previous experiments. It is thought that the concept of "local" experimental computing will not exist and the events will be sent directly from the event buffer farm to global (virtual) storage systems for Grid-like reconstruction and analysis. This is clearly very nebulous at this point and we have not bid to study any aspect of this part of the DAQ.

7. *General question: why no plans to continue the association with RAL/ID Systems Design group?*

   The current ECAL readout boards bear no relation to the DAQ system which we envisage for the eventual ILC detector. Hence there was no obvious requirement for a continuity of expertise.

   In addition, PCB the actual designs proposed for these DAQ studies are relatively modest and do not involve very complex, highly multi-layer boards. Hence, it was felt that the work to be undertaken could be performed more efficiently (and cheaply) in-house at the respective universities.

# 3 Workpackage 3

1. *You should respond to the specific questions raised by one of the referees:*

   (a) *Surely the pad size of the detector is controlled by the Molière radius of $W \sim 10\,mm$? Why do you want $10^4$ times the granularity? What is really gained in terms of the physics?*

   The pixel size for MAPS is not driven by the wish to separate close-by showers more efficiently. The motivation for having small pixels is to reduce the probability of more than one charged particle passing through each pixel to a low level. The concept is that the pixels have binary readout, so the only information available is whether a charge consistent with a MIP (or more) was deposited. The necessary pixel size is explained on page 24 of the Case For Support and slide 17 of P.D.Dauncey's talk; the EM shower density of $\sim 100$ particles per $\mathrm{mm}^2$ means pixel sizes of around $50 \times 50\,\mu\mathrm{m}^2$ are needed. Larger pixels will have a higher probability of multiple particles and so will lead to saturation effects. This is shown in Figure 1 where the linearity and resolution determined from simulation are shown for several choices of pixel size.

   In fact, as shown in Figure 7 of the Case For Support, the smaller pixel size also does appear to improve the two particle separation. Although the pixel size is well below the Molière radius of 9 mm, this radius is really only meaningful several radiation lengths into the shower, when in has had time to spread. In the first few layers of the calorimeter, the shower is significantly narrower; with pixels, these first layers allow a better separation than for the large diode pads; they effectively act as a preshower detector.

   (b) *The Landau in thin silicon layers is broadened significantly; how does this affect the S/N and consequently the noise hits over threshold?*

   As shown in slide 21 of P.D.Dauncey's presentation, the distribution of deposited energy in thin layers is broadened considerably compared with thick layers. For the example of $10\,\mu$m of silicon shown there, the distribution extends down to around 40%

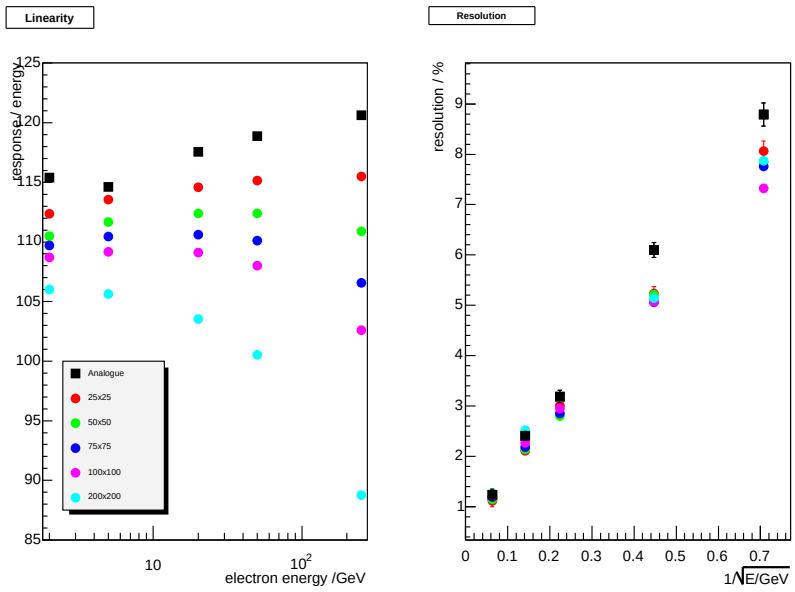


Figure 1: *ECAL linearity (left) and resolution (right) as a function of the incident electron energy, for differing MAPS pixel sizes (in $\mu$m) and the diode pad option (Analogue).*

of the most probable MIP value. This thickness is similar to the range of epitaxial layers being considered and so is a good indicator of what would be expected.

To keep the noise rate below the beam-related background hit rate, then the binary readout comparator needs to be set around $5\sigma$. To have a very high efficiency, then the comparator clearly must also be around 0.4 of the most probably MIP value. Hence defining the signal as this most probable value, then the required signal/noise for a single pixel is at least $5/0.4 = 12.5$. To allow for variations in the comparator level or pedestal and for charge sharing between pixels, we have set a requirement target of signal/noise of 20.

A signal/noise level of 20 has been achieved [2] for clusters of smaller ($15 \times 15\,\mu\mathrm{m}^2$) pixels with an $8\,\mu$m epitaxial layer, as also shown on slide 21. For the ECAL, we intend to double the thickness (and hence signal), use large pixels (which should gather more of the charge into a single pixel on average) and attempt to reduce the noise using new reset techniques (as discussed on slide 20).

It should also be considered that the underlying low resistivity silicon substrate can also contribute to the charge collected. This contribution is calculated to be of the order of the diffusion length [3].

(c) *How many pixels contain charge and would a pixel or cluster threshold be applied on-chip?*

The threshold would be applied within each pixel, so each has its own comparator; this is essential to reduce the data rate out of the sensor.

A recent paper from the MAPS collaboration [2] showed results from $15 \times 15\,\mu\mathrm{m}^2$ pixels with an $8\,\mu$m epitaxial layer thickness. The charge is mainly confined within a $3 \times 3$ pixel array. One of the goals of our proposal is to determine the optimum size of the pixels to maximize the charge collection. Pixels could be bundled together and their charge fed to a single comparator that could have a threshold. The threshold would be common to the chip or to area of the chip, but we will also investigate the need to have a single comparator threshold adjustment.

In terms of the total number of pixels hit in the ECAL as a whole, then we estimate a rate of $\sim 10^{-2}$ hits above threshold per pixel per bunch train. These are due to both noise and beam-related background in the ECAL.

(d) *As charge is collected by diffusion the charge collection efficiency is sensitive to the diffusion length which is altered by irradiation.* $10^{12}$ *hadrons cm*$^{-2}$ *or* $10^{13}$ *electrons (above 10 MeV) cm*$^{-2}$ *would reduce the electron diffusion length to 25 microns and start to affect the signal size. The radiation levels at ILC are significantly less than at LHC, but what are they in the calorimeter, and does this matter?*

This was discussed in our written reply to Referee 2 and some results are shown in the backup slides 30 and 31 of P.D.Dauncey's talk. MAPS do show some effects after $10^{12}$ hadrons cm$^{-2}$ but have been shown [2] not to degrade seriously up until $10^{14}$ hadrons cm$^{-2}$. The rates expected in the ILC ECAL are much lower; rates of around $10^9$ (worse case $10^{10}$) hadrons cm$^{-2}$ per year are predicted. Similar fluxes for electrons are also expected.

Note, MAPS are being discussed both for the ILC vertex detector (where rates are expected to be at least one order of magnitude higher than in the ECAL) and also for SLHC applications, where rates will be orders of magnitude higher again. We believe radiation hardness is not one of the critical issues for the ECAL application which needs to be studied by us within the period of the proposal.

(e) *Is ref. [30] available ? [Internal LC-Note from PDD describing the MAPS concept] What feedback has the UK received from CALICE collaborators about this idea?*

Reference [30] of the Case For Support has been included with this submission. It could have been supplied to the referees before they wrote their reports if the request had been forwarded to us by the PPRP secretariat.

This is a working document, acting as a repository of ideas within the ECAL MAPS group. Hence, as well as containing a description of the MAPS concept and etimates of data rates, it also lists the issues which need to be addressed. This is the basis for the items we wish to study through this proposal.

In our written reply to Referee 1, we stated that the whole proposal, including of course the MAPS part, was presented by M.Wing at the CALICE collaboration meeting in DESY on 8 December 2004 and we got useful feedback. In addition, the letter submitted to the PPRP by J.-C.Brient, the CALICE Spokesperson, shows he is aware and supportive of the proposal.

2. *Please provide a summary of the key results from existing work on MAPS that convince you the approach is viable for calorimetry. Also more detail on the simulation used for initial studies, e.g. Figs 6 and 7 in the proposal.*

The key results have been mentioned above in answers to questions 1b and 1c. Reference [2] is a good recent summary of the status of the work from the MAPS collaboration. A list of further references can be found at [4].

We would like to correct the impression which might have resulted from the discussion in the closed session that MAPS are in some way an unproven technology. MAPS which demonstrate clear MIP signals have been around for several years. An early paper in 2001 from the Strasbourg group [5] (which includes R.Turchetta as an author) demonstrated very high efficiency ($99.5 \pm 0.2\%$) for charged particles with a $15\,\mu$m epitaxial layer, which is the thickness we propose to use (at least for the first sensor fabrication round). It is absolutely incontravertible that MAPS can efficiently detect MIPs; what we are trying to demonstrate is whether they can also be used in an ECAL.

All the above papers are from applications of MAPS to tracking. There are no results on calorimetry use; this is obviously because our application is novel. However, a sampling calorimeter requires only charged particle detection in the sensitive layers and it is already proven that MAPS can do this, so there are no obvious reasons why they could not work well for an ECAL. The simulation certainly indicates this to be the case; as stated in Section 5.2 of the Case For Support and on slide 17 of P.D.Dauncey's presentation, it indicates the number of tracks passing through the sensitive layer is a better estimate of the shower energy than the energy deposited in the sensitive layer. It also shows some improvement in the two-particle shower separation.

The MAPS simulations were based on the Tesla TDR ECAL design. The sensitive silicon layers were changed from $500\,\mu$m to $5\,\mu$m thick (which is thinner than current ideas for MAPS but these particular simulation results should not depend strongly on this). The space left by the silicon was left filled with air and no reduction of the ECAL size to take advantage of the thinner layers was done. The pixel size set to $25 \times 25\,\mu\text{m}^2$ with the pixels ganged together as appropriate for subsequent studies. The model for the energy deposition was the default of GEANT4, with the range cut-off set to $5\,\mu$m to match the pixel thickness. This is equivalent to a cut-off at about 1 keV of energy.

For the linearity/resolution studies, the analogue diode pad version was based on $500\,\mu$m thick pads and the sum of deposited energy (applying a threshold of 0.3 times the MIP peak) was computed. For MAPS, the number of cells with energy deposition greater than 0.3 MIP was taken. However, for the MAPS case, the Landau of the MIP peak is of course broadened considerably; the distribution obtained from GEANT4 is consistent with the plot shown on slide 21 of P.D.Dauncey's presentation, indicating that this part of the simulation is reasonable. In applying these thresholds the MIP value for MAPS was taken to be 0.01 times that for the analogue; in consequence the cut was in fact at about 0.5 times the peak position for MAPS, i.e. the comparator was assumed to be set to around 50% of the most probable value.

For the two-particle resolution studies, the standard Cambridge clustering code (tuned on the analogue design) was run as is; just the MIP threshold was adjusted, and the response recalibrated. No attempt to retune the algorithm was made.

3. *Why is it necessary to start sensor design now? What would be the consequence of a 6-12 month delay? Could you develop the MAPS concept in useful directions in the interim, e.g. with more detailed simulation?*

   We believe it is critical to have put MAPS sensors in a calorimetry beam test before they can be accepted as a viable option for the ECAL. The schedule for development in the proposal is not relaxed but does provide this crucial test in the third year. This would be a year before the TDR is written and so would give time for analysis and presentation of the beam test data to the ILC community. The effect of a delay is then clear; six months delay would make completion of the analysis difficult to achieve in time for the TDR (and would be more risky in terms of schedule slip). A one year delay would mean we would only start taking data around the time of the TDR submission.

   There is a significant amount of simulation work to be done for MAPS. However, we have already scheduled this in parallel with the sensor design itself during the first year of the proposal so as not to delay the project. In addition, this detailed work needs dedicated effort; the Imperial RA-2 will do these studies and has 5 SM of effort assigned to this in the first year. We do not currently have this level of effort available among the academic staff involved. Hence, we would still need the RA even if the project was delayed to do more simulation.

Finally, the simulation needs to be guided by MAPS-specific studies, preferably from real data but also from device-level simulations, as foreseen to be done by E.G.Villani. Otherwise, we cannot be sure whether the simulation is modelling the response of the sensors correctly. The discussion in the closed session concerning the example of a possible large number of low energy photons shows that there could be effects which do not occur in the simulation but which could make a critical difference to the performance of the sensors. Hence, there is only a limited amount which can be done longer term through simulation and experimental input will always be needed for a real decision on viability.

4. *On WP3 (MAPS), the Panel would like to see the work programme presented with some explicit staging. Ideally one would identify a decision point after O(12) months where work could be stopped if the MAPS technology is shown to be non-viable either for technical or managerial/political reasons. It is expected that funding approval would be requested for the full 36 months, so that securing the release of the second tranche of funds after the break point would not require a full bid; a favourable report from the Oversight Committee might be sufficient.*

   Staging the programme as described would be perfectly viable for us in principle as it would not introduce further delays. However, there are two issues which will cause practical problems.

   We cannot (legally) hire RAs for longer than the money is committed. Hence, with a checkpoint each year we would have to hire them for one year at a time. This could mean they would not be of the calibre we would hope for and would make the positions more difficult to fill. In addition, the Birmingham RA-1 and Imperial RA-2 posts are shared with other workpackages and this potential lack of continuity would be disruptive for the work there. We believe realistically it is necessary to hire people for a minimum of two year periods. Hence, one possibility might be to have a checkpoint only after two years. An alternative would be to fund the RAs in full for the period of the proposal (as they are needed for the other workpackages anyway) and only decide whether to continue with the rest of Workpackage 3 during the annual reviews. The RA costs in the second and third years total £182k out of the total Workpackage cost of £944. Even if the MAPS work was thought not worth pursuing beyond the first year, then the RAs would be extremely valuable. There is a major scope for enlargement of their analysis and simulation work in both Workpackages 1 and 5, where we are completely effort-limited; there are no other significant resource implications as this work would require no extra equipment. Hence, the UK would be able to produce more results in both these areas in this (we hope pessimistic) scenario.

   The other problem with a checkpoint after one year is that there would be very little to review, given the the schedule proposed. The sensor design will continue for the first 13 months, with the first round of sensors coming back after 17 months. Hence, there will be no concrete results from real sensors within this time. The other work in the first year is the MAPS simulation studies where, within a year, results on the relative importance for physics performance of crosstalk, S/N, etc, should be available. However, until the actual sizes of these effects are known, this still does not allow anyone to judge whether the concept is viable or not. Also, as stated above, there will still be some doubt about the degree to which the simulation is realistic. Clearly the review could judge whether the work is progressing well, but there would be effectively no new information on whether MAPS is a viable concept for an ECAL one year from now.

5. *The panel also raised the question as to whether any studies, in particular beam tests, could be done using existing sensors from the previous MAPS collaboration and/or MI*$^3$.

Given the overlap between CALICE and the other two groups, then there is clearly some room for cooperation. A Liverpool group within the MAPS collaboration has just finished a beam test at DESY. This used similar sensors to the ones for which results were shown on slide 21 of P.D.Dauncey's presentation. However, their studies were for a vertex detector application and so did not involve EM showers. Hence, unless there is a major upset, we assume they will observe a similar signal/noise and so we will not learn anything new for the ECAL application. In fact, following the comments from the PPRP closed session, we contacted the people running these tests and asked if it would be possible to do a quick test of one of their sensors behind several radiation lengths of lead. Unfortunately, while they were very willing to do this, they were not able to schedule the test within the restricted period of their beam time.

If we were to do a beam test ourselves of an existing MAPS sensor then we could do this test within a shower. However, it is not clear how much would be learned even then; the sensors are around $5 \times 2\,\mathrm{mm}^2$ so the shower is not fully contained within them, making it hard to understand what is going on. Even then, the sensor is subdivided into several $1 \times 1\,\mathrm{mm}^2$ blocks of different designs with different efficiencies, etc, meaning interpretation is made more difficult. Furthermore, the pixel size and epitaxial layer thickness are quite different from our application. Such a beam test would necessarily involve purchasing equipment for readout which would not be applicable to the ECAL sensor designs as the existing sensors are analogue, not binary. It addition, it would divert effort away from sensor design and/or simulation in the first year. We did not consider the potential payback from such a test to be worth the extra resources needed. However, if the PPRP considers this essential and can provide the extra resources, we will of course undertake this test.

As stated in slide 18 of P.D.Dauncey's talk, we will have access to a few sensors of the $\mathrm{MI}^3$ work by J.Crooks. These will have an on-pixel comparator and memory together with a readout bus. This will be useful for evaluating the digital circuit functionality but will not provide much information on the analogue parts of the sensor.

# 4 Workpackage 4

1. *Can you strengthen the justification for undertaking this work now? What is really needed for the 2009 TDR? In particular, why is work on assembly robots required now?*

   The construction of a Si-W high granularity calorimeter entails the mass production of detector systems which is far beyond current established practice. Similar calorimeters have been constructed as forward luminosity detectors for the LEP experiments, and were assembled with individual care and attention by experts. CALICE is proposing to extend the scale four orders of magnitude, from $\mathrm{cm}^2$ to $\mathrm{m}^2$. There will also be increased demands on reliability due to inaccessibility.

   Clearly, by the time of the TDR we have to be confident that we can build this device, and that we can build it to specification in positioning and reliability, and in an sufficiently automated way to keep labour costs reasonable. It may be that we can get it built by industry, but even in that case we would certainly have to do the R&D ourselves. We cannot do this just by scaling up experience from the LEP Si-W construction.

   We are not proposing to have a full scale assembly line ready by 2009. We want to do enough R&D to understand the problems that will be encountered in setting up such an assembly line, and inform the construction criteria and schedules that go into the TDR. To speak of "robots" is perhaps exaggerated: we mean the prototyping of semi-automated

("robotic") systems which will provide the proof of principle needed to let us propose a system which can actually be built on a reasonable budget within a reasonable timescale.

The activity level on this is low, as can be seen from Annex A3 of the Case For Support. By doing the work over a longer period, rather than in a rush at the end, we are better able to match the evolving design. By starting thinking and consulting about this now, we can get established within the collaboration as the experts on this topic, and will be well placed to take a leading role in future. Some assembly of future prototypes will enable us to learn from experience and will also raise our profile.

A continuing schedule also enables us to keep the existing Manchester (ATLAS) assembly team in practice, and ensure the equipment we intend to convert to CALICE use is not lost to other projects.

We point out that the resources being requested for this are minimal in both equipment and staff costs, and that the staff costs involved are on the rolling grant and do not entail any new expenditure for PPARC. Also, all effort to be transfered from ATLAS has been approved by the ATLAS-UK management.

## References


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