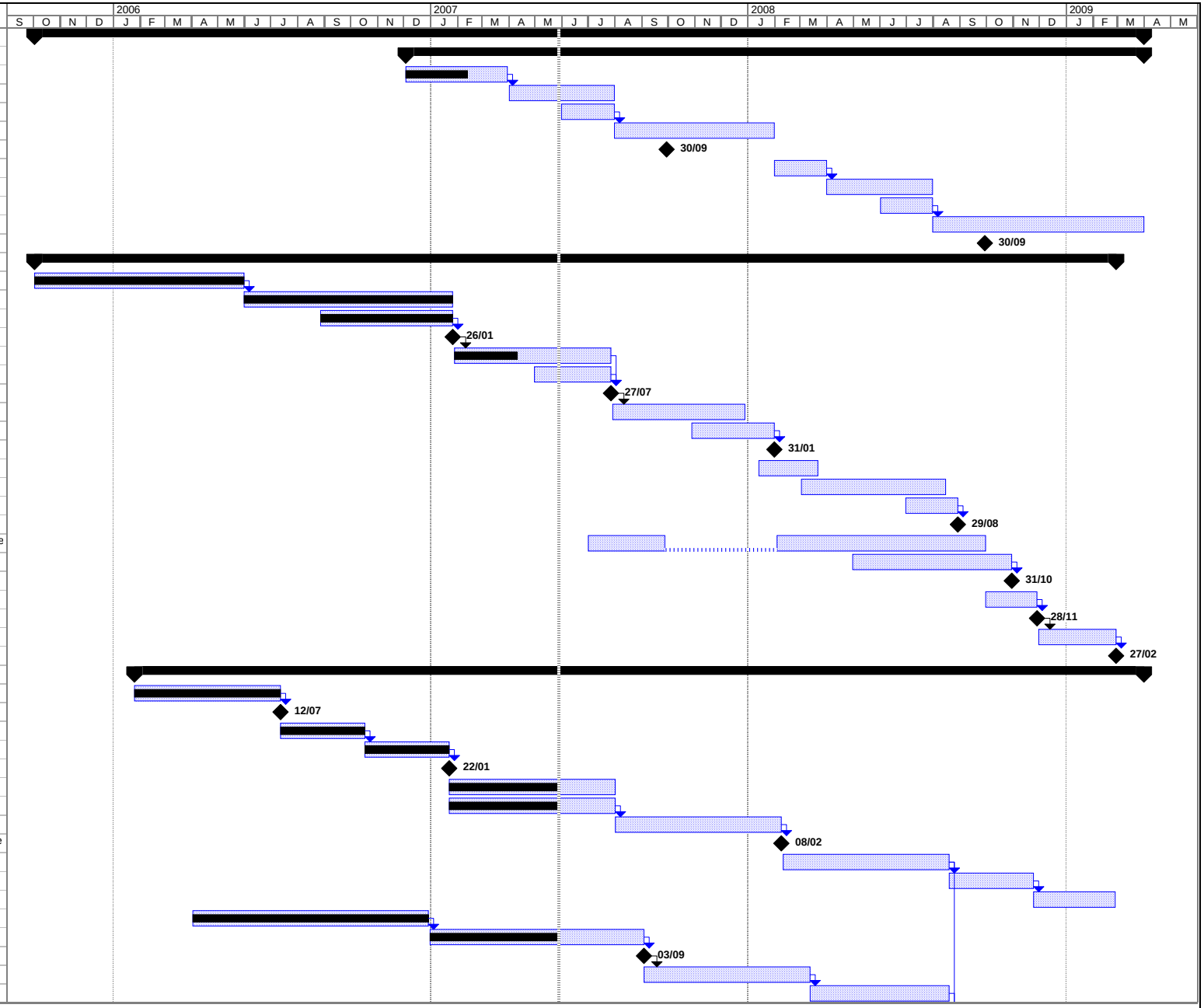
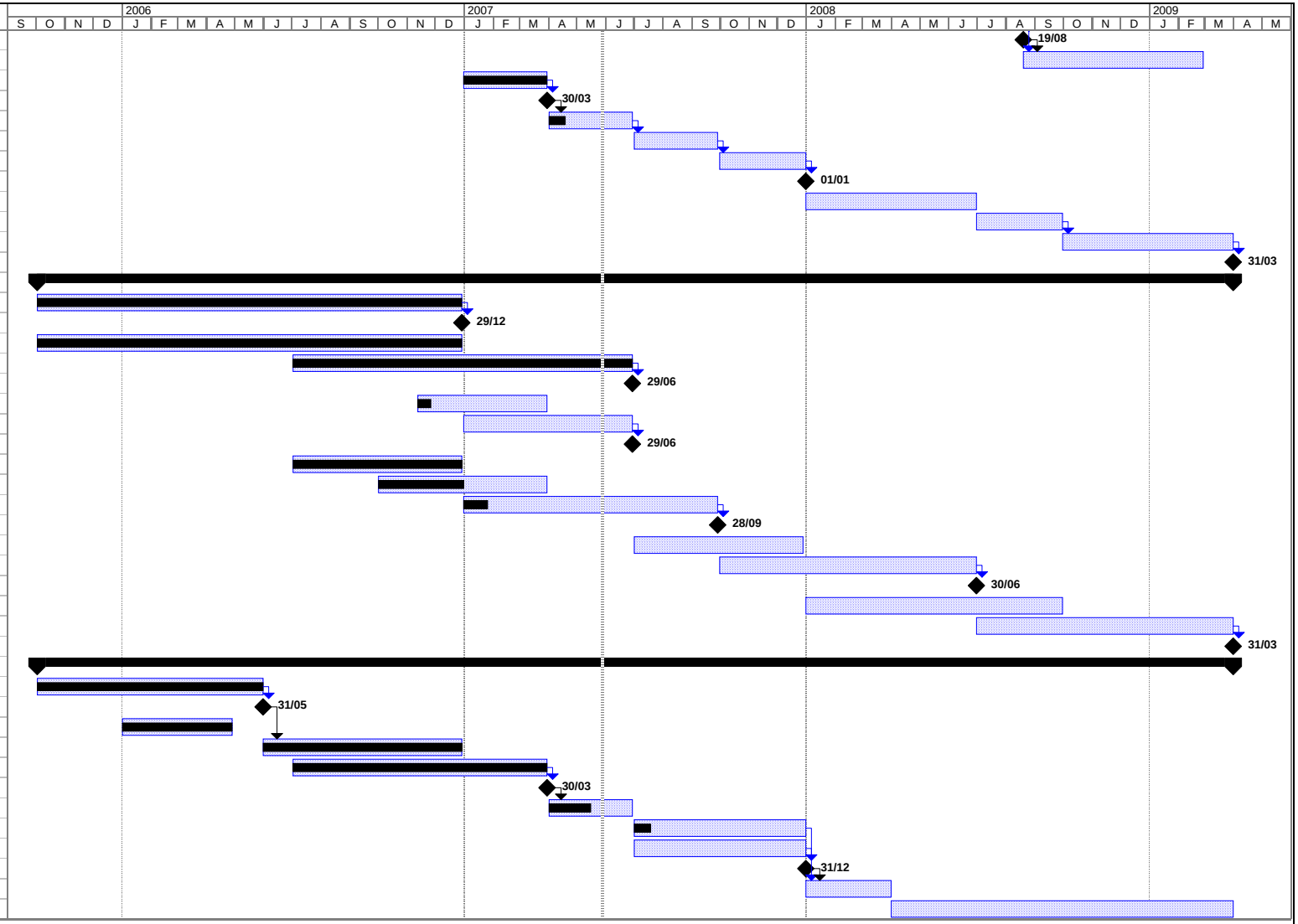
ID	Task Name
1	**CALICE WP2 - M. Wing (UCL)**
2	**Readout of prototype VFE ASICs**
3	Prepare ASIC test DAQ
4	Test single ASIC PCB phase 1
5	Design and fabricate PCB phase 1
6	Readout ASICs in bulk phase 1
7	Successful readout of 2007 ASICs
8	Upgrade ASIC test DAQ
9	Test single ASIC PCB phase 2
10	Design and fabricate PCB phase 2
11	Readout ASICs in bulk phase 2
12	Successful readout of 2008 ASICs
13	**Study of data paths over 1.5m slab**
14	Preliminary design study and preparation
15	Test Panel 0 design, fabrication and commissioning
16	FE board 0 design, fabrication and commissioning
17	Test bench 0 hardware ready and commissioned
18	Test bench 0 + host PC tests and measurements
19	Results analysis concepts definition for phase 1
20	Concepts established for 1.5m data path
21	Test panel 1 design, fabrication and commissioning
22	FE board 1 design, fabrication and commissioning
23	Test bench 1 hardware ready and commissioned
24	Test final timing and slow control implementation
25	Test and measure performance of multi-slab readout
26	Test 1 complete; define remaining issues and tests
27	Realistic design of VFE system established
28	System integration with DAQ and LAL multi-ASIC pane
29	Beam tests including radiation tolerance
30	TFE design finalised
31	Decide on design concepts and technology
32	Freeze VFE system design
33	Write report for DAQ section in TDR
34	Complete draft of TDR section
35	**DAQ Networking**
36	FPGA to 1 Gig ethernet firmware development
37	FPGA 1 Gig Ethernet MAC firmware complete
38	1Gb data transfer tests
39	1Gb FPGA to multiple destination network tests
40	Report on FPGA ethernet work
41	Generic data source development
42	Re-package generic input data as ethernet
43	Data Multiplexing
44	Report on suitability of FPGAs for real-time data conve
45	10Gb daughterboard development
46	10Gb bandwidth tests
47	10Gb networking and routing tests
48	Set up 10Gb lab
49	Bandwidth tests of commercial components
50	Component selection
51	Component acquisition and system build
52	10Gb system tests



Project: WP2
Date: Mon 28/05/07

Task | Progress | Summary | External Tasks | Deadline
Split | Milestone | Project Summary | External Milestone

ID	Task Name
53	Report on 10Gb performance
54	Networking tests with FPGA data source
55	Survey of optical switches available
56	Acquire optical switch
57	Build network test rig using optical switch
58	Evaluate network performance
59	Re-evaluate performance with switching
60	Demonstrate optically switch network
61	Build busy signal
62	Develop trigger interface
63	Develop automatic switching system
64	Delivery of busy system
65	**Transport of configuration, clock and control data**
66	Simulate radiation environment at FE
67	Present simulation results
68	Literature search for expected problems
69	Design prototype board and test system
70	Make proposal for robust/flexible test system
71	Design remote configuration hardware
72	Expand hardware to multiple units
73	Demonstrate remote FGPA reset and reconfigure
74	Define clock and trigger requirements
75	Design/prototype clock extraction system
76	Adapt remote configuration hardware
77	Demonstrate system lock from data interface
78	Evaluate jitter
79	Evaluate use of commercial hardware fanout
80	Demonstrate trigger (and C + C) fanout
81	Build large system
82	Design required interfaces
83	Demonstrate workability from single trigger source
84	**Prototype off-detector receiver**
85	Investigated latest PCI technology
86	Buy PCI cards
87	High level system design
88	Produce prototype firmware
89	Write system software
90	Initial prototype complete
91	Tests of initial prototype
92	Enhancements - s/w to h/w for speed improvements
93	Enhancements - data to pseudo-file format
94	Initial system complete
95	Tests of initial system
96	Build and test full-scale system



Project: WP2
Date: Mon 28/05/07

Task | Progress | Summary | External Tasks | Deadline
Split | Milestone | Project Summary | External Milestone