On- and near-detector DAQ work for the EUDET calorimeters

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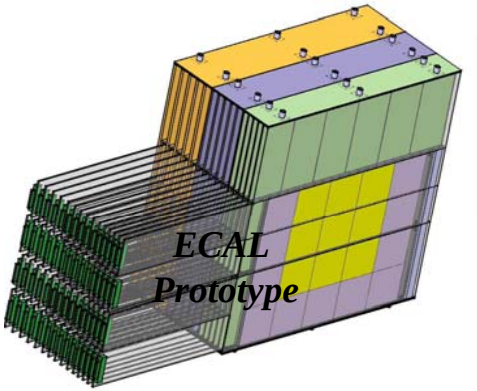
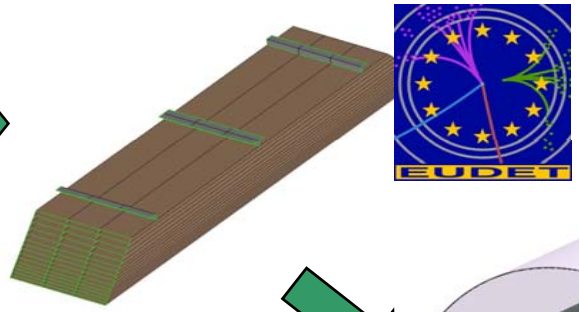
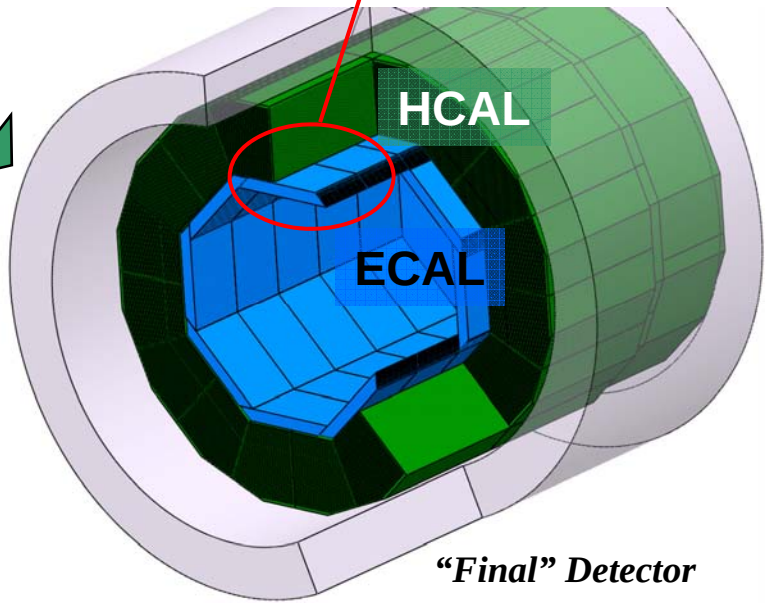
ILC Calorimeter





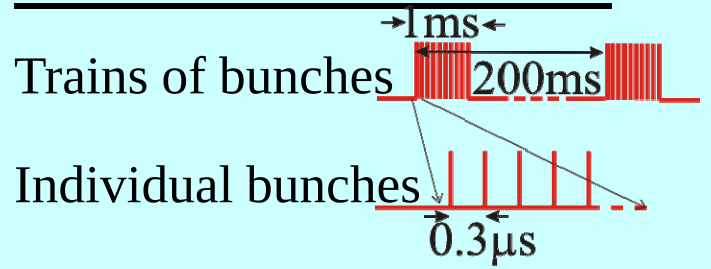


- ILC Calorimetry will use particle flow algorithms to improve energy resolution
  - => 1cmx1cm segmentation results in 100M channels with little room for electronics or cooling
- Bunch structure *interesting:*
  - ~200ms gaps between bunch-trains
  - Trains 1ms long, 300ns bunch spacing
- Triggerless

=> ~250 GB of raw data per bunch train need to be handled

M. Anduze

Time structure of bunches

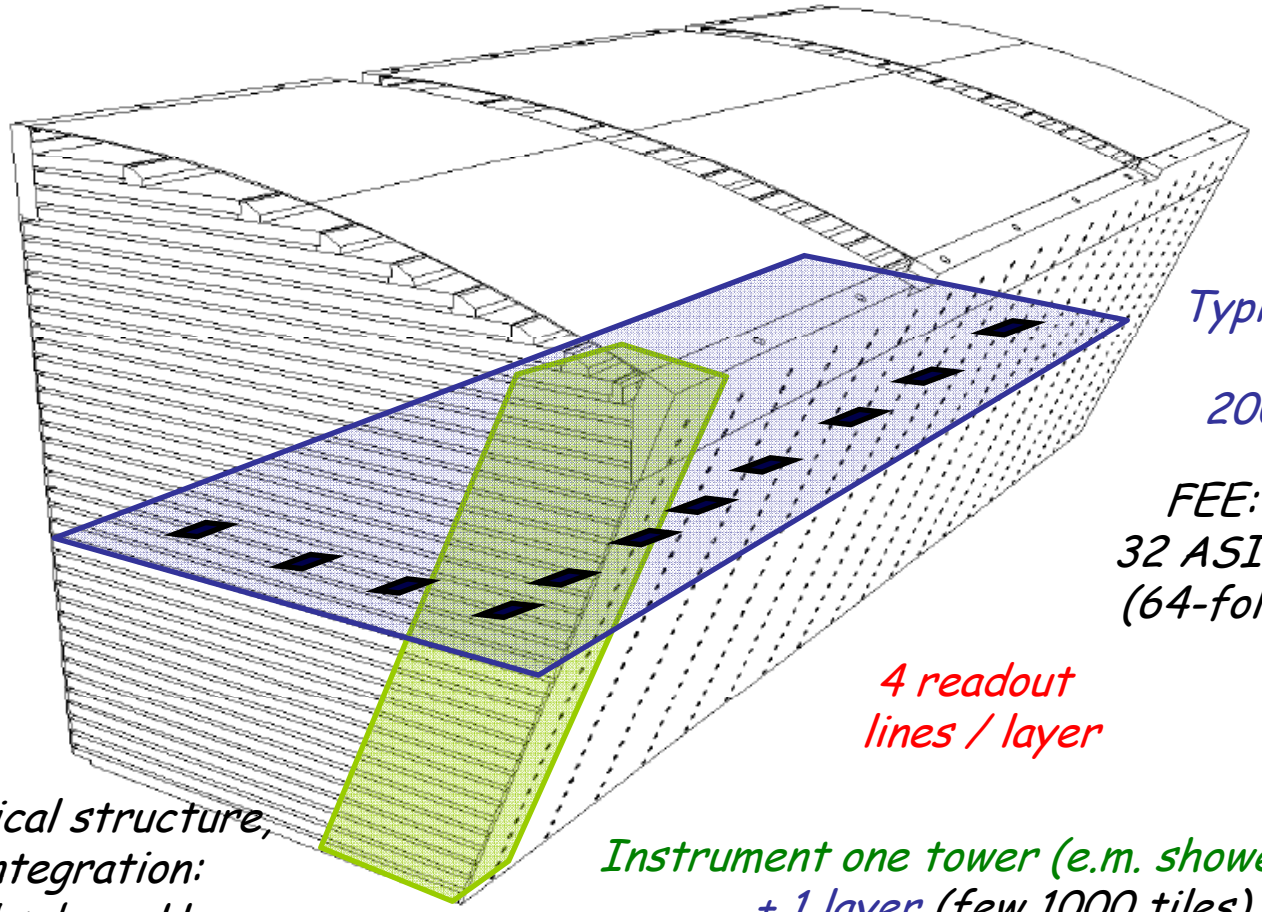


Objectives

- Utilise off the shelf technology
  - Minimise cost, leverage industrial knowledge
  - Use standard networking chipsets and protocols, FPGAs etc.
- Design for Scalability
- Make it as generic as possible
  - exception: detector interface to several subdetectors
- Act as a catalyst to use commodity hardware

⇒ **build a working technical prototype (to verify assembly, mechanical structure) and DAQ system to be used for prototype by 2009**

EUDET prototype (example AHCAL)



38 layers
80000 tiles

Typical layer
2m²
2000 tiles

FEE:
32 ASICs
(64-fold)

4 readout
lines / layer

***EUDET**: Mechanical structure,*
electronics integration:
DESY and Hamburg U

Instrument one tower (e.m. shower size)
+ 1 layer (few 1000 tiles)

- 3 different detector types: ECAL, AHCAL, DHCAL
- study of full scale technological solutions

DAQ architecture

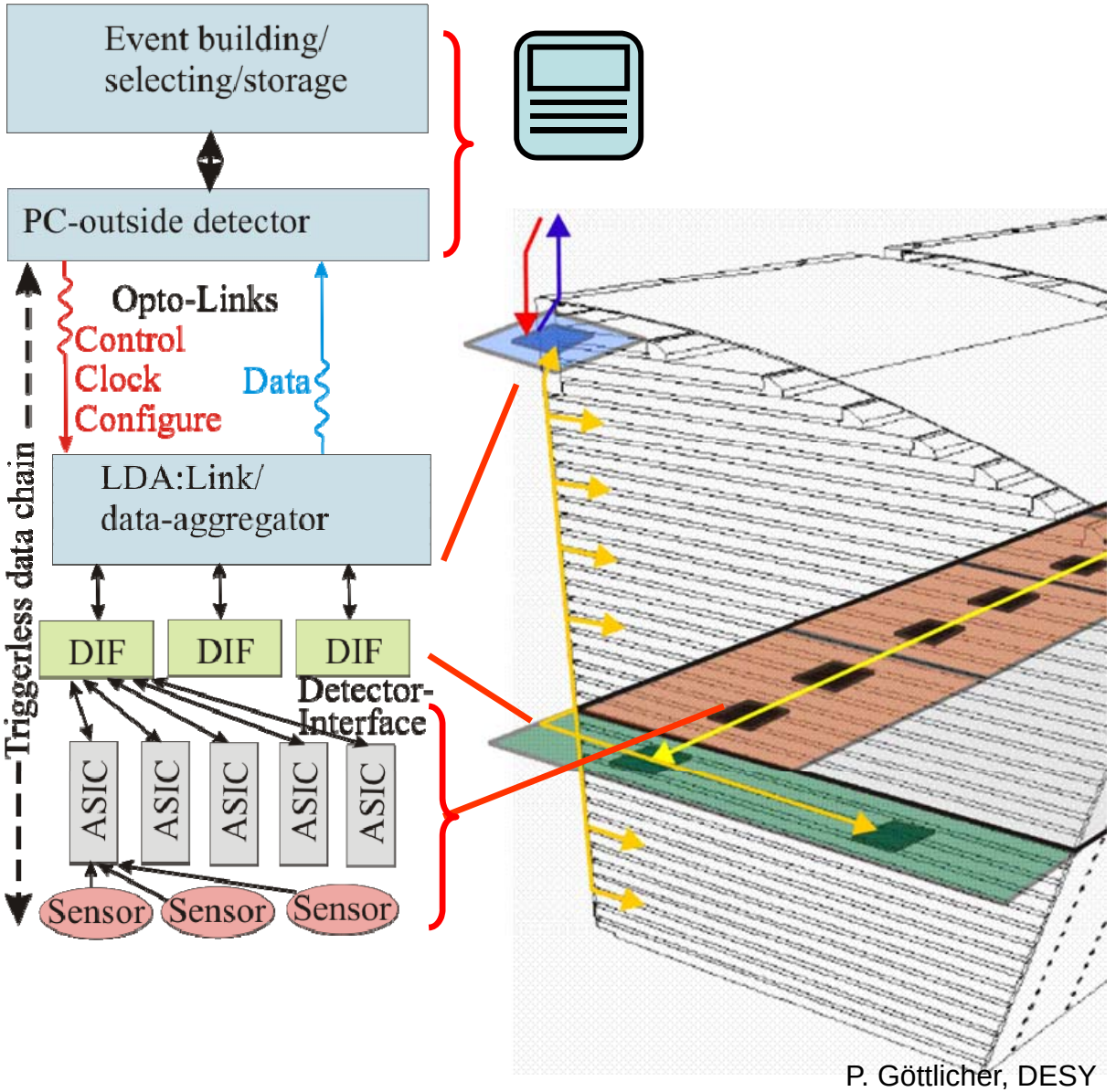
DAQ software

Off Detector Receiver (ODR)

Link Data Aggregator (LDA)

Detector Interface (DIF)

Detector Unit

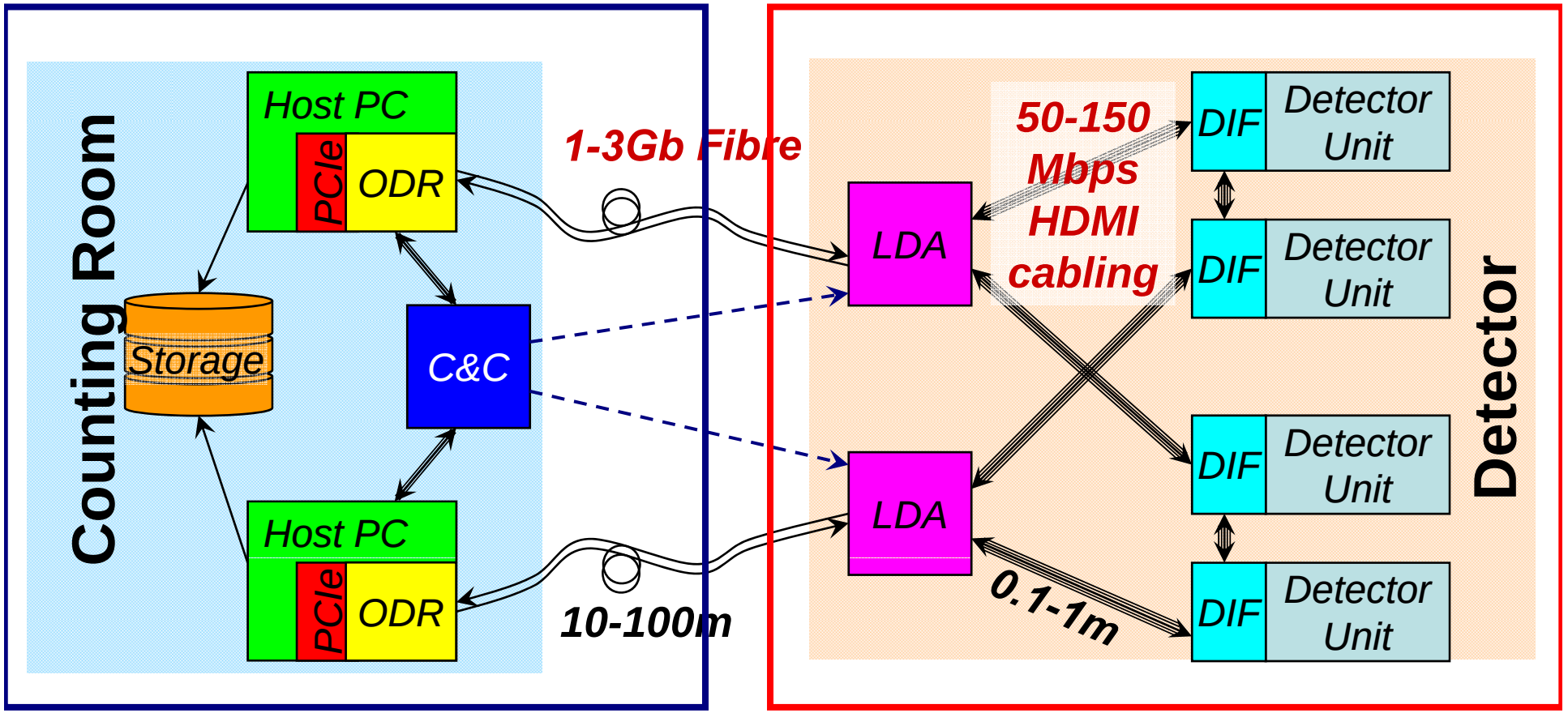


P. Göttlicher, DESY

DAQ architecture

covered in Tao's talk

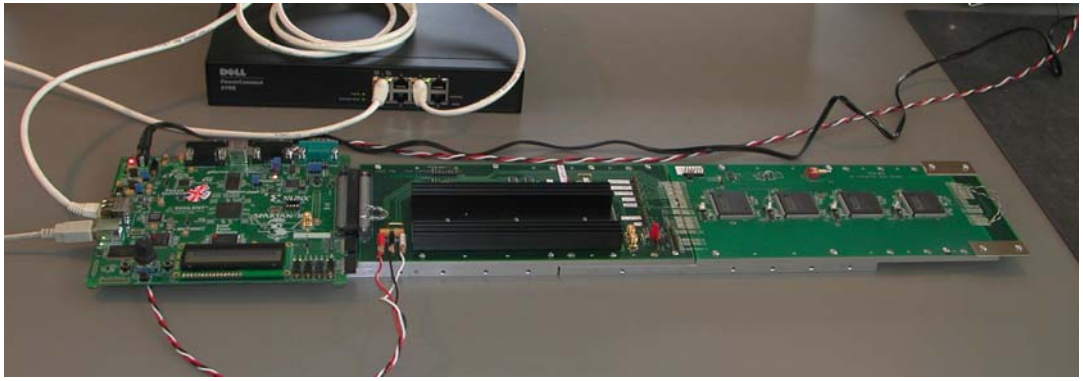
covered in Valeria's talk

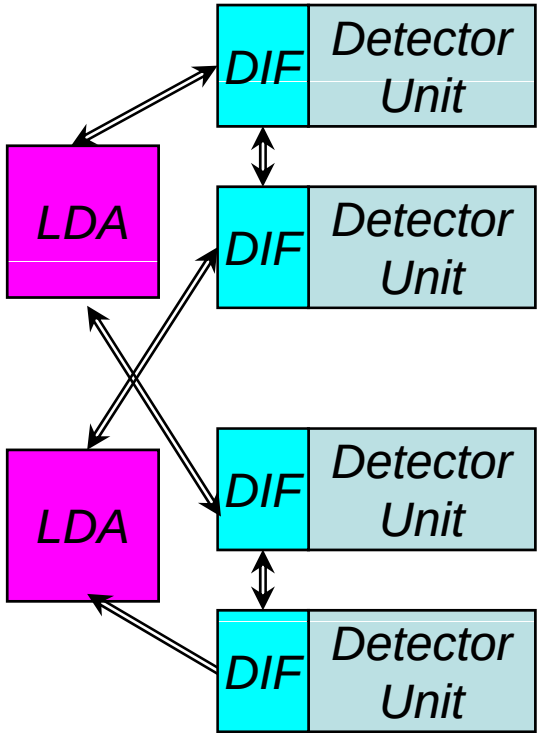


Detector Interface (DIF) status

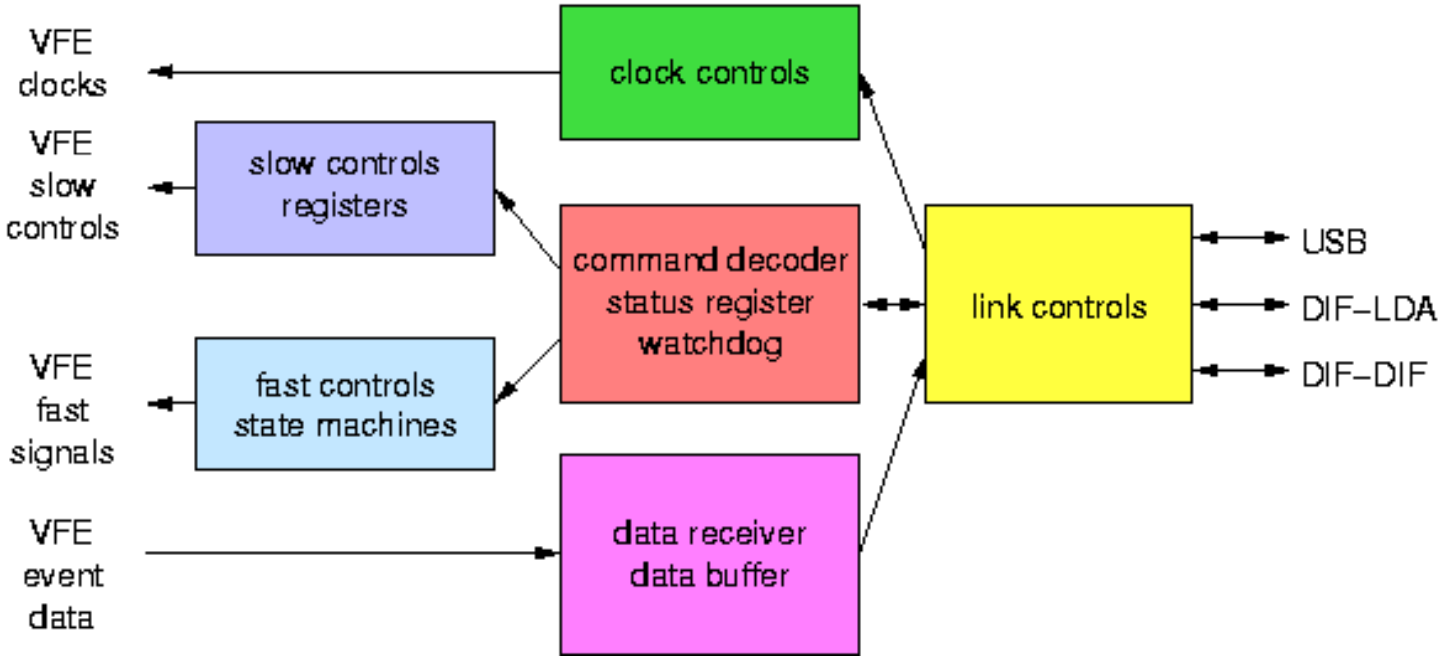
- Two halves – Generic DAQ and Specific Detector
  - 3 detectors: ECAL, AHCAL, DHCAL
  - 1 DAQ Interface!
- Transmits configuration data to the Detector Unit and transfers data to downstream DAQ
- Designed with redundancies for readout
- Signal transmission along ECAL test slab

and ECAL slab interconnects being tested





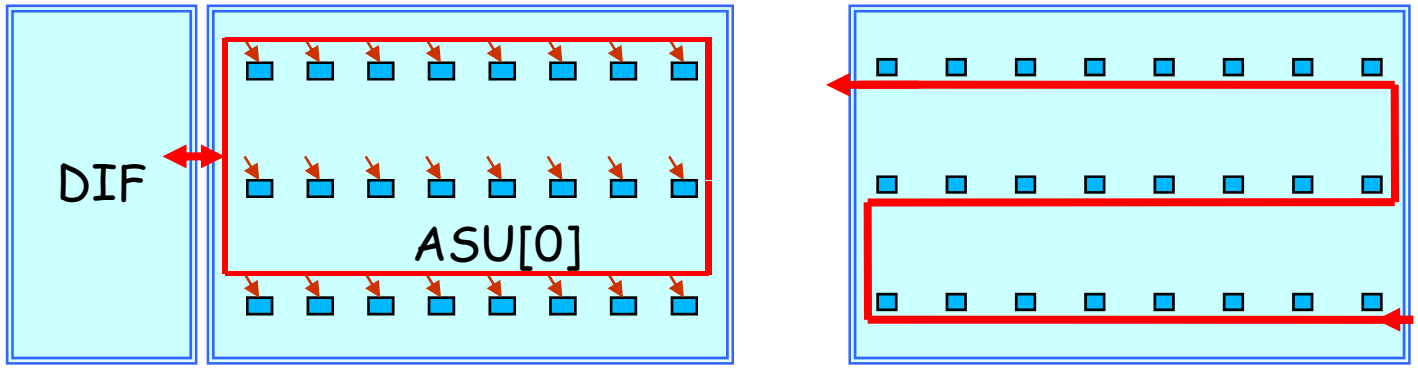
Detector Interface (DIF) status



- keep DIF simple hence predictable (no local ‘memory management’, for example)
- DIF proto: large Xilinx FPGA, to be slimmed down for final DIF
- board is delivered

ECAL slab interconnect

- geometry investigated (multi-rows preferred)

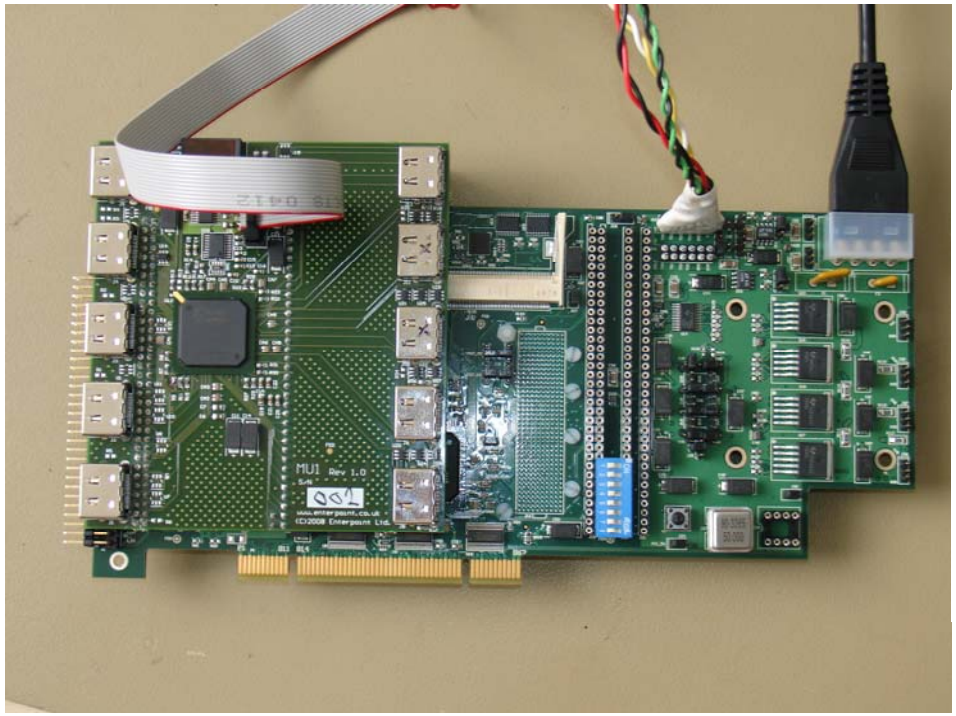


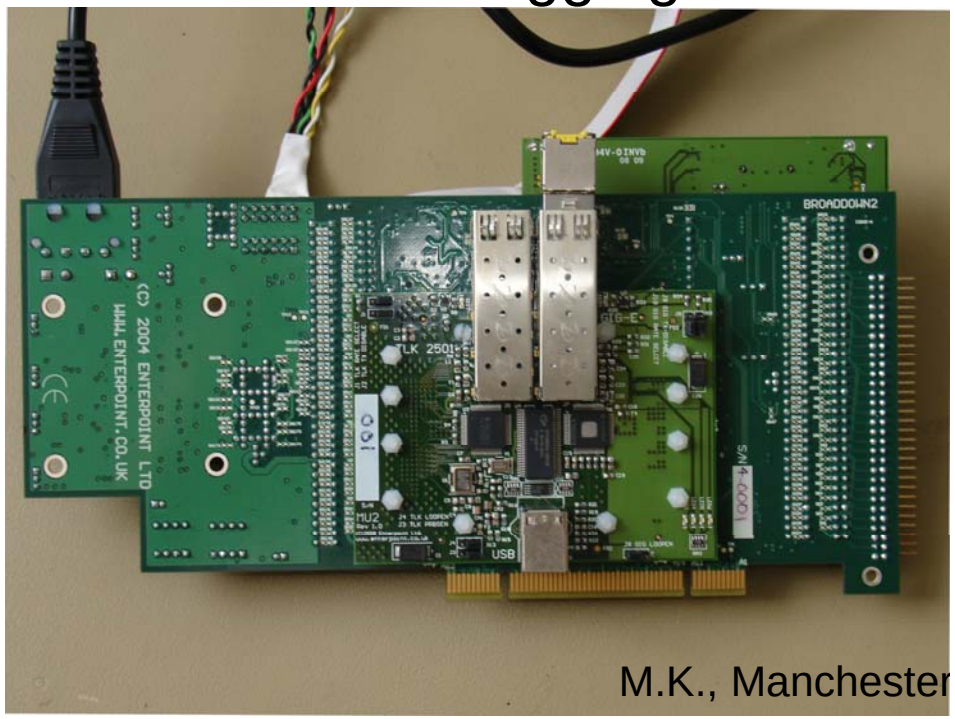
- technology: conductive adhesive vs. flat flexible cable (FFC), with preference to FFC
- soldering technologies are being investigated (Hot-Bar soldering, laser soldering, IR soldering)

Link Data Aggregator (LDA)

Hardware:

- PCBs designed and manufactured
- Carrier BD2 board likely to be constrained to at least a Spartan3 2000 model
- Gigabit links as shown below, 1 Ethernet and a TI TLK chipset
- USB used as a testbench interface when debugging





M.K., Manchester

Link Data Aggregator (LDA)

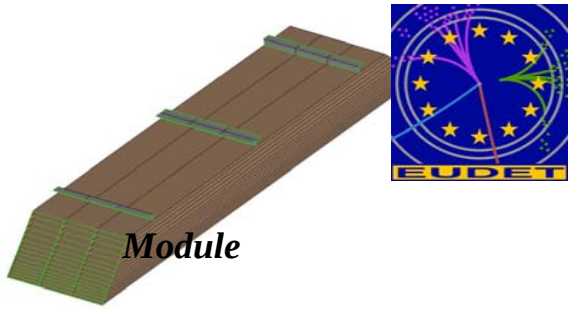
Firmware:

- Ethernet interface based on Xilinx IP cores
- DIF interface based on custom SERDES with state machines for link control. Self contained, with a design for the DIF partner SERDES as well
- Possible to reuse parts from previous Virtex4 network tests
- No work done on TLK interface as of yet

1 Link Data Aggregator can serve 8 Detector Interfaces

- Might not be enough for DHCAL => 2nd prototype will be designed

Summary

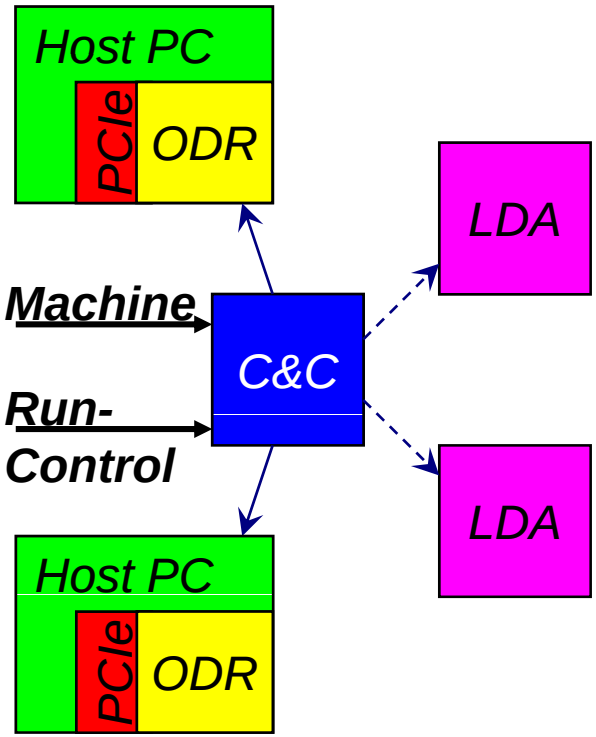


• testbeam for the EUDET module in 2009

• prototypes of all hardware components
(Detector Interface, Link Data Aggregator and
Off Detector Receiver) built and tests started
⇒ Debugging and improving of each component before putting the components together

Backup slides

Clock and Control (C&C) board

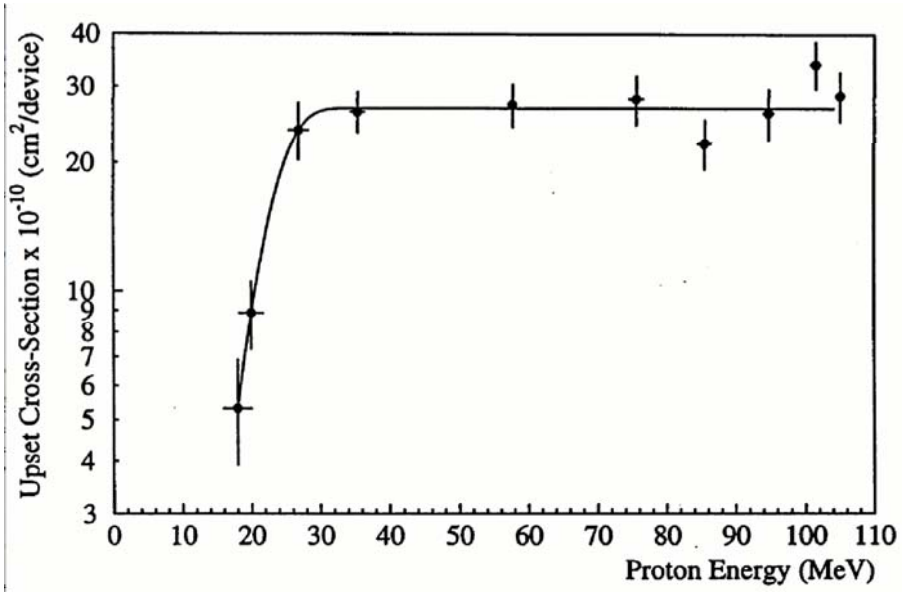


- C&C unit provides machine clock and fast signals to 8x Off Detector Receiver/Link Data Aggregator.
- Logic control (FPGA, connected via USB)
- Link Datas Aggregator provides next stage fanout to Detector Interfaces
  - Eg C&C unit -> 8 LDAs -> 10 DIFs = 80 DUs.
- Signalling over same HDMI type cabling
- Facility to generate optical link clock (~125-250MHz from ~50MHz machine clock)

Board is already designed, will be build soon

Single Event Upset (SEU) Study

finalised, accepted by NIM



SEU cross section depending or

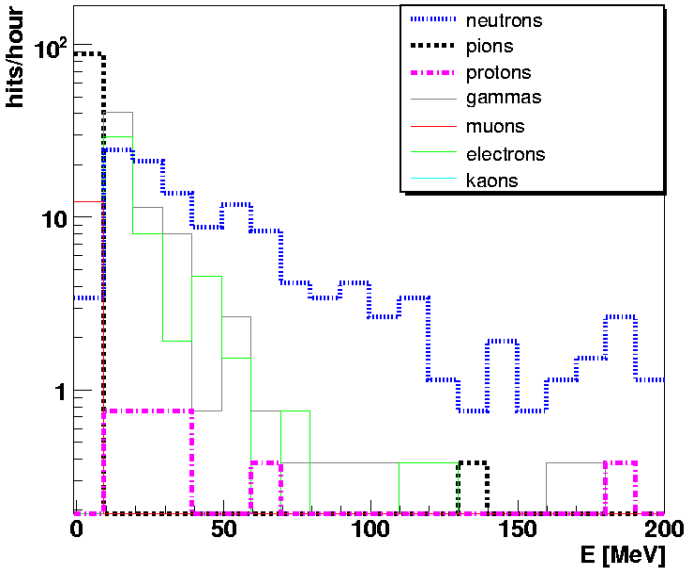
- FPGA type
- traversing particle (n,p,π)
- energy of traversing particle

=> need to study particle spectra

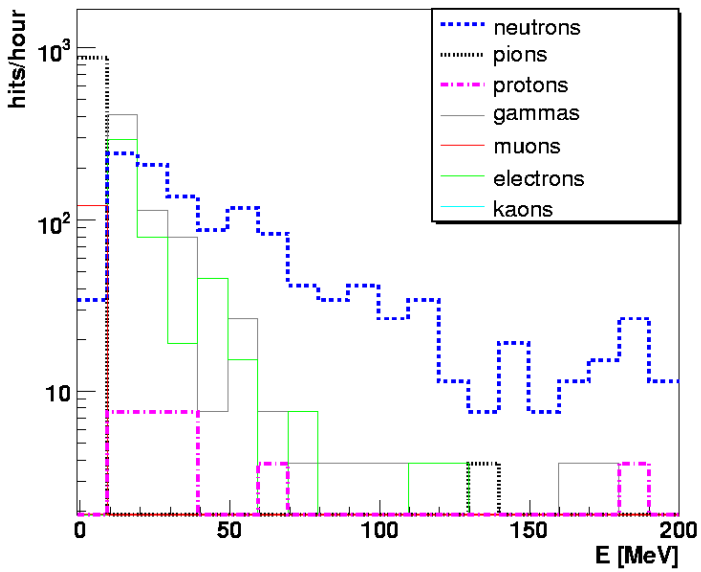
Single Event Upset (SEU) Study

Main backgrounds: (tt, WW and bhabha scattering also studied)

$\gamma\gamma$ (from beamstrahlung) -> hadrons



QCD events



$\Rightarrow$ SEU rate of 14 min-12hours depending on FPGA type for the whole ECAL, needs to be taken into account in control software

$\Rightarrow$ fluence of $2*10^6$/cm per year, not critical

$\Rightarrow$ radiation of 0.16Rad/year, not critical

$\Rightarrow$ occupancy of 0.003/bunch train (not including noise)