
Digital ECAL: Lecture 2

Paul Dauncey
Imperial College London

DECAL lectures summary

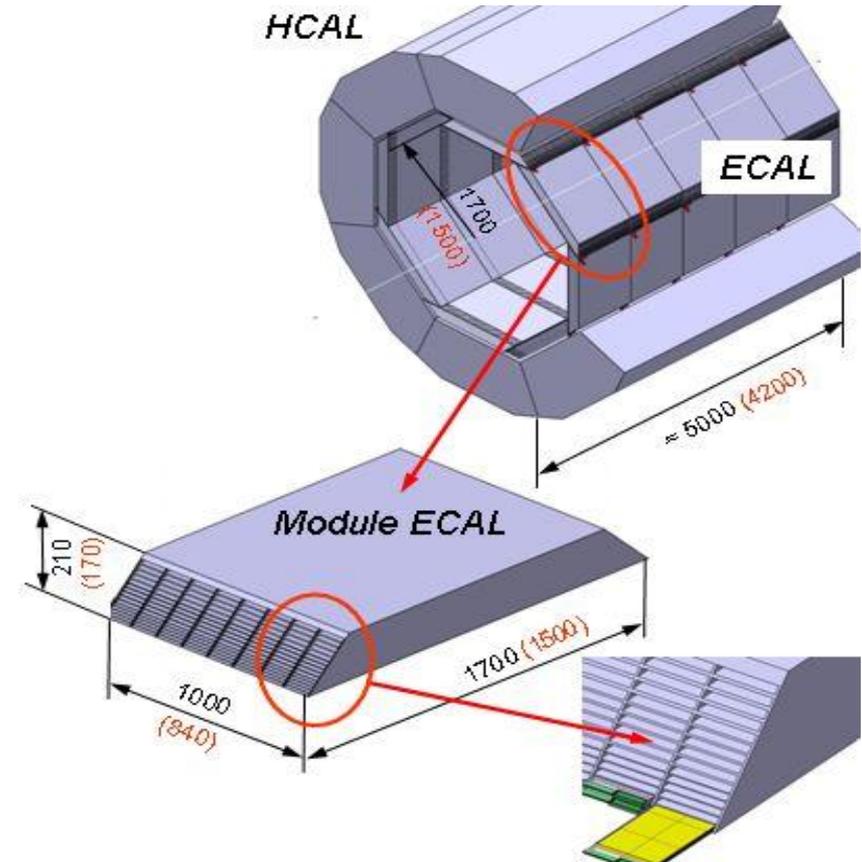
- **Lecture 1** – Ideal case and limits to resolution
 - Digital ECAL motivation and ideal performance compared with AECAL
 - Shower densities at high granularity; pixel sizes
 - Effects of EM shower physics on DECAL performance
- **Lecture 2** – Status of DECAL sensors
 - Basic design requirements for a DECAL sensor
 - Current implementation in CMOS technology
 - Characteristics of sensors; noise, charge diffusion
 - Results from first prototypes; verification of performance
- **Lecture 3** – Detector effects and realistic resolution
 - Effect of sensor characteristics on EM resolution
 - Degradation of resolution due to sensor performance
 - Main issues affecting resolution
 - Remaining measurements required to verify resolution

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Basic scale for full DECAL

- Typical ILC SiW ECAL calorimeter
 - 30 layers, each a cylinder of $\sim 5\text{m} \times 10\text{m} \sim 50\text{m}^2$ surface area
 - Total sensor surface area including endcaps $\sim 2000\text{m}^2$ needed
- DECAL sensor aims to be “swap-in” for AECAL silicon
- For DECAL, with pixels $\sim 50 \times 50 \mu\text{m}^2$ i.e. $\sim 2.5 \times 10^{-9}\text{m}^2$
 - Need $\sim 10^{12}$ pixels in total
 - “Tera-pixel calorimeter”



Constraints for implementation

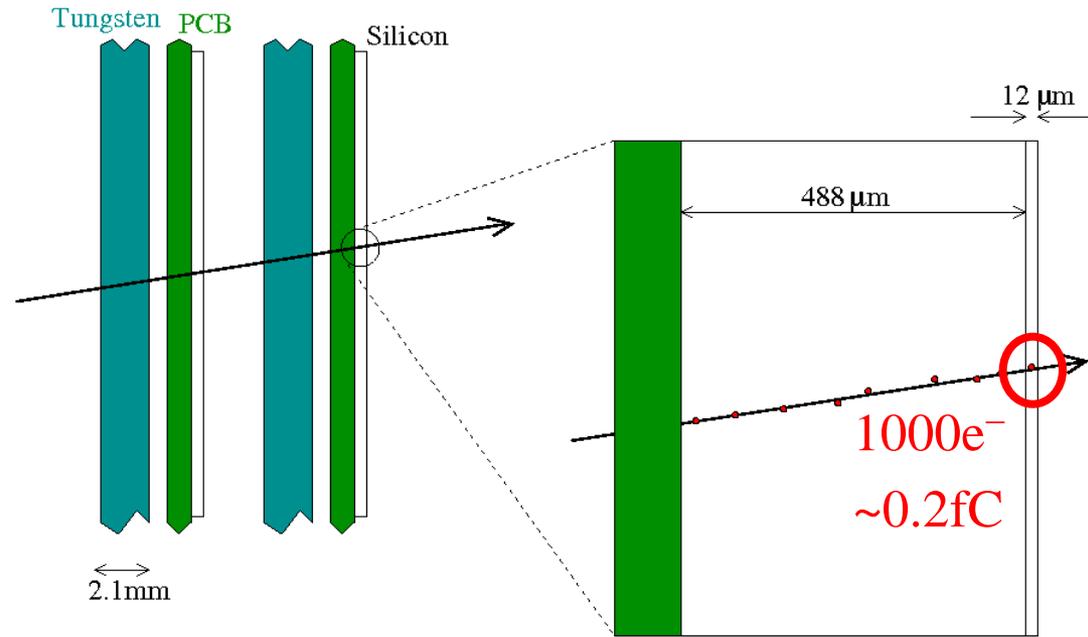
- 10^{12} is a **VERY** large number
- Impossible to consider individual connection for each pixel
 - Needs very high level of integration of electronics
 - Make sensor and readout a single unit
 - “Monolithic active pixel sensor” = **MAPS**
- Difficult to consider any per-channel calibration
 - Even only one byte per pixel gives 1TByte of calibration data
 - Need to have **highly uniform response** of pixels

CMOS as a sensor

- Physical implementation chosen uses **CMOS**
 - C = Complimentary; can implement both p-type and n-type transistors
 - MOS = Metal-Oxide-Semiconductor; type of transistor
 - Since both types of transistor are available, can have complex readout circuit on sensor
- Readout circuitry is all on top surface of sensor
 - Occupies $\sim 1\mu\text{m}$ thickness
- Standard production method as for computer chips, digital cameras, etc.
 - Can be done at many foundries; could be **cheaper** than AECAL sensors!

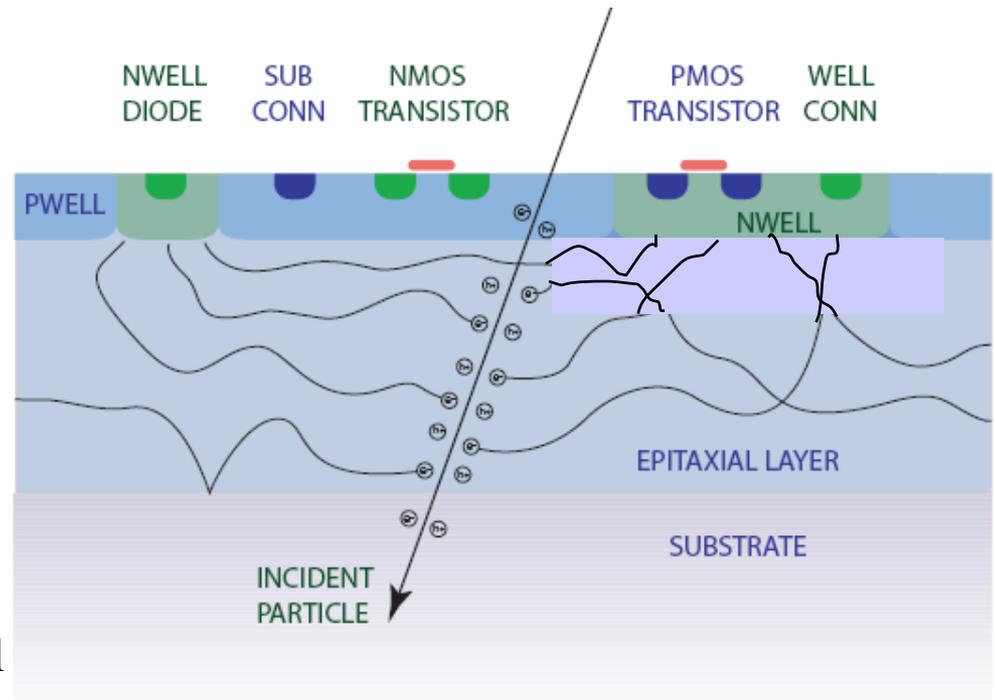
CMOS epitaxial layer

- Sensor has an “epitaxial layer”
 - Region of silicon just below circuit
- Typically is manufactured to be 5-20 μm thick
 - We use 12 μm
- Only ionised electrons within this region can be detected



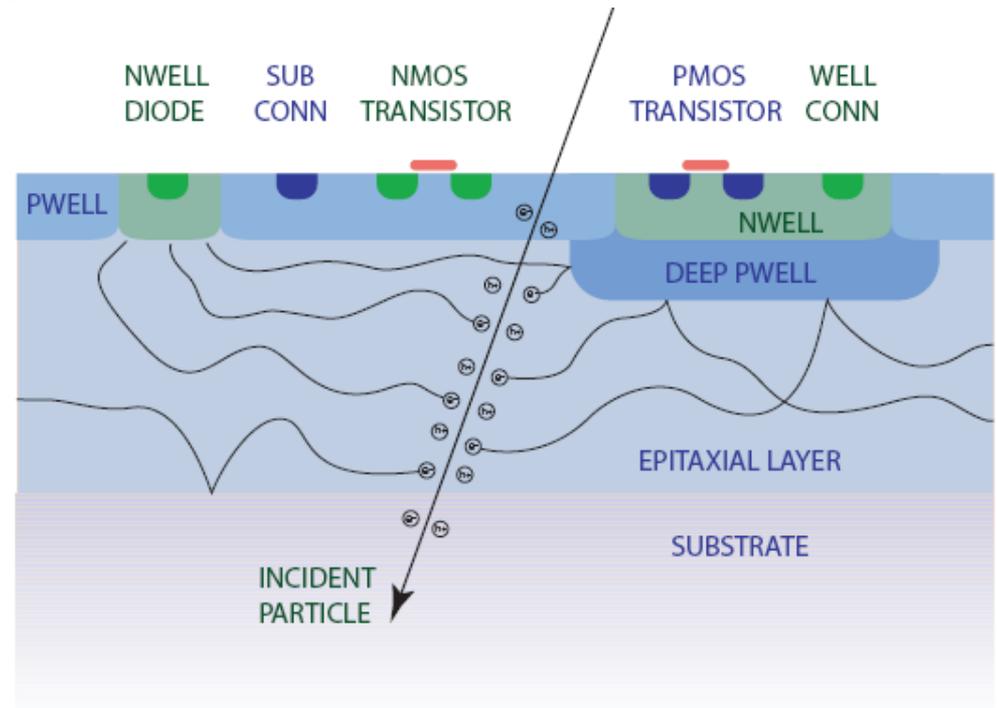
Signal collection

- Electrons move in epitaxial layer simply by **diffusion**
 - Ionised electrons can be absorbed by an n-well structure
 - Make n-well diodes for signal collection within circuit layer
 - Takes **~100ns**; OK for ILC
- **PROBLEM**: p-type transistors in CMOS (“p-MOS”) also have an n-well
 - Any p-type transistors in circuit will also absorb signal so it is lost
 - Low collection efficiency or restrict circuit to use n-type transistors only?



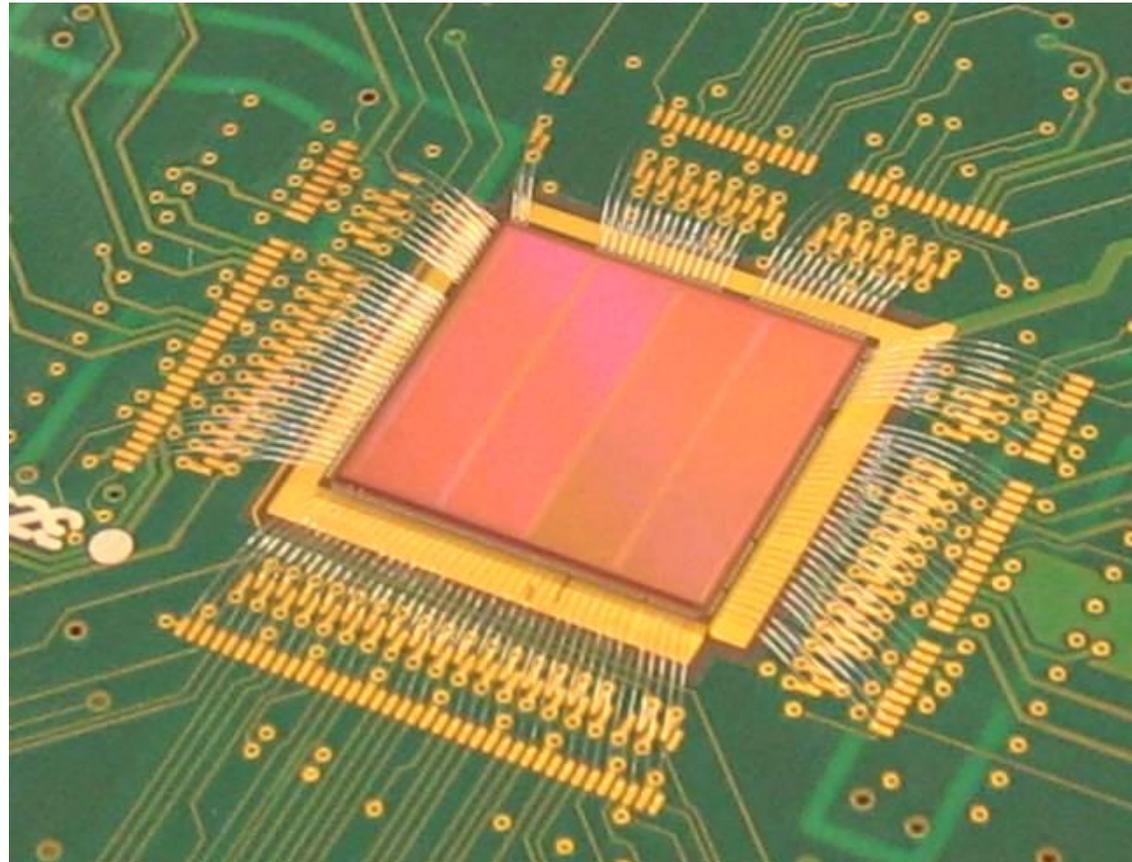
Deep p-well process

- Developed “protection” layer for circuit n-wells; “**deep p-well**”
- Cuts off n-wells from epitaxial layer and so prevents them absorbing signal
- Allows **full** use of both n-type and p-type transistors without large signal loss

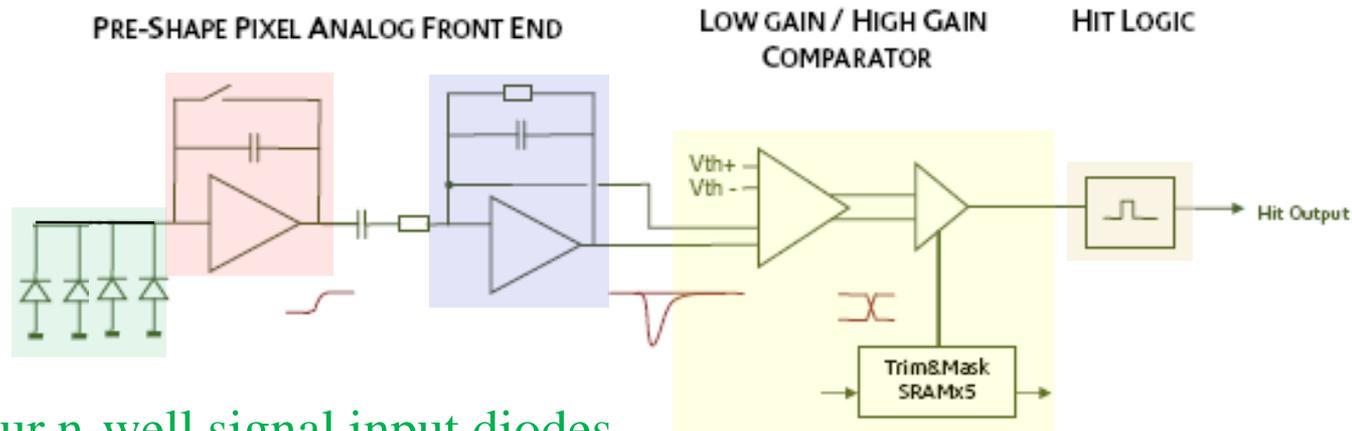


TPAC1

- Tera-Pixel Active Calorimeter sensor
- To investigate issues of DECAL; not a realistic ILC prototype
- 168×168 array of $50 \times 50 \mu\text{m}^2$ pixels
- Analogue test pixel at edge
- Total $\sim 28,000$ pixels
- Size $\sim 1 \times 1 \text{cm}^2$
- Made with $0.18 \mu\text{m}$ CMOS deep p-well process

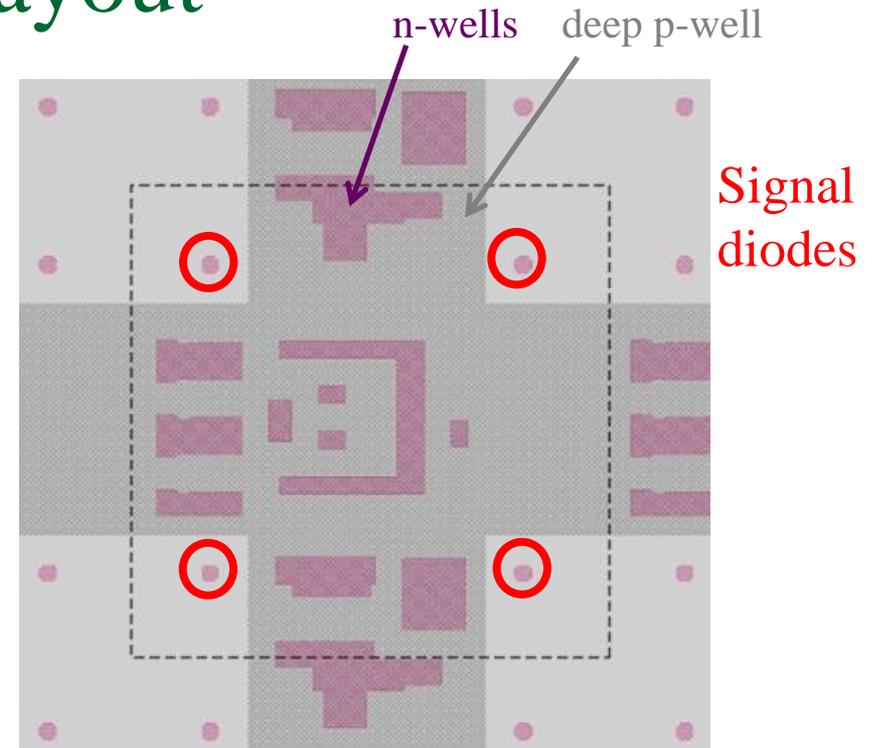
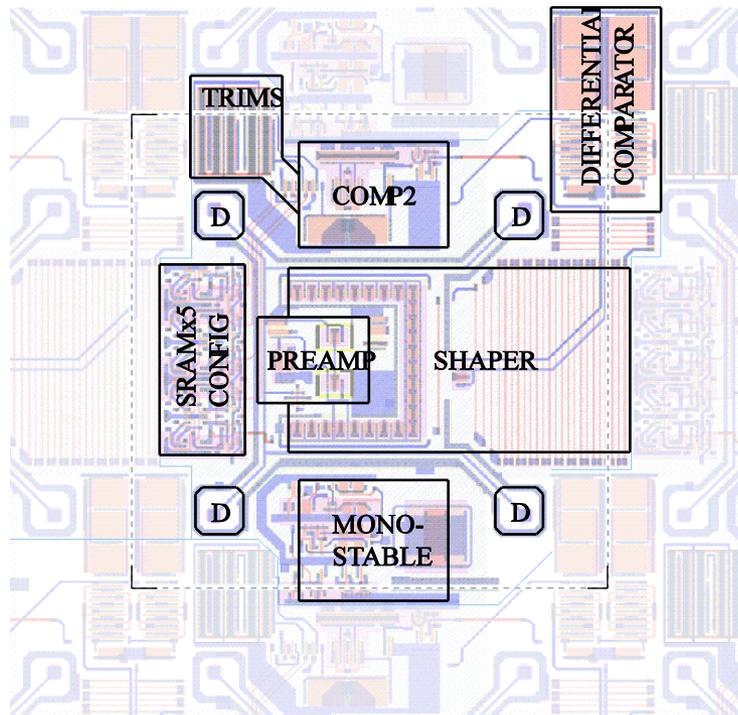


TPAC1 in-pixel circuit



- Four n-well signal input diodes
- Charge integrating pre-amplifier
- Shaper with RC time constant ~ 100 ns
- Two-stage comparator with configurable per-pixel trim
- Monostable for fixed-length output

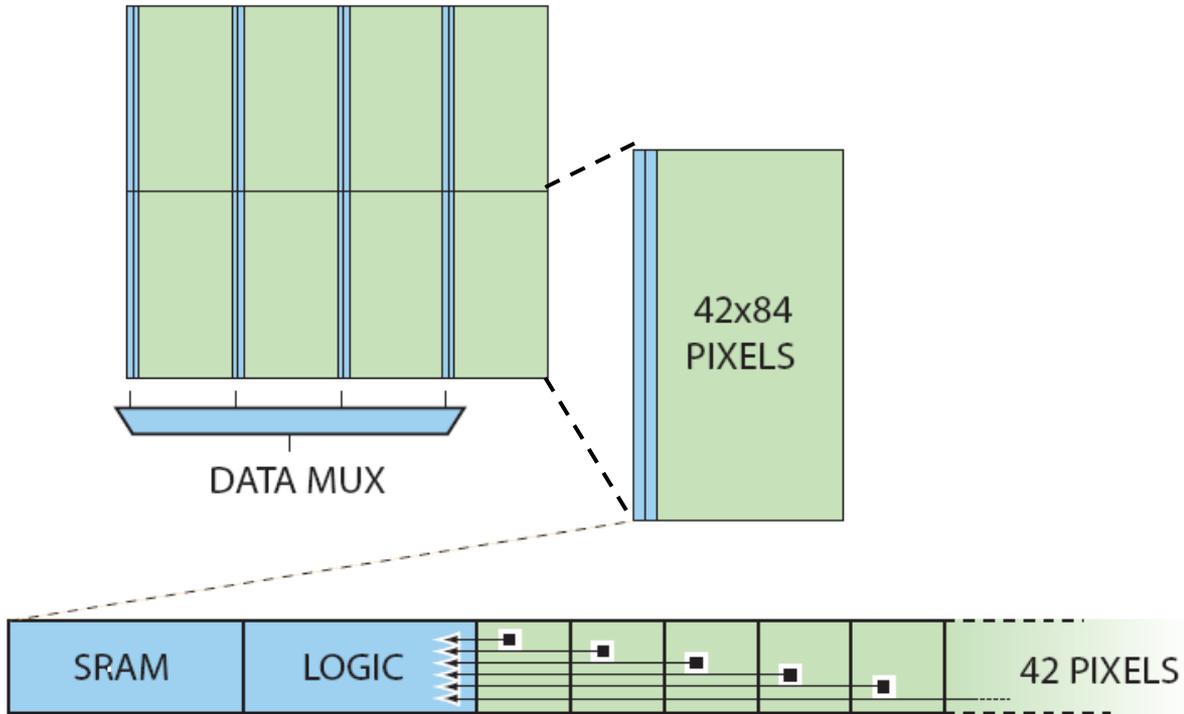
TPAC1 signal diode layout



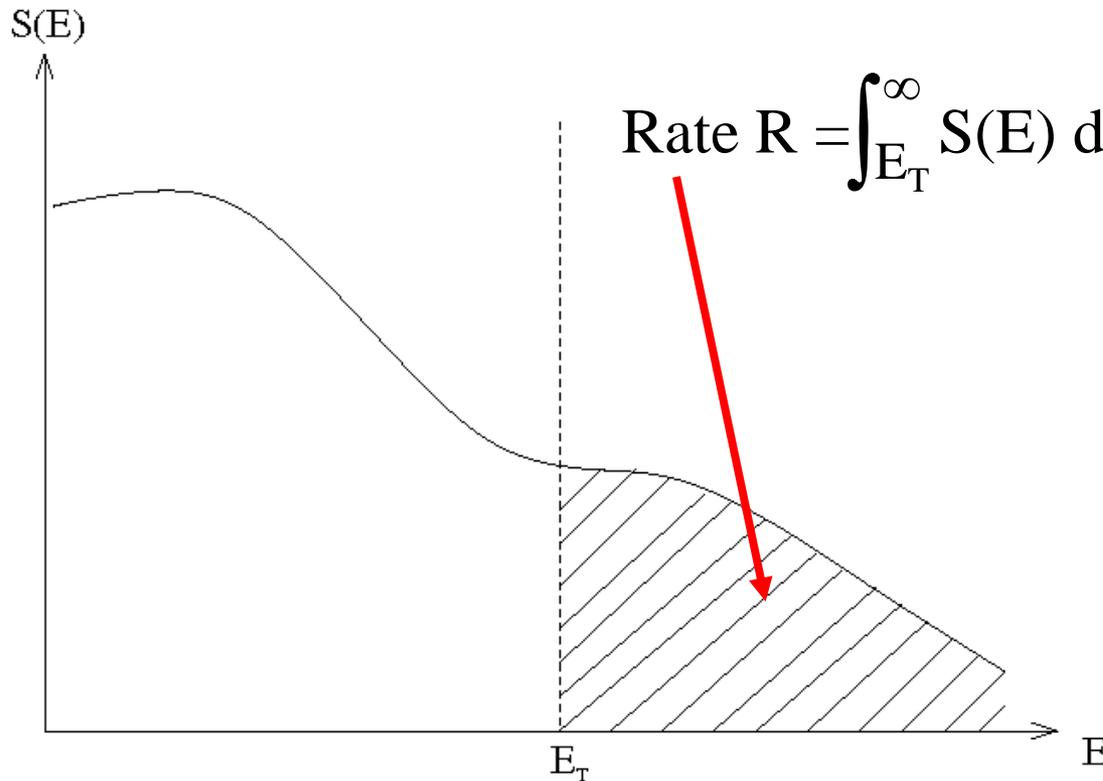
- Pixel effectively completely full; high component density means **high power**
 - $\sim 10\mu\text{W}/\text{pixel}$ when running; $\sim 40\mu\text{W}/\text{mm}^2$ including ILC power pulsing

TPAC1 on-sensor memory

- Monostable outputs from 42 pixels in each row tracked to memory regions
- A hit above threshold is stored in memory with timestamp (i.e. bunch crossing ID)
- Need four memory regions, each 5 pixels wide
- Dead space; $5/47 \sim 11\%$



Digital readout and threshold

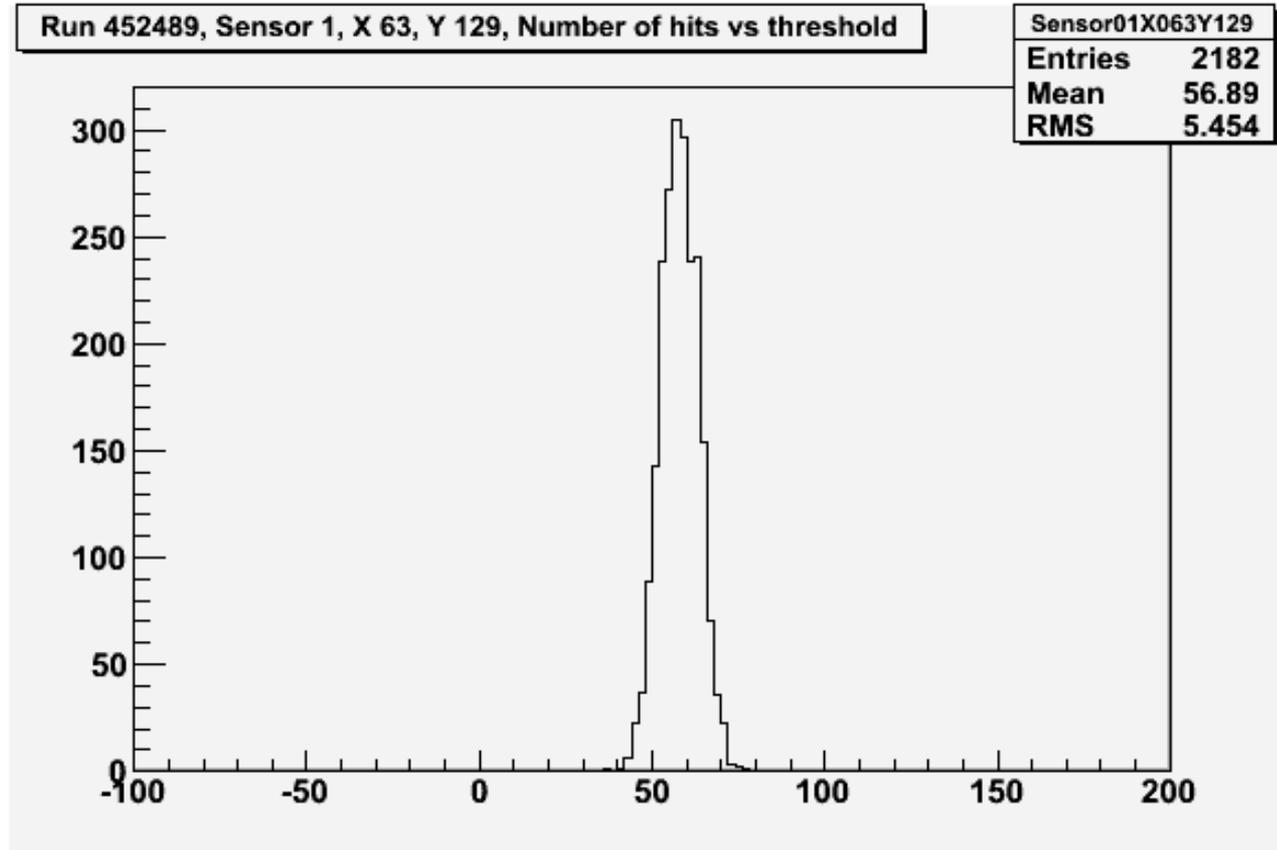


$$\text{Rate } R = \int_{E_T}^{\infty} S(E) dE$$

$$\rightarrow S = -dR/dE_T$$

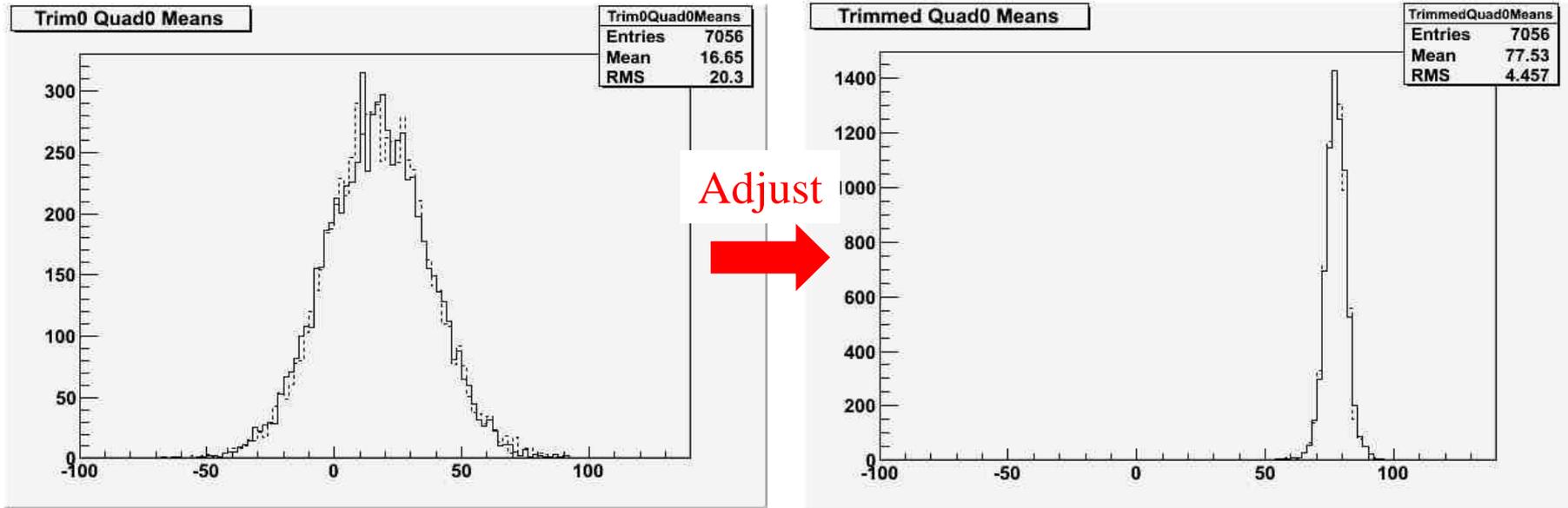
- Can measure spectrum even with digital readout
- Need to measure rate for **many** different threshold values
- Scan threshold values using computer-controlled DAC

No signal: pedestal and noise



- Typical single pixel
- Note, mean is **NOT** at zero = pedestal

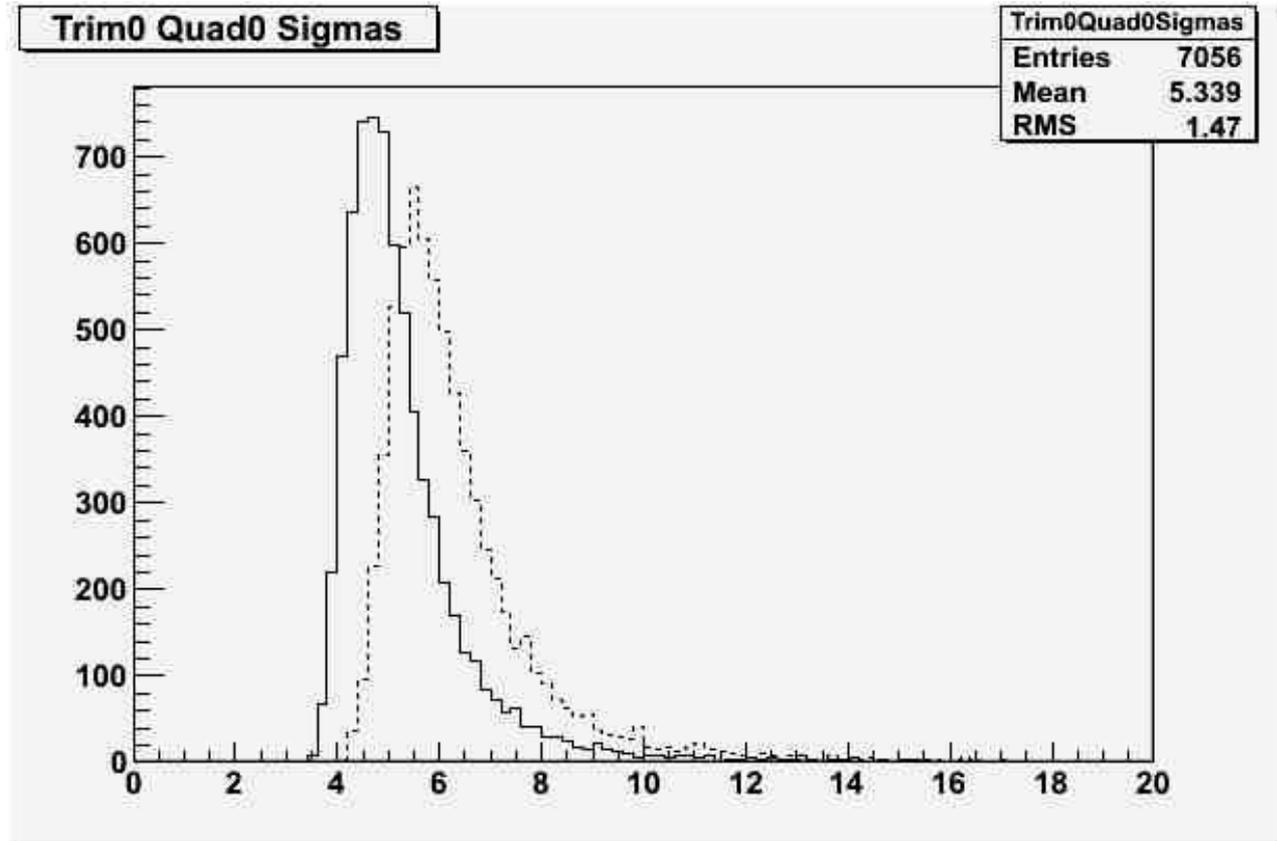
Pedestal spread



- Pedestals have large spread ~ 20 TU compared with noise
- Caused by **pixel-to-pixel variations** in circuit components
 - Pushing component sizes to the limit
- Per-pixel adjustment used to narrow pedestal spread
 - Probably not possible in final sensor

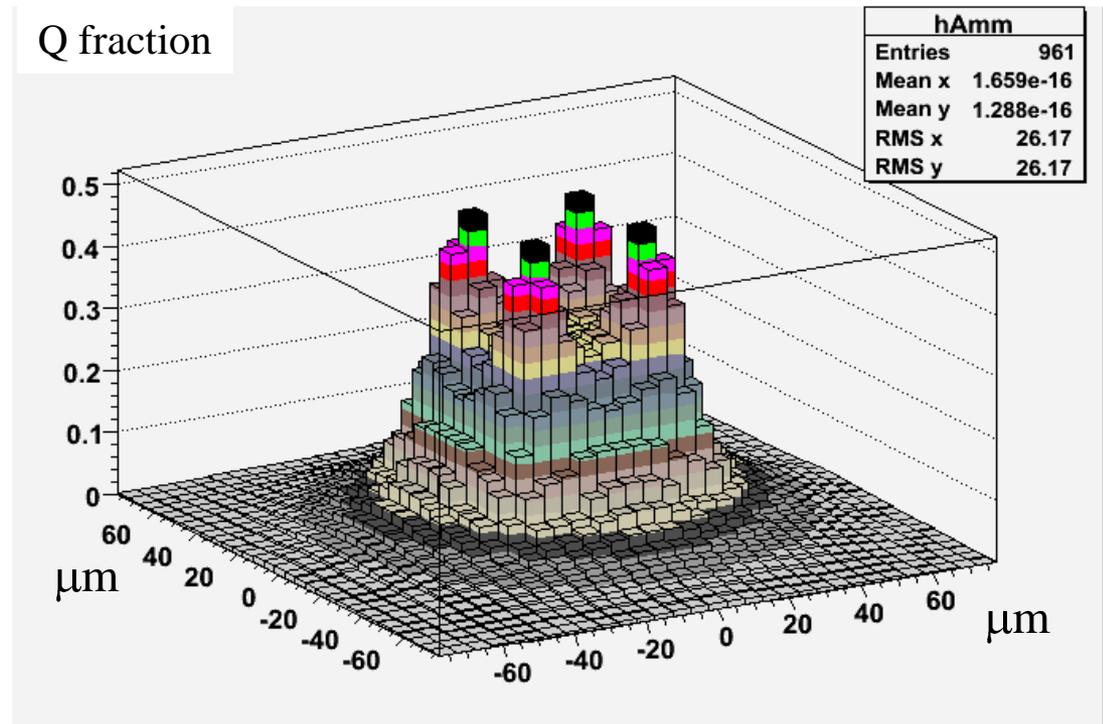
Noise spread

- Noise also has large spread
- Also caused by variations in components
- Average $\sim 6TU$



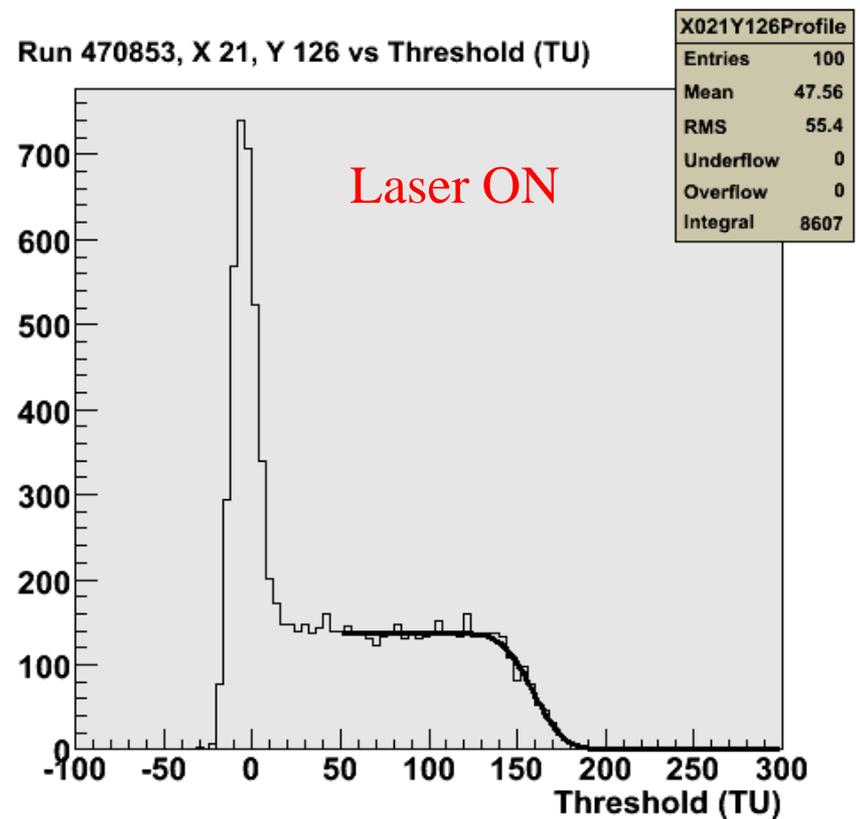
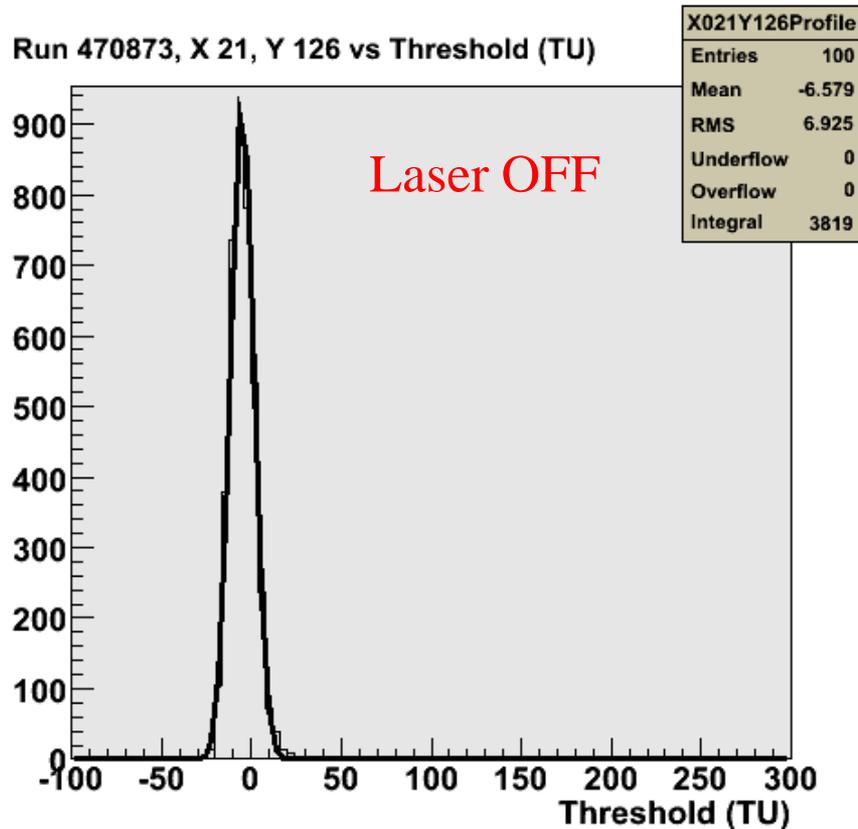
Charge diffusion

- Signal charge diffuses to signal diodes
- But also to neighbouring pixels
- Pixel with deposit sees a maximum of $\sim 50\%$ and a minimum of $\sim 20\%$
- Average of $\sim 30\%$ of signal charge
- The rest diffuses to pixel neighbours



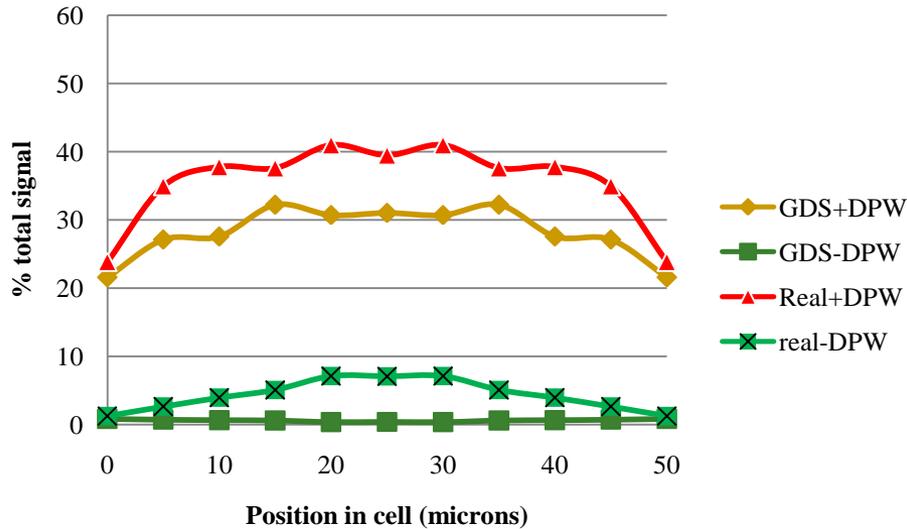
Charge diffusion measurements

- Inject charge using IR laser, 1064nm wavelength; silicon is transparent

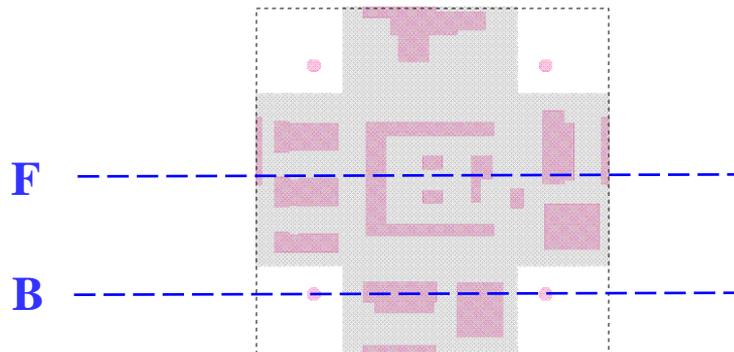
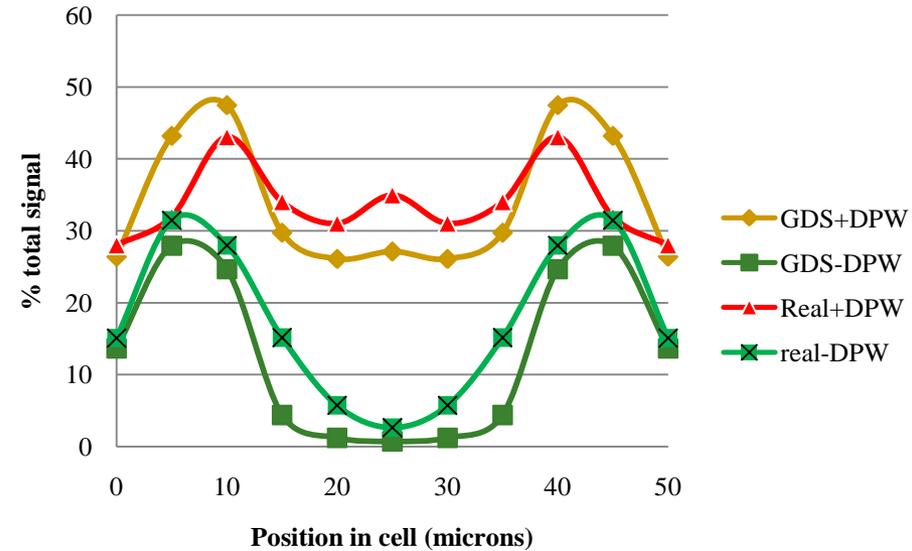


Charge diffusion measurements

Profile F; through cell

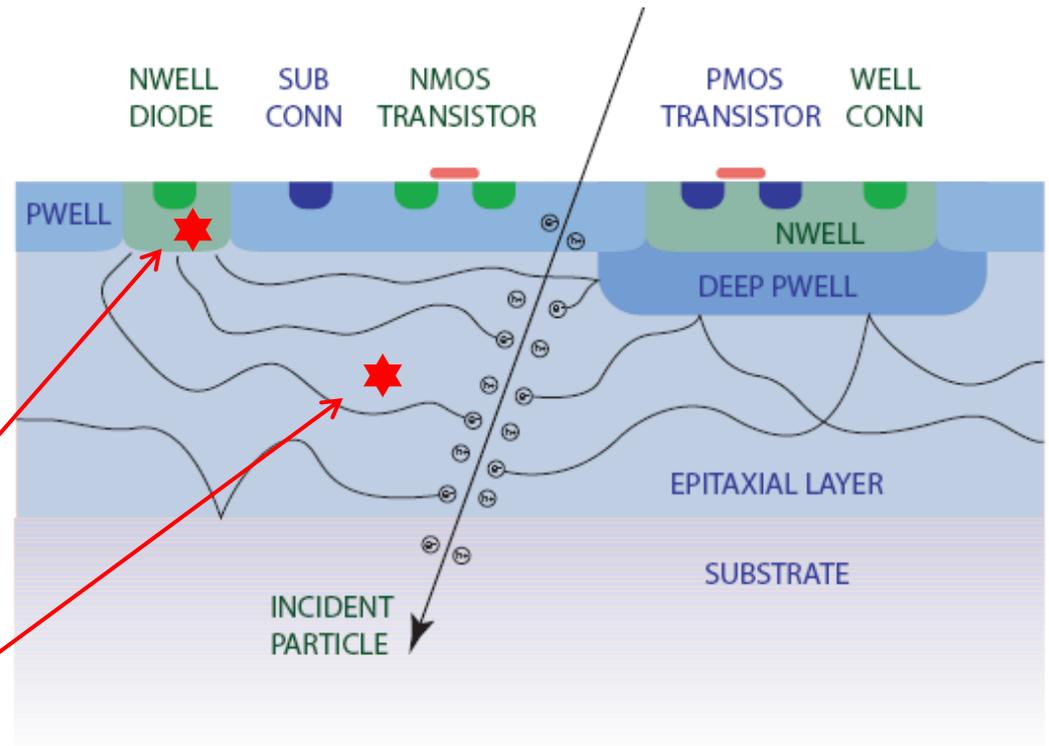


Profile B; through cell



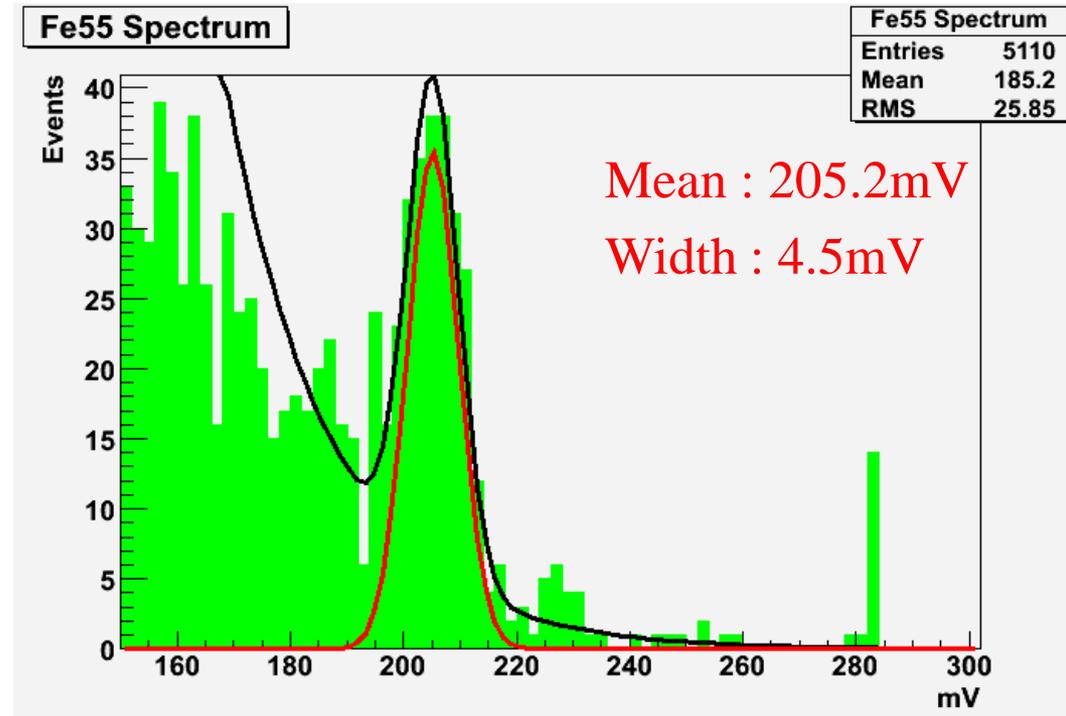
Calibration: ^{55}Fe source

- Use ^{55}Fe source; gives 5.9keV photons, compared with $\sim 3\text{keV}$ for charged particle
- Interact in silicon in very small volume $\sim 1\mu\text{m}^3$ with all energy deposited; gives $1620e^-$
- 1% interact in **signal diode**; no diffusion so get all charge
- Rest interact in **epitaxial layer**; charge diffusion so get fraction of charge



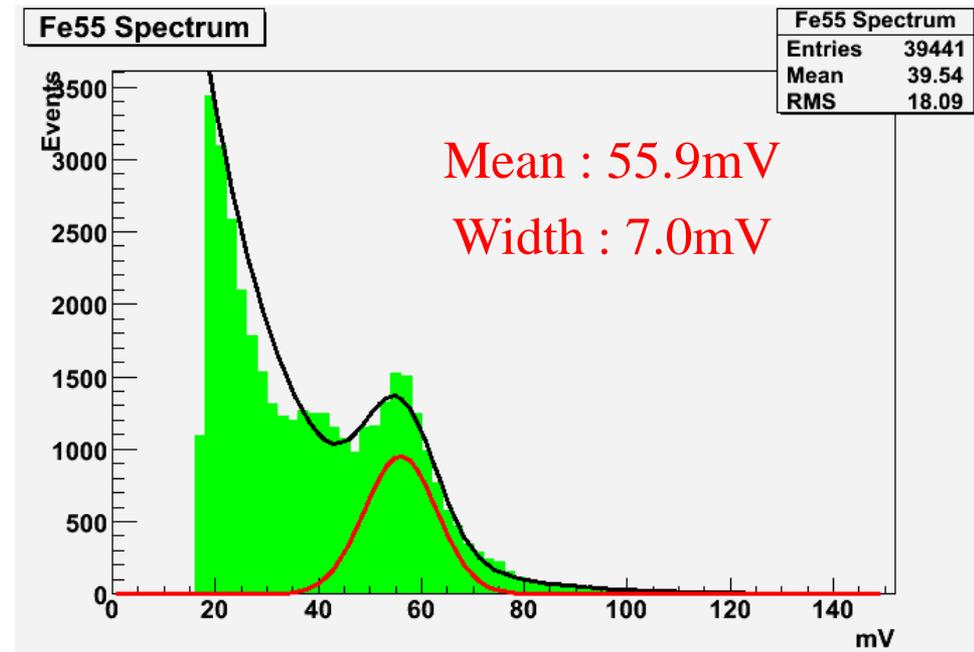
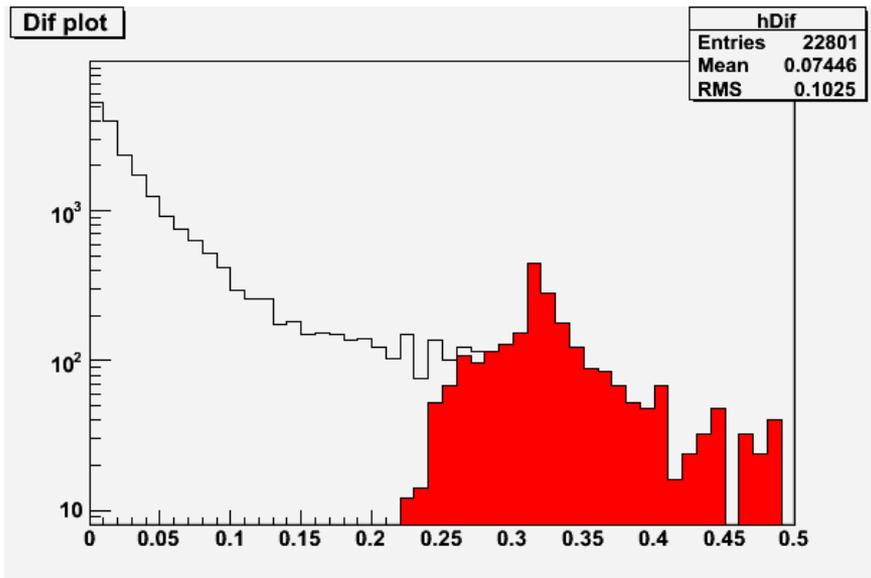
Calibration: test pixel analogue signal

- Interactions in signal diode give **monoenergetic** calibration line corresponding to 5.9keV
- Can see this in test pixel as analogue measurement of spectrum



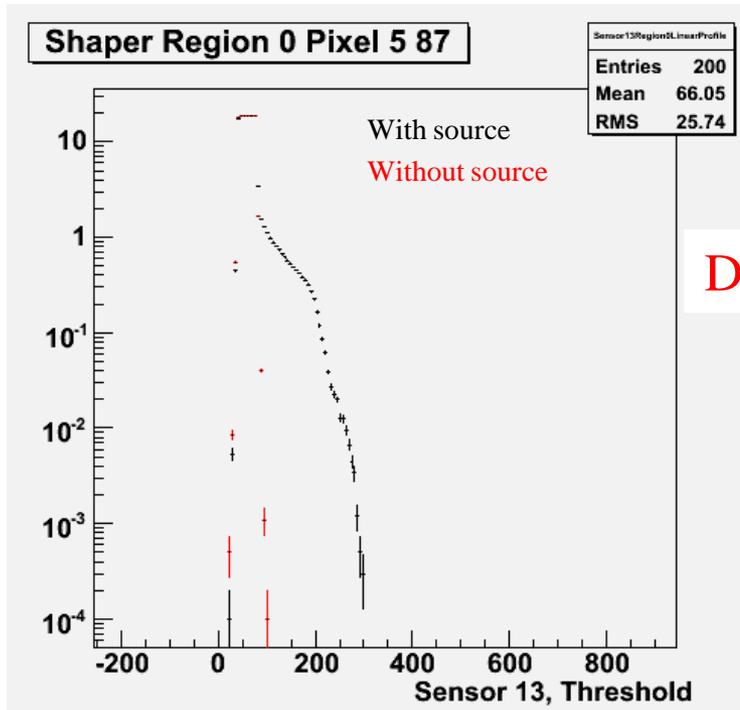
Calibration: test pixel analogue plateau

- Can also use lower plateau from charge spread $\sim 30\%$ of 5.9keV

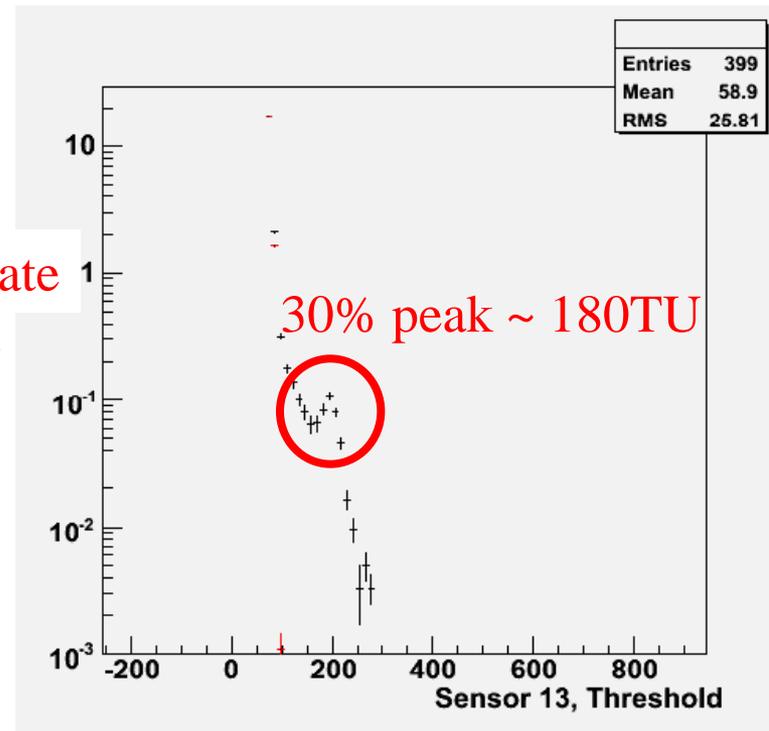


Calibration: digital pixel analogue plateau

- Comparator **saturates** below monoenergetic 5.9keV peak; cannot use ☹
- In digital pixels can only use lower plateau
- Sets scale: 1 TU $\sim 3e^-$ so **noise (ENC) $\sim 6TU \sim 20e^-$**



Differentiate



Critical points

- TPAC1 sensor is understood
- Fundamental signal charge $\sim 1000e^-$
- Charge reduced by diffusion to neighbouring pixels
- Maximum $\sim 500e^-$, minimum $\sim 200e^-$, noise $\sim 20e^-$
- Dead area from memory storage $\sim 11\%$
- Not realistic ILC sensor
 - Too small $\sim 1 \times 1 \text{cm}^2$
 - Pixel variations (pedestal, noise) too big
 - Power consumption too high