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# MAPS Workpackage

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# News

- Meeting with Renato Turchetta
  - Wed 3 Nov: Nigel and myself
  - Based on MAPS (very rough) conceptual design document V0.1
- Very positive meeting
  - Renato seems enthusiastic
  - He is willing to sign proposal; adds credibility
- Many technical areas discussed
  - Many open questions
  - Need some thought on both sides (see later)
- Also clarified possible scope, costs, effort and schedule

# MAPS scope

- Will investigate both options; sum and individual pixel readout
  - Individual pixels are more uniform; probably technically easier
  - Renato suggested analogue version; direct equivalent of VFE
  - Opens a large can of worms; put on the back burner for now
- Aim for two iterations
  - First: small  $\sim 1 \times 1 \text{cm}^2$  chips with multiple MAPS sensors ( $\sim$ nine) on each
    - Each sensor has a different design;  $\sim 20$  chips total to be fabricated
    - Special shared run; only possible every six months but schedule not yet known
  - Second: Larger (standard size)  $\sim 2 \times 2 \text{cm}^2$  chips with single MAPS per chip
    - Will not try stitching for even larger sizes; commercial R&D in this area already
    - Standard run; possible at any time
    - Usual processing is six wafers, each with  $7 \times 7$  chips  $\sim 300$  chips  $\sim 1000 \text{cm}^2$
    - Enough for several layers of a beam test
- Readout: can use simple interface to FPGA development board
  - Sufficient for all tests except at beam; need more specialised DAQ?

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# Schedule

- The rough schedule from the discussion with Renato was
  - First iteration:
    - Months 1-3: Feasibility study for the two (three?) options
    - Months 4-13: Design
    - Months 14-17: Fabrication (ideally; specialised slot available near this time?)
    - Month 18: Basic tests at RAL
    - Months 19-30: Detailed tests at Universities
  - Second iteration:
    - Months 19-26: Redesign
    - Months 27-30: Fabrication
    - Month 31: Basic tests at RAL
    - Months 32-36: Detailed tests at Universities and beam test

# Effort and cost

- Effort:
  - 1 FTE of RAL design engineer; would be one real person full time ☺
  - 0.1 FTE of Renato: technical direction and management
  - University RA: average ~0.5FTE
    - Low level until first sensors available to test; first 17 months
    - High level thereafter: next 19 months
- Cost:
  - RAL engineer: £80-120k/year so could be £90k+£12k=£102k/year
  - University RA: £40k/year so average = £20k/year
  - Iteration 1: 600 euros/mm<sup>2</sup> so total ~£50k in May-Aug 06, i.e. FY06/07
  - Iteration 2: £60k in Jun-Sep 07, i.e. FY07/08
    - Would need ~20% and ~10% contingency, respectively
  - Readout infrastructure cheap: ~£5k total? Beamtest DAQ in other w/p?
  - Travel: purely within UK until beam test ~£20k total?
  - Total cost: £501k; FY profile £128k, £179k, £194k (not inc. contingency)

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## Next steps

- Will have another meeting with Renato ~end Nov
  - Revise conceptual design document
  - Need to firm up simulation requirements
- Need significant simulation work
  - Particularly requirements for
    - Pixel size
    - Charge sharing (crosstalk)
- I am concerned we won't have a strong case unless this work really starts soon