Case for Support - CALICE
Calorimetry for the International Linear Collider

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Executive Summary

The International Linear Collider (ILC) is seen by high energy physicists in all regions of the world as the most important new project in the subject. Its physics program has been shown to complement that of the LHC; in particular the ILC will be able to perform many high precision measurements. The CALICE collaboration brings together physicists from all parts of the world who have an interest in calorimetry for an ILC detector. The immediate focus for CALICE is the construction and testing of prototypes of highly granular calorimeters, using technologies suitable for the ILC, in test beams during 2005-6. Five UK groups were approved by the PPRP at the end of 2002 to join CALICE.

The UK contribution was to provide readout electronics and DAQ software for the CALICE electromagnetic calorimeter, and also to contribute strongly to software and analysis efforts. During the past two years, the electronics has been successfully constructed and the prototype is about to move into a test beam. We have also made a leading contribution to the software work in CALICE.

The present proposal serves two main purposes. The first is to seek support for completion of the test beam campaign and analysis of the data. The second is to build on our successful contributions in CALICE and perform further generic R&D for ILC calorimetry. It is anticipated that experimental collaborations will start to form around 2008, working towards technical design reports in 2009. Our proposed R&D addresses some of the key issues which need to be attacked before that point. In this way, we intend that the UK be well placed to design and construct a substantial part of the calorimeters for an ILC detector.

The work proposed will cover the next three financial years and is divided into five (strongly interconnected) workpackages:

- **WP1: Completion of test beam program**
  We request travel funds, and support for RA posts, to ensure that the UK groups participate fully in the data taking and exploitation of the data. Total cost to PPARC £0.30M.

*Spokesperson

- **WP2: Data Acquisition**
  We propose several areas of generic R&D which address key issues associated with reading out a highly granular and compact detector. In particular, large data volumes must be transported reliably, in the minimum of physical space. Total cost to PPARC £0.72M.

- **WP3: Monolithic Active Pixel Sensors**
  We propose to investigate an attractive and novel approach for ILC electromagnetic calorimetry, namely digital readout of small pixels, building on existing UK expertise in MAPS technology. Total cost to PPARC £0.94M.

- **WP4: Mechanical and Thermal Studies**
  We propose to deploy existing UK expertise to address several issues connected with heat flow and thermal modelling, and the assembly of very large silicon pad arrays. Total cost to PPARC £0.17M.

- **WP5: Simulation and Physics**
  We propose to build on existing leadership and expertise in these areas. We plan to continue developing tools and to perform simulation studies, especially of calorimetry, which will allow us to participate in global detector design and optimisation. Simulation expertise will also be needed by the other workpackages. Total cost to PPARC £0.35M.

As part of the support for these packages, we request five new RA posts, the continuation of the existing CALICE RA post at Cambridge, and additional effort at UCL and RAL/ID, in addition to effort already funded through rolling grants and the RAL SLA. The overall total cost to PPARC of the proposal is £2.48M, or £2.66M including the working allowance.

Contents

1 Introduction

1.1 The International Linear Collider

The International Linear Collider (ILC) [1] is a worldwide enterprise to construct an e^+e^- linear collider operating in the energy range 0.5 to 1 TeV. There is a widespread consensus [2] among the particle physics community that such a machine is vital for the future of the subject, and that it complements the LHC [3]. In broad-brush terms, the LHC will be a powerful discovery machine to reveal the new physics which is expected to emerge on the TeV scale in, for example, the Higgs and supersymmetry sectors, while the ILC will be better adapted to performing high precision tests.

The original accelerator R&D for the Linear Collider was centred around DESY [4], SLAC [5] and KEK [6], and viable designs were produced based both on conventional (warm) RF cavity technology and on superconducting (cold) technology. A major item of progress in the past year was the establishment of an International Technology Recommendation Panel, to advise the community on the technology to pursue. In August 2004 this panel recommended the adoption of the cold technology [7]. Efforts in all three regions are now directed towards jointly producing a fully costed accelerator technical design by 2007. For detector R&D, one important aspect of the accelerator technology choice is that it better defines the time profile of the bunch structure of the beam, with important implications for DAQ and readout.

Amongst the main physics areas to be addressed by the ILC will be precise measurements of Higgs boson properties, accurate investigation of the SUSY spectrum, probing of strong electroweak symmetry breaking, and precision top quark physics. A common requirement for most of these physics studies is good measurement of hadronic jet energies, and this places stringent requirements on the calorimetry. There is general agreement that the way to achieve the required jet energy precision is via the "Particle Flow" (aka "Energy Flow") paradigm. This requires the energy deposits of different particles in the calorimeters to be separated, which in turn leads to an emphasis on granularity and spatial resolution rather than single-particle energy resolution. These granular detectors are often referred to as "tracking calorimeters". It also demands a holistic approach to the detector design, where the interrelationship between different components of the detector is taken into account from the beginning. This is the approach taken by the CALICE collaboration.

It is expected that there will be a call for ILC detector Technical Design Reports (TDR) to be submitted in 2009. The programme proposed here should allow the UK to define its contribution to the TDR by that time. It is intended that the UK should have a clear lead in the areas where it is contributing, so as to give us influence over the future ILC detector programme.

1.2 The CALICE Collaboration

The CALICE collaboration [8] is undertaking a major programme of R&D into calorimetry for the ILC. It now has 167 members from 26 institutes worldwide and is by far the largest group studying calorimetry for the ILC. It is also the only collaboration within the ILC community studying both electromagnetic (ECAL) and hadronic (HCAL) calorimeters in an integrated way. We believe this overall calorimetry approach is the only way to obtain a calorimeter system which will be capable of meeting the demanding physics requirements of a high energy ILC detector. The breadth of the project and the size of the collaboration ensure that CALICE will be strongly involved in a future ILC detector.

The collaboration intends to test pre-prototypes of an electromagnetic calorimeter (ECAL) along with at least two types of hadronic calorimeter (HCAL) in electron and hadron beams over the next two years. The CALICE programme also covers simulation studies incorporating the results of these tests, all directed towards the design of an ILC calorimeter optimised for both performance and cost. In addition, the collaboration serves as an umbrella organisation for longer-term ILC calorimeter projects where developments can be tested together.

One of the main motivations for CALICE is to verify the simulation programs, particularly for hadronic showers, such that the design and optimisation of the final ILC detector calorimeters can be done using these simulation programs with confidence. The optimisation is not purely for physics performance; for example, cost is one of the main constraints for the favoured ECAL design, which is a silicon-tungsten (Si-W) sampling calorimeter. The cost of the large area of silicon wafers required is high and so studies to reduce this cost, in terms of less area or cheaper alternatives, are a major part of this programme.

1.3 General status of CALICE

The CALICE ECAL prototype is a silicon-tungsten sampling calorimeter and consists of 30 layers of silicon wafers interspersed between tungsten sheets. Each wafer layer contains a 3×3 array of silicon wafers, each containing 36 $1 \times 1\,\mathrm{cm}^2$ diode pads. There are around 10,000 channels in total occupying a volume of approximately $(18\,\mathrm{cm})^3$. The ECAL assembly is currently paced by the silicon wafer production; more than half of the silicon wafers are now manufactured and the rest are expected over the next three months. Around one third of the layers were ready by the end of 2004 and the rest are expected to be complete by April 2005.

The analogue HCAL (AHCAL) is a sampling calorimeter with 40 layers of steel absorber sheets instrumented with scintillator tiles. The total volume is approximately $(1\,\mathrm{m})^3$. The tiles are of varying sizes, with the highest granularity central region using $3 \times 3\,\mathrm{cm}^2$ tiles, increasing to $12 \times 12\,\mathrm{cm}^2$ for the outermost tiles. As the name implies, the readout will be analogue, with the off-detector electronics being common to the ECAL. The AHCAL has around 8,000 channels and is scheduled to be completed by September 2005. It is complemented by a "tail-catcher", consisting of 96 cm of iron instrumented with 16 layers of 5 mm $\times$ 5 cm scintillator strips, which will tag leakage and detect muons.

The digital HCAL (DHCAL) is a binary readout sampling calorimeter. The sensitive layers will be mainly resistive plate chambers (RPC) although for some of the tests, one or more layers may be replaced with gas electron multiplier (GEM) detectors. The RPC (or GEM) pads will be $1 \times 1\,\mathrm{cm}^2$, giving 400,000 channels, each reading one bit. As one of the main aims of the beam tests is to compare the performance of these HCAL options, the same absorber structure and tail catcher as for the AHCAL will be used, so as to eliminate any spurious differences which might otherwise arise. Hence, the DHCAL is also around 1 m^3 in volume. The DHCAL is being developed by US groups, who are applying for funds for the readout electronics (common to RPC and GEM) early in 2005. Assuming funding is secured, the DHCAL should then be completed by summer 2006.

The first ten layers of the ECAL will be exposed to a low energy electron test beam at DESY in January 2005. This will be a technical commissioning run to debug the system and provide a first look at the ECAL performance. This test is expected to continue intermittently over the following six months as the rest of the ECAL is assembled and installed. The completed ECAL will then be run until July.

In September 2005, the ECAL will move to FNAL to take hadron beam data. Even without any HCAL behind it, it has been shown [9] that significant differences between hadronic shower models can be seen in the ECAL alone. These tests will continue until around November, when the AHCAL will be ready. The two detectors are then expected to take data for six months. Around summer 2006, the DHCAL should then arrive at FNAL and again, around six months is expected for data taking with the ECAL and DHCAL together.

1.4 Background to the proposal

The CALICE UK groups were approved by the PPRP in December 2002 for an initial programme with the CALICE collaboration. This was to provide the readout electronics for the ECAL and perform simulation studies. The approval covered the first two years of the CALICE programme.

The PPRP stated at the time of approval that the groups should return towards the end of the two year period to bid for continuation of the funding. The committee expected this bid to include funds both to complete the current CALICE programme as well as to define a longer-term major project which would lead more directly to the ILC detector TDRs. This is the purpose of the current proposal.

The work proposed is being done within the context of the global organisation building towards an ILC on the timescale of first collisions in 2015. In terms of calorimeters, construction is likely to take around three to four years and so would need to start early in 2012. Prototyping will require around two years prior to this, specifically 2010 and 2011. Hence, the two detector TDRs expected in 2009 will represent a major milestone in narrowing down the choices for the ILC detectors and will determine which technologies should proceed to the prototyping stage. This is why we view it as critical that the UK builds a programme over the next three years which will allow us to contribute very strongly to the TDRs.

For future planning purposes, we also wish to make the PPRP aware that there is interest in joining CALICE within the Edinburgh HEP group. They have recently had a new academic post approved specifically aimed at ILC studies and so will advertise for candidates very soon. Until this post is filled, they feel unable to commit to joining the collaboration. However, when the new lecturer is in post, then they may bid to join the UK groups with an additional proposal which would bring added value to the UK CALICE contribution. A letter from the senior members of the Edinburgh group explaining their position is attached. Note, however, that the current proposal does not assume this extra effort is available and should be evaluated on its own merits.

This proposal is organised as follows: Section 2 describes the status of the work funded in the original proposal; Sections 3 to 7 outline the five proposed workpackages for the current bid; Section 8 describes the management of the UK groups; Section 9 gives further information on benefits to the wider community. Details of the proposed workpackages and financial details are given in the annexes, together with a public outreach statement and a list of talks and proceedings.

2 Status of the current UK effort

We report here on the work done by the UK groups in CALICE in the last two years. The talks given and proceedings produced as a result of this work by the members of these groups over the period of the previous grant are listed in Annex E.

2.1 Status of the UK electronics

The UK commitment was to design, build and commission the VME readout system for the ECAL. This work was done by Imperial, RAL/ID and UCL and is essentially complete.

Upstream of the UK electronics, the signals from the silicon wafer pads are amplified and read out with the very front end (VFE) ASIC chip [10] designed by the LAL-Orsay group. The wafers and VFE chips are mounted on the VFE PCB, designed by the same group. The 60 VFE PCBs required for the full ECAL are connected to the UK electronics via mini-SCSI cables. The UK is responsible for all the readout electronics and online software downstream of the VFE PCBs.

2.1.1 Readout electronics

The readout system consists of six 9U VME boards which provide the control and the digitisation of the analogue signals from the VFE PCB. They also provide local buffering of data for up to 2000 events, which should be more than sufficient for each spill. One of the boards also provides trigger logic and control, with the trigger being fanned out from this central board to the other boards in the system (including itself) using point-to-point connections on a custom-built PCB which attaches to the VME J0 connectors across the crate backplane. The maximum allowable trigger latency is set by the peaking time of the shaped VFE preamplifer signal and is around 180 ns.

The boards were designed as a modification of the CMS silicon tracker Front End Driver (FED) design [11]. The CALICE design required a complete replacement of the FED front end (FE), which receives the input data, with a new design. The back end (BE) and VME interface were less substantially modified. Because of this commonality, there has also been some firmware shared between the two boards, reducing the engineering effort required. An overview of the structure of the CALICE boards is shown in figure 1 together with a photograph of one of the actual boards.

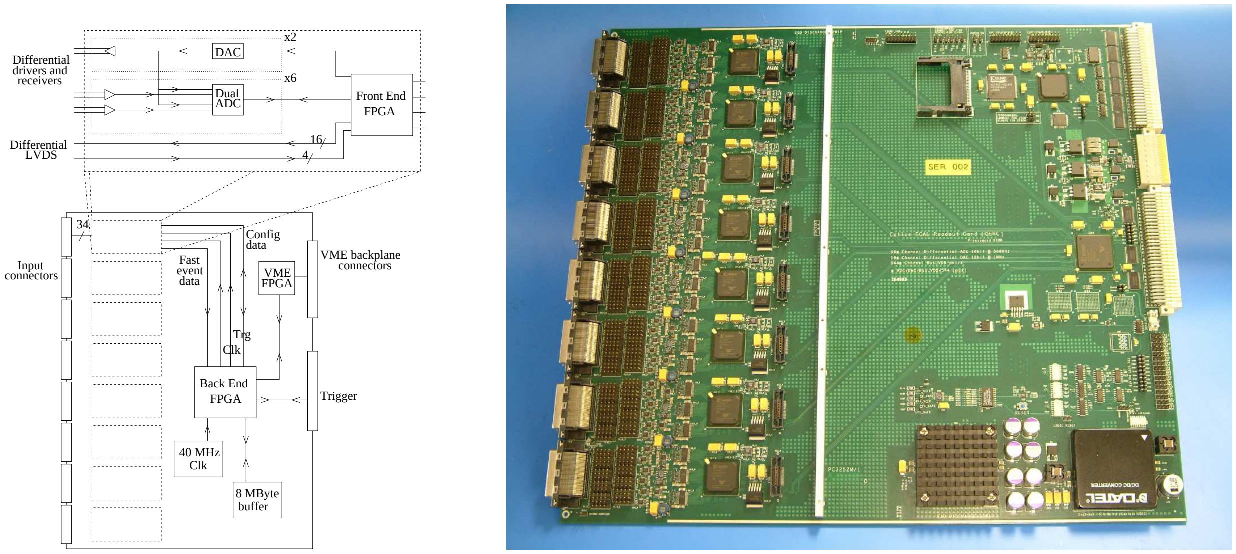

Figure 1: *Overview of the structure (left) and photograph (right) of the VME ECAL readout boards.*

Two prototype boards were fabricated by November 2003 and were thoroughly tested over the following year. These tests included a suite of stand-alone tests and calibrations using the on-board DAC. In addition, tests with the VFE PCB preproduction boards were done during early summer 2004. These involved using the DAC to calibrate the VFE PCBs, as well as using radioactive sources and cosmic rays. These tests showed that the boards were working very well [12] and only minor improvements were implemented in the design for the production versions.

Nine boards were fabricated for the production run in October 2004, of which only two were populated immediately. These two were again extensively tested before the remaining seven were released for assembly in December 2004. The seven are expected to be completed in February 2005.

The first two production boards were taken to Paris for cosmic ray tests in December 2004. A system with ten layers of the ECAL, totalling over 2000 channels, was assembled in a cosmic teststand at Ecole Polytechnique. Data were taken using the UK boards over the Christmas period and a total of over 1 million events were recorded. Figure 2 shows an example of an event where a clear track is seen through all ten layers of the ECAL; this indicates clearly why the phrase "tracking calorimeter" is used.

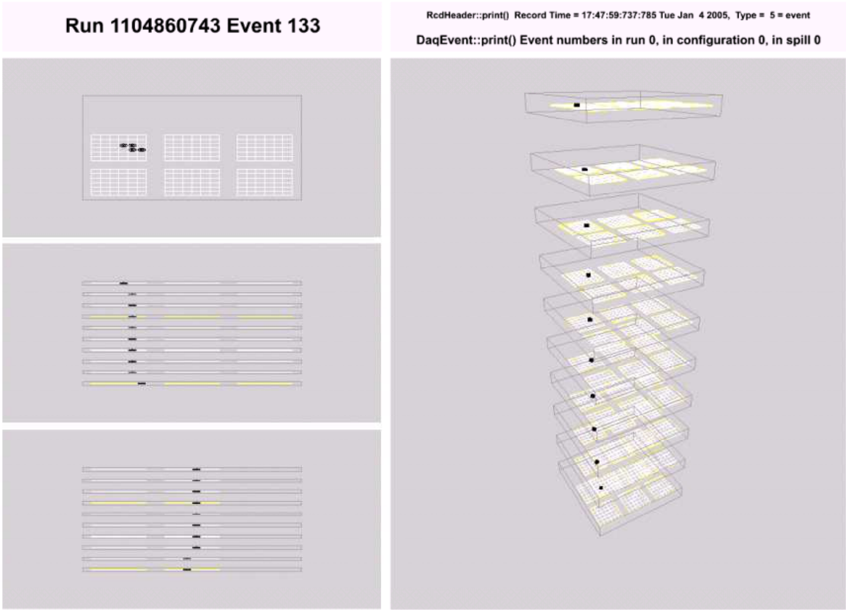

Figure 2: *Example of one event of the ECAL cosmic data taken over the last month in Paris.*

A signal/noise of around 9 for minimum ionising particles (MIP) was seen, well above the minimum requirement of 5. Figure 3 shows an example of the very clean separation of pedestal and MIP signals, where the Landau shape is visible in the latter. These data will allow the calibration for these channels to be determined to 1%, which is sufficient for the first round of ECAL studies.

The whole ECAL system has been transferred to DESY for the initial beam test which will start in January 2005 and will continue for several months.

The development of the UK boards has been seen as a major success within the collaboration. The AHCAL and tailcatcher have decided to use the same boards for their readout and are currently placing an order with RAL to produce another seven of them. This will also make the DAQ software integration easier.

2.1.2 Data acquisition software

The UK groups also provided the software data acquisition (DAQ) system for the whole of the CALICE readout.

The aim of the CALICE beam tests is to collect around 10^6 events for each configuration of beam energy, particle, type, angle of incidence, etc. This implies a complete sample of order 10^8 events. To acquire this in a reasonable time, the DAQ system should achieve an average of 100 Hz readout rate. Given the spill structure at FNAL, this means an instantaneous rate during a spill of at least 1 kHz. There will be no threshold suppression applied online as studies of pedestal stability and noise are fundamental to this work. Each event is therefore expected to be around 50 kBytes in size, giving a total raw data volume of around 5 TBytes.

The DAQ software was designed from scratch to allow a very lightweight, fast system to be

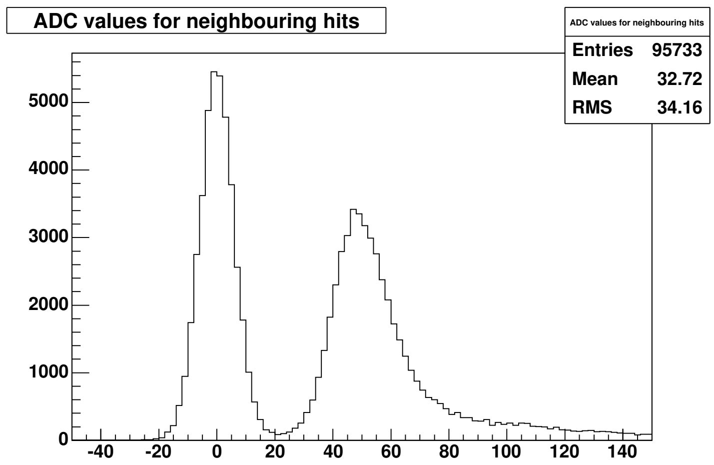

Figure 3: *Pedestal and minimum ionising signal peaks from the ECAL cosmic data taken over the last month in Paris.*

developed which was tailored to the needs of CALICE and so capable of achieving the high rates needed. It was implemented in C++ on Linux and only uses ROOT [13] and the Hardware Access Library software from CERN [14].

The DAQ system has been used for all the UK board tests so far and has been running in the cosmics tests in Paris. The trigger rate there was limited by the physical rate of cosmics to around 1 Hz. However, in calibration runs, readout of the two production boards at rates of 150 Hz has been achieved. This implies a sustained rate with six boards of around 50 Hz would be possible now. With further firmware and software developments this is expected to be improved. The biggest limiting factor currently, however, is the CPU power of the PC being used; it is an old 400 MHz machine which has been borrowed from the Imperial group. The purchase of a faster, high-performance, multi-processor DAQ PC was included in the original bid but has been postponed until now in order to get realistic experience of the bottlenecks and requirements, as well as the best possible system for the available money. This new PC will be bought before the end of the current FY and will give large increase, of at least a factor of four, in CPU speed. Extrapolating from the rates observed now, the 100 Hz requirement should be straightforward to achieve.

2.2 Status of the UK simulation effort

The PPRP, when they first considered the UK groups' application to join CALICE in 2002, strongly encouraged a vigorous participation in various areas of simulation and other software, to complement our electronics contribution to the prototypes. We report here on some of the activities in this area, which were mainly produced by Birmingham and Cambridge. The PPRP recognised the importance of this field by awarding an RA post to Cambridge (filled in August 2003 by G. Mavromanolakis, who has contributed strongly to the simulation work and preparations for the test beam).

2.2.1 Hadronic shower modelling

Apart from testing the hardware concepts, one of the most important goals of the CALICE test beam campaign is to gather data on the properties of showers, especially hadronic showers, in highly granular calorimeters. We therefore embarked on a program of systematic comparison between different shower packages.

The standard Monte Carlo program for simulation of the CALICE calorimeters (both for the test beam, and for the full ILC detector) is Mokka [15], which is based on Geant4 [16]. Geant4 provides a toolkit approach, whereby a variety of different interaction models can be combined in different energy ranges. The Geant4 authors provide a number of standard packages combining these models which are tailored to suit different "use cases". We have examined all those which are considered appropriate for high energy calorimetry. In addition, Mokka provides a facility for writing out a FORTRAN description of the detector geometry suitable for inclusion in a Geant3 program. In this way we gain access to the physics models available in Geant3 [17], namely Gheisha, Fluka, Gcalor and Micap. However, the old version of Fluka interfaced to Geant3 is now deprecated by the authors, and the current version is not yet interfaced to Geant4. In order to gain access to this interesting model, we have employed a package called Flugg [18], which provides an interface between the Geant4 geometry and materials, and the physics and transportation code of Fluka [19].

In total, seventeen different models or combinations of models have been studied [20], at different energies, for different particle species, and for two different HCAL detector technologies: scintillating tiles operated in analogue mode and RPCs operating in digital mode. Figure 4 shows some typical comparisons between these models for the case of 10 GeV π^- at normal incidence to the prototype calorimeter. In all cases the results have been normalised to the "LHEP" model which is the default in Mokka. A few of the significant findings are these:

- The response of the ECAL varies by up to $\sim 5\%$ between different hadronic models in Geant4. The response in Geant3 is systematically higher, but this is likely to be correlated with similar differences in the electromagnetic response seen for electron showers in the ECAL (but not for the HCAL). This is under study, but is thought largely to arise from the different algorithms used to treat multiple Coulomb scattering in each model.
- The response of the HCAL varies considerably more from model to model.
- The scintillator and RPC HCAL technologies show different levels of sensitivity to the hadronic model, with the scintillator being more sensitive. This seems largely to result from the interaction of low energy neutrons in the hydrogen-rich scintillator.
- The Flugg model shows a significantly greater ECAL response compared to the Geant models, both for hadrons and electrons; this is still under investigation, but is suspected to be associated with issues such as tracking cutoffs and precision.
- The shower width is an important determinant of the spatial resolution between showers, and we see sizeable differences between models of up to 50%. The models which use the Bertini cascade model (which is favoured by many experts) predict particularly broad showers. The scintillator HCAL is particularly sensitive to the modelling of low energy neutron transport.

All in all, these studies reinforce the need for appropriate data against which to validate these models. It may well turn out that none of the models accords with data, but this will either allow us to tune models, or to assign realistic systematic uncertainties to their predictions when optimising the final detector design.

2.2.2 Pattern recognition

The primary motivation for a highly granular tracking calorimeter design for an ILC detector is to separate the energy depositions of different particles within hadronic jets. This permits the use of a "Particle Flow" algorithm, in which the charged particles will be measured using the tracking chambers, and the neutrals by appropriate combinations of ECAL and HCAL

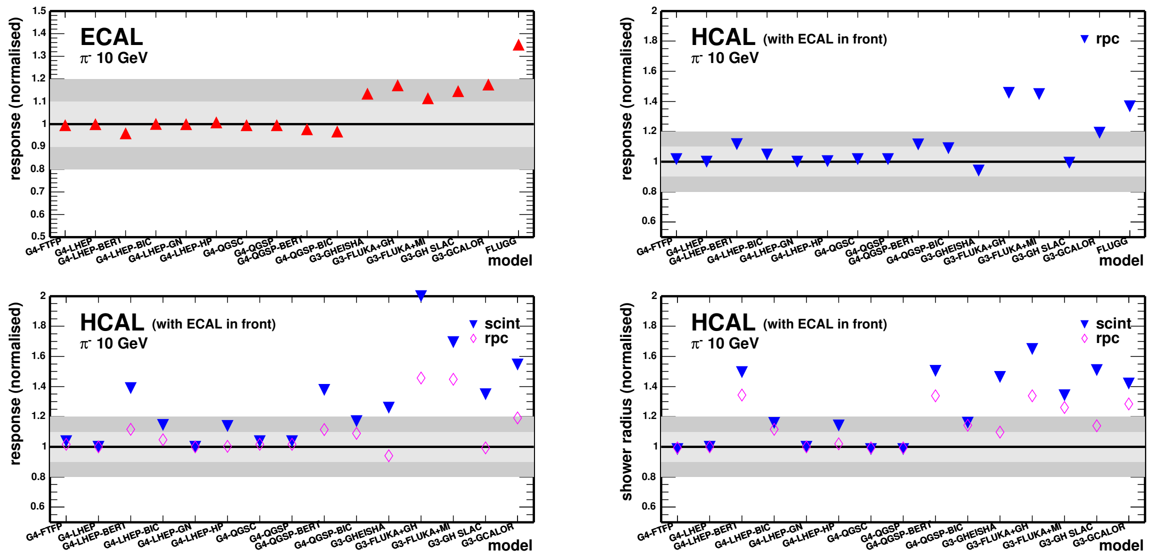

Figure 4: *Comparisons between different hadronic models for 10 GeV π^-. In each case, the results are normalised to the predictions of the LHEP model in* `Geant4`. *The upper left figure shows the response (i.e. mean energy deposited) in the* ECAL*; upper right the response (number of cells hit) in the RPC DHCAL; lower left compares the tile AHCAL response with the DHCAL; lower right compares the shower radius in the two HCALs. The shaded bands denote 10% and 20% differences.*

information. Experience from LEP, and early studies for the Tesla TDR, showed that this was the most promising way to achieve the $\sim 30\%/\sqrt{E}$ jet energy resolution demanded by linear collider physics. This resolution is not driven by the intrinsic energy resolution of either calorimeter, but by the extent to which confusion between different showers can be avoided.

Such energy flow algorithms have already been written for early ILC studies. However, these codes tend to be tied to specific simulation packages and detector geometries. In view of the need to optimise global detector designs for cost and performance, it is clearly desirable to have a flexible algorithm which can readily be adapted to new setups.

A necessary first stage is to develop a versatile and robust calorimeter reconstruction algorithm. Inspection of simple event displays in the CALICE calorimeters shows that, with the 1 cm^2 cells and fine longitudinal sampling envisaged, substructures like tracks or small clusters are commonly observed within showers. This suggests that the optimal clustering algorithm for such a calorimeter may not be a conventional "merge contiguous hits" algorithm. Within the UK we have pursued two complementary approaches to these problems. These have been presented at several CALICE meetings and Linear Collider workshops, and been well received. Both algorithms are interfaced to the LCIO data format [21], which is becoming the agreed standard for ILC studies. In this way, it should be straightforward for others to use our code, and to integrate it with tools (such as tracking) developed elsewhere.

The first algorithm [22] takes a tracking approach. The calorimeter is treated in coaxial layered shells, automatically calculated for each geometry. Seed clusters are formed in the first layer of the calorimeter, and then hits in each layer travelling outwards are considered in turn. Each hit is compared with extrapolations of hits in previous layers, taking account of knowledge of the direction of the cluster from previous layers, and the best match found. If no acceptable match exists, a new cluster is seeded. In coding the algorithm, care is taken to encapsulate geometrical information and cuts in a single place. The algorithm was developed and tested on a variety of different samples – single particles, pairs of particles, and physics events such as hadronic Z^0 and W^+W^- events – simulation models and geometries. The performance seems to be quite robust. An example of the performance is given in Fig. 5. We see that photons can already be well separated from hadrons for separations above $\sim 3-5$ cm, while the separation power is a little worse for neutral hadrons. The separation power has been found to be significantly degraded if, for example, the Bertini hadronic model, which yields wider showers (seen in Fig. 4), is used.

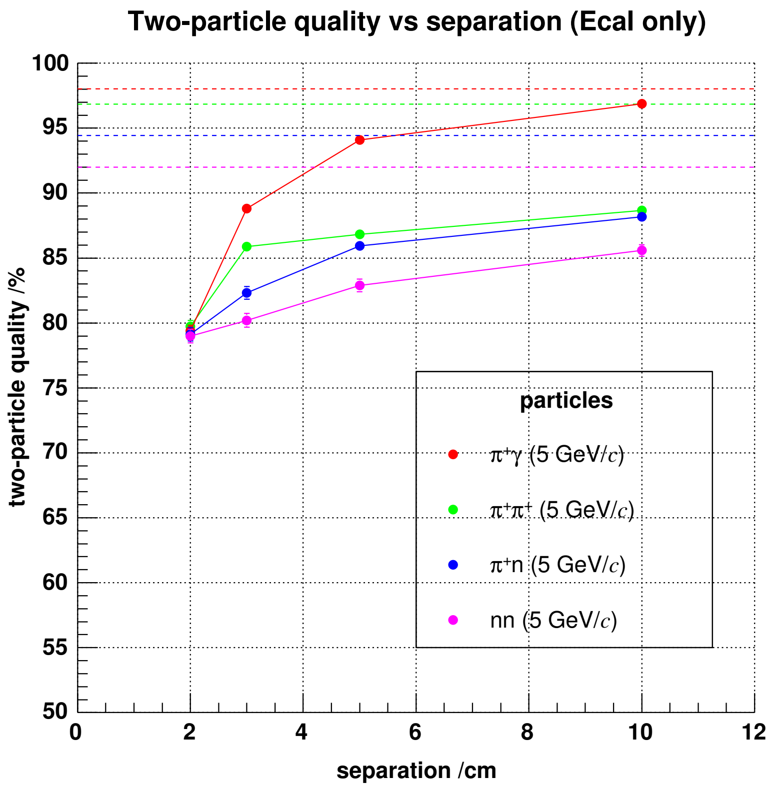

Figure 5: *Reconstruction quality (defined as the fraction of energy which has a one-to-one relation between truth and reconstruction) for various pairs of 5 GeV particles, as a function of separation at the front of the calorimeter. The dashed lines indicate the quality for single particles, i.e. the asymptotic values at infinite separation.*

The second approach to clustering [23], based on Minimal Spanning Trees (MST), is quite different. Each calorimeter hit is regarded as a node in a tree, and the MST represents the way of connecting all the nodes, with no loops, which minimises the sum of the "lengths" between nodes. Geometrical information only occurs in the metric which defines the "length", which does not have to be the geometrical distance. There are standard algorithms which efficiently compute the MST. This effectively forms the whole event into one cluster; an algorithm is then applied to form smaller clusters by cutting the tree.

2.2.3 Preparation for test beam

The simulation studies, comparing different models, have had a direct bearing on the test beam proposal for CALICE [24]. For example, we have examined the statistical precision required to distinguish between models, the particle species and energy regimes required. We have also performed studies of the possible usefulness of exposing the ECAL alone to a hadron beam [9].

In addition we are contributing strongly to the software infrastructure for analysis of the test beam data. Obviously, because of our responsibilities for the DAQ, we are in a prime position to understand the data. We are also preparing the code for converting the raw data from the DAQ into LCIO format for subsequent analysis and comparison with simulation.

2.3 General contributions

In addition to their work directed towards the CALICE test beam, some UK members of CALICE are contributing to generic international software activities for the ILC. D.R. Ward is a convener for the Simulation group (covering simulation and reconstruction tools) for the ECFA study, and also for the worldwide LCWS workshops in Paris (April 2004) and Stanford (March 2005), while M.A. Thomson is a convener of the Global Detector Performance group for the ECFA study.

2.4 Financial status

The previous award was £110k for equipment, £111k of travel, 20 staff months (SM) of RAL/ID effort and two years of funding for an RA at Cambridge (the post filled by G. Mavromanolakis). There was no working allowance or contingency included in the award.

The equipment cost has come in very close to the budget. The exact total will not be known until the final seven UK boards are assembled and the high performance DAQ PC purchase is complete, but the projected total is within a few £k of the award. The remaining purchases will all be completed by the end of this FY.

Travel has been significantly underspent as the original schedule had the first FNAL test beam within the two years of the previous grant and this was a major fraction of the travel budget. This beam test has been delayed until later this year, moving it into the period of the current proposal. Again, the exact total which will be spent on travel by the end of FY04/05 is not yet known, but is estimated to be £50k.

In contrast, the staff effort needed was underestimated. RAL/ID has charged us a total of 25 SM, a 25% increase on their original estimate. This extra effort, costing around £30k, has been funded from the unused travel funds, leaving a projected £30k of travel unspent.

The RA post was filled in August 2003, which means there is almost four months of funded RA effort remaining to be used in the next FY. In addition, there was some staff effort at the Universities and RAL/PPD allocated to the CALICE ringfence beyond FY04/05, i.e. after the period of the previous approval.

However, to prevent any ambiguity, for the purposes of this proposal we ignore the unspent travel and staff funds and treat all future costs beyond this FY as part of the current bid, without assuming anything will be carried over.

3 Workpackage 1: Completion of CALICE test beam program

In our original 2002 application to the PPRP, we requested three years of funding to support the construction of the CALICE ECAL prototype, and its exposure to test beams with a variety of HCAL prototypes behind. In this workpackage, we are seeking the remaining funding to complete this program. This essentially consists of: travel funds to participate in test beam running and related CALICE meetings; some DAQ development effort, particularly when the HCAL detectors are integrated into the system; and staff effort so that the UK simulation expertise built over the past two years can be fully exploited in the analysis of the data.

3.1 Beam tests

To support the beam tests, technical work is needed to maintain and enhance the DAQ system. This is in both the firmware for the UK readout boards and also the online software. In addition, UK personnel will need to take part in the data-taking work, participating in shifts and other activities at the beam area.

Task 1.1: Support for beam tests

The firmware for the readout board FPGAs is still under development. In particular, some modifications for the AHCAL will be needed and further work to increase the maximum trigger rate and reliability is needed. This should be completed within the next nine months.

The software is also still under development. The ECAL tests performed so far only required a single VME crate system, which allowed synchronisation relatively simply. However, when the AHCAL tests begin later this year, a multi-crate system will be needed, which will most likely be implemented using multiple readout PCs. This additional functionality exists but has not been extensively used and so will need to be thoroughly tested over the next six months.

The work required may be summarised in the following tasks:

- Improvement of the firmware for the reliability, speed, trigger latency and functionality. There is currently a low rate of lost triggers, thought to be due to the asynchronous trigger timing in the BE firmware and this needs to be cured in order that the readout is completely reliable. Another issue is the data readout rate; firmware work is needed to optimise the data output rate from the boards so as to be sure of achieving the 100 Hz requirement with the full system. In addition, the trigger latency is constrained to be 180 ns by the shaping time of the VFE ASIC preamplifier. While this has been achieved in the cosmics tests, it is a tight constraint and so any extra overhead which can be gained for the DESY and FNAL beam tests would be useful. Work on the trigger path in the firmware could potentially gain back at least 10 ns. Finally, extra functionality in the firmware, particularly in the trigger data buffering and readout, would allow better diagnostics and pile-up rejection.

- Enhancements of the firmware for the AHCAL are needed. Although the physical readout boards will be identical to those for the ECAL, some of the I/O signals from the front panel connectors will be used for different purposes. This requires them to have different FE firmware to drive and receive the data.

- Enhancement of the software for the AHCAL and DHCAL integration are also needed. The DAQ has been written to allow a straightforward extension to multi-PC operation, where the trigger itself is used as the synchronisation marker and unsynchronised inter-PC communication and control uses socket calls. This remains to be implemented.

- Running shifts and general maintenance of the electronics during the beam tests.

3.2 Analysis and simulation

The simulation work already performed in the UK has contributed significantly to the planning for CALICE test beam running. Some of the key points to emerge are as follows:

- Our broad objective is to characterise the properties of hadronic showers to 1% precision, which therefore demands samples of at least 10^4 events. Monte Carlo studies have shown that significant differences between models are seen with such a level of statistics.

- Differences between the predictions of models have been seen over a wide energy of energies, from 1 to 50 GeV. This is therefore the range of hadron energies we would wish to study, which covers the range of typical energies of hadrons in jets at the ILC.

- The differences between models are different for baryons and mesons. It is therefore desirable to obtain data with both proton and pion beams. We have checked that the effects seen in Monte Carlo for neutral hadrons are similar to those for charged hadrons.

- We shall wish to perform position scans across the calorimeters (probably by exploiting the natural width of the beam) and to record data at several angles of incidence in the range $0°$ to $45°$.

This work divides naturally into two phases – tests of the ECAL alone in an electron beam, and combined tests with the CALICE HCAL prototypes in hadron beams.

Task 1.2: Analysis of DESY test beam data

The CALICE ECAL prototype is being moved to an electron test beam at DESY in January 2005. We expect the complete prototype to be fully equipped by April 2005. The data taking at DESY will continue beyond this, with the completed calorimeter taking data up to July 2005. During this period, we shall record electron data with energies in the range 1–6 GeV. This phase of operation will be of great importance in commissioning the hardware, and in starting to understand the problems associated with real data.

In addition, the data analysis will clearly continue through much of 2005. The electron beam data, together with cosmic muons, will be of great importance in understanding the detector response, and in tuning the Monte Carlo to describe it. The current Monte Carlo describes the raw $\mathrm{d}E/\mathrm{d}x$ energy deposits in the silicon pads, but clearly the UK groups will have a key rôle to play in adding realistic simulation of electronics effects such as noise and crosstalk. First versions of this exist [25], but will require tuning and adjustment in the light of experience.

The electron data will also be of importance in tuning parameters of the Monte Carlo simulations. Our early studies have shown that the simulated detector response is somewhat sensitive to details of the low-energy particle transport (such as tracking cutoffs or the precision with which multiple scattering is followed); these details can easily change the response by a few percent. Before assessing the hadronic response, it will be important to tune the simulations to model the electromagnetic response in data.

The generation of preliminary Monte Carlo samples, the establishment of an analysis framework, and first comparisons between data and Monte Carlo will already have been done by the end of FY04/05. The remaining work required may be summarised in the following tasks:

- Understand the properties of the DESY beam; implement a realistic simulation of the beam and of the beam defining detectors (MWPCs).

- Understand and tune the detector response in the light of real data. In particular the UK groups will be needed to simulate the behaviour of the electronics, building on existing work [25].

- Generation of sizeable Monte Carlo samples will then be able to begin. This will use RAL CSF as well as CPU resources in the Universities. Work is also starting at Imperial to port the simulation code to the Grid.

- Continue data and Monte Carlo comparisons throughout. The aim is to ensure that both `Geant3` and `Geant4`, and probably `Fluka`, are all tuned so as to be capable of describing the electromagnetic response (electrons and muons) of the CALICE ECAL.

- Publish the results of this work, along with a technical description of the detector.

Task 1.3: Analysis of FNAL test beam data

CALICE has applied to Fermilab [26] for time on the MTBF (Meson Test Beam Facility) test beam. This is a recently commissioned, general purpose facility which can provide a proton beam of 120 GeV and secondary hadron beams in the energy range $\sim 5 - 80$ GeV, matching our needs well. The secondary beam will contain both pions and protons, and is equipped with Čerenkov counters for particle identification, and MWPCs for beam definition. Electrons should also be available.

Our present expectation is that we shall expose the ECAL prototype in the Fermilab beam in autumn 2005. For this run, it will be placed in front of the analogue HCAL prototype and a tail catcher, so as to provide complete instrumentation of hadronic showers. For this configuration, we shall wish to record samples of data, typically of order 10^6 events, over a wide range of energies, for example 10-15 energy points ranging from 5 to 50 GeV. In addition, data at non-normal incidence should be recorded at a few energies.

As part of the preparations for the test beam, we have also performed studies [9] which demonstrate that, in the unlikely event that there are problems or delays with the HCAL prototypes, an exposure of the ECAL prototype to a hadron beam (particularly if additional tungsten absorbers were placed in front) would yield valuable information, especially for low energy hadrons. It is also important, of course, to record data on the performance of the Si-W ECAL in higher energy electron beams than available at DESY.

A key part of the CALICE programme is to compare different detector technologies for the HCAL. Specifically, RPCs and GEMs with digital readout are being designed. The main limitation on this is funding for the RPC electronics (which would also be used for the GEMs), and for this reason we envisage that the digital HCAL tests will not occur until 2006. We shall have a clear responsibility to keep our DAQ and electronics working throughout the test beam program, and an obvious intellectual interest in contributing to the interpretation of the results, using our expertise in the simulation area. We can therefore envisage some limited activity continuing well into 2007.

The work required may be summarised in the following tasks:

- Maintainenance of our capability of using the `Geant3`, `Geant4` and `Fluka` hadronic codes, and also of using relevant new models which become available in `Geant4`.
- Understand the properties of the hadron beam, and how to use the beam detectors for particle identification and definition of the beam position. We shall need to implement a realistic simulation of the beam, and of the beam defining detectors (MWPCs and Čerenkovs).
- Generation of sizeable Monte Carlo samples. This will use RAL CSF as well as CPU resources in the Universities and on the Grid.
- Comparison of data and Monte Carlo, for many different hadronic models. Tuning of beam simulation and detector response as required, and iteration. This process will clearly start as soon as data are recorded, with the aim of identifying those models which provide an adequate description of data.
- Repeat the above tasks for the digital HCAL.
- Publication of findings on the properties of hadronic showers, and on comparisons with models.

4 Workpackage 2: Data acquisition

The design [4] for an ECAL calorimeter for a future ILC detector poses challenges to the data acquisition system (DAQ) mainly due to the large number of channels to be read out. In this work package we propose to address some of the key issues envisaged.

A generic scenario for the DAQ system is as follows. Mechanically, the calorimeter will consist of around 6000 slabs, each of length 1.5 m, and each containing about 4000 silicon diode pads of $1 \times 1\,\mathrm{cm}^2$, giving a total of $\sim$24 million pads. At the very front end (VFE), ASIC chips will be mounted close to the silicon wafers. The ASICs will perform pre-amplification and shaping and should also digitise the data and *may* even apply threshold suppression. The current design [27] for such chips has 16 channels, although this may be higher in the final calorimeter. The data will be digitised in the ASIC and the data transferred to the front-end (FE) electronics which are placed inside the detector at the end of the slab. It is expected that threshold suppression will be done at the FE in FPGAs to reduce the data volume significantly. The data will then be transferred, probably via a switch, to an off-detector receiver which may be PCI cards in a PC farm.

If we assume the bunch timing of the 800 GeV TESLA design, the following parameters have to be considered. There will be a bunch crossing every 176 ns, with 4886 crossings in a bunch train, giving a bunch train length of about 860 μs. The bunch train period is 250 ms, giving a duty factor between trains of about 0.35%.

In a shower, up to 100 particles/mm^2 can be expected, which in a $1 \times 1\,\mathrm{cm}^2$ pad equates to 10,000 minimum ionising particle deposits. The ADC therefore needs a dynamic range of 14 bits. Assuming 2 bytes per pad per sample, then the raw data per bunch train is $24 \cdot 10^6 \times 4886 \times 2 = 250$ GBytes which equates to 0.3–2.5 MBytes for each ASIC (assuming they each process between 32 and 256 channels, as expected for the final design). These data are generated within a bunch train length of 860 μs giving a potential data rate out of the ASIC of 0.4–3 GBytes/s. Threshold suppression and/or buffering (to allow readout between bunch trains) within the ASIC could reduce this rate. However, suppression in the ASIC may not be flexible enough compared with doing this in the FE and buffering requires some ASIC power to remain on between bunch trains, potentially generating too much heat. Hence the rates after the VFE depend on the assumptions and system layout and will be discussed for each individual case where necessary.

In this proposal, DAQ equipment will be developed which attacks likely bottlenecks in the future system and is also sufficiently generic to provide the readout for new prototype calorimeters. Alternative designs of a DAQ system which could affect the layout of the final detector or functionality of components are also considered. For example we consider a setup where more information is processed on the ASIC or off the detector and hence there is no need for FE electronics. This could save space, and hence cost, and reduce the amount of heat dissipated inside the detector.

The proposal is split into five tasks which investigate the three principal stages of the DAQ system: the connection from the VFE to the FE; the connection from the on- to off-detector; and the off-detector receiver. A strong under-pinning thread here is to attempt to make use of commercial components and identify any problems with this approach.

The programme detailed below will allow us to continue assisting development of new technologies for the DAQ system. We would expect to write a chapter in the future technical design report on the DAQ system for the calorimeter. For the final calorimeter, the DAQ should ideally be the same for the ECAL and HCAL. Although CALICE-UK has so far concentrated on the ECAL, our proposals for R&D contained in this document are sufficiently generic that both calorimeter sections should be able to converge to use the DAQ system we design. This will place us in a leading position to build the DAQ system for future large-scale prototype calorimeters and the final system.

4.1 Connection from the VFE to the FE

There are two tasks within this area.

Task 2.1: Readout of prototype VFE ASICs

The current version of the VFE ASIC chip [10] is being used to read out the existing CALICE ECAL. This chip does not meet the requirements for the ILC ECAL and the development of the design is an ongoing project in LAL/Orsay. In the next 1–2 years, they expect to have a version of such a chip with low enough power and noise that would serve as a realistic prototype. This ASIC is expected to have 16 channels, an internal ADC per channel, multiple gain ranges, and optional threshold suppression and digital buffering to reduce the required output rate. They expect to submit the ASIC for a fabrication round roughly once per year in early summer. We propose to build simple readout systems to study these ASICs.

The steps in this task are as follows:

- The LAL/Orsay group produce single-ASIC PCBs to study the chip performance. They will supply us with some of these PCBs with chips from each production round. This will allow us to understand the chip clocking and control.
- We propose to design build a PCB to hold at least 32 chips, thereby reading out about 500 channels. This would need to use the threshold or buffering option to keep the rate low enough for straightforward readout.
- We will then mount and test multiple VFE ASICs on the PCB to give us practical experience in the associated issues of clock, control and configuration of these prototypes in bulk, as well as allowing studies of pedestal and noise stability. How these chips behave will significantly influence the design (and cost) of the final on-detector DAQ readout system and so early data here will be invaluable.

A similar PCB readout system as used to readout the MAPS PCBs (as detailed in Section 5) would be used, thereby consolidating firmware effort. This UK activity is obviously paced by the work of the LAL/Orsay design team so is anticipated that activity will start in the middle of the second financial year but will be mainly concentrated in the final year.

Task 2.2: Study of data paths over 1.5 m slab

If threshold suppression or buffering could be done in the VFE ASIC, the rate to the FE would be reduced by two orders of magnitude. Current designs cannot do this and it may not even be desirable or practical, so we have to allow for data rates of order GByte/s needing to be transferred out of each VFE ASIC during the bunch train. Whether an electrical or optical connection would be needed has to be investigated. Although chip-to-chip fibres are not yet standard technology, this is an active area of industrial research [28].

The construction of a 1.5 m long fully operational calorimeter prototype is unlikely on timescales of the next few years. However, issues of how the data would be transported from the VFE to FE have to be considered and can be done already without a real prototype. Transporting of order GByte/s of data over 1.5 m in a very limited space is a challenge. The conventional approach would be to use copper but here the effects of noise and interference will have to be considered. There is also the possibility of using optical fibres although here there are also design considerations: the size of connectors would have to be investigated as the vertical clearance at the VFE is of the order of mm and the power needed to transmit light out would also need to be investigated. This work ties in closely with the mechanical and thermal aspects of the design as discussed in Section 6.

The steps in this task are as follows:

- In preparation for a real prototype, we propose to build a test system with a 1.5 m PCB containing FPGAs to emulate the VFE and FE, linked electrically. This would begin with two 500 mm PCBs for initial tests and investigations before moving onto three 1600 mm PCBs for final tests.
- The bandwidth and cross-talk of the data transfer will be simulated using CAD tools and compared with measurements from the PCBs.
- The clock and control distribution from the front-end to the VFE chips will be investigated to determine whether one transmission line per chip is needed or multi-drop is possible.

This task would run over the three years of the proposal.

4.2 Connection from on- to off-detector

In this section, we consider two possible scenarios:

Standard Configuration. In our assumed standard detector configuration, communication from the VFE will pass via the electronics at the FE to an off-detector receiver. We assume that threshold suppression will be done at the FE, and hence the rate would be significantly reduced from that at the VFE. Assuming that the rate is reduced to 1% of the original data volume of 250 GBytes per bunch train and each sample above threshold needs channel and timing label, the total data volume to be read out from the calorimeter is about 5 GBytes or about 1 MByte per slab. These data have to be read out within a bunch train period of 250 ms, giving a rate of 5 MBytes/s.

Alternative configuration. Here we imagine that the FE is removed and the communication is directly from the VFE to the off-detector. The need for FE electronics becomes questionable if more processing is done on the ASIC chip, such as threshold suppression. In such a scenario, transporting the data directly from the ASIC off the detector could be done and so the FE would become redundant. The number of fibres required to read-out the 24 million channels would vary between 750 000 to about 90 000 depending on whether the ASIC handles 32 or 256 channels. If we assume that the diameter of a fibre is 150 μm, or with cladding 250 μm then if half of the circumference of 12 m had fibres running along it, the bundle would be up to 1 cm in depth, but could be as little as 1 mm, depending on the number of ASICs and hence fibres. This would leave ample room for other cables and power supplies. This concept would revolutionise the whole calorimeter design and so needs to be considered now when changes in its general structure could be considered. Our research in this area will provide important feedback to groups designing the ASIC chips.

The off-detector receiver, as described later, is assumed to consist of PCI cards housed in PCs. As PCs are not 100% reliable, a switch will be necessary to send data efficiently to working PCs. The standard scenario would require less high-speed equipment off the detector, whereas the alternative would require many optical fibres with dedicated optical switching. The alternative scenario would, however, remove material from inside the detector which would ease construction and have a potentially advantageous impact on event reconstruction and, hence, physics measurements. It would also reduce the number of processing components within the detector which could be attractive since they would be inaccessible for long periods of time.

Task 2.3: Connection from on-detector to the off-detector receiver

We propose to set up a test system to validate the effectiveness of high-rate switching. This will investigate the issues in directing multiple 10 Gbit data flows with the linear collider time structure to high-performance processors.

The steps in this task are as follows:

- The test system will consist of four 10 Gbit ethernet interfaces each housed in a high-performance PC. These will be connected to six 1 Gbit ethernet PCs capable of driving data through the system. The 1 Gbit network interface cards will be a mixture of different cards and characterising them will be part of the goals of the project.
- After building the system, a series of tests will be done. Firstly the network interface cards, motherboards and network switch will be characterised considering jitter, latency, throughput, etc.. Then simple data flows will be examined for different scenarios. Finally the data flow will be examined for rates expected from the accelerator timing structure.
- To investigate the alternative, we propose to set up a test system to validate the use of fibres to transport the necessary data rates from the VFE to the off-detector receiver and to ascertain whether an optical ("layer-1") switch can re-route data with high efficiency. The test setup would contain a bundle of fibres coming into a switch from an effective VFE. A bundle would then come out of the switch to the off-detector receiver. The off-detector receiver, to be produced as part of Task 2.5, would be a set of PCI cards housed in PCs. The same PCI card would be used in our test system to emulate the VFE chip.
- The optical switch efficiency would then be tested when PCs fail and the data have to be swapped to another PC. Also if a PC contains a large amount of interesting data and takes up a large amount of processing time, a busy signal would be sent to the optical switch which would again re-route new incoming data. As it is assumed that some clustering will be done on the PCI cards, overlaps in geometrical areas of the calorimeter will be necessary. Therefore, the optical switch would also have to be able to send the same data to different PCs. The test system would consist of an optical switch connected via optical fibres to the PCI cards housed in PCs. We assume scalability of the optical switch, so we would use a relatively small 16×16 lane switch.

Task 2.4: Transport of configuration, clock and control data

In a scenario requiring an FPGA on-detector at the front end, it is imperative that the device can be re-configured remotely. This is necessary not only because of the number of FPGAs but also because of the uncertainty in the detector performance, in terms of data suppression, pedestal drifts, bad channel identification etc., all of which have to be implemented in the FE FPGA. The optimal algorithms for these tasks will only be determined after some experience of operating the calorimeter. However, this is complicated by the relative inaccessibility of the devices so that a failsafe system is required. To facilitate this, some sort of non-volatile memory that boots the device into a communicative state, or an external control system that provides an interface between the unconfigured FPGA and the outside world is required. Using devices with non-volatile memories built-in may have advantages here, but increased cost and limited re-programming cycles make these less attractive. Questions surrounding the reliability in the detector environment of these memories over the lifetime of an experiment also need to be addressed. In contrast modern SRAM-based FPGAs boast that they can re-configured infinitely and can therefore be 'refreshed' at regular intervals to ensure their configuration is not corrupted. The option of running with different firmware for different types of run is also attractive. Reducing the number of components on the front-end-module would be advantageous from a cost, reliability and dead material point of view. In this task we propose to research a means of connecting a commercial network receiver package to an FPGA with the absolute minimum of components, so as to reliably reset and configure the device remotely.

To ensure the on-detector electronics captures data from actual collisions all components in a detector system need to be synchronised to a bunch-crossing clock. Although a 'trigger-less' system is envisaged it is still useful to consider a signal that moderates readout, such as 'bunch-train-start' signal. One of the scenarios considered in this proposal makes use of standard network protocols to tag data at the front-end such that a commercial network can deliver it to a waiting event-builder PC. To co-ordinate this requires that busy information from the event-builder system is used to derive available data destinations that needs to be sent to the front-end. This can be called a trigger ID at some level. Although the need to build a large scale system is still some way off, the means of interfacing these time-dependent signals into the more asynchronous commercial network arena needs to be understood. The aim of this task is to investigate means of distributing clock and control signals using commercial networking equipment and components, as opposed to a more traditional bespoke system. This couples well with the work of investigating the FPGA failsafe in that it attempts to minimise components and connections on the front-end-module. In many ways this will be an investigation to verify that a single clock, control and configuration system can be constructed using a commercial hardware for both receiver and transmitter hardware. Although it is envisaged that fibre optic will be the dominant communications technology in a final design, lower speed copper based systems are sufficiently similar to allow the first stage of development to use this technology.

The steps in this task are as follows:

- We will consider a literature survey of the response of various FPGAs to radiation and rates of single event upsets and how to circumvent them.
- A simple test system for the failsafe studies will be set up, requiring a PC with a network card and a development board with cables and connectors.
- The clock and control test system will build on the previous FPGA failsafe work and use much of the same equipment. Additional network cards, a fanout board and switch will be required.

4.3 Off-detector receiver

An ideal system would have all data from the detector for each bunch train sent directly to a single PC where full event reconstruction would be performed. However, considering that the calorimeter alone will contain more than 20 million channels, even after data suppression this seems unfeasible.

It would, however, probably be desirable to get as much of the calorimeter into one processor as possible. This would permit local clustering which could be used as an input to full event reconstruction later. The fundamental questions to be answered are how much of the calorimeter can be received into one PC and how much needs to be received to make local clustering effective. The impact this has on full event reconstruction and on simulated physics needs to be evaluated. This task therefore involves a combination of hardware and simulation work.

Task 2.5: Prototype off-detector receiver

We propose a system comprising PCI cards mounted in PCs. These cards will be capable of performing local clustering, as well as being able to be reconfigured to act as data transitters to excercise the receivers. Recent developments in PCI cards have led to high bandwidth which is scalable due to future increases in the number of lanes using PCI Express technology.

The steps in this task are as follows:

- We will use cards based on this technology using a PCI Express bus. We propose to design and build our own PCI card to provide maximal flexibility for the tests we wish to perform.
- We would build a test system consisting of 4 PCs each with a PCI card in them and the possibility to move PCI cards between PCs so as to maximise the data rate to a single computer. To act as the VFE or FE sending the data, 4 further PCI cards would be required, housed in two PCs. Two rounds of prototyping of two cards would be done before building the final eight. In the test system, they would also be used to emulate the VFE or FE sending data off detector.
- In conjunction with the network workpackages discussed previously, tests will be made to see how efficiently data are transferred if a PC is unreachable or busy. Although it is hard to predict what technology will be available for the final system, gaining experience of cutting-edge technologies now, such as PCI Express, will prove valuable for estimates of how much data can realistically be received by each computer. So, whilst not trying to absolutely maximise the amount of data which can be transferred into a PC in the test system, the model should be scalable.
- With sufficient data transported to one computer local clustering and removal of isolated hits can be performed before full event reconstruction is done offline. This would involved firmware programming of the FPGA on the PCI card, its simulation and subsequent effect on full reconstruction and performance in a physics analysis.

5 Workpackage 3: Monolithic active pixel sensors

5.1 Introduction

All studies for a Si-W ECAL for the ILC currently consider diode pads as the sensitive elements in the silicon wafer. However, mainly outside the ILC community, work on monolithic active pixel sensors (MAPS) has developed this technology to a level of maturity such that they can now be considered as a possible alternative. The main goal of this workpackage is to study the use of MAPS for an ILC ECAL and, over the three year period of the grant, to either validate this concept or show that it is not a feasible option. If MAPS are a viable alternative to diode pads, then working to this timescale would allow the UK to contribute to the detector TDR in this area and would place MAPS as a technology being considered in which the UK would have clear leadership.

MAPS have been developed over the last decade for imaging purposes, but their application to PPARC science really took off with the collaboration led by R.Turchetta. This group has been supported by PPRP seedcorn funding for the last two years [29] and this sucessful project has attracted interest for tracking applications not only from the vertex detector groups involved in the ILC, but also for SLHC applications. However, as far as we are aware, there is no other proposal to use MAPS in a calorimeter.

MAPS implement both the sensitive silicon detector and the readout electronics onto the same wafer, using standard commercial CMOS processes for fabrication. The actual charged particle detection is done using electron-hole creation in the epitaxial layer. This is of order $10\,\mu$m thick and is located immediately below the surface layer where standard CMOS circuitry can be implemented for readout. The charge liberated diffuses within the layer and is collected by contacts passing from the surface electronics to the epitaxial layer.

The basic concept which this workpackage will develop is to use MAPS with binary readout on the sensor pixels. The channel count is extremely high and so analogue readout would produce prohibitive amounts of data. By making the pixels small enough, the probability of more than one minimum ionising particle (MIP) passing through each pixel can be kept small. Hence, a single bit to indicate the presence of a MIP is sufficient information. The data would then be stored during the bunch train in memory implemented within the pixel and read out before the next train. This idea is described in more detail in the following subsection; a more complete description of the conceptual design of a MAPS ECAL can be found in [30].

5.2 MAPS concept

To be able to use binary readout for MAPS pixels, the probability of multiple charged particles per pixel must be small. Simulations show the density of charged particles in the core of a 500 GeV electromagetic shower is around $100/\text{mm}^2$, which implies pixel sizes of at most $100 \times 100\,\mu\text{m}^2$, although an actual size of $50 \times 50\,\mu\text{m}^2$ is more realistic. This results in a huge pixel count; for an ECAL the size of that in the TELSA TDR [4], this would be around 10^{12} pixels. The only possible way to handle such a large number of channels is to do a huge amount of data processing directly at source and so build data suppression into the MAPS sensor itself. This can then reduce the data volume which needs to be stored and subsequently read off the sensor to a manageable level.

Since the MAPS sensors have similar mechanical and thermal properties to diode pad wafers, the structure of the ECAL is somewhat independent of which is used. However, since the MAPS actually measure different physical quantities and have no external readout electronics, there are several advantages to using them over diode pad wafers:

- **Energy resolution.** The proposed MAPS would essentially measure the number of particles passing through the silicon, rather than the energy deposition which the diode pads measure. While these two measurements would be expected to be correlated, the energy deposited is smeared out due to Landau fluctuations, non-normal incidence and the velocity dependence of the ionisation rate. Preliminary simulation studies show the higher quality MAPS information improves both the energy resolution and the linearity for electromagnetic showers from single electrons, as shown in figure 6.

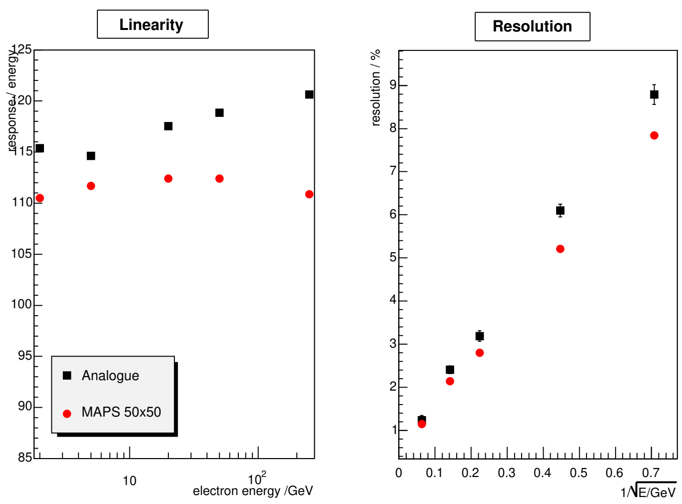

Figure 6: *Linearity (left) and resolution (right) of the ECAL response to electron showers as a function of the incident electron energy for an analogue (diode pad) and a MAPS calorimeter.*

- **Pattern recognition.** The granularity of the MAPS ECAL is much finer than for the diode pad option, by two orders of magnitude. The natural spread of the showers prevents this from having as dramatic an impact on the cluster reconstruction, but improvements on quantities such as two cluster separation are seen in simulations, as shown in figure 7.

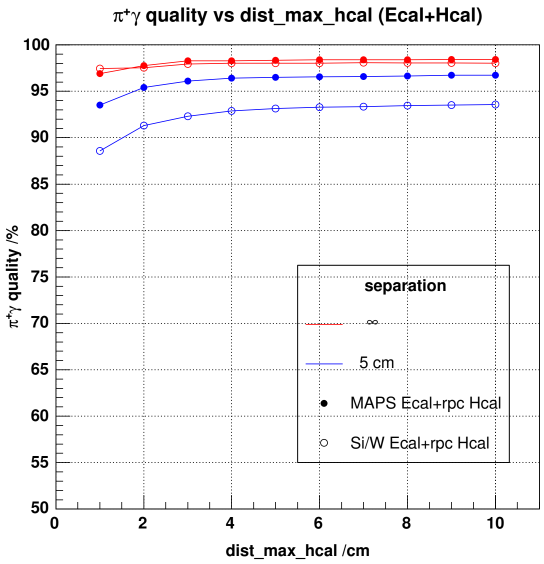

Figure 7: *Reconstruction quality (as defined for figure 5) as a function of the main clustering cut for a diode pad and a MAPS calorimeter. The clustering algorithm was developed for the diode pad option and has not been retuned for the MAPS case.*

- **Size.** The absence of a VFE ASIC readout chip on the detector results in a significant reduction of the VFE PCB module thickness, potentially by around a factor of two. This impacts in several areas. The gaps between the tungsten layers can be correspondingly reduced, giving a smaller shower spread between layers and hence decreasing the effective Molière radius. This contributes directly to improved pattern recognition between layers. In addition, the radial thickness of the ECAL can be reduced by around 10-20%, with a subsequent decrease in cost not only of the ECAL itself, but also of the HCAL and the solenoid magnet, both of which lie outside the ECAL. This could be a significant saving; the magnet cost alone is estimated to change by around \$2M per cm radius [31].

- **Thermal issues.** The main heat source in the ECAL is in the readout electronics. For the diode pad option, this is concentrated in the small, packaged VFE chip. For the MAPS option, the heat production is spread evenly over the whole surface of the bare sensor, which has an area larger by two orders of magnitude. This makes a good thermal contact much easier for the MAPS case, reducing the problem of heat removal.

- **Cost.** The cost of a Si-W ECAL is large and is dominated by the surface area of silicon needed. Even with estimates of around \$2/cm^2 for processed high resistivity silicon by 2010 (a factor of five below current prices), the silicon alone in the TESLA TDR ECAL would cost \$60M. While the price of such wafers in several years' time is hard to predict, the relative cost of diode pad type wafers compared with standard CMOS processes, as used for MAPS, is potentially less uncertain. Currently, ignoring non-recurrent costs which will be negligible compared to the wafer costs in the final system, high resistivity diode wafers cost around a factor of two more than CMOS. Thus, there is potentially a large reduction in the dominant cost of such an ECAL through using commercially standard, widespread fabrication methods.

However, despite these potential advantages, there are several issues which need to be studied before MAPS can be considered to be a viable alternative to diode pad wafers. The main issues are:

- **Signal/noise.** To operate with binary readout, a good signal/noise ratio must be achieved. To achieve a high efficiency, as required for good pattern recognition, the threshold must be set well below the most probable MIP level. Specifically, the actual deposited energy can be as low as 70% of the most probable value, or possibly even less if a very thin epitaxial layer is needed. To be efficient, it is necessary to set the threshold at least 2σ below this level, where σ is the r.m.s. noise. However, in order not to get too many noise hits, the threshold must be at least 4σ or even 5σ. This leads to a requirement of a signal/noise ratio of at least 10/1, which means a noise hit probability of around 10^{-6}; a non-trivial requirement. The signal depends on the epitaxial thickness, while the noise in MAPS tends to be dominated by the reset; schemes allowing "soft reset" to minimise this are being studied. Given the assumed relatively long time of several hundred ns between bunch crossings and the low physics rate at the ILC, an alternative approach would be never to reset, but instead to let the charge leak off with a characteristic time of the same order.

- **Crosstalk.** As stated above, the binary nature of the proposed MAPS readout gives a good measure of the number of particles passing through the silicon and is expected to improve the energy resolution. However, if each charged particle often resulted in more than one binary hit being recorded per layer, this potential improvement could be lost. Such crosstalk effects would result from inefficient charge collection in the epitaxial layer leading to longer diffusion distances and hence charge being collected by neighbouring pixels. In addition, a thick epitaxial layer compared with the pixel size dimension would cause more charge sharing between pixels for tracks at non-normal incidence, as they would be more likely to cross the epitaxial layer beneath two pads. The design of the collection pads needs to be optimised to reduce the former effect. Minimising the epitaxial layer thickness will reduce the latter effect, but at a cost of directly reducing the signal size; the balance of these two will be a major part of this study.

- **Uniformity and stability.** The binary readout needs a threshold to determine if the bit should be set or not. There are far too many pixels to allow each threshold to be set separately for each pixel, so the MAPS must be made uniform enough at least so the pixels within each sensor can operate with a common threshold. In addition, there are likely to be thermal fluctuations as the electronics is powered on and off with the bunch trains. If the threshold is not stable with temperature then this would result in excess noise or loss of efficiency.

- **Power.** One of the major problems with the mechanical structure of a Si-W ECAL is how much cooling will be required and how it would be implemented; indeed the workpackage described in Section 6 proposes that the UK become involved in these crucial studies. It is clear that the MAPS option would need to be at least similar to the diode pad option in terms of total power dissipation to be taken seriously. Techniques to reduce the power consumption, such as powering on the comparators for the shortest possible time, will form part of the work programme.

5.3 MAPS concept verification

The aim of this workpackage is to investigate all of these and evaluate whether MAPS sensors are feasible for this application. There is only one task as this work cannot be sensibly subdivided into independent parts.

Task 3.1: Sensor production and testing

It is foreseen that two rounds of sensor fabrication will be required to get a design close to the specifications needed. The first design will test several different ideas within the same sensor, while the second fabrication round will produce uniform sensors iterating on the best design found in the first round. For the fabrication, we are planning to have two dedicated runs, probably in a $0.35\,\mu$m CMOS sensor process. Since larger sensors (potentially close to the full size of a wafer) may be needed in the long term, the choice of foundry may be influenced by their ability to integrate large structures in the future.

The steps in this task are as follows:

- There will be an initial feasibility study during the first three months to look at design options and limitations resulting from physics needs. This will reduce the number of possible designs to the level that the remaining designs can be implemented into one sensor.

- The first production round will produce small sensors, around $1 \times 1\,\mathrm{cm}^2$, which means around 40k pixels total per sensor. Four good wafers are guaranteed (although more may be available if the yield is good), which would result in around 800 such sensors. The sensor will contain pixels with a number of designs, allowing comparisons of various ideas without needing a production run for each. It is estimated that the design of this first sensor will take around 14 months, with the fabrication of the sensors being completed 18 months into the grant period. The sensors will be tested electrically for correct functionality and then studied to measure their properties using sources, cosmics, a 5 T magnetic field, etc. Control, clocking and readout would be supplied by using a commerical FPGA development board connected directly to a PC. These tests will take the next six months to complete.

- The iteration of the design for the second fabrication round will take around six months, much of which will happen in parallel with the tests of the first batch of sensors. The fabrication run itself should be completed by month 30. The sensors will be the maximum size allowed within standard CMOS processes without stitching, which is $2 \times 2\,\mathrm{cm}^2$. The sensors will have a uniform design for all pixels and the four wafers would produce 200 sensors, or more if the yield is good. These sensors would again be subjected to similar tests to the first fabrication round.

- Several of these sensors will be put into a test beam. If they are mounted on a PCB with the same dimensions as the CALICE ECAL wafer PCBs, then one or two layers of diode pad wafers could be replaced by MAPS sensors within the tungsten structure used for the CALICE beam tests. This would allow a direct comparison of MAPS against diode pads. It would also allow some study of possible single-event upset effects resulting from dense electromagnetic showers passing through the MAPS sensor circuit. To cover the same surface area as a full VFE PCB, namely $12 \times 18\,\mathrm{cm}^2$, would require 54 working sensors per layer. Hence, at least two layers would be equipped in this way, although with a good yield, more would be possible. The PCBs to hold and read out such a number of MAPS sensors would require significant design effort. The control and readout would also be more complicated than for the single sensor tests. However, the existing CALICE readout boards have the flexibility to do completely digital I/O, by setting jumpers to bypass the ADC inputs and connect directly to the FE FPGAs. Hence, with some firmware development, the same boards can be used for both the diode pads and MAPS readout.

6 Workpackage 4: Thermal and mechanical issues

6.1 Introduction

We have identified a set of new linked topics which are important to the mechanical ECAL design but are currently not being pursued within the CALICE collaboration. The Manchester group will investigate these issues, which match their expertise in detector building, in particular in their most recent experience on ATLAS. The proposed work divides into three tasks as outlined in the sections below.

A further area of interest which was considered is the design of the endcap for the ECAL. There is currently no existing realistic design and this would be a major contribution to the collaboration, positioning the UK to play a visible and leading rôle in the experiment. However, it is a major task and we do not currently have the academic resources to pursue it. We are not including it in the present request, but may come back with a future proposal in this area if circumstances develop favourably.

6.2 Thermal issues

A theoretical and practical understanding of thermal management is a fundamental part of the detector design. If the experiment electronics overheats it will fail. However overconservative thermal policies will greatly add to the cost and complexity.

Task 4.1: Thermal studies

Heat is generated in the front end electronics, and flows through the readout boards, the tungsten and the carbon fibre. This process is critical to operation, as the electronics requires stable operating temperatures. It is also critical to the design, since placing the electronics processing as near the front end as possible would minimise the background pickup problems associated with small analogue signals going down long cables. However, the extent to which this can be done depends on heat and temperature considerations. These considerations are interlinked with each other, and also with the electronics design, making the studies interdependent.

We envisage the following stages in the work:

- **Power Dissipation.** We first need to check the power output actually produced by the existing readout chips, making actual measurements and cross-referencing them with manufacturers' data sheets, and to follow subsequent developments. This principally involves measurements of the VFE ASIC which does preamplification and shaping, and, in future versions, possibly digitisation and threshold suppression. The silicon detector pads will run at low power and should not contribute significantly to the thermal output, and a few simple measurements on wafers, as they can be briefly made available without impacting the assembly, should be enough to check this. The later FE FPGA circuitry will also require cooling, though this is less critical as there are fewer circuit elements and they are more accessible.

- **Thermal design.** We shall investigate the chip and circuit design to see what can be done to minimise heat production; in particular, to look at the possibility of cycling the chips so that they are only powered during the passage of the bunch train. This activity must continue as an input to the design process for the VFE and FE. Furthermore, if we move to MAPS sensors the issues of thermal stability and control will need to be re-examined.

- **Thermal modelling.** The heat flow from the source to the outside can be modelled using software already available and licensed. The process is in principle simple, although the non-isotropic thermal conductivity properties of the carbon fibre will require care. The key difficulty in this activity will be to ensure that the detector being thermally modelled really does contain all the elements and properties of a realistic design, requiring us to be well integrated with the rest of the design team.

- **Thermal Measurements.** The predictions of the thermal model must be validated against measurements to give them credibility. We will construct assemblies of silicon, tungsten and carbon fibre that mimic the detector design as currently proposed. Measurements will be done with thermal generators and sensors to increase our understanding of the thermal modelling and to validate it. As in the previous section, it is important that this model includes realistic features (fixings, extra brackets, etc) rather than just being a conceptual ideal. Through this approach the credibility of the thermal model should be established, and its use to inform the final design choices as we approach the TDR will be justified.

- **Cooling Technology.** We need to establish what temperature stability is actually required by the calorimeter (for its different proposed readout options). A pulsed-power solution, which would keep the heat down, has implications for the electronics front end. There is a provision for a thin (0.5 mm) aluminium cooling channel within the current design, which would use water. This has significant problems with pressure drops and temperature gradients over its long (3-4 m) length. This needs to be refined, for example by the use of binary freon rather than water, so that the whole pipe could be at the same temperature. The practical details of temperatures and flow rates need to be worked out, backed up by measurements as appropriate.

6.3 Mechanical issues

The bonding of the silicon detector to the readout PCB is by means of conducting glue. This assembly of the detectors onto the PCBs must also be done reliably and sufficiently quickly, to get the detector built on a reasonable timescale.

Task 4.2: Glue studies

The 1 cm^2 silicon detector pads are connected to the board by conducting glue. This connection has to persist mechanically, thermally and electrically for the entire lifetime of the experiment for each of the 24 mllion pads. Ageing techniques can be studied by thermal cycling in a programmable oven.

The steps in this task are as follows:

- **Study of existing glues.** Adhesives are widely used in mechanical design, and considerable knowledge exists as to their properties, both in general behaviour and specific examples. A first task will be a literature search to ensure that we benefit from existing research on the performance issues facing us, both for guidance in experimental technique and to ensure that we do not repeat measurements that have already been performed.

- **Glue characterisation.** We will conduct studies of existing adhesives through thermal cycling in a programmable oven, investigating the mean time between failures and the nature of such failures. We will also need to check whether the performance of the silicon as a particle detector is adversely affected by glue molecules diffusing into the semiconductor.

Task 4.3 Assembly studies

The assembly of 6000 boards, each involving the gluing of 4000 pads, is a major task. The detectors have to be positioned accurately and glued firmly, connections have to be made for the readout electronics, and the integrity of the whole board has to be verified. Information on the whole process has to be stored in a database for monitoring the progress of the build, and for later use.

This is in several ways similar to the building process for the ATLAS SCT currently being undertaken at Manchester; several of the people involved in this workpackage were responsible for the design of the automated alignment assembly system used for the construction of the ATLAS SCT Forward Silicon detectors at several sites. This achieved placement accuracies of a few microns. CALICE is larger, so the required position accuracy is correspondingly coarser at 50-100 μm, but the process has many similarities, and we will exploit this expertise for the CALICE detector assembly planning. We envisage the assembly process as proceeding along the following lines:

1. The required patterns of conducting glue are deposited onto the PC boards using a pneumatic glue dispenser mounted on a positioning robot. (We anticipate our existing SONY robot could be adapted for prototype tests.)

2. Silicon wafers are picked up on vacuum chucks.

3. Machine vision software with automated pattern recognition (based on Labview) is used to recognise fiducials and edges on the wafer and on the PC boards, giving precise coordinate information.

4. Large linear stages are used to move the wafer along the PCB 'plank'. These do not have to be high precision.

5. Small $x - y - \theta$ stages are used for the final alignment of the wafer. We may be able to re-use some of the ATLAS stages for this.

A large range of industry standard components and subsystems (extrusions, linear slides, vacuum pickups, controllers etc.) are available for building such machines from several manufacturers (such as Bosch and Paletti). Their use will make prototypes modular and minimise manpower costs for construction.

We propose the following program of work:

- **Robot design.** Design an automatic, or semi-automatic, process that will locate the detectors on the PCB with the desired position accuracy, applying adhesive and curing.

- **Robot prototyping and testing.** Based on the design, construct a proof-of-principle device that can demonstrably perform the assembly to the required precision and at the required rate.

7 Workpackage 5: Simulation and physics

7.1 Introduction

The successful design of an ILC detector, and in particular the expected call for detector TDRs in 2009, requires the development of much simulation and event reconstruction software during the next three years. Based on their work since 2002, the UK groups are now in a strong position to make leading contributions to this whole area, in addition to the ongoing simulation effort directed specifically towards the CALICE test beams themselves.

The major aim of the worldwide ongoing simulation studies is to design the optimal detector for physics at the ILC. This will inevitably require a compromise between high performance and realistic cost. This process will require two types of comparison. The first will be variation within a given detector technology, to find the optimal size, segmentation and design; the second will be a comparison of optimised detector designs for different detector technologies – this may ultimately be done after detector collaborations have formed. When comparing variations within a single detector technology it is clearly desirable to be able to use a single reconstruction algorithm in which the explicit dependence on specific geometric details of the detector is kept to a minimum. When comparing competing detector technologies this would also be an advantage, so that differences arising from the design and implementation of the reconstruction algorithm did not contribute significantly to the comparison. One possible approach is the development of generic tools which have at most a weak dependence on the geometry and technology of the detectors themselves, and which lend themselves to being easily adapted. The tools should also conform to common data structures and interfaces in order to facilitate comparisons.

The work is divided among four tasks. The development and study of energy flow algorithms will consume the greatest effort, followed in order of decreasing effort by simulation studies to support other work packages, optimisation of the global detector design, and physics studies.

Task 5.1: Energy Flow algorithms

Development of generic Energy Flow algorithm(s) will concentrate on analysis of physics processes, typically partial events which would test the performance of the algorithm using quantities such as two particle separations, single particle and jet energy resolutions. While several groups have presented work using energy flow algorithms, to date these have been closely coupled to particular detector geometries and simulation packages, making objective comparisons somewhat unclear. Work has already started in the UK to produce flexible and generic tools for calorimeter reconstruction (see Section 2.2), and we seek support to build on these developments, and to proceed to their use in a complete energy flow algorithm.

The goal of this work would be to deliver the design and implementation of an algorithm that lends itself to use across different detector designs with minimal adaptation, and which would be based on LCIO objects to facilitate this.

The work required can be broken down into the following tasks:

- Review of existing work/code (SNARK, REPLIC, etc.) and identification of factors which limit resolution. Identification of corresponding simple physics benchmark processes (linking all detectors, but in limited regions, e.g. t-quark decay, Z^0 jets). It will be important to maintain contact with other developers outside the UK.

- Algorithm brainstorming; at least two contrasting approaches to energy flow should be pursued. In part these may be based on the work already started in the UK.

- Definition of the tools required by the algorithm (e.g. calorimeter clustering, tracking, association).

- Controlled comparison of existing codes for a single process and detector geometry.

- First implementation of single new algorithm, and study of the interplay between hadronic modelling uncertainties and energy flow, making use of the new information accumulated from the CALICE test beam.

- Physics benchmark comparison, feedback on tools.
- Further algorithm development and evaluation/refinement. Clearly a good deal of iteration will be required at this stage.

Task 5.2: Global detector design

The optimisation of global detector designs will build upon the generic energy flow algorithms and physics studies. Physics analyses implemented within Task 5.4 will provide a set of representative performance measures for whole detector optimisation. The main aim of this design task will be to optimise individual detector concept(s) and to do so in such a way that the differences between optimised designs arise primarily from the detector configuration rather than the event reconstruction or implementation of the physics analysis used to gauge performance. This activity will require strong interaction with colleagues around the world.

The work required can be broken down into the following tasks:

- Use of first benchmark physics analysis (complete physics processes including background rejection) on first detector concept/parameter set.
- Application of analysis to alternative detector concepts (coordinated with activities of LCWS, ECFA etc.; not only a UK effort).
- Extension of study with additional physics benchmark analyses.
- Variation of detector parameters, such as radii of detector components, sampling frequency, transverse segmentation, resolution, magnetic field.
- Comparison of results leading to optimal design for each concept.

Task 5.3: Support of other workpackages

Expertise within the UK in the use of simulation tools will be an important resource for other workpackages to draw upon. Workpackage support is important to workpackages 2–4, each of which will require detailed simulations of the detector performance to inform design choices and determine the future direction of the R&D work. The timing of this work will be to a large extent dictated by activity in other workpackages and often closely linked to hardware developments.

We envisage that the work required can be broken down into the following tasks:

- Study of the impact of DAQ design on local clustering, etc.
- Study of the impact of passive material in alternative DAQ designs.
- Simulations of mechanical imperfections and their effect.
- Implementation of the geometry of MAPS detectors in `Mokka`, both for few wafer (prototype) tests and for the whole detector.
- Simulations supporting studies of various configurations of MAPS sensors.
- Simulation studies for the MAPS test beam.

Task 5.4: Physics studies

Physics studies are important as they will develop tools which can be used as benchmarks to determine the performance of other aspects of this workpackage. The emphasis will be on developing tools that can be readily applied to different detector designs and, so far as this is possible, different technolgies also. It is not intended that the analyses developed will necessarily compete with the "state-of-the-art" analyses, such as those presented in the LCWS series of meetings.

The physics case for the ILC is well established and therefore the emphasis within this task is on delivering complete, packaged physics analyses which will allow people other than their authors to measure and optimise key performance characteristics of a particular detector design. There is the need to be able to provide physics-based performance measures both for energy flow algorithm studies and for global detector design.

The work required can be broken down into the following tasks:

- Survey of existing analyses and benchmarks, for both energy flow algorithm development (aspects of detector to be tested, intrinsic resolutions, particle separations), and identification of a set of complete physics benchmark processes (global detector design).
- Implementation of a simple, robust version of a single analysis using generic tools (does not have to be "state-of-the-art").
- Development of additional physics benchmark analyses.
- Understanding of the interplay between hadronic modelling uncertainties and energy flow and their impact on physics.

8 Management plan

The CALICE collaboration has several management committees. The overall direction of the collaboration is determined at the Steering Board, where the UK Spokesperson (currently P.D.Dauncey) serves ex officio as the UK representative. There is also a Technical Board, for which D.R.Ward is Software Coordinator and P.D.Dauncey is Online Coordinator, and a Speakers' Bureau, chaired by D.R.Ward.

The proposed UK management structure is shown in figure 8. This is based on our experience of directing the UK effort over the last two years. Within the UK, the main direction is given by the UK Steering Board, which has been operating throughout the current grant period. This board consists of the group heads of the UK institutes. P.D.Dauncey, as UK Spokesperson, chairs this board and reports on its activities to the central CALICE Steering Board. This reporting path is for information only as the CALICE Collaboration has no direct financial input from the UK. The UK Steering Board meets as required, which has been approximately every four months on average. This would be expected to increase with the enlarged scope of the current proposal.

The workpackage leaders will report to the UK Steering Board. Each leader will have responsibility for their workpackage and hence will manage the activities of the groups within each workpackage through the relevant CALICE-UK group leaders. The workpackage leaders are responsible for the workpackage budget and schedule. The workpackage activities will be organised through frequent meetings, both face-to-face and phone. This has worked well for both the electronics [33] and simulation [34] effort over the last two years, where meetings have been held every two or three weeks.

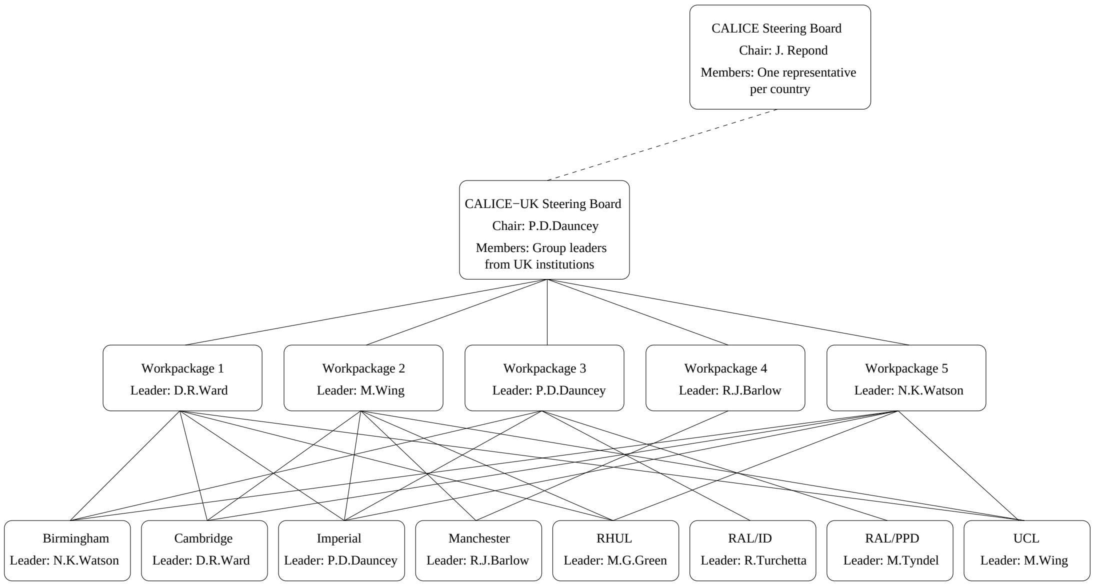

Figure 8: *CALICE-UK organisational structure.*

All decisions within each workpackage will be taken at the workpackage level by the workpackage leader, after discussion with the groups involved. Decisions which affect several workpackages (such as a reallocation of funds between the workpackages) will be taken at the UK Steering Board level.

9 Benefits to the wider community

9.1 Relevance to PPARC science strategy

The physics of the ILC directly addresses several of the fundamental questions listed as the priority for PPARC in the Science Committee Strategy Paper, namely "What are the basic properties of the fundamental particles and forces?" and "Is there a 'Theory of Everything' and if so what form does it take?". It may also help to elucidate several other questions listed in the document related to the origin of the Universe, its structure, and missing mass through the discovery or exclusion of new particles.

The paper also lists PPARC's strategic goals, amoung which are "Strengthen the UK's capability in accelerator science and R&D to position it to be a full partner in the next generation of global accelerators, and in particular, a Linear Collider and Neutrino Factory" as well as "Invest in blue-skies technology R&D, which will underpin longer-term facility development". This proposal also addresses both of these goals.

The ILC has been identified as the next large facility required by the HEP community. PPARC have recently heavily invested in accelerator R&D and a significant fraction of these funds have gone to ILC accelerator studies. Sums up to £300M have been mentioned as the UK long term contribution to an ILC and for this substantial level of investment, a large physics payback would be expected.

This proposal is a step towards the UK positioning itself in the ILC detector R&D area so as to influence the future design of the detector, take leading roles within the future collaboration and eventually producing the invaluable physics output which would come from such a detector.

9.2 Student benefits and training

The current CALICE work has involved one student, C.Fry (Imperial), whose thesis work is split between CALICE and ZEUS, with CALICE at a 40% level. Her work has been on electronics prototype tests and simulation and she will contribute to the DESY electron beam test and data analysis.

A larger project, such as that proposed here, would be expected to take at least one student per institute over the three year period of the proposal. Depending on which workpackage(s) the students get involved in, the work could involve cutting edge silicon technology, high performance object-oriented computing, FPGA firmware design or high-speed networking. Any of these would be extremely valuable following a Ph.D. degree, either inside or outside the field.

9.3 Industrial benefits

While many of the equipment items listed in the proposal will be purchased from industry, there is no explicit industrial partnership involved in this work. We view the status of these R&D items as being too preliminary for this to be attractive to companies at this stage.

However, assuming the work proposed here is successful, then there are clear areas where UK industry could benefit in the future. The most obvious would be if the MAPS sensors were accepted for an ILC detector ECAL. A huge area, around $3000\,\mathrm{m}^2$ of silicon, would be needed for the complete detector and this would all need to be industrially produced. The companies which had manufactured the prototypes (required to get to the stage of acceptance) would have a very clear advantage in the bids for the final contracts. If the UK has been leading the field in this area, then these companies would be in the UK. Another potential area is in the DAQ networking, where large amounts of fibre and switch equipment will be needed. In the same way, the links made with UK companies now will prove advantageous for contracts in the future.

10 Conclusions

The UK groups joined CALICE two years ago. Since then, they have built up a strong and influential presence both within the collaboration and also the ILC community as a whole. The UK has delivered the electronics, data acquisition and simulation work that it set out to do in the original proposal.

The current proposal builds on this success by aiming to position the UK to make a big impact in the ILC detector TDRs in several areas where the UK would be leading the effort and so would have significant influence. The timescale for this proposal is set by the expected date of 2009 for the TDRs and we believe this investment now will enable the UK groups to achieve this goal.

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[34] `http://www.hep.ucl.ac.uk/~sboogert/calice-simulation.html`.

Annex A: Workpackage Details

The background information and tasks for each workpackage are given in the main body of the text of the proposal. The following gives the details for each workpackage in terms of responsibilities, inputs, outputs, justification and full costs. The five new RA posts are indicated by RA-1 (Birmingham), RA-2 (Imperial), RA-3 (RHUL), RA-4 (UCL) and RA-5 (RAL/PPD).

The full costs are estimated using an engineering build-up method, where the project is broken down into its component parts, which are costed separately. Some level of detail of this break down is given in the tables below.

All personnel are already funded as part of the group rolling grants or the RAL SLA except for the extension of the existing Cambridge RA post, the five new RA posts, N.Pezzi, and the RAL/ID effort. Note, RAL/PPD RA-5 is funded as part of the RAL SLA for FY05/06 so it is only a new post for FY06/07 and FY07/08. N.Pezzi's effort needs to be purchased from his current project. D.R.Price will retire during the period of the proposal; it is assumed his replacement will continue his work and so he is listed for the whole period. The salaries are the exact total costs for each named person where applicable. For new RA posts, salaries assume appointments will be made at Point 6 for Universities or Band 5 for RAL. In all cases, salaries are assumed to be incremented each year at the usual rate. All costs (salary and others) are mainly tabulated in terms of costs in FY05/06, with indexation (at an assumed 2.75% as instructed, although we note this may be low for salaries) being added to the overall figure at the end of the table. There are no exceptional or indirect costs so these have not been included in any of the tables.

We have chosen to include travel and management costs within each workpackage rather than put them in separate workpackages for the overall proposal. In both cases, these costs are closely associated with particular workpackages and we feel this gives a clearer view of the true workpackage costs. We have also chosen to provide a GANTT/schedule chart for each workpackage separately rather for the whole proposal, for similar reasons.

Various miscellaneous consumables, such as paper, basic computing equipment, etc., will be provided through the institute rolling grants or SLAs.

Manchester is in the process of appointing two new members of academic staff. It is anticipated that at least one of these will have a significant commitment to CALICE, though the exact level of this effort is not yet known. It will be used within Workpackages 2 and 4.

The Manchester group contains people currently also involved in ATLAS UK. While the total Manchester effort listed here does not violate the ATLAS ringfence, some of these people are considered valuable to ATLAS and so the exact distribution of effort between them is provisional, subject to discussions with ATLAS UK.

P.D.Dauncey has a total of 40% FTE assigned to this proposal, spread over several workpackages. He has applied for a PPARC Senior Fellowship which would cover most of the period of this proposal. If successful, his total effort would be increased to 70% FTE, with the increases mainly in Workpackage 3 (increasing the amount of MAPS testing) and Workpackage 1 (more data analysis). However, the proposal as presented here does not assume this extra effort is available.

Annex A1: Workpackage 1

Responsible institutes

Birmingham, Cambridge, Imperial, RHUL and UCL are the responsible institutes, with D.R.Ward (Cambridge) being the workpackage manager.

Input

None from other workpackages. The physical calorimeters being constructed by the non-UK CALICE collaborators are needed to complete this work.

Output

Publication of results on the beam test data and simulation models, by the end of the proposal period.

Justification of costs

The largest staff cost is the extension of the Cambridge RA post (filled by G.Mavromanolakis) to the three year duration requested in the original proposal; this effort is still required. The original proposal also asked for a further RA post during the third year, i.e. the data-taking period of CALICE. This 1 FTE of effort is also still required, so three of the new RA posts will devote some fraction of their time to the existing CALICE program in the early stages. All this effort will bolster the UK's contribution and influence in the interpretation of these data. This is particularly needed as the two PPARC fellows current working in this area (C.G.Ainsley and D.Bowerman) will come to the end of their fellowships within the first FY.

O.Zorba and M.Warren will complete the firmware for the existing UK electronics over the next year. The Imperial RA-2 will work on the DAQ software to maintain it during the rest of the DESY beam test and also help upgrade it for the AHCAL and DHCAL tests. Some cost for shipping and maintenance of the UK hardware for the beam tests has been included, although it is hoped the latter will not be needed if the system works reliably.

G.Mavromanolakis, the three new RAs and F.Salvatore will take shifts and perform the analysis of these beam test data.

The major part of the travel costs is to take the data during the beam tests. Each week of shifts at FNAL is costed at £1k. The AHCAL beam test will start in November 2005 and data taking will then effectively merge into the DHCAL beam test in summer 2006. It is assumed on average one UK person will be at the beam test at all times, resulting in 20 staff weeks of visits in FY05/06 and 40 in FY06/07. It will be necessary to have frequent collaboration meetings over this period and it is foreseen that they will be held monthly, particularly towards the end of this period. Each meeting is assumed to have on average two UK attendees, each costing £500. Some level of UK collaboration travel and conference travel for presenting the results outside the CALICE collaboration are also requested.

Workpackage 1	People/Items	Cost (£k)
Staff	New RA-1	10
	G.Mavromanolakis	65
	O.Zorba	5
	New RA-2	46
	F.Salvatore	10
	M.Warren	9
	New RA-4	29
Equipment	None	0
Consumables	Shipping	1
	VME Electronics M&O	10
Travel	UK travel	9
	Collaboration meetings	28
	Conferences	12
	Beam tests	60
Total		293
Indexed total		298

Effort

The effort per FY in staff months proposed for staff paid from this proposal and for staff paid from other sources is shown in the table below.

Workpackage 1			FY05/06	FY06/07	FY07/08	Total
Name	Institute	Funding	(SM)	(SM)	(SM)	(SM)
Funded from this proposal						
New RA-1	Birmingham	Project	2	1	0	3
G.Mavromanolakis	Cambridge	Project	12	6	0	18
O.Zorba	Imperial	Rolling grant	1	0	0	1
New RA-2	Imperial	Project	6	5	1	12
F.Salvatore	RHUL	Rolling grant	1	1	0	2
M.Warren	UCL	Rolling grant	1	1	0	2
New RA-4	UCL	Project	4	4	0	8
Funded from other sources						
N.K.Watson	Birmingham	HEFCE	2	1	0	3
D.R.Ward	Cambridge	HEFCE	5	3	1	9
C.G.Ainsley	Cambridge	PPARC Fellow	6	0	0	6
P.D.Dauncey	Imperial	HEFCE	2	1	0	3
D.Bowerman	Imperial	PPARC Fellow	3	0	0	3
M.Wing	UCL	HEFCE	1	0	0	1

GANTT Chart

Workpackage 1	FY05/06				FY06/07				FY07/08			
	1	2	3	4	1	2	3	4	1	2	3	4
Task 1.1: Support for beam tests												
Complete board firmware	=	=	=									
Optimise DAQ software	=	=	=	=	=							
Upgrade DAQ for HCALs					=	=	=	=				
Task 1.2: Analysis of DESY electron test beam data												
Beam simulation	=											
Tune detector simulation	=											
Generate MC samples	=	=										
Data/MC comparisons	=	=	=									
Publish results			=	=								
Task 1.3: Analysis of FNAL test beam data												
Maintain hadron codes	=	=	=	=	=	=	=	=	=	=		
Understand beam line		=	=									
Generate MC samples		=	=	=								
Compare data/MC		=	=	=	=	=						
Repeat for DHCAL						=	=	=	=			
Publish results									=	=		

Milestones

The milestones associated with this workpackage are:
Completion of DESY ECAL-only beam test (month 4).
Completion of FNAL ECAL and AHCAL test beam (month 15).
Completion of FNAL ECAL and DHCAL test beam (month 24).

Deliverables

The main deliverables are:
Operating data acquisition system for all calorimeters.
Publication of beam test results from all three data-taking periods.

Annex A2: Workpackage 2

Responsible institutes

Cambridge, Imperial, Manchester, RHUL and UCL are the responsible institutes, with M.Wing (UCL) being the workpackage manager.

Input

Some ongoing input from the simulation studies of Workpackage 5.

Output

A report on the possible architectures for an ECAL DAQ system. Several pre-prototypes of parts of the system. Experience of operating the critical components of such a system.

Justification of costs

The VFE test PCB for Task 2.1 will be designed by D.R.Price at Imperial and laid out by HEFCE-funded technicians at Imperial. It will be manufactured and assembled commercially. Clock, control and readout will be provided an FPGA development board read out by a PC. The firmware for the development board and the VFE PCB will be produced by O.Zorba and the Imperial RA-2. The development board will be identical to the one used for MAPS tests (Workpackage 3) so there should be some reuse of firmware for these two systems.

For the 1.5 m slab studies of Task 2.2, the resources required would initially be multi-layer 500 mm PCBs for initial tests and investigations. Cambridge (M.J.Goodrick, R.Shaw and C.Barham, in addition to B.Fromant who is HEFCE funded) will use their expertise to focus on issues such as bandwidth, data integrity and crosstalk; this will involve the design, construction and testing of PCBs as well as CAD modelling. There will also be several iterations on final, full-length 1500 mm PCBs. All PCBs will be designed and assembled by these personnel at Cambridge, with the PCB fabrication being done commercially. The firmware and testing will be done by the same people. Hardware for bit error rate testing will used the ATLAS design. CAD tools will be required, particularly in the initial phase.

Within Task 2.3, two on- to off-detector network test systems will be considered, one led by Manchester (R.Hughes-Jones and S.Kolya) and RHUL RA-3, with input from UCL (N.Pezzi, M.Warren and RA-4) and one led by UCL with input from Manchester. One system would include a 10 Gbit ethernet card with four ports, four optical data transceivers and the six 1 Gbit ethernet cards. This work is to be led by Manchester and RHUL. UCL will provide the FPGA to fibre communication interface, related to the clock and control package. A test system using an optical switch connected via optical fibres to the PCI cards housed in PCs would be setup at UCL. We assume scalability of the optical switch, so we would use a relatively small 16×16 lane switch. As part of the bid, N.Pezzi brings the necessary networking expertise to the project. This work will led by UCL. To consolidate costs, equipment would be shared between Manchester, RHUL and UCL.

In Task 2.4, the FPGA failsafe test system will require a PC with a network card and a development board with cables and connectors. This work is closely connected to the clock and control work and will be carried out at UCL (M. Postranecky, M.Warren, RA-4). The C&C test system will use much of the same equipment. Additional network cards, a fanout board and a switch will be required.

The final system for the PCI option of off-detector receivers for Task 2.5 would consist of four PCs each with a PCI card in them and the possibility to move PCI cards between PCs so as to maximise the data rate to one computer. To act as the VFE or FE sending the data, four further PCI cards would be required housed in two PCs. Two rounds of prototyping, each of two cards, would be done before initially building the final eight. The design and manufacture of the PCI card would be undertaken by Cambridge (M.J.Goodrick, R.Shaw, C.Barham and B.Fromant), UCL (M.Postranecky, M.Warren and RA-4) and RHUL (G.Boorman, B.J.Green and RA-3) in conjunction with Manchester and UCL's work on networking. The PCI cards and PCs would be shared by Manchester and UCL for the network system tests.

As this is an almost exclusively UK project, most travel will be within the UK between the respective institutes. However, some overseas travel will be required to liaise with the VFE ASIC designers in Paris to ascertain how this affects the immediate readout to be provided by Imperial and studies of a full sized 1.5 m PCB to be researched by Cambridge and Manchester.

The UCL RA-4 will be travelling to DESY and FNAL for beam tests over much of the first two years of this proposal (Workpackage 1) as well as within the UK for this workpackage and so will require a laptop to work efficiently.

Workpackage 2	People/Items	Cost (£k)
Staff	M.J.Goodrick	41
	R.Shaw	18
	C.Barham	26
	New RA-2	20
	D.R.Price	29
	O.Zorba	11
	R.Hughes-Jones	31
	S.Kolya	18
	G.Boorman	13
	B.J.Green	35
	New RA-3	44
	New RA-4	77
	N.Pezzi	24
	M.Postranecky	75
	M.Warren	62
Equipment	Task 2.1: PCB manufacture	6
	Task 2.2: Active GHz probes	4
	Task 2.2: GHz bit error rate tester	4
	Task 2.2: Short, 0.5m, PCB manufacture	6
	Task 2.2: Long, 1.5m, prototype manufacture	6
	Task 2.2: Long, 1.5m, production manufacture	12
	Task 2.3: 4-port, 10Gbit ethernet switch	11
	Task 2.3: Four optical data transceivers	6
	Task 2.3: Six 1Gbit ethernet cards	11
	Task 2.3: 16-port optical switch	18
	Task 2.3: Switch options	6
	Task 2.5: Prototype PCI cards	10
	Task 2.5: Production PCI cards	12
	Task 2.5: Six high performance PCs	7
Consumables	Task 2.1: DAQ PC	2
	Task 2.1: DAQ FPGA development board	1
	Task 2.2: CAD licence	2
	Task 2.4: GHz PCB FPGA development board	1
	Task 2.4: Development board 10Gbit module	2
	Task 2.4: PC with specialised networking	2
	Task 2.4: Miscellaneous cables, connectors, etc.	1
	Task 2.4: Second development board/card	1
	Task 2.4: Switch	1
	Task 2.4: 10Gbit ethernet PCI card	2
	Task 2.4: Fanout PCB	2
	UCL RA-4 laptop	2
Travel	UK travel	18
	VFE meetings in Paris	8
	Conferences	7
Total		695
Indexed total		720

Effort

The effort per FY in staff months proposed for staff paid from this proposal and for staff paid from other sources is shown in the table below.

Workpackage 2			FY05/06	FY06/07	FY07/08	Total
Name	Institute	Funding	(SM)	(SM)	(SM)	(SM)
Funded from this proposal						
M.J.Goodrick	Cambridge	Rolling grant	2	2	3	7
R.Shaw	Cambridge	Rolling grant	1	2	2	5
C.Barham	Cambridge	Rolling grant	1	3	4	8
New RA-2	Imperial	Project	0	1	4	5
D.R.Price	Imperial	Rolling grant	0	1	3	4
O.Zorba	Imperial	Rolling grant	0	0	2	2
R.Hughes-Jones	Manchester	Rolling grant	1	2	2	5
S.Kolya	Manchester	Rolling grant	1	1	1	3
G.Boorman	RHUL	Rolling grant	0	1	2	3
B.J.Green	RHUL	Rolling grant	2	2	2	6
New RA-3	RHUL	Project	0	6	6	12
New RA-4	UCL	Project	7	7	7	21
N.Pezzi	UCL	Project	1	1	2	4
M.Postranecky	UCL	Rolling grant	4	4	6	14
M.Warren	UCL	Rolling grant	2	5	6	13
Funded from other sources						
D.R.Ward	Cambridge	HEFCE	1	1	1	3
B.Fromant	Cambridge	HEFCE	0	1	4	5
P.D.Dauncey	Imperial	HEFCE	0	1	1	2
Electronics technicians	Imperial	HEFCE	0	0	7	7
R.J.Barlow	Manchester	HEFCE	1	1	1	3
M.G.Green	RHUL	HEFCE	2	2	2	6
M.Wing	UCL	HEFCE	2	2	2	6
M.Lancaster	UCL	HEFCE	2	2	2	6

GANTT Chart

Workpackage 2	FY05/06				FY06/07				FY07/08			
	1	2	3	4	1	2	3	4	1	2	3	4
Task 2.1: Readout of prototype VFE ASICs												
Tests with LAL/Orsay PCBs							=	=				
Design and layout of PCB								=	=	=		
Write test PCB firmware									=	=		
Readout ASICs in bulk										=	=	=
Task 2.2: Study of data paths over 1.5 m slab												
Preliminary design studies and preparation	=	=	=	=								
Short board fabrication and tests				=	=	=	=	=				
Long board fabrication and tests								=	=	=	=	=
Task 2.3: Connection from on-detector to the off-detector receiver												
Investigation of technologies and test criteria	=	=	=	=								
Set up and operate 10 Gbit test-bench				=	=	=						
Examine traffic flow performance						=	=	=	=			
Link Test for optical network							=	=	=			
Explore switching performance									=	=	=	=
Task 2.4: Transport of configuration, clock and control data												
Radiation tolerance and SEU rates	=	=	=	=								
Test system for signals on high-speed network		=	=	=	=	=	=					
Evaluate the clocking requirements					=	=	=					
Build network for testing trigger timing spills							=	=	=			
Extend to 10000 link test system									=	=	=	=
Task 2.5: Prototype off-detector receiver												
Investigation of latest PCI technology	=	=										
Design and build PCI card		=	=	=								
Test PCI card				=	=							
Fabricate PCI cards and setup test system					=	=	=					
Efficiency and volume of data transfer							=	=	=	=	=	=

Milestones

The milestones associated with this workpackage are:
Task 2.1:
Complete build and programming of board to readout ASIC chips (month 28).
Task 2.2:
Complete build of short, 0.5 m, board for data transfer tests (month 15).
Complete build of long, 1.5 m, board for data transfer tests (month 27).
Task 2.3:
Setup of 10 Gbit networking test bench (month 18).
Setup optical networking test bench (month 27).
Task 2.4:
Complete test system for reprogramming FPGAs (month 15).
Complete test bench for method of synchronising clock and control data (month 27).
Task 2.5:
Build and test prototype PCI card (month 15).

Fabrication of final PCI cards and setup of test system (month 21).

Deliverables

The main deliverables are:
Provide readout board for testing prototype ASIC chips.
Produce a functional pre-prototype of a PCI off-detector receiver card.
Write one or more linear collider notes on results of data acquisition workpackage.
Position UK groups to be in clear lead in the area of DAQ so as to later write chapter on data acquisition for calorimeter for the TDR.

Annex A3: Workpackage 3

Responsible institutes

Birmingham, Imperial, RAL/ID and RAL/PPD are the responsible institutes, with P.D.Dauncey (Imperial) being the workpackage manager and R.Turchetta (RAL/ID) the workpackage lead engineer.

Input

Some ongoing input from the simulation studies of Workpackage 5.

Output

A report on the validity of MAPS concept for an ILC ECAL sensor, by the end of the proposal period. If valid, then also a pre-prototype design of such a sensor.

Justification of costs

R.Turchetta and M.Tyndel will lead the RAL/ID and RAL/PPD groups, respectively. Both are members of the existing MAPS collaboration funded from PPRP seedcorn funds, as is E.G.Villani. R.Turchetta, and E.G.Villani (and J.Crooks currently) are also members of the MI^3 collaboration developing MAPS for other applications, funded through Basic Technology. There is some overlap between these projects and there will be mutual benefits from using the same personnel.

An initial feasibility study to narrow down the possible designs will be done. This will include R.Turchetta, J.Crooks, M.Tyndel and E.G.Villani.

The sensor design itself will be done within the RAL/ID group. The design will require a full-time microelectronics design engineer; this will be J.Crooks and he will be overseen by R.Turchetta. Sensor simulation to guide the design will be done by E.G.Villani in RAL/PPD, overseen by M.Tyndel. The Birmingham RA-1 and Imperial RA-2 will perform physics-level simulations to model the effects of particular design choices. Fabrication will be done commercially.

Initial basic tests will be done within the RAL/ID group by these personnel. This will use existing equipment in their laboratory.

The design of the simple PCBs to hold single sensors during bench tests will be done by D.R.Price at Imperial. The PCBs will be laid out by HEFCE-funded technicians at Imperial and fabricated commercially. Mounting of the sensors on the PCBs, involving gluing and wire-bonding, will be done by the technicians at Imperial and Birmingham. Mechanical holders for the PCBs, to align several sensors to form a multi-layer cosmic telescope and allow them to be inserted into a 5T magnetic field at DESY, will be built by I.Clark at Imperial. O.Zorba will provide firmware to use the FPGA development board as a clock, control and DAQ driver of the PCB-mounted sensors.

The detailed bench tests will take place at Imperial, Birmingham and RAL/PPD, as outlined below, and this work will be mainly done by the three new RAs, one at each site.

The PCB to hold the MAPS during a beam test will be designed by R.J.Staley at Birmingham. The layout and manufacture of this PCB will be done commercially. Firmware for this PCB will be provided by R.J.Staley, the Birmingham RA-1 and the RAL/PPD RA-5. Firmware to adapt the ECAL readout boards for MAPS use will be done by O.Zorba, who designed the existing firmware.

The biggest items under equipment costs are the two sensor fabrication rounds and the price given is based on a similar MAPS design currently being sent to XFAB by RAL/ID.

There will need to be three teststands for the bench tests, one at each of Imperial, Birmingham and RAL, so as to get all the foreseen tests done in the time available. One will be mainly for cosmic tests, where a dedicated system with multiple sensor readout is required in order to build up sufficient statistics over a long period. The other two will concentrate on shorter term studies. One of these two will also be transported to DESY for high magnetic field tests. Each of these teststands will contain a DAQ PC, one or more FPGA development boards to interface to the sensor PCBs, and power supplies for the system. Some of this equipment may be purchased well in advance of the first fabrication round as there is a possibility of access to sensors from the MI^3 project in the first year. The Imperial group also request a digital oscilloscope as this is essential for such tests but all existing oscilloscopes at Imperial are tied to ongoing projects. The bench tests will require miscellaneous equipment, which is costed at £1k per teststand per year of operation. This includes cables, DVMs, a ^{90}Sr source (and the cost for its eventual disposal), light-tight boxes, the mechanical PCB holders, temperature measuring devices, CD data storage, etc. In addition, the cosmic test bench will require a HV power supply and some trigger logic; the PMTs are already available at the institutes.

The beam test PCB is a complex board due to the several thousand I/O signals foreseen from the $\sim$50 sensors which will be mounted on it. This is likely to be a 15-20 layer board containing around ten FPGAs and so has significant design, layout and manufacturing costs. The design and firmware can be done at Birmingham but there is no effort available for layout so this will be done commercially. It is estimated that 6 SM of effort will be needed for this layout. Fabrication will also be done commercially. Effort for the beam test and the analysis of the data will come from the three new RAs.

The Imperial RA-2 will be travelling to DESY and FNAL for beam tests over much of the first two years of this proposal (Workpackage 1), as well as travelling frequently between Imperial, Birmingham and RAL, and so will require a laptop to work efficiently.

As the workpackage is based within the UK, ongoing travel is costed around £5k per year. When results become available in the third year of the proposal, then travel to conferences to present them is needed. The beam test will be at DESY and will last for several months. One UK person will be required at DESY at all times, costed at £500 per week for ten weeks. Two DESY visits to test the sensors in a large aperture 5 T magnet are also required.

Workpackage 3	People/Items	Cost (£k)
Staff	R.J.Staley	23
	New RA-1	24
	Birmingham electronics technicians	9
	O.Zorba	26
	New RA-2	47
	D.R.Price	14
	I.Clark	14
	R.Turchetta	34
	J.Crooks	213
	E.G.Villani	78
	M.Tyndel	20
	New RA-5	133
Equipment	First fabrication round	76
	First round test PCBs	3
	Bench test DAQ PCs	5
	Bench test DAQ FPGA development boards	3
	Oscilloscope	6
	Second fabrication round	76
	Second round test PCBs	4
	Beam test PCB manufacture	20
Consumables	Imperial RA-2 laptop	2
	Bench test DAQ power supplies	2
	Miscellaneous items (see text)	6
	HV supply and logic for cosmic trigger	2
	Crate for cosmic trigger logic	3
	Beam test PCB layout	40
Travel	UK travel	15
	Conferences	7
	Beam test	5
	DESY high B field test	1
Total		911
Indexed total		944

Effort

The effort per FY in staff months proposed for staff paid from this proposal and for staff paid from other sources is shown in the table below.

Workpackage 3			FY05/06	FY06/07	FY07/08	Total
Name	Institute	Funding	(SM)	(SM)	(SM)	(SM)
Funded from this proposal						
R.J.Staley	Birmingham	Rolling grant	0	2	2	4
New RA-1	Birmingham	Project	1	2	4	7
Electronics technicians	Birmingham	Rolling grant	0	1	2	3
O.Zorba	Imperial	Rolling grant	0	2	3	5
New RA-2	Imperial	Project	1	5	6	12
D.R.Price	Imperial	Rolling grant	0	1	1	2
I.Clark	Imperial	Rolling grant	0	1	2	3
R.Turchetta	RAL/ID	Project	1	1	1	3
J.Crooks	RAL/ID	Project	12	12	12	36
E.G.Villani	RAL/PPD	RAL SLA	2	5	5	12
M.Tyndel	RAL/PPD	RAL SLA	1	1	1	3
New RA-5	RAL/PPD	SLA/Project	3	12	12	27
Funded from other sources						
N.K.Watson	Birmingham	HEFCE	2	2	2	6
J.A.Wilson	Birmingham	HEFCE	1	2	2	5
P.D.Dauncey	Imperial	HEFCE	2	2	4	8
Electronics technicians	Imperial	HEFCE	0	4	4	8

GANTT Chart

Workpackage 3	FY05/06				FY06/07				FY07/08			
	1	2	3	4	1	2	3	4	1	2	3	4
Task 3.1: Sensor production and testing												
Initial feasibility study of options	=											
First sensor design		=	=	=	=							
First sensor fabrication					=	=						
Basic functional tests						=	=					
Detailed bench tests							=	=	=	=		
Second sensor design							=	=	=			
Second sensor fabrication									=	=		
Basic functional tests										=	=	
Detailed bench tests										=	=	=
Beam test PCB design and fabrication								=	=	=	=	
Beam test												=

Milestones

The milestones associated with this workpackage are:
First fabrication round completed (month 18).
First fabrication bench testing completed (month 30).
Second fabrication round completed (month 30).
Beam test started (month 33).

Second fabrication bench testing completed (month 36).

Deliverables

The main deliverables are:
Evaluation of whether MAPS are a viable option for silicon-tungsten ILC ECAL.
If the concept is proved valid, then a working MAPS pre-prototype for the ECAL application.

Annex A4: Workpackage 4

Responsible institutes

Manchester is the responsible institute, with R.J.Barlow (Manchester) being the workpackage manager.

Input

None directly from other workpackages. However, the detailed design of the detector is driven by the simulation studies of Workpackage 5 and other groups across the whole collaboration.

Output

Knowledge that the detectors can be assembled and will operate stably over the lifetime of the experiment, and how to achieve this, as an input to the TDR.

Justification of costs

S.Snow, who has used the FlexPDE software for thermal flow studies in ATLAS, will do the thermal studies. M.Perry will perform measurements and literature searches on thermal outputs of the electronics components used in the readout. M.Perry and A.Elvin will carry out measurements using mockups of detector modules to validate the simulations of S.Snow.

R.J.Thompson will do a literature search on glue characteristics and conduct ageing tests using our existing programmable oven.

R.J.Thompson, A.Elvin and J.Freestone will work on the design and prototyping of the assembly robot system (with some assistance from S.Snow). This team was responsible for the ATLAS SCT assembly system, and will apply that knowledge (and some of the apparatus) to establishing a proof-of-principle pre-prototype for a production line system such as could eventually be used for the actual calorimeter.

For the thermal measurements, some new sensors, connection blocks, insulation and heat sources (to simulate readout chips) will be needed. The main cost will be tungsten/carbon fibre/silicon assemblies to reproduce various interface conditions (particular care is needed over carbon fibre orientations). We will work with the Ecole Polytechnique group and can use some of their assemblies, but estimate a cost of £4k for additional materials.

For cooling studies, we will need to buy a chiller, pumps and flowmeters, and construct many different cooling channels.

We will use an existing PC and Keithley 2000 DVM and multiplexor as a measurement system for the thermal studies.

As this work is within one institute, there is less need for UK travel than in some other workpackages. However it will be very important to work closely with the Ecole Polytechnique group to ensure we are totally familiar with all construction and fabrication issues, and specific allowance is made for that. We will also need to attend collaboration meetings regularly to present our preliminary findings for feedback, and to keep abreast of any likely design changes.

Workpackage 4	People/Items	Cost (£k)
Staff	R.J.Thompson	43
	S.Snow	18
	J.Freestone	26
	A.Elvin	19
	M.Perry	8
Equipment	Task 4.1: Carbon fibre and other materials	4
	Task 4.1: Chiller, pumps, flowmeters	8
	Task 4.3: 500 mm slide	5
	Task 4.3: Vacuum, pneumatics, construction components	8
Consumables	Task 4.1 FlexPDE 3D software licence	6
	Task 4.1: Sensors, connection blocks, heat sources	1
	Task 4.2 Conducting glue, syringes	3
	Task 4.3 Upgraded IMAQ/Labview	3
	Task 4.3: Camera and optics	2
Travel	UK travel	3
	Collaboration with French groups	6
Total		162
Indexed total		167

Effort

The effort per FY in staff months proposed for staff paid from this proposal and for staff paid from other sources is shown in the table below.

Workpackage 4			FY05/06 (SM)	FY06/07 (SM)	FY07/08 (SM)	Total (SM)
Name	Institute	Funding				
Funded from this proposal						
R.J.Thompson	Manchester	Rolling grant	1	2	4	7
S.Snow	Manchester	Rolling grant	1	1	1	3
J.Freestone	Manchester	Rolling grant	2	2	2	6
A.Elvin	Manchester	Rolling grant	2	2	2	6
M.Perry	Manchester	Rolling grant	1	1	1	3
Funded from other sources						
R.J.Barlow	Manchester	HEFCE	1	1	1	3

GANTT Chart

Workpackage 4	FY05/06				FY06/07				FY07/08			
	1	2	3	4	1	2	3	4	1	2	3	4
Task 4.1: Thermal studies												
Chip measurements	=	=										
Thermal simulation		=	=	=								
Thermal measurements				=	=	=	=	=				
Thermal design					=	=	=	=				
Cooling system							=	=	=	=	=	=
Task 4.2: Glue studies												
Review current knowledge	=	=										
Studies of ageing			=	=	=	=						
Task 4.3: Assembly studies												
Conceptual design preparations	=	=	=									
Wafer handling				=								
Coordinate autorecognition					=	=	=					
Wafer placement on PCBs								=	=	=	=	=

Milestones

The milestones associated with this workpackage are:
Task 4.1:
Measured thermal outputs of readout chips (month 6).
Thermal simulation of realistic detector configuration (month 12).
Task 4.2:
Literature search of existing glues (month 6).
Task 4.3:
Camera and software system for fiducial autorecognition for assembly procedure (month 7).
Conceptual design on assembly procedures (month 9).
First automated placement of detector wafer on PCB (month 9).

Deliverables

The main deliverables are:
A report on cooling system issues and possibilities, to be used as input for the design of the detector.
A report validating the glue and gluing techniques to be used.
A pre-prototype assembly system demonstrating the viability of a establishing a similar system for construction of the detector.

Annex A5: Workpackage 5

Responsible institutes

Birmingham, Cambridge, Imperial, RHUL and UCL are the responsible institutes, with N.K.Watson (Birmingham) being the workpackage manager.

Input

Partially dependent on simulation studies from Workpackage 1.

Output

Reports on simulation studies of resolutions, pattern recognition, critical issues, physics constraints, etc., for both the ECAL and HCAL, by the end of the proposal period.

Justification of costs

Development of a generic energy flow algorithm represents a significant amount of work and is estimated to require approx. three staff years of new effort. This is an important activity that would have large contributions from G.Mavromanolakis and Birmingham RA-1 as well as staff at Birmingham and Cambridge. Involving two RAs on this is important to stimulate new ideas and also to mitigate the risks of having essential knowledge with only single personnel.

Global detector design will require significant international and inter-regional contact and it is natural that the Cambridge group would lead this through M.A.Thomson and his position as a co-convener of the Global Detector Performance Group of the ECFA study. G.Mavromanolakis will contribute here also.

Work package support is important to work packages 2–4 and will receive contributions from all RAs, most significantly from Birmingham RA-1, Imperial RA-2 and UCL RA-4.

Physics studies will be driven by the RHUL group and is estimated to require half of the effort of RHUL RA-3, a substantial fraction of F.Salvatore and smaller contributions from other RAs, in particular UCL RA-4.

Given the nature of the work, laptops are requested for new RAs who will primarily contribute to this workpackage. This is essential to allow them to perform efficiently while attending workshops and collaborating with colleagues away from their home institutes.

Although extensive use will continue to be made of telephone and video conferencing, a significant amount of travel will be required in this workpackage. This is both to present results at international meetings and workshops/collaboration meetings and to maintain a significant presence and leadership at the international level. The cost is based on the following assumptions. Travel within the UK is estimated to cost £3k p.a., assuming six meetings per year, five people travelling and a cost of £100 per trip. International travel is estimated to cost £8k in each of the first two years and £12k in the final year. This assumes an average of four people travel to three workshops in each of the first two years, that trips within Europe cost £0.5k, outside Europe cost £1k, and that 2/3 of meetings are outside Europe. In the final year, as preparation of detector TDRs approaches, a 50% increase in travel is expected to be necessary.

Workpackage 5	People/Items	Cost (£k)
Staff	New RA-1	87
	G.Mavromanolakis	69
	New RA-2	27
	F.Salvatore	40
	New RA-3	44
	New RA-4	26
Equipment	None	0
Consumables	Birmingham RA-1 laptop	2
	RHUL RA-3 laptop	2
Travel	UK travel	9
	Conferences and workshops	35
Total		340
Indexed total		352

Effort

The effort per FY in staff months proposed for staff paid from this proposal and for staff paid from other sources is shown in the table below.

Workpackage 5			FY05/06	FY06/07	FY07/08	Total
Name	Institute	Funding	(SM)	(SM)	(SM)	(SM)
Funded from this proposal						
New RA-1	Birmingham	Project	9	9	8	26
G.Mavromanolakis	Cambridge	Project	0	6	12	18
New RA-2	Imperial	Project	5	1	1	7
F.Salvatore	RHUL	Rolling grant	1	1	6	8
New RA-3	RHUL	Project	0	6	6	12
New RA-4	UCL	Project	1	1	5	7
Funded from other sources						
N.K.Watson	Birmingham	HEFCE	2	3	4	9
C.M.Hawkes	Birmingham	HEFCE	1	1	1	3
D.R.Ward	Cambridge	HEFCE	0	2	4	6
M.A.Thompson	Cambridge	HEFCE	2	2	2	6
M.G.Green	RHUL	HEFCE	1	2	2	5
M.Wing	UCL	HEFCE	0	1	1	2

GANTT Chart

Workpackage 5	FY05/06				FY06/07				FY07/08			
	1	2	3	4	1	2	3	4	1	2	3	4
Task 5.1: Energy Flow Algorithms												
Understand resolution drivers	=	=	=									
Algorithm brainstorming	=	=	=	=								
Tool definitions		=	=									
Comparison of existing codes			=	=								
Algorithm implementation				=	=	=						
Physics benchmark results						=	=					
Algorithm development							=	=	=	=	=	=
Task 5.2: Global detector design												
Physics benchmark, 1 concept			=	=	=							
Other detector concepts				=	=							
Further physics benchmarks					=	=	=	=				
Detector parameter variation							=	=	=	=		
Optimisation for each concept				=	=	=	=	=	=	=	=	=
Task 5.3: Workpackage support												
DAQ local clustering				=	=	=						
Mechanical imperfections			=				=		=			
MAPS into `Mokka`	=	=	=									
MAPS sensor variation studies		=	=	=	=	=	=					
MAPS test beam										=	=	=
Task 5.4: Physics studies												
Survey existing analyses/benchmarks	=											
Implement generic analysis		=	=	=								
Additional benchmarks				=	=	=	=	=	=			
Hadronic modelling sensitivity				=	=	=	=	=	=	=	=	=

Milestones

The milestones associated with this workpackage are:
Task 5.1:
Comparison of existing energy flow algorithms (month 9).
Physics benchmark results (month 18).
Task 5.2:
First physics benchmark of detector concept (month 15).
Task 5.3:
MAPS implemented in Mokka (month 6).
Simulations for MAPS test beam (month 30).
Task 5.4:
Present plans for generic physics analysis at regional workshop (month 6).
Generic physics analysis implemented (month 12).

Deliverables

The main deliverables are:
Code for generic energy flow algorithm.

Significant contributions to detector CDRs and LoIs, positioning the UK to contribute strongly to the TDR.
Positions of responsibility in global LC software activity.
Report on simulations for Workpackages 2, 3 and 4.
Framework for physics analysis benchmarking of detector designs.

Annex B: Financial summary

Annex B1: Staff overview by institute

Staff funded from the proposal are listed below. Most numbers are before indexation, with this being added in explicitly at the bottom of each table. All costs are given in £k and all effort is given in staff months.

Birmingham					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
R.J.Staley	Engineer	Apr05	Mar08	Oct	0	0	12	2	12	2	23	4
New RA-1	RA	Apr05	Mar08	Oct	38	12	40	12	42	12	120	36
Elec. technicians	Technician	Apr05	Mar08	Aug	0	0	3	1	6	2	9	3
Total					38		54		59		152	
Indexed total					38		56		63		157	

Cambridge					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
G.Mavromanolakis	RA	Apr05	Mar08	Oct	42	12	45	12	46	12	133	36
M.J.Goodrick	Engineer	Apr05	Mar08	Oct	12	2	12	2	18	3	41	7
R.Shaw	Technician	Apr05	Mar08	Oct	4	1	7	2	7	2	18	5
C.Barham	Technician	Apr05	Mar08	Oct	3	1	10	3	13	4	26	8
Total					61		73		84		218	
Indexed total					61		75		89		225	

Imperial					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
O.Zorba	Engineer	Apr05	Mar08	Oct	5	1	10	2	26	5	41	8
New RA-2	RA	Apr05	Mar08	Oct	45	12	47	12	48	12	140	36
D.R.Price	Engineer	Apr05	Mar08	Oct	0	0	14	2	29	4	44	6
I.Clark	Technician	Apr05	Mar08	Oct	0	0	5	1	10	2	14	3
Total					50		76		113		240	
Indexed total					50		78		120		248	

Manchester					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
R.Hughes-Jones	Physicist	Apr05	Mar08	Oct	6	1	12	2	12	2	31	5
S.Kolya	Engineer	Apr05	Mar08	Oct	6	1	6	1	6	1	18	3
R.J.Thompson	Engineer	Apr05	Mar08	Oct	6	1	12	2	25	4	43	7
S.Snow	Physicist	Apr05	Mar08	Oct	6	1	6	1	6	1	18	3
J.Freestone	Engineer	Apr05	Mar08	Oct	8	2	9	2	9	2	26	6
A.Elvin	Technician	Apr05	Mar08	Oct	6	2	6	2	7	2	19	6
M.Perry	Technician	Apr05	Mar08	Oct	2	1	3	1	3	1	8	3
Total					40		54		68		162	
Indexed total					40		55		72		167	

RAL/ID					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
R.Turchetta	Engineer	Apr05	Mar08		11	1	11	1	12	1	34	3
J.Crooks	Engineer	Apr05	Mar08		68	12	71	12	74	12	213	36
Total					79		82		85		247	
Indexed total					79		84		90		254	

RAL/PPD					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
M.Tyndel	Physicist	Apr05	Mar08		7	1	7	1	7	1	20	3
E.G.Villani	Engineer	Apr05	Mar08		13	2	33	5	33	5	78	12
New RA-5	RA	Jan06	Mar08		15	3	59	12	59	12	133	27
Total					34		98		98		230	
Indexed total					34		101		103		238	

RHUL					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
G.Boorman	Engineer	Apr05	Mar08	Aug	0	0	4	1	9	2	13	3
B.J.Green	Engineer	Apr05	Mar08	Aug	12	2	12	2	12	2	35	6
New RA-3	RA	Apr06	Mar08	Aug	0	0	43	12	44	12	87	24
F.Salvatore	Physicist	Apr05	Mar08	Aug	10	2	10	2	30	6	50	10
Total					21		69		95		186	
Indexed total					21		71		101		193	

UCL					FY05/06		FY06/07		FY07/08		Total	
Staff Name	Grade	Start Date	End Date	Incr. Date	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)	Cost (£k)	Effort (SM)
M.Warren	Engineer	Apr05	Mar08	Oct	14	3	28	6	30	6	72	15
New RA-4	RA	Apr05	Mar08	Oct	43	12	44	12	46	12	133	36
N.Pezzi	Engineer	Apr05	Mar08	Oct	6	1	6	1	12	2	24	4
M.Postranecky	Engineer	Apr05	Mar08	Oct	21	4	21	4	34	6	75	14
Total					82		98		122		303	
Indexed total					82		101		129		312	

Annex B2: Overview of costs to PPARC

All costs are after indexation and are given in £k. The last line gives the “new money” totals, i.e. the costs not already within the rolling grants or RAL SLA. This therefore includes all equipment, consumables and travel as well as the staff costs for the project RAs, N.Pezzi and the RAL/ID personnel.

	FY05/06	FY06/07	FY07/08	Total
Staff Effort				
Birmingham	38	56	63	157
Cambridge	61	75	89	225
Imperial	50	78	120	248
Manchester	40	55	72	167
RAL/ID	79	84	90	254
RAL/PPD	34	101	103	238
RHUL	21	71	101	193
UCL	82	101	129	312
Equipment				
WP1	0	0	0	0
WP2	13	59	52	123
WP3	3	92	106	201
WP4	6	9	11	26
WP5	0	0	0	0
Travel				
WP1	34	55	22	112
WP2	9	10	15	34
WP3	5	7	17	29
WP4	3	3	3	9
WP5	13	13	19	45
Consumables				
WP1	6	5	0	11
WP2	4	9	6	20
WP3	3	9	45	58
WP4	5	6	4	15
WP5	2	2	0	4
Totals				
Staff Effort	407	622	767	1795
Equipment	22	160	168	350
Travel	64	89	76	229
Consumables	20	32	56	108
New Money Totals	359	657	704	1720
Overall Totals	513	903	1067	2482

Annex B3: PPARC supported contributions to workpackages by institute

All costs are after indexation and are given in £k.

	Birmingham	Cambridge	Imperial	Manchester	RAL/ID	RAL/PPD	RHUL	UCL	Equipment and Travel	Total
WP1	10	65	52	0	0	0	10	39	123	298
WP2	0	88	63	51	0	0	96	246	177	720
WP3	58	0	106	0	254	238	0	0	288	944
WP4	0	0	0	117	0	0	0	0	50	167
WP5	89	72	27	0	0	0	87	28	49	352
Total	157	225	248	167	254	238	193	312	687	2482

Annex C: Working allowance, risks and contingency

Annex C1: Working allowance

Most of the salary costs are for people in post and so are known accurately except for the level of future pay settlements. There is some possibility of a person leaving and having to be replaced, but this would be likely to be at worst cost neutral if they are not on the critical path (see contingency below). To allow for the pay settlement uncertainty, we allow a 2% working allowance on these salaries for each year.

The exceptions to this are the new RA posts. As these posts will require a substantial mix of skills, namely in hardware and analysis and, for some of them, a willingness to learn basic firmware design, then some leeway may be needed to attract and (in particular) retain candidates with the right background. Hence, the working allowance should allow these posts to be filled at up to two points higher than the standard Point 6. This is estimated to be £8k per RA post over the period of the proposal.

In terms of the individual workpackage uncertainties, the main contributions to the working allowance for Workpackage 1 are in travel and any M&O above the allocated amount which might be needed for electronics repairs. We have allowed 10% for each of these.

For Workpackage 2, the working allowance is set to 10% of the equipment and travel budgets, except for the non-commercial items, specifically the PCB designs, where 20% is allocated.

For Workpackage 3, the biggest cost is in the sensor fabrication, for which the price is known reasonably accurately. Hence, the main uncertainty for which the working allowance is required is in the design, layout and manufacturing of the complex beam test PCB. As the requirements for this board will not be known until the MAPS sensor is better developed, then a 20% uncertainty is given for this item. We allow 10% for the remaining equipment and travel.

For Workpackages 4 and 5, which have low non-staff costs, a 10% uncertainty on all non-staff costs is allocated.

Annex C2: Contingency

Staff costs are again a significant factor in the contingency. Were someone to leave mid-way through the project, it may be necessary to attract a replacement at short notice with a correspondingly higher cost. Also, if someone in a time-critical area were to fall ill, it may be necessary to increasing other people's effort to keep to schedule. In both cases, a contingency of around six months salary would be needed for any such personnel.

The main uncertainties for Workpackage 1 are external to the UK and would result in extended beam test periods. The contingency here is the cost of extending the beam test for another six months.

For Workpackage 2, the main contingency item is £20k for a failure or accident with a large commercial component, e.g. the network switch.

For Workpackage 3, the biggest risk, that of a failure of a sensor fabrication round, would require a quick turnaround to produce another sensor fabrication within the period of the proposal. Without this quick redesign, it might be that the concept is not verified in time to contribute to the TDR. The contingency is therefore the cost of this refabrication.

For Workpackages 4 and 5, all items are not dependent on groups external to the UK, so no contingency beyond staff is deemed necessary.

Annex C3: Risk analysis

The risks associated with the workpackages, their effects and steps which will be taken to mitigate them are outlined in the table below. Note, if the detector TDR itself is delayed beyond 2009, then many of the items related to schedule could be extended into another funding round.

WP	Risk	Effect	Risk Score			Mitigation
			L	I	L×I	
WP1	Failure of AHCAL and/or DHCAL.	Loss of data for simulation comparisons.	2	2	4	Develop ECAL-only studies and extend ECAL-only beam test if necessary. Work closely with both HCALs to optimising probability of at least one being ready on schedule.
	Extended beam test period required due to problems with calorimeters, beams or DAQ.	Higher travel costs.	2	1	2	Thorough testing of equipment before moving to FNAL. Close contact with FNAL beam delivery organisation. Formal MoU with FNAL signed before starting tests.
WP2	Failure of VFE ASIC production so no chips available for PCB test within period of proposal.	Delay resulting in non-verification of VFE ASIC by the time of the TDR.	1	2	2	Close collaboration with French groups designing ASIC so aware of schedule changes. Designs will be reviewed extensively before submission.
	Not able to find manufacturer for 1.5 m board.	Study cannot be completed in time for TDR.	2	2	4	Reduce scope by using a shorter board with looped tracking.
	Delays in sourcing commercial optical components.	Delays in schedule.	1	2	2	Work with available (but non-optimised) hardware, e.g. LHC spares.
WP3	Failure of design within a fabrication round.	Three to four month delay in schedule, resulting in reduced time for bench testing.	2	2	4	Review designs extensively before submission. Prepare basic tests to identify major problems immediately.
All	Delays/problems in RA appointments.	Corresponding delay in schedule or less skilled people appointed, reducing UK impact.	2	1	2	Advertise promptly, use contacts to encourage strong candidates.
	Loss of staff with required skills	Loss of expertise mid-way through project, half year delay to particular activity.	3	2	6	Ensure personnel work closely with other UK colleagues, avoid only single person knowing about any given activity, be aware of upcoming job opportunities for RAs.
	Illness of staff in critical positions	Reallocation of effort to other existing staff, causing delay to activity.	2	2	4	As above.

Annex C4: Summary of Additional Costs

The working allowance and contingency that are estimated to be required for each workpackage are detailed in the table below.

WP	Working Allowance (£k)	Contingency (£k)
Staff	109	30
WP1	12	26
WP2	22	20
WP3	24	76
WP4	5	0
WP5	4	0
Total	176	152

Annex D: Public Outreach

One of the biggest questions in our understanding of the smallest particles of Nature is why they have mass. According to current theory, the existence of fundamental particles with a mass which is not zero requires a special new particle to be introduced. This is the famous Higgs boson which has never been observed experimentally. As the Higgs is so basic to our understanding of the origin of mass, it is generally accepted that we cannot claim to understand mass until we have found the Higgs boson and have checked that it has the properties we expect.

The International Linear Collider is a huge undertaking involving hundreds, if not thousands, of physicists and engineers worldwide. It will use a novel technique of pointing two long, 30km accelerators straight at each other to collide beams of electrons and their antiparticles, positrons, at higher energies than ever achieved previously in this reaction. At these energies, the electrons and positrons will be able to make Higgs bosons as well as many other particles. One of the main goals of this experiment is to measure the properties of the Higgs boson with high accuracy to really see if its properties correspond with the current theories. It might also be that completely new particles, never before observed, may be created. These in turn would allow us to extend our understanding of Nature into unexpected directions.

The research being done as part of the international CALICE collaboration concerns the detector which will observe these Higgs particles. To give the detailed and accurate results needed, the detector has to have unprecedented precision in measuring the energy of the decay products of the Higgs. CALICE is studying ways of building detectors with the required precision.

Press enquiries should be addressed to:

Dr Paul Dauncey
Physics Department
Imperial College London
Prince Consort Road
London, SW7 2AZ

More information on the International Linear Collider, CALICE and the UK groups involved can be found at:

`http://www.interactions.org/linearcollider/`
`http://polywww.in2p3.fr/flc/calice.html`
`http://www.hep.ph.imperial.ac.uk/calice/`

Annex E: Talks and Proceedings

Talks given within the last two years by UK members of CALICE at conferences and workshops outside of CALICE collaboration meetings are listed below. These and other talks are collected at [32].

- P.D.Dauncey, "First Ideas for CALICE Beam Test DAQ," ECFA/DESY03 Workshop, Amsterdam, April 2003.
- D.R.Ward, "Geant3/Geant4 Comparisons – Status," ECFA/DESY03 Workshop, Amsterdam, April 2003.
- M.A.Thomson, "Update on the Tesla Detector," ECFA/DESY03 Workshop, Amsterdam, April 2003.
- S.T.Boogert, "Top Mass Measurements and Luminosity Spectra," ECFA Workshop, Montpellier, November 2003.
- N.K.Watson, "FLUKA and GEANT4," ECFA Workshop, Montpellier, November 2003.
- G.Mavromanolakis, "GEANT3 and GEANT4: Comparison of Tracking Cutoffs," ECFA Workshop, Montpellier, November 2003.
- C.G.Ainsley, "Cluster Finding in CALICE Calorimeters," International Conference on Linear Colliders LCWS04, Paris, April 2004 and proceedings thereof.
- P.D.Dauncey, "CALICE ECAL Readout Status," International Conference on Linear Colliders LCWS04, Paris, April 2004 and proceedings thereof.
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