# KAI-1010 Series

# 1024(H) x 1024(V) Pixel

# Megapixel Interline CCD Image Sensor

# Performance Specification

**Eastman Kodak Company**
**Microelectronics Technology Division**
**Rochester, New York 14650-2010**

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# Table of Contents

1.1 Features ..... 5
1.2 Description ..... 6
1.3 Architecture ..... 6
1.4 Image Acquisition ..... 6
1.5 Charge Transport ..... 7
1.6 Output Structure ..... 8
1.7 Electronic Shutter ..... 9
1.8 Color Filter Array (optional, for KAI-1010CM only) ..... 9
2.1 Packaging Configuration ..... 10
2.2 Pin Description ..... 11
2.3 Absolute Maximum Range ..... 13
2.4 DC Operating Conditions ..... 14
2.5 AC Clock Level Conditions ..... 15
2.6 AC Timing Requirements for 20 MHz Operation ..... 16
Frame Timing - Single Register Readout ..... 17
Line Timing - Single Register Readout ..... 18
Pixel Timing - Single Register Readout ..... 19
Electronic Shutter Timing - Single Register Readout ..... 20
Frame Timing - Dual Register Readout ..... 21
Line Timing - Dual Register Readout ..... 22
Pixel Timing - Dual Register Readout ..... 23
3.2 Image Specifications ..... 24
Electro-Optical for KAI-1010CM ..... 24
Electro-Optical for KAI-1010M ..... 26
CCD ..... 29
Output Amplifier @ $V_{DD}$ = 15V, $V_{SS}$ = 0.0V ..... 29
General ..... 30
3.3 Defect Classification ..... 32
4.1 Climatic Requirements ..... 33
4.2 Quality Assurance and Reliability ..... 33
4.3 Ordering Information ..... 34

## Figures

Figure 1 Functional Block Diagram ..... 5
Figure 2 KAI-1010CM ..... 6
Figure 3 True 2 Phase CCD Cross Section ..... 7
Figure 4 Output Structure ..... 8
Figure 5 CFA Pattern ..... 9
Figure 6 Device Drawing #6 Die Placement ..... 10
Figure 7 Pinout Diagram Top View ..... 12
Figure 8 Recommended Output Structure Load Diagram ..... 14
Figure 9 Frame Timing - Single Register Readout ..... 17
Figure 10 Line Timing - Single Register Output ..... 18
Figure 11 Pixel Timing Diagram - Single Register Readout ..... 19
Figure 12 Electronic Shutter Timing Diagram - Single Register Readout ..... 20
Figure 13 Frame Timing - Dual Register Readout ..... 21
Figure 14 Line Timing - Dual Register Output ..... 22
Figure 15 Pixel Timing Diagram - Dual Register Readout ..... 23
Figure 16 Nominal KAI 1010CM Spectral Response ..... 25
Figure 17 Nominal KAI-1010M Spectral Response ..... 26
Figure 18 Angular Dependence of Quantum Efficiency ..... 27
Figure 19 Frame Rate versus Horizontal Clock Frequency ..... 28
Figure 20 Typical KAI-1010Series Photoresponse ..... 30
Figure 21 Example of Vsat versus Vsub ..... 31

## Tables

Table 1 Package Pin Assignments ..... 11
Table 2 Absolute Maximum Ranges ..... 13
Table 3 DC Operating Conditions ..... 14
Table 4 AC Clock Level Conditions ..... 15
Table 5 AC Timing Requirements for 20 MHz Operation ..... 16
Table 6 Electro-Optical Image Specifications KAI-1010CM ..... 24
Table 7 Electro-Optical Image Specifications KAI-1010M ..... 26
Table 8 CCD Image Specifications ..... 29
Table 9 Output Amplifier Image Specifications ..... 29
Table 10 General Image Specifications ..... 30
Table 11 Climatic Requirements ..... 33
Table 12 Part Numbers - Monochrome, Microlens, Sealed Glass ..... 35
Table 13 Part Numbers - Monochrome, Microlens, Taped Glass ..... 35
Table 14 Part Numbers - Monochrome, Taped Glass ..... 35
Table 15 Part Numbers - Color, Microlens, Sealed Glass ..... 36
Table 16 Part Numbers - Color, Microlens, Taped Glass ..... 36

## Appendix

Appendix1 Part Number Availability ..... 35

## 1.1 Features

- **Front Illuminated Interline Architecture**
- **1008 (H) x 1018 (V) Photosensitive Pixels**
- **9.0µm(H) x 9.0µm(V) Pixel Size**
- **9.1 mm(H) x 9.2 mm(V) Photosensitive Area**
- **Progressive Scan (Noninterlaced)**
- **Electronic Shutter**
- **Integral RGB Color Filter Array (optional)**
- **Advanced 2 Phase Buried Channel CCD Processing**
- **On-Chip Dark Reference Pixels**
- **Low Dark Current**
- **Patented High Sensitivity Output Structure**
- **Dual Output Shift Registers**
- **Antiblooming Protection**
- **Negligible Lag**
- **Low Smear (0.01% with microlens)**

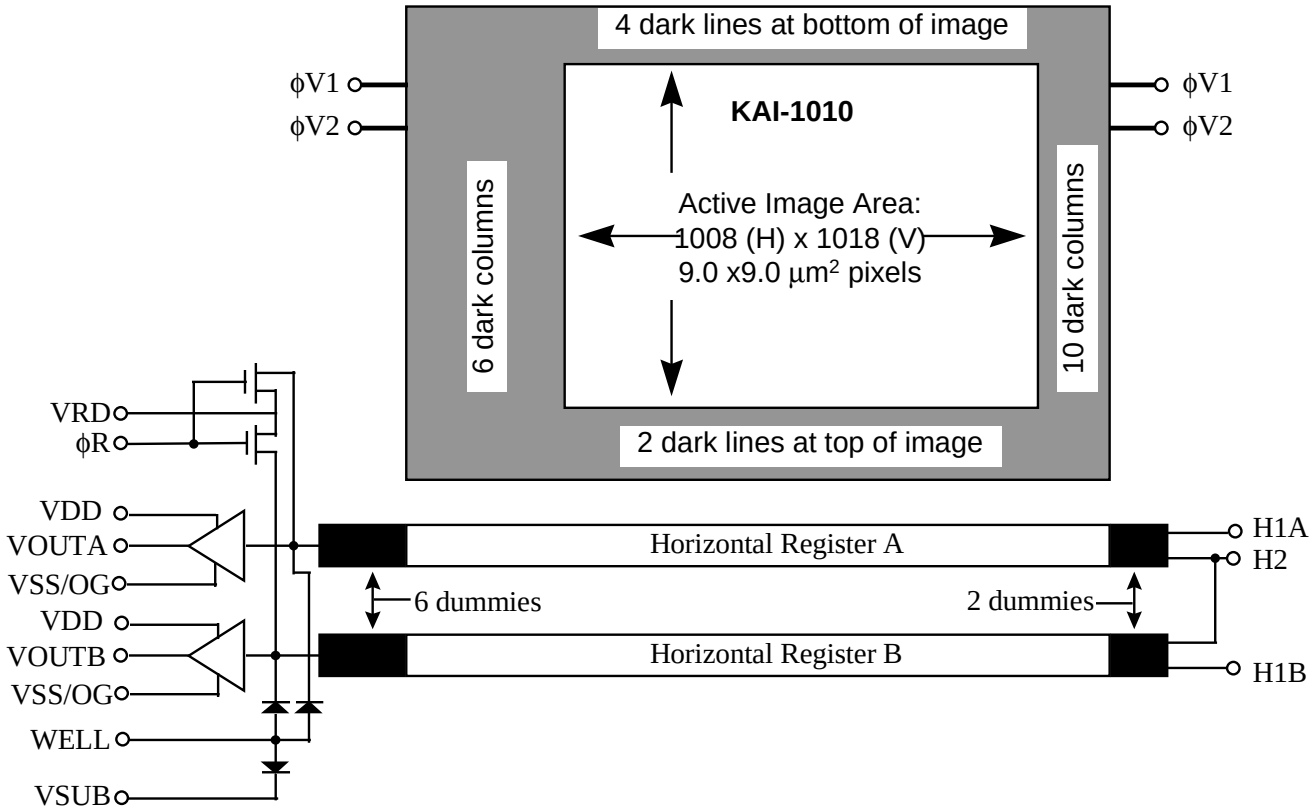



Figure 1 Functional Block Diagram

## 1.2 Description

The KAI-1010 series is a high resolution charge coupled device (CCD) image sensor whose noninterlaced architecture makes it ideally suited for video, electronic still and motion/still camera applications. The device is built using an advanced true two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodetector elements eliminate image lag and reduce image smear while providing antiblooming protection and electronic-exposure control. The total chip size is 10.15 (H) mm x 10.00 (V) mm. The KAI-1010 comes in monochrome and color versions, both with microlens for sensitivity improvement.

| Device | Color | Microlens |
|---|---|---|
| KAI-1010M | No | Yes |
| KAI-1010CM | Yes | Yes |

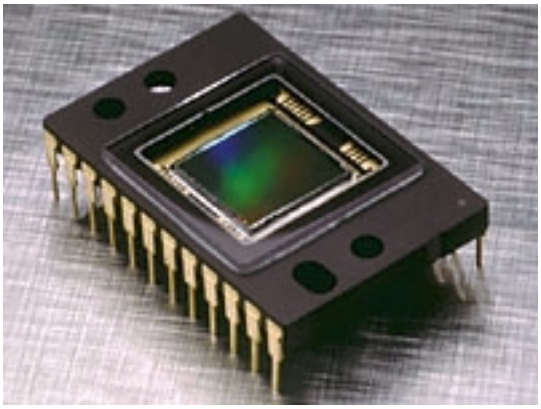


Figure 2 KAI-1010CM

## 1.3 Architecture

The KAI-1010 consists of 1024 x 1024 photodiodes, 1024 vertical (parallel) CCD shift registers (VCCDs), and dual 1032 pixel horizontal (serial) CCD shift registers (HCCDs) with independent output structures. The device can be operated in either single or dual line mode. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The active pixels are arranged in a 1008 (H) x 1018 (V) array with an additional 16 columns and 6 rows of light-shielded dark reference pixels.

## 1.4 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

## 1.5 Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (øV1). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, øH2, these charge packets are dumped over the output gate (OG, Figure 4) onto the floating diffusion (FDA and FDB, Figure 4).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the HCCDs begins when øV2 is clocked high and then low (while holding øH1A high) causing charge to be transferred from øV1 to øV2 and subsequently into the A HCCD. The A register can now be read out in single line mode. If it is desired to operate the device in a dual line readout mode for higher frame rates, this line is transferred into the B HCCD by clocking øH1A to a low state, and øH1B to a high state while holding øH2 low. After øH1A is returned to a high state, the next line can be transferred into the A HCCD. After this clocking sequence, both HCCDs are read out in parallel.

The charge capacity of the horizontal CCDs is slightly more than twice that of the vertical CCDs. This feature allows the user to perform two-to-one line aggregation in the charge domain during V-to-H transfer. This device is also equipped with a fast dump feature that allows the user to selectively dump complete lines (or rows) of pixels at a time. This dump, or line clear, is also accomplished during the V-to-H transfer time by clocking the fast dump gate. To operate either of the features, please consult Eastman Kodak Company for details.

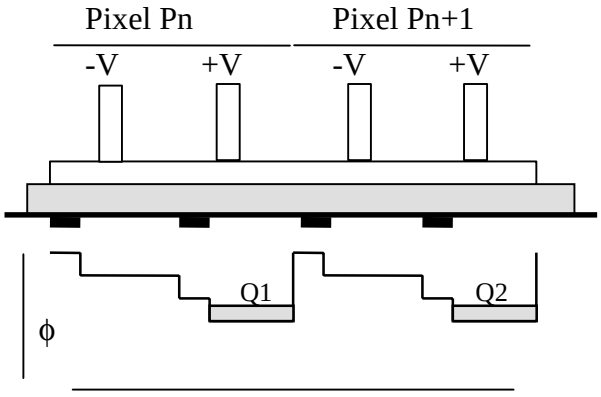



Figure 3 True 2 Phase CCD Cross Section

## 1.6 Output Structure

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression ΔVfd=ΔQ/Cfd. A three stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of µV/e⁻. After the signal has been sampled off-chip, the reset clock (øR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage(VRD).

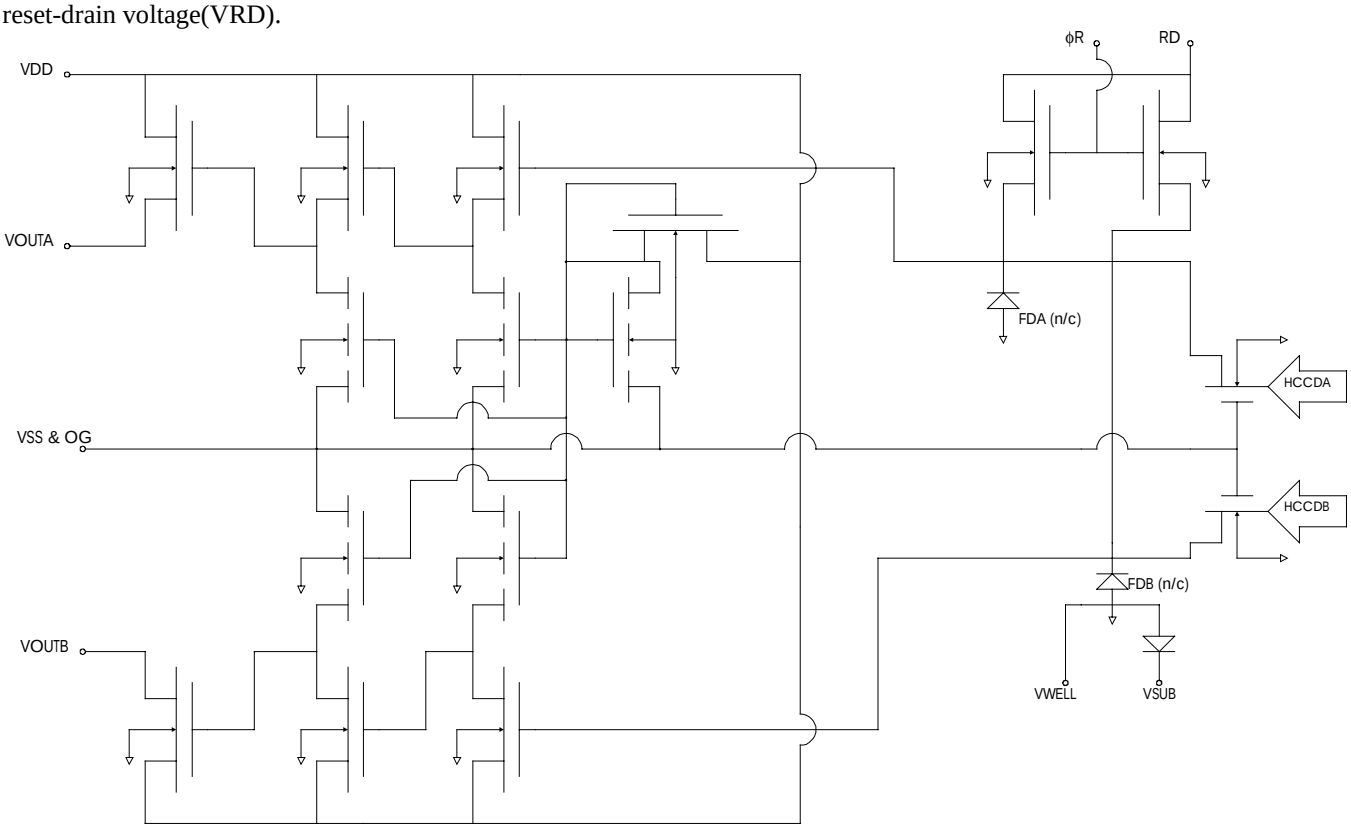



Figure 4 Output Structure

## 1.7 Electronic Shutter

The KAI-1010 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD) . This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on ϕV1. The integration time is then the time between the falling edges of the substrate shutter pulse and ϕV1. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feedthrough. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

## 1.8 Color Filter Array (optional, for KAI-1010CM only)

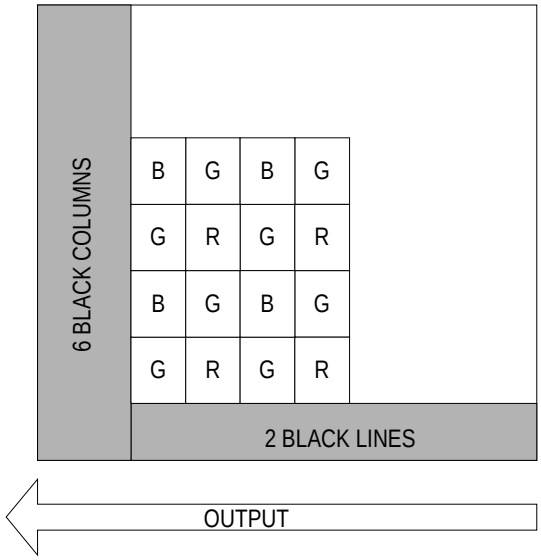
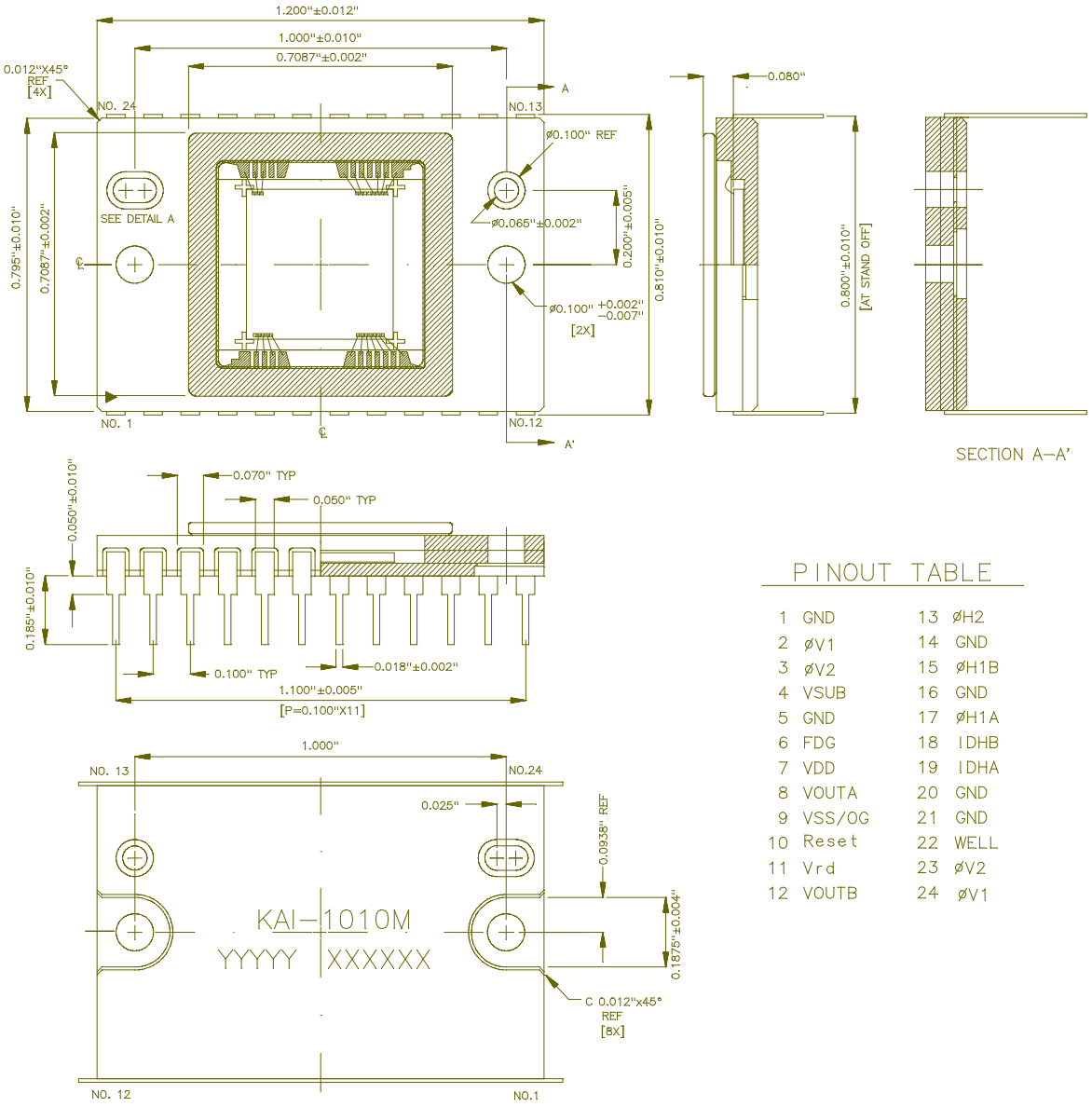



Figure 5 CFA Pattern

## 2.1 Packaging Configuration




PINOUT TABLE

| | | | |
|---|---|---|---|
| 1 | GND | 13 | øH2 |
| 2 | øV1 | 14 | GND |
| 3 | øV2 | 15 | øH1B |
| 4 | VSUB | 16 | GND |
| 5 | GND | 17 | øH1A |
| 6 | FDG | 18 | IDHB |
| 7 | VDD | 19 | IDHA |
| 8 | VOUTA | 20 | GND |
| 9 | VSS/OG | 21 | GND |
| 10 | Reset | 22 | WELL |
| 11 | Vrd | 23 | øV2 |
| 12 | VOUTB | 24 | øV1 |

Figure 6 Device Drawing #6 Die Placement

## 2.2 Pin Description

| PIN NO. | SYMBOL | DESCRIPTION | Notes |
|---|---|---|---|
| 1,5,14,16,20,21 | GND | Ground | 1 |
| 2, 24 | øV1 | Vertical CCD Clock - Phase 1 | 2 |
| 3, 23 | øV2 | Vertical CCD Clock - Phase 2 | 3 |
| 4 | SUB | Substrate | |
| 6 | FDG | Fast Dump Gate | |
| 7 | VDD | Output Amplifier Supply | |
| 8 | VOUTA | Video Output Channel A | |
| 9 | VSS | Output Amplifier Return & OG | |
| 10 | øR | Reset Clock | |
| 11 | VRD | Reset Drain | |
| 12 | VOUTB | Video Output Channel B | |
| 13 | øH2 | A & B Horizontal CCD Clock - Phase 2 | |
| 15 | øH1B | B Horizontal CCD Clock - Phase 1 | |
| 17 | øH1A | A Horizontal CCD Clock - Phase 1 | |
| 18 | IDHB | Input Diode B Horizontal CCD | |
| 19 | IDHA | Input Diode A Horizontal CCD | |
| 22 | WELL | P-Well | |

Table 1 Package Pin Assignments

Notes:
1. All GND pins should be connected to WELL (P-Well).
2. Pins 2 and 24 must be connected together - only 1 Phase 1 clock driver is required.
3. Pins 3and 23 must be connected together - only 1 Phase 2 clock driver is required.

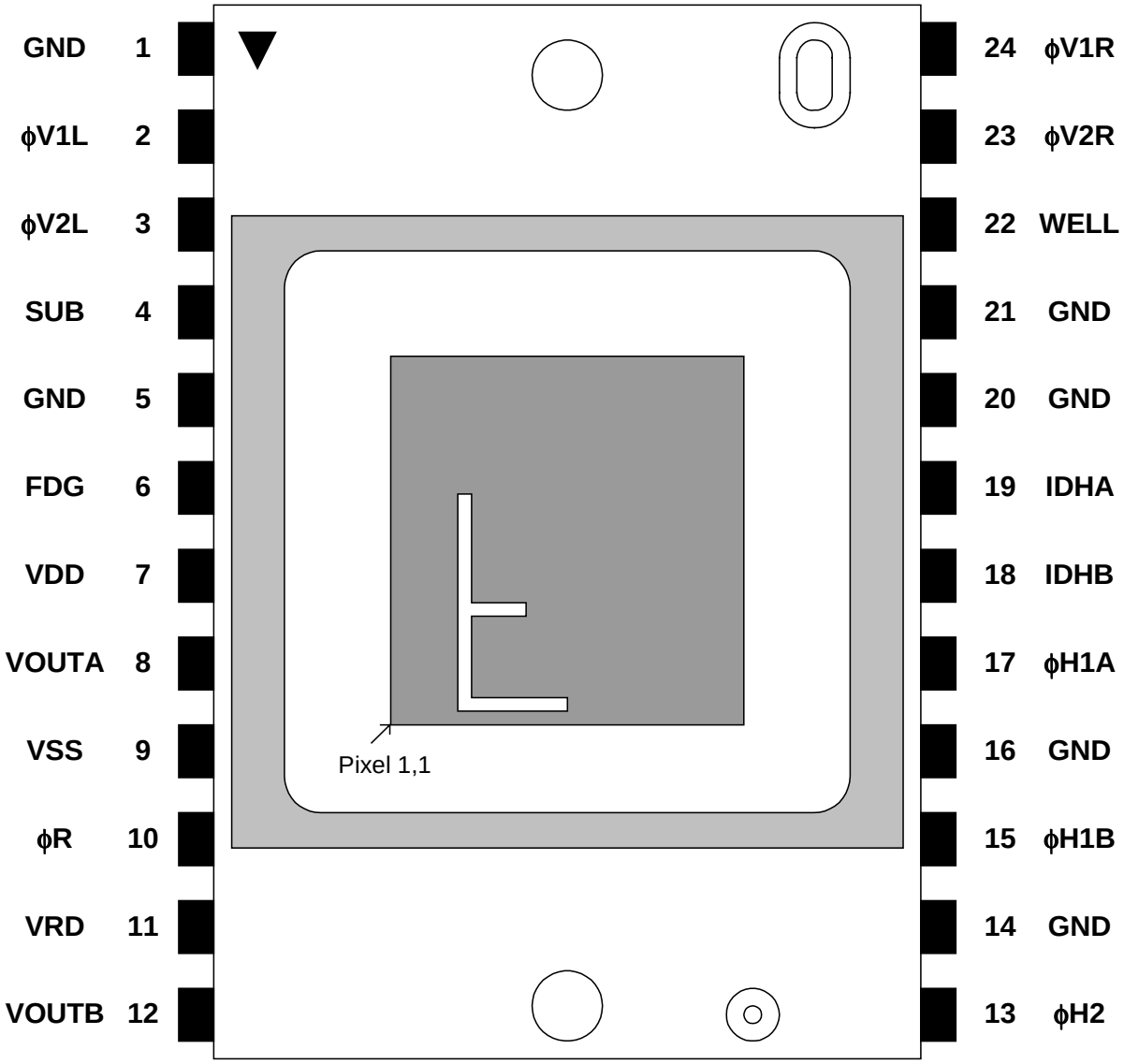



Figure 7 Pinout Diagram Top View

## 2.3 Absolute Maximum Range

| RATING | DESCRIPTION | MIN. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|
| Temperature | Operation Without Damage | -50 | +70 | °C | |
| (@ 10% ±5%RH) | Storage | -55 | +70 | °C | |
| Voltage | SUB-WELL | 0 | +40 | V | 1 |
| (Between Pins) | VRD,VDD,OG&VSS-WELL | 0 | +15 | V | 2 |
| | IDHA,B & VOUTA,B - WELL | 0 | +15 | V | 2 |
| | ϕV1 - ϕV2 | -12 | +20 | V | 2 |
| | ϕH1A, ϕH1B - ϕH2 | -12 | +15 | V | 2 |
| | ϕH1A, ϕH1B, ϕH2, FDG - ϕV2 | -12 | +15 | V | 2 |
| | ϕH2 - OG & VSS | -12 | +15 | V | 2 |
| | ϕR - SUB | -20 | 0 | V | 1,2,4 |
| | All Clocks - WELL | -12 | +15 | V | 2 |
| Current | Output Bias Current ($I_{out}$) | ---- | 10 | mA | 3 |

Table 2 Absolute Maximum Ranges

Notes:
1. Under normal operating conditions the substrate voltage should be above +7V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
3. Per Output. $I_{out}$ affects the band-width of the outputs.
4. ϕR should never be more positive than VSUB.

## 2.4 DC Operating Conditions[7]

| SYMBOL | DESCRIPTION | MIN. | NOM. | MAX. | UNITS | PIN IMPEDANCE[6] | NOTES |
|---|---|---|---|---|---|---|---|
| VRD | Reset Drain | 8.5 | 9 | 9.5 | V | 5pF, > 1.2MΩ | |
| IRD | Reset Drain Current | | 0.2 | | mA | | |
| VSS | Output Amplifier Return & OG | | 0 | | V | 30pF, >1.2MΩ | |
| ISS | Output Amplifier Return Current | | 5 | | mA | | |
| VDD | Output Amplifier Supply | 12 | 15.0 | 15.0 | V | 30pF, >1.2MΩ | |
| Iout | Output Bias Current | | 5 | 10 | mA | | 5 |
| WELL | P-well | ---- | 0.0 | ---- | V | Common | 1 |
| GND | Ground | ----- | 0.0 | ---- | V | | 1 |
| FDG | Fast Dump Gate | -7.0 | -6.0 | -5.5 | V | 20pF, >1.2MΩ | 2 |
| SUB | Substrate | 7 | Vsub | 15 | V | 1nF, >1.2MΩ | 3 |
| IDHA, IDHB | Input Diode A, B Horizontal CCD | 12.0 | 15.0 | 15.0 | V | 5pF, > 1.2MΩ | 4 |

Table 3 DC Operating Conditions

Notes:
1. The WELL and GND pins should be connected to P-well ground.
2. The voltage level specified will disable the fast dump feature.
3. This pin may be pulsed to Ves=40V for electronic shuttering
4. Electrical injection test pins. Connect to VDD power supply.
5. Per output. Note also that $I_{out}$ affects the bandwidth of the outputs.
6. Pins shown with impedances greater than 1.2 Mohm are expected resistances. These pins are only verified to 1.2 Mohm.
7. The operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.

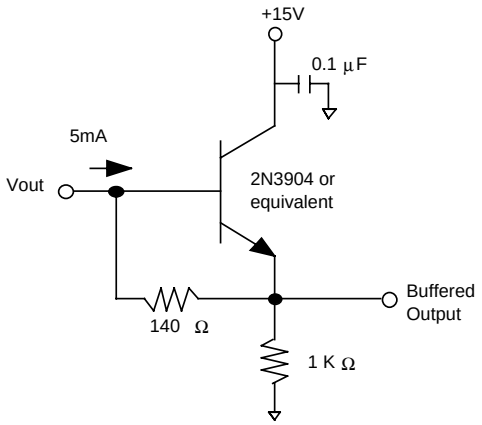



Figure 8 Recommended Output Structure Load Diagram

**Cautions:**
**In order to obtain maximum device performance, gate protection is not provided. Extreme care must be taken in handling to prevent electrostatic discharge which may permanently damage the device. Care must be taken not to short the outputs to ground or VDD during operations.**

## 2.5 AC Clock Level Conditions[1]

| SYMBOL | DESCRIPTION | Level | Min. | NOM. | MAX. | UNITS | PIN IMPEDANCE[2] |
|---|---|---|---|---|---|---|---|
| ϕV1 | Vertical CCD Clock | Low | -10.0 | -9.5 | -9.0 | V | 25nF, >1.2MΩ |
| | | Mid | 0.0 | 0.2 | 0.4 | V | |
| | | High | 8.5 | 9.0 | 9.5 | V | |
| ϕV2 | Vertical CCD Clock | Low | -10.0 | -9.5 | -9.0 | V | 25nF, >1.2MΩ |
| | | High | 0.0 | 0.2 | 0.4 | V | |
| ϕH1A | ϕ1 Horizontal CCD A Clock | Low | -7.5 | -7.0 | -6.5 | V | 100pF, > 1.2MΩ |
| | | High | 2.5 | 3.0 | 3.5 | V | |
| ϕH1B[4] | ϕ1 Horizontal CCD B Clock (single register mode) | Low | -7.5 | -7.0 | -6.5 | V | 100pF, > 1.2MΩ |
| | | | | | | | |
| ϕH1B[4] | ϕ1 Horizontal CCD B Clock (dual register mode) | Low | -7.5 | -7.0 | -6.5 | V | 100pF, > 1.2MΩ |
| | | High | 2.5 | 3.0 | 3.5 | V | |
| ϕH2 | ϕ2 Horizontal CCD Clock | Low | -7.5 | -7.0 | -6.5 | V | 125pF, > 1.2MΩ |
| | | High | 2.5 | 3.0 | 3.5 | V | |
| ϕR | Reset Clock | Low | -6.5 | -6.0 | -5.5 | V | 5pF, > 1.2MΩ |
| | | High | -0.5 | 0.0 | 0.5 | V | |
| ϕFDG[3] | Fast Dump Gate Clock | Low | -7.0 | -6.0 | -5.5 | V | 20pF, > 1.2MΩ |
| | | High | 4.5 | 5.0 | 5.5 | V | |

Table 4 AC Clock Level Conditions

Notes:
1. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
2. Pins shown with impedances greater than 1.2 Mohm are expected resistances. These pins are only verified to 1.2 Mohm.
3. When not used, refer to DC operating condition.
4. For single register mode, set ϕH1B to -7.0 volts at all times rather than clocking it.

This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

## 2.6 AC Timing Requirements for 20 MHz Operation

| SYMBOL | DESCRIPTION | MIN | NOM | MAX | UNITS | NOTES | FIGURE |
|---|---|---|---|---|---|---|---|
| tϕR | Reset Pulse Width | | 10 | | nsec | | Figure 11 |
| t es | Electronic Shutter Pulse Width | 10 | 25 | | µsec | | Figure 12 |
| t int | Integration Time | 0.1 | | | msec | 1 | Figure 12 |
| t ϕVh | Photodiode to VCCD Transfer Pulse Width | 4 | 5 | | µsec | 2 | Figure 9 |
| t cd | Clamp Delay | | 15 | | nsec | | Figure 11 |
| t cp | Clamp Pulse Width | | 15 | | nsec | | Figure 11 |
| t sd | Sample Delay | | 35 | | nsec | | Figure 11 |
| t sp | Sample Pulse Width | | 15 | | nsec | | Figure 11 |
| t rd | Vertical Readout Delay | 10 | ---- | ---- | µsec | | Figure 9 |
| t ϕV | ϕV1, ϕV2 Pulse Width | 3 | ---- | | µsec | | Figure 10 |
| t ϕH | Clock Frequency ϕH1A, ϕH1B , ϕH2 | ---- | 20 | | MHz | | Figure 11 |
| t ϕAB | Line A to Line B Transfer Pulse Width | | 3 | | µsec | | Figure 14 |
| t ϕHd | Horizontal Delay | 3 | | | µsec | | Figure 10 |
| t ϕVd | Vertical Delay | 25 | | | nsec | | Figure 10 |
| t ϕHVES | Horizontal Delay with Electronic Shutter | 1 | | | µsec | | Figure 12 |

Table 5 AC Timing Requirements for 20 MHz Operation

Notes:
1. Integration time varies with shutter speed. It is to be noted that smear increases when integration time decreases below readout time (frame time). Photodiode dark current increases when integration time increases, while CCD dark current increases with readout time (frame time).
2. Antiblooming function is off during photodiode to VCCD transfer.

## Frame Timing - Single Register Readout

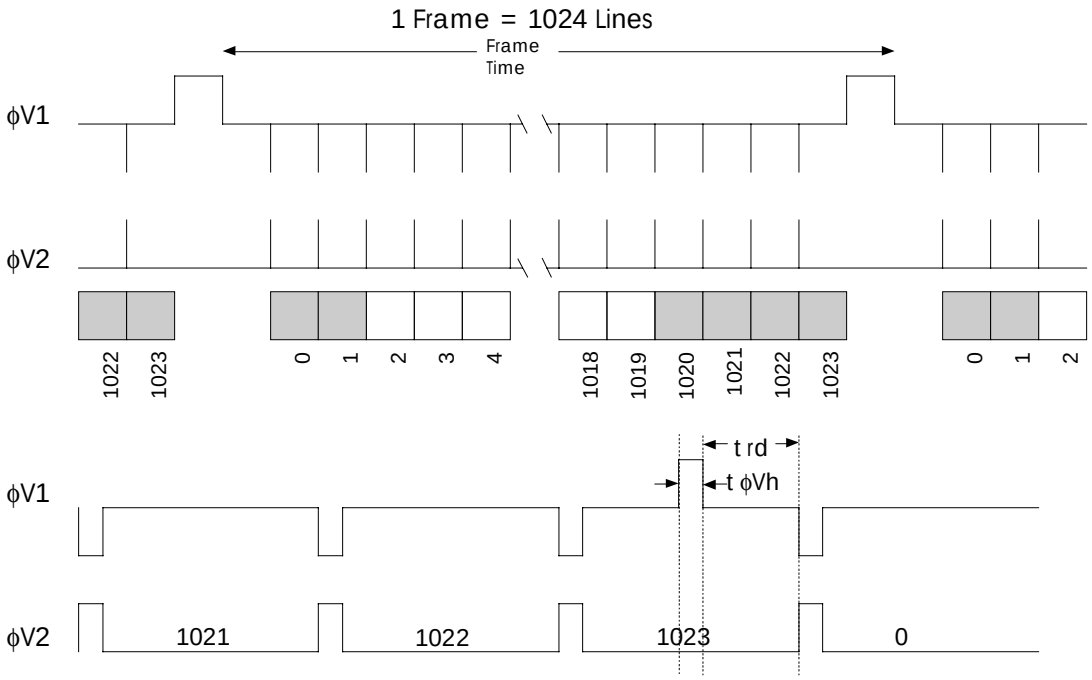
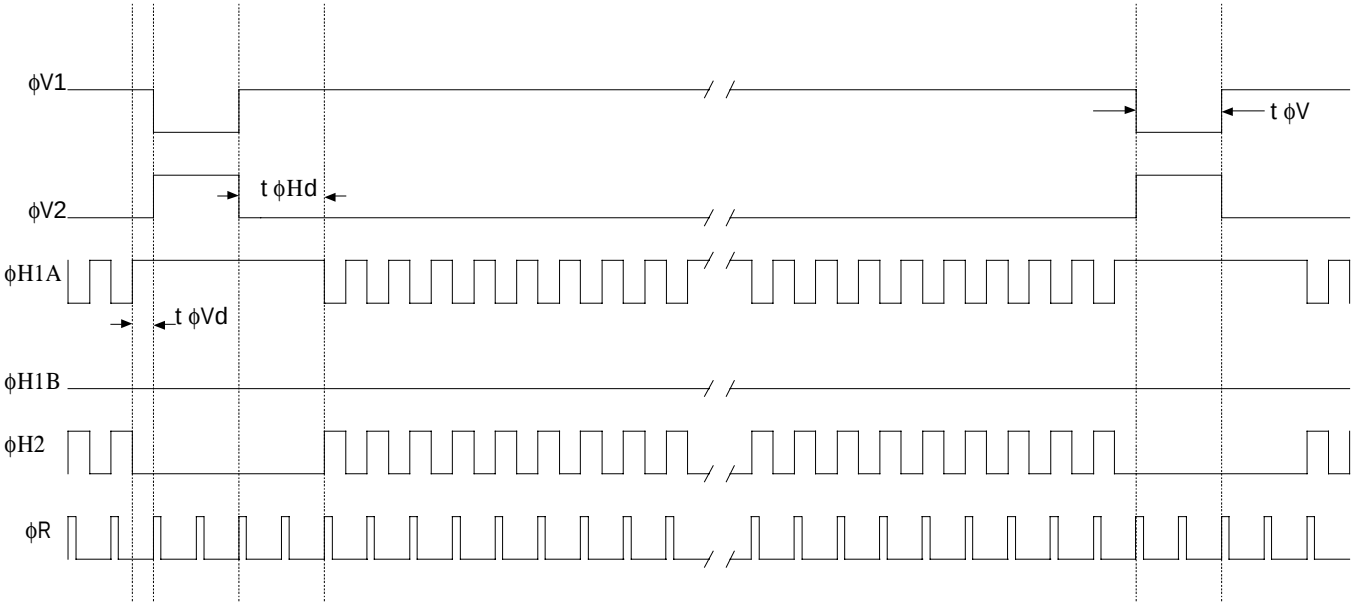



Figure 9 Frame Timing - Single Register Readout

Note : When no electronic shutter is used, the integration time is equal to the frame time.

## Line Timing - Single Register Readout




H1B held low for single register operation

Line Content

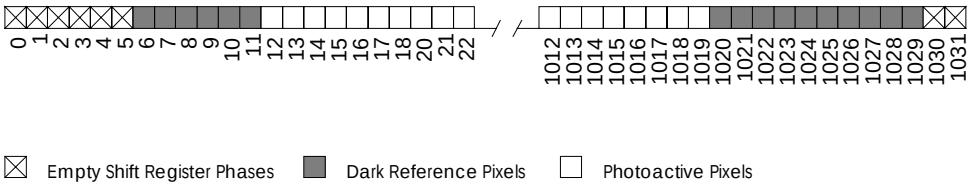



Figure 10 Line Timing - Single Register Output

## Pixel Timing - Single Register Readout

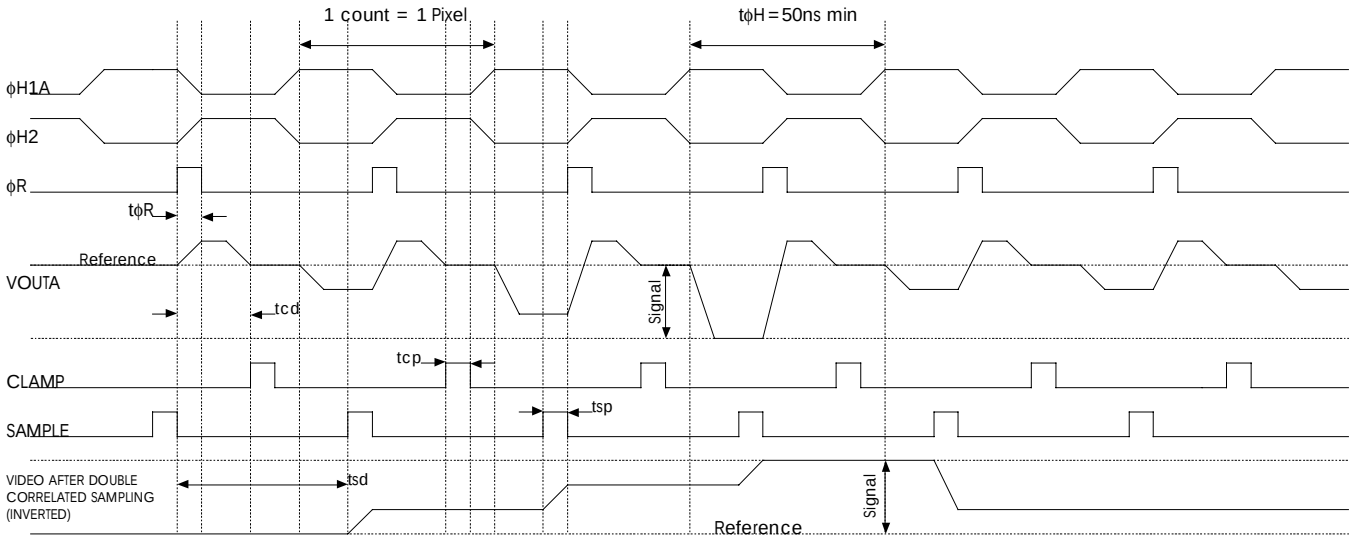
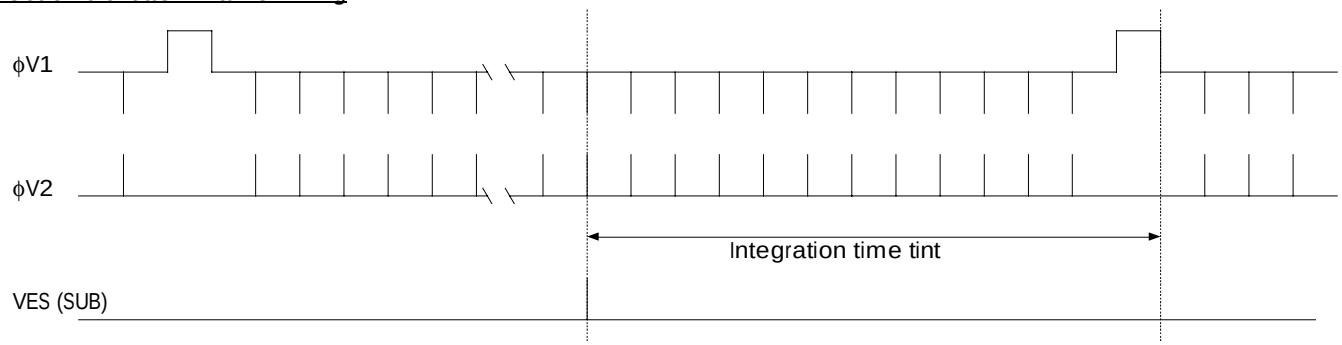


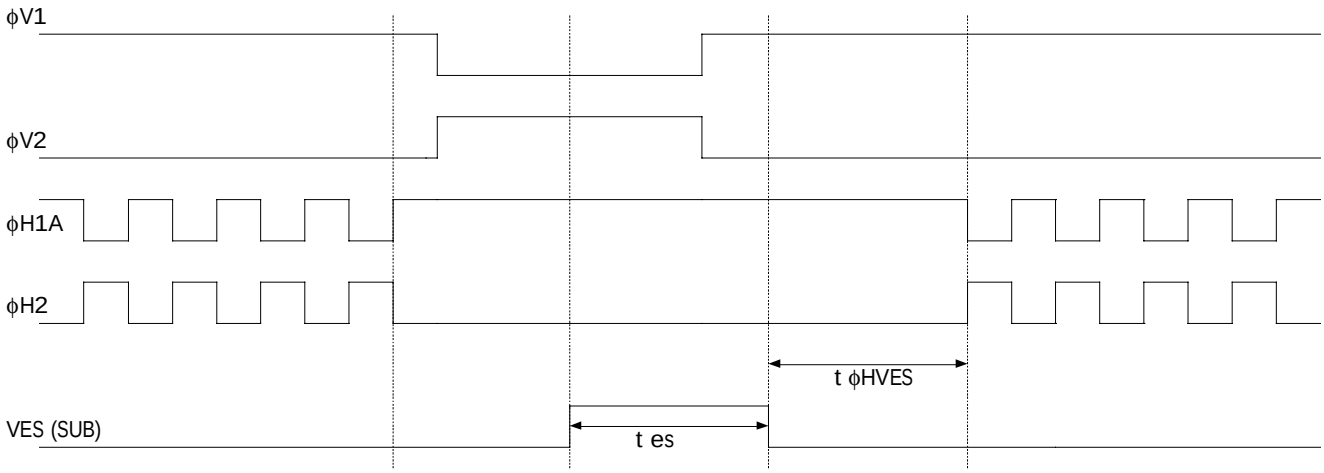

Figure 11 Pixel Timing Diagram - Single Register Readout

## Electronic Shutter Timing - Single Register Readout

Electronic Shutter - Frame Timing




Electronic Shutter - Placement




Electronic Shutter - Operating Voltages

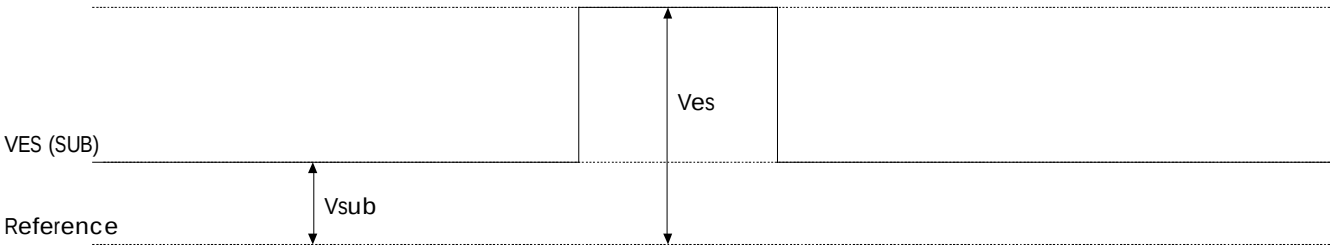



Figure 12 Electronic Shutter Timing Diagram - Single Register Readout

## Frame Timing - Dual Register Readout

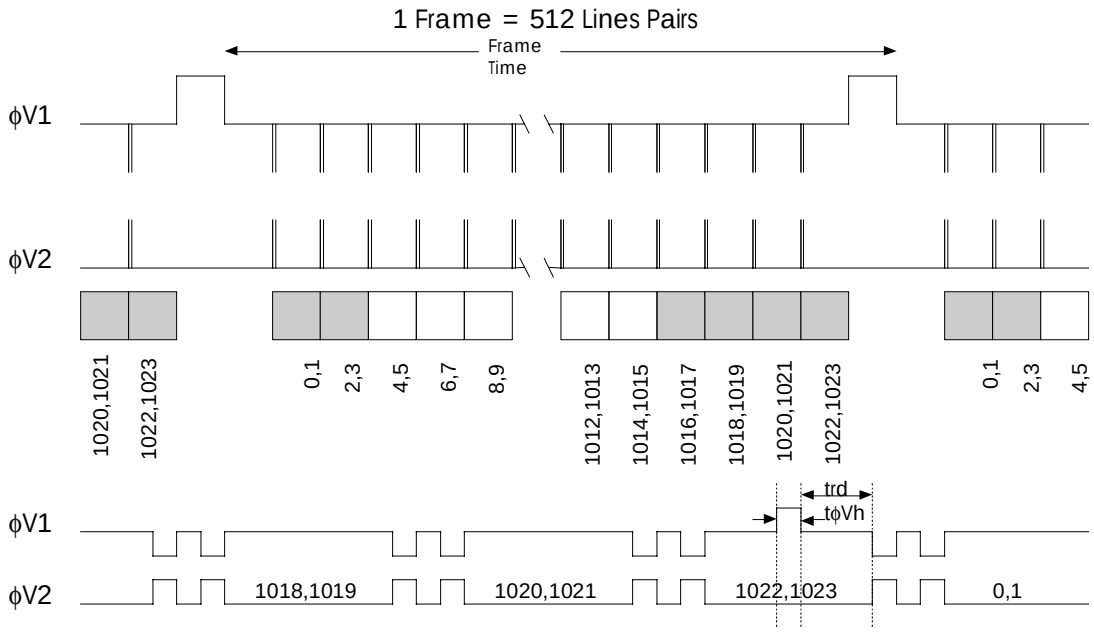
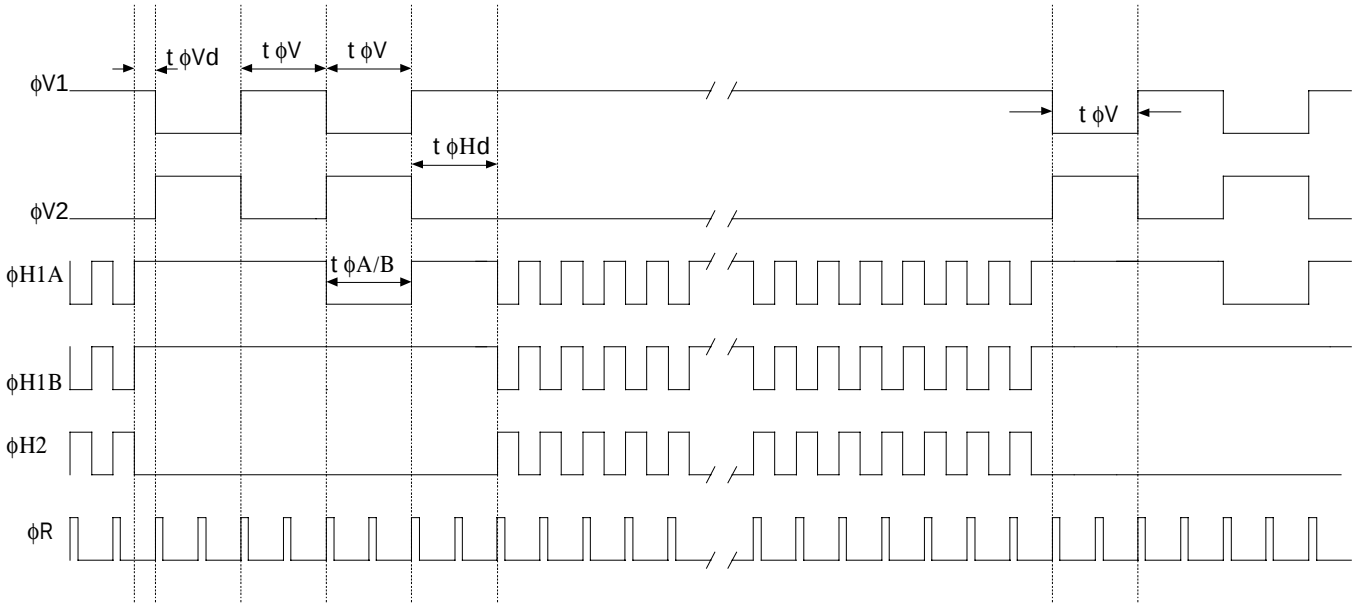



Figure 13 Frame Timing - Dual Register Readout

Note : When no electronic shutter is used, the integration time is equal to the frame time.

## Line Timing - Dual Register Readout



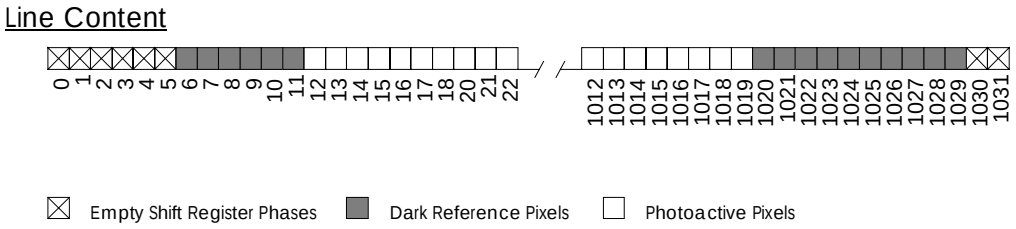




Figure 14 Line Timing - Dual Register Output

## Pixel Timing - Dual Register Readout

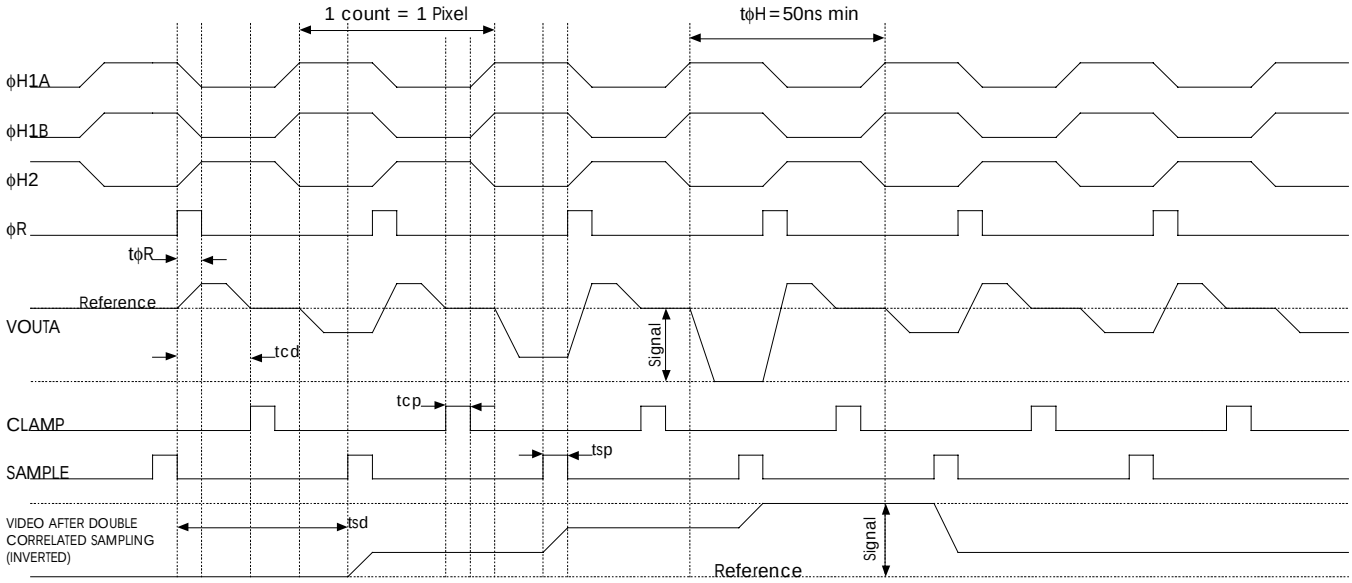



Figure 15 Pixel Timing Diagram - Dual Register Readout

## 3.2 Image Specifications

All the following values were derived using nominal operating conditions using the recommended timing. Unless otherwise stated, readout time = 140ms, integration time = 140ms and sensor temperature = 40°C. Correlated double sampling of the output is assumed and recommended. Many units are expressed in electrons, to convert to voltage, multiply by the amplifier sensitivity.
Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

### Electro-Optical for KAI-1010CM

| SYMBOL | PARAMETER | MIN. | NOM. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| F F | Optical Fill Factor | | 55.0 | | % | |
| $E_{sat}$ | Saturation Exposure | | 0.046 | | $\mu J/cm^2$ | 1 |
| $QE_r$ | Red Peak Quantum Efficiency $\lambda$ = 650nm | | 22 | | % | 2 |
| $QE_g$ | Green Peak Quantum Efficiency $\lambda$ =530nm | | 28 | | % | 2 |
| $QE_b$ | Blue Peak Quantum Efficiency $\lambda$ = 450nm | | 20 | | % | 2 |
| $R_{gs}$ | Green Photoresponse Shading | | 6 | | % | 4 |
| PRNU | Photoresponse Non-uniformity | | 5.0 | | p-p % | 3 |
| PRNL | Photoresponse Non-linearity | | 5.0 | | % | |
| | Amplifier Sensitivity | | 11.5 | | $\mu V/e^-$ | |

Table 6 Electro-Optical Image Specifications KAI-1010CM

Notes:
1. For $\lambda$ = 530nm wavelength, and Vsat = 350mV.
2. Refer to typical values from Figure 16 Nominal KAI 1010CM Spectral Response.
3. Under uniform illumination with output signal equal to 280 mV.
4. This is the global variation in chip output for green pixels across the entire chip.
5. It is recommended to use low pass filter with $\lambda_{cut\text{-}off}$ at ~ 680nm for high performance.

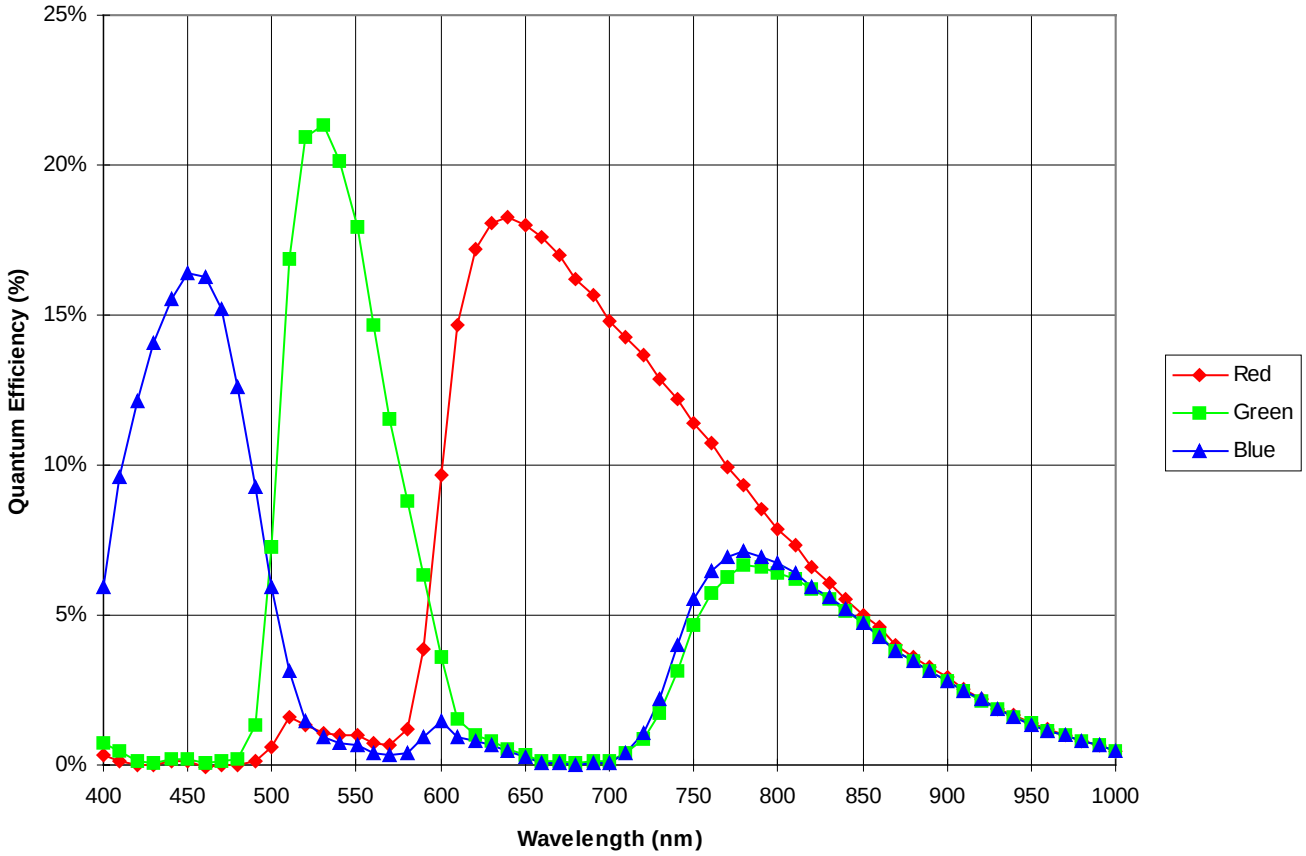



Figure 16 Nominal KAI 1010CM Spectral Response

## Electro-Optical for KAI-1010M

| SYMBOL | PARAMETER | MIN. | NOM. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| F F | Optical Fill Factor | | 55.0 | | % | |
| $E_{sat}$ | Saturation Exposure | | 0.037 | | $\mu J/cm^2$ | 1 |
| QE | Peak Quantum Efficiency | | 37 | | % | 2 |
| PRNU | Photoresponse Non-uniformity | | 5.0 | | p-p % | 3 |
| PRNL | Photoresponse Non-linearity | | 5.0 | | % | |

Table 7 Electro-Optical Image Specifications KAI-1010M

Notes:
1. For λ = 550nm wavelength, and Vsat = 350mV.
2. Refer to typical values from Figure 17 Nominal KAI-1010M Spectral Response
3. Under uniform illumination with output signal equal to 280 mV.

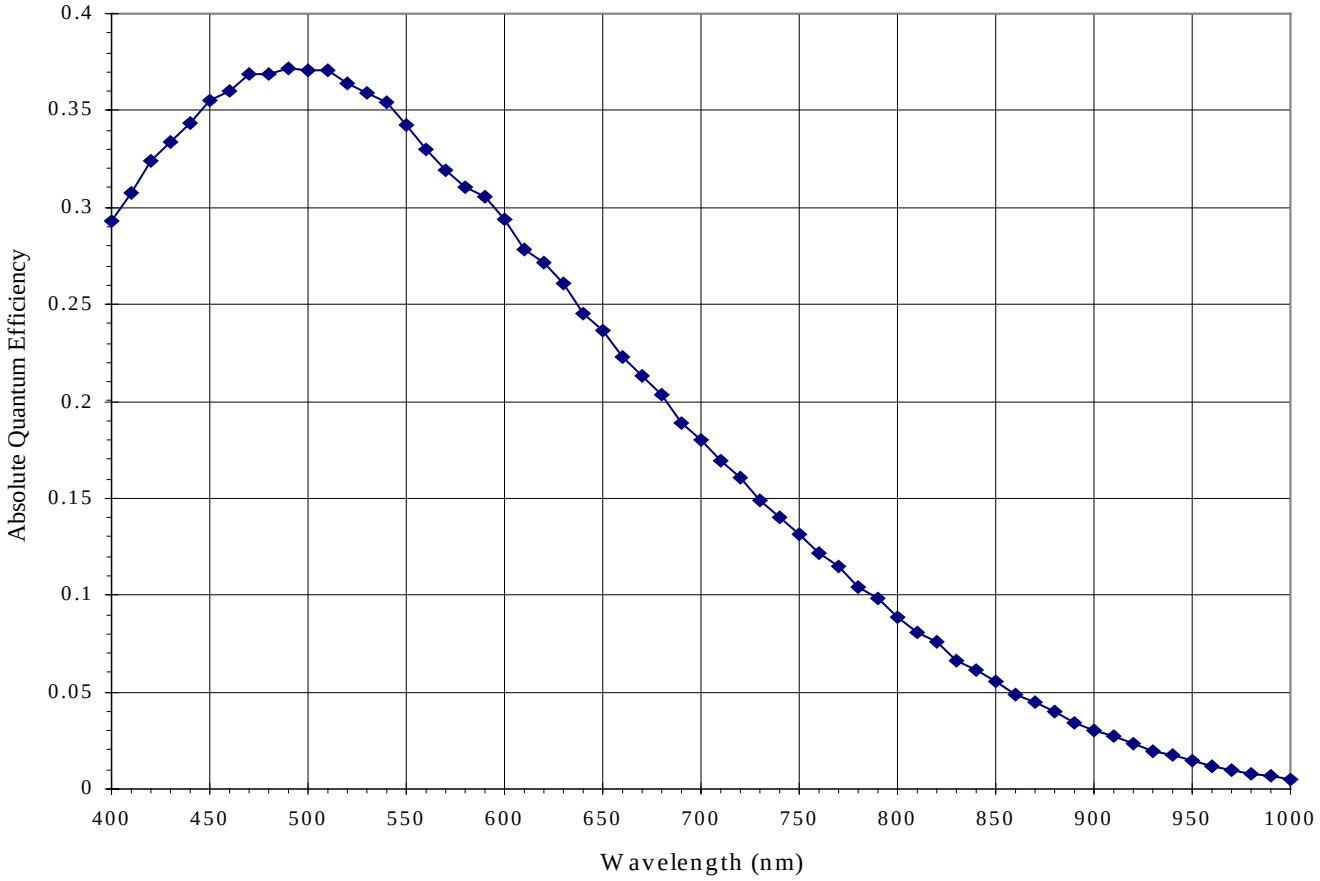



Figure 17 Nominal KAI-1010M Spectral Response

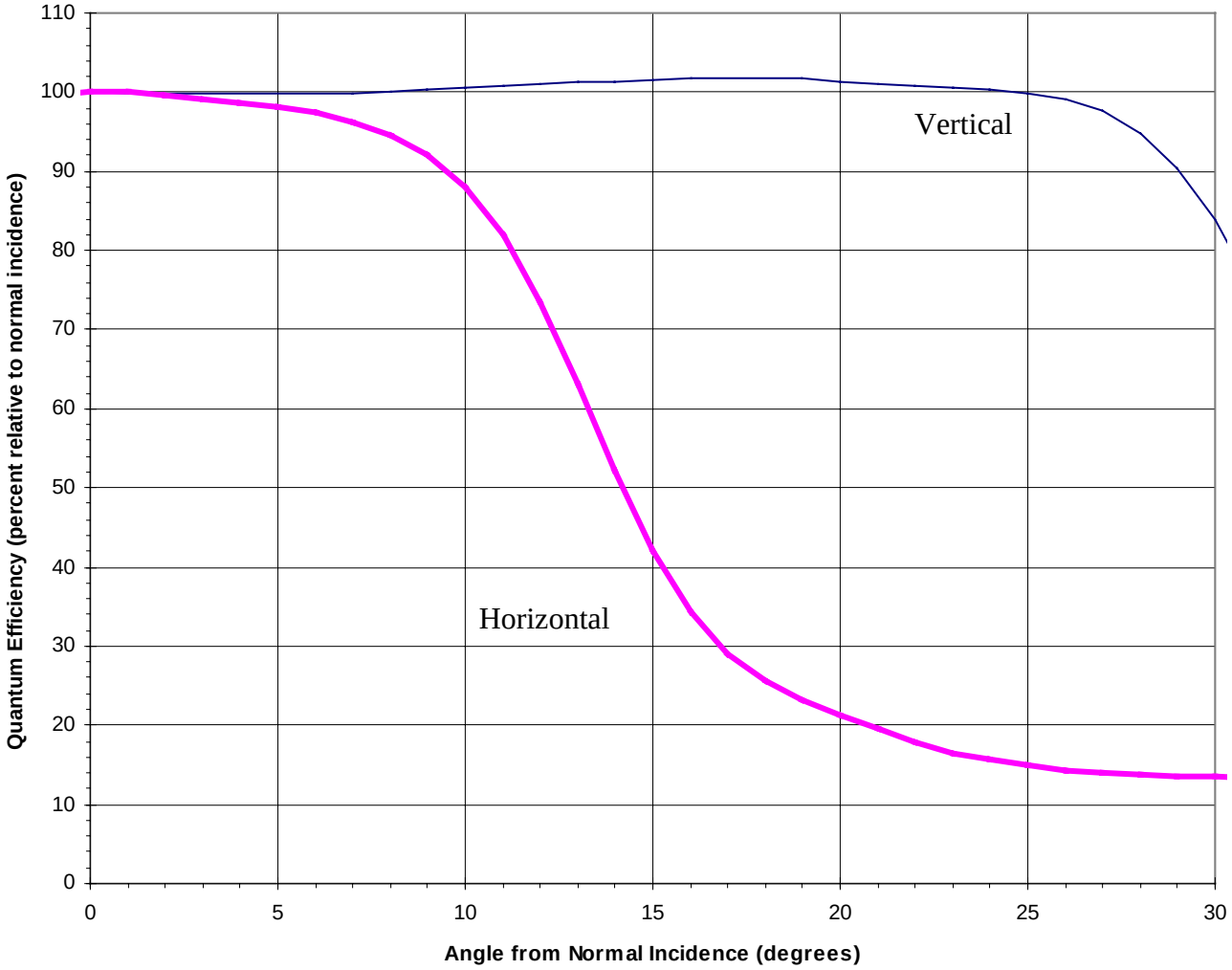



Figure 18 Angular Dependence of Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD. For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

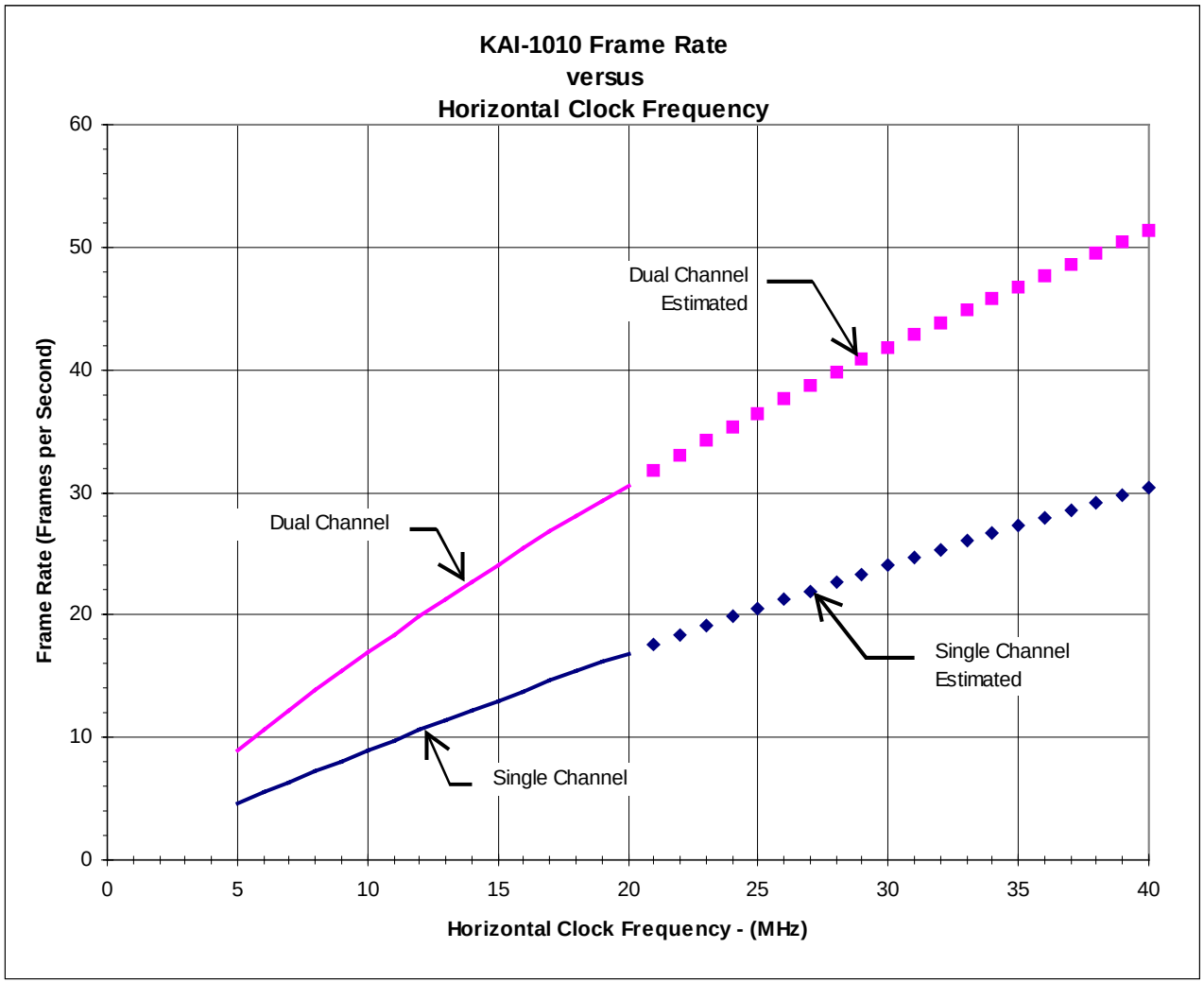



Figure 19 Frame Rate versus Horizontal Clock Frequency

## CCD

| SYMBOL | PARAMETER | MIN. | NOM. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Vsat | Output Saturation Voltage | | 350 | | mV | 1,2,8 |
| $I_d$ | Dark Current | | | 0.5 | nA | |
| DCDT | Dark Current Doubling Temp | 7 | 8 | 10 | °C | |
| CTE | Charge Transfer Efficiency | | 0.99999 | | | 2,3 |
| $f_H$ | Horizontal CCD Frequency | | | 40 | MHz | 4 |
| IL | Image Lag | | | 100 | $e^-$ | 5 |
| Xab | Blooming Margin | | | 100 | | 6,8 |
| Smr | Vertical Smear | | 0.01 | | % | 7 |

Table 8 CCD Image Specifications

Notes:
1. Vsat is the green pixel mean value at saturation as measured at the output of the device with Xab=1. Vsat can be varied by adjusting Vsub.
2. Measured at sensor output.
3. With stray output load capacitance of $C_L$ = 10 pF between the output and AC ground.
4. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
5. This is the first field decay lag measured by strobe illuminating the device at (Hsat,Vsat), and by then measuring the subsequent frame's average pixel output in the dark.
6. Xab represents the increase above the saturation-irradiance level (Hsat) that the device can be exposed to before blooming of the vertical shift register will occur. It should also be noted that Vout rises above Vsat for irradiance levels above Hsat, as shown in Figure 20.
7. Measured under 10% (~ 100 lines) image height illumination with white light source and without electronic shutter operation and below Vsat.
8. It should be noted that there is trade off between Xab and Vsat.

## Output Amplifier @ $V_{DD}$ = 15V, $V_{SS}$ = 0.0V

| SYMBOL | PARAMETER | MIN. | NOM. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Vodc | Output DC Offset | | 7 | | V | 1,2 |
| Pd | Power Dissipation | ---- | 225 | ---- | mW | 3 |
| $f_{-3db}$ | Output Amplifier Bandwidth | | 140 | | MHz | 1,4 |
| $C_L$ | Off-Chip Load | | | 10 | pF | |

Table 9 Output Amplifier Image Specifications

Notes:
1. Measured at sensor output with constant current load of $I_{out}$ = 5mA per output.
2. Measured with $V_{RD}$ = 9v during the floating-diffusion reset interval, ($\phi$R high), at the sensor output terminals.
3. Both channels.
4. With stray output load capacitance of $C_L$ = 10 pF between the output and AC ground.

## General

| SYMBOL | PARAMETER | MIN. | NOM. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Vn - total | Total Sensor Noise | | 0.5 | | mV, rms | 1 |
| DR | Dynamic Range | | | 60 | dB | 2 |

Table 10 General Image Specifications

Notes: 1. Includes amplifier noise and dark current shot noise at data rates of 10MHz. The number is based on the full bandwidth of the amplifier. It can be reduced when a low pass filter is used.
2. Uses 20LOG(Vsat/Vn - total) where Vsat refers to the output saturation signal.

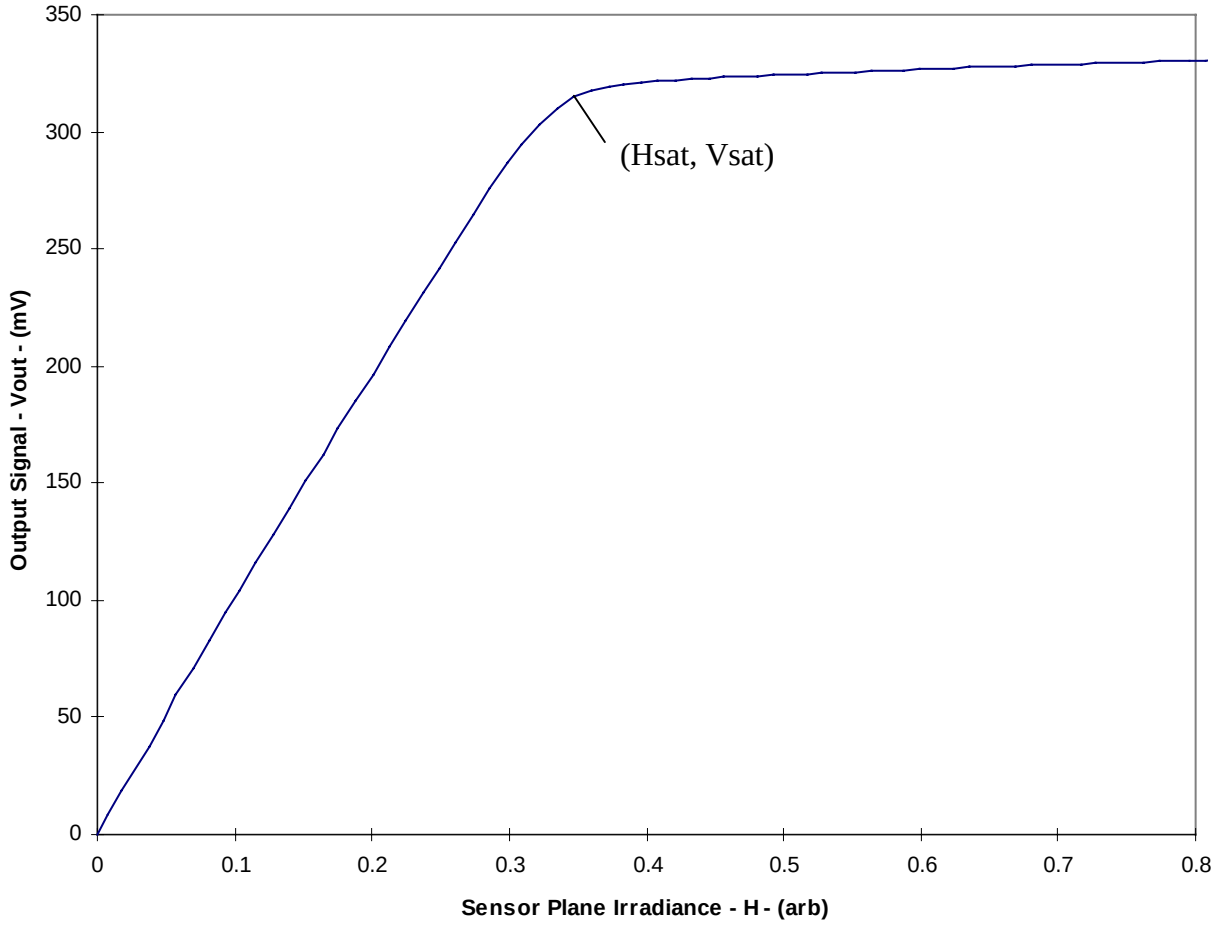



Figure 20 Typical KAI-1010Series Photoresponse

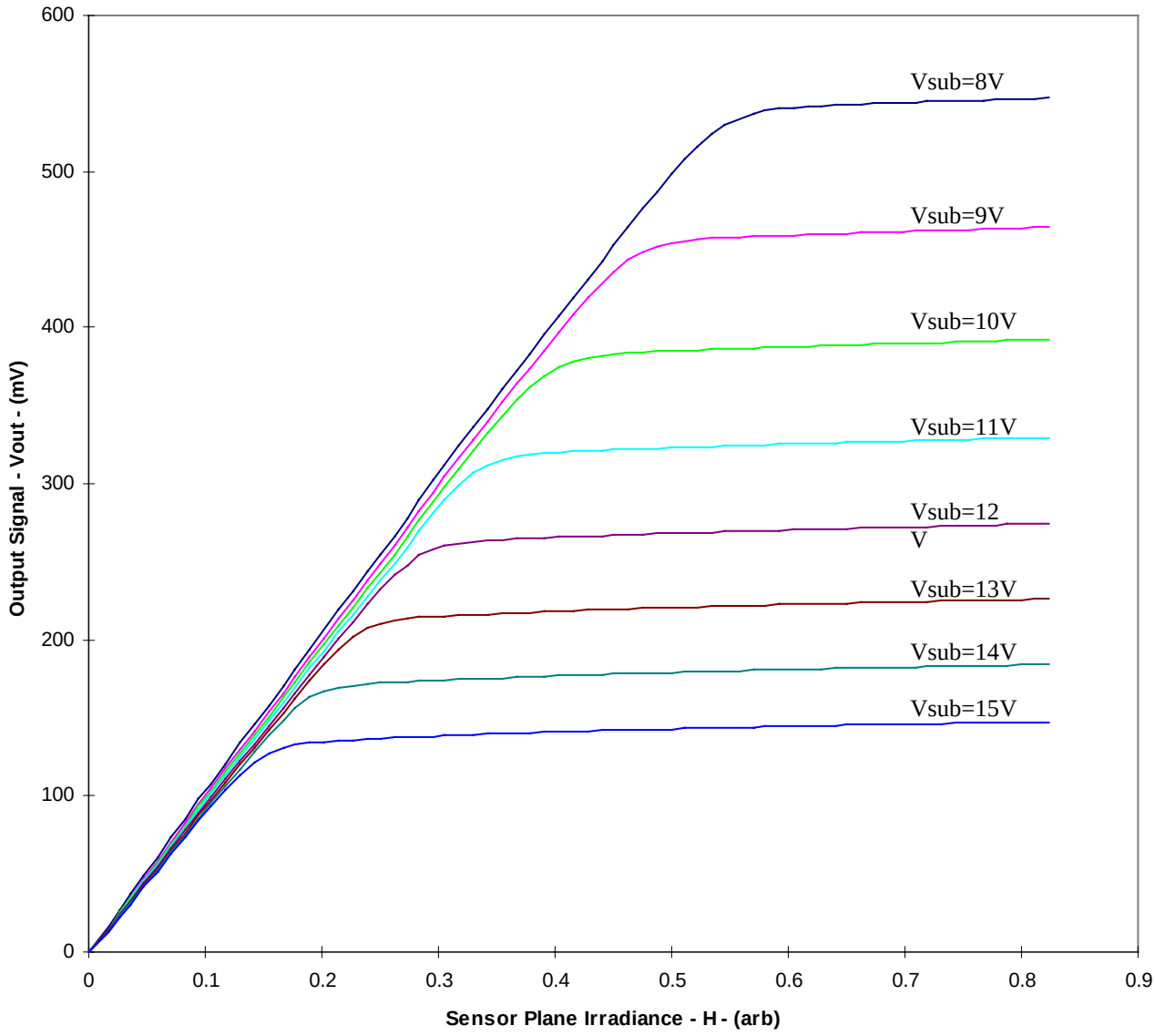



Figure 21 Example of Vsat versus Vsub

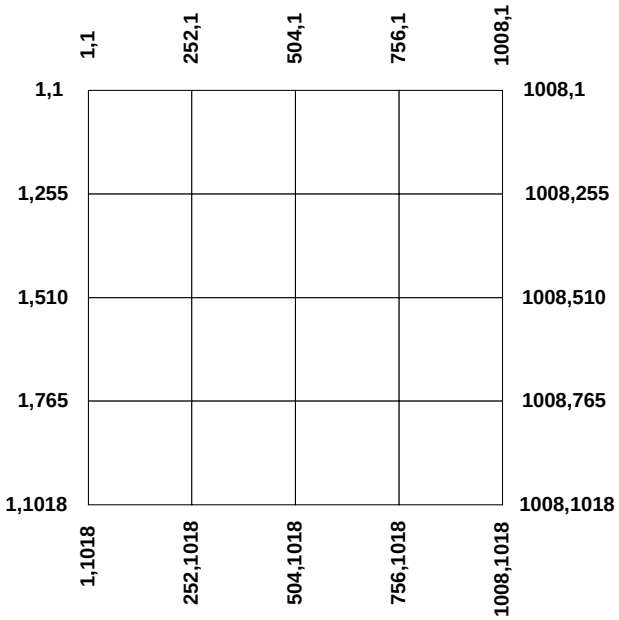
As Vsub is decreased, Vsat increases and anti-blooming protection decreases.
As Vsub is increased, Vsat decreases and anti-blooming protection increases.

## 3.3 Defect Classification

All values derived under nominal operating conditions at 40°C operating temperature.

| Defect Type | Defect Definition | Number Allowed | Notes |
|---|---|---|---|
| Defective Pixel | Under uniform illumination with mean pixel output at 80% of Vsat, a defective pixel deviates by more than 15% from the mean value of all pixels in its section. | 12 | 1,2 |
| Bright Defect | Under dark field conditions, a bright defect deviates more than 15mV from the mean value of all pixels in its section. | 5 | 1,2 |
| Cluster Defect | Two or more vertically or horizontally adjacent defective pixels. | 0 | 2 |

Notes:
1. Sections are 252 (H) x 255 (V) pixel groups, which divide the imager into sixteen equal areas as shown below.
2. For the color device, KAI-1010CM, a defective pixel deviates by more than 15% from the mean value of all active pixels in its section with the same color.




Test Conditions

| | |
|---|---|
| Junction Temperature | $(T_j)$ = 40°C |
| Integration Time | $(t_{int})$ = 70msec |
| Readout Rate | $(t_{readout})$ = 70msec |

## 4.1 Climatic Requirements

| ITEM | DESCRIPTION | MIN. | MAX. | UNITS | CONDITIONS | NOTES |
|---|---|---|---|---|---|---|
| Operation to Specification | Temperature | -25 | +40 | $^{o}$C | @ 10% $\pm$5% RH | 1, 2 |
| | Humidity | 10$\pm$5 | 86$\pm$5 | %RH | @ 36 $\pm$2$^{o}$C Temp. | 1, 2 |
| Operation Without Damage | Temperature | -50 | +70 | $^{o}$C | @ 10% $\pm$5% RH | 2, 3 |
| Storage | Temperature | -55 | +70 | $^{o}$C | @ 10% $\pm$5%RH | 2, 4 |
| | Humidity | ----- | 95$\pm$5 | %RH | @ 49 $\pm$2$^{o}$C Temp. | 2, 4 |

Table 11 Climatic Requirements

Notes:
1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
4. The image sensor shall meet the specifications of this document after storage for 15 days at the specified conditions.

## 4.2 Quality Assurance and Reliability

4.2.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

4.2.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale.

4.2.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

4.2.4 ESD Precautions: Devices are shipped in a static-safe containers and should only be handled at static-safe work stations.

4.2.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.

4.2.6 Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

## 4.3 Ordering Information

See Appendix 1 for available part numbers.

Address all inquiries and purchase orders to:

Microelectronics Technology Division
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
Web: www.kodak.com/go/ccd
E-mail: ccd@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

**WARNING: LIFE SUPPORT APPLICATIONS POLICY**

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

## Appendix1 Part Number Availability

Note:
This appendix may be updated independently of the performance specification.
Contact Eastman Kodak Company for the latest revision.

### Monochrome, Microlens, Sealed Glass

| Device Name | Available Part Numbers | Features |
|---|---|---|
| KAI-1010M | 2H4614 | 1008(H) x 1018(V) active pixel, progressive scan CCD with Microlens, Sealed MAR glass |
| KAI-1010M | 2H4115 | 1008(H) x 1018(V) active pixel, progressive scan CCD with Microlens, Sealed MAR glass, Engineering Class |
| KAI-1010M | 2H4116 | 1008(H) x 1018(V) active pixel, progressive scan CCD with Microlens, Sealed MAR glass, Mechanical Class |

Table 12 Part Numbers - Monochrome, Microlens, Sealed Glass

### Monochrome, Microlens, Taped Glass

| Device Name | Available Part Numbers | Features |
|---|---|---|
| KAI-1010M | 2H4613 | 1008(H) x 1018(V) active pixel, progressive scan CCD with Microlens, Taped MAR glass |
| KAI-1010M | 2H4121 | 1008(H) x 1018(V) active pixel, progressive scan CCD with Microlens, Taped MAR glass, Engineering Class |
| KAI-1010M | 2H4122 | 1008(H) x 1018(V) active pixel, progressive scan CCD with Microlens, Taped MAR glass, Mechanical Class |

Table 13 Part Numbers - Monochrome, Microlens, Taped Glass

### Monochrome, Taped Glass

| Device Name | Available Part Numbers | Features |
|---|---|---|
| KAI-1010 | 2H4615 | 1008(H) x 1018(V) active pixel, progressive scan CCD, Taped MAR glass |

Table 14 Part Numbers - Monochrome, Taped Glass

**Color, Microlens, Sealed Glass**

| Device Name | Available Part Numbers | Features |
|---|---|---|
| KAI-1010CM | 2H4611 | 1008(H) x 1018(V) active pixel, progressive scan CCD with CFA and Microlens, Sealed MAR glass |
| KAI-1010CM | 2H4106 | 1008(H) x 1018(V) active pixel, progressive scan CCD with CFA and Microlens, Sealed MAR glass, Engineering Class |
| KAI-1010CM | 2H4107 | 1008(H) x 1018(V) active pixel, progressive scan CCD with CFA and Microlens, Sealed MAR glass, Mechanical Class |

Table 15 Part Numbers - Color, Microlens, Sealed Glass

**Color, Microlens, Taped Glass**

| Device Name | Available Part Numbers | Features |
|---|---|---|
| KAI-1010CM | 2H4612 | 1008(H) x 1018(V) active pixel, progressive scan CCD with CFA and Microlens, Taped MAR glass |
| KAI-1010CM | 2H4111 | 1008(H) x 1018(V) active pixel, progressive scan CCD with CFA and Microlens, Taped MAR glass, Engineering Class |

Table 16 Part Numbers - Color, Microlens, Taped Glass

**Part Number Definitions**

MAR: Multicoated, both sides, anti-reflective coating