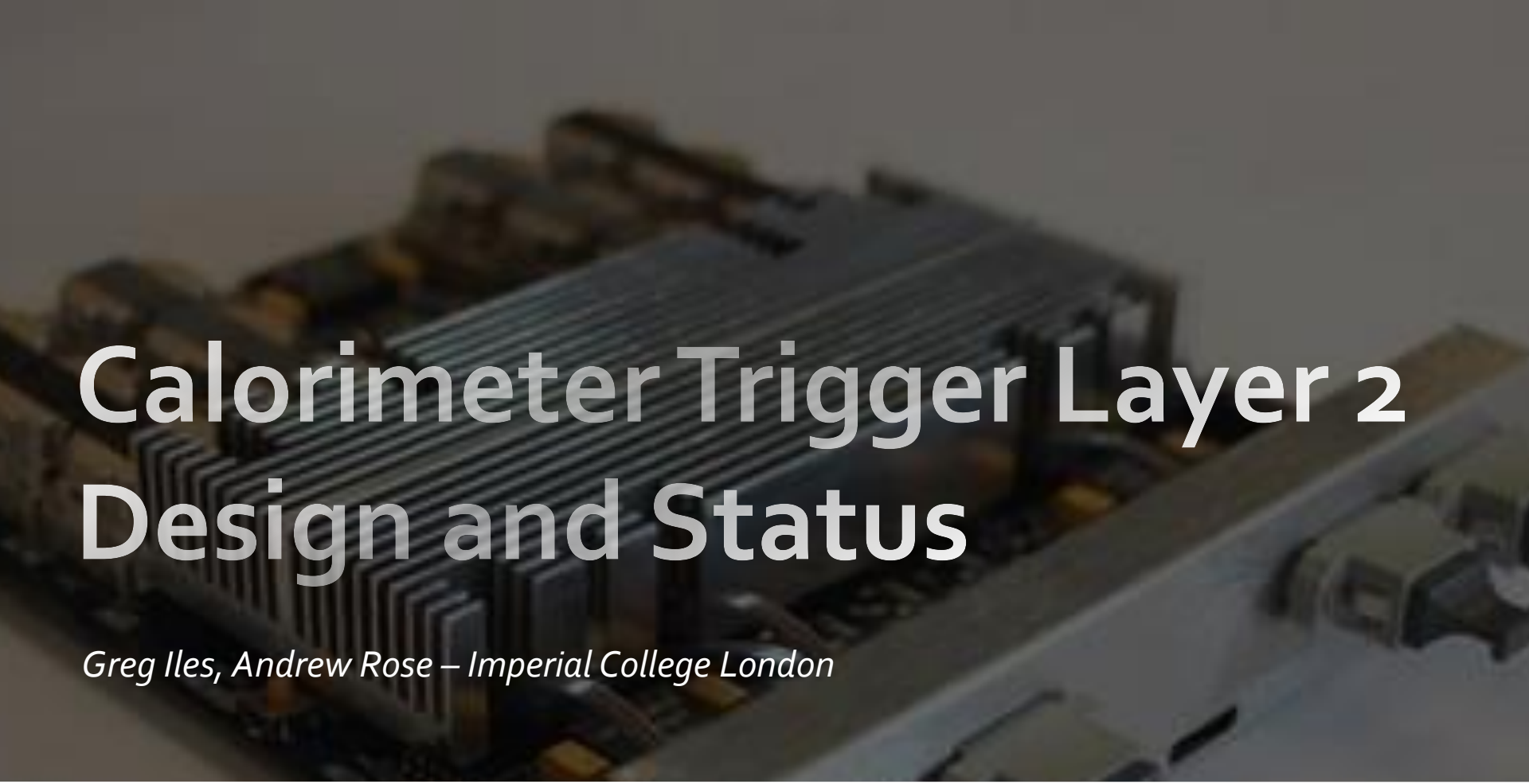


Calorimeter Trigger Layer 2 Design and Status

Greg Iles, Andrew Rose – Imperial College London

Mark Baber, Aaron Bundock, Simon Fayer, Sarah Greenwood, Geoff Hall, Sarah Ives, Robyn Lucas, Jad Marrouche, Alex Tapper – Imperial College London

John Jones – Iceberg Technology

Robin Aggleton, Jim Brooke, Sudeshna Dasgupta, Mark Grimes, Christopher Lucas, Dave Newbold, Sudarshan Paramesvaran, Tom Williams – University of Bristol

Tim Durkin, Kristian Harder, Sam Harper, David Petyt, Dave Sankey, Claire Shepherd-Themistocleous, Alessandro Thea – Rutherford Appleton Laboratory

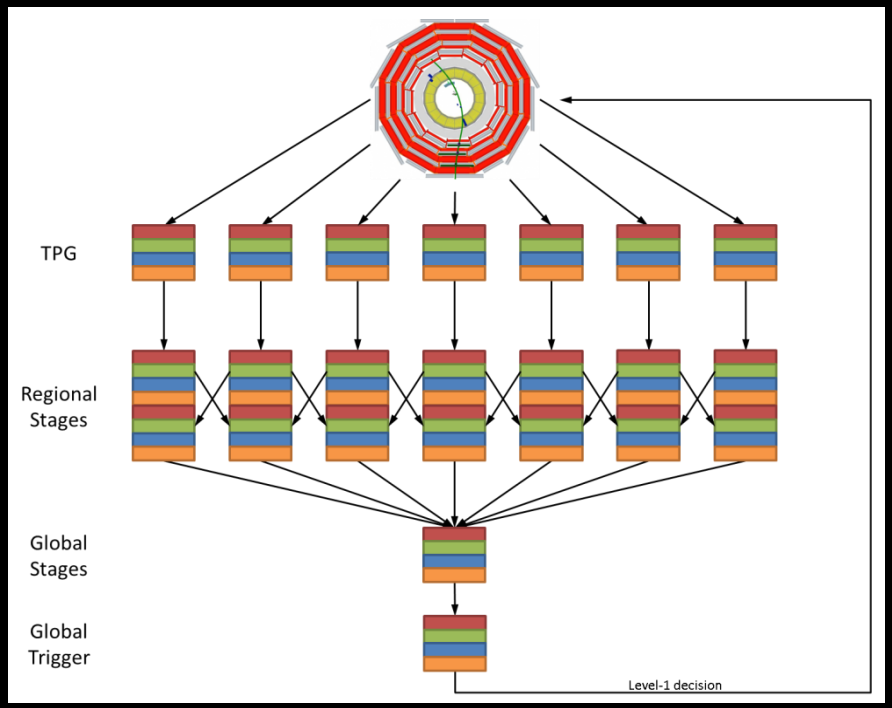
Florian Beaudette, Philippe Busson, Luca Mastrolorenzo, Benoit Renaud, Thierry Romanteau, Jean-Baptiste Sauvan, Alex Zabi – LLR

Overview

- Introduction
- Status of the TMT concept
  - Results of the September TMT Integration Test
- Status of the Layer-2 hardware
  - The MP7 processor card
  - Status of standalone testing
  - MP7 R1
  - Planning and Production
- Status of the Layer-2 firmware
- Status of the Layer-2 software
- Overall Project Status
- Conclusions

Introduction

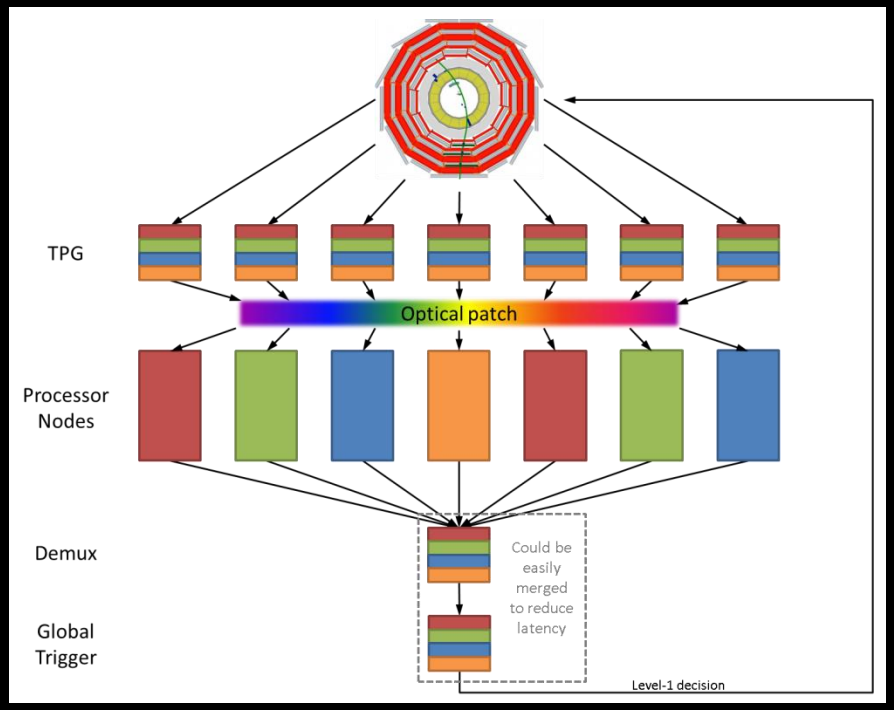
Conventional trigger



Conventional Trigger

- Data is processed in regions
- Boundaries between regions must be handled by sharing or duplicating inputs
- Volume of data reduced at each stage by selecting and discarding candidates
- When volume of data has been sufficiently reduced it can be passed to the global trigger

Time-multiplexed trigger



Time-Multiplexed Trigger

- Data from an event is buffered and retransmitted to the first processing node over *N* bunch crossings
- Data from the next event is buffered and retransmitted to the second processing node, again, over *N* bunch crossings
- Process is repeated in round-robin fashion across ≥*N* processing nodes
- Because both algorithm latency and data volume are constant, dataflow is fully deterministic and no complex scheduling mechanism is required

Reminder of TMT concept

- The Time-multiplexed architecture allows all data to arrive in geometric order:
  - Towers at given ϕ always occupy the same bits on the same optical links
  - Towers arrive in order of increasing |η|
- This converts a 2D geometric problem to a 1D problem
- This allows all algorithms to be fully pipelined†:
  - The processing is localised
  - Fan-outs reduced
  - Routing delays minimised
  - Register duplication eliminated
  - Also only need to develop one FPGA design

†That is, pipelined at the full data rate, not at the bunch-crossing rate

Status of the TMT concept:
TMT integration test

September TMT test objectives

https://twiki.cern.ch/twiki/pub/CMS/L1Calo2013/TMTtestdemonstration_final.pdf

7. Test criteria:

A Pass of the TMT test requires the following objectives to be met:

- Reliable transmission of data @ 10Gbps asynch between PP and MP (36 links with full error checking) - “reliable” to mean running for a series of at least 6 hour runs with zero alignment errors
- Successful alignment of all links
- Implementation of an algorithm and successful transmission of data through it
- Verification of latency and how it compares to TDR value -in particular the SerDes link

TMT layout

MP7's used here as PP's

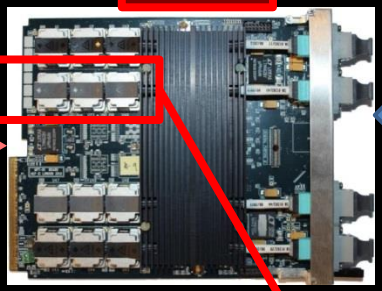
TPG input to PP not part of test

oSLB

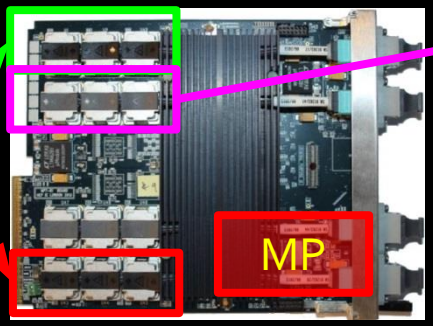
uHTR

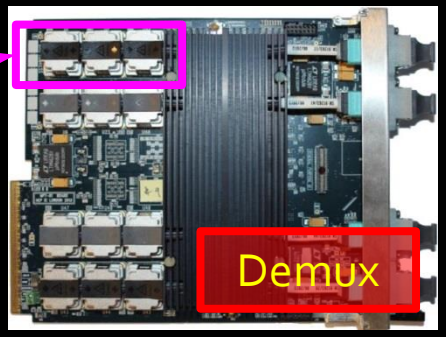
Test set-up @ 904

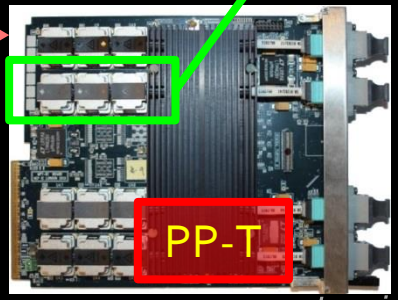
PP-B



Simulating half of the PP cards with a single MP7

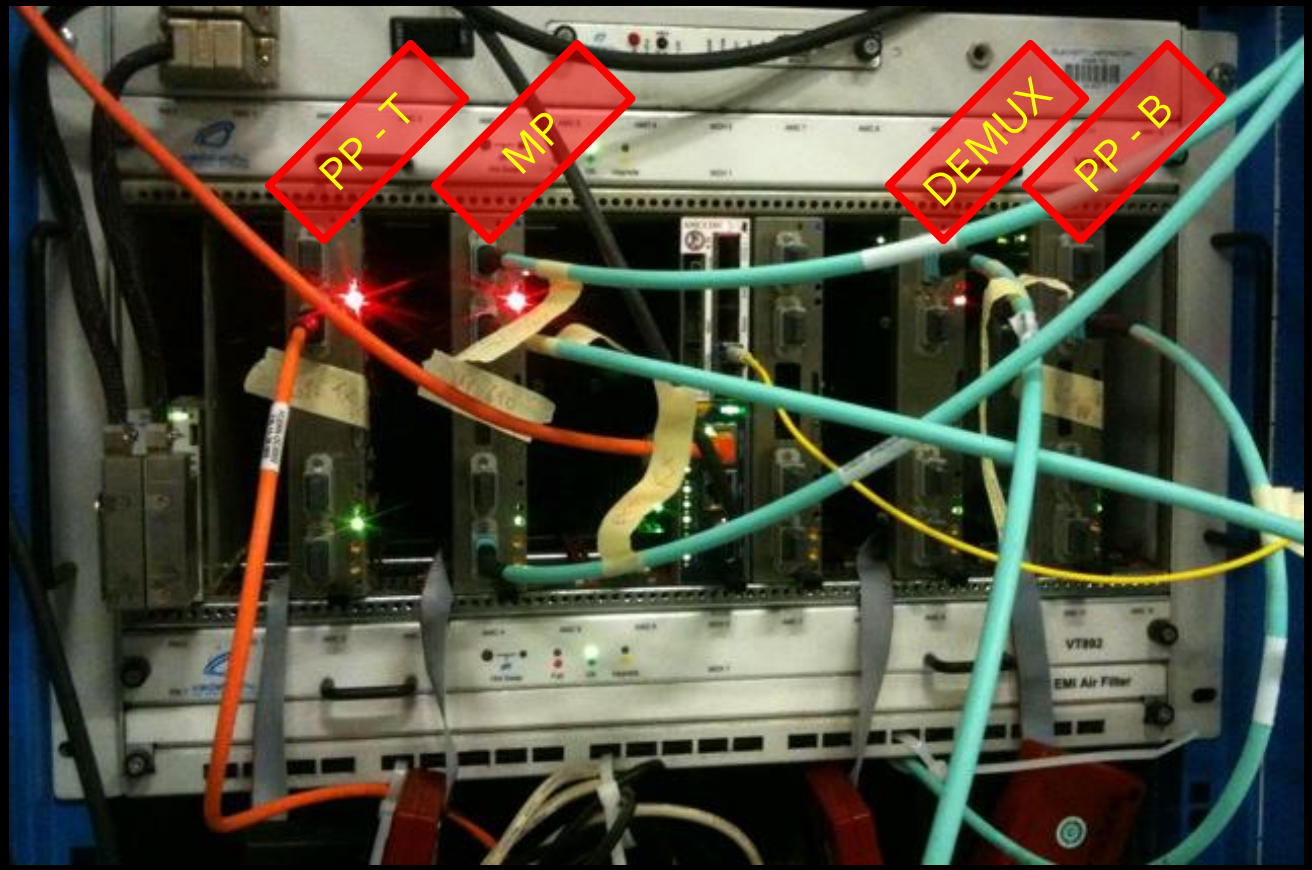






Simulating half of the PP cards with a single MP7

TMT test setup @ 904



720 Gbps of data going through the MP board
The MP is processing data from the entire calorimeter

Results

7. Test criteria:

A Pass of the TMT test requires the following objectives to be met:

- Reliable transmission of data @ 10Gbps asynch between PP and MP (36 links with full error checking) - “reliable” to mean running for a series of at least 6 hour runs with zero alignment errors
- Successful alignment of all links

The stability of the MP7 links was extensively tested several times overnight for 8 hours at a time, 72 links operating, monitoring the CRC counters and the alignment flags.

NO CRC errors
NO alignment errors

September TMT test objectives

Key aim of the September integration test:

- Implementation of an algorithm and successful transmission of data through it

Must necessarily be representative of final complexity!

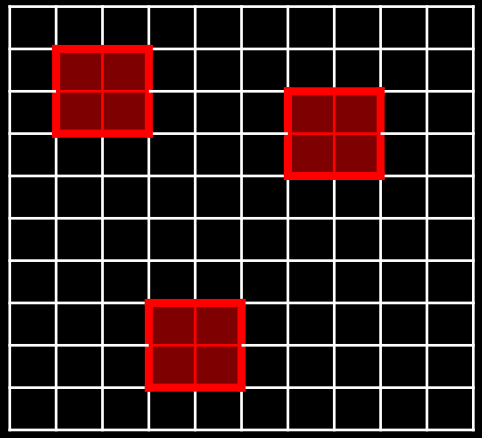
Calorimeter trigger algorithms can be broadly divided into three categories:

- Compact objects – e/γ/τ
- Extended objects – Jets
- Global objects – Ring sums

September TMT test objectives

- Compact objects – e/γ/τ
  - Use the 2×2 Wisconsin clustering algorithm
  - Baseline algorithm currently in CMSSW
- Extended objects – Jets
  - Use an 8×8 tower circular jet
  - Equivalent to cone jet (r=0.35)
  - Other algorithms available
- Global objects – Ring sums
  - Use full granularity equivalent of what is done in current trigger

TMT algorithms - Clusters

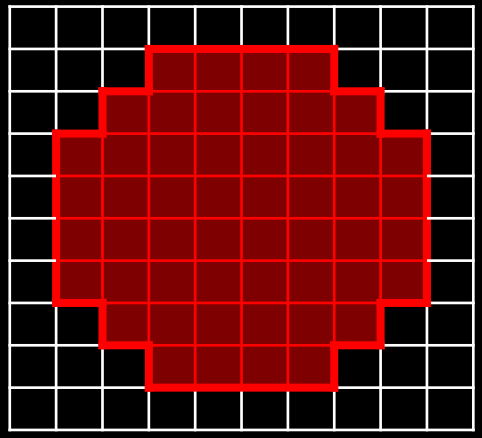


Many algorithms available, each with comprehensive test suite
Subset of algorithms were used in TMT integration tests

Algorithm	Written	Full VHDL Test-bench	Used in integration test
2x2 sum	✓	✓	✓
Cluster overlap filter	✓	✓	✗
Cluster classifier (e, γ, τ)	✓	✓	✗
Cluster isolation	partially	✗	✗
Cluster sort in ϕ	✓	✓	✓
Cluster sort in η	✓	✓	✗†

†Excluded to increase statistics for validation

TMT algorithms - Jets



Many algorithms available, each with comprehensive test suite
Subset of algorithms were used in TMT integration tests

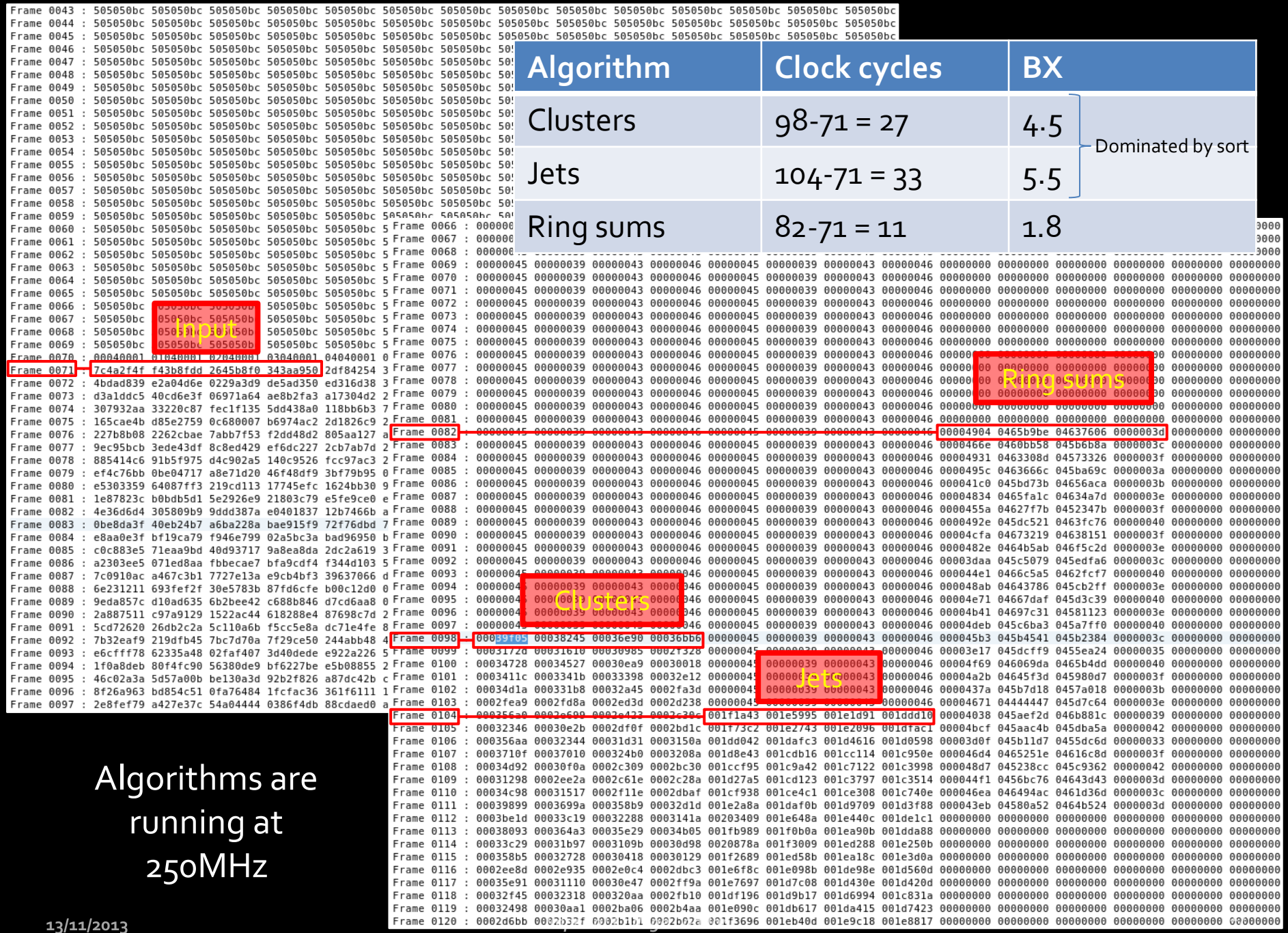
Algorithm	Written	Full VHDL Test-bench	Used in integration test
2x1, 4x1, 6x1, 8x1 strip formation	✓	✓	✓
2-, 3-, 4-, 5-, 6-, 7-, 8-strip wide sums	✓	✓	✓
• 4x4, 6x6, 8x8 square jets	✓	✓	✗
• 4x4, 6x6 circular jets	✓	✓	✗
• 8x8 circular jets	✓	✓	✓
Jet overlap filter	✗	✗	✗
Jet sort in ϕ	✓	✓	✓
Jet sort in η	✓	✓	✗†

†Excluded to increase statistics for validation

TMT algorithms - Ring sums

Many algorithms available, each with comprehensive test suite
Subset of algorithms were used in TMT integration tests

Algorithm	Written	Full VHDL Test-bench	Used in integration test
Multiply by trigonometric coefficients	✓	✓	✓
3x1, 9x1, 18x1, 36x1, 72x1 strip formation	✓	✓	✓
• Scalar sum (ET)	✓	✓	✓
• Vector sum (MET)	✓	✓	✓
• Count towers over threshold (PU estimator)	✓	✓	✓
Accumulate in η	✗	✗	✗



Algorithm	Clock cycles	BX	
Clusters	98-71 = 27	4.5	Dominated by sort
Jets	104-71 = 33	5.5	
Ring sums	82-71 = 11	1.8	

Algorithms are running at 250MHz

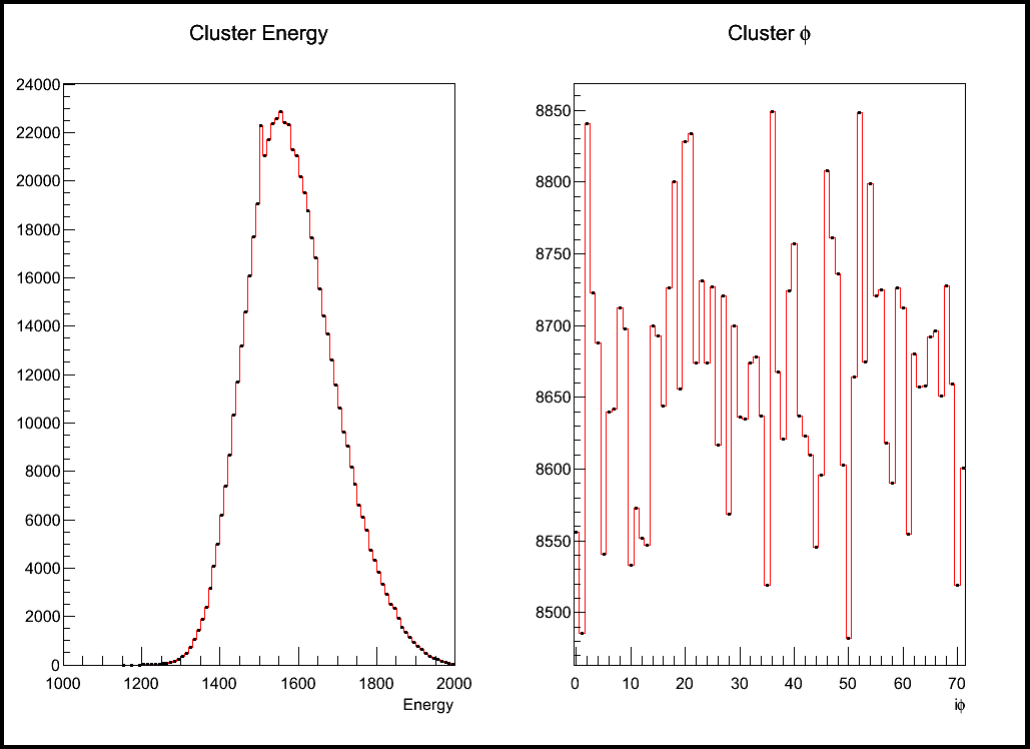
Results (1)

- Implementation of an algorithm and successful transmission of data through it
  - Random data passed through an emulator was used in the testing of the algorithms

Data injected into PP → Time-multiplexed → Optical Fibre → **Clustering algorithm (2x2)** → Sort → Capture

Compared emulated results (solid line) with those from the MP7 (markers)

C++ emulator and hardware match precisely



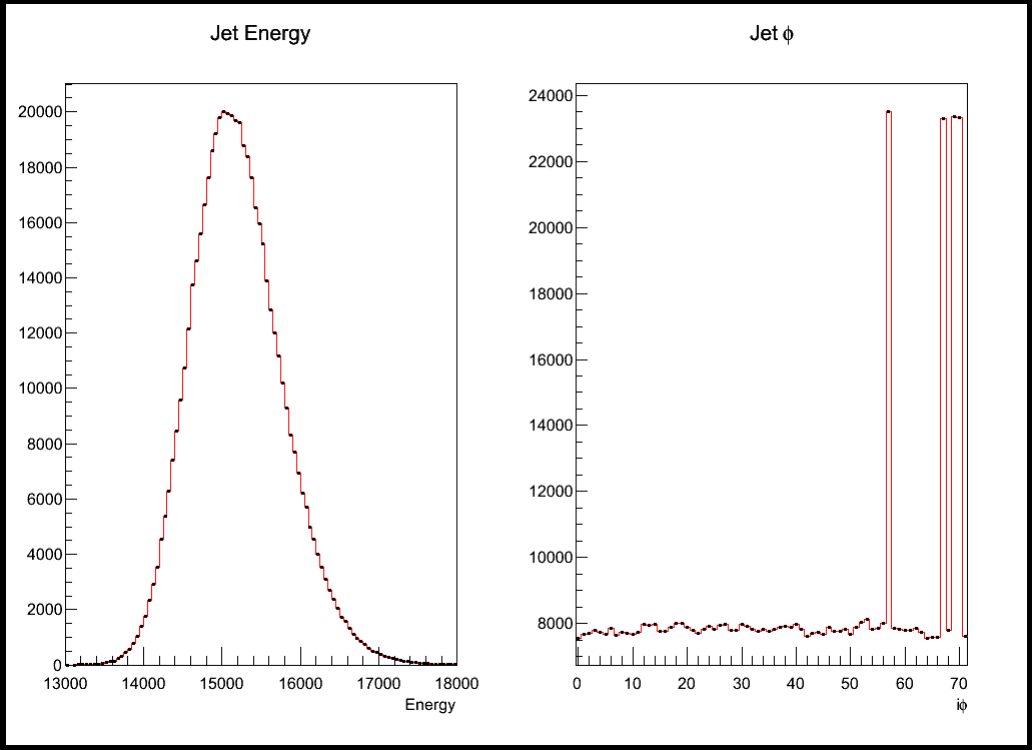
Results (2)

- Implementation of an algorithm and successful transmission of data through it
  - Random data passed through an emulator was used in the testing of the algorithms

Data injected into PP → Time-multiplexed → Optical Fibre → **Circle jet algorithm (8x8)** → Sort → Capture

Compared emulated results (solid line) with those from the MP7 (markers)

C++ emulator and hardware match precisely



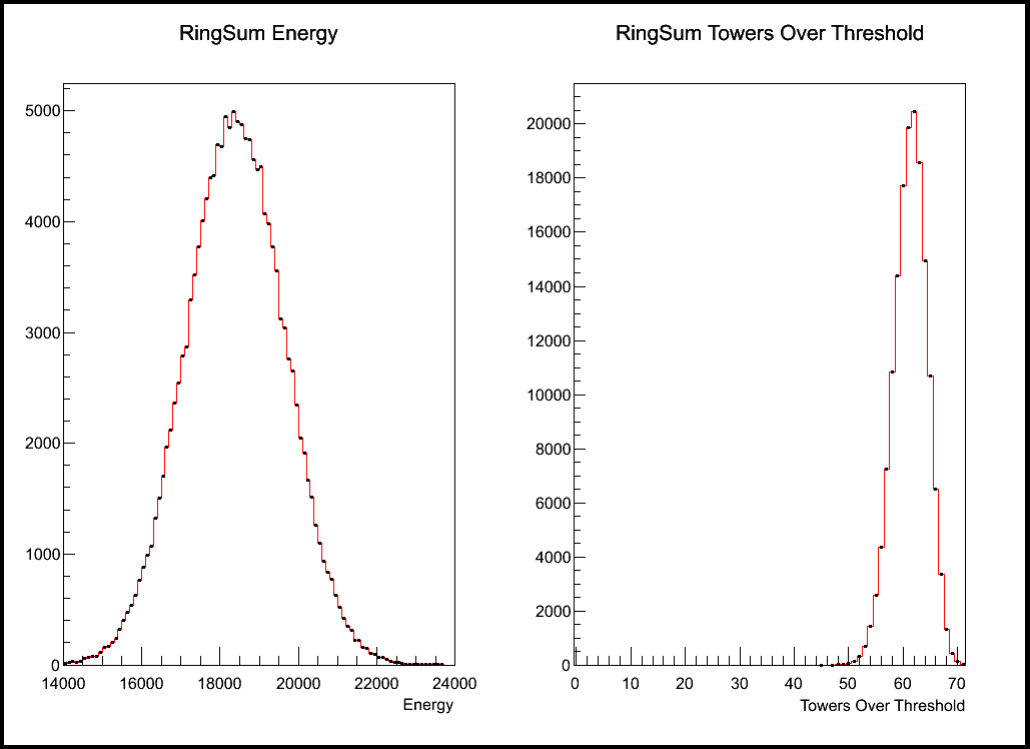
Results (3)

- Implementation of an algorithm and successful transmission of data through it
  - Random data passed through an emulator was used in the testing of the algorithms

Data injected into PP → Time-multiplexed → Optical Fibre → **Ring sums** → Sort → Capture

Compared emulated results (solid line) with those from the MP7 (markers)

C++ emulator and hardware match precisely



Results

- Implementation of an algorithm and successful transmission of data through it

TMT integration test successfully demonstrated simultaneous operation of:

- Compact algorithms (e/γ/τ)
- Extended algorithms (jets)
- Global algorithms (ring sums)

These algorithms are representative of the complexity of algorithms expected in the final system

Results – Latency Measurement

- Verification of latency and how it compares to TDR value -in particular the SerDes link

Source of Latency	BX (TDR)	BX –measured in Sept 2013
L1 processing + TM	10	7
L1/L2 SerDes (Tx+Rx) @ 10Gbps	5	5
L1/L2 SerDes Align Data	1	1
L1/L2 cable (20m)	4	4
L2 Processing	8	5.5 (clustering, jets, ring sums)
L2/GT SerDes (Tx+Rx)	5.5	5 (identical link to L1/L2 above)
L2/GT SerDes Align Data	1	1 (identical link to L1/L2 above)
L2/GT cable	0.5	0.5
De-multiplex	6	7
TOTAL	**41**	36

Lessons learned from test

- Floor-planning
  - Huge impact on algorithm design
  - Structure the algorithm to map optimally onto the FPGA
  - Reduces risk that after many hours of routing 6 million nets just 1 or 2 fail to meet timing - exceedingly annoying
  - Significant timing improvement
  - Only viable if signals remain relatively local
- Full pipelining of algorithms is essential - even relatively innocuous looking fan-outs in chips this large have the potential to kill off the entire design
- uHAL and IPbus are working well, and have made debugging and multi-user crate access both possible and easy
- AMC13 has worked extremely well for us during the test

Integration test summary

- Have demonstrated successful TMT setup @ CERN
- Pipeline tested from injecting data into PP and capturing at the MP
- Many algorithms were loaded and results were in perfect agreement with expectations
- The TMT test was very successful – can be measured by the objectives set-out before the test began:

All test criteria were met

Integration test setup: Next Steps

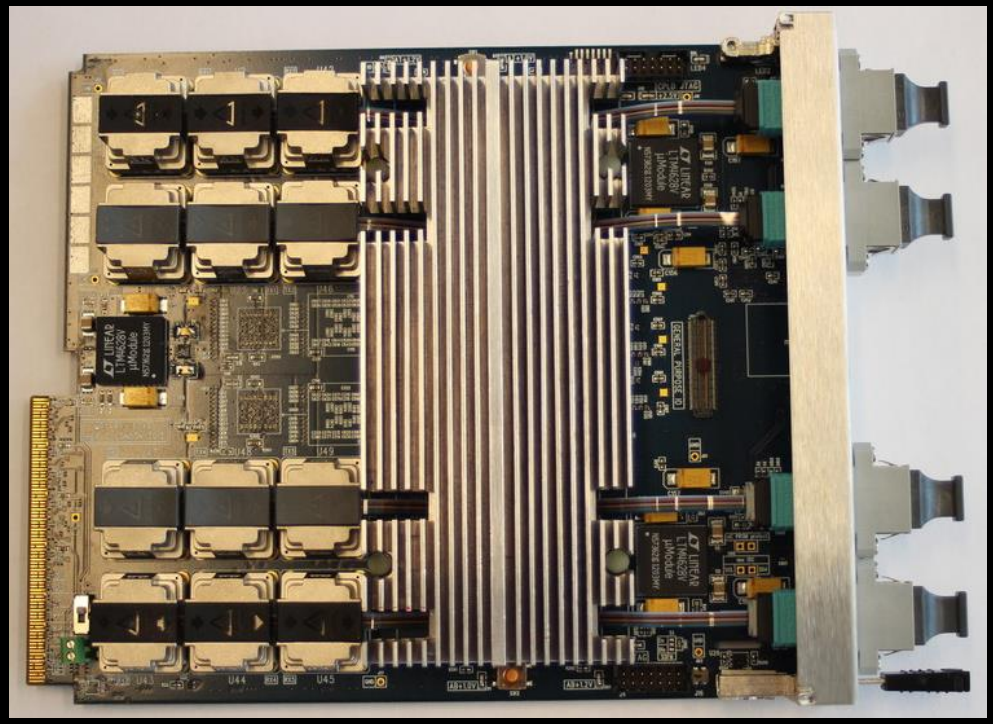
- Plan is to continue implementing and testing algorithms over the next few weeks – have a testbench, now performance and resource-usage can be measured
- Improve structuring of algorithms
- Integrate with other CMS components, i.e. DAQ via AMC13, IPMI and other µTCA infrastructure
- Make the MP7s and infrastructure firmware available to others to start working with and gaining experience
- Start putting into place 'polished' online software

Hardware:

processor card

The Master-Processor, Virtex-7 (MP7)

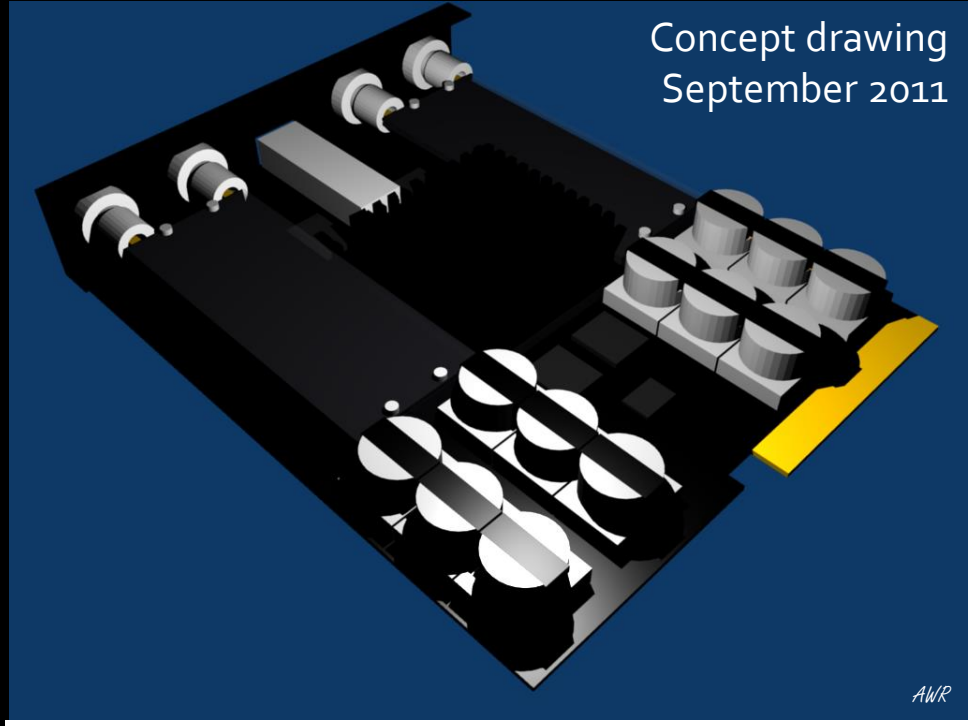
- uTCA form factor
- ~1.5Tb/s signal processor
- Latest-generation Xilinx Virtex-7 FPGA technology
- GbE, AMC13/TTC/TTS, PCIe, SAS, SATA, SRIO
- Advanced boot-loader & diagnostics (full system test at start-up)
- On-board firmware repository
- Pin-compatible FPGAs allow cost-performance balance
- 2×144Mbit 550MHz QDR RAM (optional)
- USB-OTG serial-debug console

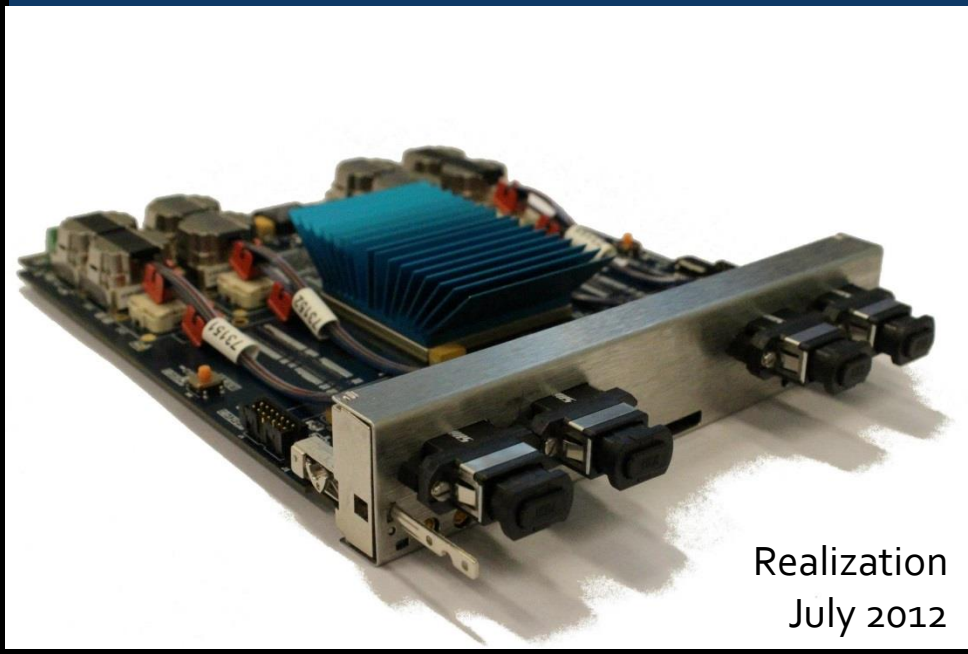


XC7VX690T, 72 TX + 72 RX @ 10Gb/s

History

- Summer 2011 – started considering successor to the Mini-T5
- November 2011 – schematics started (before Virtex-7 or MiniPODs were available!)
- June 2012 – first manufacturing run
- Autumn 2012 to Summer 2013 – extensive testing, several further manufacturing runs
- June 2013 – submit a first revision of the board prior to production runs
- August 2013 – first revision boards now in hand and under test





Current Hardware in Hand

- 2 revision-0 cards with 48 links (XC7VX485T) engineering silicon
- 3 revision-0 cards with 48 links (XC7VX485T) production silicon
- 3 revision-0 cards with 72 links (XC7VX690T) engineering silicon
- 1 revision-1 cards with 48 links (XC7VX485T) production silicon
- 5 revision-1 cards with 72 links (XC7VX690T) production silicon

---

14 cards in-hand†

† 1 at Imperial College, UK
1 at RAL, UK
1 at Berkeley, USA
5 at CERN B904
3 at CERN Meyrin under final validation
2 at CERN Meyrin under test
1 at CERN Meyrin in display case

Hardware:
Standalone Testing

Working at the cutting edge

As noted previously, the board was designed before engineering silicon was even available

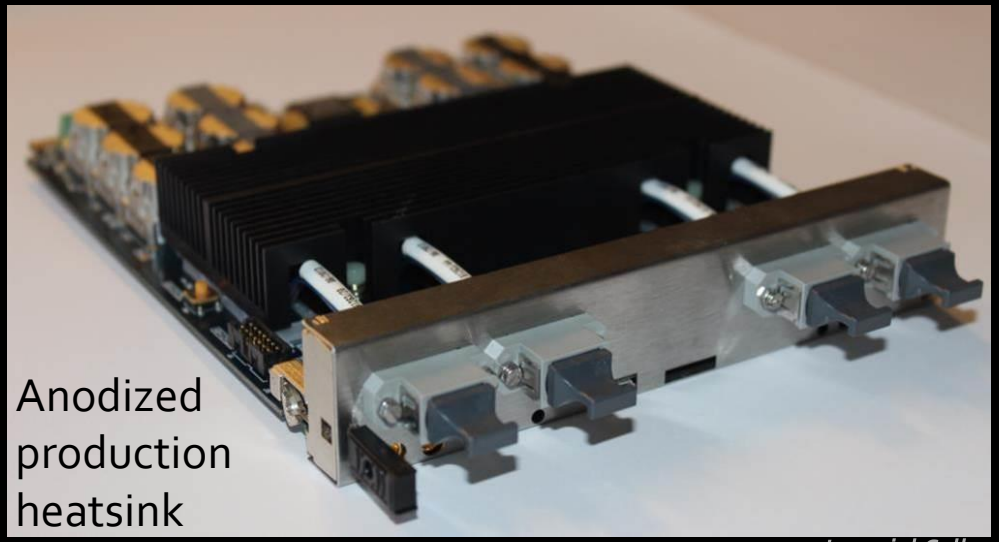
A lot of the work to understand the board involved direct contact with the Xilinx silicon engineers. This has included alerting them to errors in the datasheets. **It turns out that exactly following the datasheet is no substitute for hands-on experience**.

A lot of things changed between the original FPGA specification documents and the production silicon

Working at the cutting edge (ii)

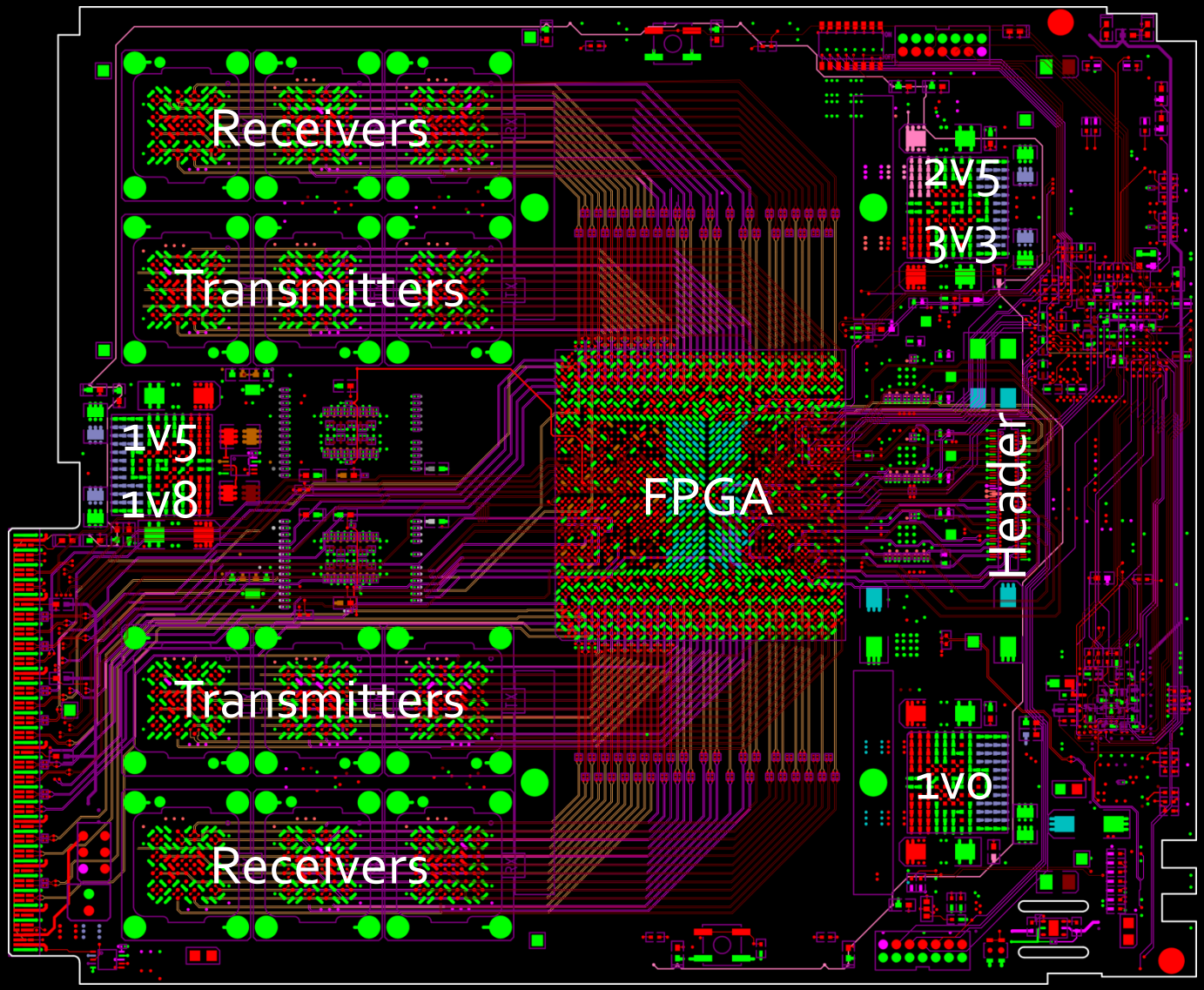
- In particular, power consumption and thermal dissipation were far higher than Xilinx original estimate
- These are now both well understood and controlled but it took time to understand these issues

Custom heatsink dissipates 40% more energy than off-the-shelf part

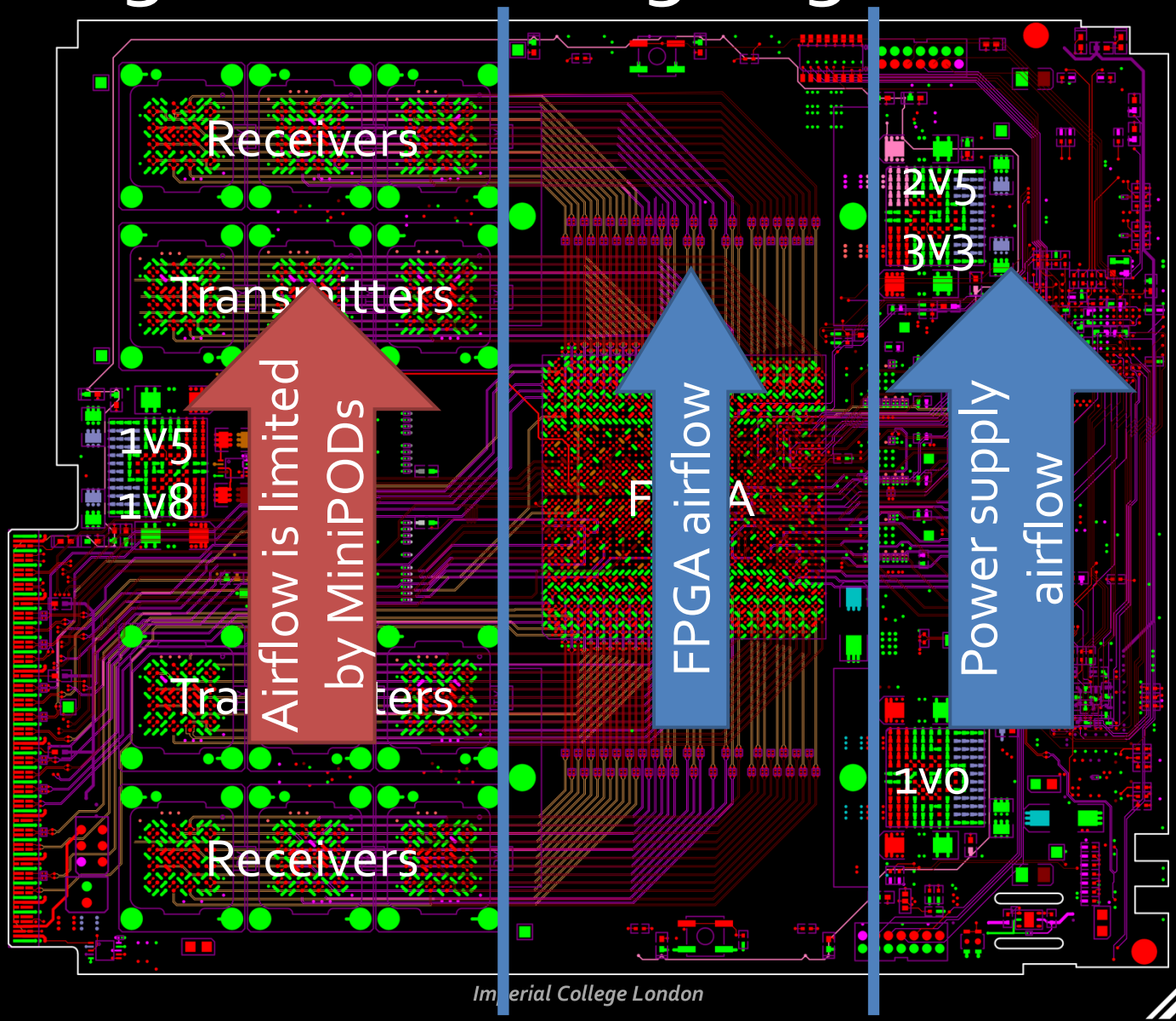


Anodized production heatsink

Working at the cutting edge (iii)



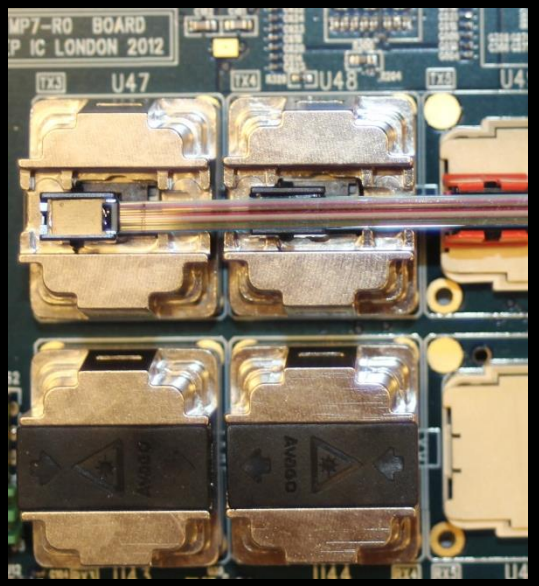
Working at the cutting edge (iv)

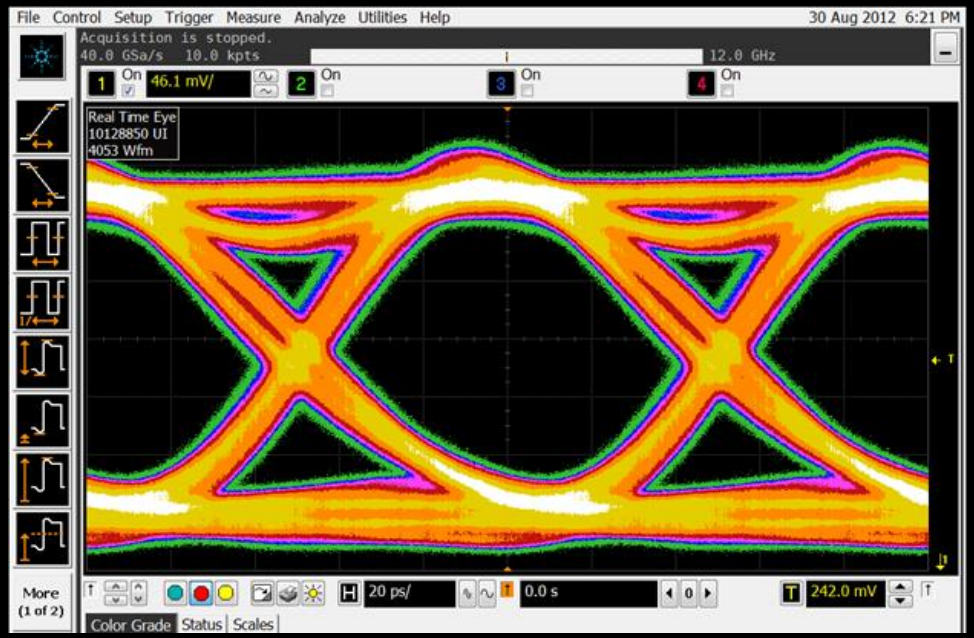


Optical link performance

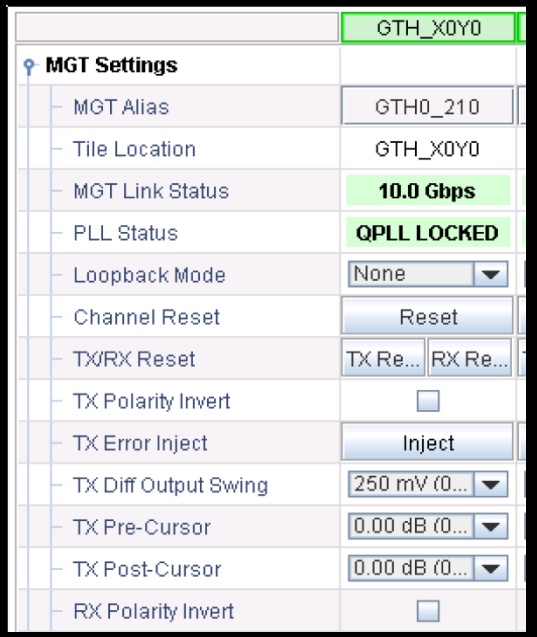
Optical links worked perfectly out-of-the-box

- MiniPODs are using default pre-emphasis (minimal)
- TX differential swing is minimal
- No pre-emphasis/de-emphasis in MGTs



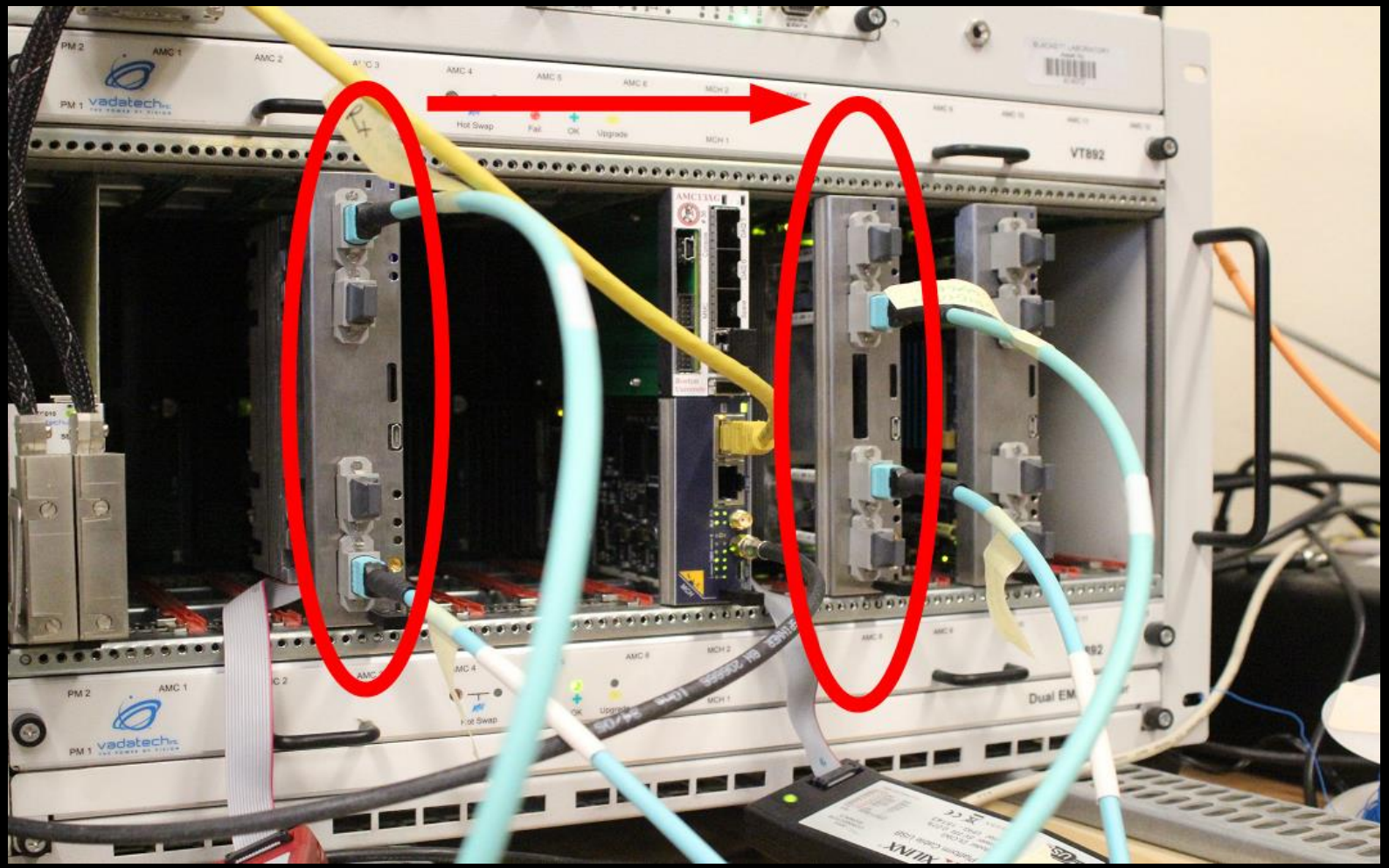


Optical eye @ 10Gb/s



Link validation

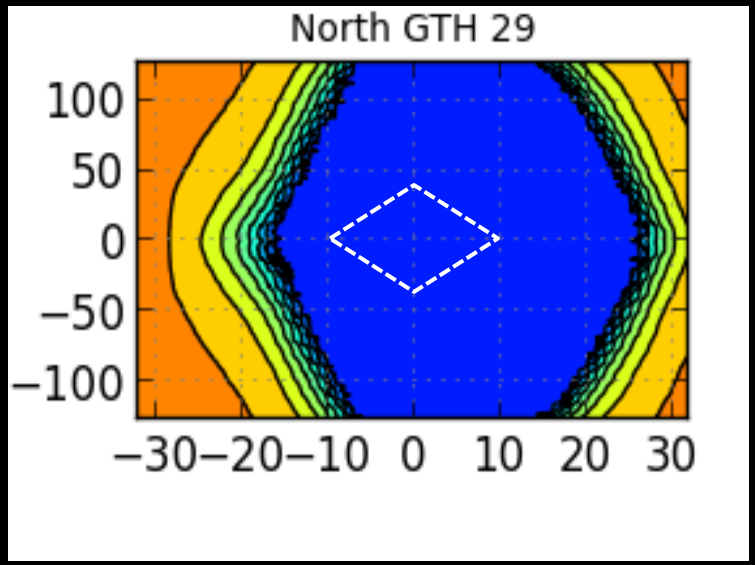
Links are validated between boards rather than in loopback – **a more rigorous test**

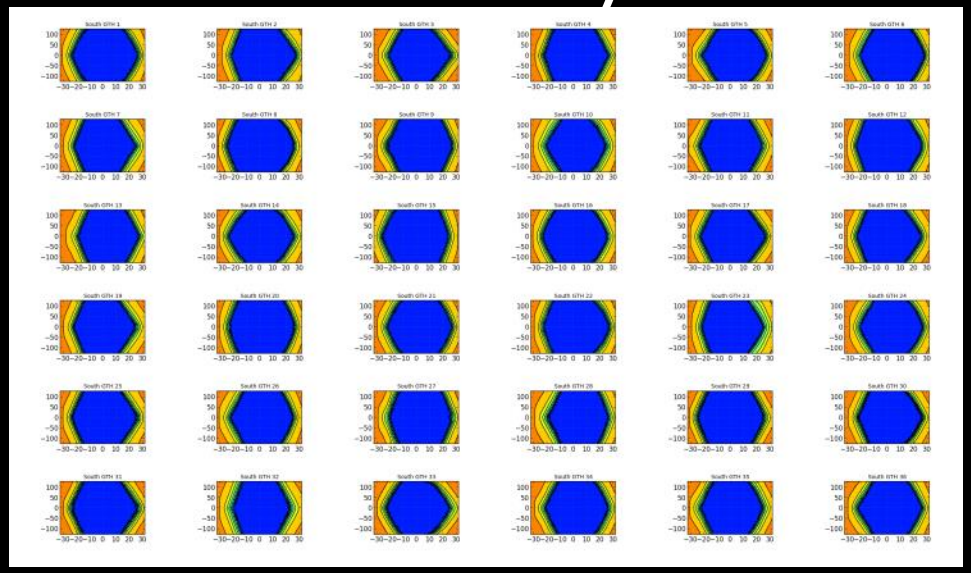


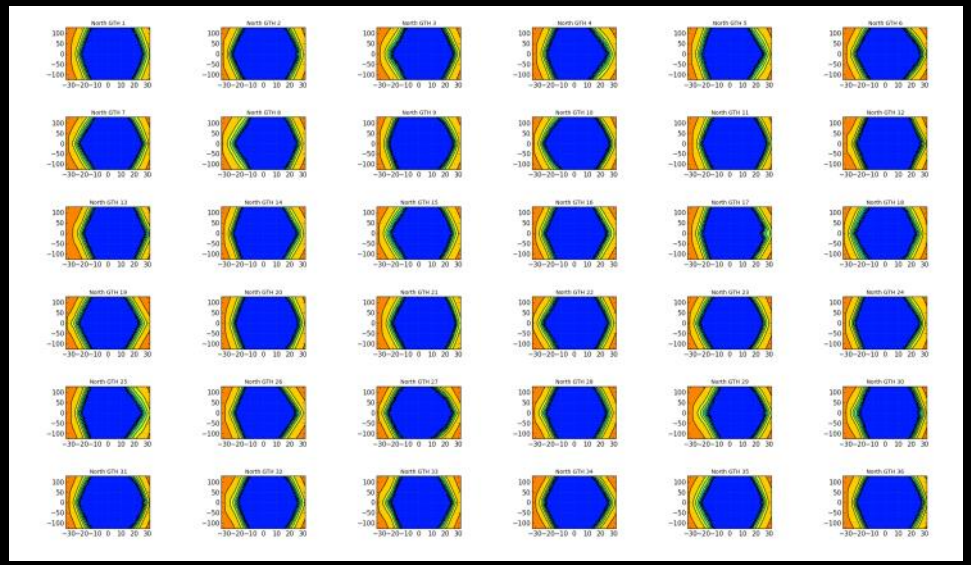
72 @ 10Gb/s → 62.2Pb/day → ~1Eb every 2 weeks

72 links validated simultaneously

- Eye-diagrams measured inside XC7VX690T FPGA
- All 72 links running PRBS7 at 10Gb/s, LPM

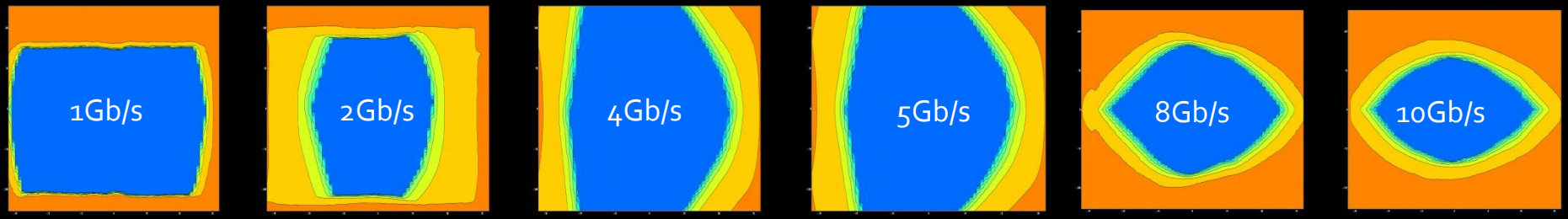




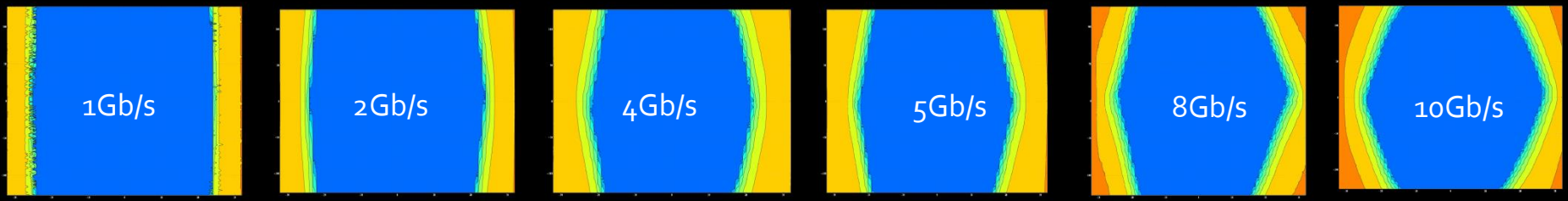


Link validation

XC7VX485T – GTX transceivers



XC7VX690T – GTH transceivers



- Various line rates validated
- Eye-diagrams for all line-rates meet industry standards
- MGT configuration **done at runtime, not build-time**, giving significantly greater flexibility and control

Link validation

- LHC-synchronous board-board communication has been demonstrated at 6.4Gb/s
- Both boards received the TTC clock over the backplane from the AMC-13
- **The MP7 has been demonstrated to work both SYNCHRONOUSLY and ASYNCHRONOUSLY, whichever way the CMS trigger decides to go**

Clocking

- The clock architecture and clocking resources of the Virtex-7 are very different from previous generations
- Several months of work has gone into understanding the configuration-options, the performance and the limitations of each of these clocking resources **so that there are no nasty surprises in future**
- This was one area with many "undocumented" features which required direct dialog with Xilinx
- We are now confident that this is thoroughly understood

Other tests

All the auxiliary subsystems on the MP7 have also been validated:

- Mezzanine I/O
- QDR-II+ RAM
- Board communication (Ethernet)
- USB 2.0 OTG, IPMI, SD card repository (microcontroller)
- SPI PROM (protected bootloader)
- Thermal dissipation, humidity & temperature monitoring
- Power consumption, phasing & monitoring

I/O fan-out mezzanine for debugging
30 differential pairs to/from the FPGA
3v3, 2v5 and 1v8 supplies
Dedicated I2C lines to the microcontroller

Hardware:
MP7 Revision 1

List of changes on R1 card

- Swap LTM4628 power module for LTM4620 (higher current rating, footprint compatible)
- Swap LTM4606 power module for LTM4601 (higher current rating, not low EMI part, different footprints)
- Add potential divider on one P/I/V/T monitor
- Invert polarity of enable line on an oscillator
- Change the value of resistors to make tri-colour LEDs glow white, not purple
- Add four extra bulk decoupling caps

Testing of the R1 cards

- 1 board already in use in 904
- 3 boards undergoing final validation (links already tested)
- 2 boards partially tested

Note that both R1 cards have been assembled with production silicon:

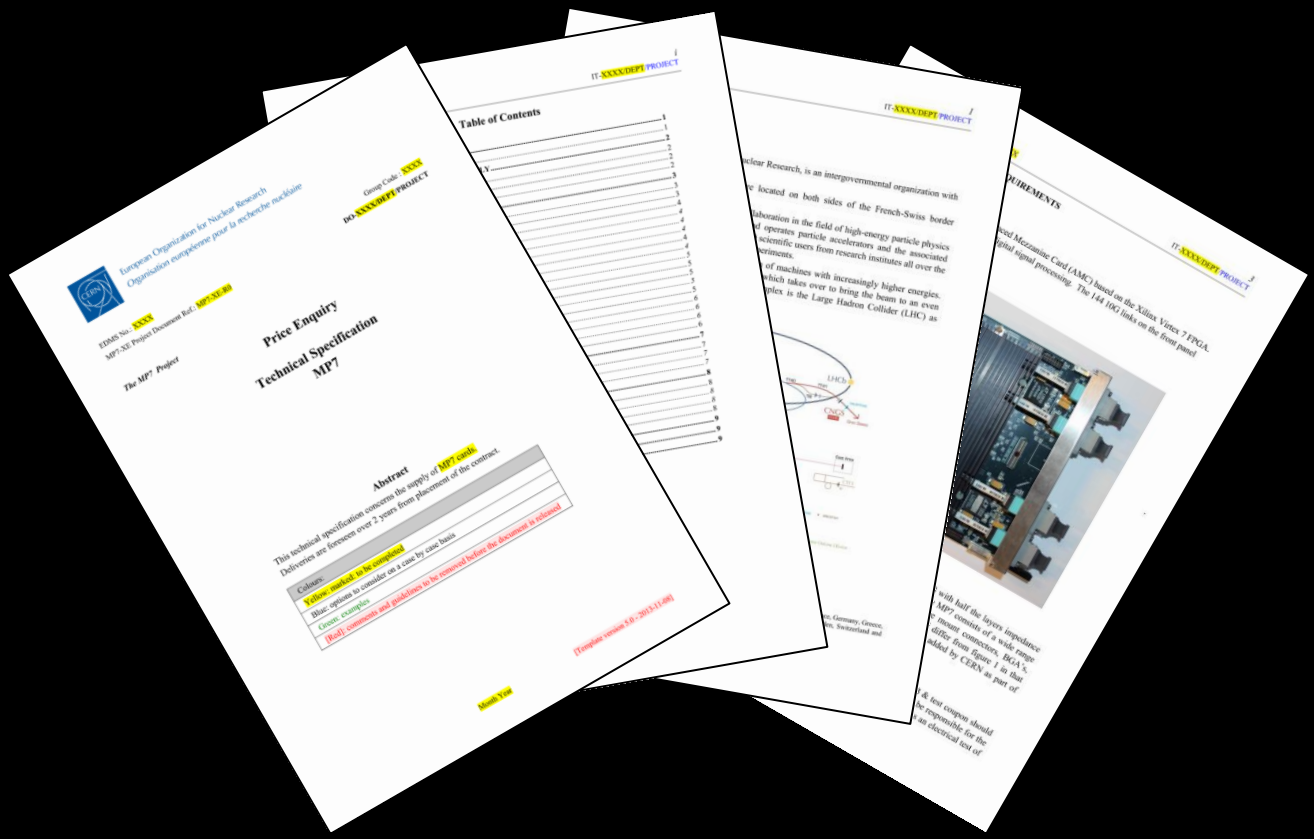
These are the FINAL FPGAs on the FINAL board design

Hardware:
Planning and Production

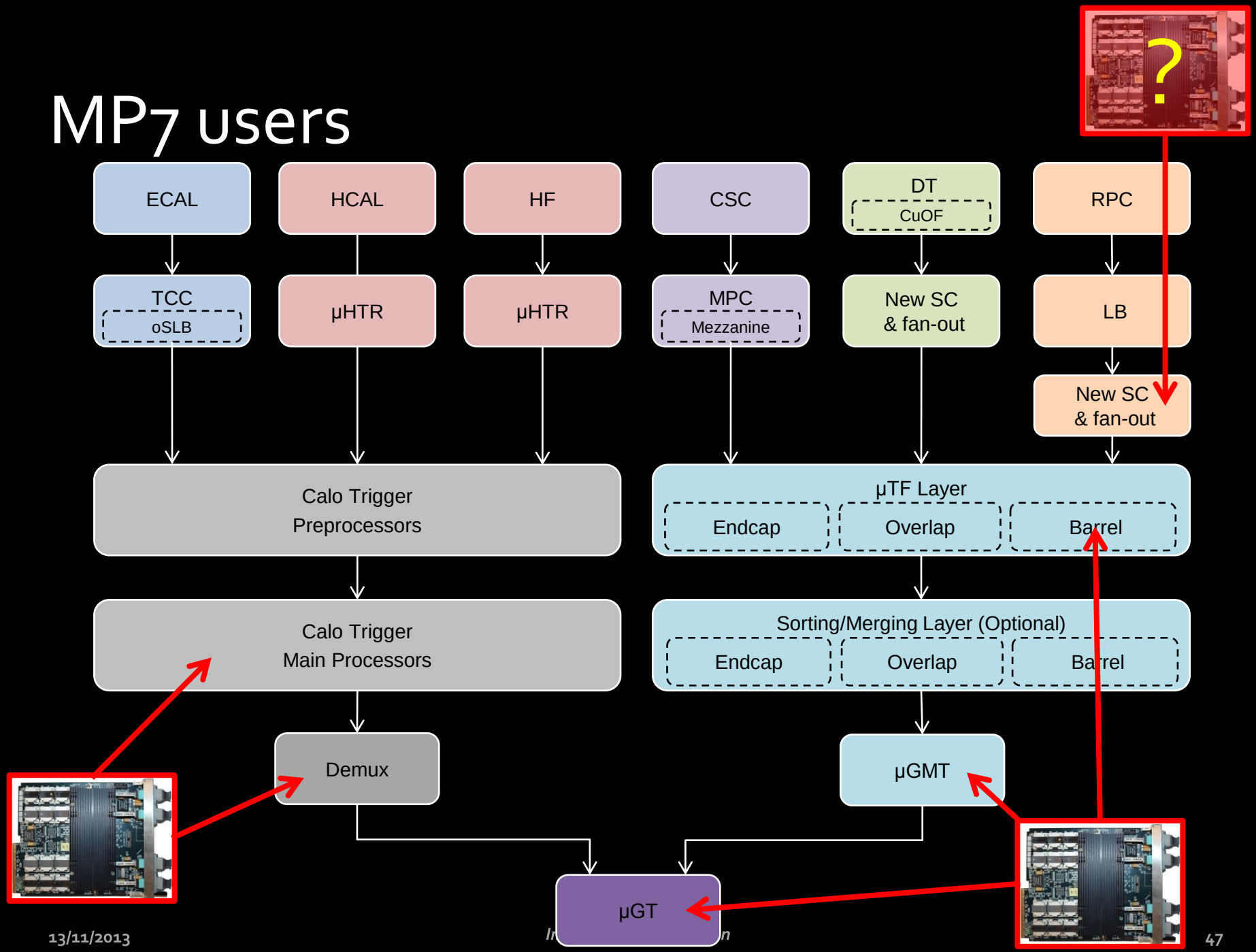
Production and Planning

A production specification and manufacturing contract document has been drawn up based on a CERN template

Been in discussion with CERN purchasing



MP7 users


?
ECAL
HCAL
HF
CSC
DT
CuOF
RPC
TCC
oSLB
µHTR
µHTR
MPC
Mezzanine
New SC
& fan-out
LB
New SC
& fan-out
Calo Trigger
Preprocessors
µTF Layer
Endcap
Overlap
Barrel
Calo Trigger
Main Processors
Sorting/Merging Layer (Optional)
Endcap
Overlap
Barrel
Demux
µGMT
µGT

Documentation

Memorandum of Understanding has been drafted specifying what will be provided and supported when a user purchases an MP7 card, in terms of

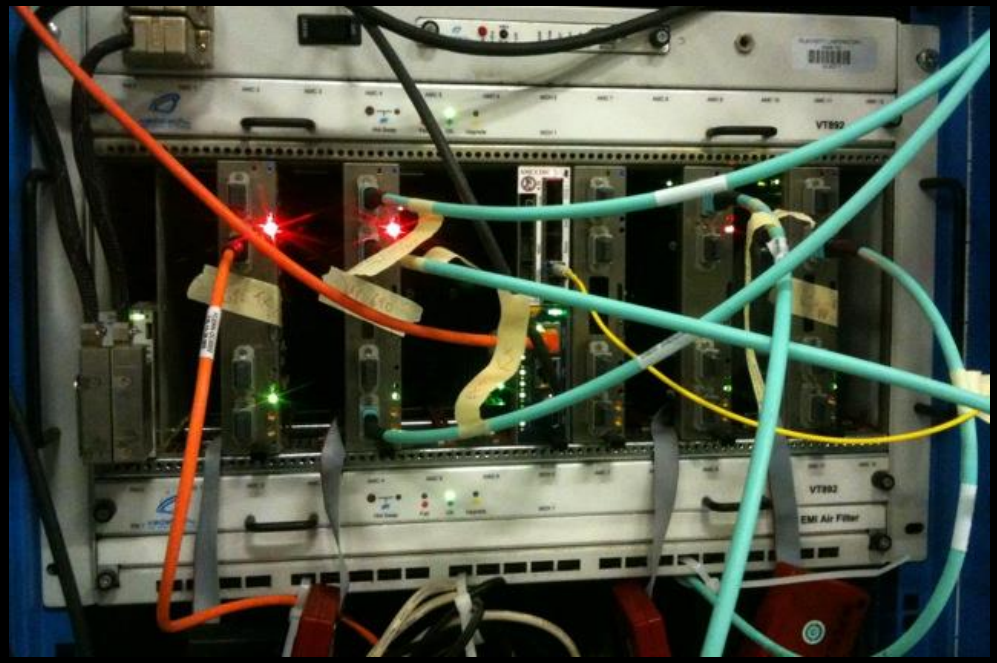
- Hardware
- Firmware
- Software

Detailed documentation on the specification and design of the board exists

Testing, servicing and maintenance documents still to be done

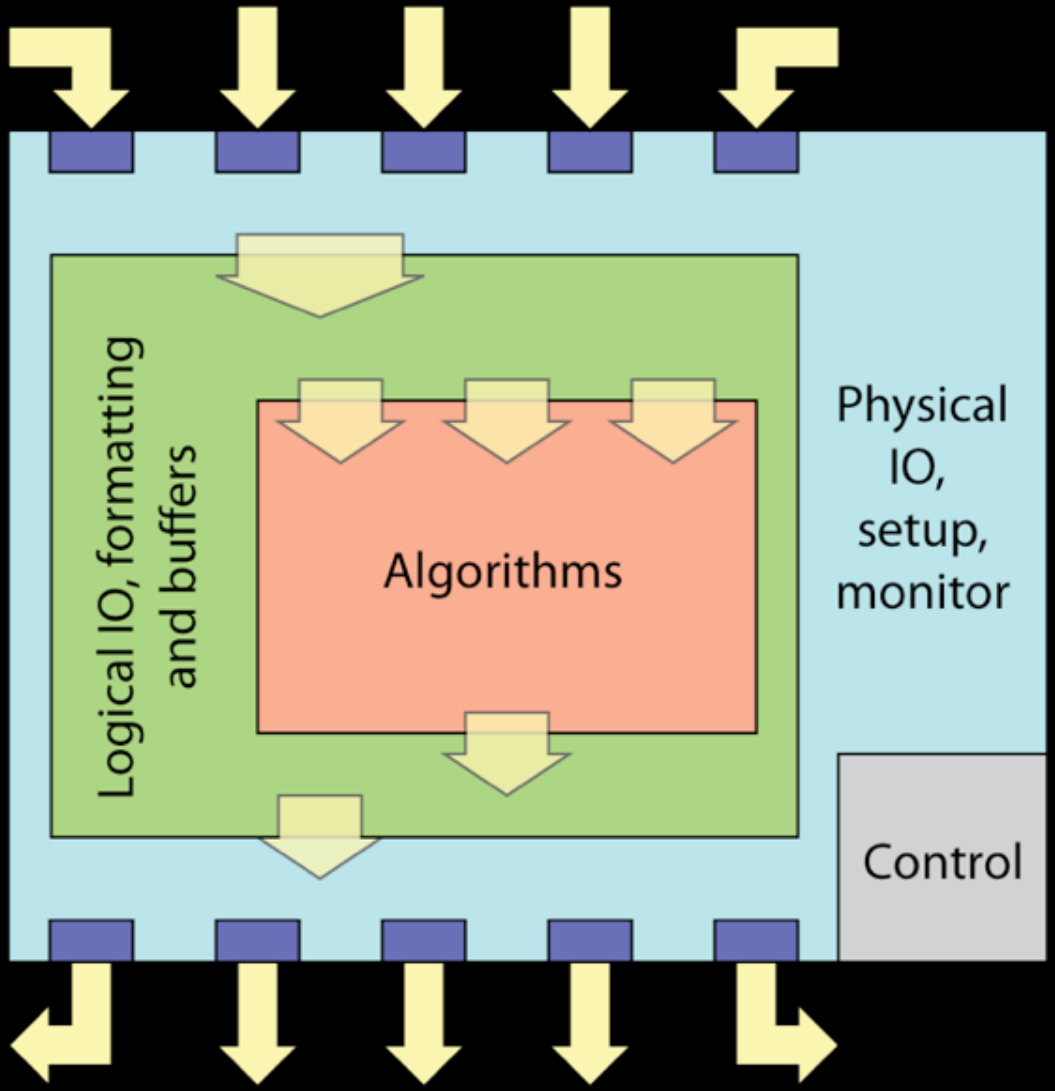
MP7 timeshare

The MP7 cards in CERN building 904 (those used in TMT integration test) are currently available on a "timeshare" basis for people who plan to use the MP7 to gain experience.



Firmware

“Base Firmware” Concept



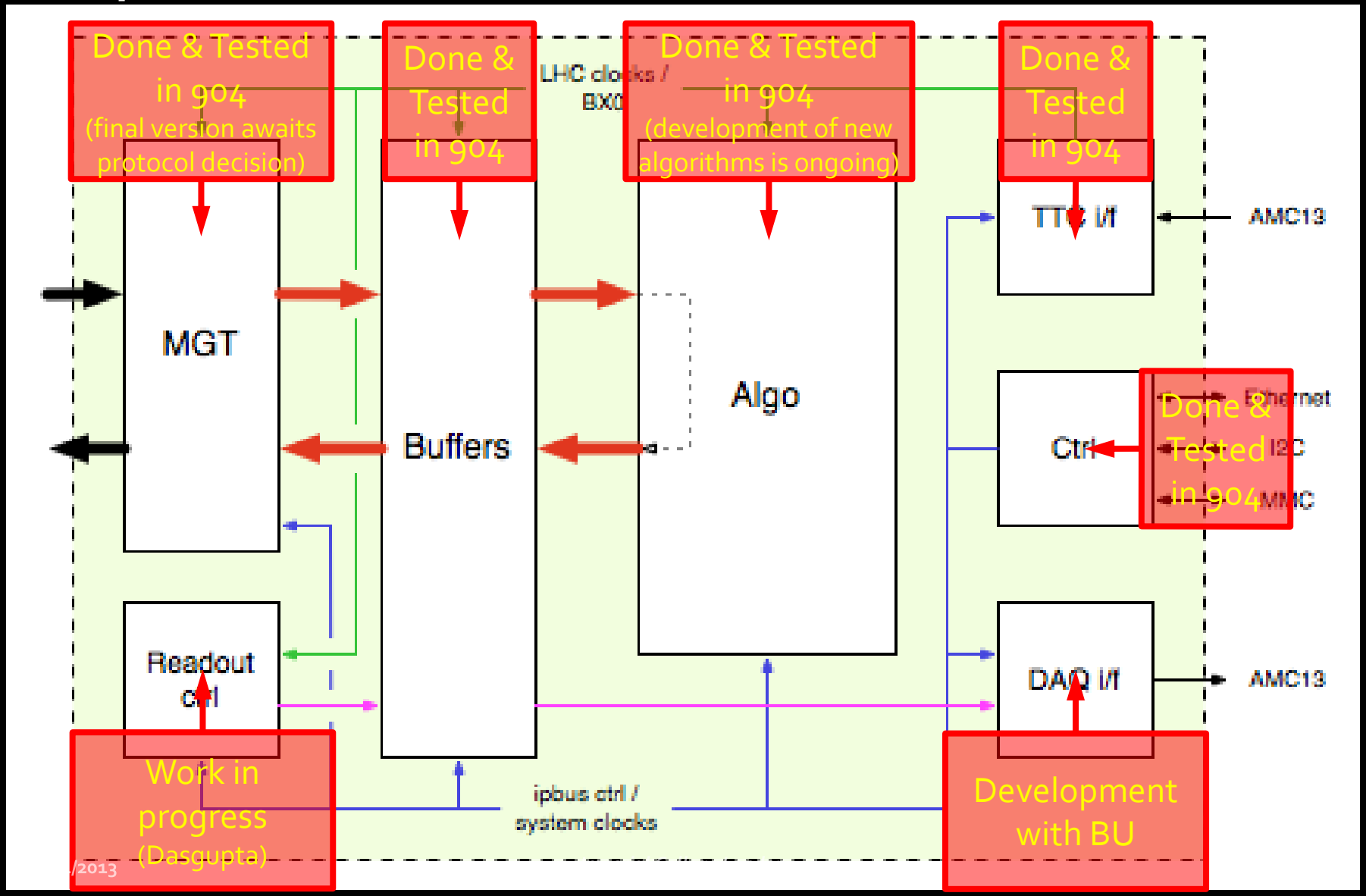
Trigger emulator
Open Development

System setup and test
Common across trigger

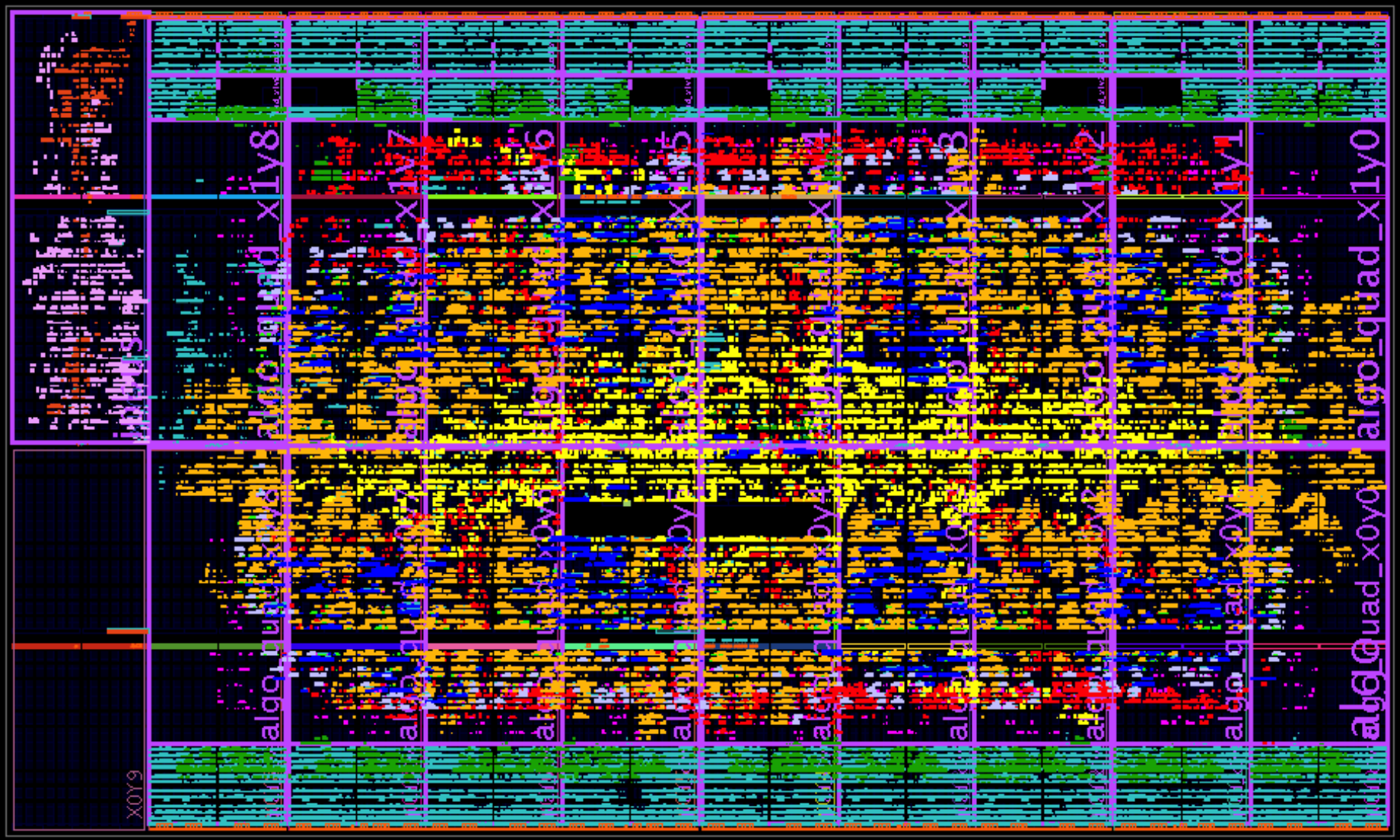
Low-level control
Hardware-specific development

uTCA infrastructure
CMS common standard

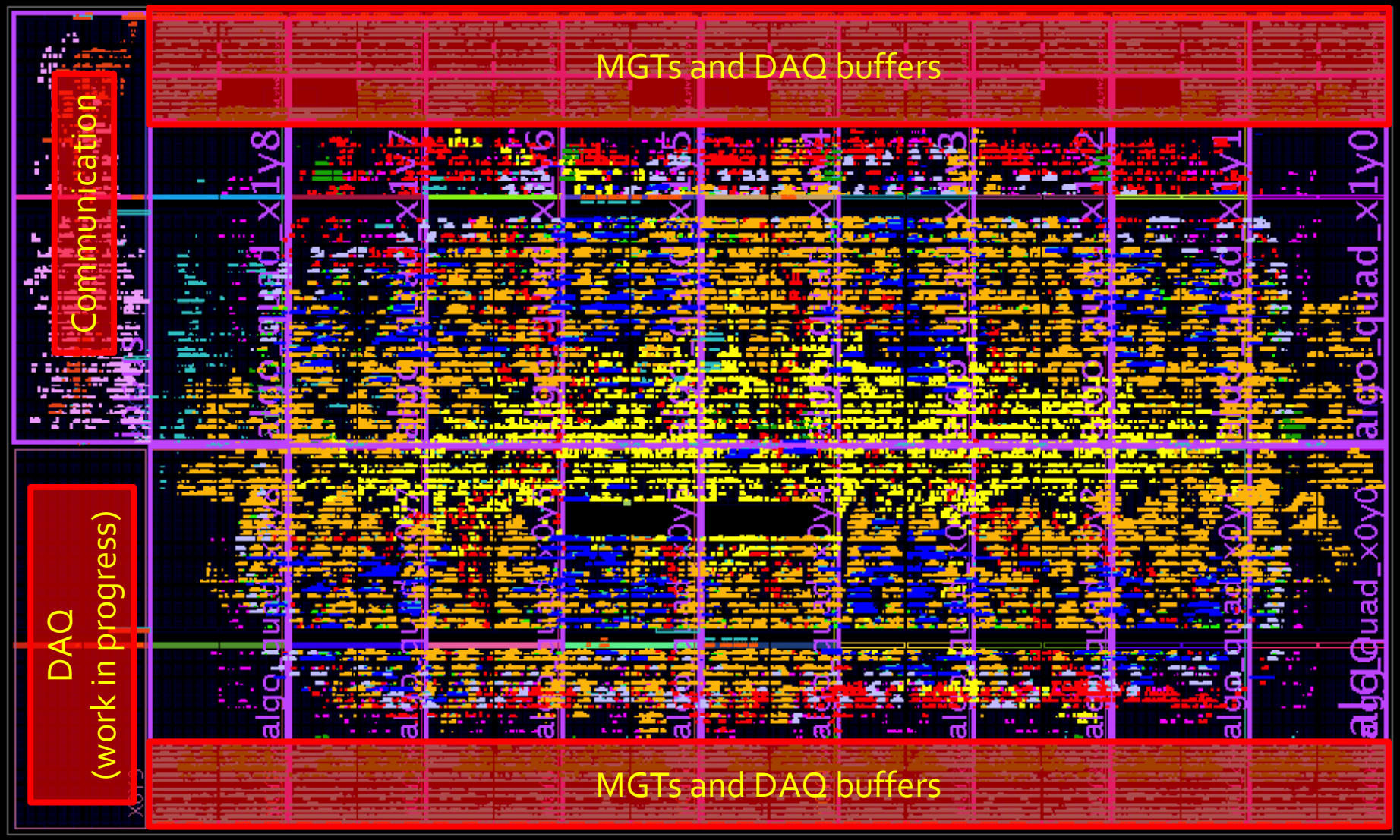
Implementation Status



Floorplan of FPGA: Integration Test



Floorplan of FPGA



Resource usage of FPGA

Resource	Fraction of Entire FPGA		Fraction of Algorithm Area used
	Used for infrastructure	Used for algorithm + infrastructure	
Registers	9%	21%	20%
LUTs	19%	36%	35%
DSPs	0%	8%	13%
BRAM	12%	12%	0%

All Algorithms and Infrastructure:

7 hour build-time

Much better than the >24 hours reported elsewhere

Some Firmware Notes

- All MP7 firmware is in the official CMS CACTUS repository
  - http://svnweb.cern.ch/reps/cactus/trunk/boards/mp7/base_fw
  - Around 50k lines of HDL – requires serious code management now
  - The source is available for re-use by other projects
  - Scripted flow allows bitfile to be built 'out of the box'
- Collaboration on firmware has been a positive experience
  - Re-use of HCAL TTC blocks, debugging & development of IPbus/UDP
- Algorithm development – looking ahead
  - Developing a UK / LLR proposal for *fully modular* algorithm firmware
    - Automatically ensures firmware-emulator bit-level consistency
    - Uniform interface to algorithm sub-blocks, with flexible dataflow
    - Data insertion / capture at any internal connection between blocks
  - Reminder: algorithm development and tuning is a shared effort across several institutes

Software

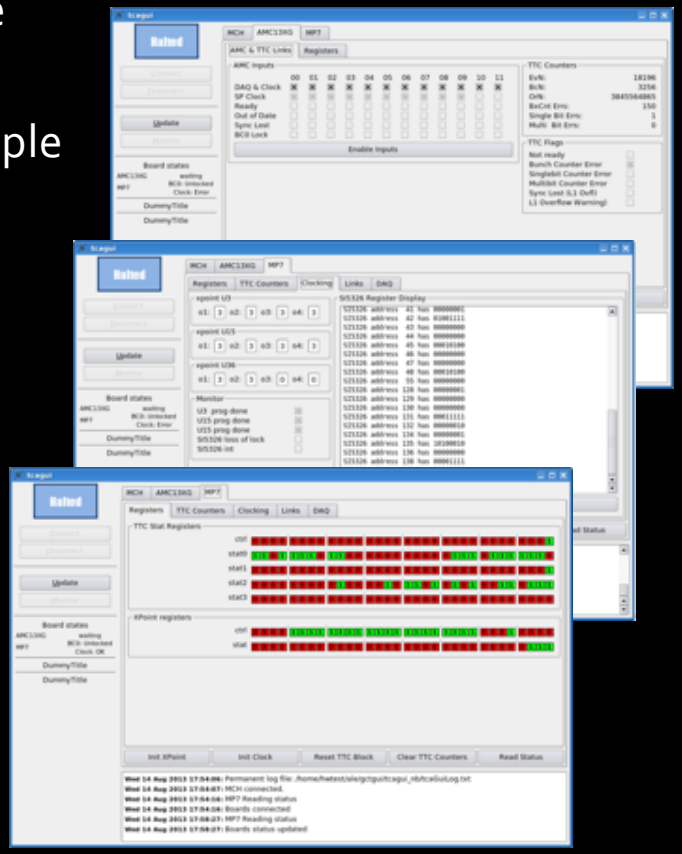
Software

- The MP7 has been built around the official CMS IPbus release
- The control software for the board is fully based on the official CMS uHAL framework, **as required by the Level-1 Trigger Online Software specification** currently under peer-review
- A set of core software modules exist to control key firmware components of the MP7 and to control peripheral components.
- These components are fully reusable and are currently being added to the official CMS trigger-upgrade SVN (CACTUS) repository

- **This software has been being used, tested and developed for over a year now!**
  - Used in the July Integration Test
  - Used in the September Integration Test

Software details

- MP7 firmware and software components tested and validated:
  - X-points, Clocking, TTC interface, Transceivers, Spy buffers
- Additional µTCA control and configuration software developed for the July Integration test
- A basic graphical frontend providing access to multiple
  - MP7 boards via IPbus & IPMI
- AMC13 frontend based on the AMC13Tool: TTC clock config, L1A and BGos monitoring
- IPMI interface
  - Based on the the IPMITool package
  - Power management, board discovery, sensor monitoring



System-level integration

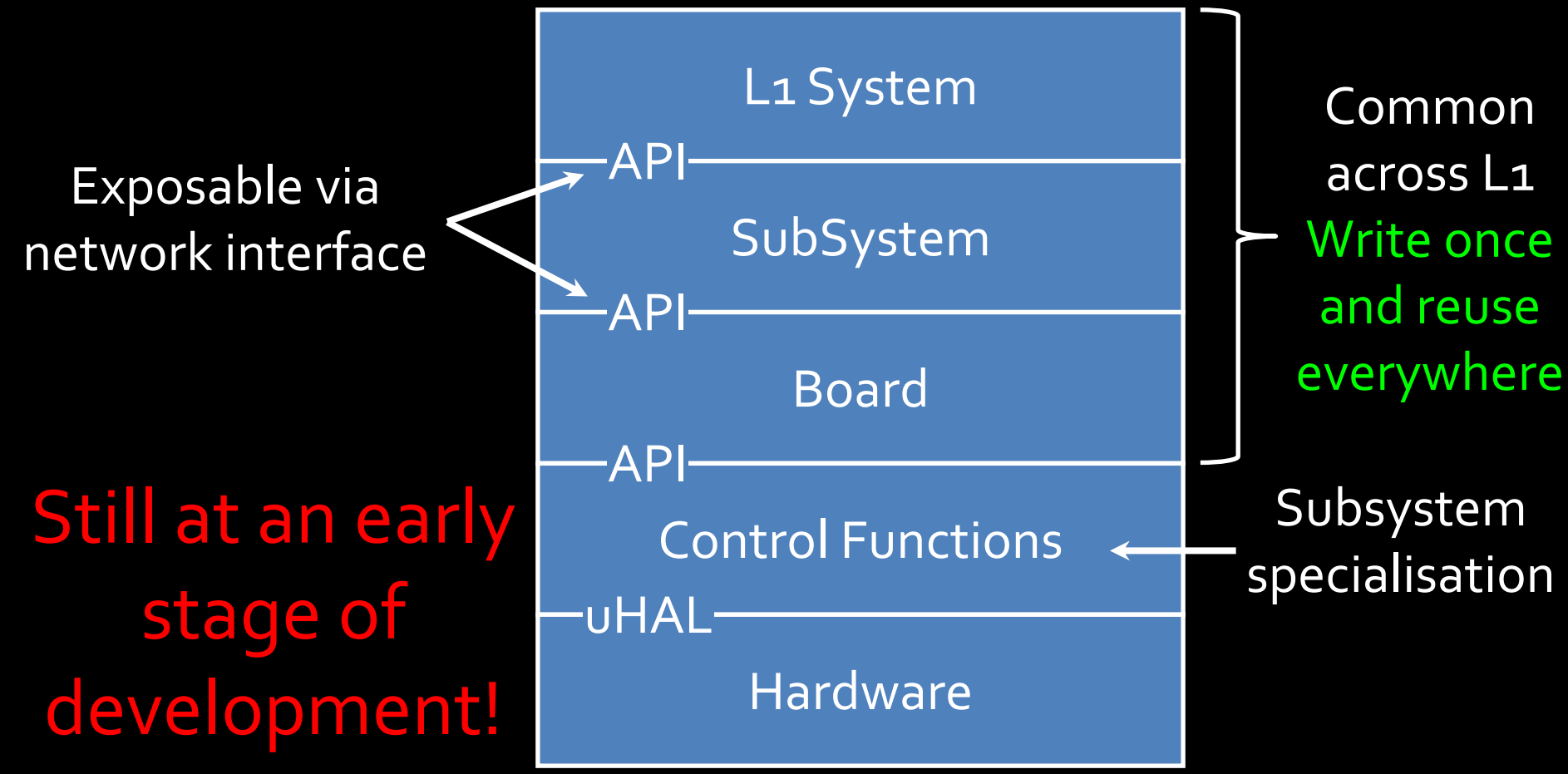
General observation:

The level-1 trigger cannot afford the effort required to repeat legacy online system development

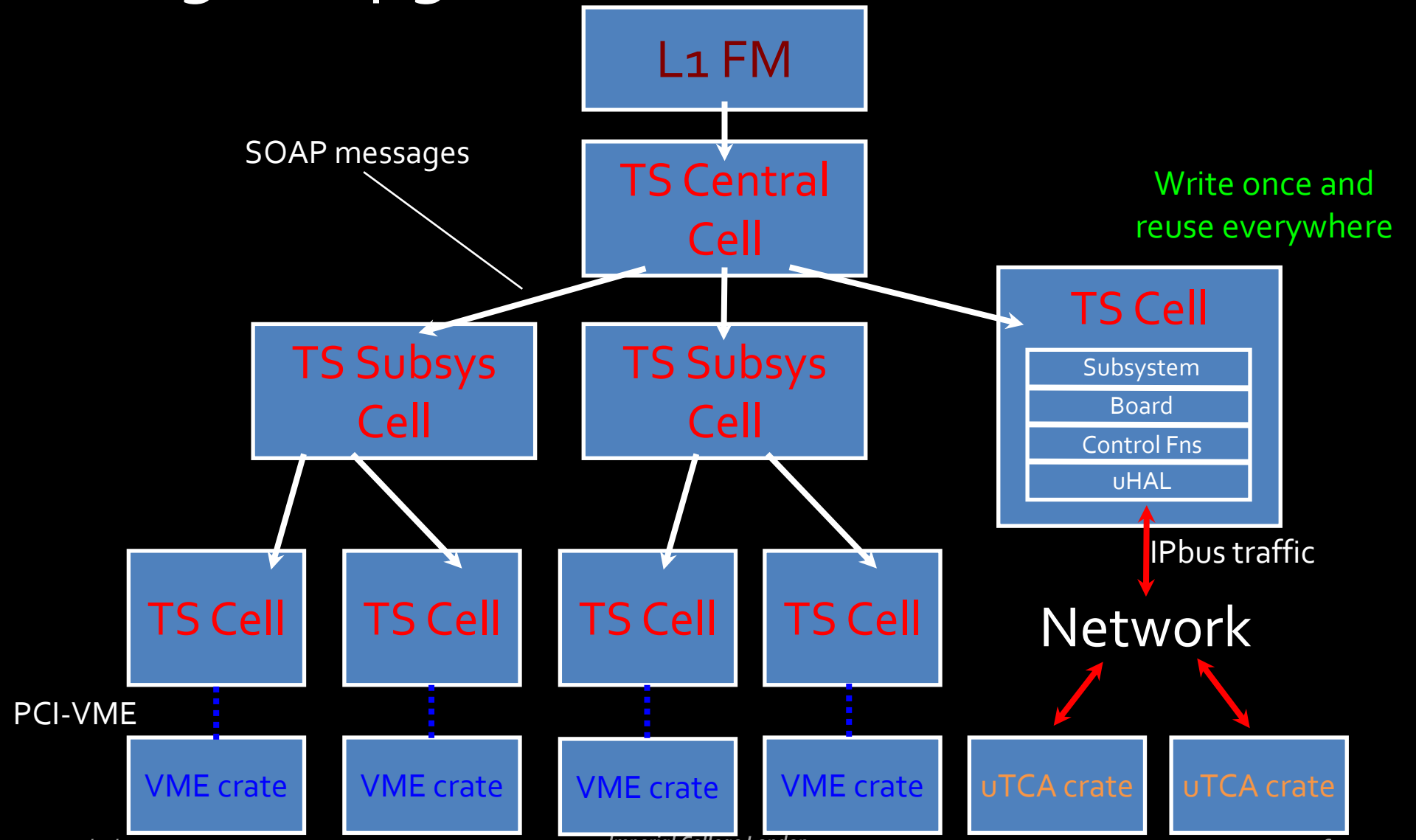
Calo layer-2 group held a kick-off meeting on how to tackle this, which was followed up with a meeting with representatives of other subsystems and then presented to the L1-trigger community as a whole

The Basic Idea

Make maximum use of the flexibility offered by µTCA, IPbus and uHAL!



Staged Upgrade



Software conclusions

We are making maximum use of the advanced position of the Layer-2 hardware, firmware and low-level software to start attacking the questions of system-level integration which will affect everyone

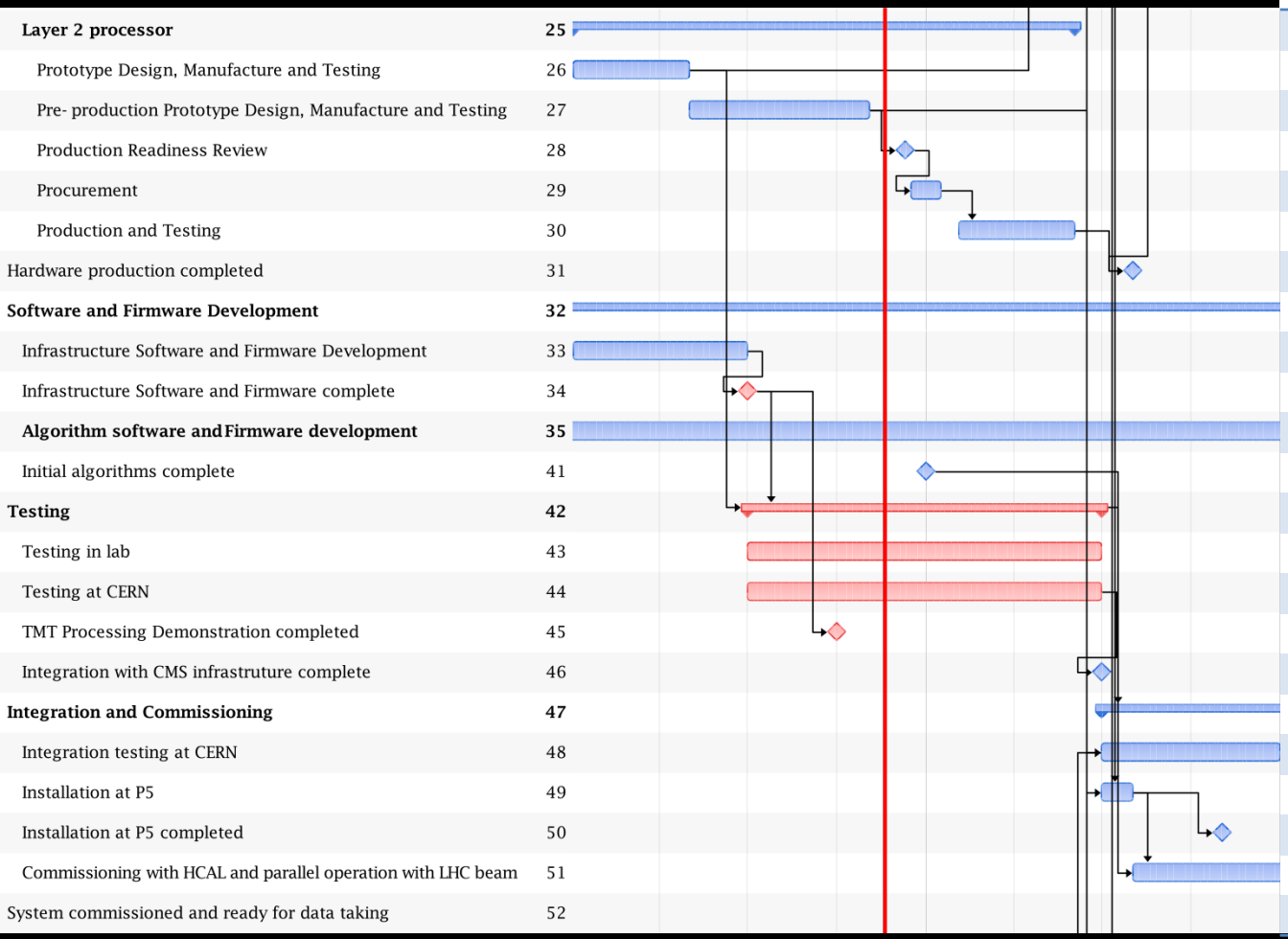
We are in open dialogue with all level-1 subsystems on this as this will affect everyone

Overall Project Status

CMS Trigger Upgrade Schedule

Relevant to Layer 2

CMS Trigger Upgrade Schedule



		Status
Layer 2 processor	**25**	—
Prototype Design, Manufacture and Testing	26	Completed on schedule ✓
Pre- production Prototype Design, Manufacture and Testing	27	Completed on schedule ✓
Production Readiness Review	28	Pending
Procurement	29	Pending (Contract prepared)
Production and Testing	30	Pending
Hardware production completed	31	Pending
Software and Firmware Development	**32**	—
Infrastructure Software and Firmware Development	33	Completed except DAQ
Infrastructure Software and Firmware complete	34	Completed except DAQ
Algorithm software and Firmware development	**35**	—
Initial algorithms complete	41	Completed and demonstrated ahead of schedule ✓
Testing	**42**	—
Testing in lab	43	Testing complete ✓
Testing at CERN	44	Testing complete ✓
TMT Processing Demonstration completed	45	Completed on schedule (using MP7s as Pre-processors) ✓
Integration with CMS infrastruture complete	46	On-going
Integration and Commissioning	**47**	—
Integration testing at CERN	48	Partially complete (waiting on other systems)
Installation at P5	49	Pending
Installation at P5 completed	50	Pending
Commissioning with HCAL and parallel operation with LHC beam	51	Pending
System commissioned and ready for data taking	52	Pending

Personnel

Management

- Hall, Tapper – Imperial
- Newbold, Paramesvaran – Bristol

Physics Studies

- Baber, Fayer, Ives, Marrouche, (Rose, Tapper) – Imperial
- Aggleton, Brooke, Grimes – Bristol
- Harper, Petyt, Shepherd-Themistocleous – RAL
- Beaudette, Mastrolorenzo, Sauvan, Zabi – LLR

Hardware

- Bundock, Greenwood, Iles, Rose – Imperial
- Jones – Iceberg Technology
- Durkin – RAL

Firmware

- Bundock, Iles, Rose – Imperial
- Jones – Iceberg Technology
- Dasgupta, (Newbold), Williams –Bristol
- Harder, Sankey – RAL
- Busson, Renaud, Romanteau – LLR

Online Software

- Bundock, Rose – Imperial
- Brooke, Lucas, Paramesvaran, Williams – Bristol
- Harder, Sankey, Thea – RAL

+ new students joining the project
+ new groups have expressed interest in joining physics/algorithm effort

Conclusions

Conclusions: TMT

- The September TMT Integration Test was a success
- Many lessons were learned which reaffirmed the motivations for choosing the TMT architecture over a conventional architecture

Conclusions: Hardware

- The MP7 card has now been in-hand for over a year
- Every part of the card has been thoroughly validated and understood, in particular the optical links and the Virtex-7 which are the most important and most complex parts of the boards
- A first revision has been received, which has only minor changes from the original design, and are either in use or in the final stages of validation

Conclusions: Software and Firmware

- The firmware for the MP7 is in an advanced state and available in the CMS trigger-upgrade SVN (CACTUS) repository
- The low-level software for the MP7 meets the official Level-1 online software requirements and is in the CMS trigger-upgrade SVN (CACTUS) repository
- All firmware is available in the CMS trigger-upgrade SVN repository
- All software and firmware has been designed to be reused by others, should they wish to do so
- Discussions on the system-level software have been initialized by the layer-2 groups with the aim of minimizing software effort required by the trigger community as a whole

The take-home message

a) The TMT principle has been proven to be very successful.

b) The MP7 is an exceptionally advanced board and is very well understood.

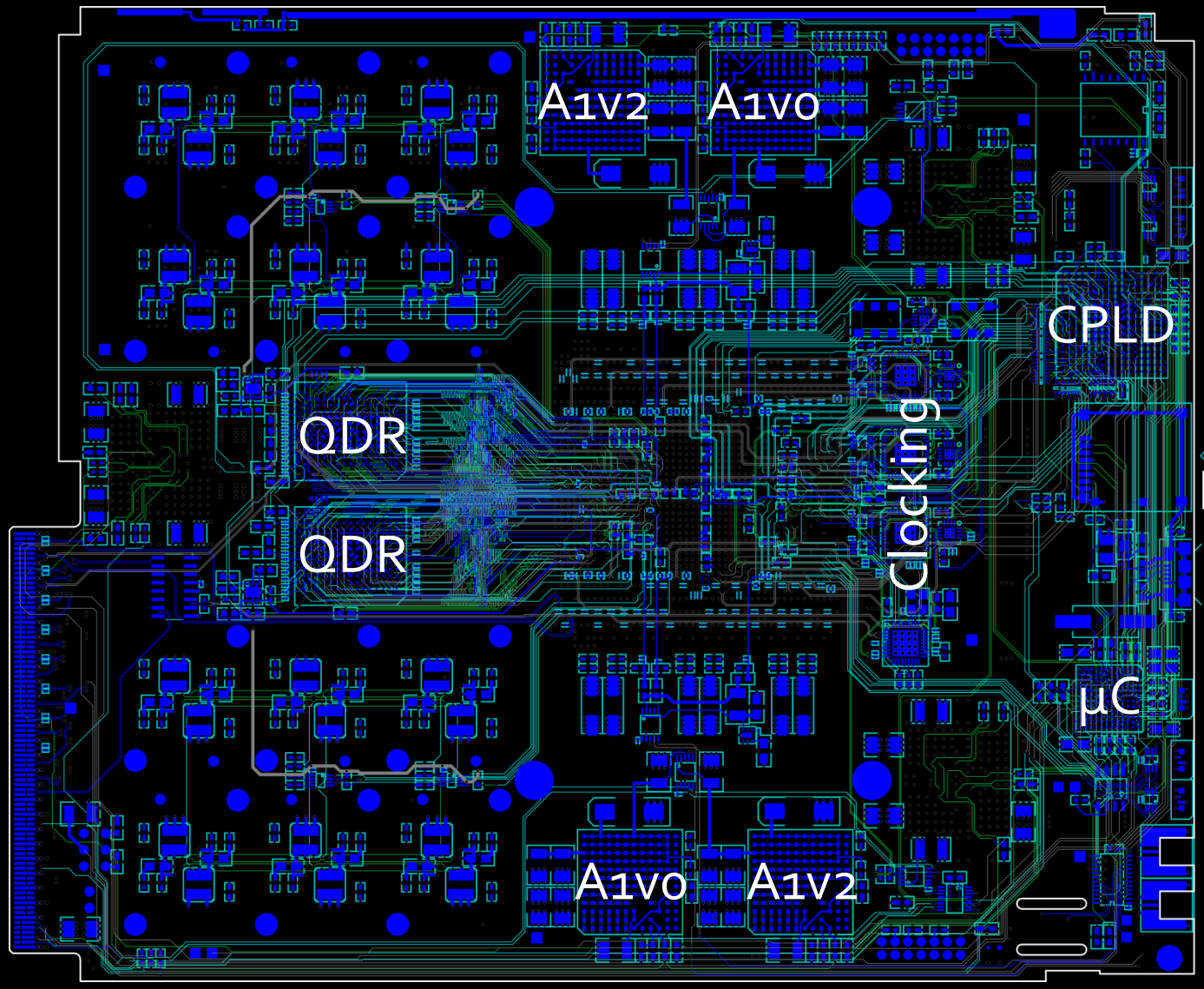
c) The firmware for the MP7 is in an advanced state.

d) The low-level software for the MP7 is in an advanced state.

e) We are using the advanced position of the rest of the project to start attacking the system-level software.

Spares

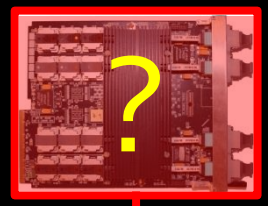
MP7 board – Bottom half



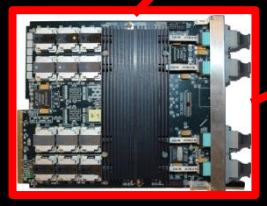
Website

www.hep.ph.ic.ac.uk/mp7

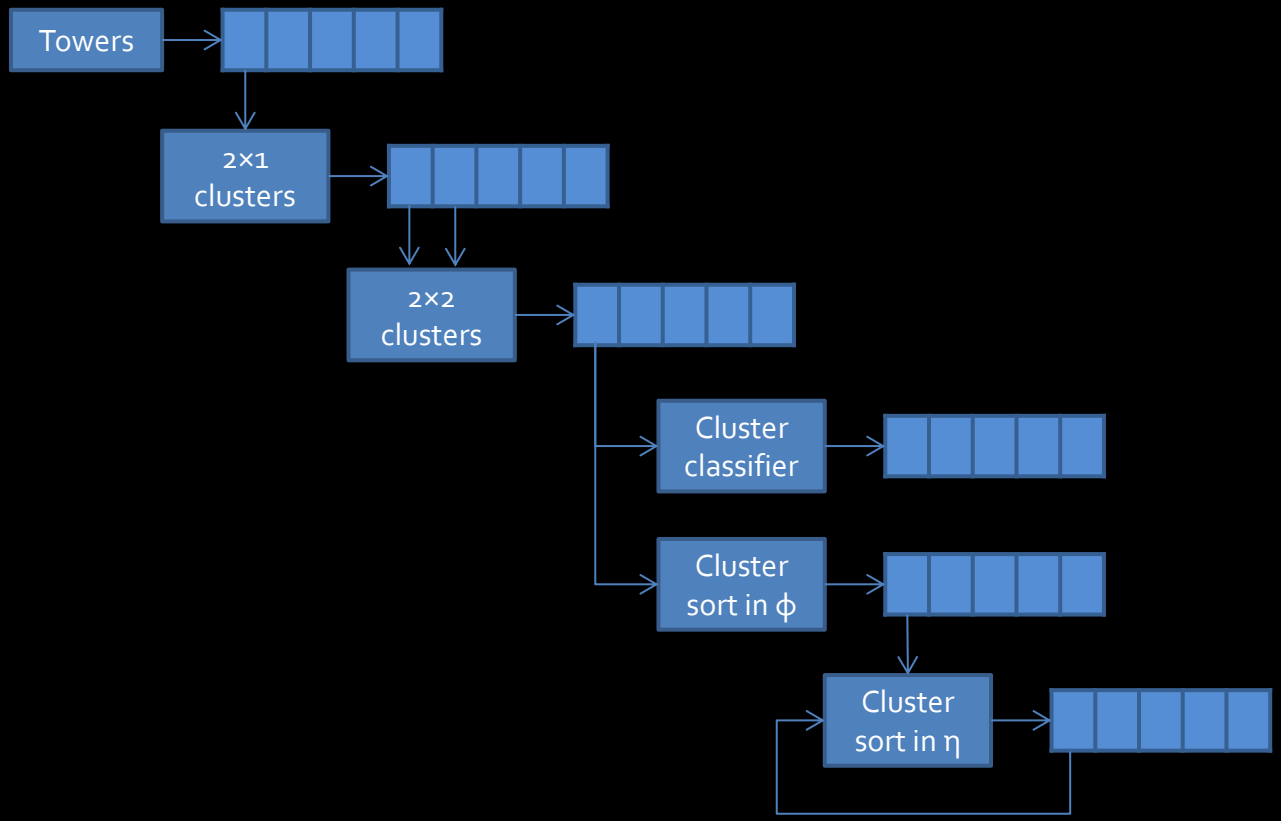
MP7 users

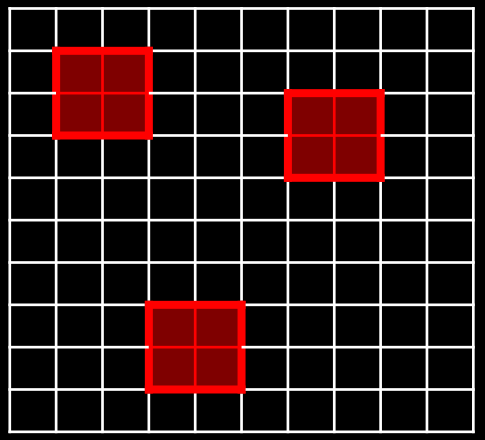


ECAL
HCAL
HF
CSC
DT
CuOF
RPC
TCC
oSLB
µHTR
µHTR
MPC
Mezzanine
New SC
& fan-out
LB
New SC
& fan-out
Fall-back solution
Calo Trigger
Preprocessors
µTF Layer
Endcap
Overlap
Barrel
Calo Trigger
Main Processors
Sorting/Merging Layer (Optional)
Endcap
Overlap
Barrel
Demux
µGMT
µGT

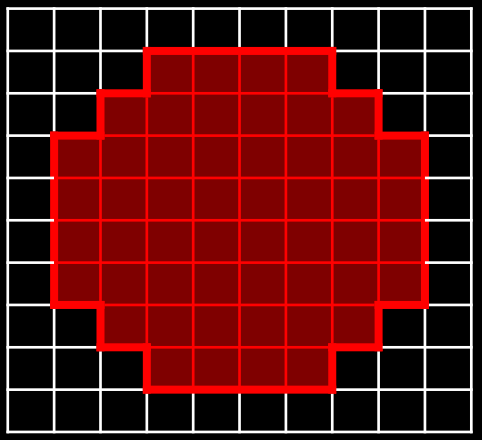


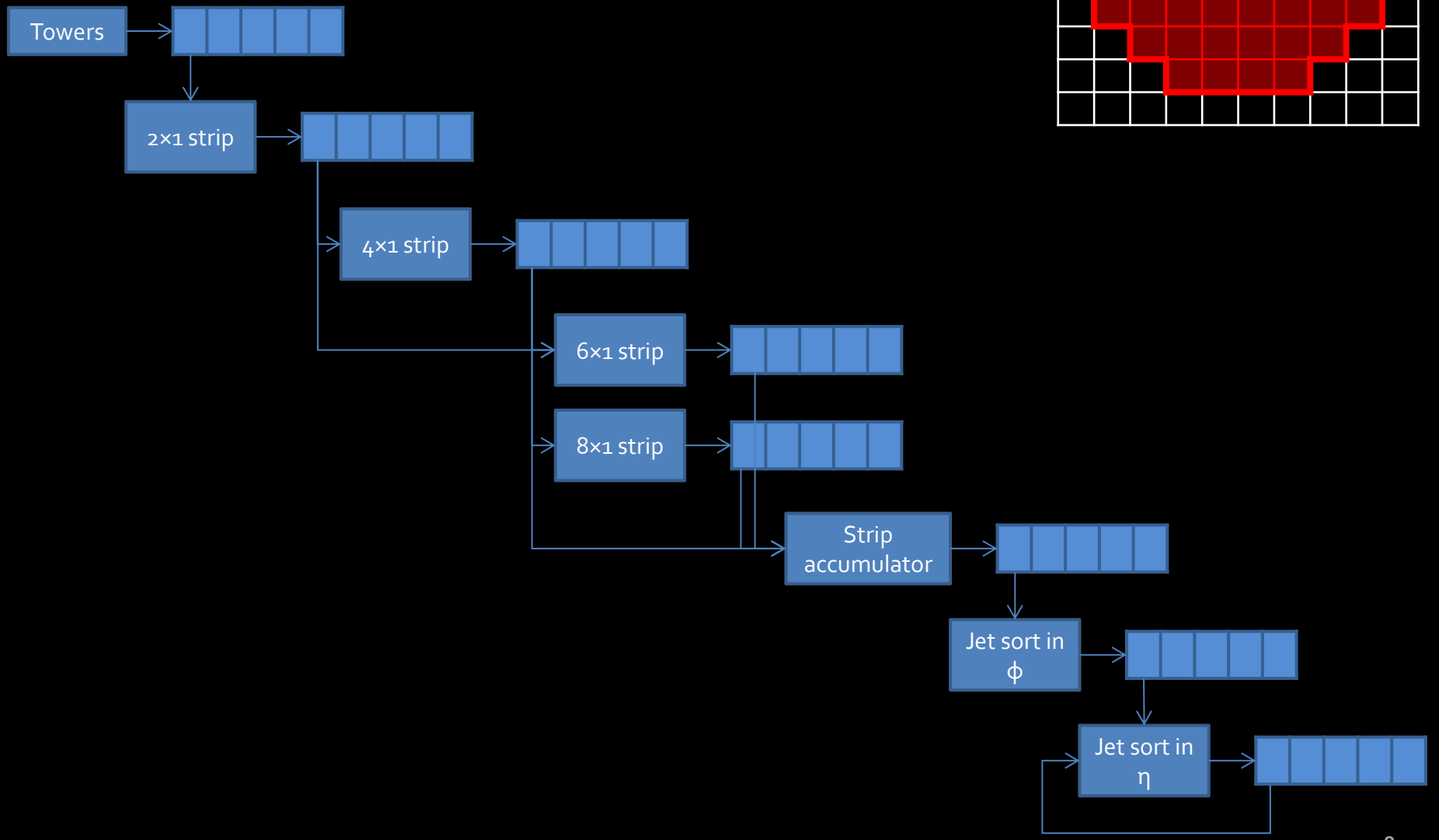
Clusters


Towers
2×1 clusters
2×2 clusters
Cluster classifier
Cluster sort in ϕ
Cluster sort in η

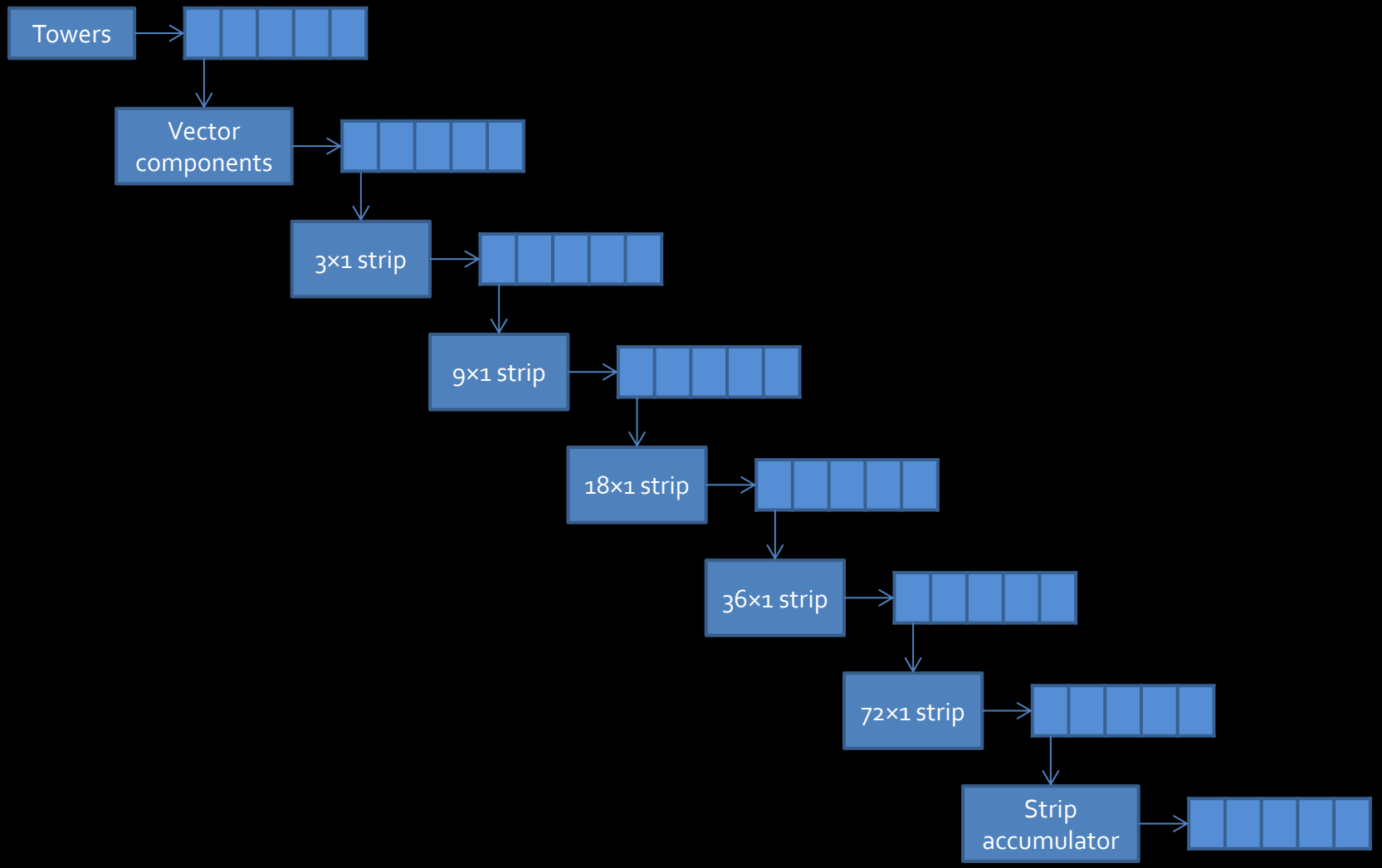


Jets



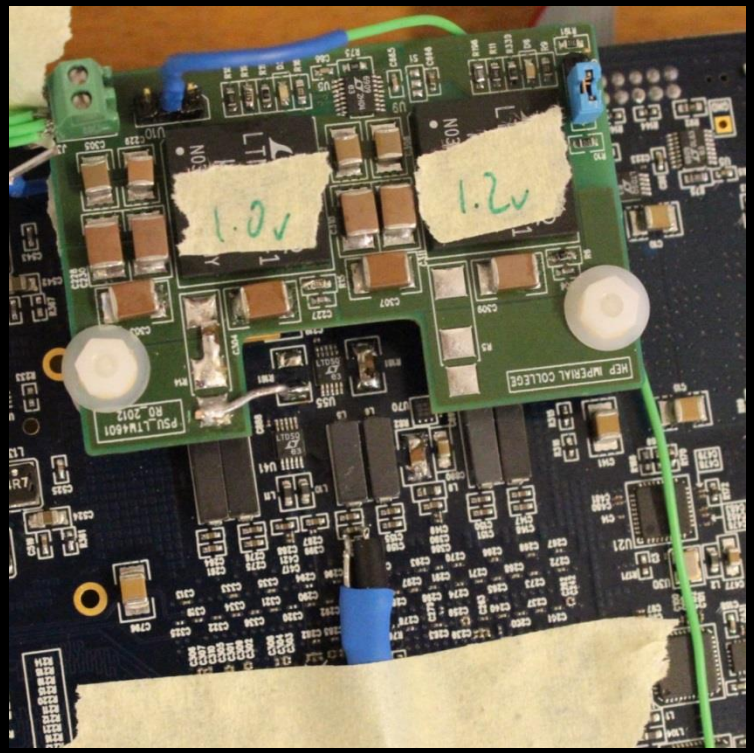

Towers
2×1 strip
4×1 strip
6×1 strip
8×1 strip
Strip accumulator
Jet sort in ϕ
Jet sort in η

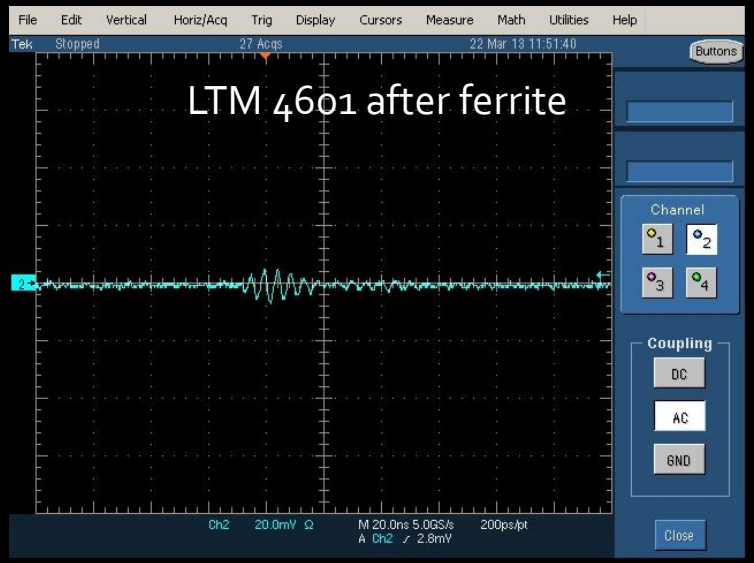
Ring sums


Towers
Vector components
3×1 strip
9×1 strip
18×1 strip
36×1 strip
72×1 strip
Strip accumulator

Power supply validation

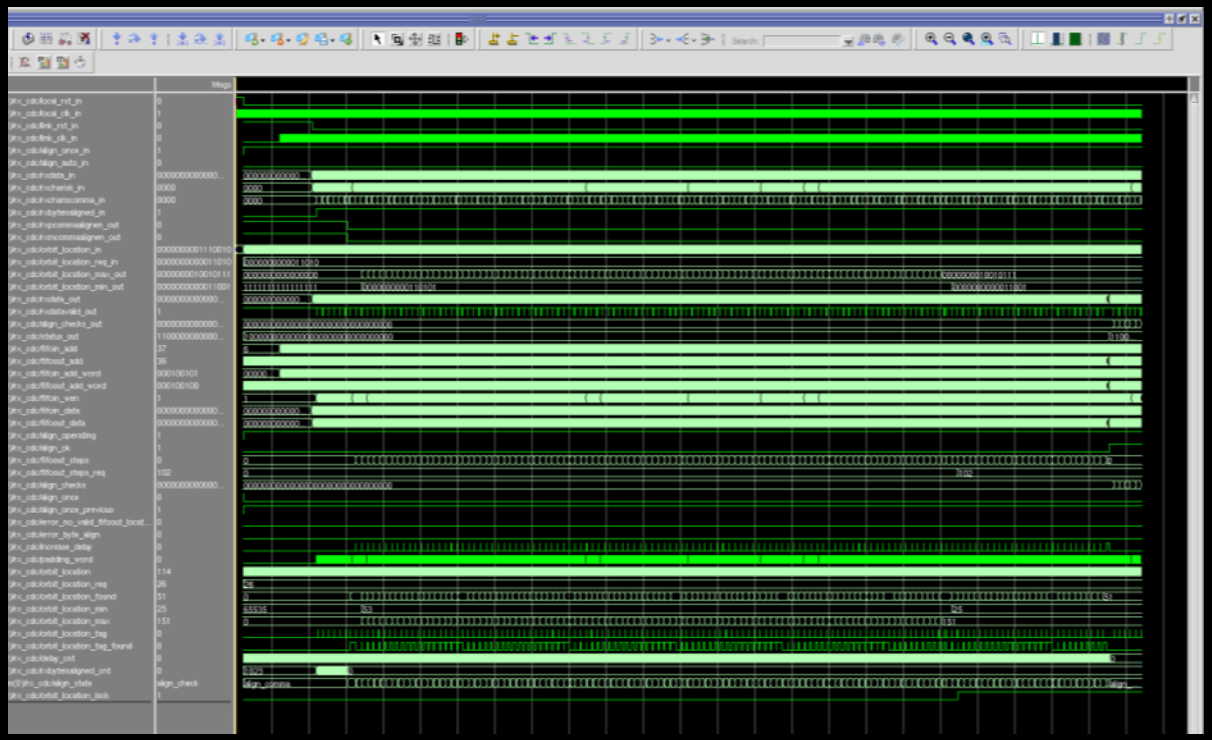
- We were very concerned about the possibility of power supply changes introducing noise
- Several test cards were made to test alternative power supply designs
- Noise was measured both electrically and by its effect on the error-rate of the 10Gb/s optical links
- No increase in bit error-rate was observed and we were happy to proceed
- These tests have left one board unsuitable for normal, non-benchtop, use. We have enough boards in-hand, however, that we could "burn" a board for the sake of progress



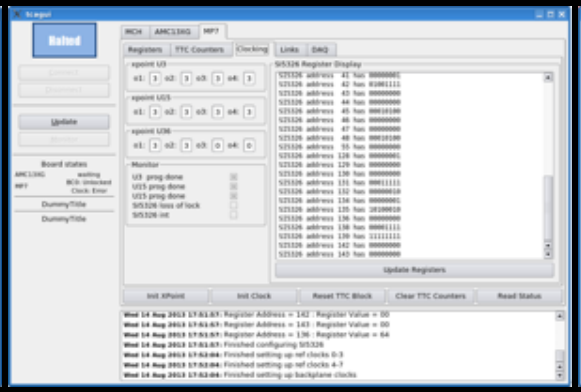


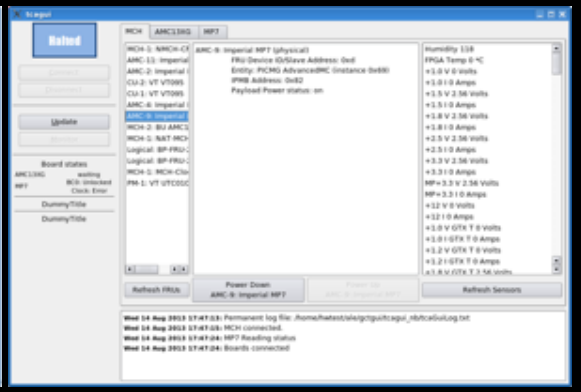
Automated Link alignment firmware

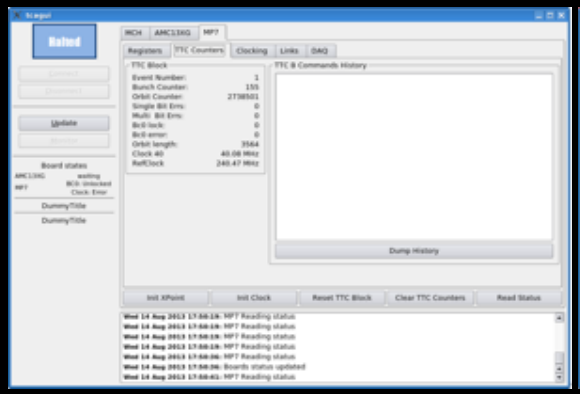
- Fixed, low Latency GTX/GTH Serdes Link
- Asynchronous or Synchronous with LHC clock
- Rx buffer bypassed for low latency & asynchronous clock capability
- CRC32 integrity checks
- Locks to TTC timing
- Spy buffer
- Only 256 orbits to align the entire system
- Has been in continuous use in hardware for many months

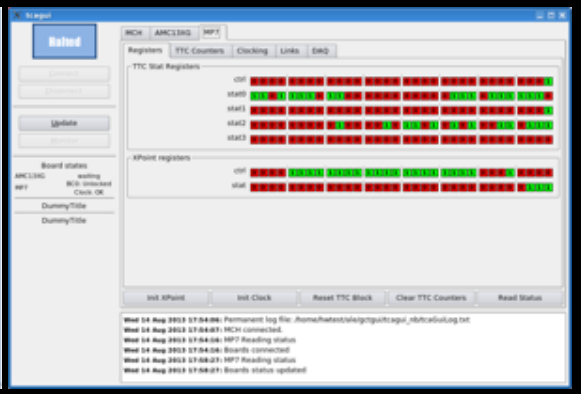


Screenshots

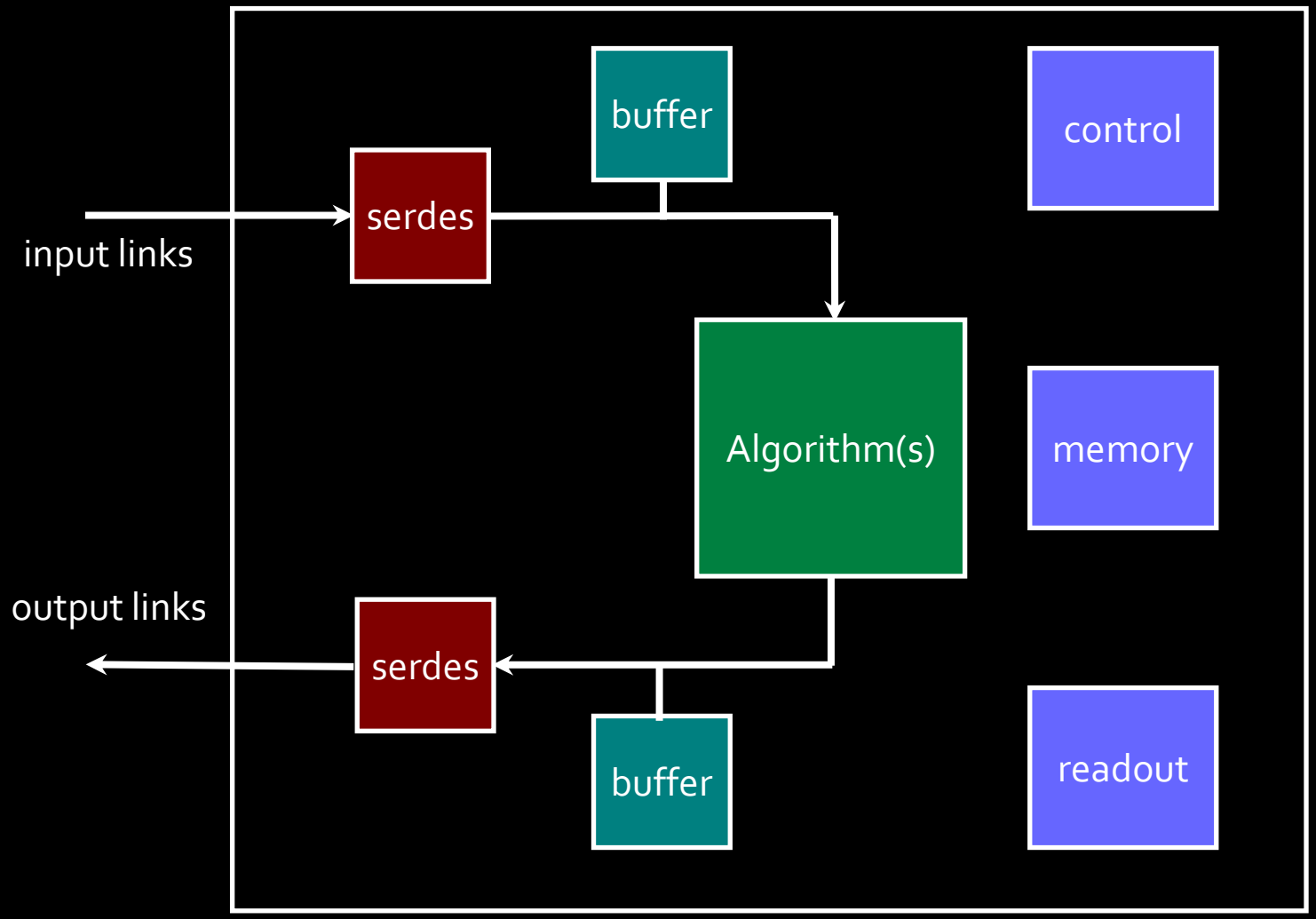








An Upgrade Processor



Software Goals

Can we rationalize the board control software?

- MP7, CTP7, MFT7 have a very similar structure
- One software class to control them all?

Can we use the same software model for production and testing?

- Standardize the concept of 'test' (what goes in, what goes out)
- Introduce flexible system-wise tests: from {system A, buffer X} to {system B, buffer Y}
- Are concurrent modes (test/production/development) possible?

Possible System