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The CMS Tracker front-end and control electronics in an LHC like beam test.

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Abstract

A complete prototype of the CMS tracker read-out and control system has been built using components as close as possible to the final design. It is based on an amplifier and analogue pipeline memory chip (APV), analogue optical links transmitting at 40Ms/s and a VME mounted digitisation and data handling board (FED-PMC), supplemented by a control architecture based on FECs which set and monitor the components of the entire system. This system has been successfully operated for the first time under LHC like beam conditions in a 25ns structured beam provided by the SPS at CERN. The objective was primarily to test the synchronisation and pile-up effects in a high trigger rate environment and to examine the many issues involved in operating a complete readout and control system.

I. INTRODUCTION

The read-out and control system for the CMS Tracker is a complex and ambitious project, meant to cope with the extremely new and hostile conditions which will be encountered at the LHC p-p machine. The electronic challenges for the system are principally to ensure a low noise during the entire operational lifetime, along with an adequate bunch crossing identification, which is ultimately limited by the speed and amplitude of signals coming from the detectors as well as by electronics.

The analogue read-out is based on APV chips [1], equipped with a charge sensitive amplifier with a time constant of 50ns whose output voltage is sampled at 40MHz. Samples are stored in a pipeline memory for a time equal to the L1 trigger latency (about 3.2 μs) and then processed, on the arrival of a trigger, by an analogue circuit which performs a weighed summation when the chip is operated in deconvolution mode.

The data are then transmitted by analogue optical links [2] to the counting room. The optical links use edge-emitting lasers operating at 1310nm wavelength, coupled to single mode fibres with 3 patch-panels and PIN photodiode arrays. The digitisation is performed by the Front End Driver, which in the test-beam version, (FED-PMC) is an 8 channels ADC on a PCI Mezzanine Card [3]. The digitised data are then sent to the main Data Acquisition System.

The timing and control path is separated from the readout path in order to ensure that control and monitoring are totally independent from the DAQ system. The Front End Controller module (FEC) [4] (at present in a PMC version) takes care of: -

a) interfacing with the Timing, Trigger and Control system [4] and hence distributing the encoded clock and trigger signals to the front-end, and
b) setting and monitoring via I^2C protocol all the parameters (e.g. bias voltages on APVs, delays on PLLs, etc.) needed to operate the system.

The communication architecture in the slow control system is based on a 'token-ring' protocol, which connects the FEC to the Communication and Control

Units (CCUs) and on a 'channel' protocol, which connects each CCU with the front-end chips.

All the components of the system can be tested (separately or partially assembled) in a laboratory, but there are questions which can only be answered in realistic operational conditions. The main reasons for using an LHC like beam can then be summarised in the following points: -

a) subtle effects in the read-out electronics can become evident only in joint tests with detectors exposed to a structured beam;

b) one of the main issues is the synchronisation of the system; only an LHC-like beam test provides suitable conditions to study possible synchronisation procedures as well as developing monitoring tools.

Furthermore the May test has offered the first opportunity to:

a) integrate and test the whole optical link system, even if in a small scale as compared with the one which will be needed in CMS;

b) integrate and test the Slow Control system.

II. MAY 2000 TEST SYSTEM DESCRIPTION

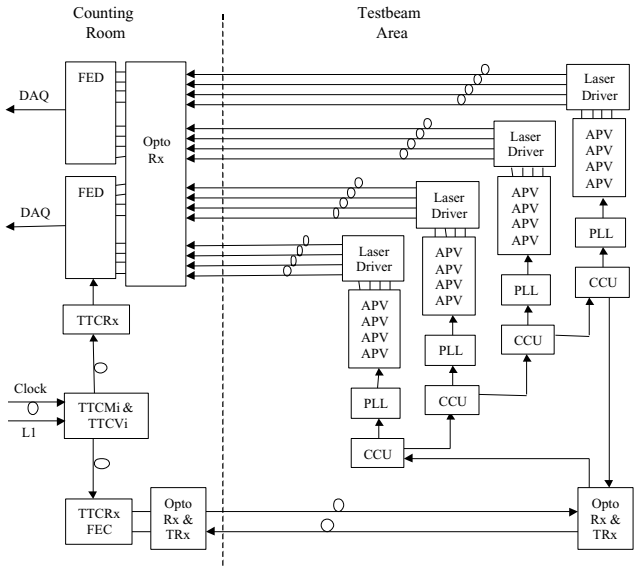

Figure 1: Schematic layout of the system installed in May 2000.

A. Timing and trigger

A TTC machine interface [5] crate, in the final version to be used in CMS, receives the 40MHz Clock and the 43KHz SPS Orbit signal from the Prevessin Control Room. These signals are distributed via optical fibres to the LHCrx module interface where they are converted to electrical signals. The clock is encoded with the trigger signal by the TTCvi module and then sent to the FEC for final distribution to the front-end via a digital optical link. The trigger signal is provided by the coincidence of two photo-multipliers (3x3 and 3x6cm^2) located along the beam line before the detectors.

B. Read-out and Control: Hardware

Four "standard" silicon strip detectors have been fully equipped and read out with four APV6s. Four 4-channel analogue optical links [6] were installed to transmit the data to the counting room. The optical links used prototype components, including 4-way laser packages and 4-way analogue laser driver chips. Data were transmitted along single-mode fibre ribbons, embedded in a prototype 96-way optical cable, having two (MT) connectorized breakpoints. The optical signals were converted to electrical ones via a prototype 4-way receiver. Two FED-PMC cards (16 channels) have been used to perform data capture and digitisation. Digitised data are then sent to the Central DAQ system.

Each detector module has been equipped with a CCU, used for decoding the clock and trigger signals as well as for the distribution of the I2C parameters to all the devices, and a PLL programmable delay unit [7] for clock regeneration and phase adjustment. The four CCUs were connected in a ring served by one FEC. Prototype digital optical links were used to transmit the digital signals at 80Mbit/s. Earlier measurements performed in the laboratory demonstrated that these optical links have a bit-error-rate $<10^{-12}$. The schematic layout of the system installed for the May test is shown in Fig 1.

C. Control: Software

A multi-processor and multi-layered software architecture has been developed: a low level library running under the LynxOS operating system on dedicated VME CPU boards handles all accesses to the hardware through the FEC boards and includes a mechanism to lock the access to any front-end device. An intermediate library contains the primitives to build tasks, running on this VME CPU, that directly access the various CCU registers. The topmost software layer allows the users to directly access the registers of the various front-end devices via the VME processor with no need of any knowledge about the interconnecting hardware.

The values of the parameters need to be stored and traced back as a function of time. A database server, running on a standard PC, based on the commercial Oracle Database (DB) management system, has been developed. Data and commands from the database server are recognised, interpreted, dispatched to the appropriate tasks and subsequently downloaded in the hardware.

D. Read-out and DAQ: Software

The readout software is subdivided into three main parts, the Readout Unit (RU), the Run Controller (RC) and the Filter Unit (FU). The RU is a modular software package designed to read-out data from the FEDs, performing their formatting and error checking. It also executes ancillary tasks such as the initialisation of the back-end read-out hardware and message transfer between the read-out crates. Finally it writes the formatted data, spill by spill, to a Dual Port Memory, from where they are picked up by a remote Filter Unit through VME/MXI or Ethernet. At this stage the data fragments coming from different crates are assembled into spills, processed and stored in an object-oriented database ready for the offline analysis. Data taking is supervised by the RC which, at each start of run, initialises all the RU tasks, and also communicates with the data base server so that all the I2C parameters can be downloaded in the front-end hardware. In parallel with the main DAQ system a spy channel on the data has been set up, aiming to perform basics tests on the quality of the data and to perform and check the synchronisation.

III. BEAM STRUCTURE

A 25ns structured pion beam (10^6 π/spill) has been provided by the SPS at CERN. A train of 84 bunches, spaced by 25ns, is delivered every 23μs (43kHz SPS revolution frequency) over a spill duration of about 2s.

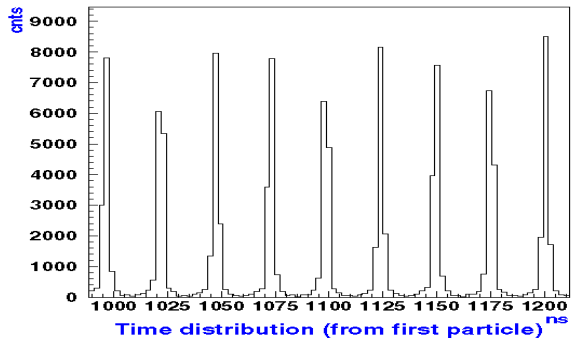

Figure 2: 25ns beam structure.

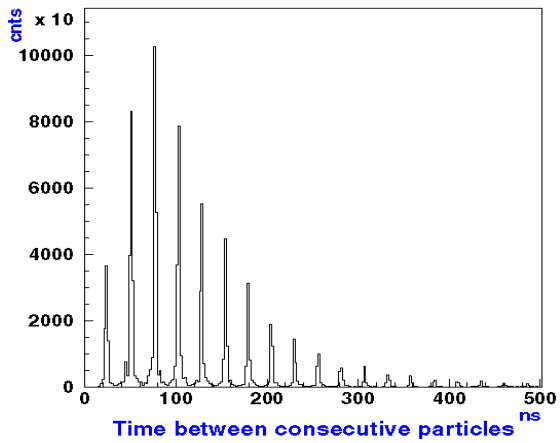

Figure 3: Distribution of the time difference

In order to confirm that the test was carried out under the expected LHC like conditions, a beam monitoring system, based on a multi-hit TDC has been carefully set-up with the purpose of measuring the time distributions of the particles in the trains and the bunch width [8]. The 40MHz structure has been observed clearly as shown in Fig. 2.

The distribution of time between full bunches (containing at least one particle) shows that intervals of 3 bunches are favoured, being present in 17% of the cases, as shown in Fig.3. This feature makes the beam adequate to study pile-up effects.

The width of a single bucket, when measured in a high rate pion beam, is a broad distribution (see Fig.4) which receives contributions both from bunches containing a single particle and bunches containing more than one particle. The latter situation occurs 74% of the cases as demonstrated by the analysis of the pulse height spectra of the ADCs connected to the counters for multiplicity studies.

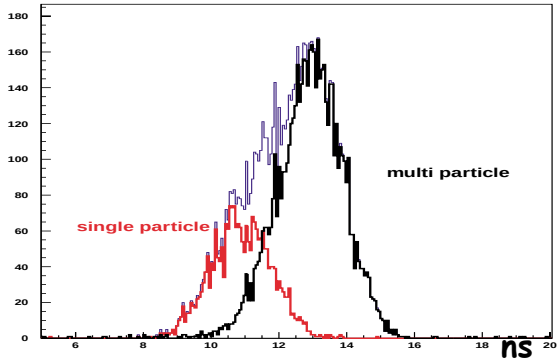

Figure 4: Distribution of the arrival times of particles with respect to the 40MHz machine clock in a pion beam. Bunches with single and multiple particles are present.

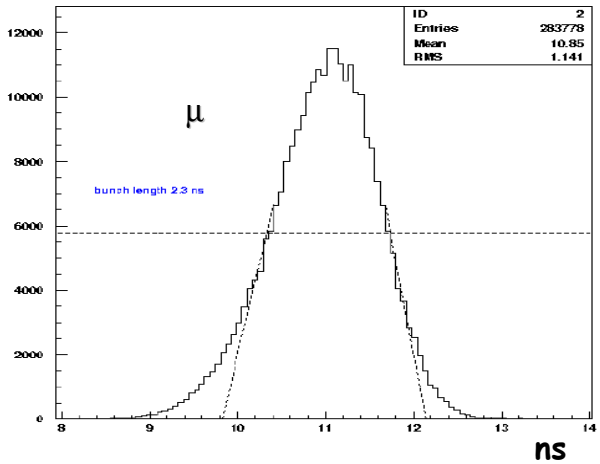

Figure 5: Distribution of the arrival times of particles with respect to the 40MHz clock in a 10^4 μ/spill beam.

With a low intensity muon beam (10^4 μ/spill) there is no overlap of particles in the counters and a clean distribution of the arrival times of the particles with respect to the 40MHz clock is obtained, as shown in Fig.5. By assuming, on statistical grounds, that all the bunches have identical shape and time evolution during the extraction, the width at the base measured with events belonging to different spills is 2.3ns, in agreement with the expectation of 2.5ns measured by the SPS.

IV. SYNCHRONISATION

One of the purposes of the May 2000 test was to check to what extent synchronisation of a modest number of modules could be achieved so that different APVs could read out data belonging to the same bunch. The chips on each detector module are, in principle, synchronous by definition because they are driven by the same clock and trigger (delivered via the CCU and PLL). In the beam test, then, the time alignment problem to be solved is twofold.

a) Modules sitting along the control ring receive clock and trigger signals at different times. The PLL delay units were programmed in order to compensate, aligning all the modules to the last in the ring. Both coarse (multiple of 25ns) and fine (steps of 1.04ns covering the 25ns interval) delays have been introduced where required. This step constitutes the very basic time tuning and no beam is required. The delays needed have been measured by the difference in the arrival time at the FED of the synchronisation pulses (tick marks) output from the APV (Fig 6).

b) After having been shaped in the APV6 preamplifier, the signal from the detectors is sampled in the pipeline every 25ns. The delays have to be adjusted so that on the occurrence of a trigger the signal is sampled at its peak, in order to maximise the S/N ratio. This essentially means that the sampling point in the pipeline has to be in phase with the arrival time of particles. This adjustment is not especially crucial when the APV is operated in 'peak mode' [1]; it is, however, when the chip is operated in 'deconvolution mode', where a displacement from the peak of ± 1ns causes a loss of about 5% of the signal.

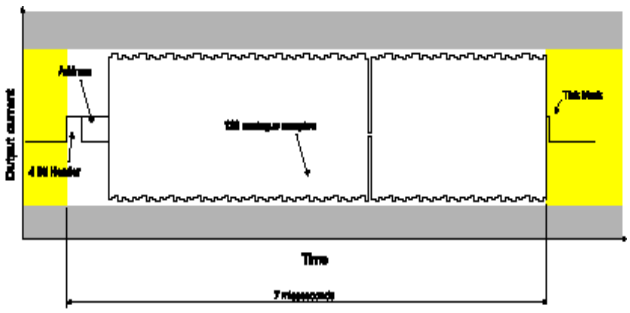

Figure 6: Example of the data stream output from the APV6. In the absence of triggers the output is just a sequence of pulses 1.75 μs apart.

V. ANALOGUE OPTICAL LINK

The setting up of the optical links required adjustments to the gains and offsets, as the separate components within the readout chain from the APV6 to FED input were not well matched. The APV6 output was 120mV/MIP and the optical link gain was 2.5-4.0, with the FED input having a maximum amplitude of 1.5V. A potential divider was therefore added at the input to the link to provide a widely adjustable dynamic range. Values of attenuation were chosen so that dynamic ranges of 5,8, and 12 MIPs were tested.

The laser dc-bias points were set to ensure that the lasers were always above threshold. The receiver offsets were then adjusted to map the optical link output onto the FED input range. These operations were done manually during the beam test, using APV synch-pulses as the reference signals. In the final system automated procedures will be used to optimise the readout chain settings.

The optical link performed well, with transmission characteristics closely matching those previously measured in laboratory. The attenuation of the input signal to the link, coupled with the large gain of the prototype links, incurs a penalty in the noise performance. Up to 3 times more noise was contributed by the link compared to the value of 350 electrons expected in the final system [2], where the link gain will be closer to unity.

VI. PRELIMINARY RESULTS FROM THE DATA

Data have been collected under various conditions, operating the APVs both in 'peak' and 'deconvolution' mode, with various trigger rates (up to about 50 KHz) using a pion or muon beam.

As far as the synchronisation is concerned, an online procedure has been successfully performed to time-in the system with respect to the beam, as mentioned in section IV (b). Nonetheless, continuous monitoring of the APVs during the data taking revealed that 4 out of 16 chips became asynchronous after about one hundred events (a reset signal was sent at the start of each spill). The address of the cell in the analogue pipeline [1] where the triggered sample is stored must be the same for all the APVs if the system is correctly timed-in and in the absence of other faults, such as in this case. On two of the four modules two APVs lost synchronicity (see Fig.7), in a random way with respect to each other, while in principle the APVs on the same module should be synchronous by construction. This particular situation can be explained in different ways (a fault in the clock, a fault in the trigger or a fault in the chip itself) and is still under investigation.

A number of runs were taken with a pion beam in 'peak' mode, forcing the physical triggers to be spaced by 75ns ('1001' type). Trigger filters protected the

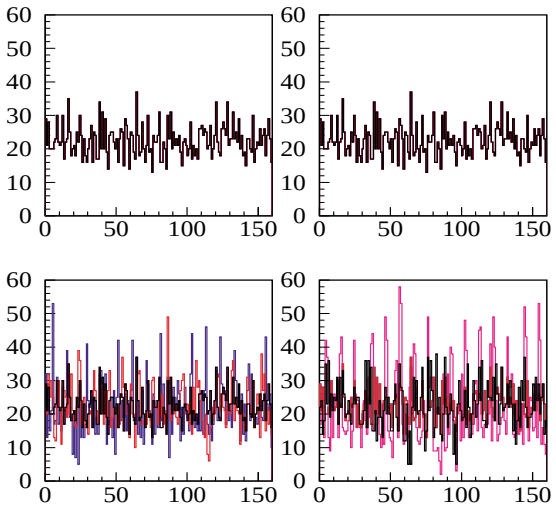

Figure 7: Distribution of the cell number in the APV pipeline which has been triggered. This number ranges from 0 to 159 in the APV6. The four plots are obtained from the 4 APV on each module. Each plot is the superimposition of 4 histograms, one per APV. In the first 2 modules (upper plots) the APVs are clearly synchronous while in the other two modules, two APV each went out of synchronicity.

APVs against overflows and hence errors in the pipeline. The '1001' sequence produces in the APVs the so called 'back-to-back' frames; the APV6 response to two triggers occurring within 7 μs consists, indeed, of two data frames from the APVs with no gap in between. The '1001' sequence was meant to study the overall performances of the read-out electronics as well as the pile-up effects on the S/N ratio; events with particles separated by 75ns have been identified in the off-line analysis but the statistics collected in this first test are too low to give an accurate quantitative estimate of the effect on the signals [9]

The correlation between the position of the hits in three of the detectors has been studied in these runs, the result of which is shown in Fig.8. An entry in the histogram is produced each time there is a position between a pair of detectors out of three and the first and second triggers are analysed separately. No significant difference between the two triggers is shown, both in the statistics and in the value of the correlation.

VII. CONCLUSIONS

A first test has been performed on a full prototype of the CMS Tracker read-out and control electronics chain. It has been operated in a 25ns structured beam and the primary goal of integrating all the components, most of them very close to their final version, has been reached very successfully.

In order to tackle problems such as the control of the entire system or the time alignment, tools aiming to make procedures of this kind automatic have been developed which can be improved in the future when a bigger system will undergo the same kind of tests.

The data collected in various conditions have only been partially studied and the off-line analysis is still on-going; the main result obtained up to now is that the synchronisation of the system has been successfully achieved and that we are confident we are able to identify correctly particles coming three time-slots apart.

Experience has been gained while dealing with the complex system and with the special beam environment.

Future tests of the same kind on more extended systems will be of great help for a deeper understanding and for the development of procedures (calibration, synchronisation etc. etc.) which are vital for the future CMS Tracker.

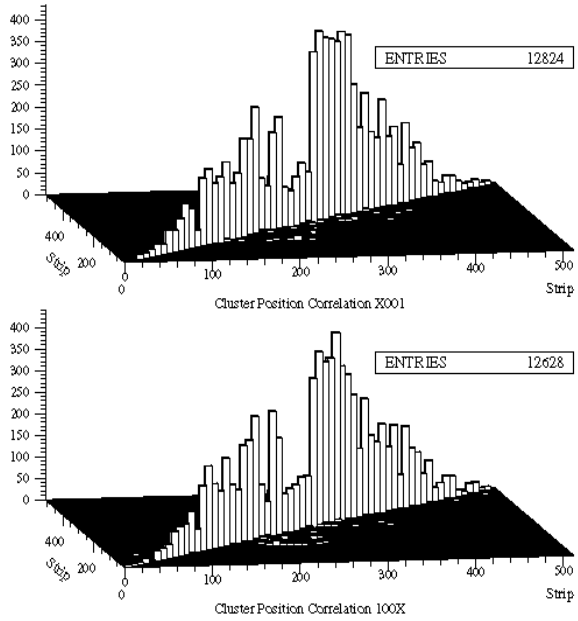

Figure 8: Correlation between hits in three of the modules put on the beam in '1001' trigger conditions. The correlation is studied by APV. Upper and bottom plots show the correlation measured in the first and second trigger respectively.

VIII. ACKNOWLEDGEMENTS

We would like to thank Mark Raymond at Imperial College and Marcus French at RAL.

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