



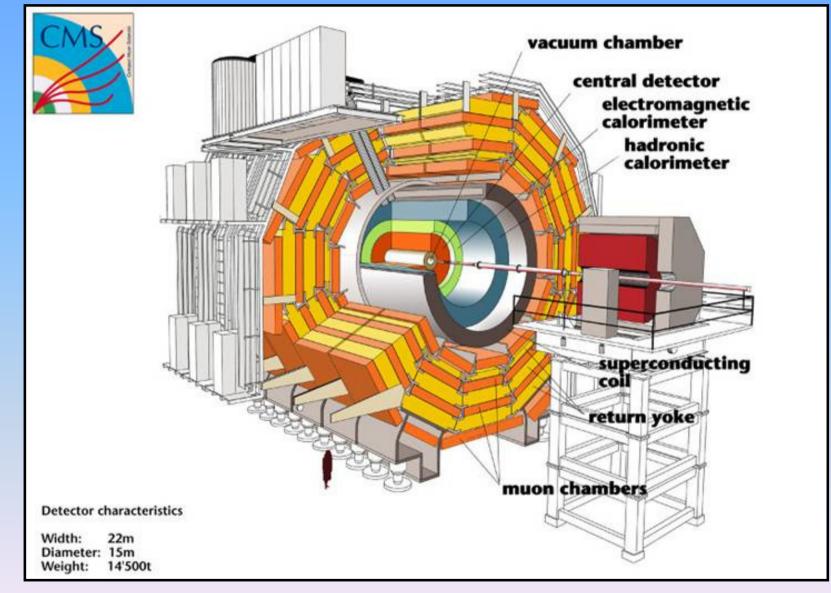
The CMS L1 trigger: from LHC to SLHC

Andrew Rose Imperial College, London IOP HEP 2008, Lancaster 31.03.08-02.04.08

Summary

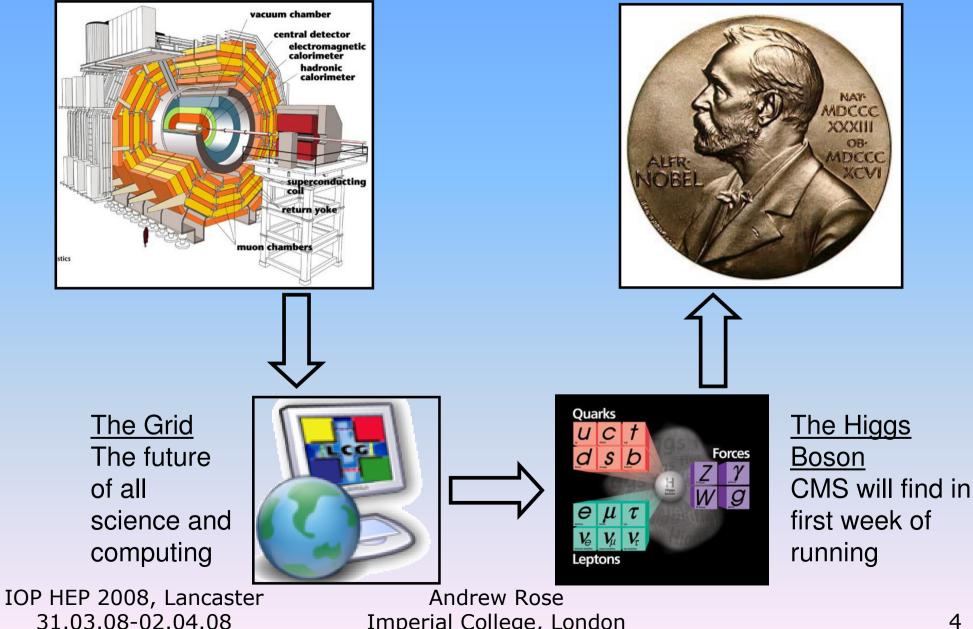
- CMS
- The data myth
- The Level-1 Trigger
- The Global Calorimeter Trigger
- LHC vs SLHC

CMS



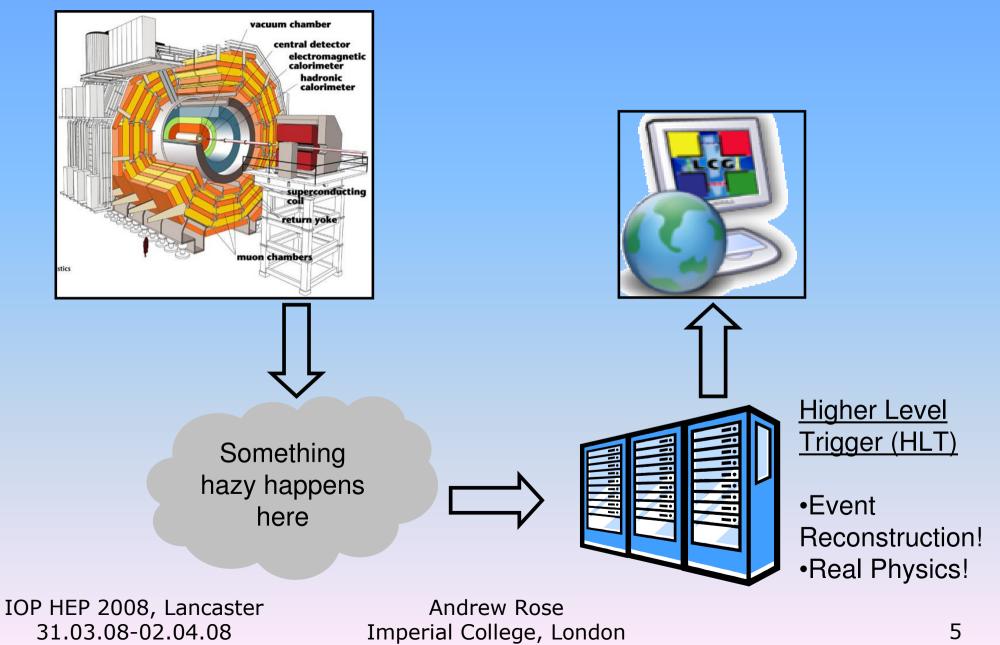
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The data myth

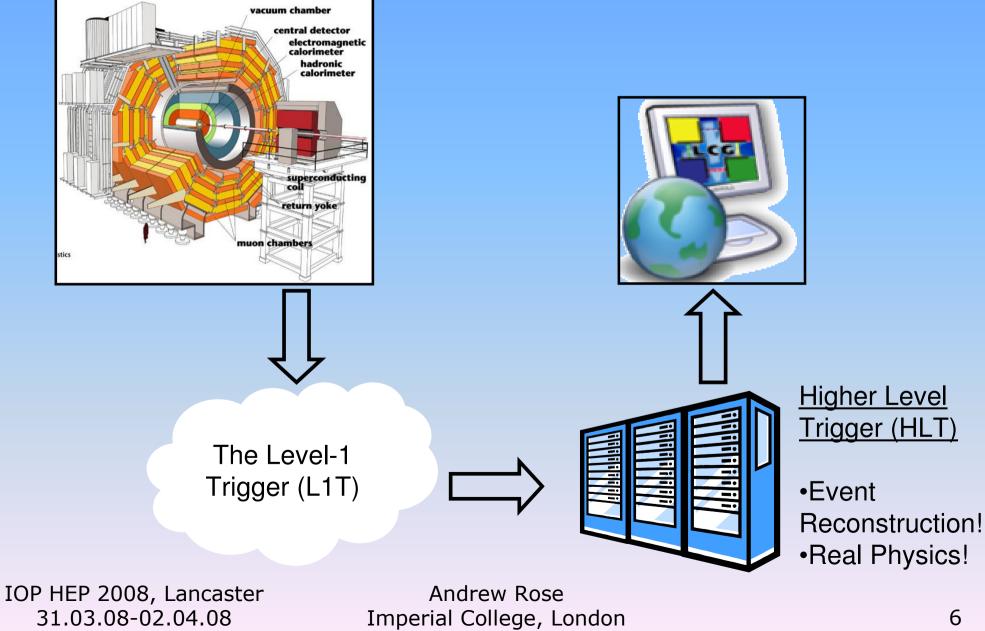


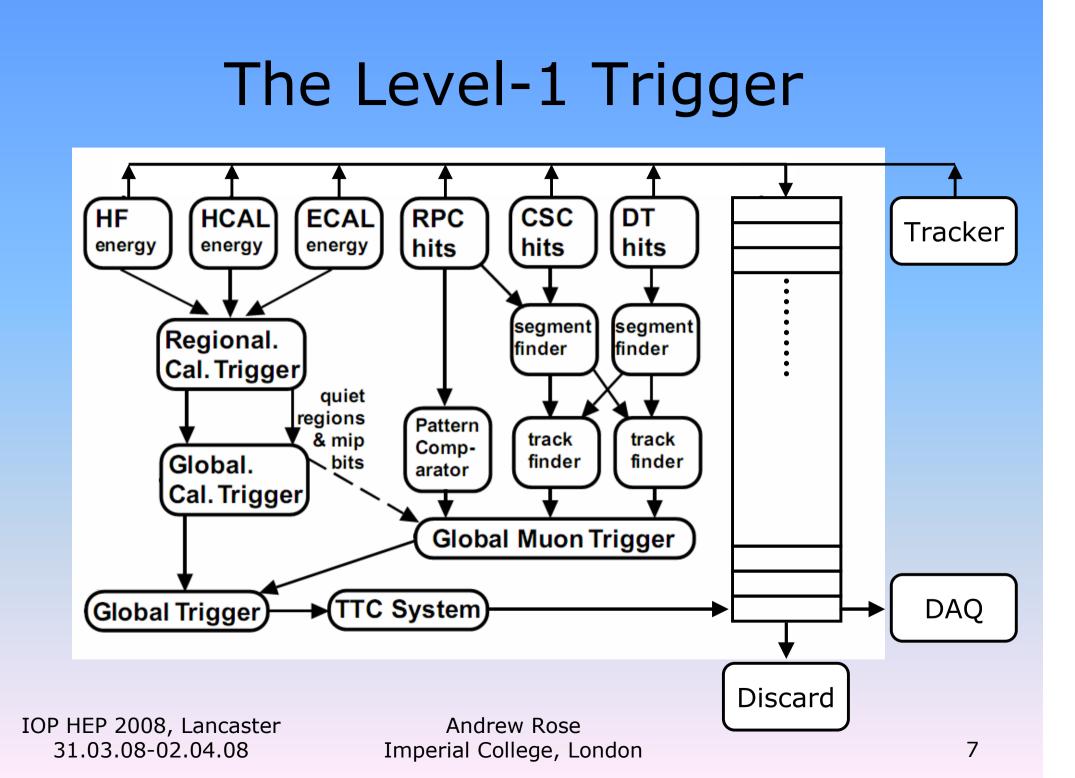
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The data myth

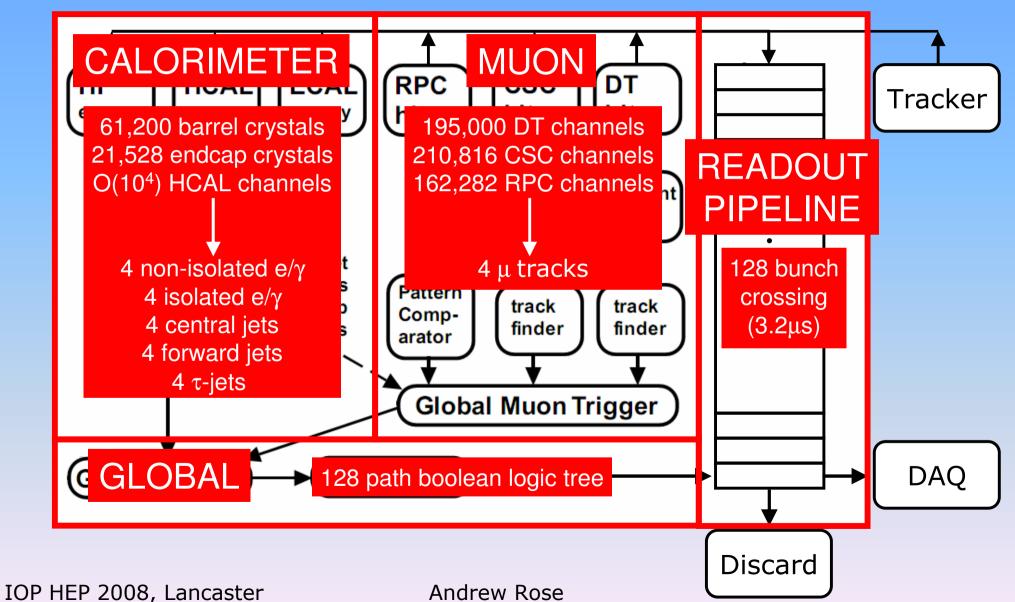


The data myth





The Level-1 Trigger



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The main problem for the GCT was physical space: The need to bring 108 32-bit wide parallel cables to a single point for processing

Achieved in stages

- Adapter cables that allowed the use of newer, smaller connectors
- Adapter cards (Source Card) which converting parallel copper links to Gbit/s optical links
- Optical patch panel to convert from single channel to 12-channel optical fibres
- 12-channel optical receivers wired directly to FPGAs with on-board Gbit/s deserialiser

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CMS GCT leaf card x1 (to scale)

CMS RCT crates x3

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Six leaf cards, mounted on two wheel cards search for jets, defined as a region (4x4 trigger towers) having energy greater than all 8 surrounding regions.

These jets are classified as

- •Central (|η|<1.5)
- •Forward (|h|>1.5)
- •Tau (if all 9 regions pass a tau veto)

The candidates are sorted by energy on each wheel card and the highest ranked candidates passed to the concentrator card where they are globally sorted. The highest 4 ranked candidates of each type are sent to the global trigger.

Two further leaf cards, mounted on the concentrator card sort the e/γ candidates and these are again forwarded to the concentrator and the highest ranked candidates sent to the global trigger.

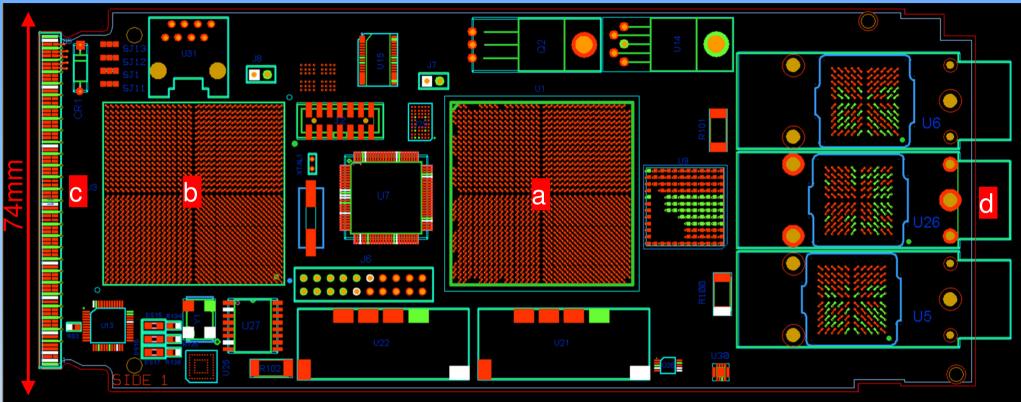
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Lessons learned from the GCT:

- Large FPGAs offer far more flexibility than processing ASICs
- Large parallel copper buses no longer have any advantage over lowlatency, high-speed serial links and are rapidly facing extinction...
- The arcane VME control bus is a severe hindrance, forcing those who want any kind of useful functionality to
 - a) customise it as is done elsewhere in L1T (yuk!)
 - b) suppliment it with modern architectures (ethernet, usb, etc) as we have had to do
- The multitude of cable standards meant a lot of wasted time and effort
- The lack of a standardised data back-plane architecture for the L1T has caused no end of grief...

The response: The matrix processor...

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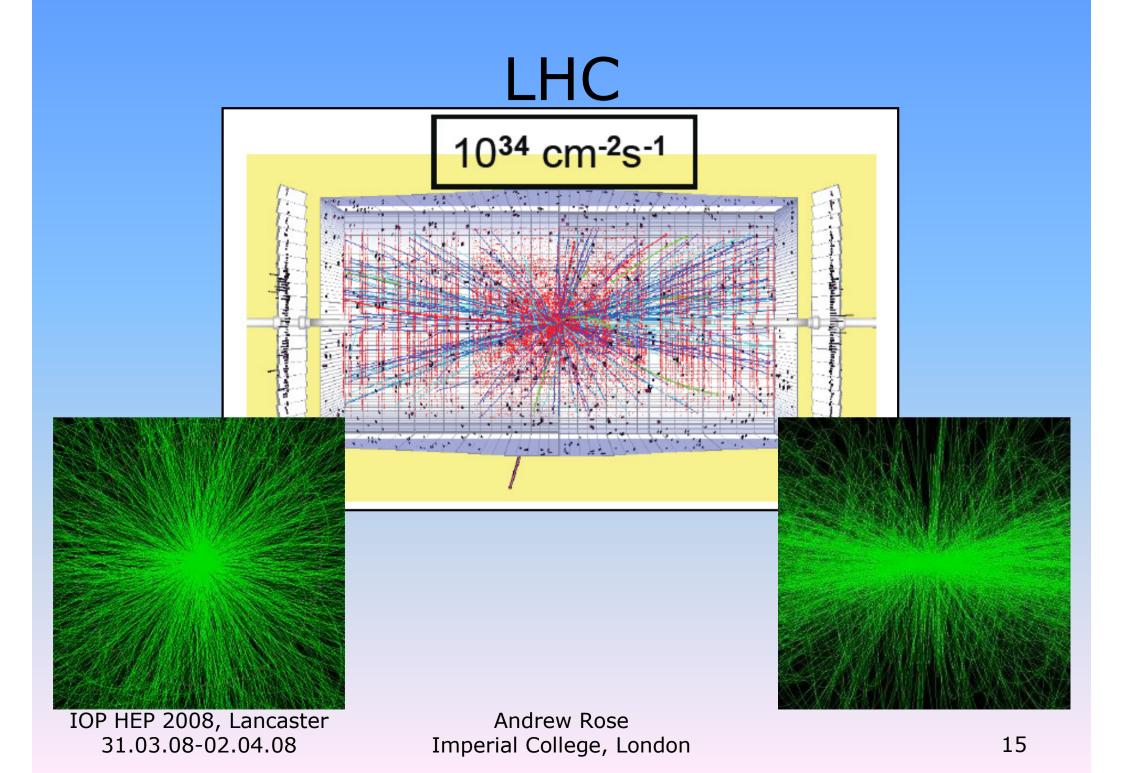
- µTCA backplane
- Ethernet control bus
- •A general purpose data processor @ 50Gbit/s

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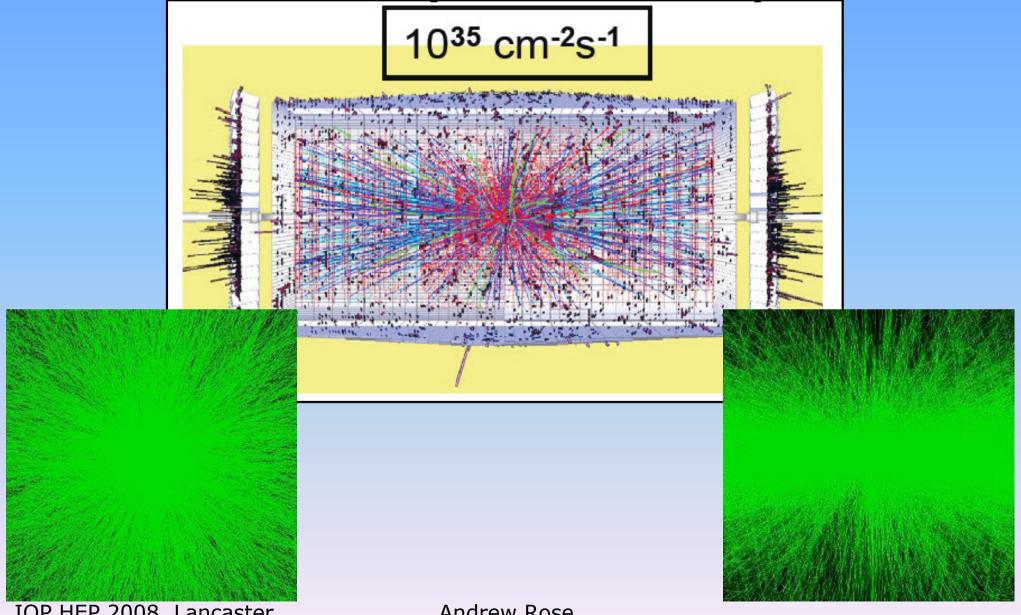
- Xilinx Virtex-5 FPGA (a)
- 72 x 72 non-blocking crosspoint switch (b)
- 20 x 2 3.2Gbit/s backplane connections (c)
- 16 x 2 3.2Gbit/s optical connections (d)

So what's to come...

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SLHC (circa 2015)



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10³⁵ cm⁻²s⁻¹

With increased luminosity the calorimeters lose the ability to separate jets/e/ γ from QCD background!

Need tracking information (see M. Pesaresi, next...)

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How to proceed: the philosophy

- Like current trigger:
 - Layer by layer approach
 - Combine at the very end
- Physics-like approach:
 - Particles 'flow' radially, can trigger behave similarly?
 - Use fine granularity data to create precision objects (or even 'events')
 - The downside: Raw trigger data from a minimal detector upgrade would top 15Tbit/s.

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How to proceed: the hardware

- Like current trigger:
 - A vast collection of assorted electrical, mechanical and optical standards with absolutely no flexibility
- GCT (esp. matrix processor) approach:
 - Flexibility! Flexibility! FPGAs and optical patch panels
 - Standardization (with industry) of back planes, control buses and links
 - Design process moves from hardware to firmware. Cheaper, faster and more easily maintained

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Conclusion

The CMS Global Calorimeter Trigger is in the final stages of commissioning ready for LHC start-up

In the process of constructing the GCT, a general purpose processing card capable of handling 50Gbit/s has been designed and built with the emphasis on flexibility and design quality

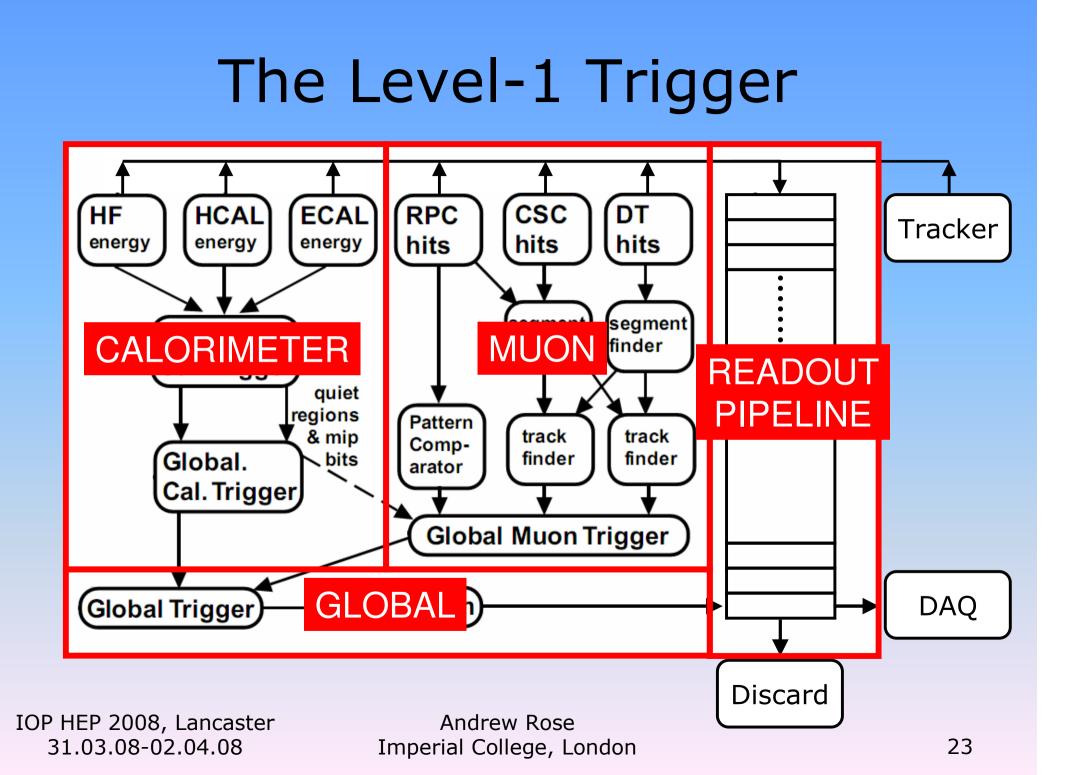
Studies are ongoing as to whether this, or similar, hardware could be used to handle fine granularity data for triggering at the SLHC

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Extra slides

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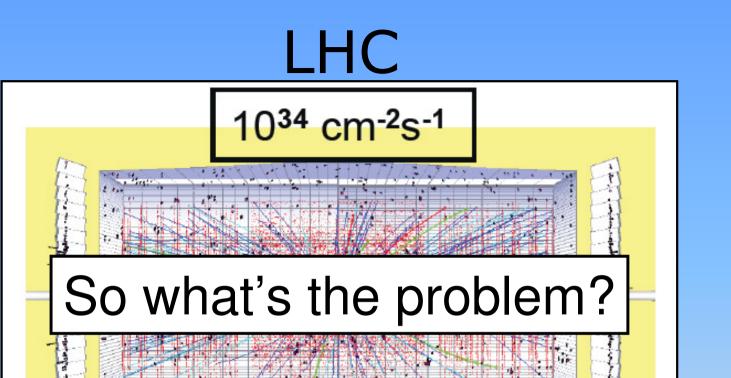


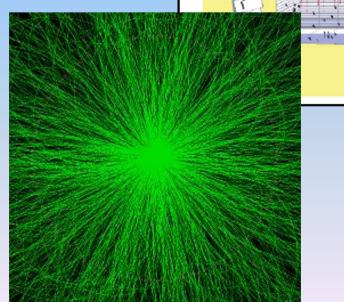
How is this done?

- By summing (eg crystals into towers, towers into regions, regions into super-regions = `candidates', etc)
- By ranking and accepting only highly ranked objects
- Parallelised comparison of data against stored patterns
- All ASIC/FPGA based custom hardware
- No iterative algorithms (too slow)
- No tracker information (too slow)

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- For political reasons, the last part of the trigger chain to be built
- As such, could take advantage of new technologies
- Built around large FPGAs (Xilinx Virtex-2, -4 & -5)
- Follow the lead of the communications industry
- Uses high speed serial links rather than large parallel buses





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