CMS Strip Readout Architecture for SLHC

OUTLINE

brief review of LHC strip readout architecture
proposed architecture for SLHC
front end amplifier design in 130nm
system architecture ideas
triggering possibilities with strips
summary

Mark Raymond – Imperial College London

ACES workshop, March 2009
CMS LHC Si strip readout system

**analog optical receivers**

**analogue readout**

APV25 0.25 $\mu$m CMOS FE chip
APV outputs analog samples @ 20 Ms/s
APVMUX multiplexes 2 APVs onto 1 line @ 40 MHz
Laser Driver modulates laser current to drive optical link @ 40 Ms/s / fibre
O/E conversion on FED and digitization @ ~ 9 bits (effective)
CMS LHC strip readout system

LHC strip readout system actually rather simple – breaks down into 3 components

**FRONT END CHIPS**
- APV25

**DATA MERGER**
- APVmux – multiplexes outputs of 2 APVs onto one line

**OFF-DETECTOR LINK**
- analogue – APVmux output drives laser driver => 2 APVs per off-detector fibre

System simplicity comes from choosing not to zero-suppress (sparsify) on front end
LHC control / readout chain overview

- ~75,000 APVs
- Fast control (CK/T1) digital opto-link
- Readout analog opto-link
- FEC
  - APVE
  - T1
- FED
  - Predicted digital header
- Trigger control system

No zero-suppression (sparsification) on detector

- All 75,000 APVs operating synchronously (all FE chips doing same thing at same time)

Advantages

- Can be emulated externally (APVE) to prevent APV buffer overflows
- No need to timestamp on front end
- Data volume occupancy independent
- Easy to identify upset chips (digital header)

- Pedestal, CM subtraction and zero suppression on FED
- Raw data also available for setup, performance monitoring and fault diagnosis

Analog, unsparsified readout provides relatively simple and robust system
SLHC challenges for CMS tracker

1) power
   higher granularity => more FE chips
   electronics related material dominates existing material budget
   (cabling, cooling) & we want to reduce this

2) triggering
   not possible to keep L1 trigger rate at 100 kHz without
   contribution from tracker

=> new features and existing architectures need re-design
   and replacement

what we like about our present system
   analog pulse height info
   made possible by custom analog off-detector link
   no on-detector sparsification
   system simplicity - no fluctuating data volumes event-to-event

what must change for SLHC
   off-detector links -> high speed digital
   => digitization on FE if want to retain pulse height info

will look at pros and cons of different FE chip architectures
LHC front end chip architecture

existing LHC architecture – APV25
slow 50 nsec CR-RC FE amplifier, analog pipeline, 2.7 mW/channel

peak/deconvolution pipe readout modes
peak mode -> 1 sample -> normal CR-RC pulse shape
deconvolution -> weighted sum of 3 consecutive samples combined to give single BX resolution

all analog approach – not compatible with digital off-detector data transmission
moving to SLHC – if want to retain pulse height information – where to digitise?
**“digital APV” architecture**

**digitization before pipeline?** (on every channel)
- early assumptions said no – ADC power too high (ITRS 2003)
  - still valid? - maybe not in future processes (90 nm, 65 nm)
  - some new ADC architectures beating previous power predictions *
  - but negligible power / channel still some way off

**digitization after pipeline?**
- negligible power/channel is achievable - ADC power shared between all front end channels
- analog pipeline remains so could retain slow shaping + analog deconvolution approach
  - but this architecture still brings some disadvantages

---

*see - A. Marchioro - http://indico.cern.ch/getFile.py/access?contribId=26&resId=0&materialId=slides&confId=41832*
digital APV architecture disadvantages

- FE amp
- Analog pipeline
- Pipe readout
  - Analog MUX
- ADC
  - CM subtract + sparsify?
  - Slow control, bias, test pulse, ...
- Serialize + O/P driver
- Off-chip

Very complicated chip – all the complexity of APV + more
- Fast ADC required
- Data volume means sparsification necessary to keep data at manageable levels
- On-chip CM subtraction probably necessary (analog pipeline contributes)

Analogue pipeline using gate capacitance may still be possible in 130nm – not in finer processes
- (Plan to increase pipeline length for SLHC)

Analogue circuitry throughout chip – harder to achieve supply noise rejection

Sparsification leads to on-detector system complexity
- Extra buffering required (more chips) to cope with varying trigger-to-trigger data volume
- Front-end timestamping

If want to keep simple un-sparsified system => pulse ht. info has to go => binary
**binary architecture – un-sparsified**

**what about binary un-sparsified?**

**much** simpler (than digital APV) particularly for pipeline and readout side

need fast front end and comparator => more power here

but no ADC power and much simpler digital functionality will consume less – this architecture **will** be lowest power

binary architecture also compatible with some approaches to track triggering layers

**can retain system features we like**

- simpler synchronous system, no FE timestamping
- data volume known, occupancy independent (no trigger-to-trigger variation)

**un-sparsified binary is the option we are currently planning to implement**

**but** less diagnostics (can measure front end pulse shape on every channel in present system)
- loss of position resolution
- common mode immunity
front end amplifier design

binary FE design has begun in 130 nm CMOS

preliminary specifications and assumptions

n-on-p sensor (signal current flows out of amplifier)
  promising option for rad hard sensors

need to tolerate leakage current up to ~ 1 μA
  allows DC coupling for lower cost sensors

need to be fast enough for acceptable timewalk
  aim for peaking time ~ 20 nsec
130nm front end amplifier

Current preferred architecture for fast FE (~20 ns peaking)

Preamp
- NMOS I/P device
  - No noise penalty - 1/f corner low enough (simulation & published measurements)
  - Better connection to sensor for PSR (sensor bias decoupling and I/P FET source both at GND)
- Real resistor feedback
  - Low Rpf (200k) allows DC leakage to be accommodated (1 \( \mu \)A -> 200 mV)
  - Uses highest resistance technology in process (1k7/square poly, +/-20%)
  - \( \frac{Rpf}{Cpf} = \frac{200k}{100fF} = 20 \text{ ns decay time constant of preamp (no pile-up)} \)
  - 200k contributes \( \sim 220e \)

Postamp
- Provides gain & risetime provides integrating time constant
- AC coupled to preamp (DC shift due to leakage decoupled)
- O/P DC level set by \( V_{\text{REF}} \) - defines DC level at output (comparator input)

Will show some simulated performance pictures – all results at preliminary stage
binary FE pulse shape and noise

pulse shapes for 4 fC input charge
(\sim 45 \text{ mV} / \text{ fC})

pulse shape tuned to keep peaking time \sim constant as \( C_{\text{SENSOR}} \) varies by increasing current in input FET (\( I_{\text{DS}} \))

preamp risetime \( \propto \frac{C_{\text{SENSOR}}}{g_m} \) (\( \propto \frac{C_{\text{SENSOR}}}{I_{\text{DS}}} \))

\Rightarrow \text{power scales linearly with } C_{\text{SENSOR}}

noise < \sim 900e \text{ for power } \sim 200 \mu\text{W} \text{ for } C_{\text{SENSOR}} \sim 6 \text{ pF}

always a trade-off between power and noise

e.g. thin sensors (< 4fC/mip) or long strips will need more power to achieve acceptable S/N
Effects of leakage current

Postamp output unaffected (AC coupled)

Preamp output shows DC shift across $R_{PF}$

1 $\mu$A leakage contributes $\sim 440e$ noise to be added in quadrature to amplifier noise (short shaping time helps with parallel noise)

e.g. $900$ (total amplifier for $C_{SENSOR} \sim 6 \text{ pF}$)

$+ 440$ (leakage)

$\approx 1000e$ total
response to overload

overload behaviour well-controlled

low $R_{PF}$ beneficial

front end recovers from 4 pC signal and sensitive to normal signals within 2.5 $\mu$s

=> no “APV-like” hips effect
baseline choice for CMS tracker powering is parallel powering (DC-DC) so PSR will be an issue

power supply rejection at postamp output to sinusoidal waveform on positive supply rail

bare response shows good rejection at low frequency, peaking at ~10 MHz

AC preamp/postamp coupling together with opamp postamp gives good low f behaviour

peaking at ~10 MHz (gain) due to coupling through bias circuits

can improve with realistic filtering, but would prefer some rejection at all frequencies to start with

needs further study
power estimate

130nm binary chip – non-sparsified readout

0.5 mW / channel seems like an achievable target (c.f. 2.7 mW for APV25)

<table>
<thead>
<tr>
<th>Component</th>
<th>Power / channel</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>preamplifier/postamp</strong></td>
<td>180 μW</td>
</tr>
<tr>
<td>e.g. 20 nsec peaking time, short strips $C_{\text{SENSOR}} \sim 5pF$</td>
<td></td>
</tr>
<tr>
<td><strong>comparator</strong></td>
<td>20 μW</td>
</tr>
<tr>
<td>estimate from preliminary simulations</td>
<td></td>
</tr>
<tr>
<td><strong>miscellaneous digital</strong></td>
<td>60 μW</td>
</tr>
<tr>
<td>estimate loosely based on APV pipe and control logic</td>
<td></td>
</tr>
<tr>
<td><strong>mux + output driver + ....</strong></td>
<td>240 μW</td>
</tr>
<tr>
<td>just guess nominal figure to bring overall power to 0.5 mW</td>
<td></td>
</tr>
<tr>
<td>will depend on implementation. e.g. choice of electrical protocol</td>
<td></td>
</tr>
<tr>
<td>can hope for saving here, but good to have contingency</td>
<td></td>
</tr>
</tbody>
</table>

digital is biggest uncertainty, and maybe largest contributor

can consider running at lower voltage (dig. power ~ $V^2$)

should keep power rails separate on chip to keep option open
full prototype in 1st iteration

relative simplicity of unsparsified binary architecture means can go for complete chip on timescale ~ 1 year
less risky than complex “digital APV”

will learn a lot sooner rather than later
will also provide collaborators with something to use to evaluate sensors and modules

choose front end most likely to suit SLHC (e.g. n-side readout?)
(can still submit test structures for alternative front ends)

**CBC (CMS Binary Chip)**

may leave out some features
  e.g. bias gen., test pulse, I²C I/F

but should have main functionality:
  pipeline, pipe control logic, and mux.,
  trimDAC for comparator thresholds,
**LHC -> SLHC strips readout system**

Recap LHC
- APV provides analogue unsparsified output data at 20 Ms/s
- Data frame 7 μs => 70% of off-detector bandwidth used for 100 kHz trigger
- 2 APVs data interleaved at 40 Ms/s on one electrical line (differential)
- One-to-one correspondence to off-detector fibre (i.e. still 2 APVs / fibre)
- Link power <10% overall channel power
moving to SLHC - early ideas
binary unsparsified, but output frame format can be similar to APV (just hits, not analog values)
CBC could provide output data at \(20\ \text{Mb/s}\)
keep data frame \(~7\ \mu\text{s}\)
\(\Rightarrow4\ \text{CBCs data multiplexed at} \ 80\ \text{Mb/s} \) onto one electrical line (GBT lane)
\(32\times80\ \text{Mb/s} \) lanes combined on \(2.56\ \text{Gb/s}\) off-detector fibre (128 CBCs / fibre)
link power \(~20\%\) overall channel power (assumes 2W / link)
LHC strips readout & control system

CCU distributes CK/T1 and I²C control busses to up to 16 FE modules
PLL chip recovers CK and T1 (missing clock pulse) on FE module
DCU chip monitors FE currents, voltages and temperatures
I²C used for programming APVs, reading DCU monitoring info, setting up AOH

CCU chip electrical control ring architecture on front end reduces no. of control fibres required
SLHC strips readout & control system

128 CBCs / GBT

system design here is not yet well defined (my thoughts here)

should be much simpler (on-detector) than LHC system
  e.g. could combine mux/PLL/DCU functionalities in one chip?

GBT based system means GBT + whatever else is needed (if anything)
  does this map to current GBT functionality?

I²C and CK/T1 could be common to a number of FE modules
Track Triggering

two concepts compatible with microstrip tracker

Cluster Width Discrimination

Two-In-One Design
bond stacked upper and lower sensor channels to adjacent channels on same ASIC
no interlayer communication - no extra correlation chip
just simple logic on readout chip, looking at hits (from 2 layers) on adjacent channels

W. Erdmann
R. Horisberger *

Cluster Width Discrimination
high \( P_T \) track -> narrow cluster width
see: Track momentum discrimination using cluster width in Si strip sensors, G. Barbagli, F. Palla, G. Parrini, TWEPP07

Pt - Trigger for TOB layers
“Two-In-One” Design

*http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580
triggering logic on FE chip

simple logic to select cluster width (programmable) (or coincidence window between layers for 2-in-1)

binary FE required
comparator needed to feed trigger logic

system architectures are evolving
e.g. further ideas to combine clusters in data concentrator chip before transmission off-module, see:
summary & plans

main SLHC design challenges are power and triggering

current plans for CMS strip tracker are:

binary unsparsified architecture
lose pulse height info, but retain some system features we like
should offer lowest possible FE chip power

full-size 130nm chip on first iteration – hope to submit this year
front end amplifier already under design – other parts will begin soon
specifications at preliminary stage – will develop over coming months

binary architecture already compatible with some track-trigger approaches under consideration
relative simplicity of readout scheme should allow to free-up resources to help develop
track-trigger solution (“two-in-one”, cluster-width, or stacked pixels)

=> more chips to develop

final words

time is short – chip and system design process is just the start, shouldn’t forget many issues to confront:
testing – bare chips and modules
new powering schemes, SEU immunity, low temperature operation,…
assembly techniques may differ from past (wire -> bump-bonding?)
chip production: more chips than in past – longer test time and/or more test equipment/centres
has to start some years (maybe 5?) before tracker installation