High rate effects on APV chips

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Summary

The effects of high event rates on the APV6 and APV25 amplifiers have been investigated by injecting charge at high rates into one amplifier channel and observing the effect on the amplifier output pulse shape. The charge is injected by applying a stepped (staircase) waveform to a known value charge injection capacitor. The step heights are adjusted to be equivalent to 1 mip pulses and the interval between steps is 500 nsec., corresponding to a channel occupancy of 5% by 1 mip signals. The dependence of pulse shape on the step from which it originated is investigated.

Both types of APV chip use conventional circuits for the charge preamplifier stages, the charge being integrated on a feedback capacitor for which a discharge path is provided by a resistor implemented by a FET. The FET resistance can be controlled by means of its gate voltage which is programmable via the I2C slow control bus. The value for the gate voltage is denoted as $V_{pre}$ for the APV6 and $V_{fp}$ for the APV25. It is important to choose an appropriate value for this parameter to avoid adverse effects at high rates.

Four plots are included here, two for each chip type. The effects are qualitatively identical for each chip type, only the magnitudes and names of the feedback resistor gate voltages being different. The "pulse shape dependence on step number" plots show pulse shapes for all steps of the charge injection pulse train superimposed in both peak and deconvolution modes for two different values of the feedback resistor voltage. For the lower value of this voltage the only effect noticeable as a function of step number is a pedestal shift in peak mode. This is much reduced in deconvolution mode which is the mode which would be used for high rate conditions. For the higher value of the feedback resistor voltage a pulse height reduction with step number is evident, resulting from the preamplifier output clipping as it reaches the limit of its voltage range.

The "pulse height dependence on step number" plots show the amplitudes of the output pulses (pedestals subtracted) as a function of the step from which they originated, for a range of values of the feedback resistor voltage. The plots indicate that, for the input signal rates simulated here, there is a range of values for the feedback resistor control voltage for which there are no significant pulse height reduction effects.

The results here have been verified by SPICE simulations and indicate that there is no need for serious concern about the operation of APV chips in signal rate conditions consistent with those expected in CMS. Nevertheless it is clear that there are some high rate pedestal effects which will dictate the required mode of operation of the chip in the experiment, and which would benefit from further study in more realistic conditions.
High Signal Rate Effects on APV Amplifiers

Amplitude limiting effects observed in APV6 by Florence group

results presented last tracker electronics meeting
A.Buffini (18th April, 2000)

~ 30% reduction in signal amplitude reported for signal rates consistent with high CMS occupancies

Not clear where/why amplitude limiting occurring (charge preamp?) and/or whether this may also occur in APV25

Phenomenon investigated for APV6 and 25 using simulation (HSPICE) and experimental methods.

close agreement between simulation and measurement
-> concentrate on measurements here
Conventional charge preamplifier designs

feedback capacitor discharge path provided by long/narrow channel FET,
gate voltage adjustable (via I2C) to obtain suitable value of resistance

note feedback resistor control voltages named differently
VPRE for APV6, VFP for APV25

APV6/APV25 designs broadly very similar

Important to choose value for VPRE/VFP to avoid pile-up effects
Choice of feedback resistor gate voltage

High signal rate => lower feedback resistance required

e.g.

At preamp quiescent point FET resistor Vd=Vs=input FET gate voltage

\[ \sim -0.5V \]

Feedback FET can operate in weak inversion but for lower resistance (high rate) VFP must be a threshold below -0.5V

\[ \text{i.e. } VFP \sim -1V \]

Similar analysis for APV6 gives VPRE > -0.3 V (NMOS FET resistor)
Choice of feedback resistor gate voltage (cont'd)

VFP (APV25) as function of I2C register value

![Graph showing the relationship between VFP (in mV) and I2C value.]

So for VFP < -1 V need I2C value of <~40 (decimal)

APV6: For VPRE > -0.3 V => I2C value <~140
(VPRE voltage decreases as I2C value increases for APV6)
Experimental Method

To simulate high rate signals use staircase waveform on charge injection capacitor connected to one channel
(essentially identical technique to that used in Florence)

Simulation conditions:

5% channel occupancy by 1 mip pulses
(1 mip pulse every 500 nsec)

By adjustment of timing between Staircase waveform trigger and APV trigger (T1) can examine pulse shape dependence on step from which it originated
APV25 pulse shape dependence on step number

Vfp=30, peak mode
pulse height independent of step no. but pedestal shift

Vfp=30, deconvolution mode
pulse height and pedestals independent of step no.

Vfp=60, peak and deconvolution mode
pulse height reduction with increasing step no.
**APV6 pulse shape dependence on step number**

**Peak**

- $V_{pre}=140$, peak mode
  - Pulse height independent of step no. but pedestal shift

- $V_{pre}=170$, peak mode
  - Pulse height reduction with increasing step no.

**Deconvolution**

- $V_{pre}=140$, deconvolution mode
  - Pulse height and pedestals ~ independent of step no.

$V_{pre}=140$, all steps overlaid
APV6 pulse height dependence on step no.

Onset of high rate pulse height limiting occurs somewhere between values of 150 and 170 for Vpre.
APV25 pulse height dependence on step no.

Onset of high rate pulse height limiting occurs somewhere between values of 30 and 50 for Vfp.
Conclusions

Experimental measurements (and SPICE simulations) indicate that APV chips can tolerate high signal rates without loss of amplitude provided an appropriate choice of preamp feedback resistor control voltage is made.

Nevertheless pedestal effects are observed, more significantly in peak mode - would benefit from further study in realistic conditions (beam).

Recommended choice of values to avoid high rate effects:

- APV25: VFP < 30 (user manual recommends 67)
- APV6: VPRE < 150 (user manual recommends 150)