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R&D in preparation for an upgrade of CMS for the Super-LHC

1 Executive Summary

The proposal was approved in Spring 2008, and funding announced in January 2009. There have been major funding problems for STFC during this entire period, which have limited our activities and ability to plan. However, significant progress has been made with all three work packages.

The three work packages are WP1: simulations of detector design, WP2: development of a readout system for the outer part of the new tracker, WP3: developments of calorimeter trigger hardware.

The PI is G. Hall. Work Package managers are WP1: D. Newbold; WP2: G. Hall with M. Raymond, C. Hill and J. Coughlan; WP3: C. Foudas.

The total cost of the 3.5 year R&D programme is £3.88M, which includes funding for existing staff and new appointments, including students. Materials costs, mainly for ASIC submissions and trigger hardware comprises £639k.

The work is well integrated into the Tracker and Trigger projects, where several individuals (Hall, Foudas, Newbold) have taken responsibilities and there are regular reports at many internal CMS meetings.

There have been significant changes to LHC operational plans, including anticipation of machine upgrades, since project approval. The operational and upgrade plan for the next few years was presented to CERN staff and users on 5 February 2010 following the recent 2010 Chamonix workshop.

The future budget for the project was reviewed in the recent STFC Council prioritisation exercise, and the outcome was reported to us on 5 February 2010.

A revised plan and reprofiled budget will be prepared in the near future to match the new circumstances.

2. Project history to date

The original proposal was submitted to STFC in October 2007. A review in January 2008 proposed modest changes to reduce costs of Work Packages 1 and 3, submitted as an Addendum in March, which was then recommended for approval. Unfortunately, the economic environment became very unfavourable and this led to some significant complications, which still persist and have affected long term planning.

First, STFC financial problems from December 2007 delayed financial allocations until January 2009 when the formal announcement of the grants was made. Although we had known the award was imminent for many months, it proved hard for STFC to predict accurately when the grants would start and, even more important, no commitments could be made by universities or RAL Technology Department until the funding was definite, especially appointments of new staff and allocation of engineering effort for ASIC design.

During the period from December 2007 until mid-2009 there were freezes on appointments of RAL staff and uncertainties about the ability to replace staff and to appoint to new posts. All of these factors significantly reduced effort planned in the original rolling grant until early 2009. Finally the announcement of the allocation of RAL funds for the year 2009-2010 (mainly engineering staff costs but also consumables and travel) reached us in mid-August 2009, i.e. half way through the financial year, which did not make planning very easy.

Meanwhile the rolling grants round of 2009 took place under difficult circumstances and the announcement of grants was made in September 2009, for just one year. In December 2009, we were informed of cuts to approved projects but, for announced grants such the CMS upgrade, with no clear indication of how the cuts would be implemented. On 5 February 2010, we were informed by STFC

"For the CMS Upgrade project, I am pleased to be able to confirm that support for the current R&D phase of the project will be maintained at its existing approved level. The planning provision for future phases of the CMS Upgrade has however been re-profiled in line with the recommendations of PPAN (and may need to be revisited again particularly with the further slow-up in the LHC schedule."

Thus, in reality, revising the planning of this project has been difficult and there has not yet been sufficient time to prepare a new plan which reflects the available resources or expected duration.

We emphasise that we fully understand that STFC has been operating under extremely difficult circumstances for the last two years and there is no intention to criticise the STFC administration.

2.1 LHC upgrade schedule and planning

At the time of the original proposal, in October 2007, the plans for the LHC machine upgrade were not worked out in detail, except that the improvements needed to the accelerator complex were identified and the stages could be envisaged. The goal was to achieve a luminosity of 10^{35} $cm^{-2}.s^{-1}$, an order of magnitude higher than the nominal LHC maximum.

In January 2008, the CERN DG explained that the machine upgrade was foreseen to proceed in two stages: Phase I, which would increase the luminosity to 2-3 x 10^{34} $cm^{-2}.s^{-1}$, and Phase II, which would deliver the full upgrade. Approximate dates for both phases were indicated but were evidently contingent on CERN Council approval which would require physics cases and financial approval. Since that time there have been some significant developments affecting the upgrade schedule.

In September 2008, the LHC was operated for the first time followed by the well known machine incident instigated by a quenching superconducting splice connector which led to significant damage to the machine.

In November 2009, the LHC was ready for restart which took place very successfully with first collisions at 900 GeV and 2.36 TeV centre of mass energy in December.

The latest Chamonix LHC workshop took place in late January 2010 which defined the immediate plans for LHC operation and outlined the likely growth of luminosity and operational scenario in the coming years. It is now foreseen that the LHC will operate at 7 TeV centre of mass energy for 2010 and 2011, with a lengthy shutdown to replace most or all of the splices before continuing to 14 TeV. It is possible the collision energy will increase above 7 TeV in 2011, but this will depend on practical considerations and experience during 2010 operation, including resources. The LHC might achieve 50 fb^{-1}/year and 100 fb^{-1} integrated luminosity by 2016. It might reach 100 fb^{-1}/year after 2019. Better estimates are expected after the first complete year of operation. These estimates are very different than the scenario foreseen, albeit with significant uncertainties, in October 2007, at the time of the original upgrade R&D proposal.

Although much of this is not unexpected, these firmer predictions of the progress of the machine have only been made public in the last couple of weeks. CMS foresaw gradual improvement to some parts of the experiment, such as the HCAL, parts of the muon system and trigger, which depend weakly on luminosity increases. Other sub-detectors, such as the pixel system, were foreseen to require replacement when the integrated luminosity reached 100-200 fb^{-1}. Complete replacement of the Tracker was expected to be required after about 500 fb^{-1}.

The R&D proposed by the UK groups remains highly relevant but should be focussed and adapted to the new schedule and evolution of overall CMS planning. The original LHC schedule was highly aggressive and allowed relatively little time for much of the R&D necessary for the very demanding SLHC conditions to be completed thoroughly and to adapt it, as undoubtedly will be required, to the physics discoveries which are expected.

However, the Phase II upgrade which foresaw replacement of the Tracker and use of Tracker data in the trigger is more distant in time than originally envisaged and the likely timing of Phase I motivates another careful look by the CMS Tracker collaboration at the planning of the replacement pixel detector. The UK R&D activities were intended to allow the UK to continue to have a significant impact on the detector to best enhance it for new physics opportunities and this will remain our goal.

3. Work Package 1: Tracker and Level-1 Trigger Simulations and Software

3.1 Objectives

WP1 covers simulation of upgraded CMS tracker and L1 trigger systems, particularly for the inclusion of tracking data into the L1 trigger decision. The work therefore has investigation of potential architectures and technologies for a tracking trigger as a primary focus.

The top-level work package goals are as follows:

1. Development of new tools for simulation and optimisation of upgraded tracker and trigger systems in a very high luminosity environment.
2. Investigation of tracker layouts and inclusion of tracking data into the L1 trigger decision.
3. Support via simulation for specification, design and testing of prototype hardware systems.
4. Assessment of the performance of selected tracker and trigger designs against realistic background conditions and physics requirements, after LHC start-up.

Delays in funding resulted in a late start, with around nine months funded work completed to date. There is now around 3FTE of post-doc effort in this area, with contributions from academics at all institutes. Further academic, post-doc and student effort will join the project during 2010. The activities depend considerably on new appointments so this work package has suffered even more than others from staff availability.

We report below on progress against milestones for project months 0 – 12, noting that a substantial fraction of the foreseen effort in the original plan has not been available to the project so far. Progress against deliverables has been steady, though the project has evolved to take account of new ideas within the tracker and trigger communities.

3.2 Progress to date

Key achievements in WP1 to date include the following:

5. Definition of the tracker-trigger simulation interface and coordination of the overall trigger simulation effort, including coordination with offline and computing projects. The UK now provides the upgrade offline co-convenor.
6. Studies of reconstruction of electron momentum at high pile-up (200) using track stubs and tracklets produced by 1, 2 or 3 layers of a stacked tracker detector.
7. Studies of trigger layers in the most general proposed upgrade geometry, which is an evolution of the existing tracker design (‘hybrid geometry’), including evaluation of transverse momentum thresholds, trigger efficiencies and rate and occupancy studies using a detailed detector model with a realistic material budget.
8. Completion of an ultra-fast four-vector level simulation tool to allow rapid assessment of the performance of stacked-layer tracking trigger over a wide range of parameters (tracker geometry, number and placement of pt layers, sensor spacing and granularity). Demonstration of a hardware-realistic algorithm for track parameter (pt, eta, phi) estimation by global correlation of local tracker stubs in track roads, and estimates of performance of stacked layer triggering in a realistic endcap geometry.
9. Testing and basic validation of fast- and full-simulation geometries of a range of proposed tracker layouts. This detailed software work is essential to allow robust estimates of the overall tracking performance at high luminosities. Recent work has included the porting of tracker geometry and reconstruction code to the latest versions of CMSSW, and investigation of approximations made in simulation of out-of-time pileup.
10. Provision of large simulated samples for use by tracker and trigger upgrade study groups. This required the integration of previously separate threads of development in tracking, track trigger and calorimeter trigger simulation, and the development of new Monte Carlo production tools to allow the use of very large memory computing resources in the UK and elsewhere.

Areas where progress has been less rapid than originally foreseen include the definition of agreed SLHC benchmark physics channels, and the incorporation of realistic background estimates from LHC data. In both cases, the rate of progress is coupled to the delayed LHC programme.

As a realistic schedule for the Phase II upgrade of CMS becomes clear, it is appropriate to revisit the emphasis and immediate goals of WP1. Whilst the overarching mission – to support the design and optimisation of upgraded tracker and trigger systems – will not change, it will be necessary to target our work at those aspects of the upgrade programme which reflect CMS priorities for the foreseeable future, which is dominated by Phase I of the LHC upgrade.

To this end, we have already started to explore opportunities in online and offline software aspects of the Phase I pixel and calorimeter trigger upgrades. Much of the experience gained over the last year can be directly applied in these areas. In both cases, UK collaborators with appropriate expertise are already working within the project. Phase II simulation studies which are under way will be completed and published, and this strand of R&D will continue at a lower level within the project, effort permitting.

3.2 Staff on project

Trigger studies: D. Newbold (Bristol, WP manager, 25%); R. Frazier (Bristol, 100%); K. Harder (RAL, 50% from Q309); A. Rose (Imperial, STFC funded student to Oct 2009); J. Brooke (Bristol, 10%)

Tracking studies: J. Goldstein (Bristol, 25%); M. Grimes (Bristol, 100% from Q409); I. Reid (Brunel, 50%), M. Pesaresi (Imperial, STFC funded student to Oct 2008, self-funded to Oct 2009).

Significant academic contributions have also come from C. Shepherd-Themistocleous (RAL), I. Tomalin (RAL), G. Hall (Imperial), C. Foudas (Imperial), P. Hobson (Brunel).

3.3 Expenditure

The expenditure to date is dominated by staff costs, with limited travel.

4. Work Package 2: Outer Tracker Readout

The objectives of WP2, stated in the original project proposal, are to develop a readout chip suitable for the outer tracker, to study options for providing level 1 trigger data, and to contribute to the development of a complete readout system including the off-detector components.

4.1 Front end chip

We have begun our development of a readout chip for short silicon microstrips (2.5 – 5 cm) which could be used in the outer tracker region (r > ~50 cm). As reported in the May 2009 CMS Upgrade Workshop [4.1], short strip outer layers would not contribute to the level 1 trigger. This chip is envisaged to form part of a system where tracking information would be provided by dedicated PT layers.

We have converged on an unsparsified binary readout architecture for reasons of chip and system simplicity, and we believe this should offer the lowest possible power consumption. In the original proposal a more complicated front end was still under consideration which would have required at least two years to develop. We now propose to submit a full chip prototype (128 channels) on the first iteration.

Design of the CBC (CMS Binary Chip) started in March 2009. Specifications have been developed and presented to the CMS Tracker community [2, 3]. The chip is being designed in 130 nm CMOS in a collaboration between Imperial College and RAL TD. Only one RAL engineer was available to be allocated to the project, though there were resources awarded for two.

The front end amplifier has been designed to match both possible sensor polarities, and can tolerate DC leakage currents up to 1 μA.

We have agreed to submit this chip for fabrication in a CERN organized MPW run in May 2010, with chips available ~3 months later. The cost will depend on the number of designs sharing the MPW run, but an upper limit for a projected chip size of 7 x 4 mm^2 is expected to be ~£54,000.

Most of the chip is now designed, and large parts have already been laid out. The current status is summarised in table WP2.1. The on-chip test pulse facility is designated as lower priority, since testing will not be compromised by its absence, but will be included if there is time.

Table WP2.1. CBC design progress (green indicates completed)

functional block	design complete (or expected completion date)	layout complete (or expected completion date)	comment
preamp			
postamp			
comparator			
comparator offset adjust			
pipeline interface logic			
pipeline + event buffer			
pipeline control logic			
output multiplexer	26/3/10	1/4/10	
fast control	5/3/10	12/3/10	
slow control – I2C		11/2/10	
bias generator		19/2/10	
test pulse	-	-	low priority – will include if time
on chip LDO regulator		9/4/10	
band-gap reference			CERN to provide
DC-DC switched cap conv.			CERN to provide
SLVS interface			CERN to provide
pads	16/4/10	23/4/10	

4.2 L1 trigger system

The importance of providing information to the level 1 trigger in CMS has stimulated a significant amount of activity within the international CMS tracker community, with working groups convened to identify and investigate plausible design concepts. We have been active in this area, as intended, although this work was originally scheduled for the second year of the programme. We are participating in, and coordinating, an international collaboration which is proposing to develop demonstrator prototypes of the stacked tracking concept, which originated at Imperial, and have proposed a possible module design [4]. This project has been presented in several conferences and workshops in the last year.

4.3 SFED developments

Due to a shortage of design effort at RAL there has been little development, or resource usage, for the off-detector readout. We have however had productive discussions with the group at CERN who are developing the common SLHC Gigabit links (GBT Project). In particular, we are converging with them on a strategy of using commercial FPGA development boards as a baseline prototyping platform. This approach would provide relatively low cost and flexible prototyping systems that can be customised for tracker readout link tests by the addition of custom-built plug-on cards (assuming industry standard FMC format). These systems could be common for both outer tracker and track trigger readout prototyping developments. We expect to have approximately 1 SY of design effort at RAL available to contribute to upgrade readout work starting in April 2010.

4.4 Power and module developments

Due to the delayed start of this project, comparative studies between powering schemes envisaged at the time of the proposal were rendered less relevant by the emergence of DC-DC converters as the CMS baseline. Instead we have contributed to the CMS Upgrade Powering WG by investigating alternative magnetic components for DC-DC converters that have intrinsically less stray field and EMI. In particular, we have prototyped and characterized a toroidal inductor fabricated in a printed circuit board. The toroidal shape reduces stray field and EMI, and use of printed circuit board technology allows higher integration of components. The toroidal idea has been adopted as the baseline by CMS.

We have also constructed a proof-of-principle transformer-based DC-DC converter with a planar transformer fabricated in a printed circuit board. Use of a transformer allows the step-down ratio to be increased with respect to a buck-converter whilst maintaining good efficiency. This reduces the power loss in the cabling. The EMI is expected to be lower than for the buck-converter based device.

A EMI test-stand has been assembled (current injection clamp, signal generator, RF amplifier current monitoring clamps and spectrum analyzer). This setup allows us to inject known amounts of noise enabling us to characterize the susceptibility to EMI of modules containing CBC chips powered by our prototype (or other) DC-DC converters.

4.5 Preparations for test-beam activities

Evaluation of modules in test beams will be needed, especially when trigger modules are developed. This task can be shared with other CMS collaborators, for example the study of a detector module read out by CBC chips. However, it is a lengthy task to prepare the ancillary equipment needed to instrument a beam test, in particular the data acquisition system and software, and it is profitable to begin now since many suitable items of equipment are, or can be made, available now but will not be so accessible in future being based on actual CMS hardware.

We are assembling the equipment needed to construct a beam telescope of up to 8 planes, which would measure two coordinates; four planes would be mounted upstream and four downstream. This requires CMS APV25 hybrids, optical links and opto-hybrids, a spare Front End Driver and the controls, which may be simpler than those deployed by CMS. We expect to use sensors from another project (D0) which have finer pitch than those used by CMS. The DAQ software will be derived from the CMS Tracker system under the supervision of J. Fulcher of Imperial, who is among the key responsibles for the CMS Tracker DAQ. We plan to use the setup in a test beam in September 2010 in collaboration with UA9 to allow measurements of crystal channelling.

In a later phase, we will develop the corresponding DAQ to read CBC modules, read with GBT and VOL high speed digital links.

At Bristol, we have procured a TTP board, designed to test VFAT2, which is a FE chip with similar functionality to the proposed CBC. We have obtained the circuit schematics, source-code for the firmware and the readout software possession of which will allow us to develop the TTP into a CBC test platform in time for the testing of the first CBC chips (and later modules).

4.6 Staff on project

G. Hall (Imperial-academic), M. Raymond (Imperial-research staff), M. Pesaresi (RA) and W. Ferguson (student) plus small fractions of support staff (finances: P Brambilla, who is also assisting with WP3, and C. Barlow, M. Khaleeq - technician). At Bristol C. Hill (Bristol-academic) and D. Cussans (Bristol- research staff) contribute, while at RAL J. Coughlan (systems group) and L. Jones (microelectronics) of TD are the staff presently involved.

4.7 Deliverables

Year 1

1) Documented system conceptual design and performance specifications

This deliverable is addressed in [4.2] and [4.3]. Although the outer tracker readout system cannot be specified in final detail at this early stage, we are converging on a system compatible with the CERN GBT off-detector link system. The baseline decision for CMS tracker powering is DC-DC, and some test structure options to explore this (on-chip low dropout (LDO) linear regulator, and switched capacitor DC-DC converter) will be included in the CBC prototype

2) Front end and other test structure circuits designed and submitted for fabrication, and test setups prepared.

Much of the design is complete; see table WP2.1. The decision to opt for a full-chip submission means that some aspects of this deliverable overlap with deliverable 2 of year 2. The planned submission date of the chip is May 2010, so chips can be expected in September. Test setups are already in the planning stage.

3) Documented results of preliminary investigations of powering schemes.

This deliverable is addressed in [4.5-4.9].

Year 2

1) Documented results of test structure evaluations.

2) Full chip prototype designed and submitted for fabrication and test setups prepared.

3) Final report on powering scheme tests.

Year 3

1) Review early results from tests of the full chip prototype will be reviewed to ensure functionality is adequate for the module and test programme planned for this year.

2) Documented preliminary chip results including outcome of review.

3) Documented results of prototype chip evaluation studies and prototype module and system tests.

4) Final pre-production chip designed and submitted for fabrication and test setups prepared.

Year 4 (additional 6 months)

1) Documented results of final prototype chip evaluation studies and prototype module and system tests.

4.8 Expenditure

In addition to staff costs, which include about 0.8 SY of RAL TD ASIC design effort so far, there has been modest materials expenditure of about £5k. This covers prototyping and test stands for powering studies, and ASIC development. The major forthcoming expense will be the estimated cost of a shared chip submission in May of approximately £54,000.

4.9 References

[4.1] CMS Upgrade Workshop, May, 2009:
http://indico.cern.ch/getFile.py/access?contribId=27&sessionId=6&resId=2&materialId=slides&confId=56210
[4.2] Tracker Upgrade Workshop, June, 2009:
http://indico.cern.ch/getFile.py/access?contribId=38&sessionId=8&resId=0&materialId=slides&confId=47292
[4.3] CBC Documentation web page: http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/
[4.4] WIT2010 Workshop on Intelligent Trackers, LBNL, February 2010.
http://indico.cern.ch/getFile.py/access?contribId=13&sessionId=4&resId=1&materialId=slides&confId=68677
[4.5] Tracker Week, February 2010:
http://indico.cern.ch/getFile.py/access?contribId=16&sessionId=2&resId=0&materialId=slides&confId=80949
[4.6] Tracker Upgrade Workshop, June, 2009:
http://indico.cern.ch/getFile.py/access?contribId=13&sessionId=9&resId=0&materialId=slides&confId=47292
[4.7] Tracker Upgrade Powering WG, February, 2009:
http://indico.cern.ch/getFile.py/access?contribId=6&resId=0&materialId=slides&confId=52199
[4.8] Tracker Upgrade Power & Readout Working Group, October, 2008:
http://indico.cern.ch/getFile.py/access?contribId=1&resId=1&materialId=slides&confId=41790
[4.9] Tracker Upgrade Joint Power & Readout Working Group, July, 2008:
http://indico.cern.ch/getFile.py/access?contribId=8&sessionId=1&resId=1&materialId=slides&confId=36581

5. Work Package 3: Design of Level-1 Calorimeter Triggers at the SLHC

5.1 Objectives of WP3

The objective of Work Package 3 is to develop a demonstrator for the off detector Level-1 Trigger (L1T) electronics for CMS at the SLHC as well as to pursue studies towards the development of new trigger algorithms using this system. This will place UK teams in a good position to claim the design and construction of a significant part of CMS Level-1 Trigger system at the SLHC. The UK team participating in this WP is Imperial College. The hardware development of WP3 was expected to complement the simulation activities of WP1, eventually leading to implementation of prototype track-trigger algorithms. However, the main focus in the three year programme was agreed to be the calorimeter trigger.

5.2 The Level-1 Trigger Demonstrator

Suitable platforms and standards for L1T systems have already been developed in industry. The most prominent example is the micro-TCA (uTCA) standard which is used by the telecom industry for applications requiring large data routing and processing. The data transfer capabilities of these systems are in the multi Gbps range. Hence, we have embarked on developing a small system around this standard. It consists of generic modular devices based on FPGAs and optical links and is the first prototype of off-detector trigger electronics for SLHC. The goal is to provide a standard device for all Level-1 triggering at the SLHC so that these modular devices can be used as platforms for all Level-1 triggers. As in the original proposal the new system consists of the following two main devices:

- A Main Processing Card: This receives data optically and runs different trigger algorithms depending on the application. The industry standard SNAP-12 family of optical receivers has been selected. Data will be processed on a large FPGA instrumented with 40 5Gbps transceivers. As with the GCT this system combines optical link transmission with modern FPGA processing capacity to provide a powerful computing device.
- The uTCA crate with a custom backplane: Up to 12 processing cards can be plugged into a uTCA crate whose backplane is customised to provide freedom for arranging links as necessary for physics applications. The custom backplane may employ two 72x72 cross-point switches.

The three-year demonstrator development program started in January 2009. As described in the original proposal and addendum of October 2008, progress is to be monitored using the following milestones:

1. Year 1:
    a. Design of the main processing card ready for production.
    b. Backplane design ready for layout.
    c. Preliminary version of the firmware ready.
2. Year 2:
    a. Working prototypes of processing card and backplane ready
    b. First uTCA demonstrator system (one card and backplane) ready.
    c. Results from the first preliminary algorithm tests
3. Year 3
    a. Algorithm performance studies complete
    b. Conference presentation of the results and publication

5.3 Progress during the first year of the project

Since January 2009 C. Foudas (Imperial-Academic), G. Iles (Imperial-engineer) and S. Greenwood (Imperial-technician) have been active in this area with J. Jones (PostDoc-Princeton) developing the first firmware versions. Recently A. Rose accepted an RA position assigned to WP3 with the purpose of working closely with G. Iles on trigger simulations, firmware and hardware development. Currently the group is experimenting with two systems:

The first system consists of two uTCA Matrix cards, which were designed and produced at LANL using UK funding, in a uTCA crate. The crate services are provided by a uTCA controller (MCH). This is a system originally designed for the CMS GCT (GCT Muon system) and is scheduled to be installed at CMS after the first year of running. In the meantime this system is used to develop the first demonstrator for a triggering system and to design the firmware framework (milestone-1-c). A number of firmware packages have been written, mainly on Ethernet-Control, Optical Link-control and actual trigger algorithms. We are collaborating with the University of Wisconsin CMS trigger group on both hardware and the trigger algorithms. Wisconsin has designed the DAQ interface (S-Link64/TTC) for this system. Work has been progressing in a satisfactory way and a first version of the system firmware has been completed, fulfilling milestone 1-c.

Fig. 1 shows a Matrix Card and uTCA crate with the associated hardware.

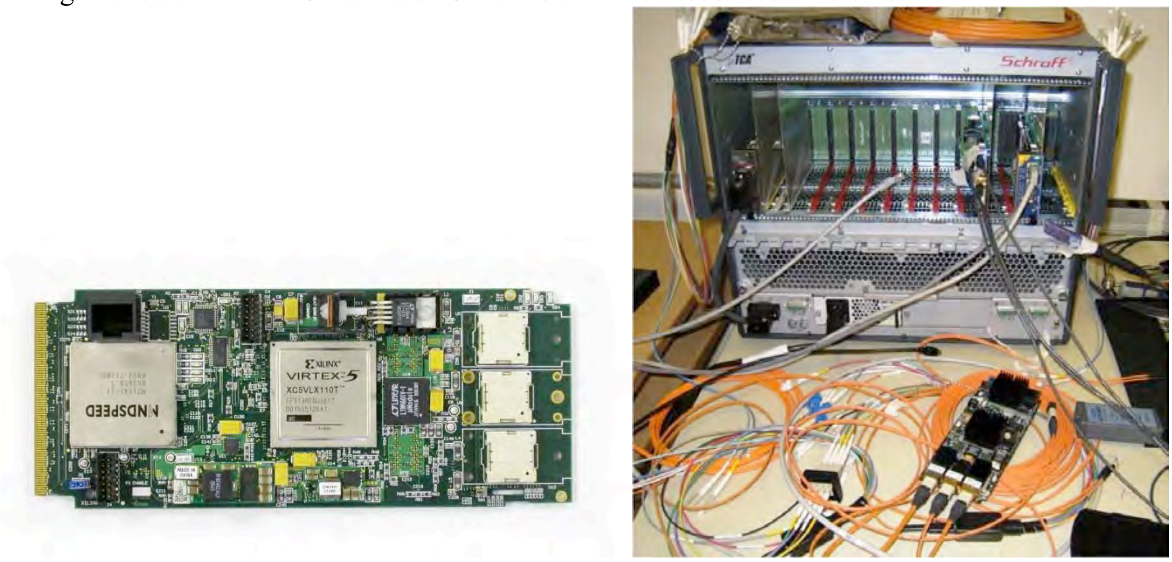

Figure 1: (a) The CMS GCT Matrix Card. Shown at the top are the three sockets for the optical modules. The card supports 12 input, 12 output and 4 bi-directional links running at 3GBps. Also shown is the Virtex-5 FPGA and the 72x72 cross-point switch close to the uTCA backplane connector. (b) The uTCA crate used for development of firmware and trigger demonstrator algorithms.

In parallel, a significant effort has been devoted in designing the main processing card (milestone 1-a) which is now called the mini-T card. The card was designed by G. Iles and layout done at Imperial by S. Greenwood. The design is based on the Virtex-5 part but unlike the Matrix card it does not have a crosspoint switch. Instead it can exchange data with other cards via front-end optical links, uTCA backplane links and LVDS links. The card supports 5 Gbps optical links and is the first of its kind at LHC. The advantage of this design is that it can use a commercial backplane which results in a simpler design than the GCT Matrix card.

The design is finished and been sent for manufacture which completes milestone1-a. Fig. 2 shows the layout of the mini-T card. Prototypes of this card are expected at the end of February 2010.

The design of a uTCA backplane (milestone 1-b) has been postponed until the results from the testing of mini-T are known. At that point a decision will be made if a backplane is necessary for the first demonstrator or if a commercial backplane can be used instead.

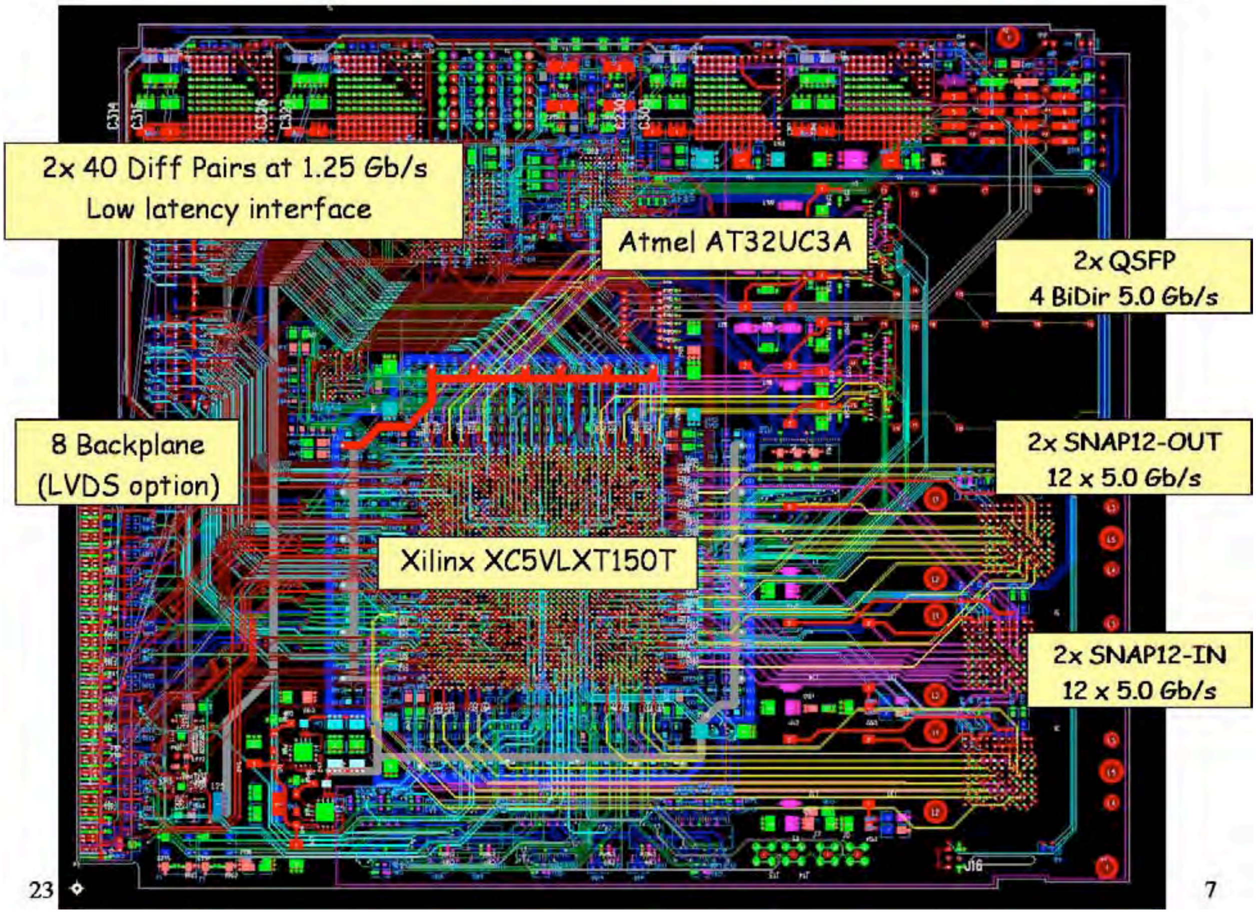

Figure 2: The layout of the mini-T card. The layout was done at Imperial.

5.4 Staff on project

The WP3 team at Imperial consists of C. Foudas (Imperial-Academic), G. Iles (Imperial-engineer) and Sarah Greenwood (Imperial-technician). J. Jones (Princeton), who completed the first firmware design, has recently left CMS. A. Rose (Imperial- RA) began work in November 2009.

The WP manager C. Foudas is expected to leave Imperial in summer 2010. Discussions are under way regarding replacement. Meanwhile the PI will take responsibility for overall supervision of the WP3 activities.

5.5 Expenditure

About £22.6k of the WP budget has been spent (including non-invoiced commitments) for the production of the MiniT, a uTCA controller (MCH) and a uTCA crate and other components.

5.7 Summary

Work on trigger demonstrator devices has made excellent progress and in 2010 we hope to have the first results from testing these systems both on the firmware and the hardware front.

6 Risk register

The current version of the project risk register is 1.1 dated 9 February 2010. It is included as a separate file. The main changes from the previous version are listed here.

Risk 1.1: STFC funding itself has not been changed, but the delay in being allowed to spend the budget and the need for reprofiling have been noted.

Risk 1.2: HEFCE funding situation has deteriorated due to significant overall budget cuts announced recently. The situation is not yet clear as to impact upon this project, if any.

Risk 2.5: The current leader of WP3 is likely to depart soon. This is not anticipated to seriously affect the project progress in this WP at present.

Risk 4.2.1: Delays in funding being available at RAL have caused some delay in WP1. The situation is now improving with recruitment of extra staff under way.

Risk 4.3.1 and **4.3.2**: SLHC machine delays; we now have a better idea of likely schedule and specifications since the Chamonix meeting and are in the process of changing our detailed plans in all WP.

7 Finances

In view of the modest expenditure so far and the late notice of the first Oversight meeting, only a summary of expenditure is provided below. There was essentially no spending in the financial year 2008/09 and the present financial year is not yet complete so the picture is of spend to date, as of mid-February. In the first year of the project much of the travel was combined with other CMS business, in addition to frequent video conference use, so travel expenditure has been limited.

It would be helpful to clarify the reporting expected for future meetings. One complication arises from the separation of funding into "new" and "old". For the universities, there is a fairly clean separation of allocations into "Rolling Grant staff" and "Staff charged to grant". In the case of RAL, all appropriate fractions of staff time are charged to the grant and the total allocation is aggregated from PPD (existing and new appointments), and TD staff.

It would also be helpful to clarify how to report the indirect and DA costs. In the tables below we report the full staff expenditure (i.e. at 100% FEC) and the net contribution by STFC to university other FE costs.

7.1 Allocations

The latest figures from STFC at listed in the table below:

CMS Upgrade costs 80% indexed (except RAL Staff and Travel - 100% indexed)						
	FY 08/09	**FY 09/10**	**FY 10/11**	**FY 11/12**	**FY 12/13**	**Total**
University New Staff Total	68,854	310,015	349,105	272,355	74,413	1,074,741
RG Staff Total	79,280	271,611	336,016	201,422	23,172	911,501
RAL Staff	70,000	480,495	546,364	77,584		1,174,442
Travel Total (RAL)	6,866	28,209	28,970	25,780	7,120	96,945
Equipment/Materials Total	65,980	432,498	127,947	12,760		639,185
Grand Total	**290,980**	**1,522,827**	**1,388,401**	**589,901**	**104,705**	**3,896,814**
Totals excluding RG	211,700	1,251,216	1,052,385	388,479	81,533	2,985,313

The RAL staff costs include £645,000 before inflation for TD staff effort.

The non-staff costs are to be distributed by WP as:

Non-staff allocation by WOP and Institute (at 100% FEC)					
	Bristol	Brunel	Imperial	RAL	Travel
WP1	47,730		210,200		45,300
WP2	45,000				39,900
WP3			370,000		11,745
Total	92,730		580,200		96,945

7.2 University grant allocations

Each university reports its spending in a slightly different way as summarised below:

	Staff (100%) and students	Non-staff total	Other	Total
Imperial	353,222	580,201	296,347	1,229,770
Brunel	47,722			47,722
Bristol	181,717	31,000	223,712	436,429
Total	582,661	611,201	520,059	1,713,921

which do not necessarily accord with the categorisation of STFC allocations, although totals should, and do, match.

	Staff on grant & overheads	Equipment and DI		Total
Imperial	664,770	565,001		1,229,771
Brunel	47,722			47,722
Bristol	362,250	74,184		436,434
Total	1,074,741	639,185		1,713,926

7.3 Actual spend to date

The following table summarises spend on the upgrade grant, which excludes Rolling Grant contributions, at the end of January. These figures should be the cost to STFC, i.e. including other contributions from universities to those items where appropriate.

		Spend to 31-Jan-10	
Account Location	**FRS code**		
RAL	FK85100	WP1 - RAL PPD Staff	58,785
Bristol		WP1 - staff and indirects/DA	87,793
Brunel		WP1 - staff and indirects/DA	25,848
Imperial		WP2 & WP3 - staff & project student and indirects/DA	83,956
RAL	FK85110	WP1 - Equipment/Consumables	
RAL	FK85200	WP2 - RAL TD Staff	71,510
RAL	FK85210	WP2 - ASIC Design	20
RAL	FK85215	WP2 - SFED Development	
Bristol		WP1 & WP2 - requisitions	9,148
Imperial		WP2 & WP3 - requisitions	14,276
RAL	FK85120	WP1 - Travel	1,098
RAL	FK85220	WP2 - Travel	5,519
RAL	FK85320	WP3 - Travel	1,262
		Total	359,215