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R&D in preparation for upgrades of the CMS detector for High Luminosity LHC

1 Executive Summary

The R&D project is now entering the final presently-funded year. Notable progress since the last report includes:

The LHC concluded a successful year of operations accumulating over 5 fb^{-1} of integrated p-p luminosity at 7 TeV centre of mass energy and is aiming for a significant further increase in 2012. This has important consequences for the Higgs search where tantalising hints were seen around 125 GeV mass by both CMS and ATLAS. Although new studies of the implications have not yet been made, either a discovery or an exclusion will further motivate experiment upgrades.

The first LHC Technical Stop, LS1, is planned to commence in November 2012 and to end in September 2014.

There has been further progress in developing, and improving the performance of, software for upgrade simulations, especially for Phase I tracking studies.

CMS has adopted IPbus, the software and firmware framework largely developed in this R&D project, as the common standard control system for all upgraded μTCA crate-based electronics.

The CMS Calorimeter trigger review concluded with a recommendation to base further developments on the UK hardware but postponed the final decision on the architecture until more simulation studies have been completed. The UK hardware can be used in both potential architectures.

The next version of the CBC is still in design with a target submission date of May 2012. This will be a coarse-pitch bump-bonded version suitable for track-trigger modules. There has been further progress in evaluation of the first version of the CBC.

Following discussion among the UK groups, we proposed to the CMS Tracker to take responsibility for providing new FEDs, and software and firmware support, for the upgraded pixel detector. This was accepted, very positively. It builds naturally on our contributions to the Tracker DAQ and will profit from work done in the UK R&D project to date on trigger hardware and online software and firmware.

Alex Tapper has taken over as CMS Trigger Upgrade Project Manager in January 2012.

Funding has been put in place to extend posts in Bristol and Brunel to the end of the present project. The RAL PPD staff situation is now much clearer and a sound basis for future planning. The preparation of a PPRP proposal for construction and continued R&D funding is under way for submission for either the June or September 2012 PPRP meeting.

2. Project history and recent developments

The original proposal was submitted to STFC in October 2007 with an upgrade of the LHC peak luminosity from 10^{34} $cm^{-2}s^{-1}$ to 10^{35} $cm^{-2}s^{-1}$ about ten years after start-up in mind. The accelerator upgrade has since been proposed to take place in two main stages, with an increase in luminosity to 2 x 10^{34} $cm^{-2}s^{-1}$ being Phase I, occurring in 2018 in the most recent CERN ten-year plan, and a further major increase in the next decade, probably to ~5 x 10^{34} $cm^{-2}s^{-1}$ levelled luminosity.

The experiment and accelerator continued to operate extremely well throughout 2011, accumulating an integrated p-p luminosity of 5.2 fb^{-1} by the end of operations, plus 140 μb^{-1} of Pb-Pb data. There was a tremendous effort to analyse potential Higgs discovery channels, in which the UK played a significant part particularly on the two photon channel and tau decay modes, with additional important roles in the review processes. CMS was successful in analysing all the major decay modes ($\gamma\gamma$, $\tau\tau$, $b\bar{b}$, $WW \rightarrow 2l2\nu$, $ZZ \rightarrow 4l$, $2l2\nu$, $2l2q$, $2l2\tau$), using the full 2011 recorded data set. There was also a very significant extension of the SUSY exclusion limits for the CMSSM parameter space, which resulted in noteworthy CMS publications.

Although the machine performed very well, there are still many features being better understood. One issue which had an impact on data taking and might still affect CMS in 2012 seems to have been successfully resolved. During 2011, there were persistent vacuum problems on one side of the detector 18 m from the interaction point, which appeared to be associated with an RF connection between two beam pipe sections. It caused an excess of beam gas events and slowed data taking, and was evidently luminosity dependent. During the winter Technical Stop, the bellows section was replaced and examination revealed that it was indeed seriously faulty. We await beam operation to be certain, but it now appears the high quality vacuum has been restored in this region.

2.1 LHC upgrade schedule and planning

There have been no further changes to the LHC operations schedule since the last OSC meeting, and at the recent LHC Chamonix workshop the planning for the near future, including Long Shutdown LS1, was explained in more detail. It is confirmed that the LHC will run at 8 TeV centre of mass energy in 2012, with 50 ns bunch spacing, and a target of 15 fb^{-1} integrated luminosity. LS1 will begin in late November after the heavy ion running, although there is room to extend the run for up to two months in case the p-p luminosity is below the objective for Higgs discovery. The LHC should restart operation, with a couple of months of commissioning, in September 2014 and be ready for physics data taking before the end of that year. At that time the machine should be ready to operate with a beam energy of up to 6.5 TeV.

2.2 CMS planning

CMS is preparing Technical Design Reports for sub-detector upgrades. The pixel TDR is in advanced draft form, with a goal to submit in Q3 2012 for presentation to the LHCC in September. The trigger TDR is also intended for submission during 2012; the document is now being planned. For longer term Tracker R&D, the overall planning has not changed since the Gantt chart presented at the last OSC meeting.

Key dates are the installation date of the upgraded pixel detector and activities during LS1, which must be completed with sufficient time to fully test and check operation of systems such as the trigger crucial to CMS data taking. The provisional date for pixel detector installation is at the end of 2016 in an extended LHC Technical Stop. This is not considered to be definite but to be used for planning, and it is viewed favourably by the LHC machine planners, as it can be adapted to their requirements by extending a standard end-of-year shutdown matching necessary machine activities without major schedule disruption. It is probably therefore the earliest date at which a new pixel detector might be installed, and constrains other aspects of the overall pixel project plan to conform.

Following the appointment of a new Spokesperson from January 2012, there have been new appointments to several major positions and gradual organisational changes. The new Upgrade Management team is interacting with sub-projects to define key reviews and internal approvals, including following up on the Calorimeter Trigger review in the near future, and producing a more comprehensive overall plan for the coming few years.

A rather detailed plan of technical coordination and sub-detector activities for LS1 already exists but does not yet contain all the trigger actions. This period is very highly constrained, particularly for the underground experimental cavern UXC55. It will include the insertion of a new beam pipe towards the end of 2013 and, prior to that, pixel modules in the endcap region. The trigger modifications do not involve UXC55 work, but do require significant work in the service cavern area USC55. This must be completed well in time for recommissioning CMS beginning in the early part of 2014, to be ready for LHC operation later in the year.

2.3 UK adaptation to CMS planning

With a clearer view of LS1 and the pixel installation date, it is now possible to define better the planning of the UK contributions to pixels and trigger. The longer term tracker, and track-trigger, plans remain unchanged with an envisaged LS3 in 2022. The UK plans are presently being updated with the PPRP proposal in mind.

A revised SoI for CMS upgrades, covering the period 2013-2019 was submitted to STFC in December 2011 and Science Board recently invited the submission of a proposal to the PPRP. The submission date of a UK Phase I construction project proposal, including long term Phase II R&D, was targeted at the June 2012 PPRP meeting. However, the expected load on the PPRP as well as the short time available for completion of the proposal, influenced by several factors such as RAL PPD reorganisation, the present grants round and the time needed for detailed costings to be signed off by university administrations, make this deadline rather challenging. It would require documents to be submitted by 12 April. The September meeting would require documents at the end of June, which is more practical and allows some of the CMS planning, including TDR developments, to have matured further.

However, this raises a crucial concern about continuity of funding. University termination procedures begin six months before grant funds expire. The duration of the approval process, including Science Board and STFC Executive approval, as well as issuing grant letters to universities, is uncertain. A gap in funding would have significant implications for short term staff appointments and TD activities, which would be highly undesirable at a critical point of a hitherto extremely successful project. Hence we would like to request STFC to put in place bridging funds for a six-month period from the end of the present grant to ensure this does not happen. This would already slow activities to some extent by preventing recruitment to any new posts awarded and limiting some expenditure. However, it would minimise the impact of a funding gap. We seek the OSC support in recommending this to STFC.

3. Work Package 1: Tracker and Level-1 Trigger Simulations and Software

3.1 Objectives

The objective of WP1 is to support with software tools the design, optimisation and prototyping of replacement detector and electronic systems for the CMS tracker and L1 trigger. The project is now mainly focussed on the Phase-I upgrade. The tools and ideas for Phase-II which were developed in the early part of the project continue to be exploited as a low-level background activity.

The top-level work package goals are as follows:

- Development of tools for simulation and optimisation of upgraded tracker and trigger systems in a very high luminosity environment
- Investigation and optimisation of tracking detector layout and inclusion of tracking data into the CMS trigger decision
- Provision of online and offline software tools and firmware to support the design and operation of upgraded electronics systems for Phase-I, including the construction and operation of hardware prototypes.
- Assessment of the performance of the upgraded CMS detector against key physics requirements and with realistic background conditions.

3.2 Progress to date

The technical details of the CMS Phase-I upgrade programme are becoming increasingly well-defined, with the subprojects of primary interest within WP1 (pixels and L1 trigger) both intending to submit Technical Design Reports in 2012. An extension to the duration of WP1 until March 2013 has been agreed by STFC, such that this time scale is well matched to that of the project. As a result, the UK will be able to make a substantial contribution to the preparation of these documents, and has taken a leading role in this process. We note that all aspects of our work have regularly been presented at international workshops and conferences in the reporting period.

Simulation tools: The UK continues to provide leadership in refactoring CMS simulation software (i.e. improving code, while respecting interfaces) for upgrade simulations. The most challenging aspect has been the upgraded pixel detector, for which large samples of GEANT4-simulated events are required, based upon a detailed and complex description of the new detector. The software has now evolved to the point where large samples with background level up to $\langle n_{events} \rangle$=50 can reliably be produced within the nominal resource constraints of a standard CMS simulation job. The required CPU time has been substantially reduced, and most importantly, the required core memory brought down to around 2GB, allowing most samples to be produced without the use of special high-memory resources. The remaining exceptions to this, typically jobs requiring exhaustive checking of reconstruction performance, may be run on small dedicated resources including clusters in the UK. A large set of samples for the exemplar Z Higgs analysis (described below) have now been produced [M. Grimes] for two different geometries.

One area of reconstruction that still requires improvement is pixel quadruplet track seeding. Work has begun [I. Reid] investigating the use of k-dimensional trees to improve seeding performance, in an approach that will also be beneficial for efficient triplet and doublet seeding in the High Level Trigger even before the upgrade.

The UK has recently taken responsibility, based on expertise from the pixel project, for the integration and release of the code base for simulation of the upgraded trigger. M. Grimes will lead this work, which will be vital in producing simulation studies for the L1 Trigger TDR. Whilst this code is less complex than the tracking simulation, integration of the many different subsystem simulations is challenging, and there are of course also dependencies on the description of upgraded detectors.

Physics performance studies: CMS is now embarking on detailed physics performance studies, based upon the Phase-I detector described in the Upgrade Technical Proposal. In addition to work on simulation tools, the UK [M. Grimes] is leading a flagship analysis which will help to commission and debug the simulation, and define the approach for following work. The chosen channel is Z+H production, with the Z decaying to muons and the Higgs to b-quarks. A pileup level of <n>=50 will be assumed. This channel has been chosen because of its challenging requirements on the upgraded pixel and muon systems, and its relevance for the Phase-I period due to the need for high luminosity samples. Work is progressing well.

The L1 trigger upgrade project, led by A. Tapper, has also recently begun to define its strategy for simulation studies leading to the TDR. This work will proceed in the three phases, beginning with object-level studies to ascertain the performance of new L1 algorithms for electrons / photons, muons, jets, taus, and global event shape and energy flow variables. In each case, the trade-offs between rate and efficiency will be examined under background assumptions of <n>=30, 60, 90. The highest pileup scenario is expected to be extremely challenging, providing valuable feedback to the CMS upgrade programme on the effects on performance. The UK [M. Pioppi, A. Rose] has taken responsibility for studies of new jet algorithms, which links closely to algorithm firmware interests within WP1 and WP3. The feasibility of online pileup subtraction techniques will be investigated.

The second phase, for which the UK [J. Brooke, D. Newbold] has taken lead responsibility, is the definition of exemplar trigger menus, illustrating trade-offs in physics reach which may be necessary under each background scenario. Whilst object level studies progress, this work will start with an examination of a 'no new L1 algorithms' menu, illustrating clearly the physics case for the L1 upgrade.

Online software: Under the leadership of R. Frazier and A. Rose, a hardware demonstrator for the IPbus protocol was delivered in 2011, and has been used extensively in the further evolution of the firmware and software components of the control system. A major new development in this area has been the adoption by CMS of IPbus as the common standard control system for all upgraded electronics. Work in this area during 2012 will therefore take place in four areas. Firstly, the existing tools will be integrated more closely with the CMS XDAQ online framework, and new release tools developed to allow easy deployment of IPbus across a wide range of subsystems. Secondly, a development system of hardware, firmware and software will be set up in the electronics integration centre at CERN, so subsystems may use the system during hardware integration exercises. Thirdly, we will continue to develop the IPbus protocol to achieve higher performance and robustness. In this area, D. Sankey will take key responsibilities for firmware aspects of the system. Fourthly, we will begin integration of IPbus components with the CMS Detector Control System, providing an end-to-end solution for the control and monitoring of electronic systems within the existing CMS framework.

Take-up of the IPbus system outside CMS continues, with the framework now in use by groups within ATLAS, LHCb and in the Daresbury and CERN accelerator divisions, amongst others.

3.3 Deliverables and Milestones

As the project will now continue longer than originally foreseen, we propose to introduce new deliverables and milestones to cover the period up to March 2013. These are listed in the milestones table, and focus largely on the delivery of contributions to the upgrade TDRs for pixels and L1 trigger. We summarise below the 'Year 3' milestones which were originally due for completion:

Track-triggering: As reported previously, our original work on track-triggering was brought to a conclusion in 2010, in order to focus on the Phase-I project. The original milestone M1.3.1 concerning trigger benchmarks we therefore propose to integrate into a new milestone for delivery in September 2012 of delivery of L1 trigger performance studies for the TDR. The milestone M1.3.3, concerning a track trigger TDR, was removed in 2010.

Trigger algorithms: The milestone M1.3.2 concerning proof-of-principle algorithms was met earlier than the original schedule, with the completion of the joint WP3/WP1 L1 calorimeter trigger demonstrator documented in this and earlier reports.

Definition of UK construction project: The milestone M1.3.4 was ahead of schedule as part of the overall UK planning for the construction phase of the upgrade project, and was documented in the recent CMS UK Statement of Intent to STFC. We have now been requested to submit a proposal to the PPRP, so more detailed work in this area will continue.

Progress against the replacement Y3 milestones is on target.

- M1.3.6 (stable release of online system) has been achieved, with the system in wide use across CMS. However, this work will clearly expand in scope as the integration effort continues.
- M1.3.7 (release of CMS upgrade code) has been achieved.
- M1.3.8 (full simulation study of L1 algorithms) has been absorbed into the overall work programme towards the L1 TDR, with the work shared between the UK and collaborators. In addition, the UK will take responsibility for the definition of the L1 menus that define the physics reach of the experiment.

3.4 Staff on project

Reported in tables. We note that the tables have been updated to reflect the extension to WP1.

3.5 Expenditure

The expenditure to date is reported in the financial tables; WP1 is dominated by staff costs, with some travel. Expenditure required in the integration of WP1 online software with prototype trigger and readout hardware in WP3 and WP2 is generally covered in the budget of those WPs.

4. Work Package 2: Outer Tracker Readout

4.1 Objectives

The objectives of WP2 are to develop a readout chip suitable for the outer tracker, to study options for providing Level 1 trigger data from a new Tracker, and to contribute to development of a complete readout system, including off-detector components for the front-end DAQ.

Up to now, the ASIC work has been most critical to the R&D project and it was foreseen that the DAQ developments would evolve to match and service the front-end readout requirements. As envisaged in the original proposal, the DAQ – or new FED – development would have been needed as the readout system architecture evolved. In practice, the project has not proceeded in quite that way, since the LHC upgrade was divided into two stages, with Phase II coming much later than anticipated. However, components, such as proto-FEDs, are required soon to enable CBC-module readout, to prototype new communications interfaces, such as the GBT, Versatile Optical Links and high speed Ethernet, which will be deployed in the future.

More recently, as the pixel replacement became better defined, requirements for Phase-I have become clearer and it is natural for the UK to take responsibility for a new pixel FED, whose specifications are now under intensive discussion, and to profit from the UK activities in WP3 towards the trigger, such as µTCA expertise and the IPbus framework.

Thus, the "SFED" developments are now becoming integrated into a broader work programme shared between Imperial, Bristol and RAL, both PPD and TD. We are also expecting contributions from Brunel. New targets are being defined for the final year of the project which build on all the developments to date.

4.2 Progress to date

Front end chip

The CBC readout chip (CMS Binary Chip) development is for short silicon microstrips to be used in the outer tracker region. The 130nm CMOS CBC was designed in a collaboration between RAL TD and Imperial College. It is a 128 channel wire-bond chip delivered in March 2011. The main features are:

- fast front end amplifier, with 20ns peaking time,
- ability to match both sensor polarities
- ability to tolerate leakage currents up to 1 µA
- comparator with programmable threshold,
- 256 deep pipeline,
- 32 deep buffer for triggered events,
- unsparsified binary readout for chip and system simplicity
- output MUX and driver, using a low power signalling standard (SLVS),
- fast (SLVS) and slow (I2C) control interfaces.
- on-chip DC-DC switched capacitor power block
- low dropout regulator to supply clean power rails to analogue stages

All features of the chip have now been evaluated and results have been presented regularly at CMS meetings[1]. Preliminary results were presented at the 8th international meeting on Front End Electronics, Bergamo, May 2011[2]. A presentation was made at the TWEPP conference in Vienna in September 2011 containing more mature results and the associated paper was subsequently accepted for publication in JINST[3]. For a sensor capacitance of 5 pF, a noise performance of less than 1000 electrons rms is achieved for a power consumption of 300 µW/channel.

Electronic measurements of chip performance were confirmed by inserting a simple single-chip-plus-sensor module in a particle beam at CERN in September 2011 (figure 4.1). The CBC module was

[1] http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/
[2] http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Lawrence_FEE2011_Bergamo.pdf
[3] http://dx.doi.org/10.1088/1748-0221/7/01/C01033

successfully operated in conjunction with the beam telescope described in a previous OSC report. Analysis of the data continues.

A setup for investigating the performance of the CBC at low operational temperatures has been developed at Bristol and preliminary results were also presented at TWEPP in September.

The performance of the on-chip switched capacitor DC-DC conversion circuit has been studied and results presented to the CMS tracker power working group. The circuit works well with high efficiency and does not affect the intrinsic noise performance of the chip. However, systematic pedestal effects are observed which depend on trigger time with respect to the DC-DC switch operation, which lead to some degradation of the noise performance. It is likely that this effect could be substantially reduced in the next version of the chip which will be bump-bonded.

Radiation (ionizing and SEU) tests of the prototype CBC are still outstanding.

The definition of the next version of the chip, CBC2, has progressed within the CMS Phase-II tracker electronics system design group which includes collaborators working on all aspects of outer tracker readout modules (mechanics, cooling, links, powering, sensors and off-detector readout). The requirement that the tracker provide information to the Level 1 trigger motivated an architecture where correlations between signals from high p_T particles traversing closely spaced layers are achieved by bringing signals from both layers together into a single chip (figure 4.2).

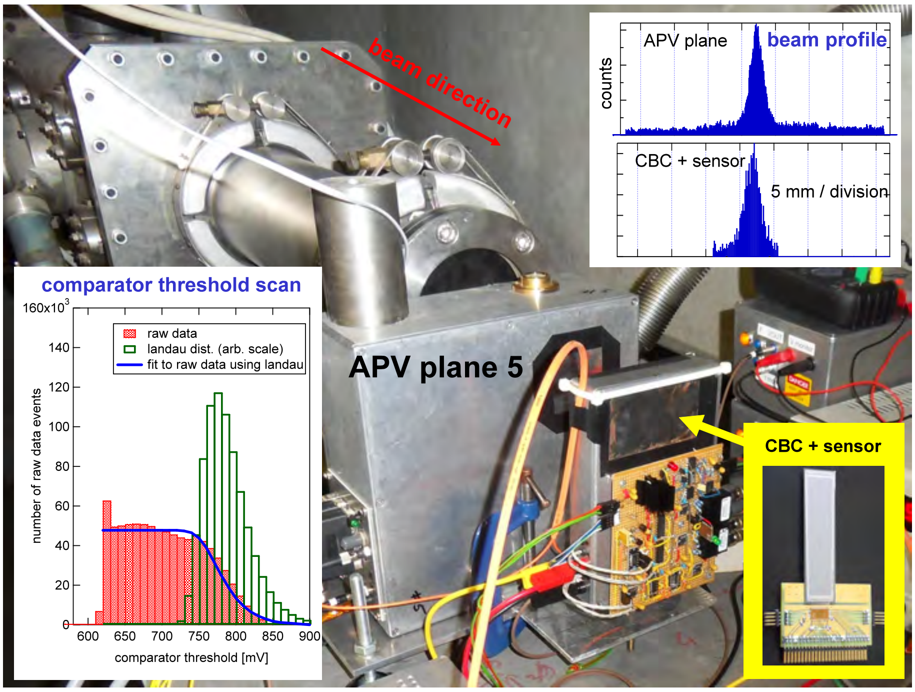

Figure 4.1. CBC readout module test beam setup and early results

The CBC2 will be bump-bondable with signals from two wire-bonded sensor layers fed to chips mounted on only one side of the module through a substrate which allows very high density traces. The substrate design and technology studies are the responsibility of a CERN-led group, and other (non-UK) groups are responsible for other components of the module.

The design of the CBC2 is well advanced, with submission scheduled for May leading to wafers in hand in the autumn. The architecture closely follows the prototype, expanded to 254 channels and with additional triggering logic and layout adjusted for bump-bonding on an array pitch of 250 microns. While we are making progress on converging on system solutions for assembling trigger information and subsequent off-detector transmission, the final architecture will not be implemented in this prototype version, and just a simple trigger output will be provided (indicating the presence of one or more positive correlation results).

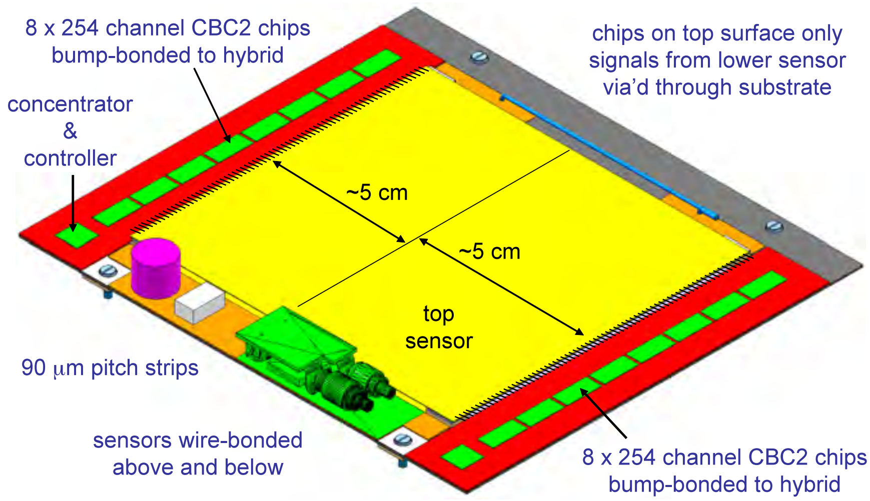

Figure 2. SS-p_T module concept

The CBC2 should allow all aspects of the design and performance of the SS module design to be studied, in collaboration with CMS colleagues. The move away from a conventional wire-bonded, single layer approach to meet the L1 trigger requirement, means significant steps in the use of new technologies and module construction, much larger than anticipated in the original proposal. Further prototyping steps in the CBC development will therefore be required, which will be addressed in a future upgrade proposal. The final achievement of this phase of the upgrade programme will therefore be the delivery of a successful prototype CBC2 chip.

SFED developments

RAL TD received a mini-T board in October 2011, set up the board in the lab and became familiar with the hardware and firmware. Subsequently RAL-written firmware was ported to the mini-T and used to control it using the IPbus system.

RAL TD worked with Bristol on the feasibility of extending the present CBC readout system for possible use in future module test beams.

The recent 10-Gbit Ethernet UDP FPGA design developed for the XFEL project at DESY has been adapted for use in the CMS environment. This has been integrated with the IPbus control system and tested using a Xilinx Virtex-6 evaluation board. 10-Gbit Ethernet is a likely choice as a common standard for future DAQ systems in CMS, including the upgraded pixel readout, and this work is therefore highly relevant to CMS developments.

Advice has been given on firmware design for a new pixel readout and possible FPGA evaluation platforms evaluated.

During the final year of the project some of the goals will change to be more relevant to the pixel DAQ activity where there is in any case a strong overlap, by prototyping using IPbus and μTCA. Currently work is underway on the design of an FPGA-based Memory Buffer management block which will provide event data readout over GbE using IPbus. The design builds on the basic memory interface firmware developed last year. The goal is to provide a simple to use data readout system which could be used in a number of development setups including CBC, pixel and trigger test systems.

4.3 Deliverables

For the front end chip component of WP2, a summary of the status of recent milestones is:

Year 3

M2.3.1 (03/12): *Review results from prototype tests to ensure adequate functionality*. As originally proposed, the milestone has been met. The CBC2 chip will include simple additional triggering functionality and be bump-bondable. Front end chip functionality, performance and requirements are regularly reviewed in CMS systems meetings dedicated to the SS module approximately every 6 weeks, which will continue for the foreseeable future.

M2.3.2 (03/12): *Documented preliminary chip results*. This milestone has been met by presented and published results at CMS meetings and TWEPP 2011.

M2.3.3 (03/12): *Documented results of prototype chip evaluation & prototype module and system tests*. A simple CBC plus sensor module was successfully operated in a test beam in September. Preliminary results have been presented at CMS meetings and TWEPP 2011, and further analysis is ongoing.

M2.3.4 (03/12): *Final pre-production chip designed & submitted for fabrication and test setups prepared*. The CBC2 chip cannot be considered as a final pre-production chip as functionality has been expanded beyond the original concept. Further prototyping stages are required, to be included in a future upgrade proposal, and adapting to the tracker definition. The CBC2 is currently scheduled for submission in May 2012 with delivery in the autumn. Because of the bump-bonding requirements special substrates are required to take the chip and these are under development in conjunction with CMS collaborators. Preliminary test setups will be based on those used for the previous prototype.

M2.3.5 (03/12): *Prototype system design*. This milestone has been met. The outer tracker triggering and readout system is based around the 2S-p_T module concept in fig. 4.2. Preliminary data acquisition and control architectures have been defined, based on the CERN GBT (GigaBit Transceiver) and Versatile Optical Link developments.

Year 4

M2.4.1 (09/12): *Documented results of final prototype*. Due to the timing of the CBC2 submission this milestone will be delayed. However, the scope is considerably more extensive than originally envisaged.

For the FED activities, the milestone to implement FPGA designs on a Mini-T or GLIB board was achieved on schedule in December 2011. New milestones have been added to the future plan:

- Implement IPbus Buffer Management and Readout firmware. Target 07/12
- Demonstrate Buffer Management and Readout FPGA system using IPbus over 1 GbE electrical link. Target 07/12
- Demonstrate High Performance Readout system using 10 GbE optical links. Target 03/13

4.4 Staff on project

Listed in the tables. No significant changes, but engineer Davide Braga from RAL TD is now registered for a PhD at Imperial College since January 2012 and the scope of his work will broaden slightly accordingly. The number of TD staff contributing to the ASIC design has increased during the last year but is expected to decline for a period following the CBC-2 submission.

4.5 Expenditure

There has been only modest consumable spending concerned with testing in the lab and test beam since the first CBC production in an MPW run. There will be a substantial expense from the next ASIC submission in May, which is planned to be shared between the XFEL project and the CBC-2, with a total cost of about \$500k. The exact sharing is in the final stages of discussion but the larger part will be paid by XFEL.

4.6 Comparisons with CMS activities elsewhere

Currently there is no significant ASIC development underway in any other CMS Tracker institution, except for CERN developments of chips for the GBT and VOL systems, and pixels. For the FEDs, the μTCA development was welcomed both as providing a system for the Phase I pixels and as a prototype of future Tracker readout.

5. Work Package 3: Design of Level-1 Calorimeter Triggers at the SLHC

5.1 Objectives

Work Package 3 is developing a demonstrator for upgraded Level-1 Trigger electronics and studying new trigger algorithms using this system. The main goal is to provide a standard device for calorimeter Level-1 triggers which can be adopted during the Phase I upgrade in the first instance.

Our system consists of generic modular devices based on FPGAs and optical links and is the first prototype of off-detector trigger electronics for HL-LHC, as well as the Phase I trigger.

5.2 Progress to date

The most significant event of the last six months was the Calorimeter Trigger Review, which was held on 14 October 2011 with several subsequent written submissions to the review committee. The final report was delivered on 31 December (Appendix). The mandate of the committee was "*to evaluate the two systems [Time Multiplexed Trigger (UK) and Conventional Trigger (US)] based on the requirements that are stated below and to recommend the form of the system to be built.*"

The committee were unable to form a definitive judgement on which architecture to adopt, however they noted that "*development of a common L1 trigger hardware platform, to be used by all trigger systems, is not only desirable but technically possible*" and that "*the development of the trigger processing board should be based on the demonstrator board built by the UK group, which at this point is the only available prototype with performance approaching the requirements*". They also added that "*The trigger processing board I/O should fit at best the needs of different trigger systems and architectures*".

The UK has responded to this with the development of the final trigger processing card – the MP7. It has been specified with the help of the CMS trigger community and is now in the final stages of layout (see fig. 5.1). It uses optical interconnects rather than the backplane for trigger data paths, thus allowing it to implement any type of trigger architecture, in contrast to the alternative under development. This approach also keeps the standard backplane ports free, thus allowing users to make full use of standard commercial μTCA capabilities (e.g. 10GbE, SRIO & PCIe).

It uses very similar optics to those pioneered in the Mini-T5 and now being adopted by many CMS groups. The MP7 will feature a 1.44 Tb/s optical interface and a 64 Gb/s electrical interface on the front panel with GbE, DAQ, etc supported on the backplane. The design is scalable so that, depending on the requirements, the most appropriate FPGA and optics may be selected and thus cost minimised.

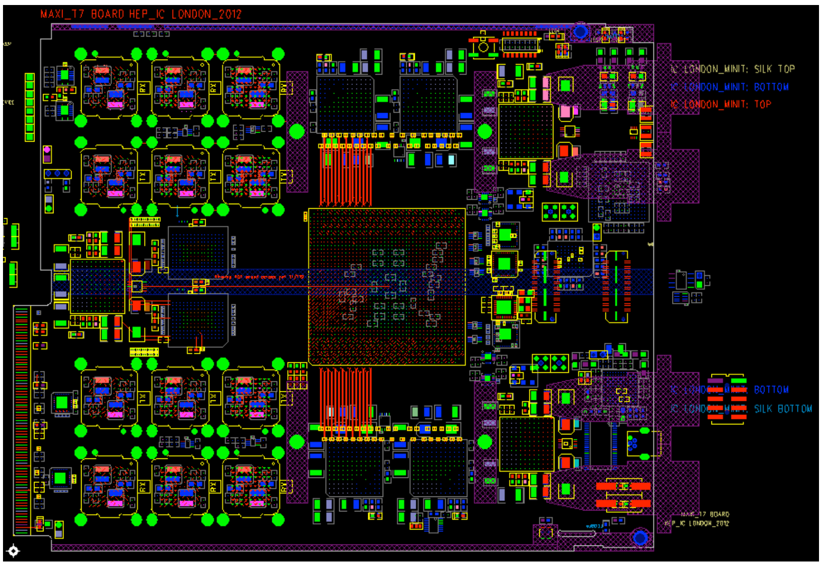

Fig. 5.1. Layout of the MP7 Trigger Processing Card.

The review committee also recommended "*the definition of a program of additional [algorithm development] studies using simulated data and collision data (high pile−up runs) to assess the performance of different algorithm options*". In response the UK groups have recruited effort from existing grant posts and students to pursue a programme of algorithm simulation studies, in the context of the planned Technical Design Report (see below).

The development of MicroHAL - the robust, high performance and scalable Ethernet Hardware Access Layer (HAL) continues with the release of beta packages to many users. Their feedback is now being incorporated into the code ready for a final release.

5.3 Overview of CMS plans

CMS aims to deliver a Technical Design Report (TDR) for the first phase of the L1 trigger upgrade by the end of 2012, allowing a review by the LHCC to begin early in 2013. Preparations for this started with a series of extended meetings to understand the status and requirements of the muon, calorimeter and global trigger sub-components and the central software. This series of meetings has been completed and the information and discussion points raised are being used to draw up detailed schedules, cost estimates and topics to follow up.

Defining physics requirements for the upgrade is one of the most urgent topics, which until now has had limited support because physics teams have been focused on analysis of current CMS data. This is changing as the upgrades gain prominence and the challenges of operating in a high pile-up environment become apparent. A detailed programme of simulation studies is planned for the TDR in cooperation with the physics analysis groups, in particular Higgs and Supersymmetry. A significant influx of manpower for these joint studies is expected through the raised profile within the collaboration. The studies should address improvements to trigger object algorithms, example trigger tables for high luminosity, high pile-up scenarios and some benchmark physics channels. The UK groups plan to contribute strongly to this programme through existing grant and student effort.

Commissioning the upgraded trigger must not put efficient data-taking at any risk. To ensure this, it is intended to duplicate incoming data upstream of the trigger electronics to allow the new system to be commissioned in parallel with the existing trigger. Installing the splitting components to achieve this is a key task which much be completed during the LS1 shutdown and is now a critical issue. In particular in the calorimeter trigger system, signals from the ECAL must be converted from electrical to optical and duplicated. To maintain the function of the existing calorimeter trigger system requires a large number of new mezzanine boards to transmit and receive these optical signals. As is noted in the Calorimeter Trigger Review report, there are considerable uncertainties remaining in the design, costing and schedule for the production of these items, which need to be addressed.

5.4 Deliverables

Of the proposed recent milestones, the following have been met or effectively retired:

First μTCA demonstrator system ready

Working prototypes of processing card and backplane ready

Client side software done.

For the remaining year, the objective is the production of the MP7 processing card which will be done in two stages, so milestones have been added for each of them. There will be a prototype production of two units, followed later by assembly of 12 modules.

5.4 Staff on project

Reported in accompanying tables. Since the beginning of 2012 A Tapper has taken over as CMS Trigger Upgrade Project Manager, and overall responsibility for WP3. The UK groups have recruited additional effort for algorithm studies through existing grant posts. M Pioppi (Imperial) and J Brooke (Bristol) will work with students from Imperial and Bristol on these studies.

5.5 Expenditure

The major items of expenditure are the optical connectors, FPGAs and Mini-T5 and MP7 card orders, which are not yet invoiced, but the overall spend is still well within the foreseen envelope. The planning for the final year of the project is being studied to ensure sufficient MP7 cards are produced in a timely fashion within the budget.

5.6 Comparisons with CMS activities elsewhere

The Calorimeter Trigger review confirmed clearly that the UK hardware developments are significantly in advance of other comparable developments and this was recognised in the report. Some differences of opinion remain on certain key aspects of the system, such as latency and the desirability of utilising a single common board. Part of this is naturally subjective but difficult for a review panel to resolve so, although we are confident in the information which we provided to the review – and was believed by us to be generally conservative, it is understandable that the panel preferred to see more evidence on algorithm implementation and latency demonstrations.

Although Wisconsin have done more simulation work than us to date, most of this has been in demonstrating improvements in trigger performance by recovering the spatial resolution which is sacrificed in the present calorimeter trigger and not in advanced algorithms for the future trigger. In addition, UK expertise in firmware is clearly much more significant, including substantial practical experience from the GCT.

The Time Multiplexed Trigger concept remains attractive and, apart from (very weak) latency arguments against it, the main objection from some is that it is a new idea, so might include hidden pitfalls. The lab demonstrator should allow us to dispense with such objections as well as implement more algorithms in firmware, so we remain optimistic that the TMT architecture will eventually be the CMS preference.

6. Work Package 4: Pixel tracker development

6.1 Objectives

This new work package has evolved considerably since the last OSC meeting. Initially, in July 2011, a proposal was made by the RAL PPD group to participate in CMS Phase I pixel detector upgrade activities, to be complemented by Bristol WP1 effort. The objective was to upgrade an existing, relatively simple, test-board to match the new digital pixel readout chips to allow it to be used for module tests throughout the collaboration and in test beam studies.

Subsequently in November 2011 we proposed a more substantial UK contribution to the pixel upgrade involving Imperial, RAL and Bristol producing and operating the new FEDs which will be required for readout of the Phase I detector. This was motivated to profit from the work carried out in this R&D project to date, by benefiting substantially from the WP3 hardware developments and the WP1 and WP3 software and firmware infrastructure already working, which is expected to become a CMS standard, particularly the IPbus protocol.

Similarly to the WP3 trigger boards, the new FEDs will be designed using the μTCA form factor, and a prototype setup is envisaged to be operated in a pixel pilot-blade sub-project, which must be installed in LS1, should the tight schedule permit.

6.2 Progress to date

The UK proposal to provide new pixel FEDs was received very positively by CMS, and the UK groups are now formally members of the Phase I pixel upgrade project. The shorter term projects: development of DAQ test systems for the digital readout chip and their application in a beam test, now become parts of the development of a full-scale pixel detector DAQ system for which the main UK emphasis will be FED design and production, with firmware and software support, and operation in CMS. Planning for the longer term, including the PPRP proposal, is now under way.

A key point in the new pixel readout architecture is that the data sent by the front end will be a moderately high speed digital stream, at 400 Mbps including balanced error coding, instead of 40 Msps analogue data, with the pulse height information transmitted as analogue levels. This requires new optical transceivers, compatible with the existing 1.3μm optical fibre system, for installation on modules and a new FED with appropriate receivers and digital processing. While we have good knowledge of the CMS DAQ software from the Tracker project, until the recent RAL work we have not worked directly with pixel modules, so experience is needed, which can be provided by the delivery of test-boards and operation of pixel modules in various environments.

The short term plan is strongly influenced by two factors to which we must adapt: the availability of the new ROC and ancillary ASICs, and the “pilot-blade” test which proposes to insert a few end-cap modules into CMS, read out by the new electronics, during LS1. This installation must probably take place in early 2013. Submission of the new ROC design was delayed by several months, and wafers are now expected to be available around the end of May. Another crucial ASIC for the new system is the Token Bit Manager (TBM) chip which merges the outgoing data, which will not be available with all required functionality until late in 2012.

Recent progress in individual UK sub-projects is summarised below.

The development of a readout system for the digital ROC has made substantial progress over the last six months. A full set of hardware components is available, which is being used for firmware and software development. This includes a ROC emulator, based on a standard Xilinx FPGA development board with custom firmware, that sends a configurable digital ROC event onto a 160 MHz serial link upon receiving a readout token. This emulator is connected to the test-board adapter designed by Bristol and RAL, the purpose of which is to decode and deserialize the 160MHz ROC data stream into a parallel interface with lower clock speed (20–40MHz). This parallel interface connects the adapter with the DAQ test-board for the existing analogue ROCs. This DAQ test-board was designed by PSI and ETH Zurich in 2005 and will remain in use temporarily until all functionality in its firmware can be transferred into newer boards with intrinsic capability to read out digital ROCs. The only hardware modification to the existing board is a USB2 mezzanine card customised by RAL to replace the slow USB1.1 card.

DAQ test-board status

With initial versions of all hardware components in place, the main focus over the last half year has been on firmware development. The ROC emulator firmware (T. Durkin) has been completed. The most crucial firmware module needed for the project is the decoder for 160MHz serial data from a readout chip.

This allows a bit-by-bit comparison of ROC readout data on a PC with known test patterns sent by the ROC emulator. Difficulties with clock routing on the low-cost Spartan-6 FPGA used for deserializing caused a delay of several weeks, but, as of February 2012, this most important part of the firmware works reliably. Focus is now shifting to testing the hand-over of data from the deserializer adapter to the DAQ test-board.

Progress has also been made with improvements to the connection between DAQ test-board and PC via the new USB2 module (G. Zhang). At the time of the last report, USB2 daughter cards were already in place, but the communication between the DAQ test-board FPGA and the USB bus was still using an asynchronous protocol which is incapable, due to timing limitations introduced by the handshaking protocol used for data transfers, of making full use the high speed mode offered by the USB2 controller chip. Switching to a synchronous protocol with block transfers between FPGA and USB2 controller will enable much faster transfer speeds, but requires modifications to the core part of the DAQ test-board firmware. This is nearing completion now. Firmware modules for synchronous data transfer have been completed, and interfacing these components to the remainder of the DAQ firmware has started.

The digital ROC readout hardware is one part of the RAL contribution to a beam test of the digital ROCs, currently foreseen for July 2012. Plans are also being made for contributions to subsequent beam tests, as a means of developing the hardware and DAQ systems needed.

Longer term plans

The UK proposal to design a new DAQ system for the phase 1 upgrade pixel detector, based on FEDs using a μTCA form factor, was accepted. The technical specifications for these new FEDs have been discussed with the CMS tracker community, in a common pixel-strip tracker DAQ working group, and a detailed technical proposal is being prepared, led by K. Harder and M. Pesaresi.

During LS1, CMS is planning to mount a small number of pilot blades in the currently unused locations for a third set of forward pixel disks. This will allow to verify the operation of the new front-end readout under real LHC conditions as well as ensure there are no unexpected effects which might degrade performance.

6.3 Deliverables

This work-package is a new one and therefore did not have a formal plan with milestones and deliverables from the outset. As described above, the scope has now matured since the document was submitted specifying possible RAL PPD activities in July 2011. We are in the process of developing a long term plan, involving all of the UK groups, with appropriate milestones, deliverables and cost estimates for inclusion in the PPRP submission. Meanwhile the most significant items from the RAL DAQ test-board activities are now included in the present work plan, which is still being adapted to the overall pixel project plan. In particular, the exact schedule for working ASICs is subject to change which clearly influences this activity. If the timescale permits, some support will be provided by RAL PPD for pixel module tests in test beams in 2012.

Milestones for this work package, as it was then foreseen, were listed in the original project document submitted to the oversight committee in July 2011 for development of DAQ test-boards for the digital ROC, for test beam DAQ, and for DAQ integration for pixel pilot modules. The present planning is adapted from that. The following milestones have been met or have had significant recent activity towards their completion:

Existing milestones

Design adapter board for connection to pixel modules. This is no longer relevant. The current deserializer adapter features a slot for a single ROC on a carrier PCB. It was originally planned to design a second revision with a connector for a pixel module once specifications for these connectors are decided upon by the PSI group. This decision has not been made as of February 2012, and thus it was decided to pursue an alternative option of mounting the module connector, once available, on a carrier board that fits into the slot for a single ROC. This eliminates the need to make any modifications to the deserializer adapter to accommodate modules.

Build prototypes of the deserializer adapter. (done)

Modify firmware of existing test-board to accommodate input of new readout chip.(ongoing) The decision to use an FPGA as deserializer on the adapter board, as opposed to hardwired electronics, meant that a lot of the firmware work moved away from the existing Altera test-board to the FPGA on the adapter board. The latter part is done, the former part is much less problematic than originally foreseen. Expected completion in March 2012 will still be several months ahead of the arrival of the first digital ROCs.

New milestones

μTCA test system in RAL. In view of progress with firmware development and hardware concepts for the pixel FED upgrade, a test stand is being set up for the new μTCA system. A μTCA crate is on order, and a mini-T board serves as a first FED prototype (without front-end optics in this revision). Pixel FED firmware and software development is making use of existing deserializer adapter prototypes, which are compatible with future FED hardware in several important respects.

DAQ test-board operation with pixel modules. This will be required in the lab and possibly, should time permit, in beam tests.

Development of specifications for the new pixel FED. This should be achieved before the submission of the pixel TDR and the PPRP proposal. However, it is expected to require further details so it is divided into two stages, with a second milestone proposed for the end of 2012.

Performance evaluation of DAQ board using pixel modules. A report should be produced summarising the performance of the DAQ test board using pixel modules before the end of the R&D phase, as a means of providing input to the final design.

6.4 Staff on project

Reported in accompanying tables. Since the last report to the oversight committee, the review of RAL PPD has concluded. RAL PPD staff levels available for the CMS pixel detector upgrade are expected to remain stable for the future.

6.5 Expenditure

The only expenditure is staff costs on RAL PPD, and at present there is no other budget allocation. Other costs are being absorbed by WP2, the travel budget and the RAL PPD budget for modest consumable expenditure.

6.6 Comparisons with CMS activities elsewhere

DAQ hardware for the digital readout chip is being developed at PSI as well as RAL. PSI is developing a board for use in special tests (wafer tests, chip debugging), whereas the RAL hardware is optimised for generic DAQ use especially with high data rate (test beams). Both groups work together and exchange hardware design blocks, firmware modules, and soon also software components to avoid unnecessary duplication of work. For example, the USB2 firmware developed at RAL is likely to be used for the PSI design. Schematics for power circuitry for the digital ROC has been developed at PSI and will be used in the RAL design. Overall, it is considered sufficiently crucial to have working readout systems available as soon as the new readout chip arrives that development of two systems is considered appropriate. From November 2012 on, both CERN and Fermilab will be in extended shutdowns affecting all test beam areas, making it very difficult to run chip tests under realistic LHC-like conditions before commissioning of the pixel pilot blades. With the digital chips expected in late

May 2012, there is not much time for revisions. On a mid-term timescale, the RAL deserializer board will become part of the pixel FED development.

A similar approach is taken with the pixel FED development. The μTCA pixel FED will replace the pixel detector DAQ for the Phase I upgrade. While we consider it feasible to have sufficiently developed prototype systems available to run with the pixel pilot system, a backup approach of modifying existing pixel FEDs for digital readout will be pursued by Vienna, Vanderbilt and Kansas State University. These modified FEDs are unlikely to be usable beyond the pixel pilot project, but provide additional risk mitigation for the needs of the project within the next couple of years.

7 Risk register

The current version of the project risk register is v5.0, revised from the version presented at the last meeting. Each line of the risk register has been reviewed recently and comments have been added where appropriate. Several risks have been retired in view of progress, changes in external circumstances and completion of many steps.

8 Finances

The financial report is summarised in the attached tables.

The STFC finance reporting system via the Research Councils Shared Services Centre is now generally reliable and usable. However, it only covers the TD and PPD staff elements of the project, and travel expenditure.

The staff costing model used for PPD requires some adjustment of the figures for internal STFC accounting reasons, which has not been included.

Upgrade travel spend has continued to increase, with beam tests, more frequent meetings in CERN and a workshop in FNAL in November 2011.

Equipment spending, which covers mainly ASIC foundry costs and trigger board manufacture, is increasing and will increase substantially in the coming year. The CBC-2 submission will require a substantial commitment and MP7 board production, including high cost FPGAs, are expected to require most of the remaining budget held at Imperial College.

Engineering staff spending at RAL has also continued to be high in view of the activities on the CBC-2 design, as expected. We are warned of a possible increase in TD staff overheads from 73% to 88%, whose start date has not been confirmed.

The Working Allowance currently stands at £220k. It has not yet been reduced but much of it will be used in the next six months to accommodate use of TD staff and CBC-2 and MP7 production.

9 Gantt chart

The Gantt chart has been updated as follows:

- there have been no major changes to the overall LHC schedule since July 2011[4], except for the details of the LS1 dates following the 2012 LHC Chamonix workshop[5].
- TDR dates for both the pixel system and L1 trigger have changed.
- A version of the simplified schedule for the Phase I pixel Tracker upgrade, based on current planning, is included. It foresees installation of the new pixel system in an extended Technical Stop at the end of 2016. This is not formally agreed but has been adopted after discussion with the LHC accelerator management as a working hypothesis, which will be adapted according to progress with the pixel construction project and the realities of machine operation, including the need to install major systems, such as Linac-4. If this does materialise as planned, the subsequent LHC schedule is also likely to change.
- A simplified version of the Trigger schedule is included. The trigger project currently does not have an agreed schedule for the upgrade, which is a concern and being addressed, so our estimate of the major activities is used.
- The UK project schedule has been updated to include the main milestones of the work packages, and include new ones.
- Finally there is a simplified section indicating the next steps for Phase I upgrade planning for the UK which will culminate in the PPRP proposal for longer term funding of a UK upgrade project and R&D for the Phase II tracker.
- The Phase II Tracker upgrade plan is in the original file, but not in the printed version.

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[4] http://indico.in2p3.fr/contributionDisplay.py?contribId=969&confId=5116
[5] https://indico.cern.ch/conferenceDisplay.py?confId=164089

10 Milestone reporting

The format for milestone reporting which we were requested by STFC administrators to use, namely a Word document in tabular format, is cumbersome and time consuming to complete. The sections of the table for achieved and imminent milestones are in a different format from the overall list, and there are columns which appear to add little or no useful information without a more detailed account. It has not been a very helpful tool for managing the project, especially in an R&D phase, although such snapshot information might be more useful for a construction project. Much more time managing the project is spent in individual or group discussions and these rarely lend themselves to consolidation in simple table form suitable for OSC reports. While inclusion of milestones in the document may be less desirable for a mere overview, it is easier to record and more informative.

For future reporting, we would like to suggest that some thought be given to a different method. it would be more valuable if it lent itself to completion by individual milestone “owners”, could be accessed from different sites and was more naturally adaptable to other tools, such as Gantt charts. We do not know if such tools exist.

Gantt charts also require specialised software which is not accessible to all participants. Currently several of us use Microsoft Project or Merlin, which is a Mac application similar to and compatible with MS Project. Although Gantt charts are often useful, we have not found them valuable at the top-level of this R&D activity. Individual activities, such as ASIC design or trigger board design, often employ Gantt-type reports but often they do not use a standard tool and are too detailed for top-level management. They are also very hard to assemble into a single Gantt chart when completely different methods are used to produce them.

Many of the reporting methods might be well suited to a construction project with a modest R&D element, taking place in a single location. They seem less well adapted to an international collaboration in particle physics, especially during the R&D and early planning phase, when many things are changing substantially, as has been the case here.

Appendix: Calorimeter Trigger Review report

Included as separate document