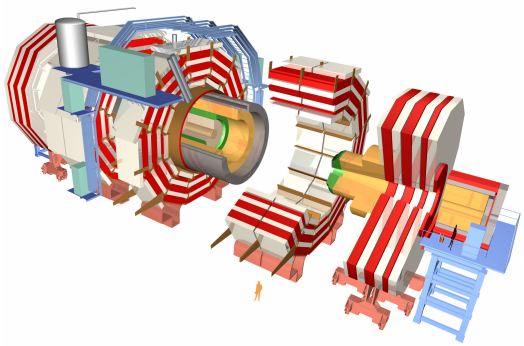
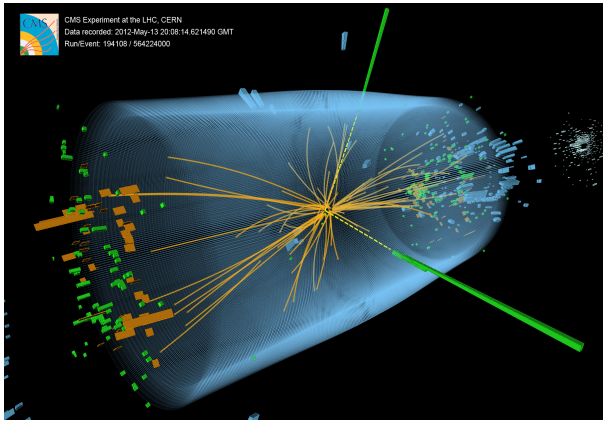




UK CMS Upgrade Oversight Committee

26 March 2013

University of Bristol
Brunel University
Imperial College London
Rutherford Appleton Laboratory

Geoff Hall

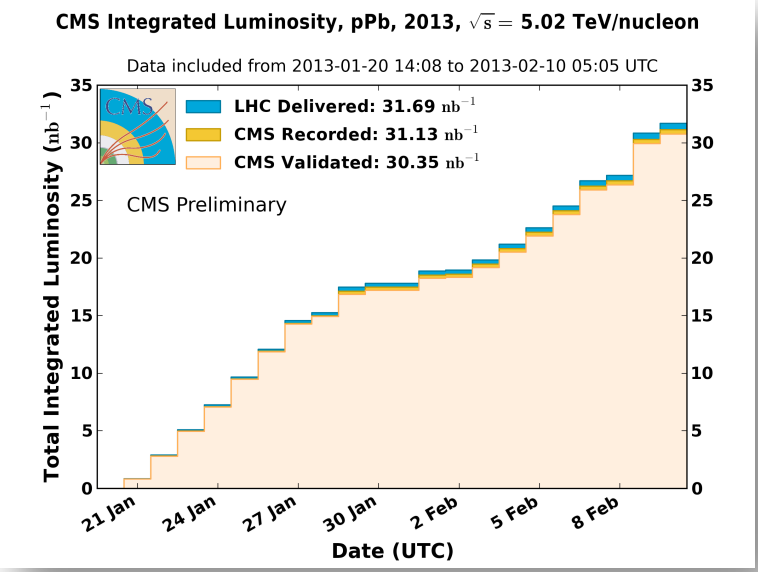
Overview

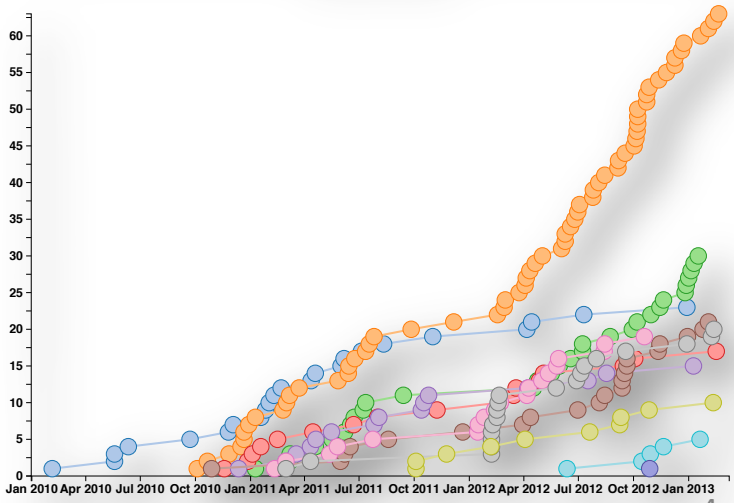
- Snapshots of CMS & LHC status
  - LHC future plans
- Summary of project
  - Recent WP progress
  - Comparison with original goals
    - Although the project has not fully ended financially, it has effectively been completed and met, or exceeded, the original goals. For this reason, there is more technical detail than usual (for illustration, or questions).
  - Won't credit everyone individually but would like to draw attention to many important contributions
- Finances
- Final (?) remarks

CMS and LHC STATUS

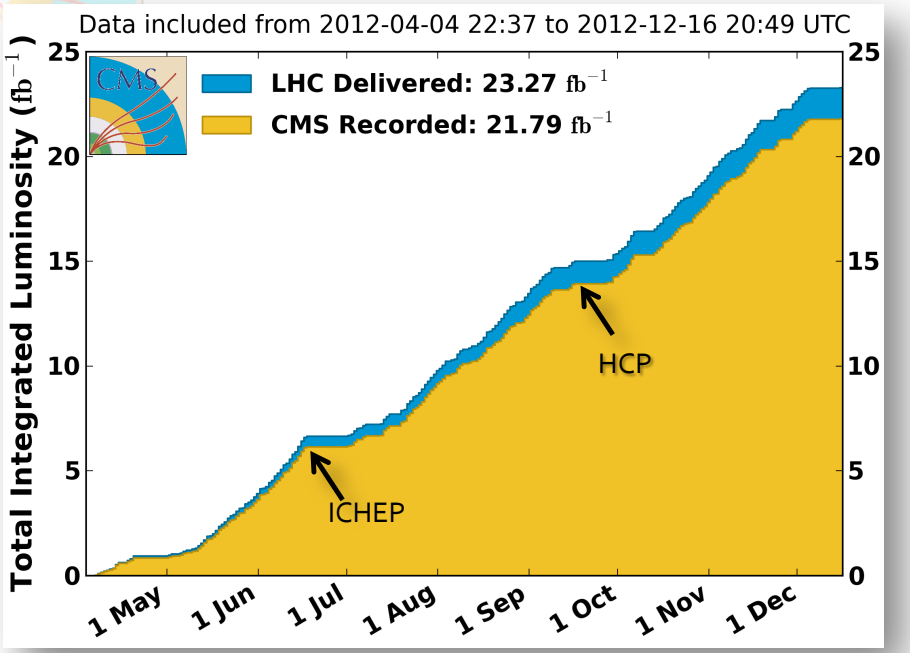
Overall status

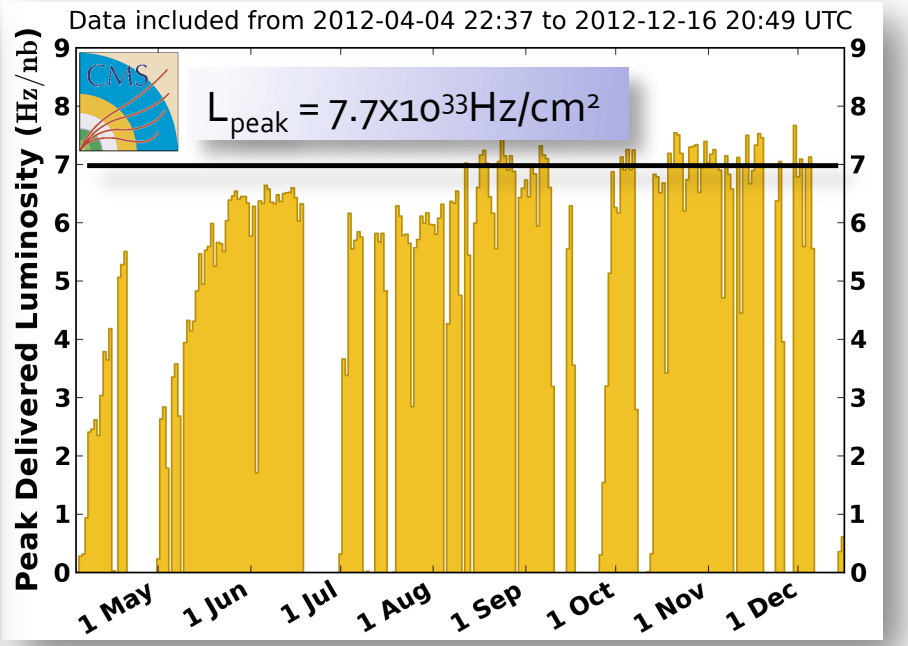
- LHC met, and exceeded, L_{int} target for 2012
  - steady increase in data taking efficiency from automating procedures
- Successful Pb-p run to mid-February
  - LS1 now underway
- Successful machine tests at end 2012 with 25 ns operation
- Physics output still steadily increasing
  - >200 papers, ~120 papers per year





Data delivered and recorded in 2012





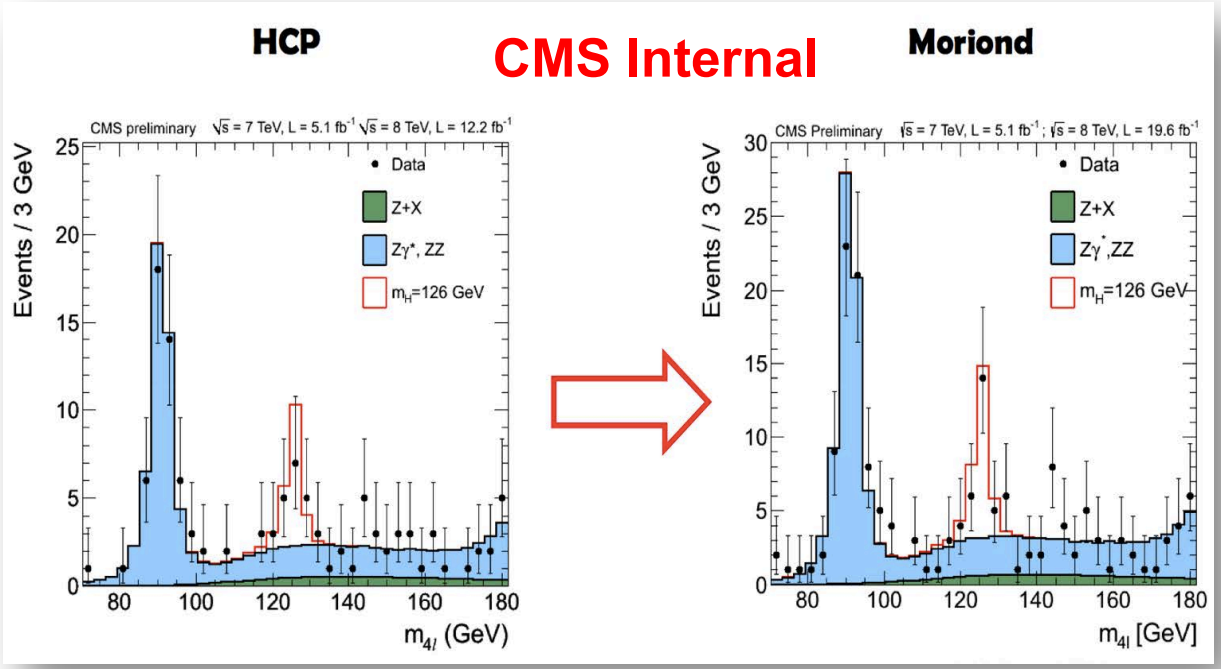
Period	Delivered* fb^{-1}	Recorded* fb^{-1}	Efficiency	Downtime	Dead-time
April - June	6.78	6.26	92.3%	5.9%	1.8%
July - 21Aug**	4.97	4.73	95.1%	3.8%	1%
22Aug - 16 Sep	2.99	2.74	94.4%	4.1%	1.5%
26 Sept – 7 Oct	1.44	1.37	95.1%	3.4%	1.5%
9 Oct – 3 Dec	6.9	6.5	94.8%	3.7%	1.5%

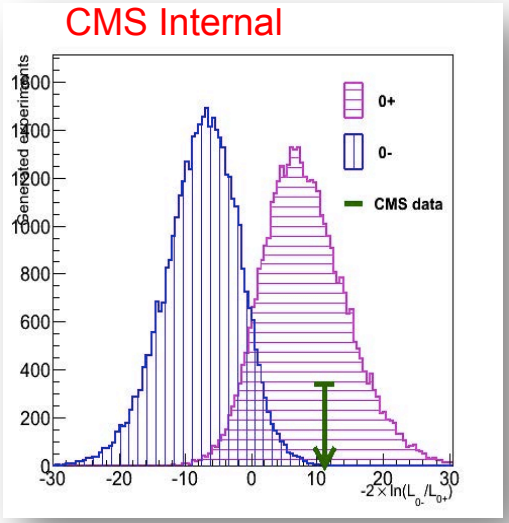
2

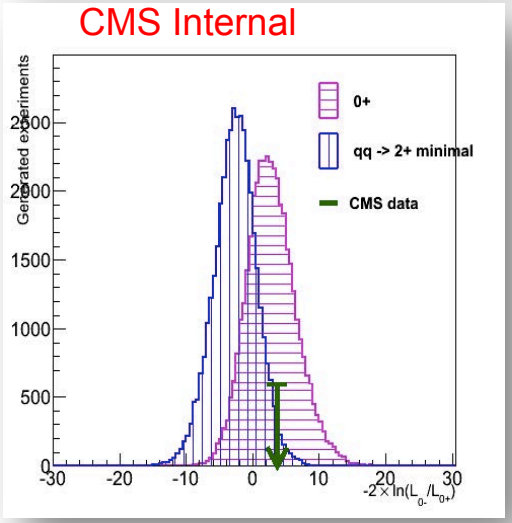
CMS Overview MB 166

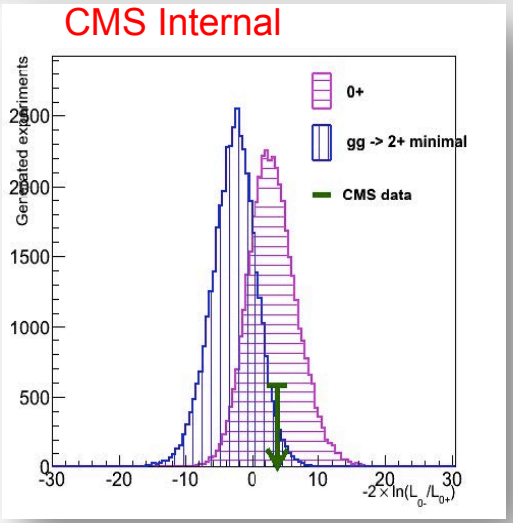
Joe Incandela
UCSB/CERN

February 11, 2013









LHC future plans

- No major changes recently, or expected
  - internal discussions about LS2 date
  - knock-on effects & other uncertainties beyond that

- Long term plan: Long Shutdowns (*later dates may change*)
  - LS1: March 2013-2015 - upgrade to full energy
    - 14 TeV, 25 ns bunch spacing, $L_{inst} < 2 \times 10^{34}$ cm^{-2}s^{-1}
    - 25 ns looks more promising following Dec 2012 tests
  - LS2: 2018 - improve collimation and other machine elements
    - 14 TeV, $L_{inst} < 4(?) \times 10^{34}$ cm^{-2}s^{-1}
  - LS3: 2022 - upgrade for very high luminosity
    - 14 TeV, $L_{inst} \sim 5 \times 10^{34}$ cm^{-2}s^{-1} (levelled)

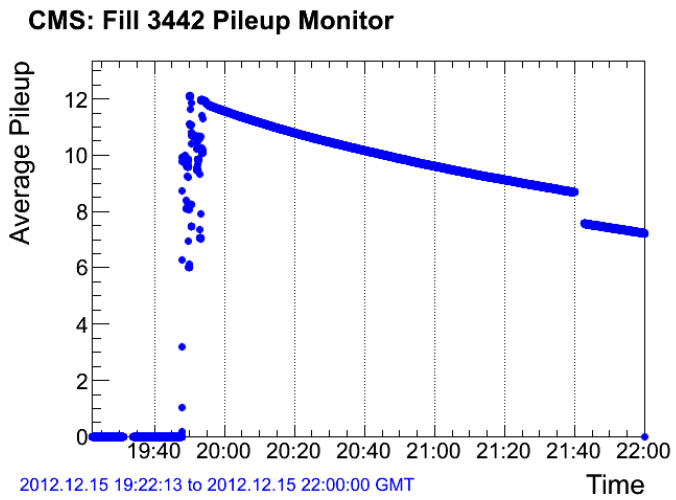
Summary

Summary from the 2012 scrubbing run at 25 ns From G. Iadarola at Evian 2012

- The 2012 Scrubbing Run has lowered the **SEY in the arcs to less than 1.45** resulting in a **reduced heat load** as well as **improved beam quality** (lifetime, emittances)
- In spite of the high heat loads, close to the cryogenics limit, **the second part** of the Scrubbing Run and the ramps to 4 TeV **did not exhibit any clear improvement** in the conditioning state of the arcs (to be investigated with additional simulations and lab measurements)
- **Emittance blow-up ascribable to EC is still observed** at injection energy with **long and closely spaced trains**
- **At 4TeV, no indication of further emittance deterioration** driven by EC
- A concentrated scrubbing run will be likely to **be insufficient to fully suppress** the EC from the arcs for 25ns beams in future operation.

25 ns physics fills in 2012

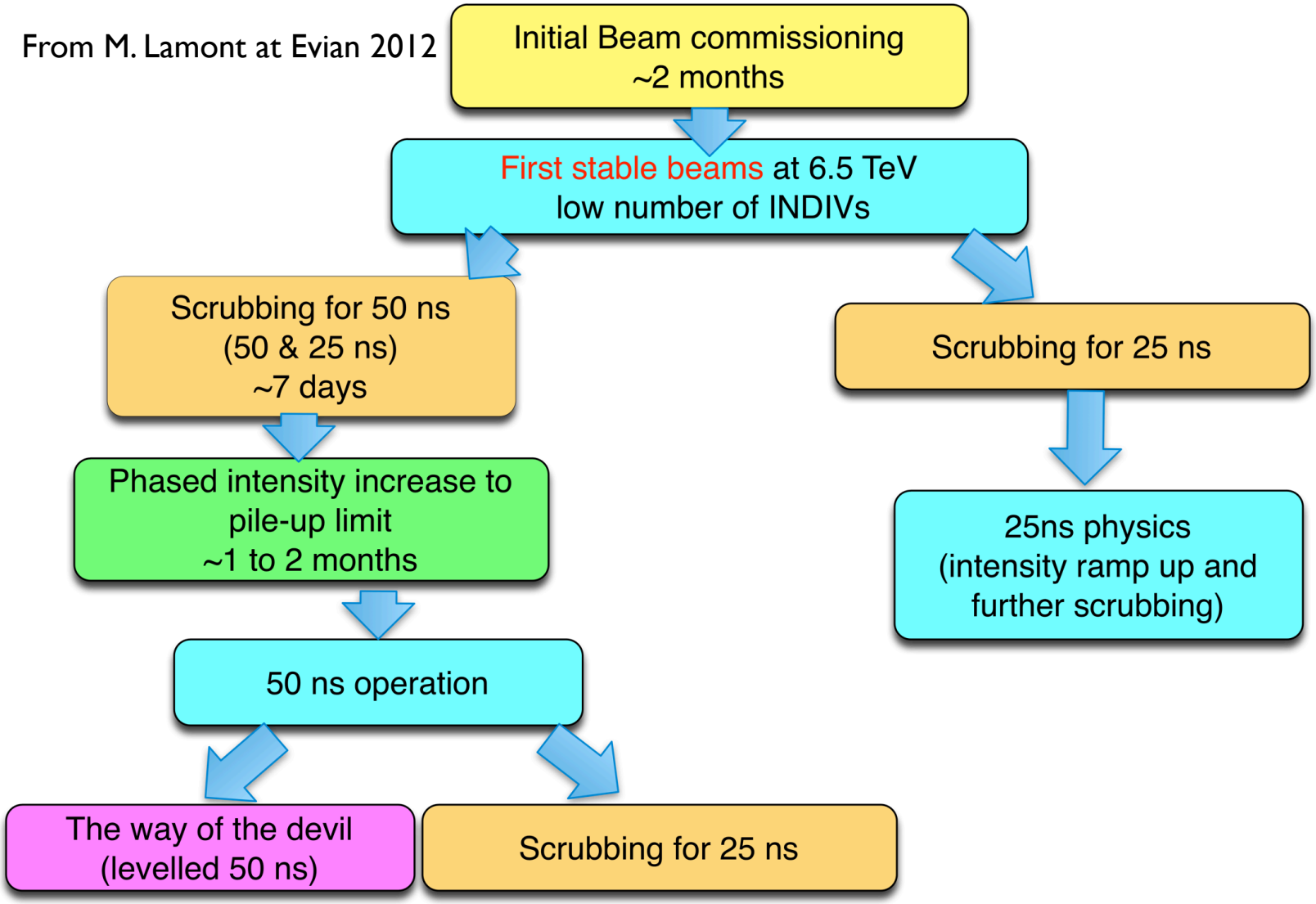
- Three physics fills with 25 ns bunch trains at 8 TeV:
  - Very low emmittances
    - Emmittances from 1.85um to 2.03um (half of nominal emmittance for 25ns beams)
  - Observed UFO rate between 5-10 times larger compared to 50 ns (not so bad)
    - None of the UFOs produced a beam dump
    - UFO are dangerous when losses are higher than Beam Loss Monitor Threshold → beam dump
  - Peak pile up 12 events/crossing at the beginning of the fill, beta*=1m
  - Nearly 400 bunches injected for the last physics fill
  - Tried a fill with 800 bunches but beams dumped by ALICE



Total delivered luminosity 14/pb
Recorded luminosity13.8/pb

Fill 3441 (108 bunches)
Fill 3442 (204 bunches)
Fill 3453 (396 bunches)

From M. Lamont at Evian 2012



M Lamont
17 Jan 2013

10 year plan

	J	F	M	A	M	J	J	A	S	O	N	D
2011		1	2	3	4	5	6	7	8	9	IONS	
2012			1	2	3	4	5	6	7	8	9	
2013	IONS	IONS	LS1 - SPLICE CONSOLIDATION									
2014												
2015	RECOM	RECOM	RAMP-UP	1	2	SCRUB 25 ns	3	4	5	6	IONS	
2016		RAMP-UP	1	2					7	8	IONS	
2017		RAMP-UP	1	2	3	4	5	6	7	8	IONS	
2018	LS2 (LIU UPGRADE: LINAC4, BOOSTER, PS, SPS…											
2019	RECOM	RECOM	RAMP-UP	1	2	3	4	5	6	7	IONS	
2020		RAMP-UP	1							8	IONS	
2021		RAMP-UP	1	2	3	4	5	6	7	8	IONS	
2022	HL-LHC UPGRADE											

LS1

PHYSICS AT 6.5/7 TeV

LS2 – Injector upgrade

"ULTIMATE" PHYSICS (~2.4e34 $cm^{-2}s^{-1}$)

LS3 – HL-LHC upgrade

- Technical stop or shutdown
- Proton physics
- Ion Physics
- Recommissioning
- Intensity ramp-up

Updates under discussion

Main CMS objectives for 2013

- Major challenges (*CMS SP March 2013*)
  1. Harvesting full 2011-12 dataset for physics
  2. LS1 consolidation, upgrades
  3. Phase 1
     - HCAL and Pixel TDRs complete and approved
     - L1 trigger TDR almost final. Submit to LHCC when cost scrutiny complete
  4. Phase 2
     - Establish first credible concept(s) for an affordable upgrade that outperforms current CMS, for Lumi up to 5E34 and <PU>~ 140
     - Establish broad support for R&D funding
  5. Run 2 preparations
     - Current [computing] resources/tools inadequate
     - In early 2014 a broad array of physics preparation exercises with 13 TeV MC samples will be necessary = similar to what was done in 2008-2009

UK R&D since 2009

UK CMS upgrade R&D achievements

- WP1 – software and simulations
  - IPbus (µTCA control) (10/11) adopted as common CMS-wide standard (02/12)
  - Simulation studies for trigger and tracker upgrade, and TDRs (09/12)
- WP2 – Outer microstrip tracker readout
  - CBC 128 channel ASIC (03/11) developed in single design iteration & evaluated
  - CBC2 254 channel ASIC submitted (07/12), with trigger data, received (2/13)
  - CBC2 lab performance and yield look extremely promising (3/13)
  - DAQ & FED studies, with CBC module beam tests (09/11)
  - FC7 design underway; submission (4/13)
- WP3 – L1 calorimeter trigger system
  - Mini-T5 (02/10) & MP7 (07/12) processor boards delivered and working
  - MP7 with final FPGA (2/13), with excellent performance
  - TMT architecture proposed (02/11) and adopted (12/12)
- WP4 – pixel DAQ
  - wrapping up, in view of PPRP decision

WP1 objectives and status

- (Recall that Phase I & II came after original proposal)

- Development of simulations and tools
  - important contributions to pixel TDR and tool development
- Online software/firmware for hardware tests
  - evolved into IPbus – in collaboration with WP3
  - additional work contributing to WP4 for pixel tests
- Tracker layout and track-trigger algorithms

- Some foreseen effort did not really materialise

WP1 Status

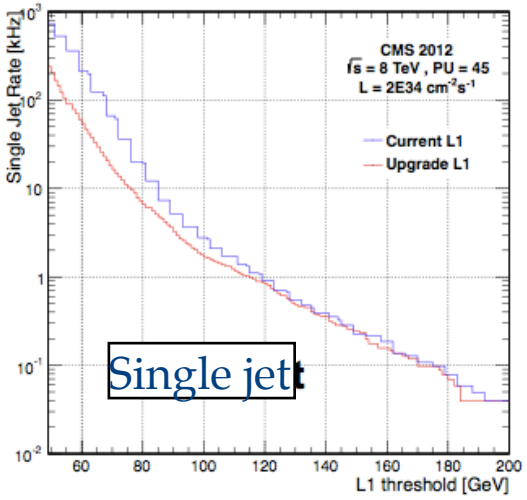
- WP1 goals
  - Software / simulation tools for upgrade tracking & trigger design
  - Online software / firmware for tracking and trigger prototypes
- Achievements in this reporting period
  - Pixel upgrade TDR approved by LHCC – M1.3.10, M1.4.3
  - Level-1 TDR studies completed (and document now in final stages) – M1.3.8, M1.4.4
  - IPbus system being used in anger for test-beam studies – M1.3.9
- WP1 status
  - WP1 does not continue as a single WP into the new project
  - On track to meet all project milestones by end of April 2013
    - Budget (essentially ~all personnel) very slightly underspent due to resignations
  - All current project personnel will continue – retention of expertise
  - WP1 deliverables form the basis for the future UK work

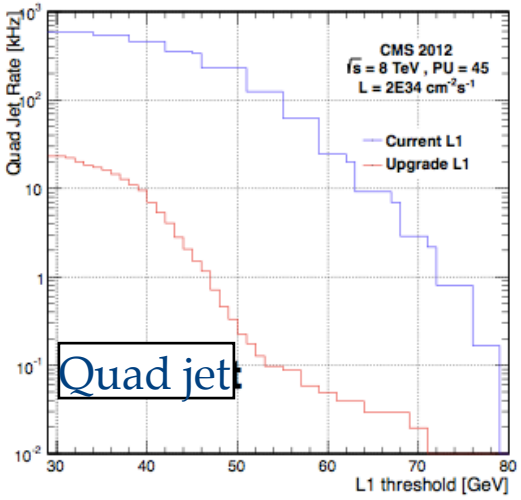
Level-1 Upgrade

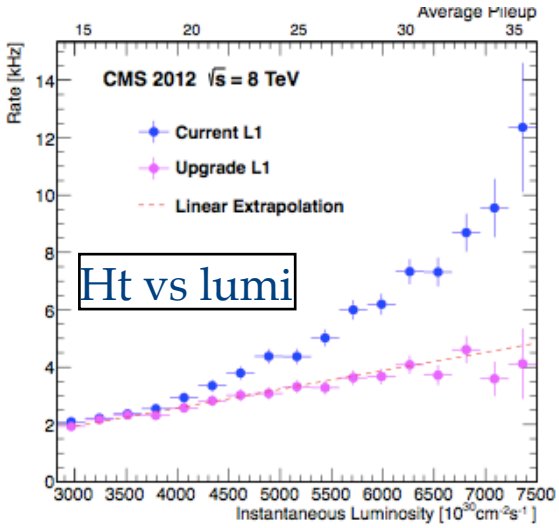
Algorithm	8 TeV 7E33 ~25 PU		14 TeV 2E34 50 PU	
	Thresh (GeV)	Rate (kHz)	Thresh (GeV)	Rate (kHz)
Single EG	22	10	46	10
Single IsoEG	18	9	31	9
DoubleEG	13, 7	9	22, 12	9
Single Muon	16	9	50	9
Dble Muon	10, open	5	35, open	5
EG+Mu	12, 3.5	3	21, 6	3
Mu+EG	12, 7	2	25, 15	2
SingleJet	128	2	188	2
DoubleJet	56	10	132	10
QuadJet	36	2	96	10
Double Tau	44	2	56	2
MET	36	7	84	7
HTT	150	2	511	2

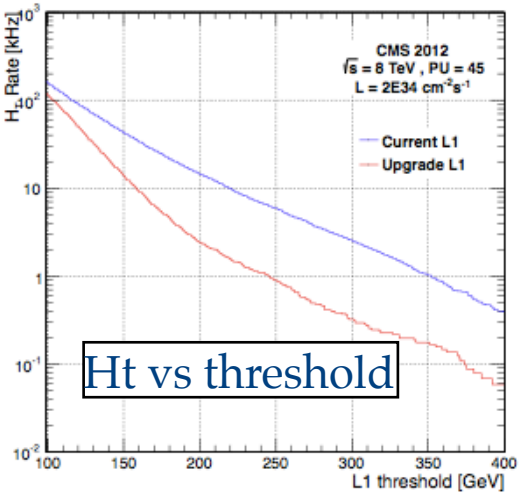
- Trigger thresholds
  - In the 'do nothing' scenario
  - 14TeV, 2e34, 50PU
    - Not even the worst case
  - Reminder: 'natural' lepton thresholds set by W, H mass
- Conclusions
  - Earliest possible L1 upgrade is essential
  - Physics impact of changes must be careful quantified
- Menu devt a UK task

Level-1 Upgrade Algorithms



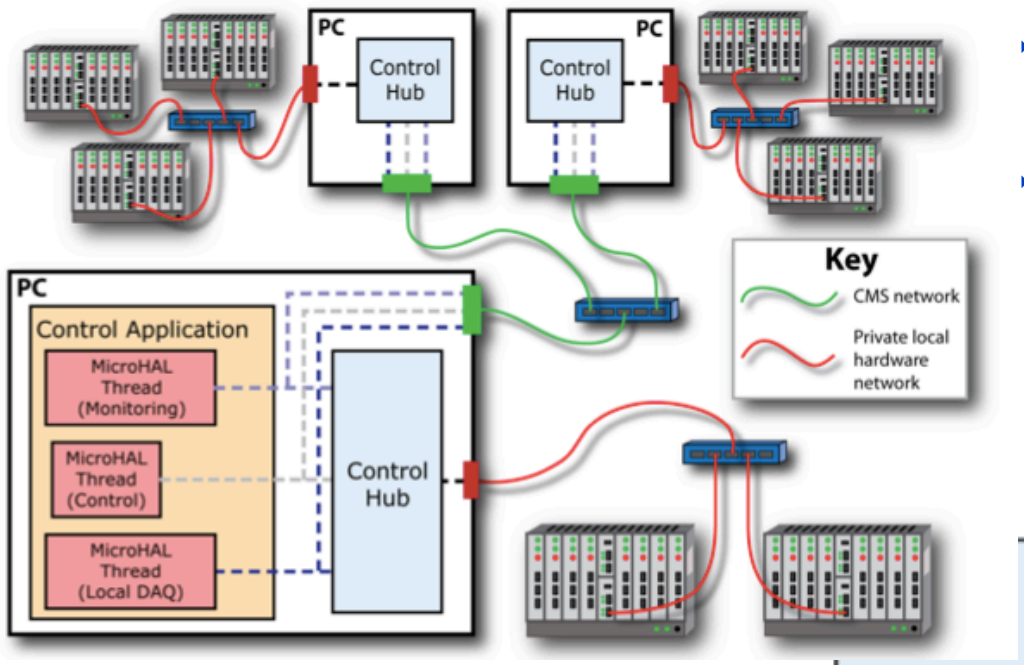




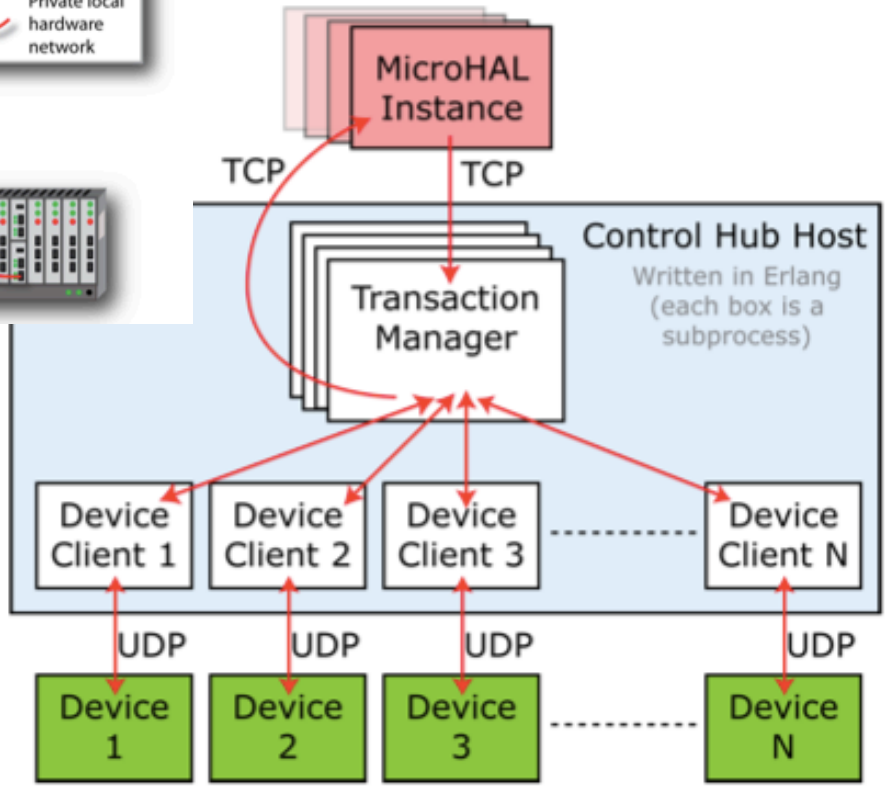


- Hadronic triggers dominate rates in high PU scenarios

IPbus Progress

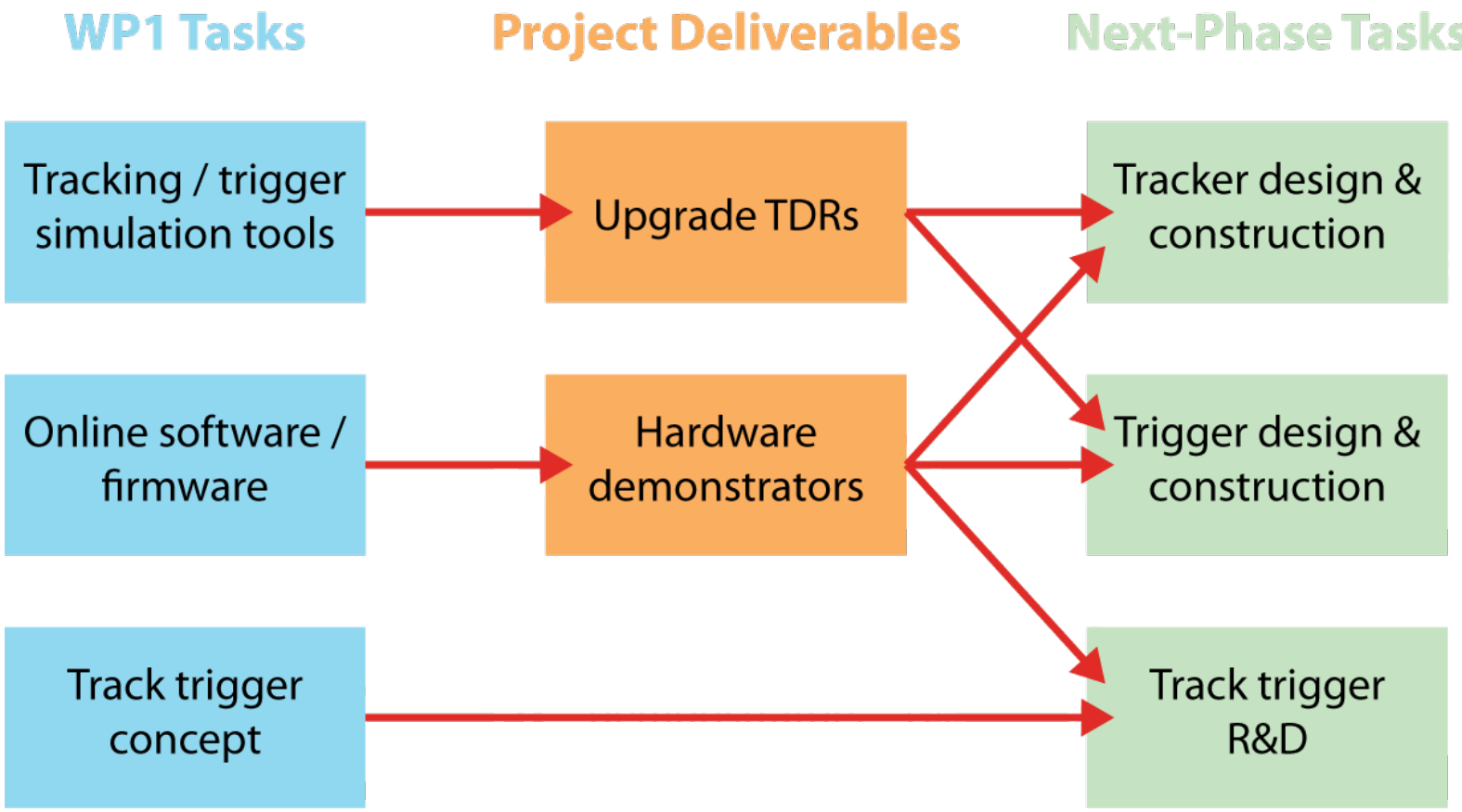


- Used as basis of successful pixel ROC test beam in 2012
- Used as basis of TMT demonstrator tests



- Control hub is now fully in CMS test environment
- IPbus 2.0 protocol is reviewed and accepted by CMS
- IPbus now in use by ~10 projects outside CMS

WP1 Future


WP1 Tasks
Project Deliverables
Next-Phase Tasks
Tracking / trigger simulation tools
Online software / firmware
Track trigger concept
Upgrade TDRs
Hardware demonstrators
Tracker design & construction
Trigger design & construction
Track trigger R&D

WP2 objectives and status

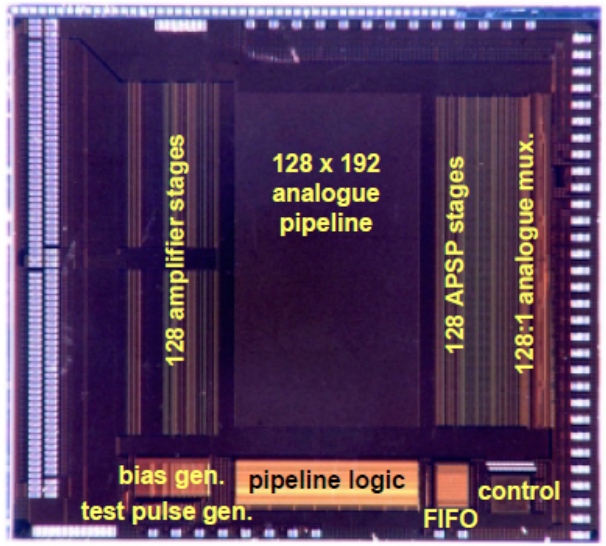
- Development of full size CMS Outer Tracker readout chip
  - expected submission and test of 128 channel ASIC
  - have demonstrated 128 channel CBC1, followed by 254 channel CBC2 ASIC for a trigger-tracking module, both working well

- Single channel FED prototype
  - demonstration work carried out
  - expected to benefit from trigger module developments
    - which proved to be the case
    - wheel has turned full circle (Tracker FED, APVe and FED tester initiated activities)
  - design of FC7 board for pixel FED and CBC module readout
    - generic-type board, to be utilised by multiple projects, in collaboration with CERN
      - (discuss with WP4)

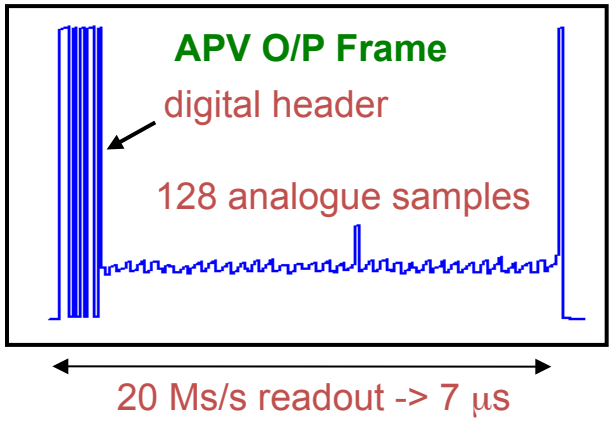
Mark Raymond

LHC -> HL-LHC

APV25

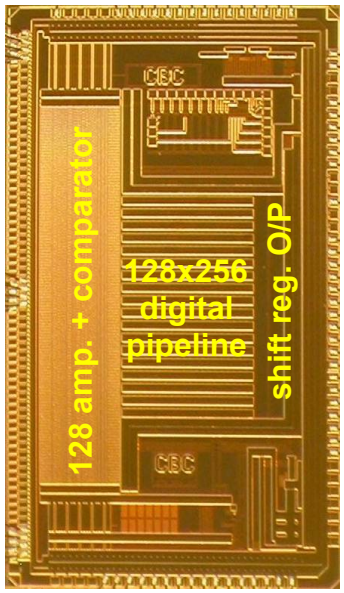


rad-hard 0.25um CMOS
unsparsified analogue readout
~ 3 mW / chan for 10-20 cm strips
analogue off-detector transmission

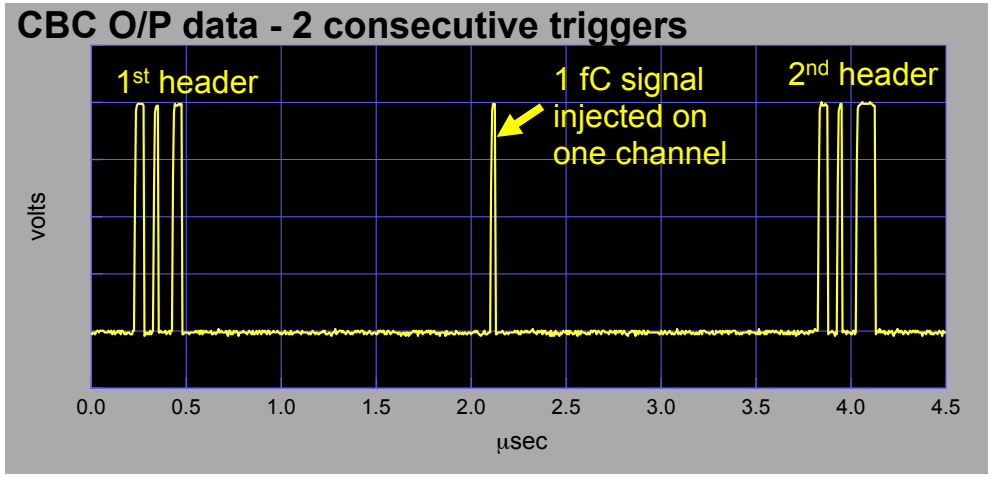


• digital off-detector links
• many more channels -> power becomes the big issue

CBC1



130 nm CMOS
unsparsified binary readout
(retain system simplicity but give up analog info)
target low-power for short strips



CBC1

features

- designed for short strips, 2.5 – 5cm, < ~ 10 pF
- full size prototype - 128 channels
  50 μm pitch wirebond
- binary un-sparsified **triggered** readout only
- powering test features
  2.5 -> 1.2 DC-DC converter
  LDO regulator (1.2 -> 1.1) feeds analog FE

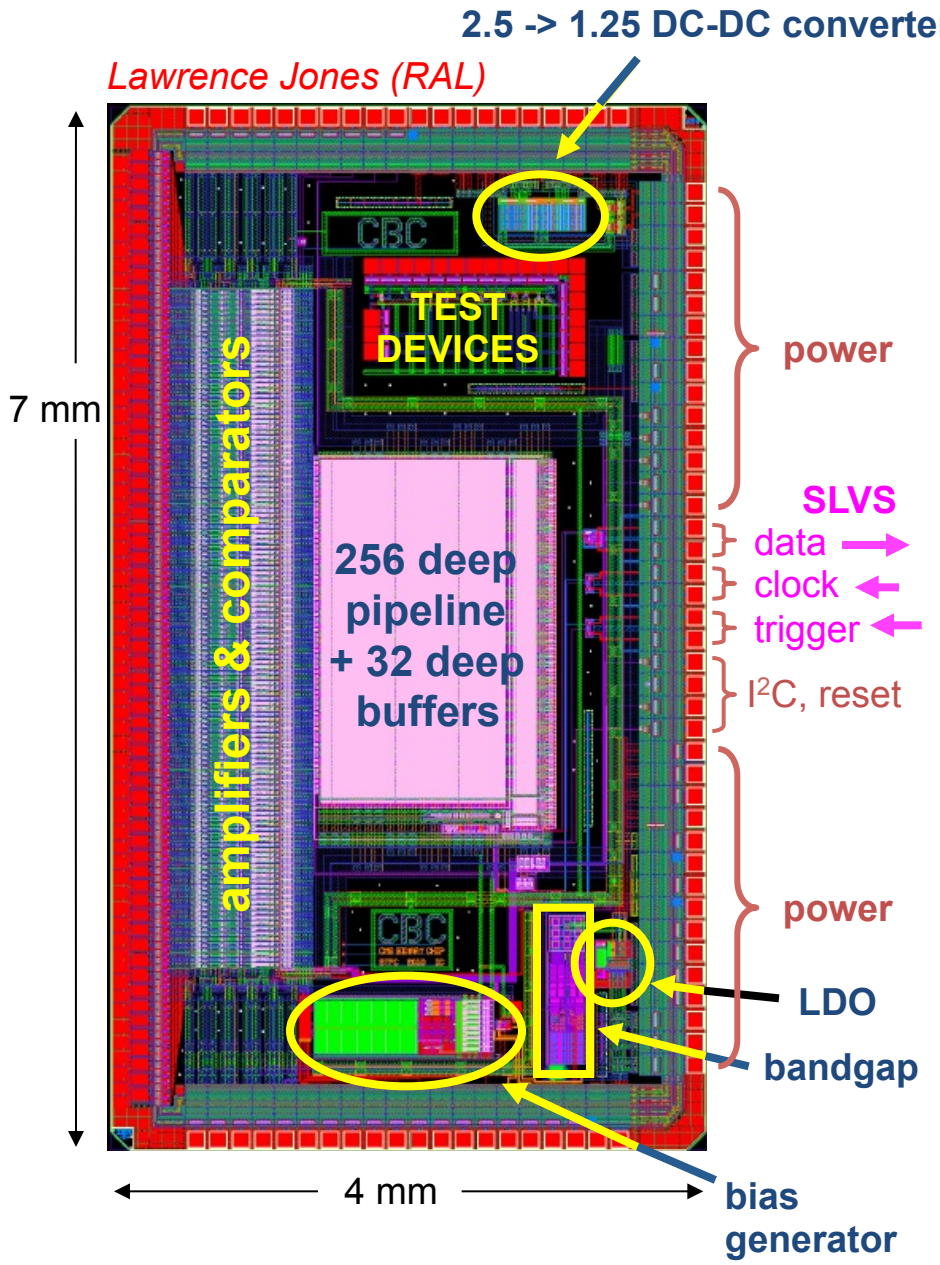
main functional blocks

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

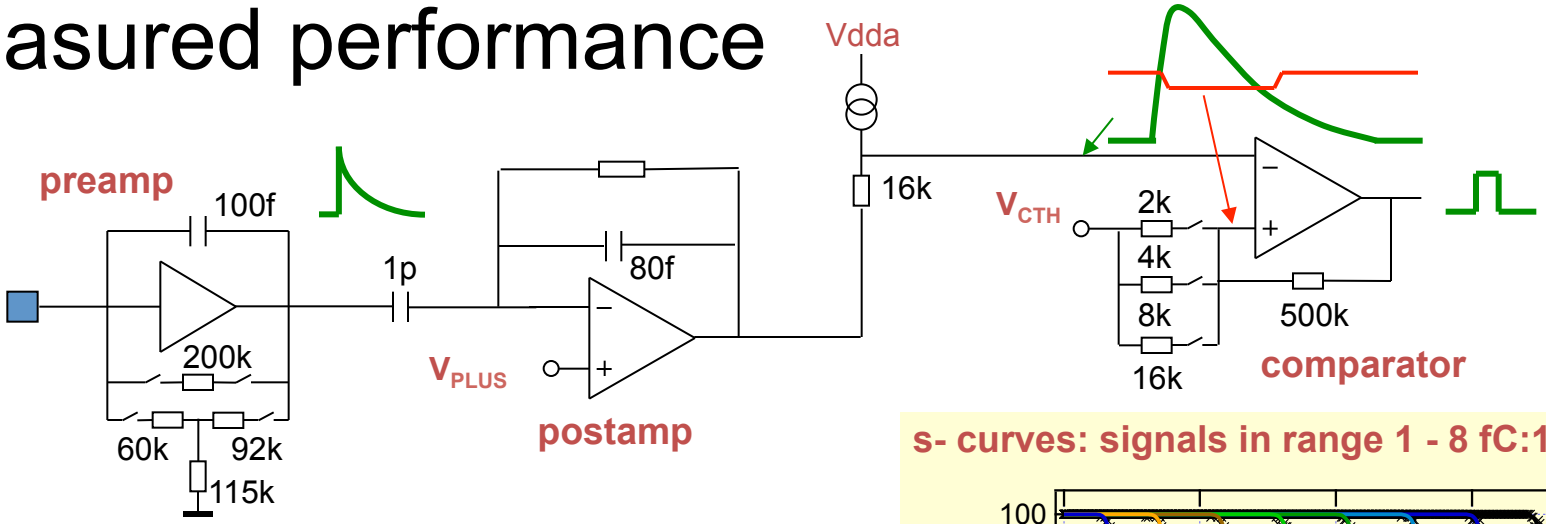
some target specs

- both signal polarities
- DC coupled to sensor – up to 1 uA leakage
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF

first chips received Feb. 2011



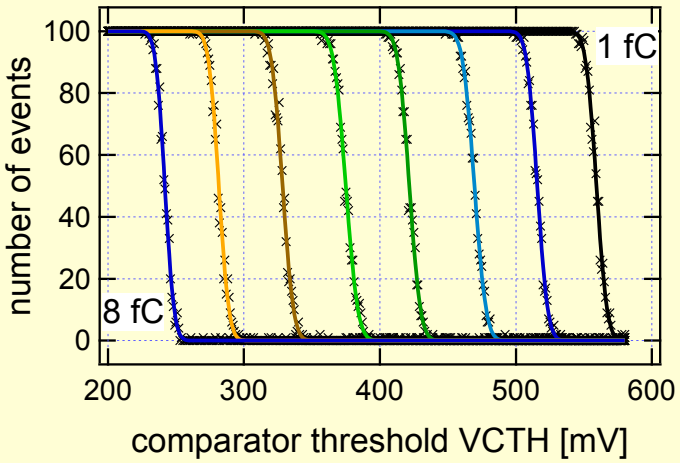
measured performance



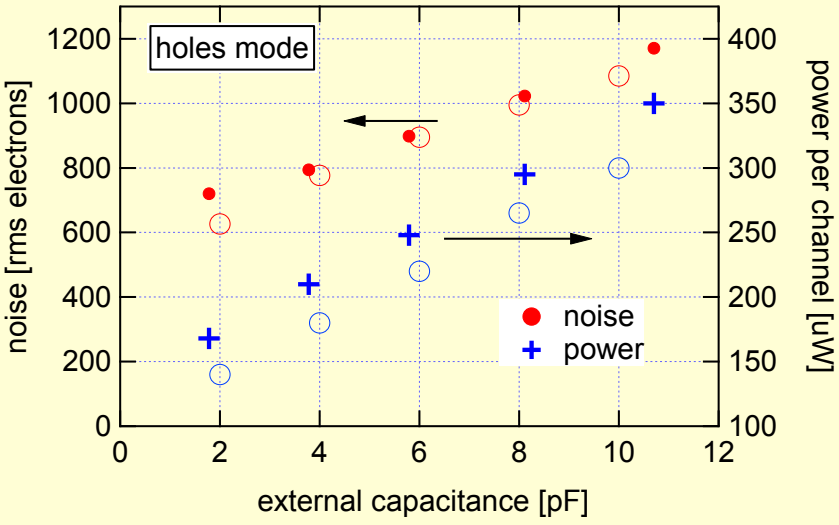
preamp: leakage tolerance 1μA verified, both polarities

postamp: gain: ~ 50 mV / fC

s- curves: signals in range 1 - 8 fC:1 fC steps



noise



noise dependence on external C

vary current in input device
=> pulse shape independent of C

e.g. for C_{SENSOR} ~ 8 pF (~ 5 cm strips)

~ 1000e achievable for
~ 350 μW tot. power/chan. (incl.digital)

comparator

thresholds

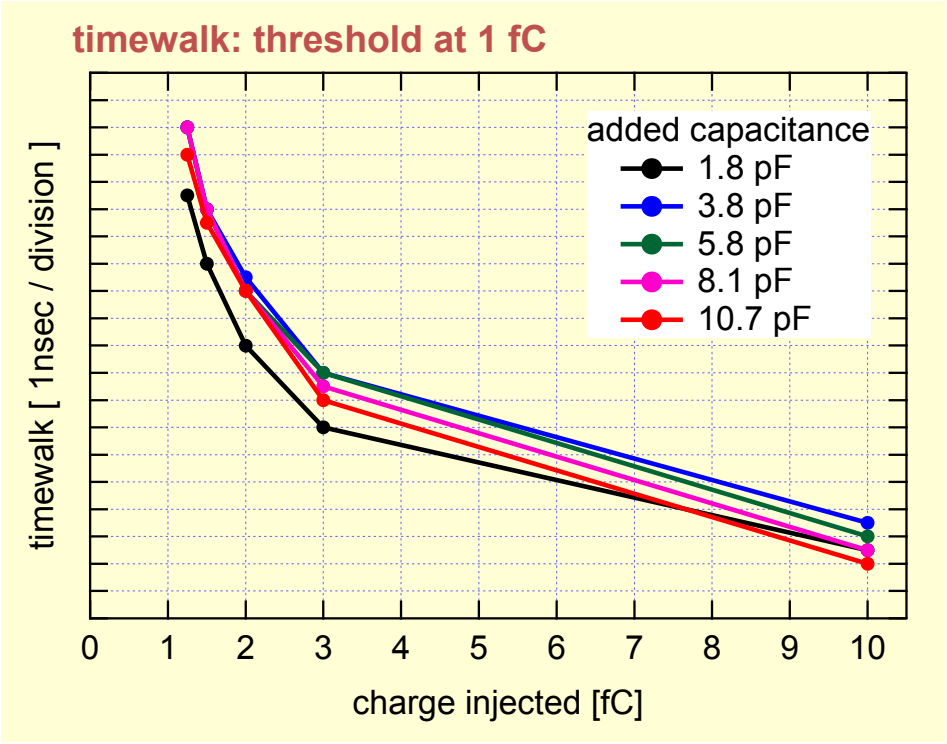
before tuning pk-pk threshold spread ~30 mV (~ 0.6 fC)

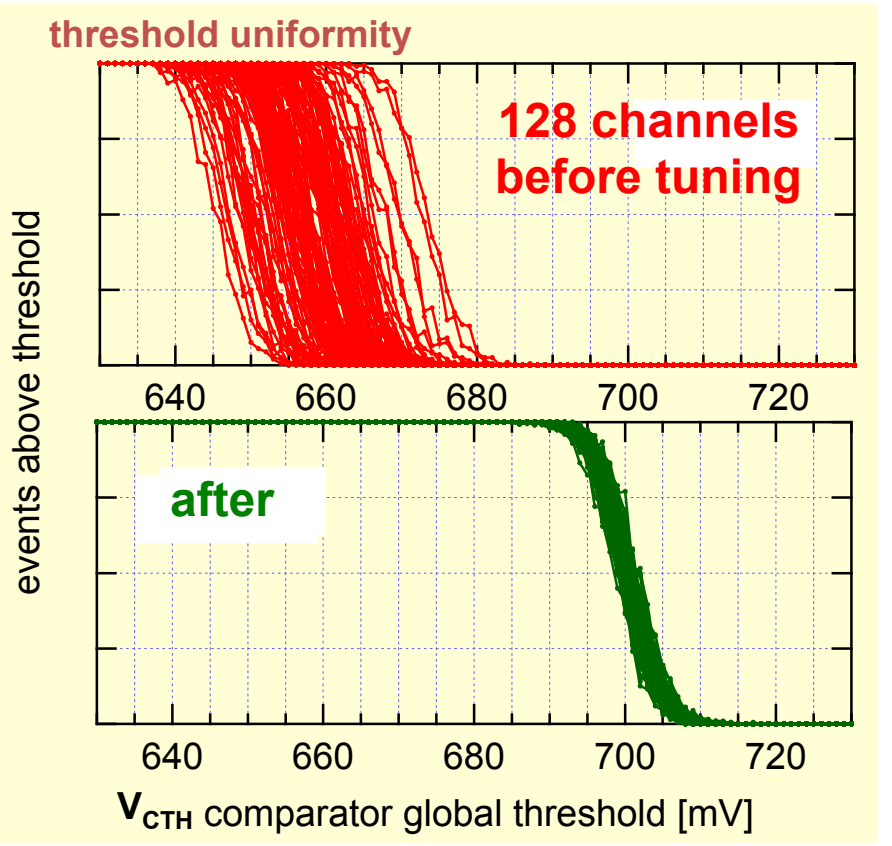
tuning reduces spread to ~ mV level

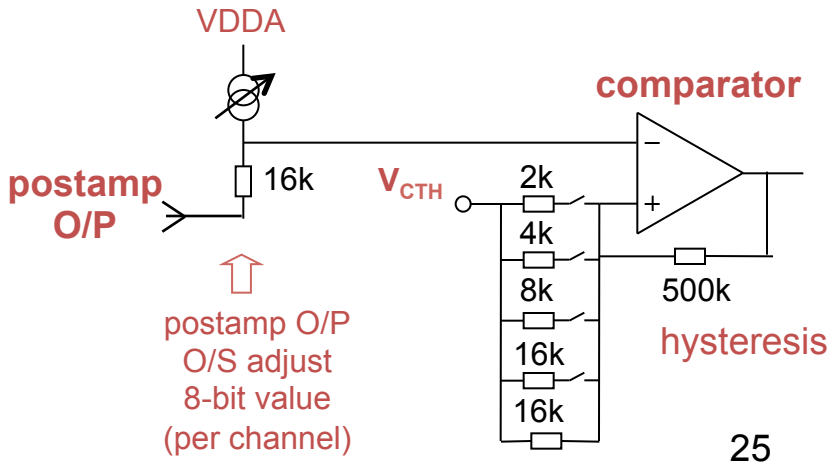
timewalk

timewalk spec.: < 16 ns between 1.25 and 10 fC signals, with comp. threshold set to 1 fC

measurements just within spec.







power features

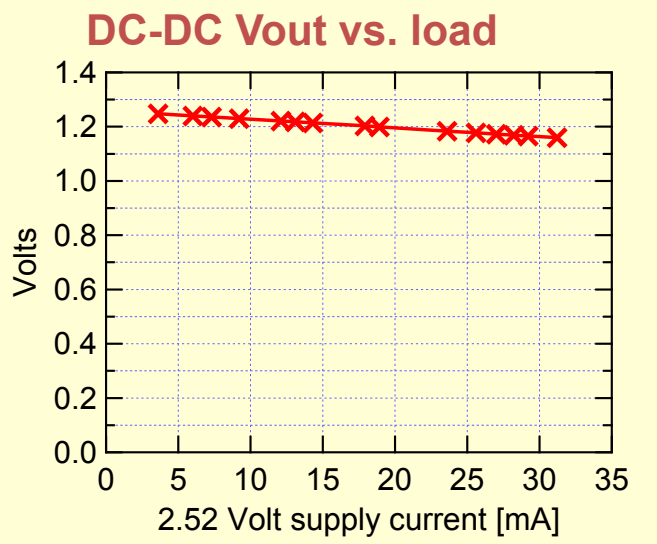
DC-DC switched capacitor converter (CERN)

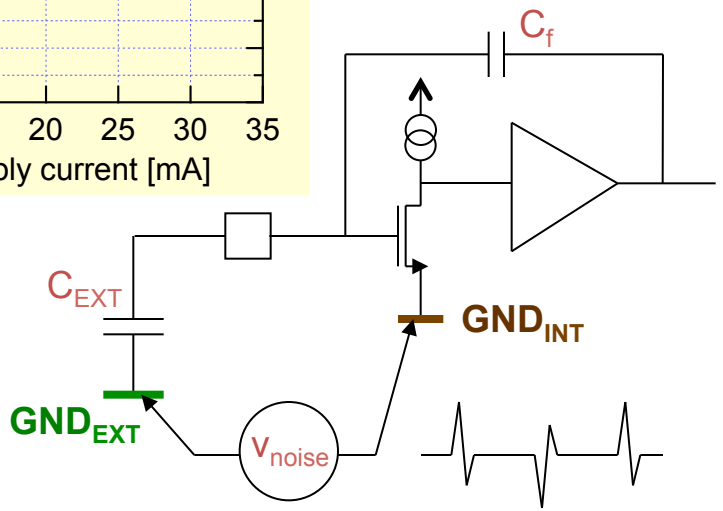
converts 2.5 -> ~ 1.2
works well: ~ 90% efficiency

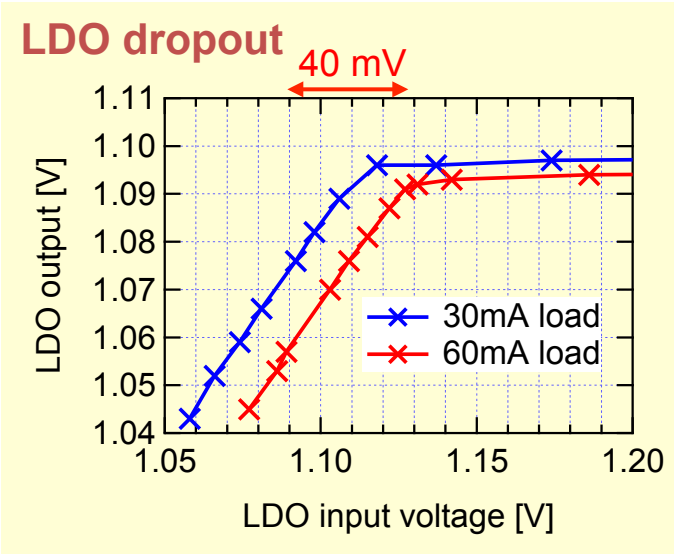
but switch noise produces difference between internal and external grounds

=> interference depending on C_{EXT}

improved circuit on CBC2, and bump-bonding should help







LDO linear regulator

provides clean, regulated rail to analog FE
(uses CERN 130 nm bandgap)

~ 1.2 Vin, 1.1 Vout

dropout ~ 40 mV for 60 mA load

provides > 30dB supply rejection up to 10 MHz

CBC1 summary

- **successful first prototype in 130 nm**

  most things worked - some bugs needed workarounds (front end CM stability issues)

- learned some valuable information

  e.g. performance vs. power trade-offs

  <1000e achievable for < 5 mW / channel (target specifications achieved)

- **performance verified in test beam**

- in the meantime... (2011 - 12)

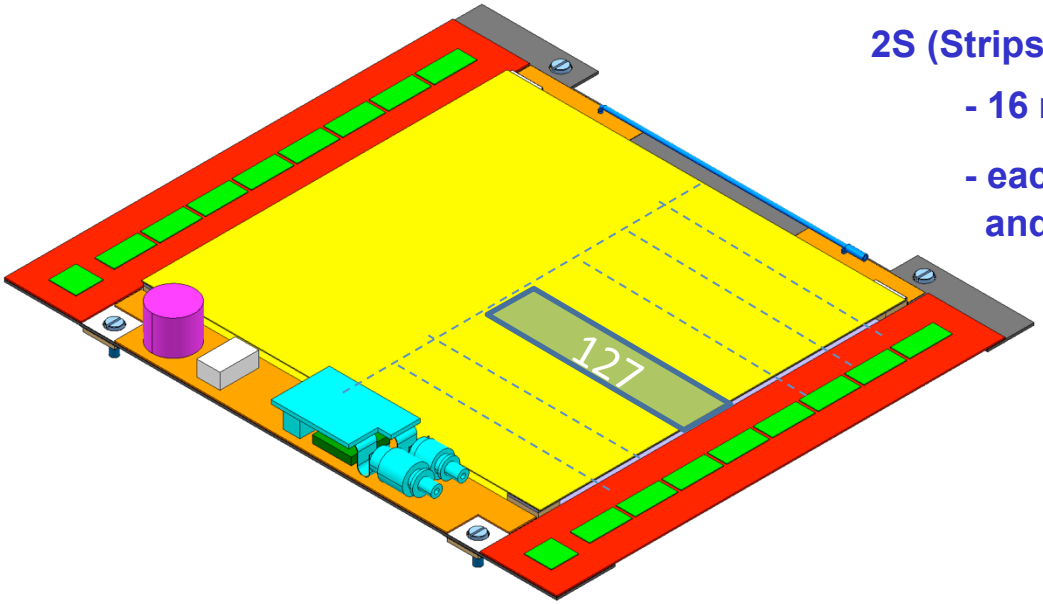
  2S-pT module concept developing

  ideas for implementing triggering functionality from strips in outer tracker

  ideas on simplifying module construction (bump-bonding)

  -> CBC2

CBC2 for 2S-Pt module



2S (Strips-Strips) module

- 16 readout chips

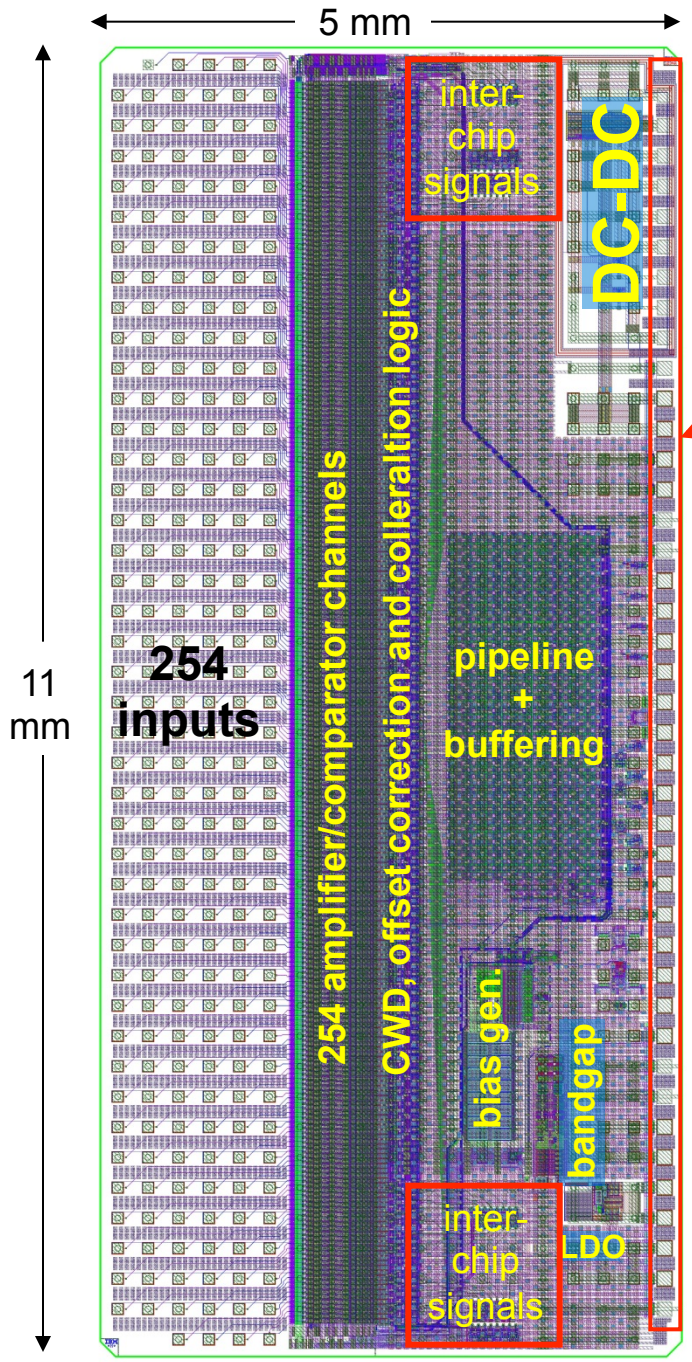
- each reads 127 strips from bottom sensor and 127 from top

CBC2

bump-bond chip, brings signals from 2 sensor layers in 1 chip (254 channels total)
provides L1 triggered readout data as in prototype
also performs cluster correlations to identify high Pt stub
positive correlation produces trigger output

=> functionality required to construct and evaluate prototype 2S-Pt module

CBC2 layout



C4 layout, 250um pitch, 19 columns x 43 rows

30 interchip signals (15 in, 15 out), top and bottom gives continuity across chip boundaries

right-most column wire-bond (for wafer probe test)

access to:

- power
- fast control
- I2C
- outputs

prototype powering features retained

CERN bandgap, LDO for analog powering,

improved DC-DC switched capacitor circuit (CERN)

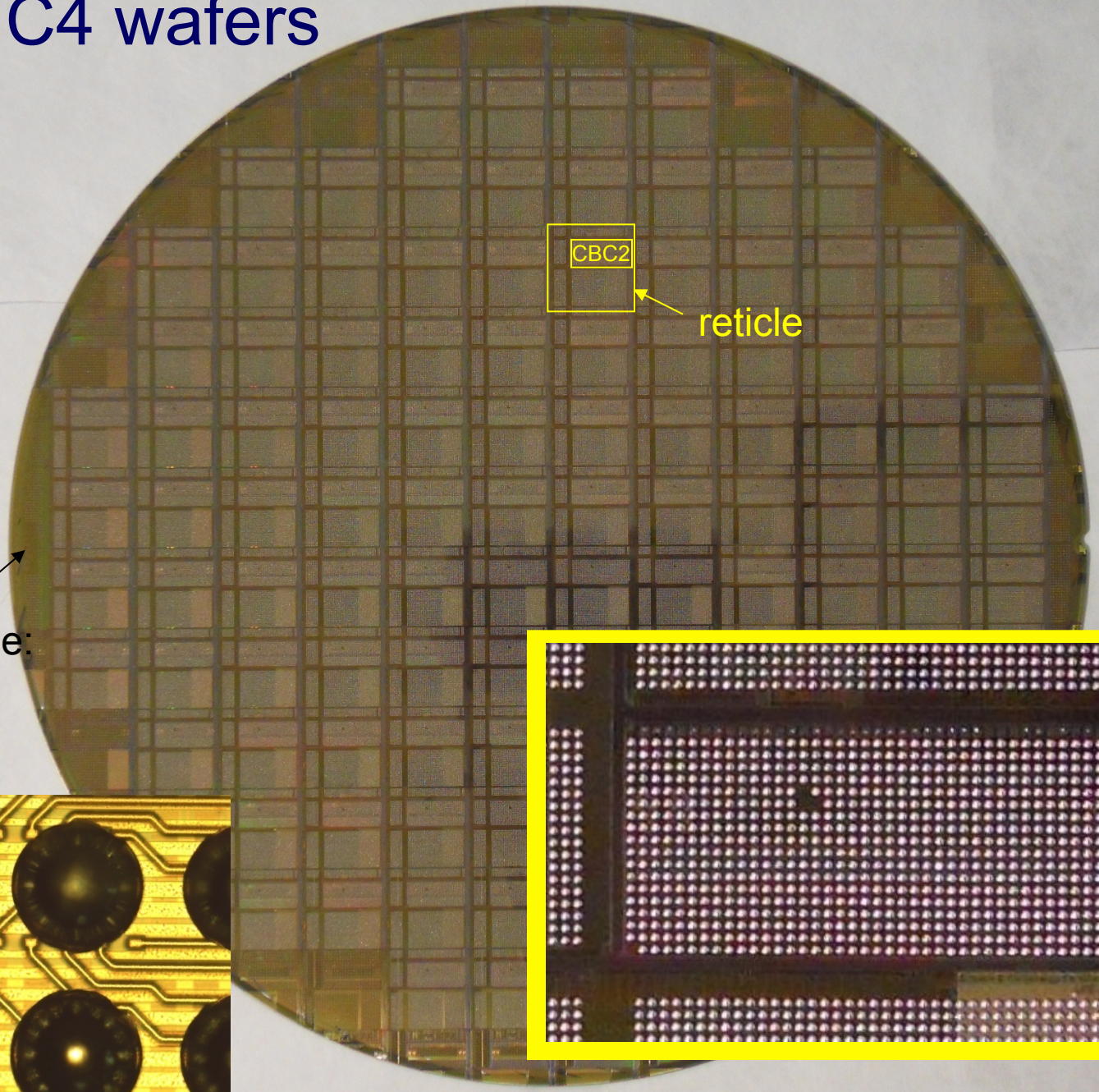
slower switching edges & rad-hard layout

Davide Braga, Mark Prydderch, Peter Murray (RAL)

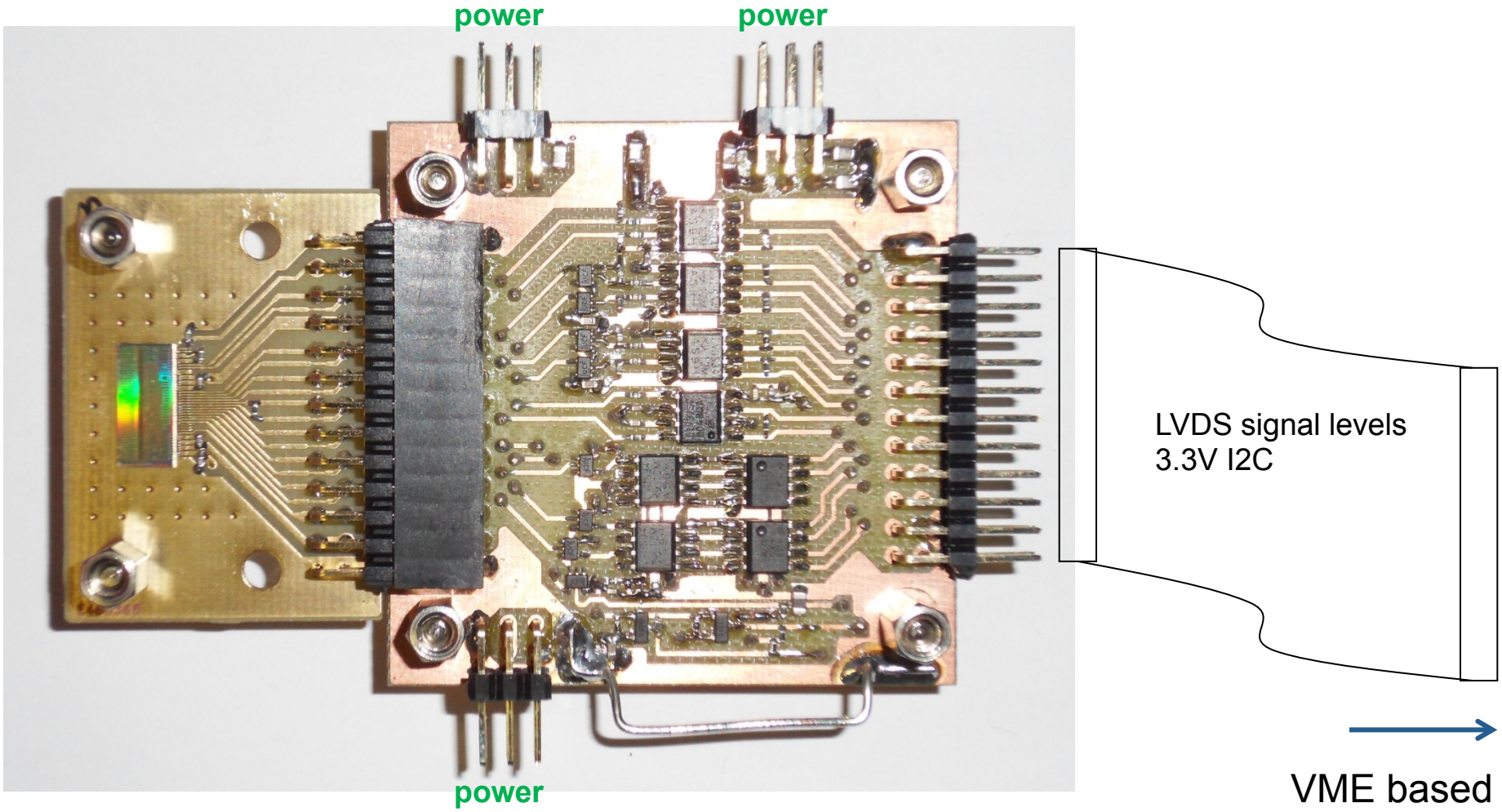
chip submitted for fabrication July 2012

wafers back January 2013

CBC2 C4 wafers



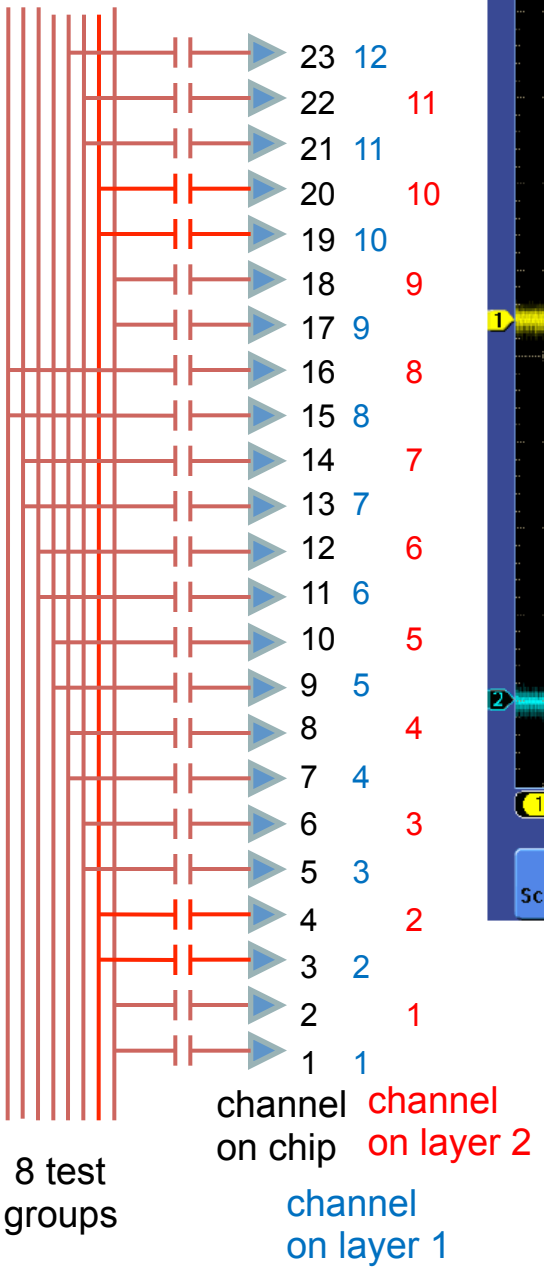
wirebond CBC2 test setup

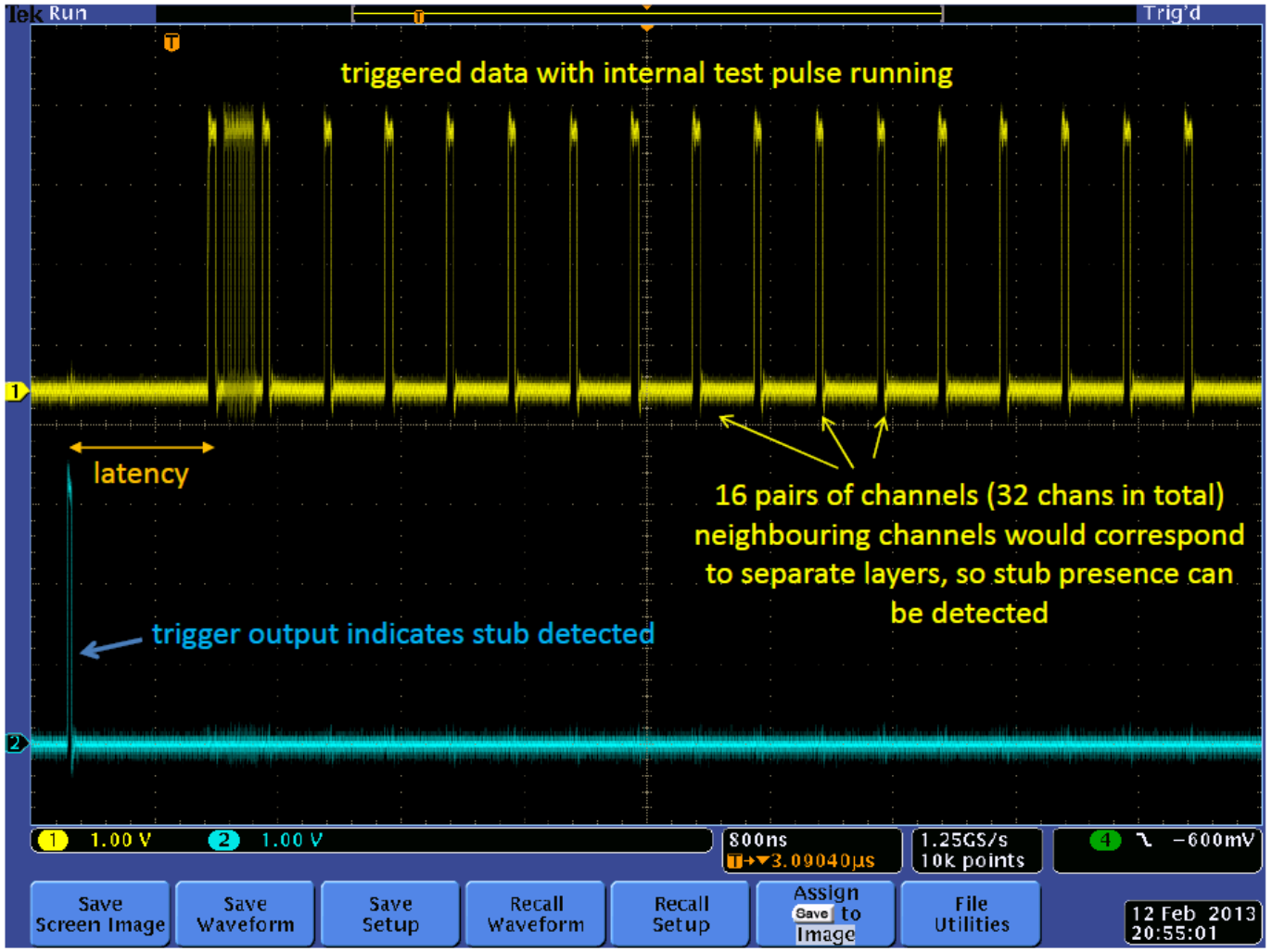


use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

convenient setup for developing detailed wafer probe procedures

first result



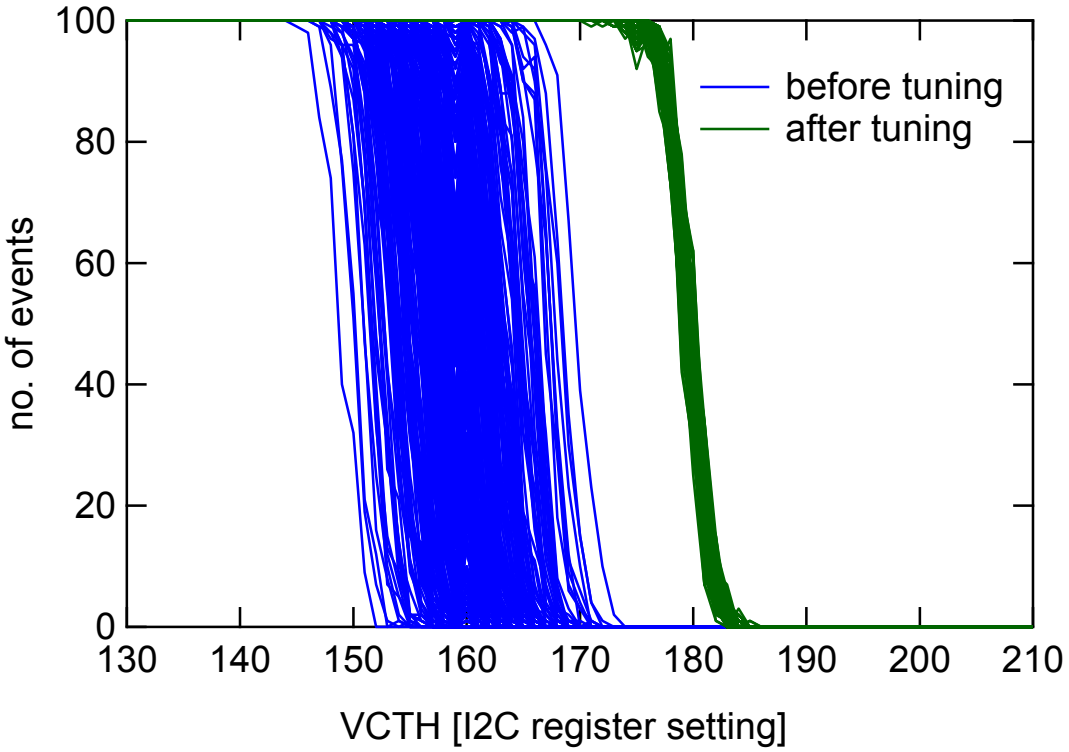


arrangement of 8 groups of test pulse connections allows to simulate signals from different layers and therefore exercise correlation logic

can also verify correlation window width using channel mask register and window offset

=> chip is working

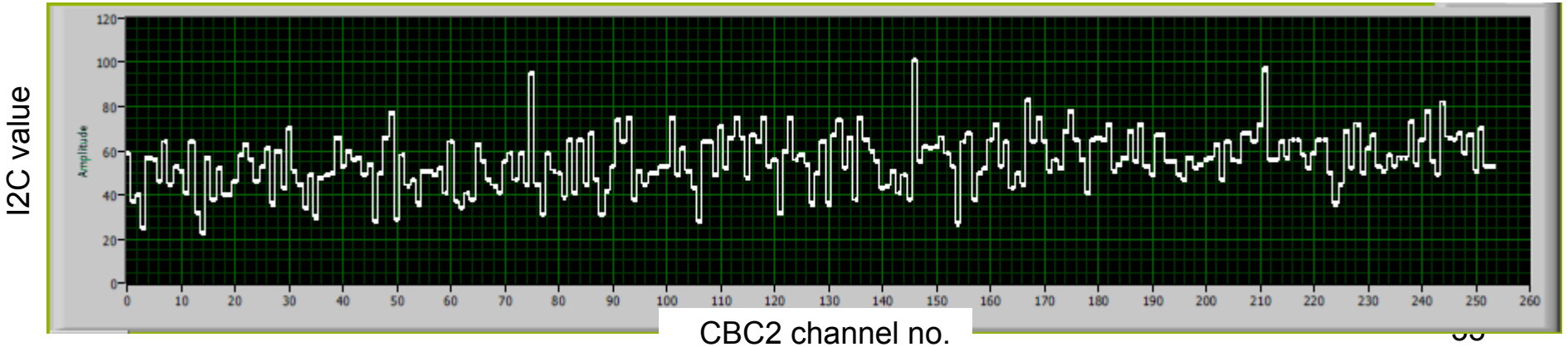
S-curves and tuning



254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to VCTH setting of 180

254 offset values after tuning



CBC2 qualitative observations

emphasis so far on verifying functionality - no detailed study

=> have spent most time preparing basic wafer probe test

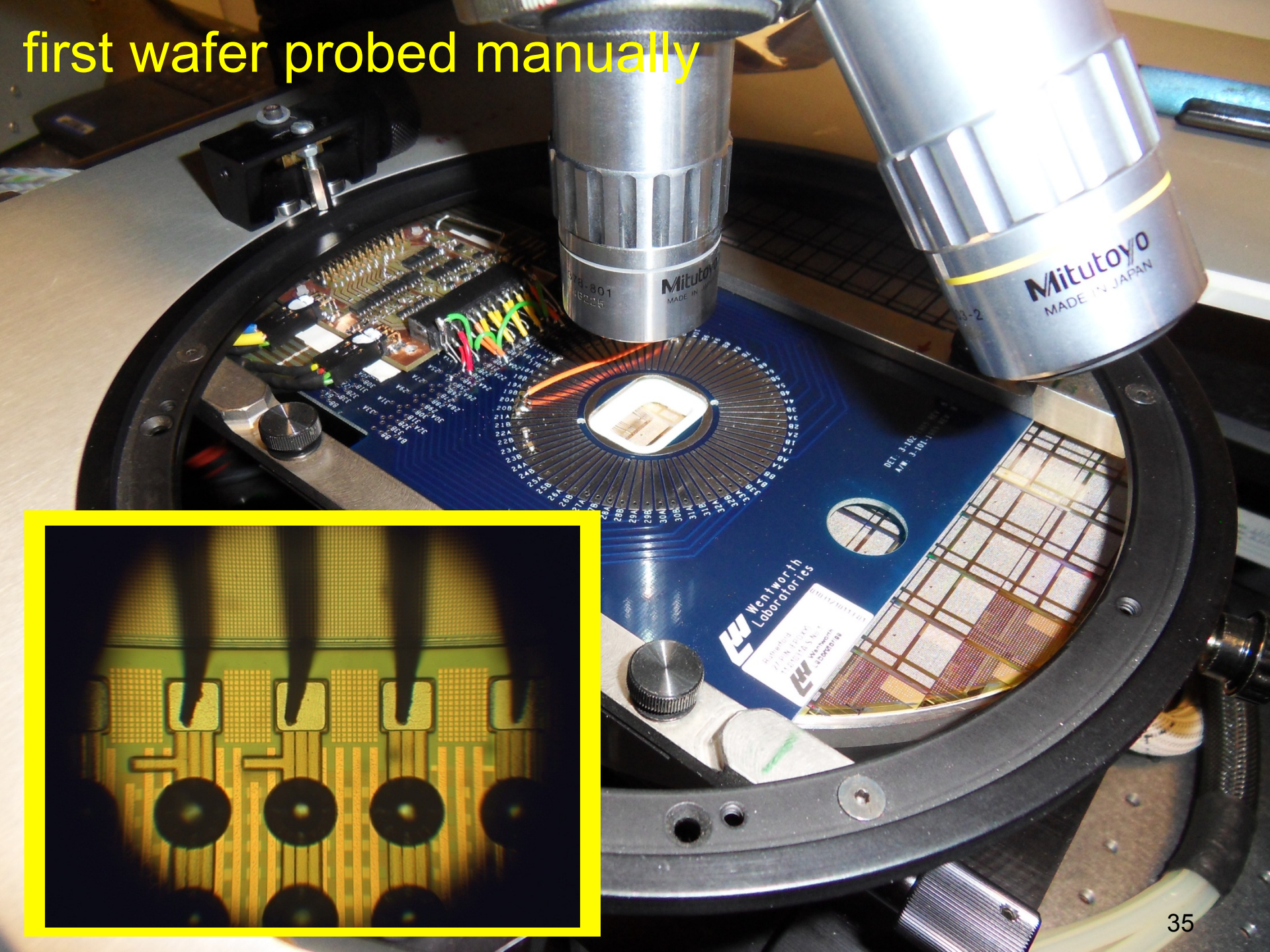
what can be said so far?

no signs of instability => fixes have worked
power consumption seems “about right”
LDO functioning as expected
2.5 -> 1.2 DC-DC converter also functioning
correlation and window logic verified as far as possible

detailed studies may yet show undesirable features, but chip almost certainly working well enough to allow module development to progress

Typically modest and cautious assessment
but look elsewhere for comparable developments

first wafer probed manually



final yield for 1st wafer

112 reticles
108 good chips
4 bad chips

bad chips due solely to physical damage from probe card

bad chip

CBC2

reticle

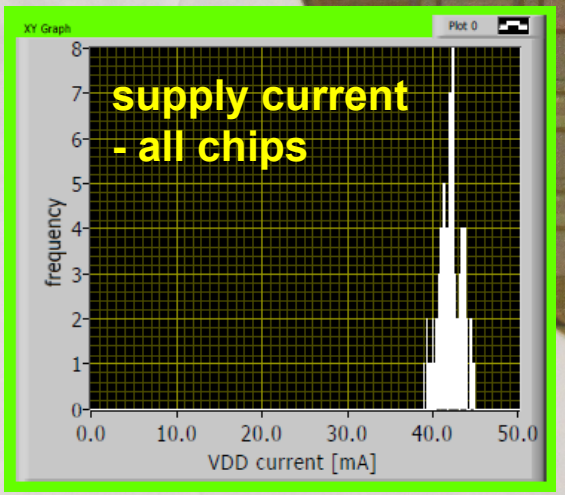
no defective channel found on any of 112 chips tested on this first wafer

=> 100% yield

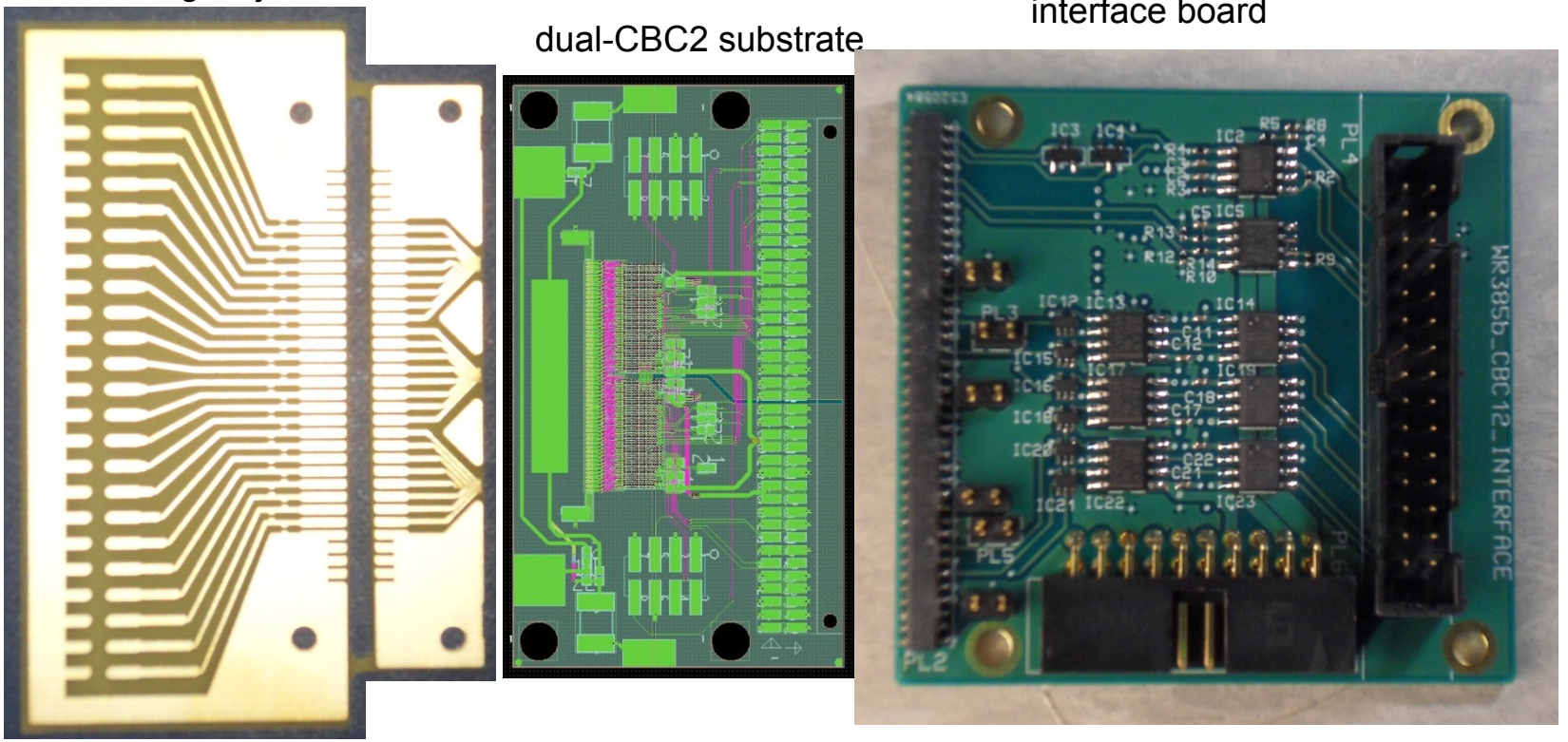
perhaps not too surprising if overall wafer yield high

CBC2 is relatively small area of reticle

& significant fraction of CBC2 area not occupied by active circuitry

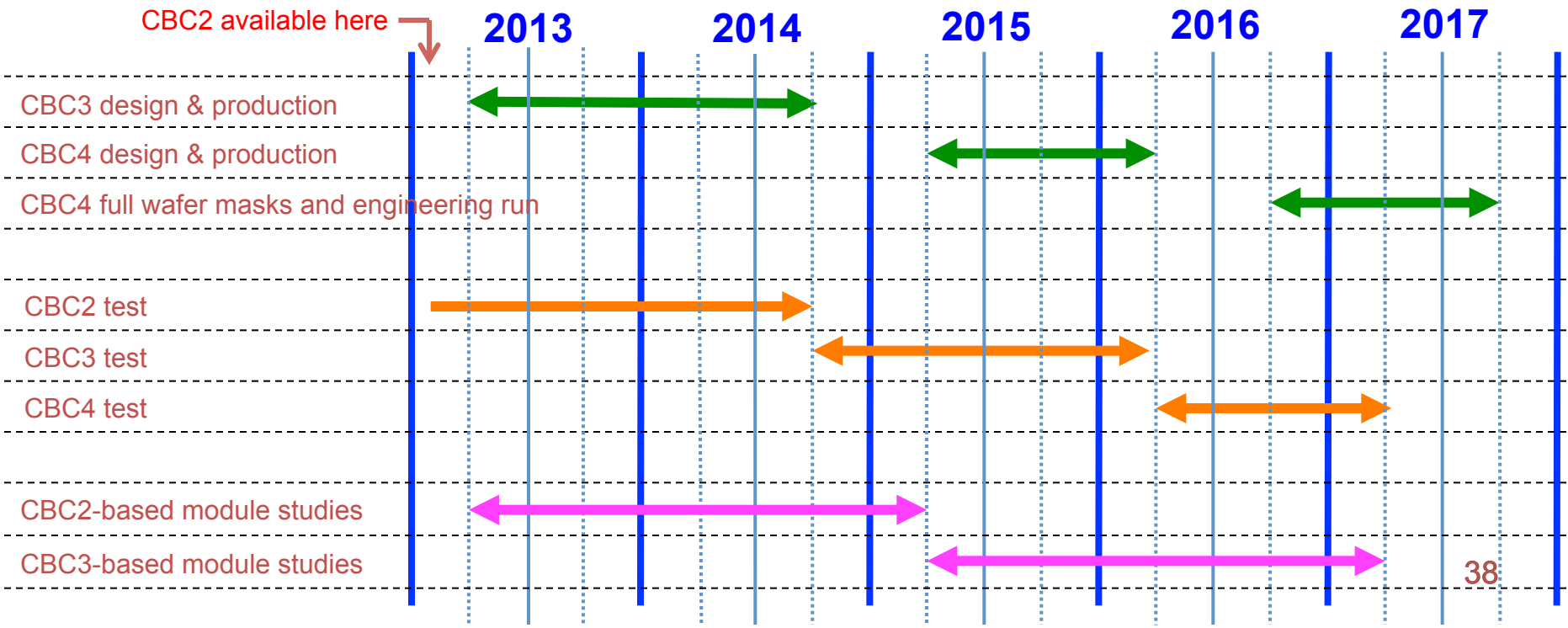


dual-CBC2 substrate test setup



2xCBC substrate + PA (both sides) becomes device under test
pluggable charge inject board allows different external capacitance

future plans



CBC2 (and modules based on CBC2) will dominate test activity over next ~ 2 years

next prototype, **CBC3**, should be very close to final chip – available towards end 2014

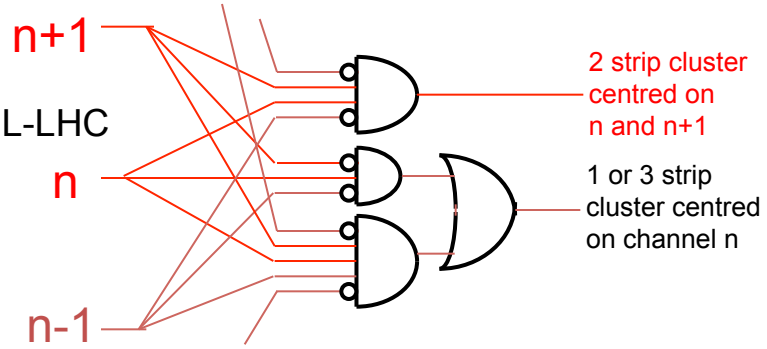
incorporate functionality to generate and transmit stub addresses

… new features

CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017

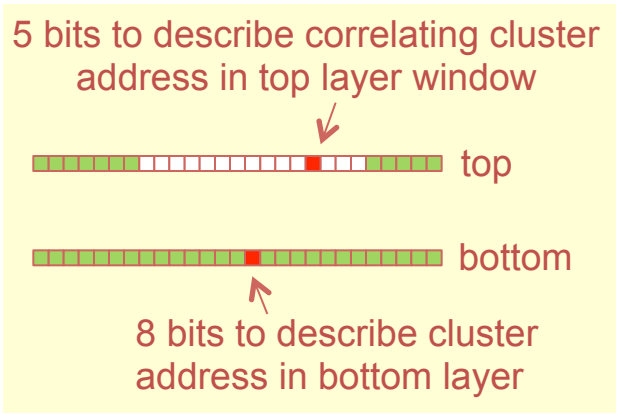
~ 5 years assumed for large scale production, module construction, integration, commissioning, …

CBC3 - the "final prototype"



next version of chip should incorporate all features required for HL-LHC

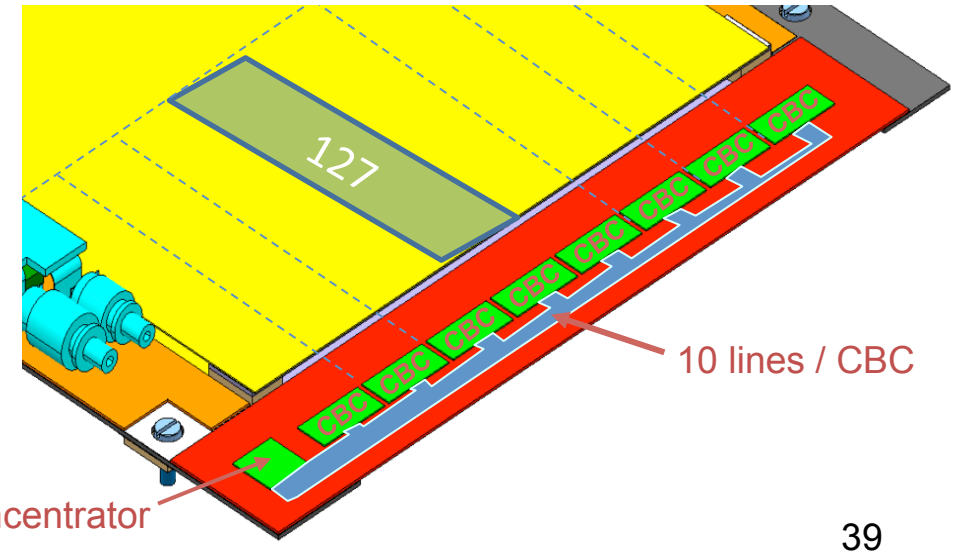
- **final choices for front end**
  - ½ strip cluster resolution
    - 2 strip cluster position assigned to mid-point
- **stub data definition**
  - 8 bits address (for ½ strip resolution) of cluster in bottom layer
  - 5 bit bend information
    - address of correlating cluster in top layer
- **stub data formatting & transmission to concentrator**
  - 13 bit / stub, up to 3 stubs/BX => 39 bits
  - +1 bit unsparsified L1 triggered readout data
  - => 40 bits / 25 nsec
    - e.g. 10 lines at 160 Mbps (per chip)
- **other useful features**
  - e.g. slow ADC to monitor bias levels
  - …



CBC data to concentrator

25 ns

S1	S1	S1	S1	S1	S1	S1	S1	B1	B1
B1	B1	B1	S2	S2	S2	S2	S2	S2	S2
S2	B2	B2	B2	B2	B2	S3	S3	S3	S3
S3	S3	S3	S3	B3	B3	B3	B3	B3	**R**



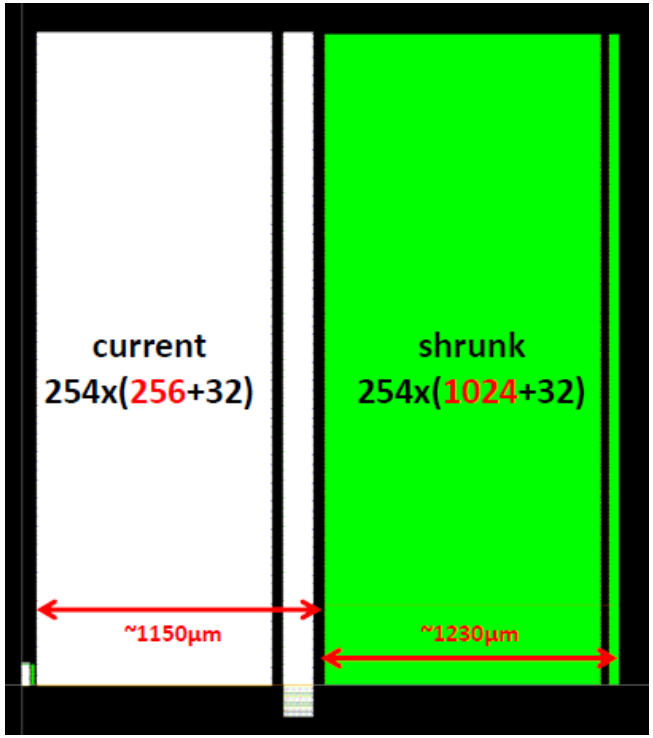
recent developments

- **up to now have assumed max. L1 latency of 6.4 usec and L1 accept rate 100 kHz**
  constraints originate in ECAL readout electronics

- ECAL now considering FE board replacement – removing these constraints

- can we increase latency on CBC?
  - factor 4 increase seems feasible ~25 usec
  - denser pipeline layout should mean chip doesn't need to grow (much)
  - longer latency beneficial for L1 data processing

- can we increase trigger rate capability (500 kHz?, 1 MHz?)
  - wider implications for architecture
  - at ~ 500 kHz unsparsified readout data dominates available off-module bandwidth
    - no room left for stub data
  - at 1 MHz sparsification becomes unavoidable
    - where to do it? front end chip? concentrator?



D.Braga (RAL)

CMS considering options to increase L1 rate and latency
to ~1 MHz & 20µs

Future physics programme severely affected by thresholds (cf WP1 slides)

WP3 objectives and status

- Develop µTCA system of crate, backplane & processors
  - feasibility studies for L1 trigger algorithms

- Final objectives
  - µTCA demonstrator (1 card & backplane)
  - algorithm performance studies

- Two major cards (mini-T5 and MP7) developed and proven
  - each using most advanced FPGA available
  - trigger demonstrator system constructed with impressive performance
  - new trigger architecture proposed and recognised
  - algorithms implemented in firmware
    - UK expertise more extensive than almost anywhere else

Prototype with final FPGA

G Iles, A Rose, J Jones, S Greenwood et al.

Two types of FPGA

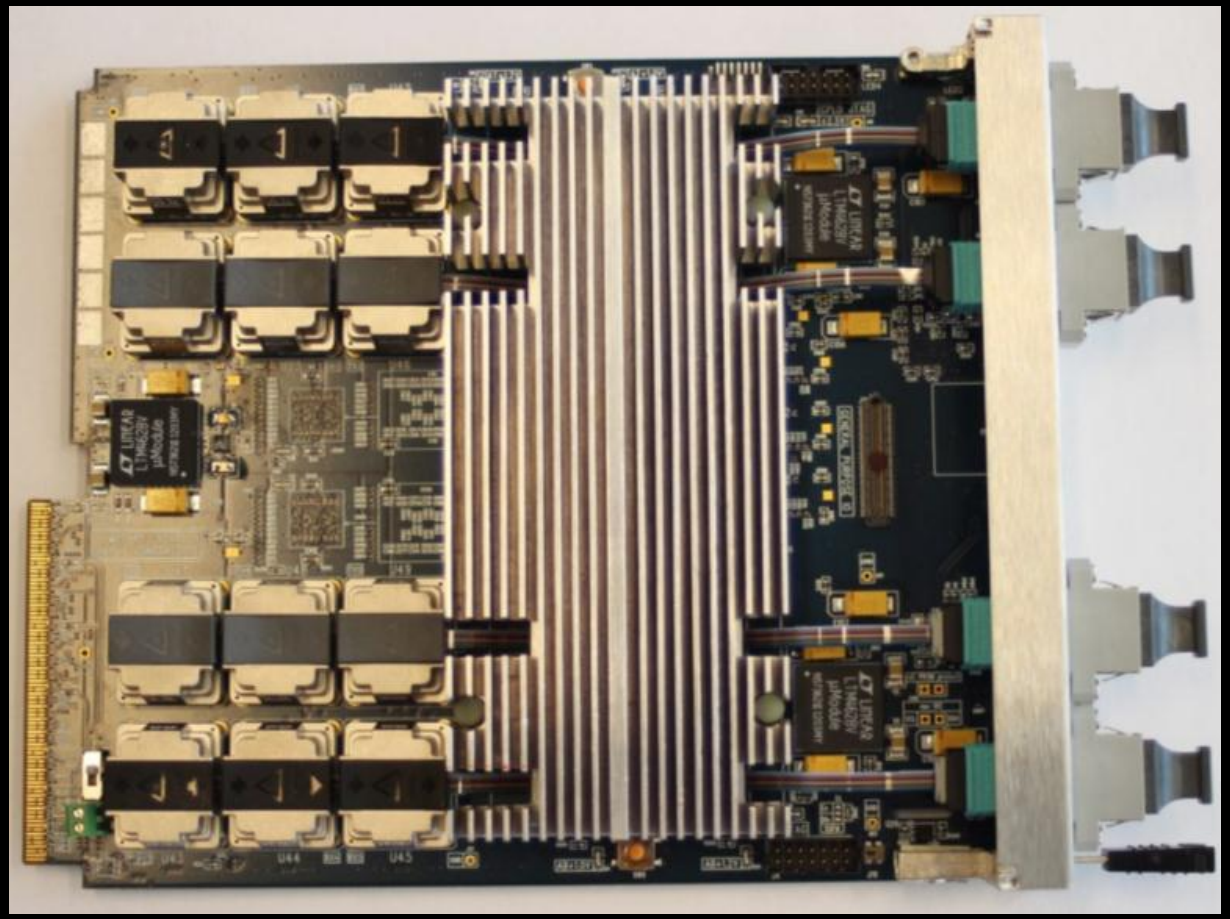
- "690" => 1.5Tb/s
- "485" => 1 Tb/s

First "690" delivered beginning of March

Calo Trigger = "690"

- 72 Tx @ 10Gb/s
- 72 Rx @ 10Gb/s

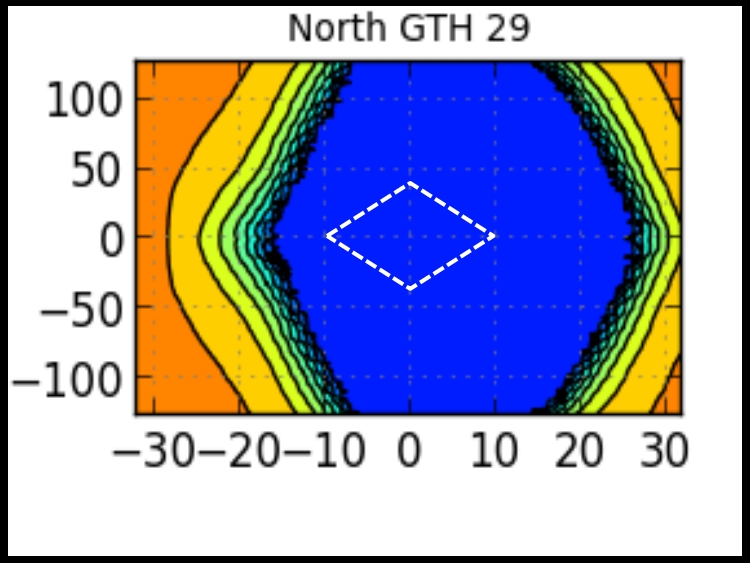
Lower cost FPGA suitable for other applications



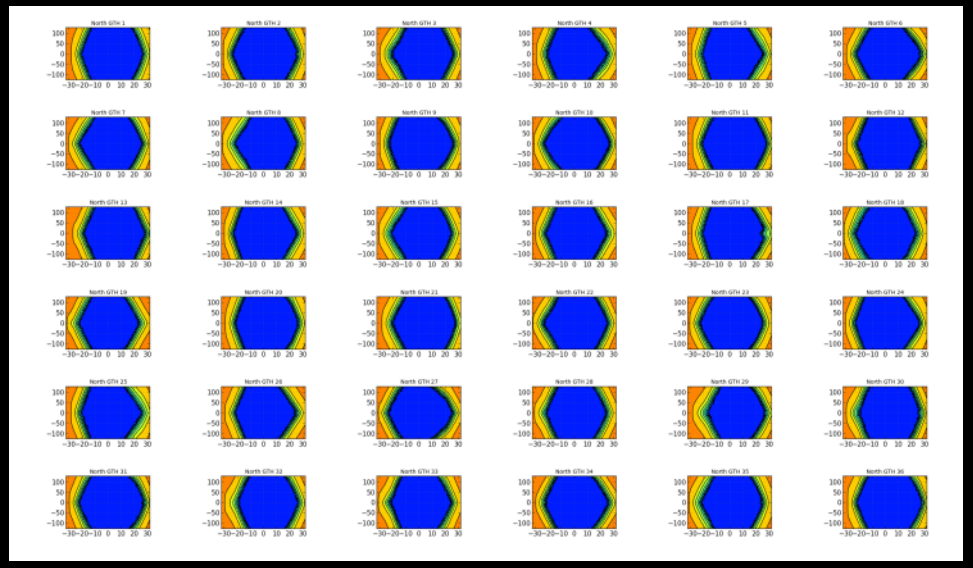
Testing of "690"

- Out-of-the-box performance of both the MP7-485 and MP7-690 is outstanding
- Tests currently use default settings everywhere no pre-/de-emphasis, minimal differential-swing) and we have plenty of options for fancier manufacturing techniques, but it does not look like these are required.

Eye diagram from GTH 29 showing excellent eye opening



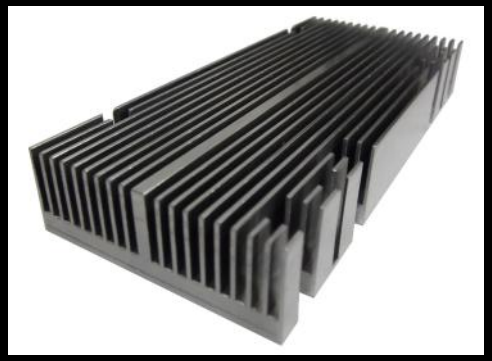
The eye diagrams from the "north" 36 links operating simultaneously

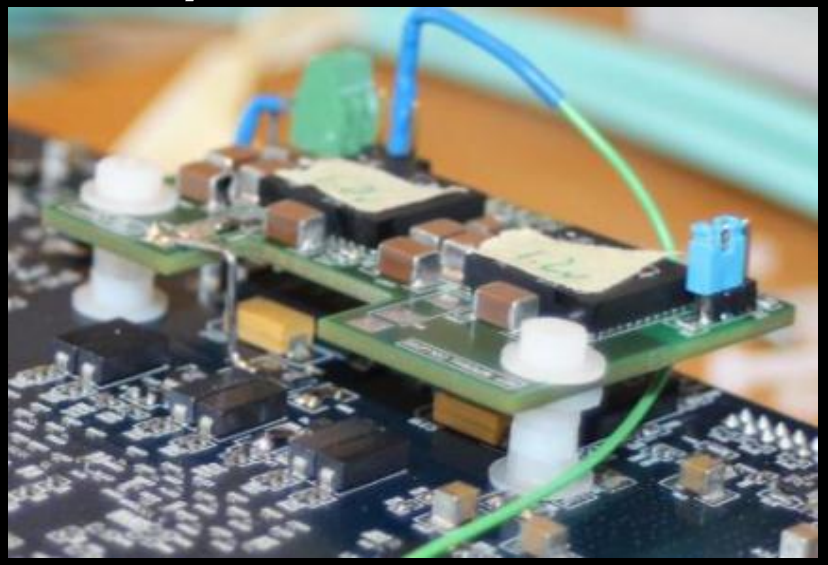


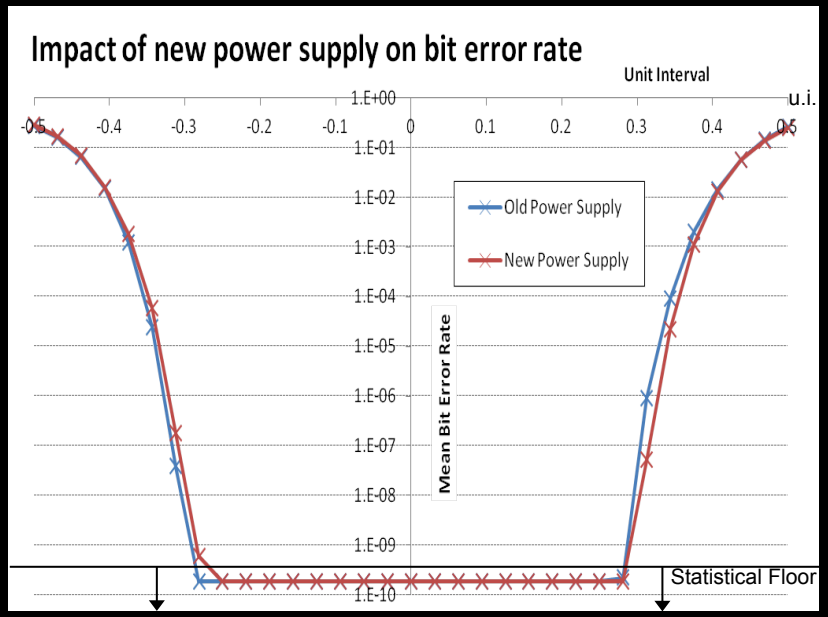
Improvements to power system

Increased power consumption by FPGA, significantly beyond original specification, now solved:

- Firmware bug fix from Xilinx reduced power consumption to some extent
- Larger power supply for serial links tested for compatibility with serial links
- Improved heat dissipation with custom heat-sink



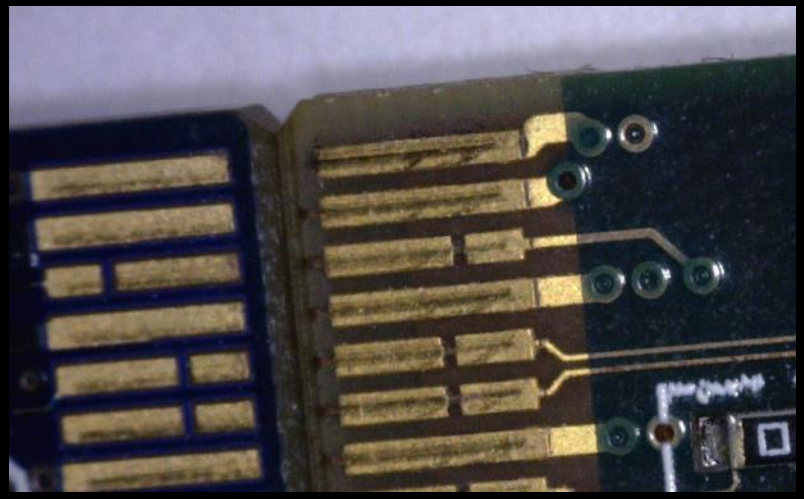




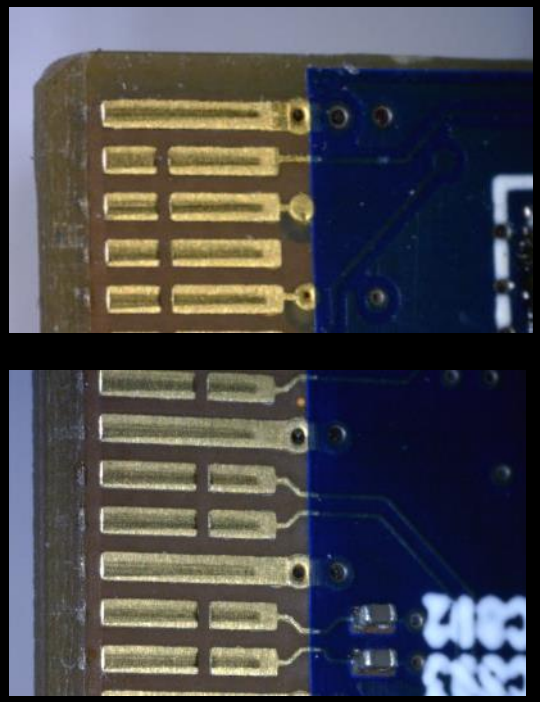
AMC edge connector

PCB edge connector quality originally insufficient

Collaborated with UK PCB company to improve PCB quality

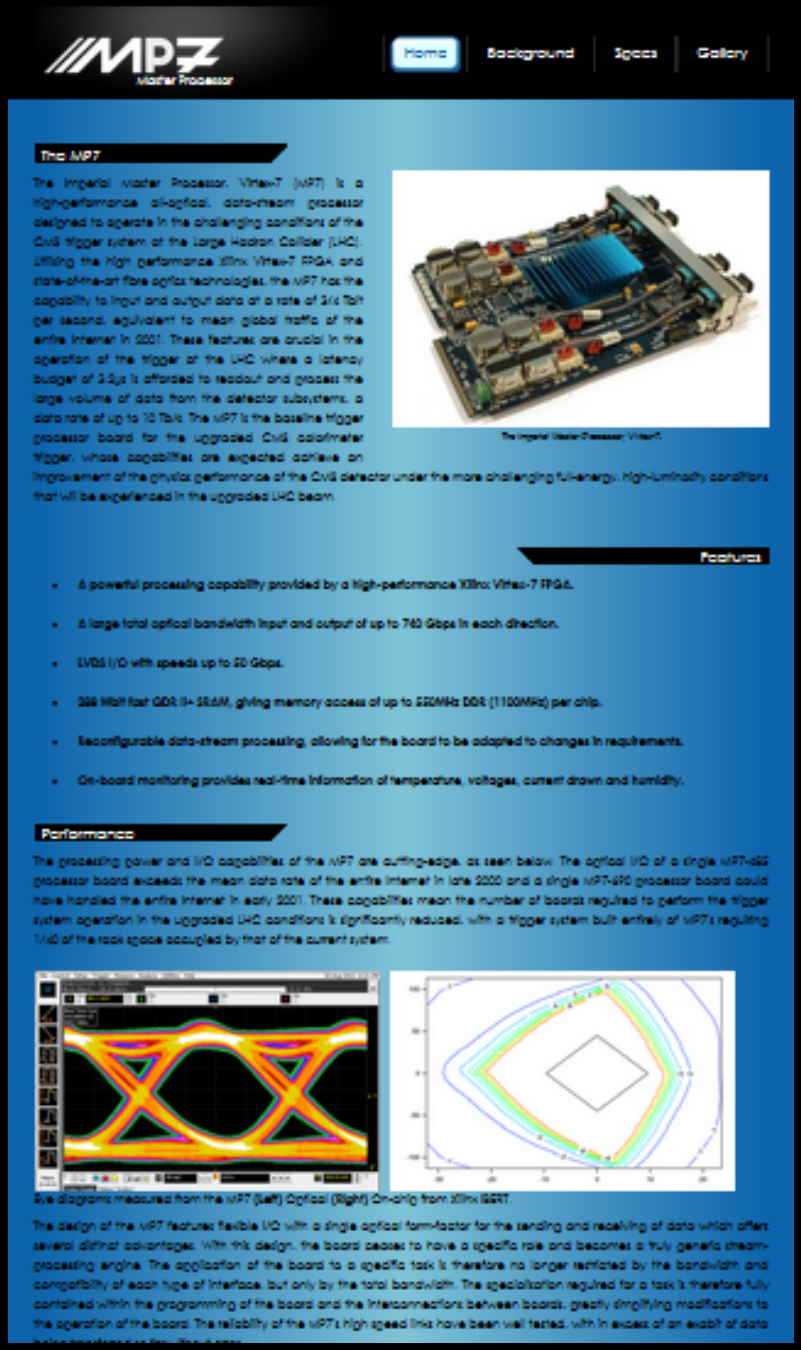


Poor alignment



Conclusions

- Have tested solutions for all problems encountered with the MP7-R0
- MP7-R1 design complete except for MGT power supply, for which a separate schematic already exists and need only be imported when we are completely happy with performance
- Ready for MP7-R1 Submission
- Website for other interested users



www.hep.ph.ic.ac.uk/mp7

Schedule

MP7-R1 Submission

- 690 FPGAs purchased, expected end of April
- R1 board submission was planned for end of March, will now be mid-April

Focus now on firmware & software development

- Base firmware under development
- Focus shifted back to algorithm development

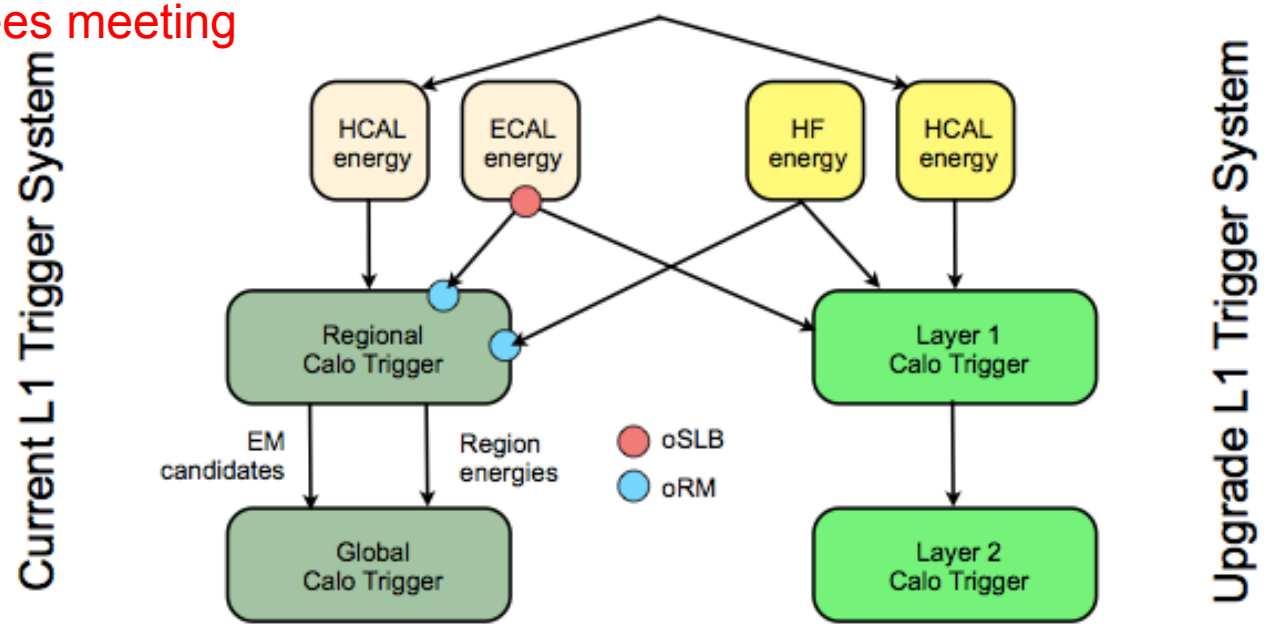
Finish base system & documentation

Important dates

- July 2013: Integration test
- Sept 2013: TMT Test

Overview: calorimeter trigger

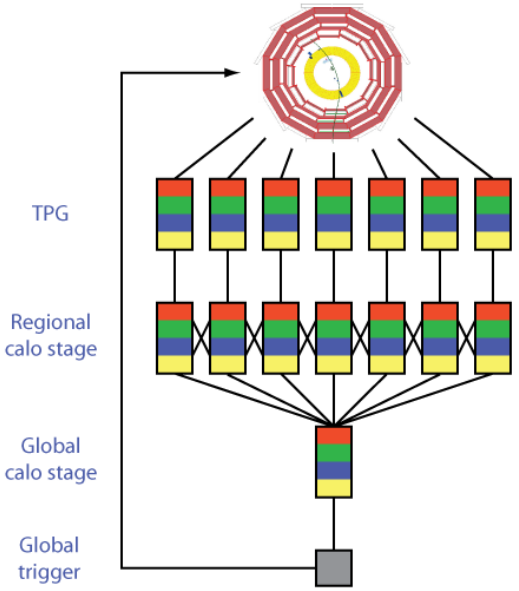
A Tapper
LHCC referees meeting



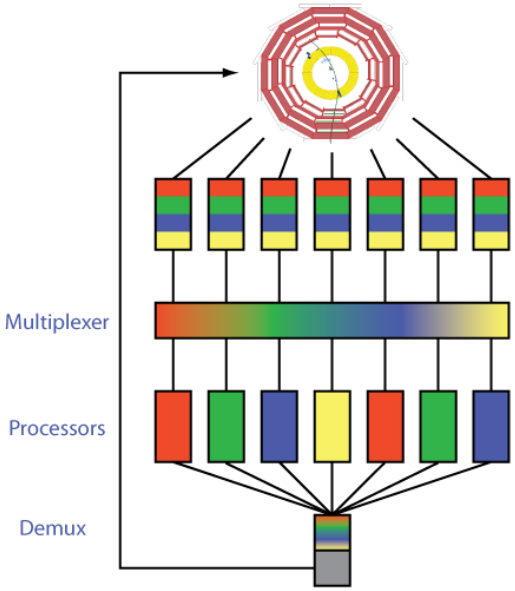
- Complete commissioning of calorimeter trigger in parallel
  - Necessary to install oSLB/oRM during LS1 (complex operation)
  - Necessary to install passive optical splitters for HCAL (LS1 and YETS)
  - Underway already

Overview: calorimeter trigger

- Two architectures investigated



Fully pipelined trigger



Time-Multiplexed Trigger

US to build

UK to build

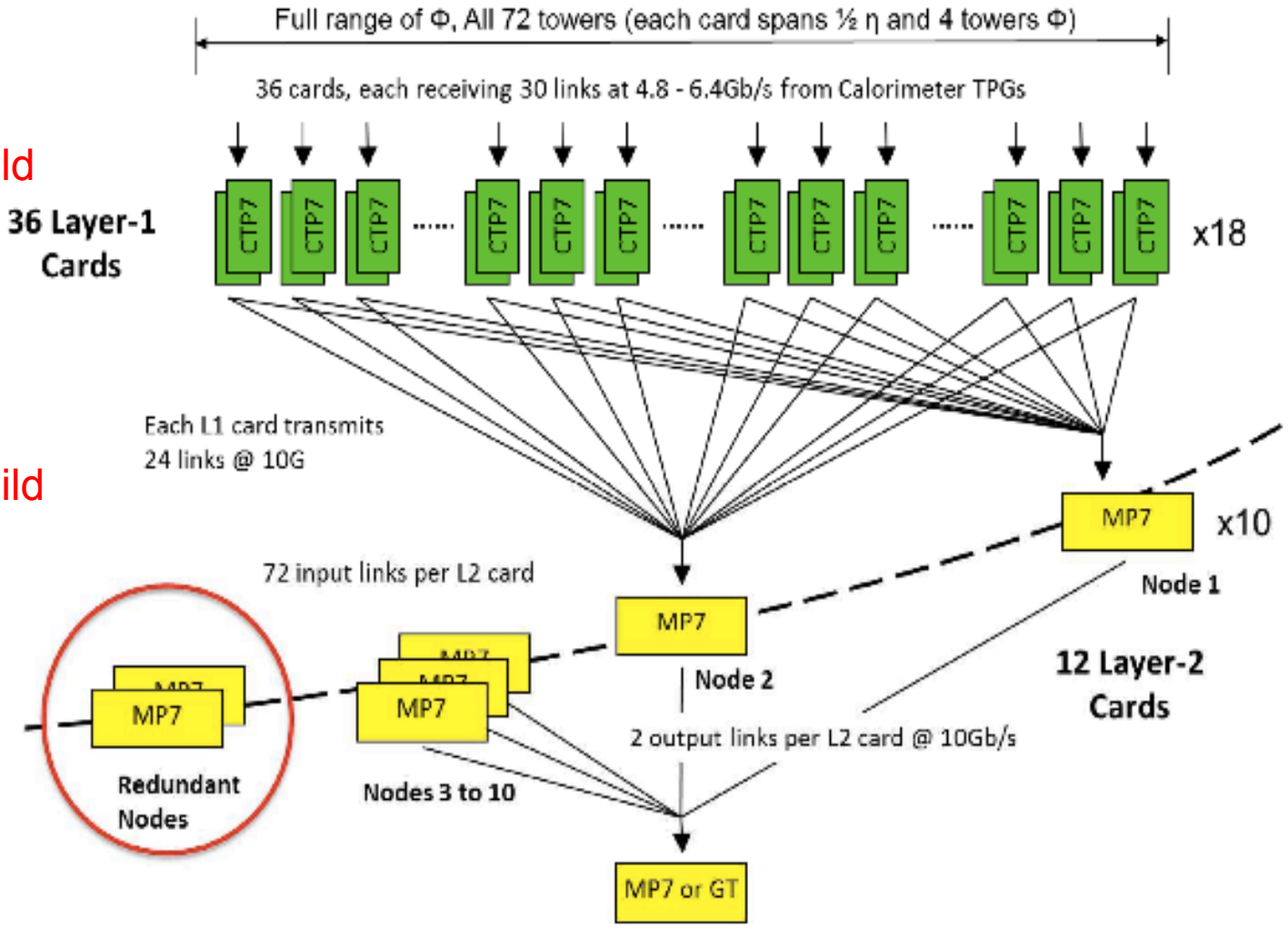
Austria, using MP7s

- Keep new trigger flexible in order to adapt to the needs of the evolving CMS physics program ➔ hardware can implement either configuration
- TMT architecture has the potential for additional flexibility in algorithms ➔ chosen as baseline design

Overview: calorimeter trigger

US to build

UK to build

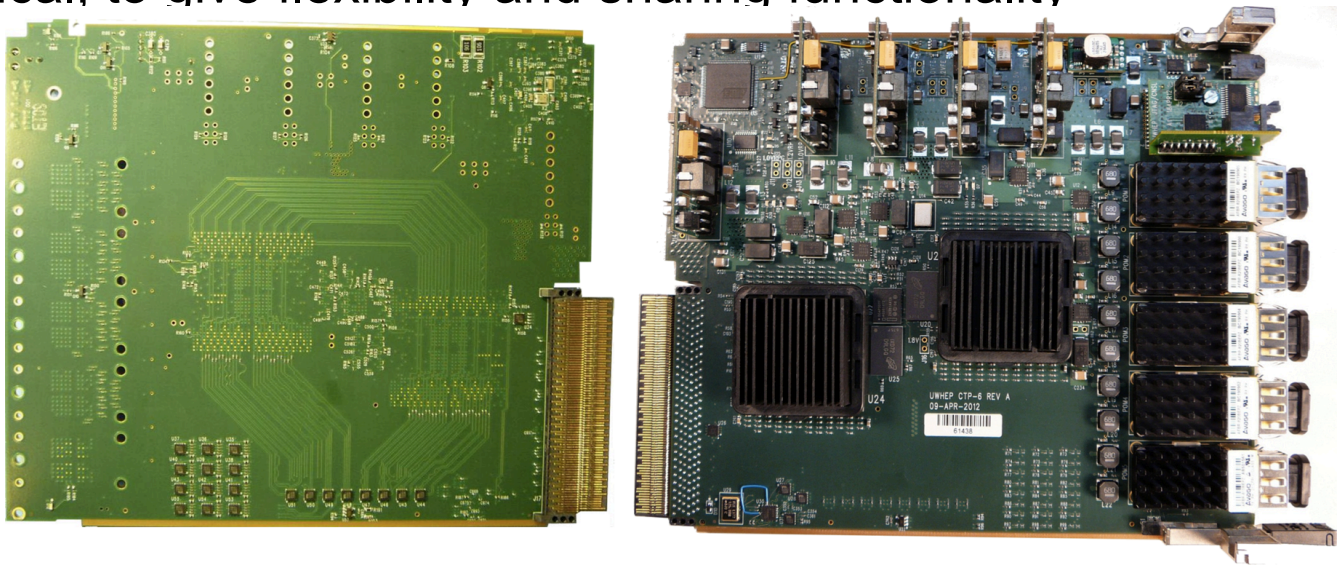


Hardware R&D status: CTP7

- First layer of the calorimeter trigger

U Wisconsin

  - Receive data from calorimeters and act as part of the switching matrix
  - Link configuration balanced between front panel optical and backplane electrical, to give flexibility and sharing functionality

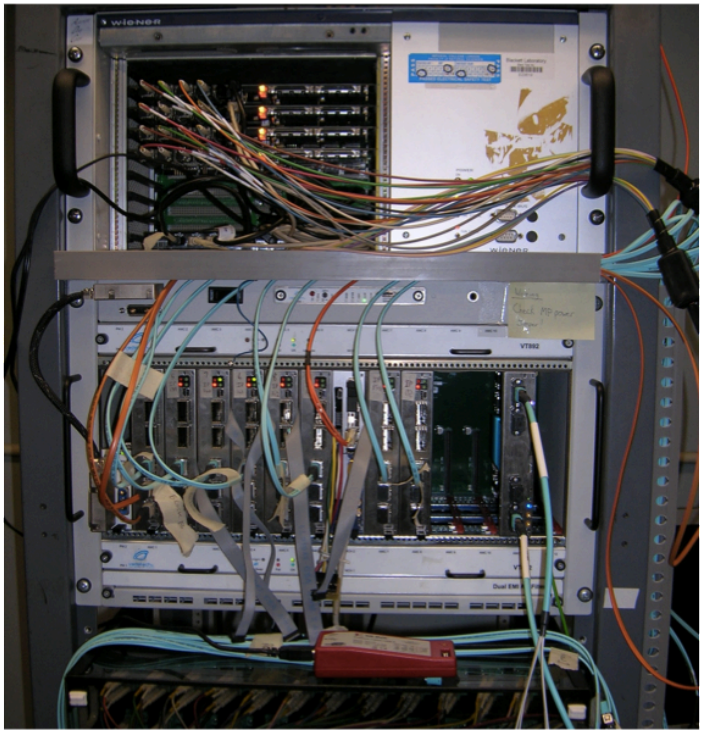


  - Current prototype, based on dual Virtex 6 FPGAs with 6.4 Gb/s links
  - Virtex 7 (single) FPGA design in progress

Hardware R&D

- Proof of TMT concept
  - 8 layer 1 cards
  - 1 layer 2 card
  - 1 AMC13 card

  } Up to ~2/3 of CMS for 1/10 of the time
- Implemented current GCT algorithms
  - Well understood benchmark
  - Run Monte Carlo events through system
- Measured latency
  - Agrees extremely well with calculation
  - Incidentally, quite a lot faster than current GCT
- Measure FPGA resource usage
  - <10% for core + algorithms
- Test synchronisation
- Tested software and firmware infrastructure



Test stand running since 2009

WP4: pixel DAQ

- WP history already known to OSC
  - partly related to origins of project in difficult financial situation
    - especially affecting RAL PPD
- PPRP 2012 WP proposal, evolved during 2011, to deliver
  - ROC test board and contribute to beam tests
    - beyond scope of original R&D proposal
    - have absorbed costs into existing WPs and travel budget
  - new µTCA pixel FED
    - compatible with µTCA future as Phase II prototype
- October 2012 beam tests successful, and FC7 at advanced design stage
  - significant beam test effort from RAL and Bristol
  - FC7: Imperial design (& collaborating with CERN to maximise utility)

Science & Technology Facilities Council

test beam team

K Harder, R Frazier, et al

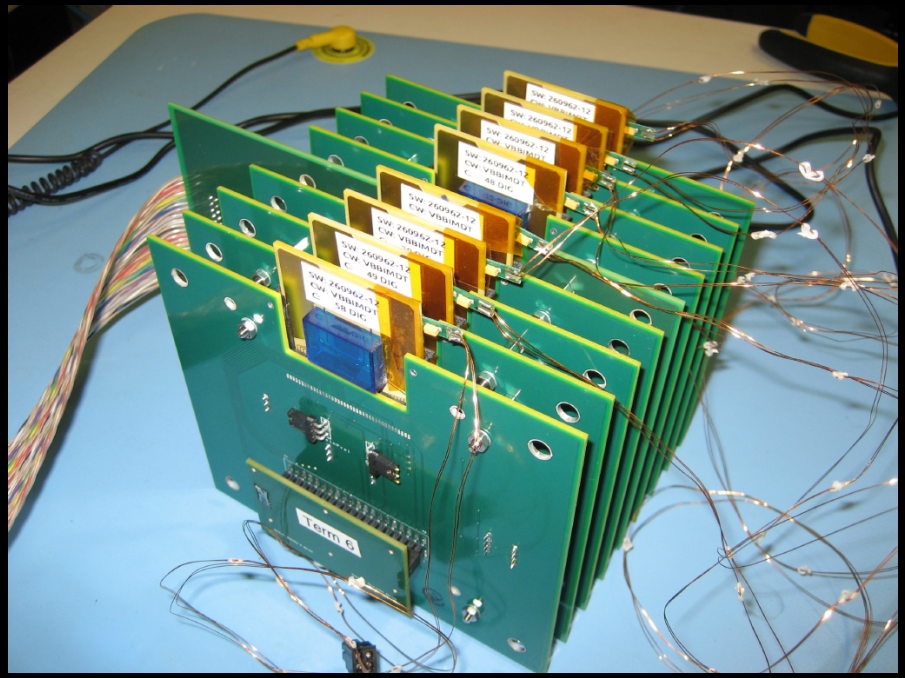
Responsibilities and effort shared among several institutes:

- **location scouting, beam time requests:** CERN
- **mechanical setup:** CERN
- **trigger hardware:** CERN
- **DAQ electronics and firmware:** RAL, Bristol
- **low level software:** RAL, Bristol
- **DQM software:** Taiwan
- **reconstruction and analysis software:** CERN, Karlsruhe, Taiwan
- **calibration software:** CERN, Karlsruhe

Science & Technology Facilities Council

beam telescope

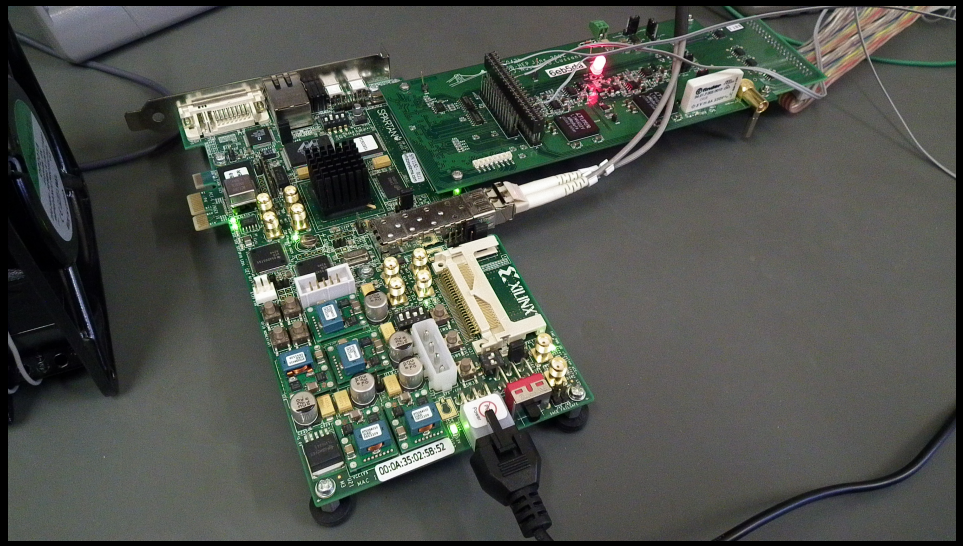
Test requires several ROCs+sensors with daisy-chained readout lined up in beam line.
Here is the low-cost modular beam telescope we used:



- **concept, schematics and layout by RAL**
- **PCB production partially sponsored by University of Kansas**

Science & Technology Facilities Council

DAQ testboard



based on Xilinx evaluation board with custom add-on ("Bridge Board"), control and readout through optical ethernet, using IPbus protocol.

- schematics, layout, production by Bristol
- DC/DC converter schematics (for ROC power) contributed by PSI
- firmware by Bristol, RAL

using similar FPGA technology as new pixel FED proposed by UK institutes

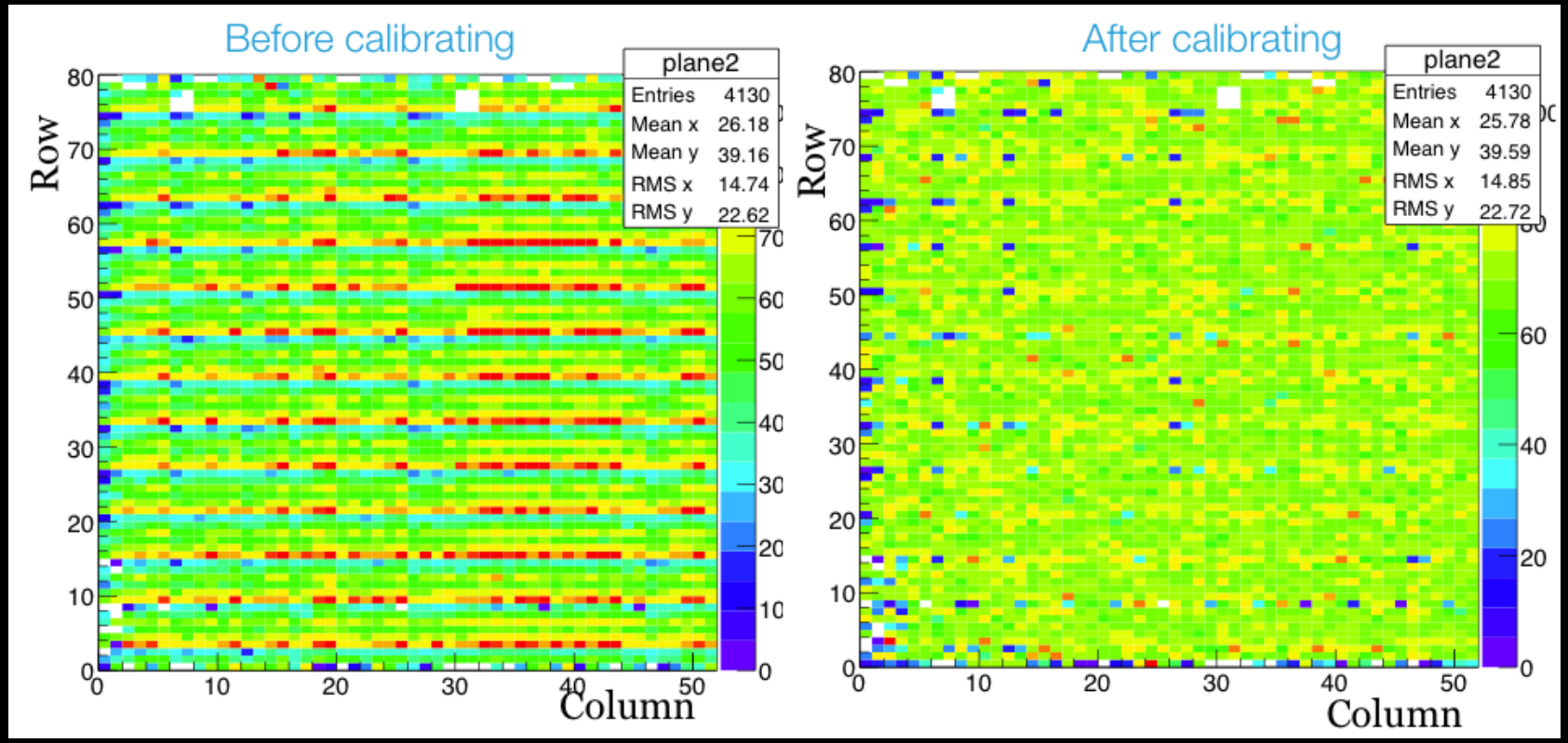
- intended to serve as FED firmware development test bed

Science & Technology Facilities Council

calibration

Writing brand new calibration code for the new UK hardware/firmware was a lot of work. Costing a lot of CERN staff nerves!

However, importance of calibration for even basic results is easy to see:



Average pulse height has patterns caused by cross-talk between pixel signal and address lines ➡ to be fixed in next revision of PSI46dig

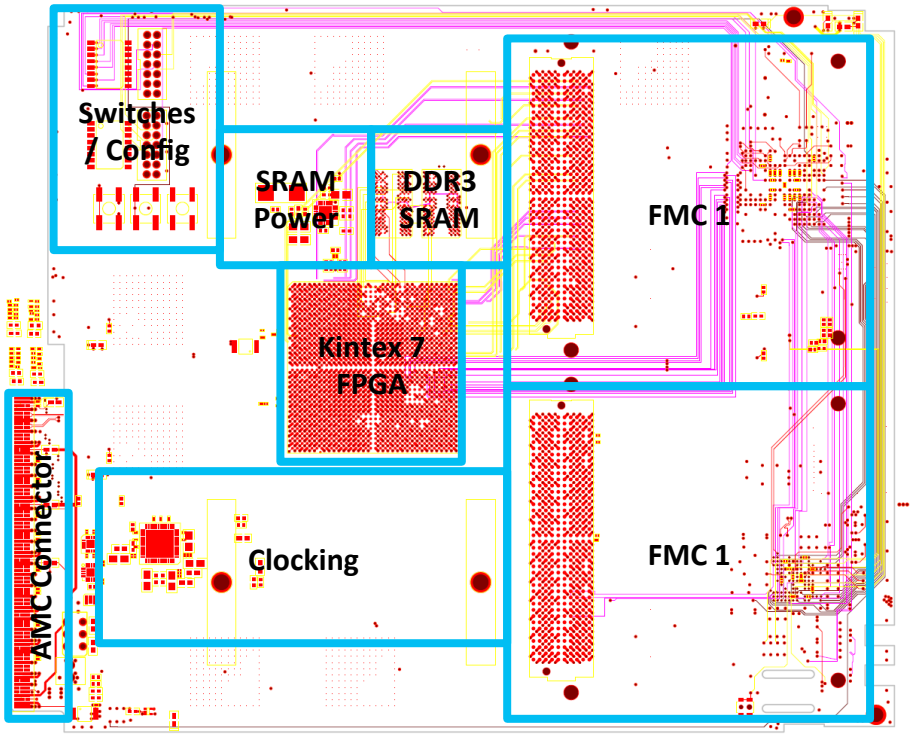
FC7 status

M Pesaresi

- flexible, µTCA compatible card for generic CMS data acquisition/control uses
- joint CERN/UK project; schematics provided by CERN, layout by Imperial
- based on existing board designs (CERN GLIB & Imperial MP7) to minimise risk
- many applications; e.g. CBC DAQ, TTCci replacement, pixel FED, GLIB successor
- current status/plans:
  - final routing in progress
  - under review before submission
  - submission mid-April at earliest (awaiting FPGAs)
  - initial testing/prototyping begins mid-May

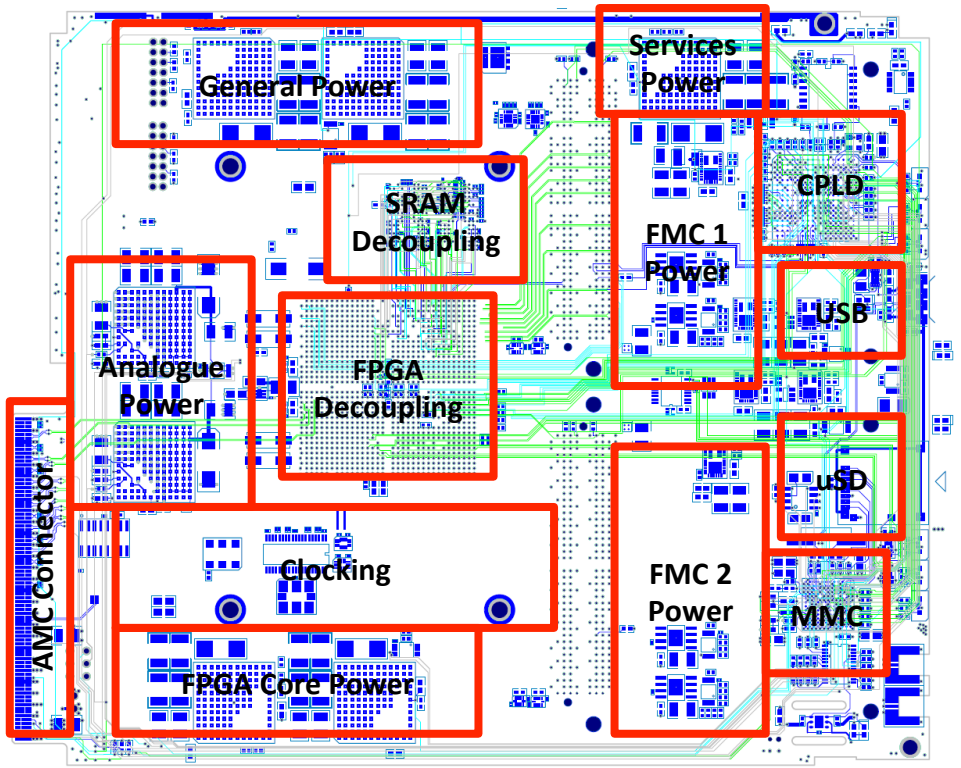
FC7 design

- double width, full height AMC card compatible with µTCA operation
- extremely flexible dual FMC carrier
- Kintex 7 FFG1156 FPGA
- 4Gb DDR3 RAM
- 34.1Gb/s total R/W bandwidth



FC7 design

- support for up to 20 serial links at 10Gbps to FMCs (MP7 compatible)
- supports a wide range of MGT protocols to backplane and FMCs
- fully compatible with CERN-GBT, pixels and CBC readout
- fully compatible with MP7 MMC, peripherals and peripheral interfaces



Finances

- Because of delays in CBC2 delivery and availability of MP7 final FPGA parts, some hold back of spending towards end of project
  - proved to be beneficial to smooth transition to new project
  - new grant to start 1 April – announcement imminent

- On target to complete project within allocations
  - Some required to fund 1 month of Imperial staff effort (Feb grant end date)
  - Significant recent spending in CERN which takes time to reappear in UK
  - TD effort should be close to target by end of FY
  - Total travel spend close to allocation
  - ~£35k materials budget yet to be spent

Conclusions

- The project is approaching the end
- The original goals changed a little, but not dramatically
  - mostly by increasing ambition
- The project started a bit later than anticipated
  - STFC financial problems in 2008
  - However, this probably worked to our advantage in aligning to Phase I & II
  - Did not prevent some work starting towards objectives
- The achievements are greater than originally proposed
- There is a solid basis for UK contributions to the CMS upgrade programme

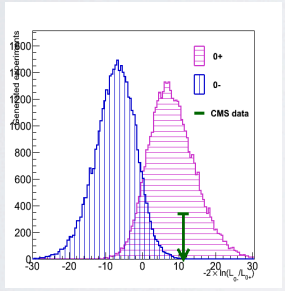
Further information

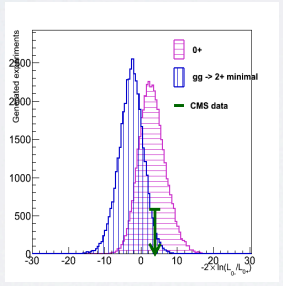
Results of the spin-parity tests

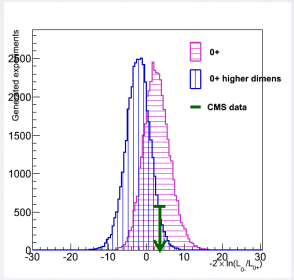
Signal hypothesis	Expect separation	Observed separation	CLs
0-	2.8 sigma	3.3 sigma	0.0014
gg-> 2+ minimal	1.7 sigma	1.9 sigma	0.0665
0h+	1.5 sigma	1.8 sigma	0.0928
Spin1+	2.0 sigma	3.2 sigma	0.0044
Spin1-	2.6 sigma	3.7 sigma	0.0007
qq-> 2+ mininal	1.6 sigma	2.0 sigma	0.0592

The observation is at tail of the distribution for some of the spin-parity test. More toys is running on to test the observed separation (for observation separation bigger than 3 sigma)

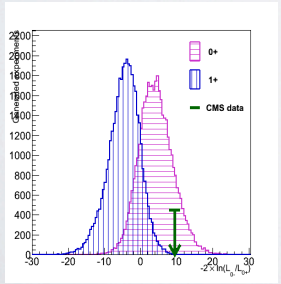
CMS Internal

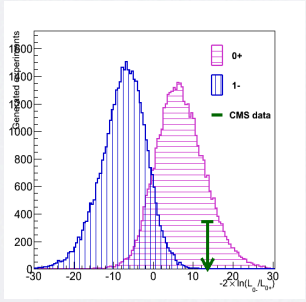


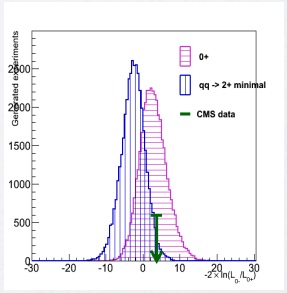




Upper row: 0-, gg->2+,0h+







Lower row: 1+, 1-, qq->2+

Project history

- Proposal submitted — Oct 2007
  - PPRP Dec 2007, Vis. Panel Jan 2008, response & revisions Mar 2008
- PPAN approval — Apr 2008
  - Award to await Programmatic Review conclusion
- Budget announcement — Jul 2008
  - requested 30% reductions to WP1 & WP3 to match available funding
- Grant announcements — Jan 2009
  - new appointments — Bristol RA Q1 09 & Q4 09

    Imperial (2 x RA) Nov 2009

    RAL: Permission to appoint currently being sought.

  Permission to hire at RAL refused at start of project. Hiring freeze imposed.
- STFC allocations for 2009/2010 — Aug 2009
- STFC reprioritisation — Dec 2009
  - told to expect 15% reduction from Apr 2010
- STFC revisions to grants — Feb 2010
  - no change in grant values, new profile requested, RG cuts

CBC1 test beam in 2012: Oct. 8th - 22nd

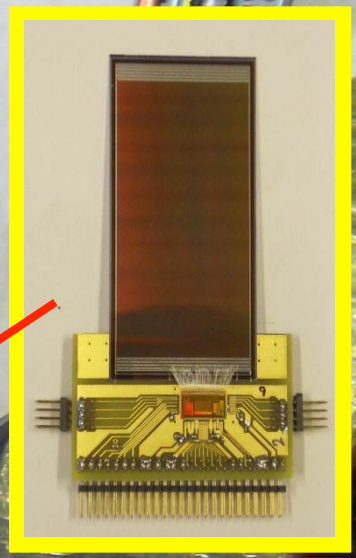
CBC prototype + Infineon sensor (Vienna)
300 um thick, p-on-n
5cm long strips, 80 um pitch
close to dimensions proposed for 2S-Pt modules

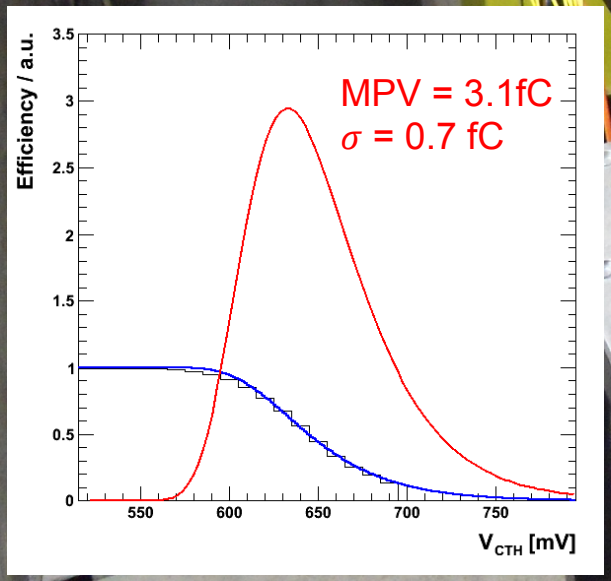
beam tracking plane using APV

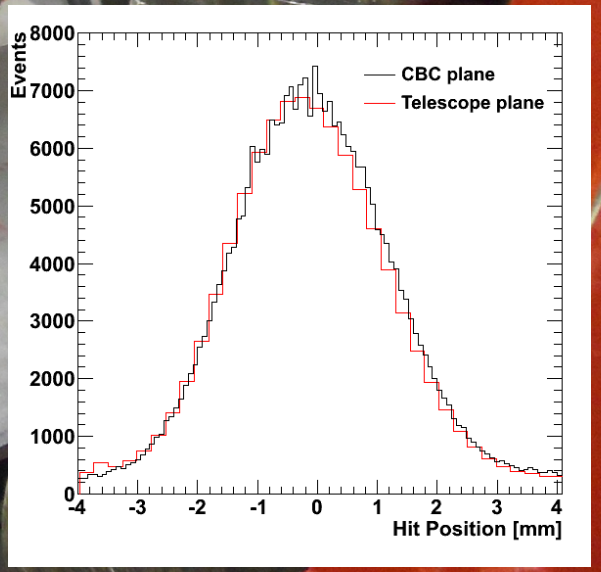
scintillator

CBC + Infineon sensor box

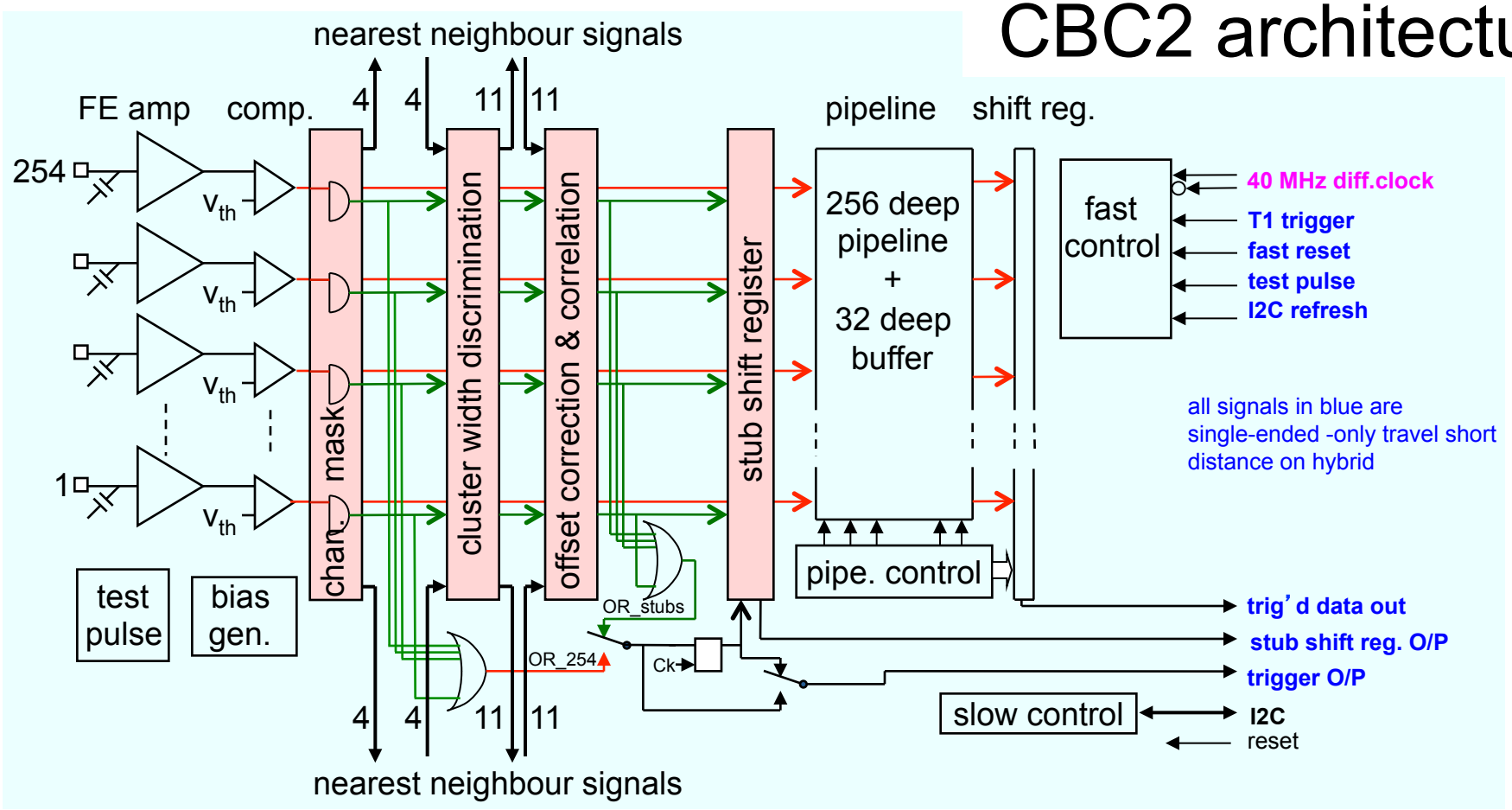
400 GeV protons







CBC2 architecture



front end, pipeline, L1 triggered readout, biasing

~ same as prototype (some bug fixes) twice as many channels

new blocks associated with Pt stub generation

channel mask: block problem channels (not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

trigger O/P: in normal operation 1 bit per BX indicates presence of high Pt stub

test pulse

charge injection to all channels (8 groups of ~32), programmable timing and amplitude

stub finding logic

cluster width discrimination (CWD) logic

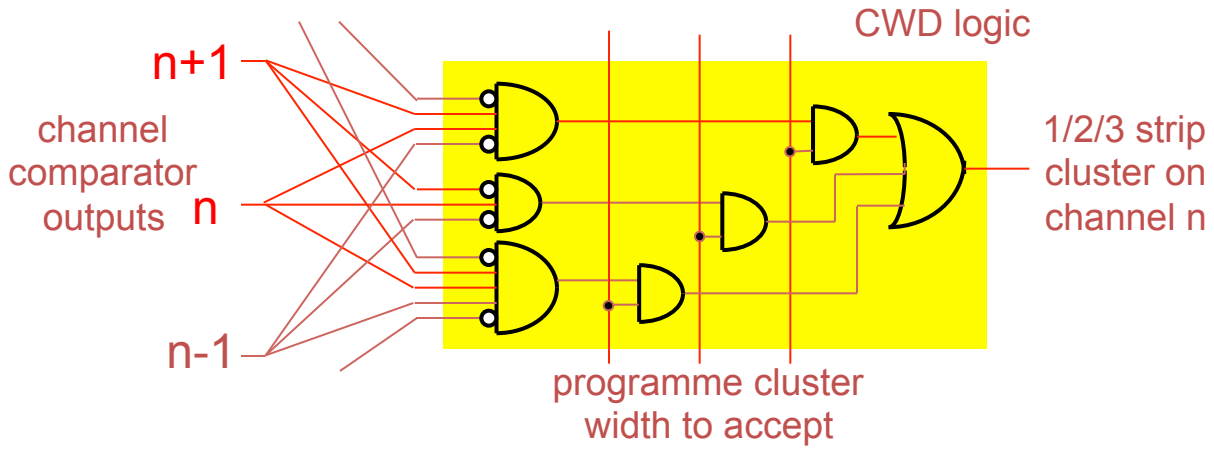
exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

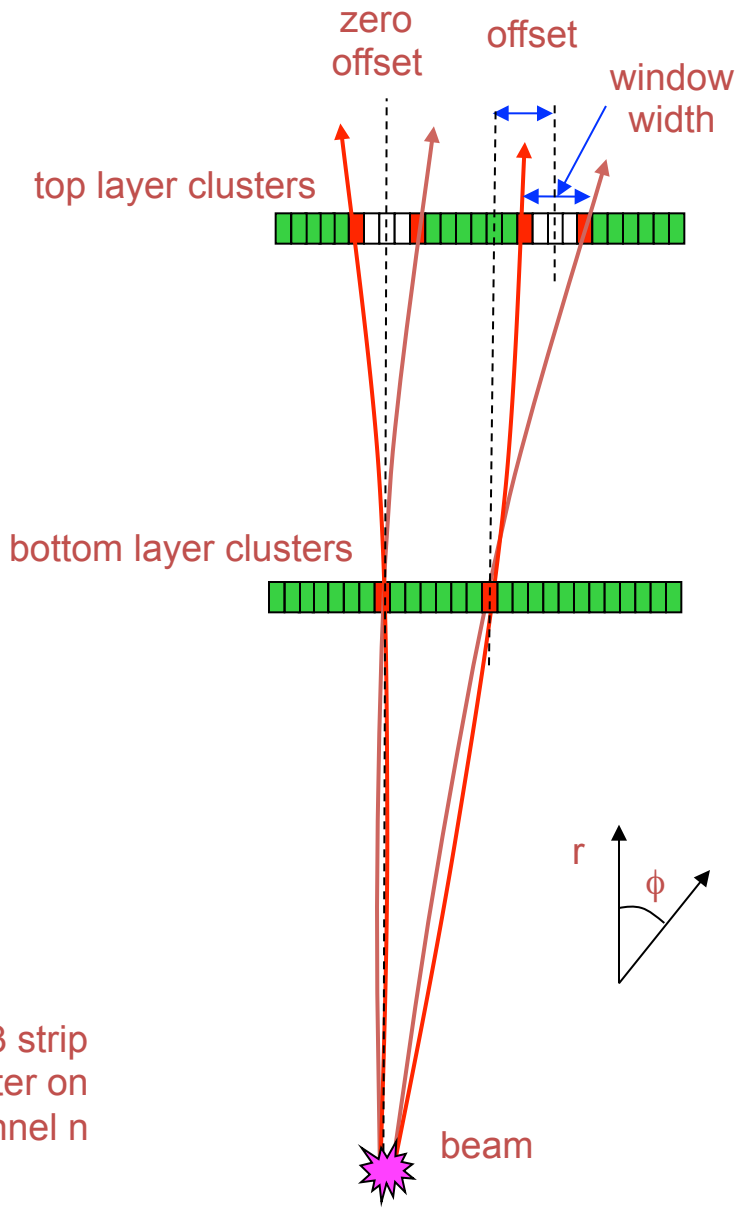
offset correction & correlation logic

for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

window width controls pT cut
stub found if cluster in bottom layer corresponds to cluster within window in top layer
window width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels





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Long Shutdown 1

- End March 2013 – November 2014
- Consolidation for 6.5 – 7.0 TeV operation
  - Measure all splices and repair defective ones
  - Repair of magnet interconnects after 2008 event with new design (clamp, shunt)
  - Finish installation of pressure release valves
  - Exchange of weak cryo-magnets and DFBAs
  - Relocation of equipment to reduce radiation effects on electronics
  - Installation of collimators with integration beam position measurement, injection absorbers refurbishment
  - Injection kickers reduction of heating
  - Experiments consolidation and upgrades
- Plus a lot of other work ongoing
  - Cryogenics, Quench Protection, electrical infrastructure, cooling & ventilation, Radio Frequency, beam dump absorber & magnet, change of dump switches (radiation), electron cloud mitigations …