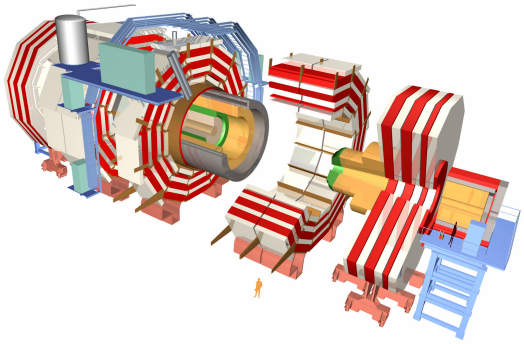
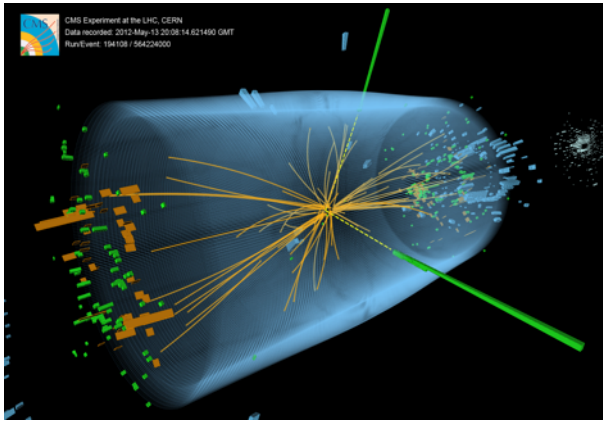




UK CMS Upgrade Oversight Committee

27 May 2015

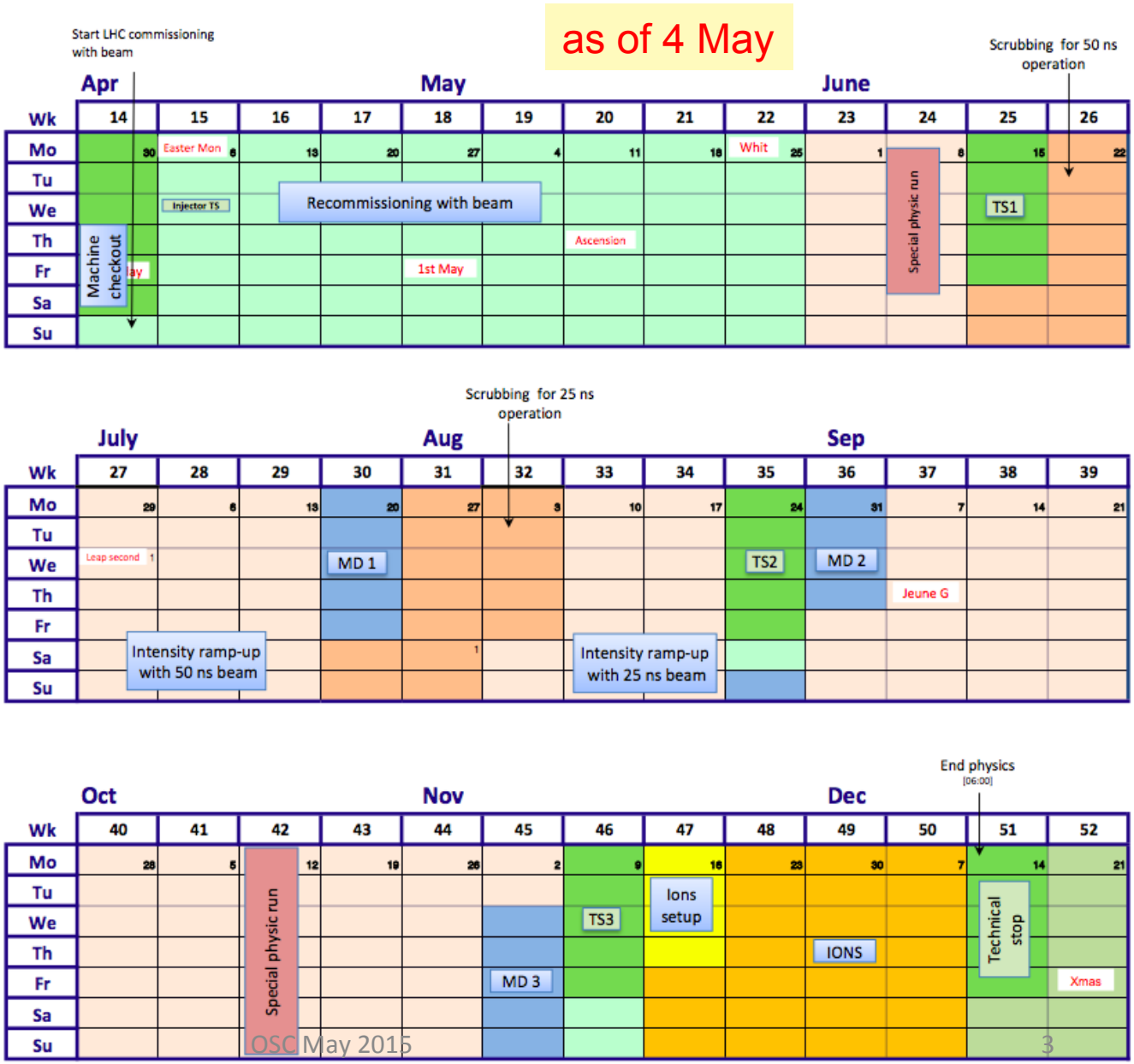
University of Bristol
Brunel University London
Imperial College London
Rutherford Appleton Laboratory

Overview

- Snapshots of LHC & CMS status
  - CMS and LHC are well into recommissioning phase
- Summary of UK upgrade project
  - Recent WP progress
- Finances

2015 LHC schedule

- Generally good progress
  - few week slippage compared to Nov 2014
  - physics foreseen from 1 June
  - but..



LHC news

CMS WGM 4 May

- Good news:
  - beams routinely ramped at 6.5 Tev
  - Beam ramped and squeezed at 40 CM
  - Injected nominal intensity bunches
- Not so good news:
  - Repeated UFO events in one sector (15R8) traced to a ULO (Unidentified Lying Object) which is located within one specific magnet. One hypothesis is that it might be a piece of insulation material
  - They are still trying to fully explore what can be done to mitigate this: plan is to find a sweet spot to steer the beam around the occlusion. This approach allows pursuing the beam commissioning program so far

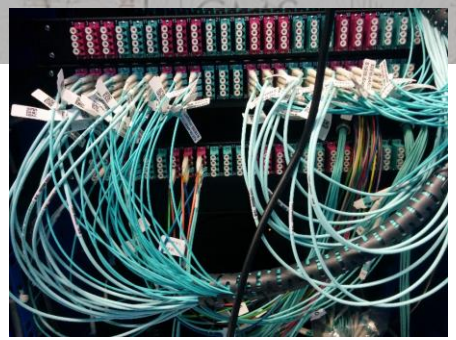
CERN Bulletin 22 May: no beam losses at obstacle in latest intensity tests

L1 trigger

CMS WGM 4 May

- Legacy trigger timed in, generally working well and ready for collisions
  - ECAL OSLBs installed and working (splits paths for legacy and upgrade)
  - Trigger menu for 50ns operation installed at P5
  - DQM plots are available, including for Calo Stage-1
- Remaining tasks
  - HCAL splitters to be installed (this month)
  - Testing of HF μHTRs to RCT input. Starting.
  - RPC splitters installation in progress (complete this month)

L1 : stage 1 calo trigger upgrade



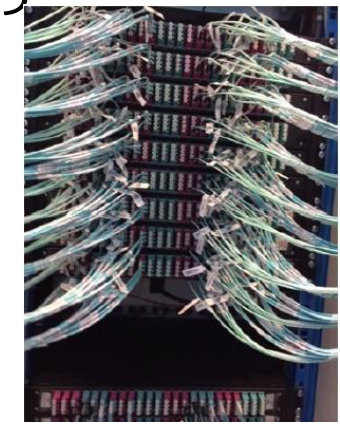
	Unpack Input	Subtract PU	Cluster/ Sum/ Isolation	Calibration	Sort	Pack	Simulator emulator match	Board emulator match
Central Jets	✓	✓	✓	✓	✓	✓	✓	✓
Forward Jets	✓	✓	✓	✓	✓	✓	✓	✓
ET, HT, MET	✓	✓	✓	NA	NA	✓	✓	✓
MHT/HT	✓	✓	✓	NA	NA	✓	✓	✓
E/g	✓	NA	✓	NA	✓	✓	✓	✓
Iso E/g	✓	NA	✓	NA	✓	✓	✓	✓
Taus	✓	✓	✓	✓	✓	✓	✓	✓
Iso Taus	✓	✓	✓	✓	✓	✓	✓	✓

Ben Kreis

- RCT/ORSCs installed, cabling and patch panel done, MP7 crate installed
- Stage-1 algorithms for pp and firmware done. Runs in one MP7 processor. Testing matches emulator.
- Algorithms and firmware for HI running in progress
- DAQ link from MP7 via AMC13 tested successfully at full bandwidth . Some work remaining to integrate with Stage-1 firmware
- Stage-1 system successfully runs in parallel with legacy trigger at P5 during data-taking using GT test crate
- Stage-1 system has successfully triggered CMS through GT at P5 at rate similar to legacy

L1 CALO Trigger Upgrade: status

- Status of data link splitting for parallel operation in 2015
  - ECAL: All fibers from OSLB to Layer-1 patch panel installed, with 16/576 links tested to Layer-1 →
  - HCAL: awaiting HB/HE splitters (1st batch shipped). First crate of HB/HE μHTRs installed at P5 and remainder by end of May
  - HCAL fibers (144) to be laid out this week and testing with the trigger should commence afterward

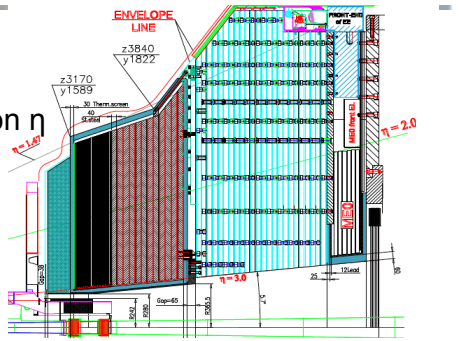


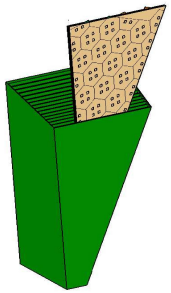
- Status of calo trigger processor installation and testing
  - All required CTP7 boards for layer-1 at CERN and 18/36 already installed.
  - Layer-2 MP7 have been under use for testing Layer-1, uGT, algorithms
  - Pattern tests of 1/9 of layer-1/layer-2 interconnections in progress
  - Pattern tests from Layer-1 → Layer-2 → μGT to commission energy sums expected by end of May

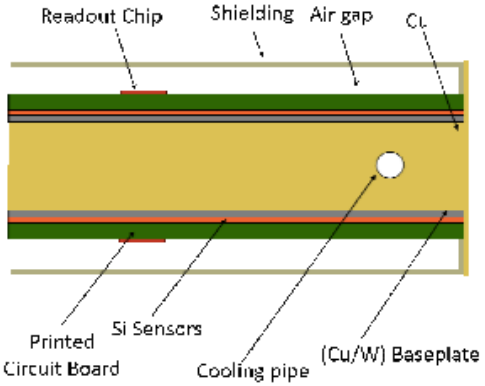
Forward calorimeter decision

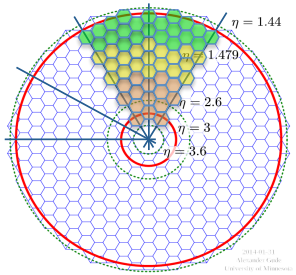
- High Granularity option chosen mainly for risk reasons
  - employs similar technology to Tracker (silicon, CO_2, ASICs)
  - T. Virdee interim PM
  - possible UK role under consideration
    - significant supplementary funding via ERC, plus PRD post

Silicon-tungsten/lead/copper EM (25 X0, 1λ) and silicon/brass front hadron (3.5λ) calorimeter
6.2M channels, pad sizes 1cm^2 or 05 cm^2 depending on η
Scintillator-brass backing calorimeter (5.5λ, low radiation environment)









UK R&D status

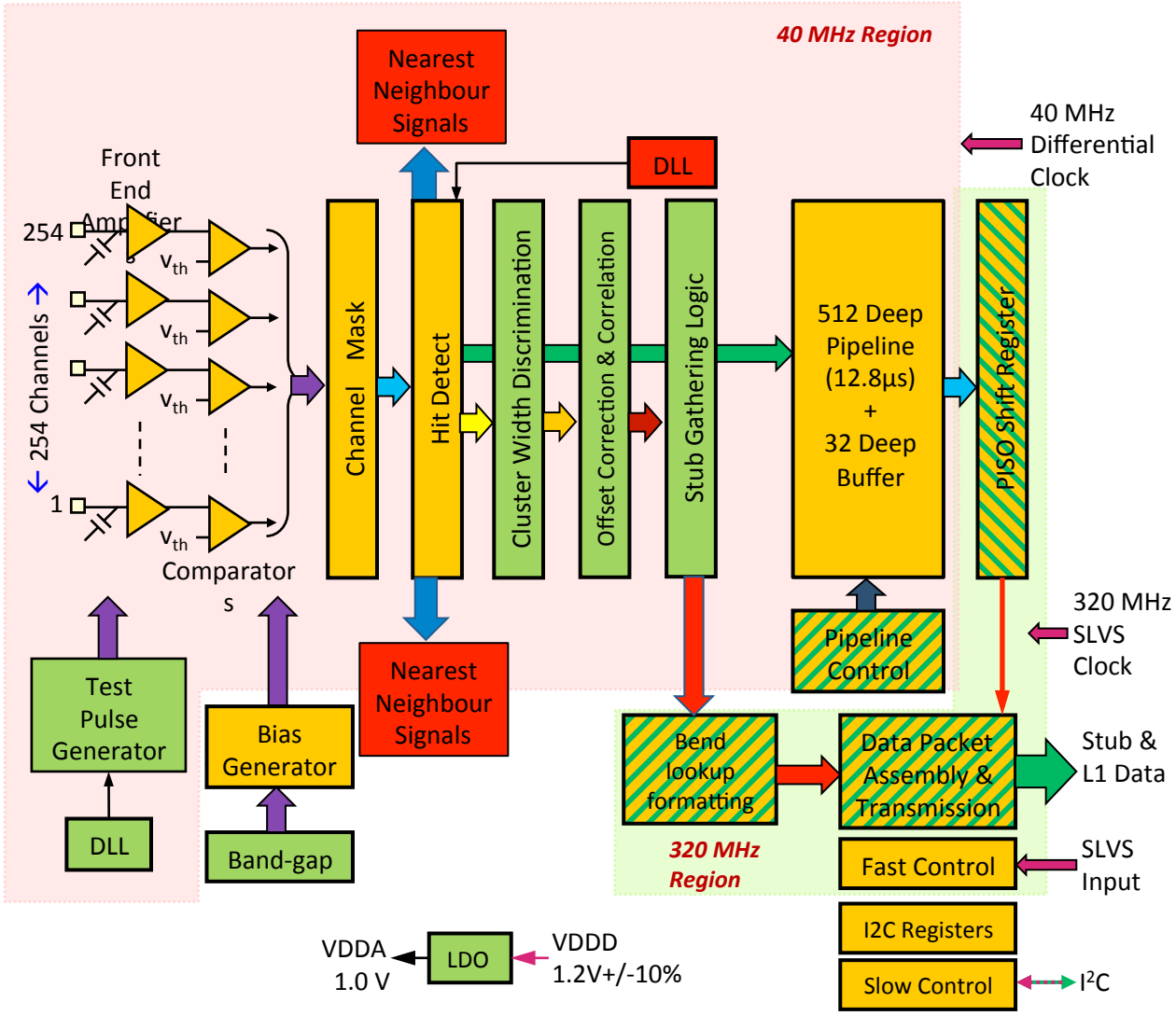
Last 6 months

- WP2:
  - continued steady progress with CBC3 design
    - expected CBC3 submission Feb 2016 in MOSIS run
  - First series of FC7 production complete but unexpected problems
- WP3: progress towards installation of TDR trigger
  - UK Stage-1 commitments essentially complete
  - UK Layer-2 for 2016 trigiger in place and being commissioned
    - details to follow
- WP2 & WP3: progress on TMTT studies
- CMS TP delayed to LHCC to June 2015
  - decision on forward calorimetry made April 2015, endorsed CB 8 May

Overview of CBC activities

- CBC2 characterization complete (reported last time)
  - including ionizing irradiation (to 180 Mrads!) and SEU testing
  - results informing CBC3 design
- CBC2 based module tests continue
  - mini-module with irradiated sensors in test beam in June
  - full-size module test beam in November
- CBC3 design now in full flow
  - all modifications and additional features agreed with CMS systems team collaborators
  - specification document complete and circulated

CBC3 status



design work progressing

main new features are:

- stub address generation & transmission off-chip @ 320 Mbps
- longer L1 pipeline (12.8 usec)
- higher L1 trigger rate capability (up to 1 MHz)

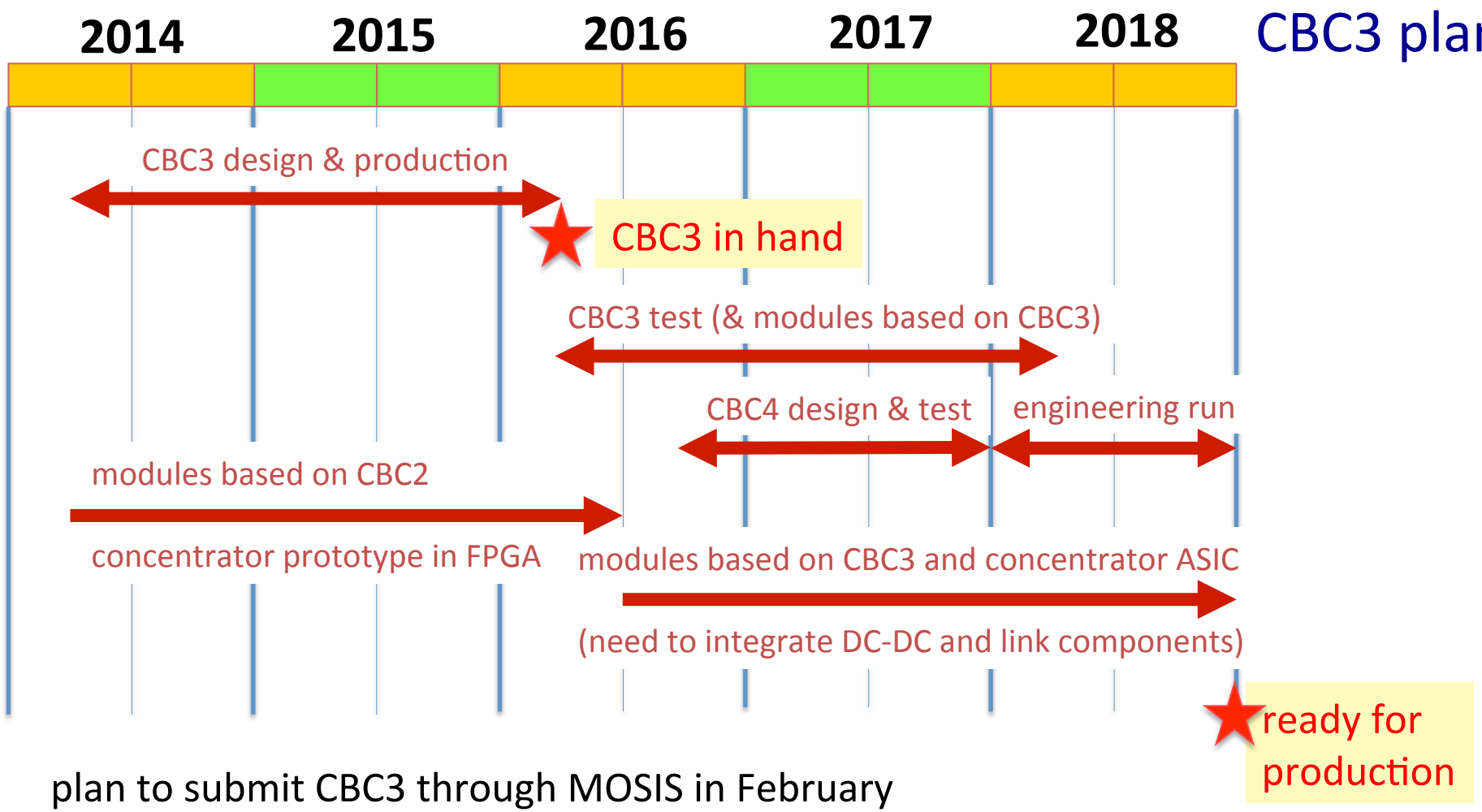
major new blocks are:

- stub gathering logic
  - ➢ complete
- data packet assembly & transmission
  - ➢ at advanced stage

review meetings held at key stages to monitor progress

Complete | Preliminary Layout | In progress | To do

CBC3 plan



plan to submit CBC3 through MOSIS in February

limited number of chips but ~ half the cost of full wafer run

can expect chips in hand ~ May

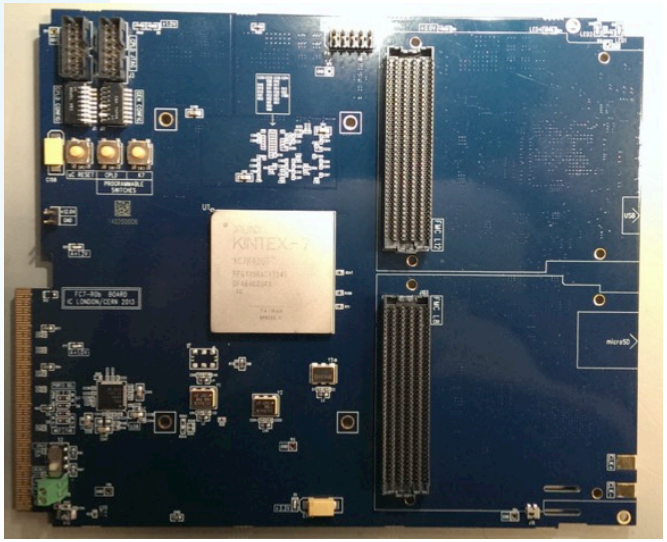
(small schedule slippage but have to comply with fixed submission dates)

FC7

- Problems discovered in boards built for TCDS project
  - upgraded CMS TTC system, on tight schedule

TCDS hardware status

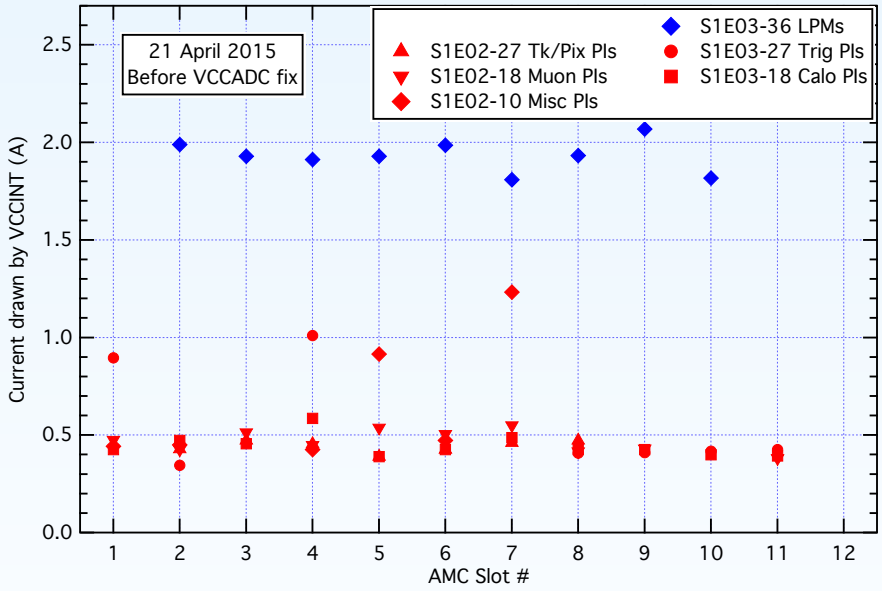
- All TCDS boards are based upon the same µTCA motherboard - the FC7
  - Collaborative design between CERN and Imperial College
    - https://indico.cern.ch/event/299180/session/5/contribution/118
- 70 FC7s produced in 2014
- Installed in P5 since August 2014
  - 10 LPMs
  - 40 PIs
- Boards have started to fail since January 2015
  - Failure modes different for LPM & PI, but very similar for a given firmware build

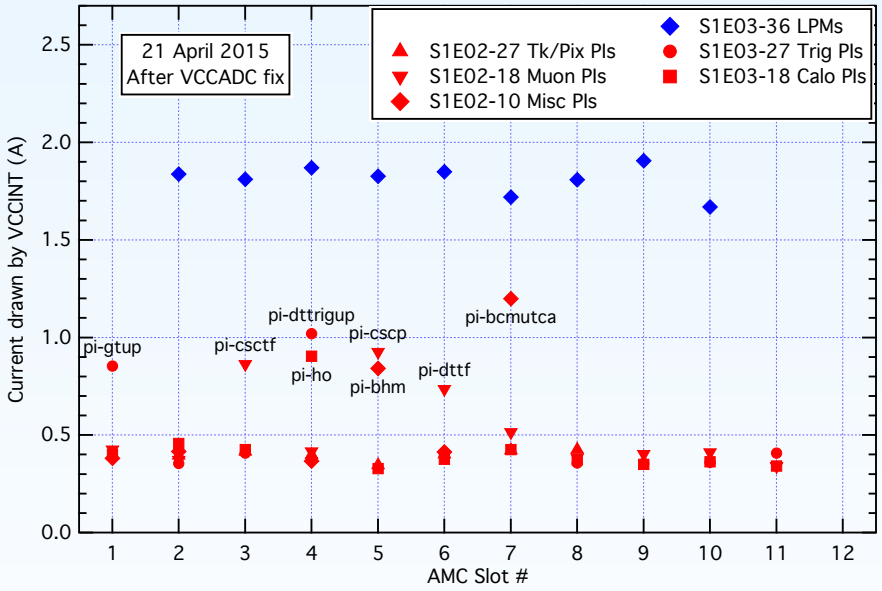


TCDS Status - 16 April 2015 *jan.troska@cern.ch* 1

FC7 failures

- Operational failures are accompanied with an increase in the current consumed in the FPGA core voltage
  - Status on 14 April 2015:

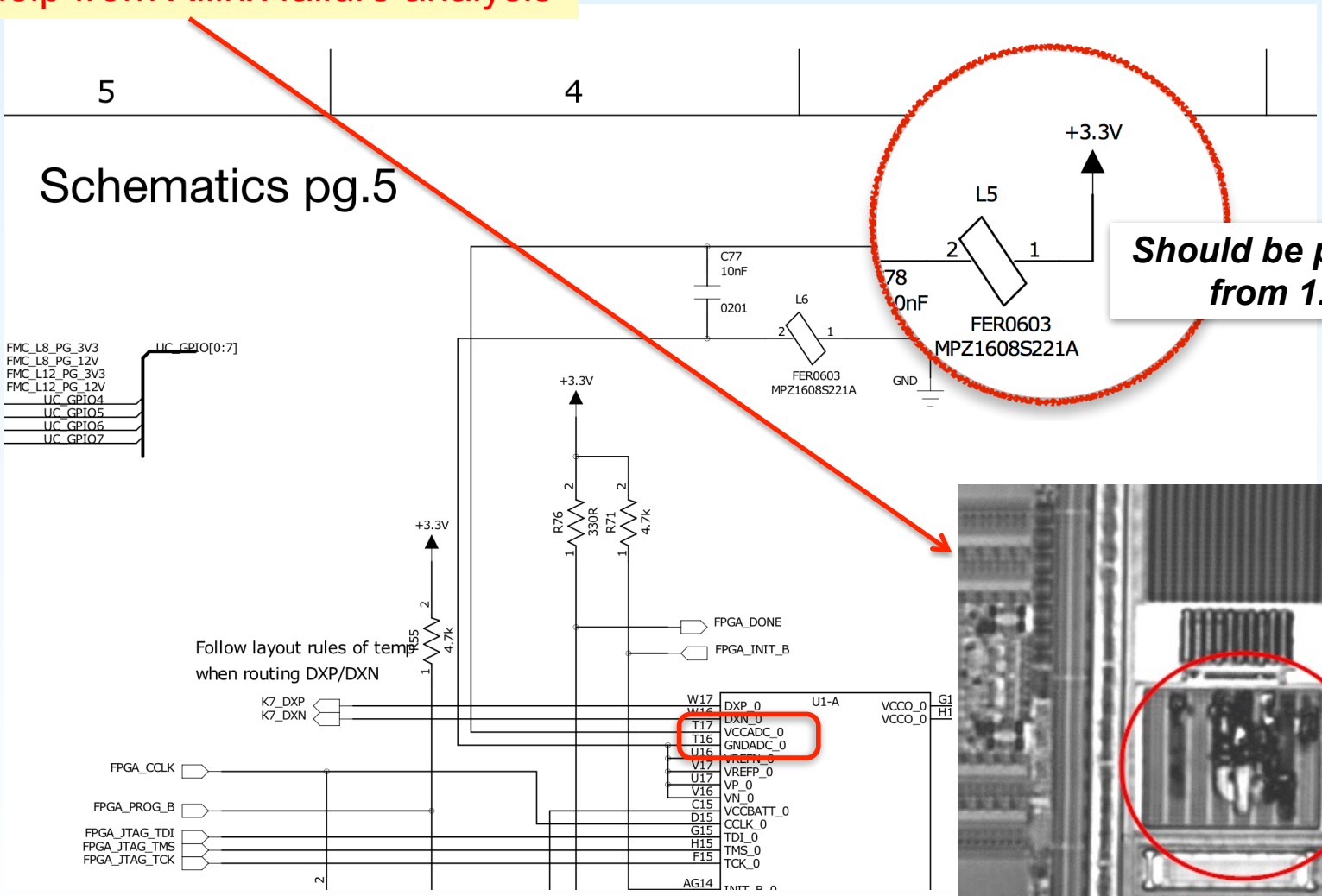




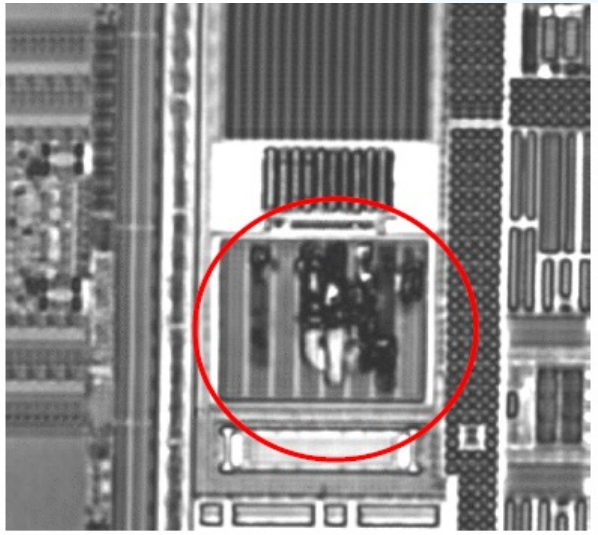
  - 8 boards with high current
  - 4 broken

XADC powering schematic

with help from Xilinx failure analysis

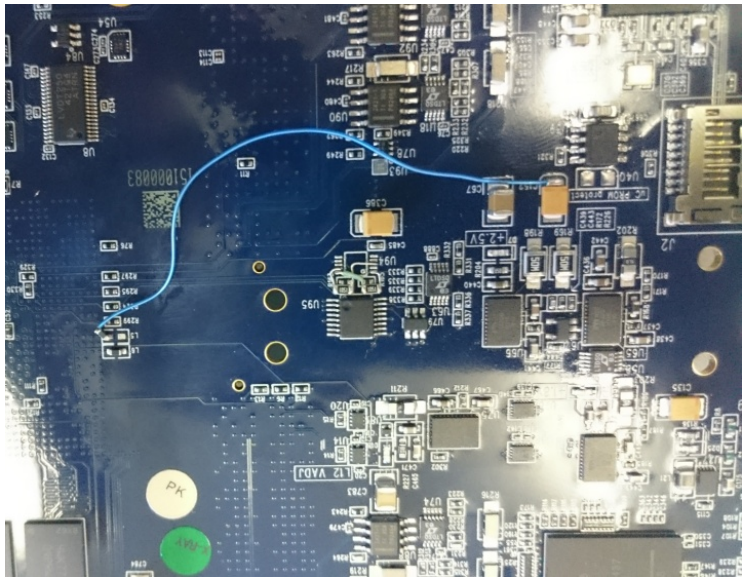


Should be powered from 1.8 V



FC7 current status

- Problem is now believed to be understood but proceeding with caution
  - simple repair to existing boards
    - however stressed boards likely to have been damaged
  - error corrected in layout for R2
  - design modified to be conservative in all respects
  - internal design review with CERN, and some outside experts, April
  - replacements underway
    - existing design, with correction for urgent needs (TCDS and pixel prototyping) reordered
    - R2 ready for submission very soon



- Some important lessons everywhere
  - listed in report

WP3 objectives and status

- Calorimeter trigger status
  - to be updated orally at meeting
    - review held April – report not yet issued
    - commissioning status (Stage-1 & TDR)
    - Plan B readiness
  - all MP7s required for UK commitments delivered
    - but some manufacturing issues and PCB material is under consideration for the future, as with the FC7

2016 Calorimeter Trigger Milestones

- **Milestones related to CTP7**
  - 25.10.2014 3 CTP7s at CERN
  - 15.11.2014 4 CTP7s at CERN (includes the previous)
  - 20.01.2015 8 CTP7s at CERN (includes the previous)
  - 28.01.2015 12 CTP7s at CERN (includes the previous)
  - 25.03.2015 28 CTP7s at CERN (includes the previous)
  - 08.04.2015 36 CTP7s at CERN (includes the previous)
- **Milestones related to commissioning of the trigger**
  - 22.12.2014 Layer-2 – Patch Panel – Layer-1 Commissioned
  - 16.01.2015 oSLB and HF uHTR systems commissioned
  - 19.01.2015 Layer-2 – Patch Panel – Layer-1 Connected to uGT
  - 25.11.2014 First Version of CTP7 firmware (incl. input playback)
  - 09.03.2015 Final Version of CTP7 firmware (except DAQ link)
  - 17.02.2015 Final design of Algorithms and data format defined
  - Decision to upgrade 2016 trigger inputs from ECAL and HCAL
  - 17.06.2015 B/E uHTR system connected to the trigger - Commissioned
  - **02.09.2015 System ready for parallel data taking**

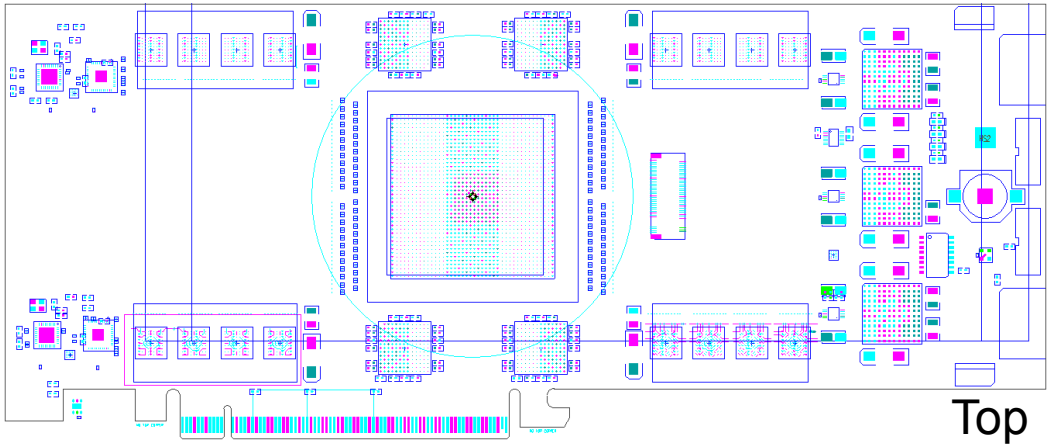
MP7 order status

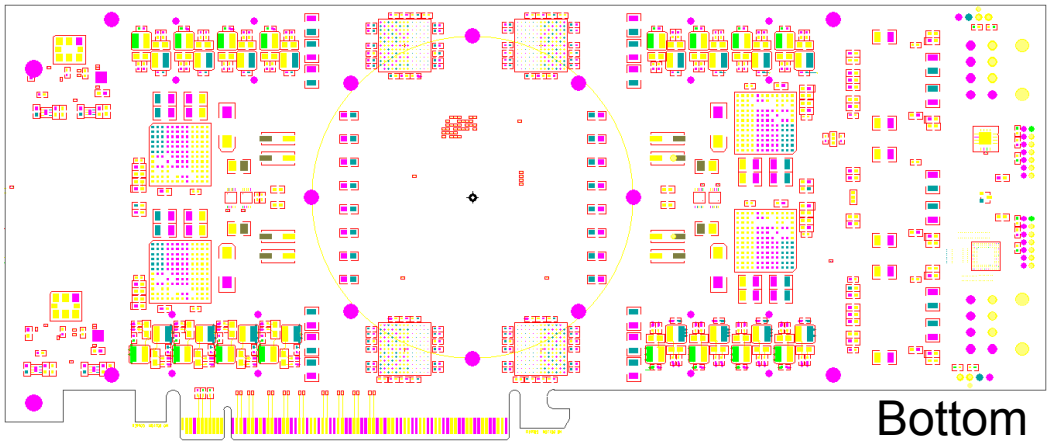
- Following prototyping/pre-production, two orders of 16 boards
  - Prod-1: 16 delivered (Hapro) + 16 from Exception, essentially complete
    - a bit of a struggle with UK company
  - Hapro orders of 8 + 32 launched in 2014 (Prod-2 and Supp Prod-1)
    - assembly error with first 8, so delay
      - now complete
    - manufacturing error with pre-series cards of 32 order.
      - delay while new PCBs procured, delivery in August

Project	*Pre-prodn*	*Prod-1*	*Supp. Prod-1*	*Prod-2*	*Future req*	*Prod Total*
Calo Trig Layer-2 & demux	*9*	*25*	*5*	*4*	*12?*	*34-46*
GT & GMT	*1*	*4*	*0*	*14*	*0*	*18*
Barrel Muon Track finder	*1*	*3*	*0*	*14*	*0*	*17*
Stage-1	*2*	*0*	*2*	*0*	*0*	*2*
LLR	*1*	*0*	*1*	*0*	*0*	*1*
Total required	*14*	*32*	*8*	*32*	*0*	*72-84*
Orders	*14*	*32*	*8*	*32*	*12?*	*72-84*
Delivery	*Done*	*Aug-Oct*	*Dec*	*Apr?*	*?*	

MP-Ultra: Successor to the MP7

- Successor to the MP7 based on Xilinx Ultrascale and Ultrascale+ FPGAs
- Up to 96+96 (Tx+Rx) links at up to 16Gbps: bandwidth > **1.5+1.5 Tbps**
- 8Gb of RLDRAM3 in four independent banks
- PCIe form-factor – easier to manufacture than µTCA
- Two variants planned spanning 3-generations/families of FPGA:
  - 48-link variant – very low-cost with maximal logic/bandwidth ratio
  - 96-link variant (Ultrascale FPGA) – maximum bandwidth
  - 96-link variant (Ultrascale+ FPGA) – maximum bandwidth & logic

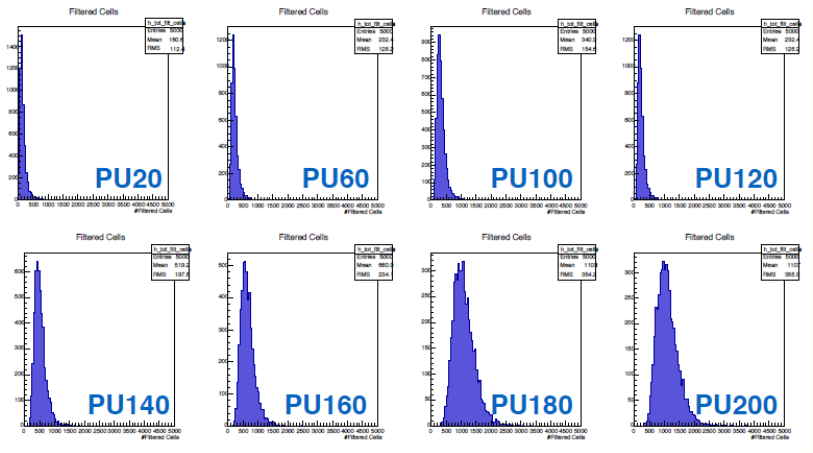

Top


Bottom

Track-trigger progress

- Now quite substantial UK-wide activity focusing on
  - simulations
  - algorithms for track finding in FPGA
  - firmware design
  - implementation in MP7 demonstrator system

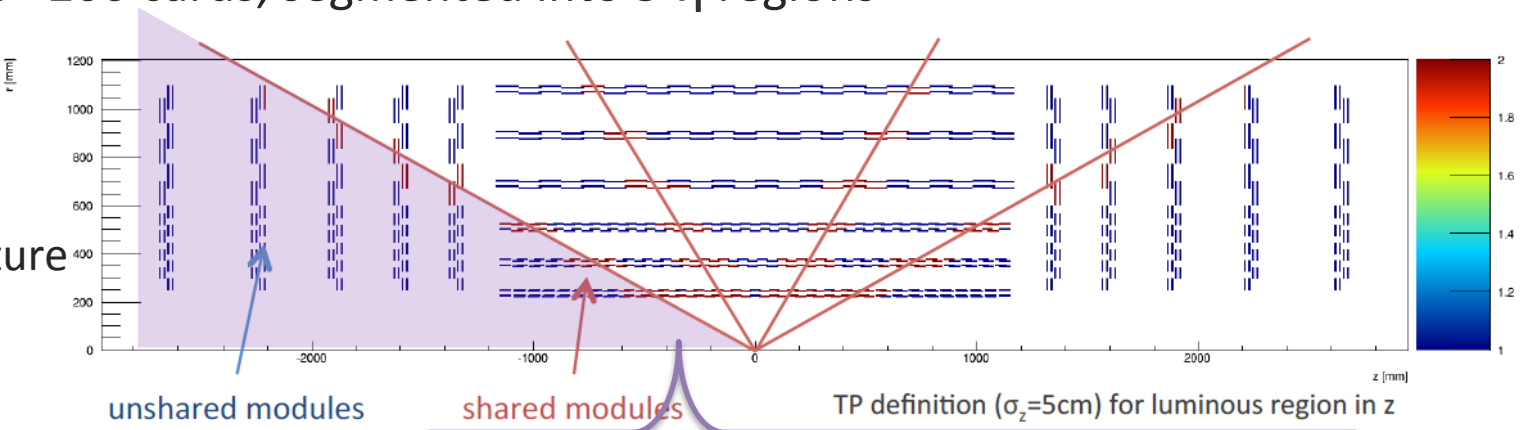
- Target: working demonstrator by August
  - of course with limited objectives compared to final system



Layout of fully Time-Multiplexed Track-Trigger

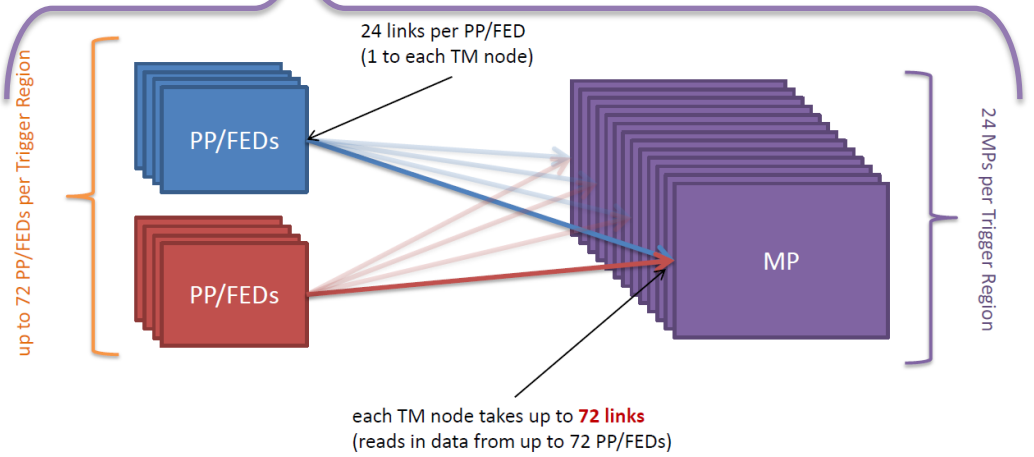
- Focusing on demonstration of the concept
  - entire tracker could be read out by MP7-like processing cards
  - requires ~200 cards, segmented into 5 η regions

- module sharing
- ≤ 2 regions
- simpler architecture
- no deghosting



- sharing defined by large luminous region in z

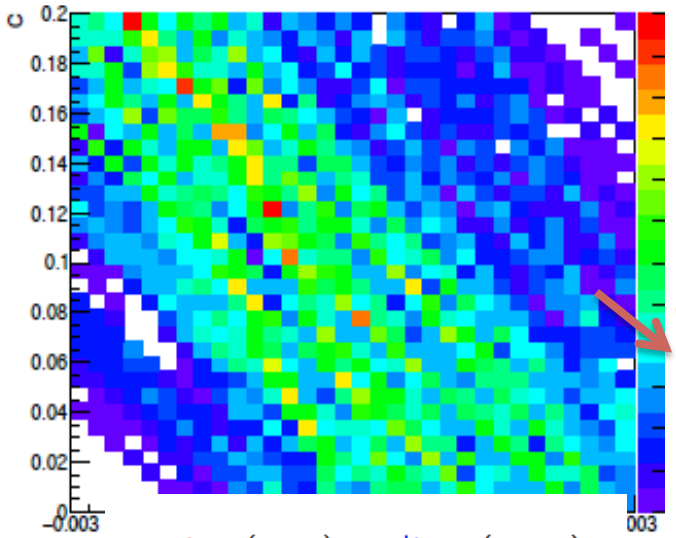
- feed time-multiplexed data to regional processors
- TM period of 24-36 BX possible using MP7s

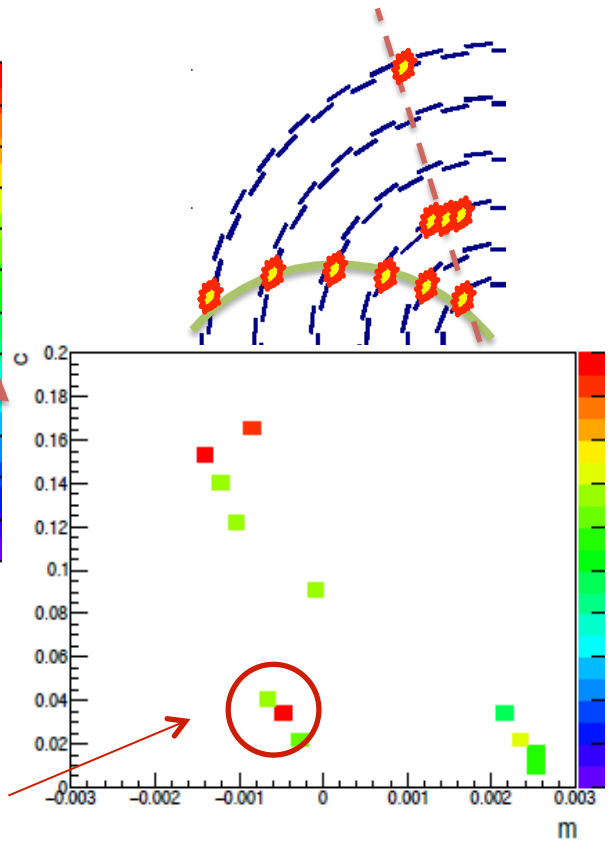


Track-finding in FPGA

- Hardware requirements already feasible, but processing in FPGA very challenging
  - exploring Hough transform approach:
  - line in real space -> point in inverse space

- pipelined dataflow
  - natural with TM
  - matches FPGA needs
- find stubs in 2D
  - 2D histogram
- selection to reduce number of candidates

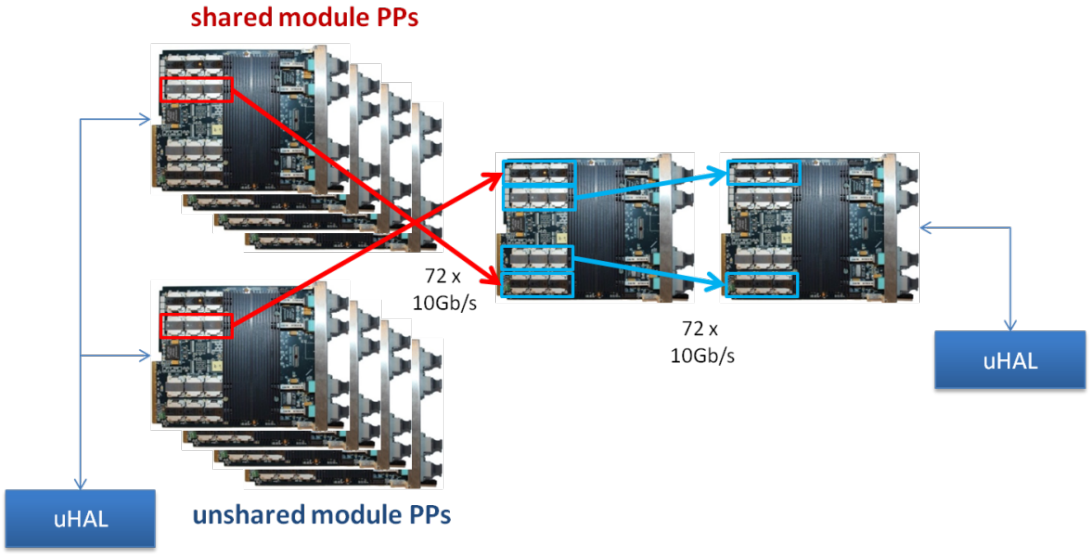


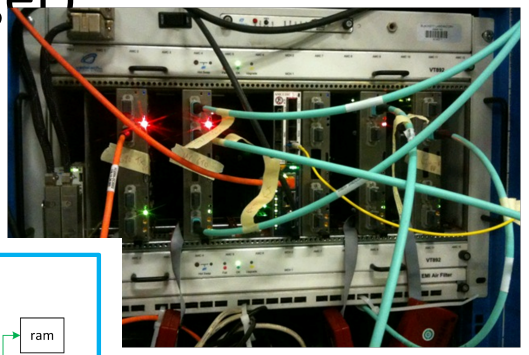


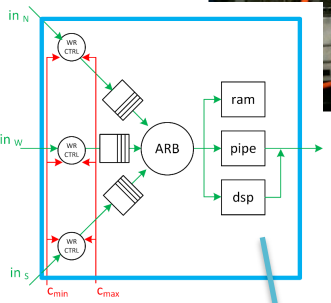
valid track where lines intersect
i.e. stubs which share the same (m,c)

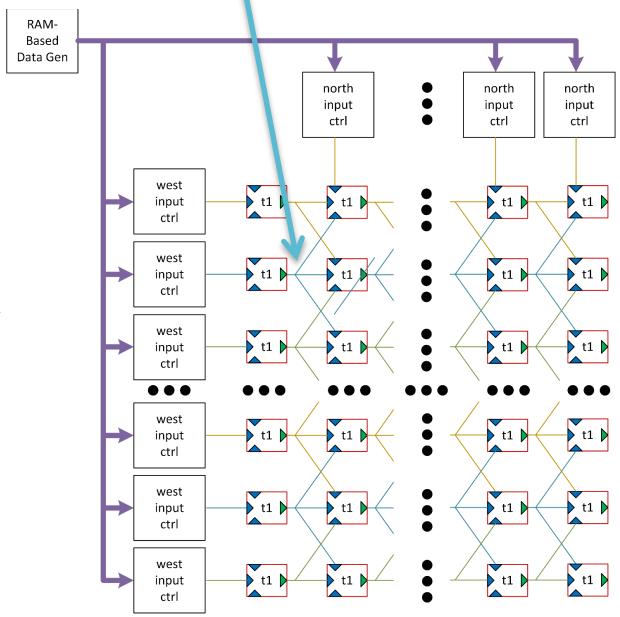
Status of demonstrator

- Hardware exists in working form (from calo trigger)
  - adapt for track-trigger time slice









  - software validation under way
- Firmware implementation of Hough array
  - self-filling systolic array
  - integrating with infrastructure firmware

Finances

- Expenditure – no special issues
  - Staff expenditure essentially as foreseen
    - including slight ramp-up in RAL TD, matching our delivery plan
  - Travel also as foreseen – further LTA commitments under way
- Materials & equipment
  - WP2:
    - CBC3 manufacture early 2016
  - WP3:
    - For purchases via CERN (FC7 & MP7) direct invoicing to Imperial now working well

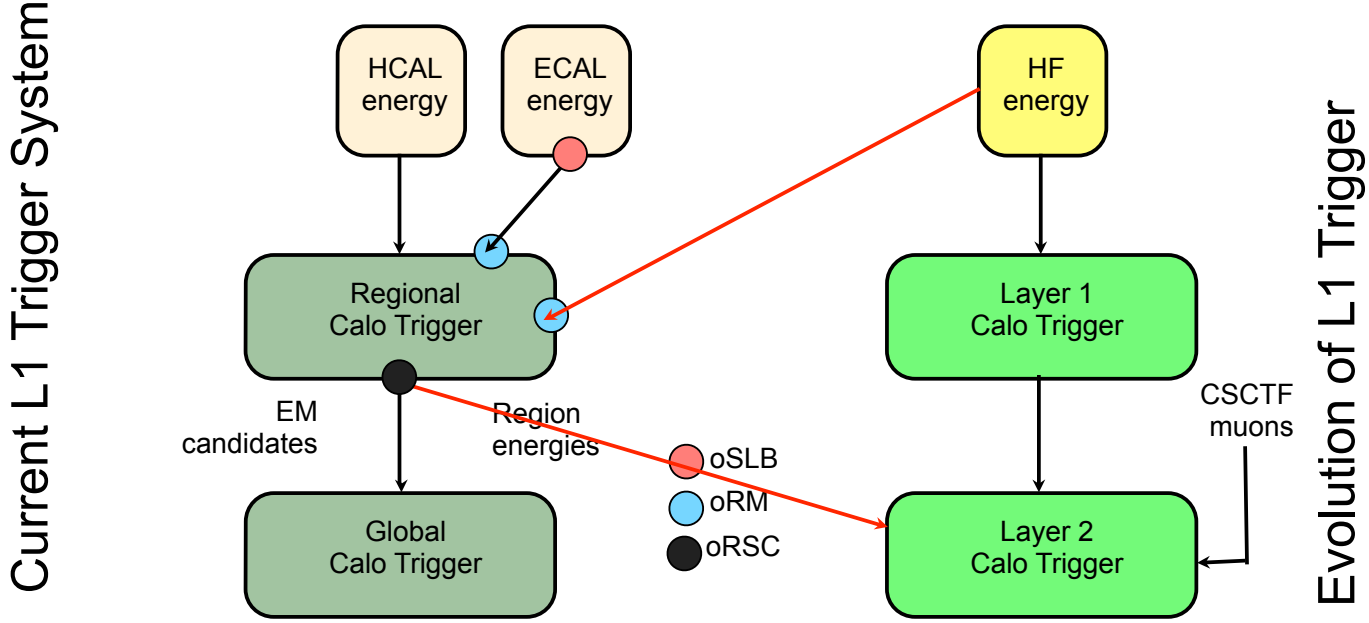
Conclusions

- Milestones
  - reported in document
- Risks
  - register revised
  - no new risks, but MP7 and FC7 issues have materialised
- Trigger project in crucial commissioning phase
  - SP team has been playing significant role

Further information

Intermediate trigger - 2015

- Limited to use current RCT and current GT



- Significant performance improvements possible in eγ, τ and jets
- Prototype processor cards and (new) oRSC cards to duplicate signals
- Retains data to legacy GCT for easy rollback with just reconfiguration