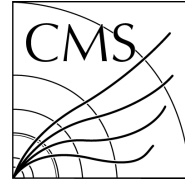


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Upgrades of the Tracker and Trigger of the CMS experiment at the CERN LHC

1	Executive Summary.....	2
2.	Project history and recent developments	2
2.1	LHC upgrade schedule and planning	2
2.2	CMS planning	4
2.3	UK adaptation to CMS planning	5
2.4	Other news	5
3.	Work Package 1: Management	6
4.	Work Package 2: Outer Tracker Readout	7
4.1	Objectives	7
4.2	Progress	7
4.3	Deliverables	10
4.4	Staff on project.....	11
4.5	Expenditure.....	11
5.	Work Package 3: Level-1 Trigger	12
5.1	Objectives	12
5.2	Progress to date	12
5.3	Overview of CMS plans	13
5.4	Staff on project.....	13
5.5	Expenditure.....	13
5.6	Deliverables	13
6.	Work Package 4: High Granularity Calorimeter.....	15
6.1	Objectives	15
6.2	Progress to date	15
6.3	Overview of CMS plans	17
6.4	Staff on project.....	17
6.5	Expenditure.....	17
6.6	Deliverables	17
7.	Work Package 5: L1 track finder	19
7.1	Objectives	19
7.2	Progress to date	19
7.3	Overview of CMS plans	21
7.4	Staff on project.....	21
7.5	Expenditure.....	22
7.6	Deliverables	22
8	Risk register.....	24
9	Finances	24
10	Gantt charts	24
11	Milestones	25
12	Glossary	26

1 Executive Summary

The new project started in April 2013; it continues work on the tracker and trigger begun in the previous R&D project. For the Phase I upgrade of the L1 calorimeter trigger, this is a construction project.

In the last six months there has been further progress with the UK activities:

- Work continues steadily on the final CBC design. Manufacturing submission is foreseen a few months later than reported before, in mid-2016.
- The FC7 modifications were very successful and new boards of the final design are now available and in use in CMS, and some other UK projects.
- Manufacturing of the MP7 is complete with a high yield.
- The development of algorithms and firmware for the Level-1 trigger is complete, now subject to final validation.
- The TDR trigger was successfully proven during the final period of 2015 running and therefore adopted by CMS for operation in 2016. It is now in the final stage of commissioning, e.g. with constants being tuned and calibrated.
- The SWATCH online software system developed for the L1 trigger with UK leadership is essentially complete, and should lead to major improvements in trigger operation and maintenance.
- A new work package has begun for the proposed High Granularity Calorimeter, which is largely funded by a substantial ERC grant at Imperial, with additional support from an STFC PRD post for two years.
- There has been considerable progress in developing a demonstrator of the Time Multiplexed Trigger architecture for the L1 track-finder needed for the future track-trigger. A new work package covers this activity.
- J. Brooke has recently taken up the post of Phase II L1 Trigger coordinator with immediate effect.

2. Project history and recent developments

The LHC upgrade is proposed to take place in two main stages, with an increase in luminosity reaching $\sim 2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ a couple of years after 2015 in LHC Run II, then after a two to three year shutdown from 2023 in LS3, to $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ levelled luminosity, denoted as Phase II at the High Luminosity (HL)-LHC. A total of 3000 fb^{-1} in integrated luminosity over about a decade is the goal. This should lead to a typical pileup of 140 events/BX but in view of the possibility to increase the luminosity even higher, or accommodate fluctuations without much degradation in performance, CMS aims to be operable at up to 200 events/BX corresponding to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ levelled luminosity.

The current phase of the project began on 1 April 2013. Until recently there had been two technical work packages: WP2 for the Phase II outer tracker readout R&D for HL-LHC; WP3 for the calorimeter trigger construction for Phase I, starting in 2015, and further R&D aimed at Phase II. As we will report, the installation and commissioning of the Phase I L1 calorimeter trigger is now complete, hence the WP3 activity will now focus more on future hardware and the L1 track-finder, in collaboration with WP2. Since the last meeting two new work packages have been defined, which report for the first time, on the forward calorimeter project and on L1 track-finding.

We note that since the last OSC meeting, CMS has elected a new spokesperson who will succeed Tiziano Camporesi in September; this is Joel Butler of FNAL.

2.1 LHC upgrade schedule and planning

Over the past six months, CMS has been working intensely and making significant progress on four major fronts:

- Operating the experiment and taking data at 13 TeV during 2015;

- Preparing for the LHC run in 2016;
- Pursuing the programme of detector upgrades: Phase I upgrades in 2015-2017 and the preparation of Technical Design Reports for the Phase II upgrade, for the HL-LHC;
- Exploiting in full the physics potential of Run I data.

Throughout 2015, CMS took high quality data, with all detector systems in use from the start of Run II, from the intensity ramp-up with 50 ns beams to the 25 ns beams of the main run. The components of CMS that were new or upgraded after Run I operated smoothly alongside the legacy components of CMS.

The major concern last year was the magnet, where there were repeated problems since March with the cryogenic system. Overall the impact on data taking was not significant - of the total integrated luminosity delivered by the LHC in 2015, ~75% of proton-proton collisions and ~95% of heavy-ion collisions were recorded with full magnetic field - but the absence of a fully understood diagnosis and corrective action was still a worry. This has now been corrected, with a major “deep clean” during the end of year technical stop.

The problem was caused by contamination in the underground Cold Box, presumed to be due to oil from the surface compressor station. At the end of the 2015 run, a task force set up in May 2015, consisting of experts from inside and outside CMS, converged on a plan to steer the actions to reinstate the cryogenics system to its normal status. A panel of international experts endorsed the proposed repair programme and also reviewed the long term risks to magnet operation. Replacement of several contaminated components, along with concurrent deep cleaning of essentially all remaining elements of the Cold Box, is now complete and the cryogenic system is believed to be fully repaired. Re-commissioning of this system is now in progress and full magnetic field should be attainable by the end of April.

Another issue that affected the YETS 2015-16 work was some cooling-water leaks in one endcap, towards the end of heavy ion running in early December. Investigations identified the source as weaknesses in the internal cooling circuits of muon chambers, present since manufacture, although all elements had successfully passed quality-control tests. Repair of the identified leaks and collateral damage, and mitigation measures to lessen the impact of any recurrence, was successfully completed by early March, allowing the detector to be closed just before Easter, meeting the target for the first LHC beams of 2016 to circulate.

A major activity during YETS 2015-16 was commissioning of the trigger and data acquisition system for the 2016 physics run. The major detector changes for 2016 include a new Level-1 trigger system and a new readout system for the Hadronic Calorimeter, both based on μ TCA electronics. A series of four short commissioning runs took place in February and March, first to re-establish the detector operation and performance achieved in 2015, and then to upgrade to the new trigger. After this was successfully integrated and timed in, consolidation of operations continued, as well as collection of cosmic muons, mainly for tracker alignment.

Over the Easter weekend the LHC re-established operations with beams (Figure 2.1). During the first week the LHC delivered “splash” events to each of the experiments which confirmed the timing of the readout of ECAL, HCAL and muons, and provided more data to further refine the understanding of the calorimeter trigger chain.

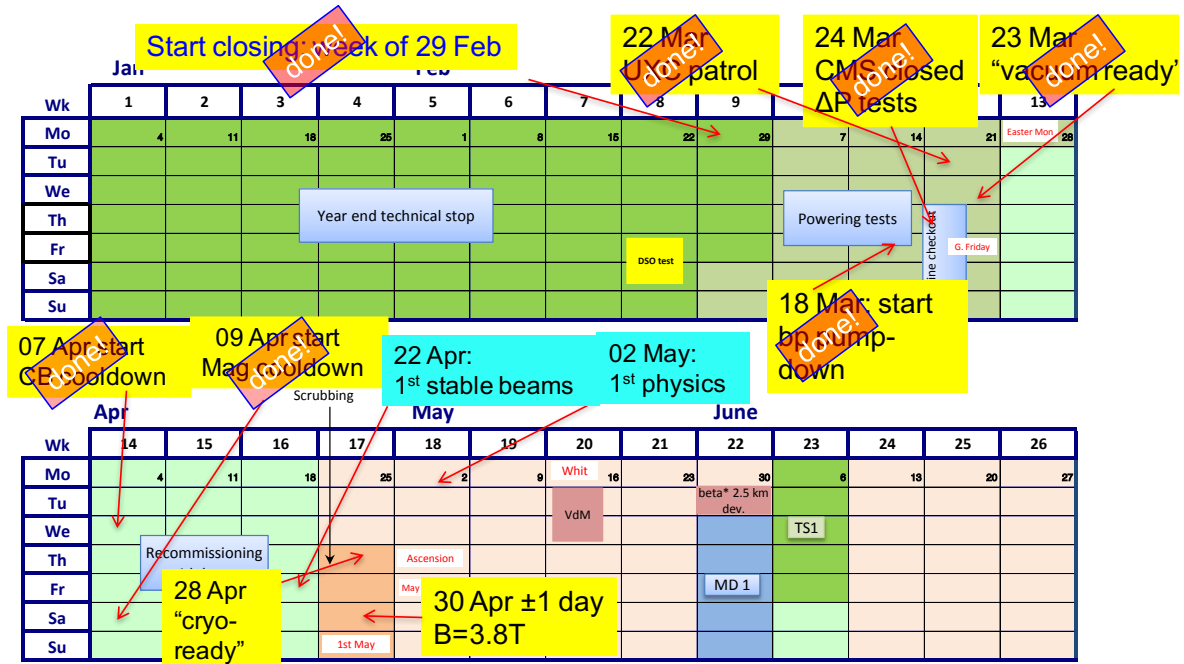


Figure 2.1: The LHC 2016 status and near future plans in mid-April.

2.2 CMS planning

In parallel to operating the detector in Run II and the completion of the Phase I upgrades, CMS is pursuing a concerted effort to plan the Phase II upgrade for the HL-LHC era. As a reminder, the upgrade is documented in a Technical Proposal (TP), which presents the main motivations and features of the upgrade, and a Scope Document (SD), which complements the TP with additional studies, including the impact of potential scope and cost reductions on the detector performance and physics reach. A review by the LHCC and the UCG concluded that the upgrade design is well advanced, has a reliable CORE cost estimate, and should meet the requirements of the HL-LHC. In October 2015, the RRB closed the first step of the Phase II upgrade approval process and encouraged CMS (and ATLAS) to proceed with the preparation of Technical Design Reports (TDR).

CMS is now preparing these TDRs for the four main detector upgrades presented in the TP: Tracker, Barrel Calorimeters, Endcap Calorimeters and Muon systems. These TDRs will be submitted to the LHCC and UCG in 2017. The Trigger and DAQ upgrades require a shorter production time, and the corresponding TDRs will be submitted at a later stage in 2019-2020, when projections for technology progress will be better known. Nevertheless, the cost estimates and the anticipated institute contributions for these projects will be updated at the time of the other TDR submissions. The upgrades to infrastructure and the logistics of work during Long Shutdown 3, including resources requested from CERN in its role as host Laboratory, will also be documented. With this plan, CMS is hoping to complete the information for resource agreements for the Phase II upgrade implementation by the end of 2017. The detailed plan of work in preparation of the TDRs and up to the delivery of the upgrades is currently being established. A preliminary description of the necessary R&D is documented in the TP and in a specific document provided to the RRB (CERN RRB-2015-062).

Most of this was described in our last report. However, with a change in CERN management in January of this year, and the first RRB under the new regime due to take place after this document is submitted, we await with interest the outcome of discussions at the RRB and indications from the funding agencies of how CMS should proceed. Of course, this applies very much to the UK as well, in times of economic uncertainty and difficulties in planning.

2.3 UK adaptation to CMS planning

As previously reported, a major question is planning of commitments and responsibilities for the Phase II upgrade, including especially an assessment of the resources likely to be available to sustain it. There has not been much recent progress on this, either in CMS or the UK, and we await guidance from the forthcoming RRB and feedback from STFC.

In the UK, we have held collaboration meetings to discuss our planning, but it is now difficult to firm things up more without STFC guidance about the likely budgets, the approval process and the timing of submissions for review by STFC.

However, one potentially significant input to our planning is a decision on the architecture on the L1 track-finding processing, where three alternatives, one of which is a UK time-multiplexed design, are under consideration and demonstrators are under construction. A proposal for how the decision process should take place has recently been drafted and partially endorsed.

In view of the TDR, due in June 2017, it was agreed in late 2014 that the three groups would build demonstrators based on existing hardware. The primary goal of such demonstrators is to provide evidence that L1 tracking will be feasible within the available latency, with at least one of the methods; this is a milestone for the TDR. The comparison of the features and performance of the three demonstrators should also provide essential information for specifying the final implementation in CMS. To that end, the demonstrator results will have to be presented and interpreted in the perspective of the final system framework.

A review committee composed of D. Abbaneo (chair), D. Acosta or C. Foudas, A. Marchioro, E. Perez, R. Van Berg (from ATLAS), F. Vasey will carry out two reviews, one in May, as a preliminary evaluation, and a second in December. After the December review, the committee will produce a concise report summarizing their findings and evaluation of the projects, along with considerations and recommendations on how to develop an optimal implementation in CMS.

The aspects to be evaluated should broadly cover:

- Final system description.
- Additional features, including performance, flexibility, and matching to the CMS trigger.
- Demonstrator results and interpretation.
- Cost and feasibility.

What is less clear and the subject of discussion is how the review committee recommendations translate into a decision, and which team(s) will construct the final system. This is a multidimensional problem with technical, financial and sociological aspects.

2.4 Other news

Although not directly relevant to the upgrade project this may be of interest. In December, CMS presented a large number of first searches for new physics in the 13 TeV data, with results including a small excess above background in the diphoton channel near a mass of 750 GeV. Since then, CMS has reanalysed the data using final calibrations obtained from the 2015 dataset, also including 0.6 fb^{-1} of additional data collected while the solenoid was switched off. With these improvements, the sensitivity of the diphoton search increased by 20% relative to the previous result. Combining results from Run I and II the local significance of this excess now stands at 3.4σ . While waiting for more data, CMS immediately intensified the search in related channels for potential signals in the same mass region. These include $Z\gamma$, WW , ZZ , and other final states. So far, no excesses are observed in other channels, but with a much larger dataset expected by summer these searches will continue to be of great interest.

3. Work Package 1: Management

A reminder of the project management is included below. G. Hall remains PI for this project. D. Newbold has been UK CMS PI since October 2015. Hall was asked to act as an advisor to the CMS spokesperson, so continues to attend CMS MBs until September 2016, when Tiziano Camporesi steps down.

Two new work packages are reported later: WP4, on the High Granularity (Endcap) Calorimeter project, and WP5 covers ongoing work on the L1 track-finder which focuses on a demonstrator for a CMS decision on the architecture at the end of 2016.

WP	Manager	Institute	Role
1	G Hall, PI	Imperial	Overall management, budgetary responsibility and supervising procurements, interface to CMS, to UK CMS PI. CMS Management Board member to Sep 2016 and Tracker Management Board member.
2	M Raymond	Imperial	Overall responsible for CBC specifications, interface to module design team, chip testing and module evaluation and CMS planning
	M Prydderch	RAL TD	Manager of ASIC design team in RAL
3	A Tapper	Imperial	Based in CERN with supervisory responsibilities for G. Iles, Imperial College engineer, also based in CERN. Currently project manager for the calorimeter part of the trigger upgrade.
	J Brooke	Bristol	Supervision of UK Phase I trigger upgrade activities, with A Tapper. Previously DPG convenor and software coordinator in the trigger project.
4	P Dauncey	Imperial	Jointly coordinating the UK HGC developments, with G Davies.
	G Davies	Imperial	Also, UK representative on the provisional HGC IB and FB.
5	M Pesaresi	Imperial	Coordinating demonstrator integration activities and hardware/firmware specifications, and general project planning.
	I Tomalin	RAL PPD	Maintaining and running the Monte Carlo analysis software, improving tracking algorithms based on offline experience and day-to-day oversight of RAL track trigger activities.

4. Work Package 2: Outer Tracker Readout

4.1 Objectives

- To complete the development of a readout and triggering chip suitable for the 2S-PT module, bringing the chip to a final state ready for mass production.
- To develop the hardware and software required for the large-scale production testing procedures, and to deliver tested wafers to the CMS experiment.
- To play a major role in construction, definition and evaluation of prototype modules.
- To contribute to development of ancillary chips required for the 2S-PT module, and to participate in the PS-PT module development.
- To contribute to the future large-scale module production programme, and to participate in integration and commissioning activities.

4.2 Progress

The front end chip development for the 2S modules continues with the CBC3 which will be the final CBC version, containing all functionality required to provide triggering information and capable of sustaining a triggered data readout of up to 1 MHz. We continue to support the test beam programme of prototype 2S modules read out by the CBC2, contributing in the areas of hardware, firmware, DAQ software and data analysis. The R&D progress of both 2S and PS systems is monitored through regular Outer Tracker Electronics systems meetings held every 6-8 weeks at CERN, ensuring compatibility between the common powering, data aggregation and off-module data transmission components, and module construction technologies.

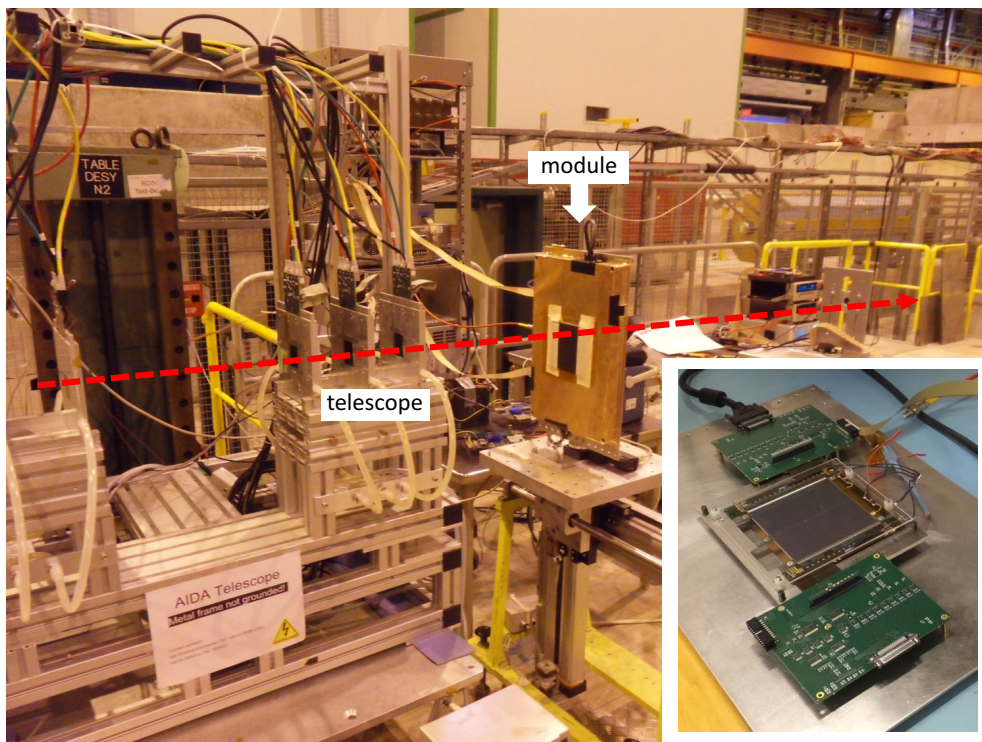


Figure 4.1: The full-size 2S-PT module situated in the H6 beam line at CERN, and inset the module can be seen mounted on its base-plate with interface cards.

Since the last report we have participated in a beam test of the full-size 2S module prototype at CERN. Figure 4.1 shows the 10 x 10 cm² sensors module with 4064 channels read out by 16 CBC2 chips on two 8CBC2flex hybrids and their associated interface cards, set up adjacent to the AIDA telescope in the H6 beam line. At the time of the last report the module had only just been assembled.

The module and its associated data acquisition system were successfully operated for a 12 day period, with high statistics runs for comparator threshold and module rotation scans. We provided effort during the test beam itself and are contributing to the data analysis. Apart from the usual silicon sensor module studies to verify the silicon strip sensor performance, on-going analyses include studies of stub finding efficiency comparing stub triggers generated by the CBC chips with reconstructed stubs from the triggered readout data.

The test beam programme will continue this year with a further test of an irradiated mini-module at CERN in May, which we will support and provide effort in the firmware and software areas.

The development of the front end hybrids for both 2S and PS outer tracker systems is the primary responsibility of CERN collaborators. The current full-size prototypes (8CBC2flex) were produced by AEMTEC, but alternative manufacturers are required, and a formal market survey is now complete with a total of 3 potential candidate companies identified. Further prototype procurements are planned to verify capabilities, and a call-for-tender specification is being prepared to specify the steps which must be followed to assess quality and costs prior to a decision on the future large scale procurement.

The CBC2 has been a success in progressing the R&D on hybrid technology suitable for construction of 2S (and PS) modules, and the CBC3 will be the final version, but there are also other developments required. A Concentrator ASIC (CIC) is needed to receive the trigger and data streams from CBC (and MPA) chips, processing and assembling data packets which are passed to the LP-GBT for off-module transmission. The CIC is a purely digital 65 nm CMOS ASIC under development by Université Claude Bernard (Lyon). We maintain contact with the CIC design team to ensure compatibility. First CIC prototypes are planned for the second half of this year. The LP-GBT is a CERN development which should be available on a similar timescale. The remaining major component required for the outer tracker modules is the power supply system which takes a single high voltage input to the module (~12V) and provides the low voltage rails using buck converter ASICs. The ASICs are a CERN responsibility and the development of the service hybrid on which they are mounted is being undertaken by RWTH Aachen. A complete prototype suitable for incorporation in a 2S module is also planned for the second half of this year.

As prototypes of all module components begin to come together a working group has been set up to develop plans for the large scale production period, looking at QA and testing procedures at the various stages of complete module, module sub-component and individual component levels.

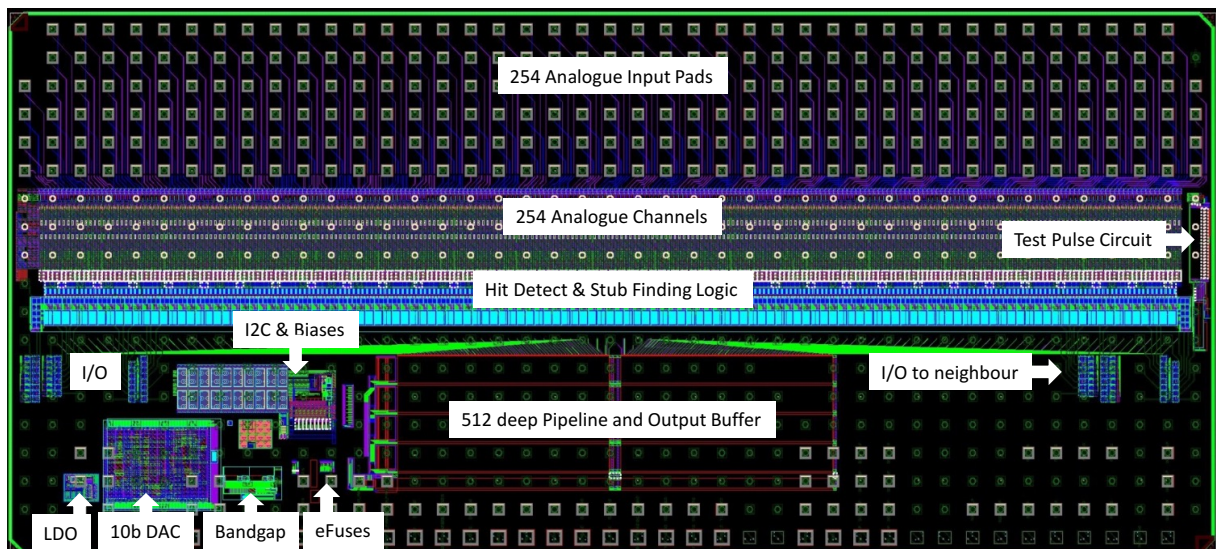


Figure 4.2: Layout of the new CBC3 chip with design blocks identified

Figure 4.2 shows the layout of the new CBC3 chip as it currently stands. All the major blocks are there, but their positions may change as the design is finalised.

At the time of the last report we were still hoping to be ready to submit the CBC3 for fabrication in February. Unfortunately at the end of 2015 a RAL TD engineer allocated to the project resigned at short notice. A detailed assessment of the remaining project tasks was carried out and it became clear that there were now more than had been originally planned. New features had been introduced recently such as the new bandgap circuit, and the use of e-fuses to trim the bandgap at wafer test time, and to define an individual chip identity. Also changes to the analogue front end layout and biasing were more than had been originally planned for. The plan was revised and the effort of two engineers (L. Jones and S. Bell) was found to bring the project to completion. Figure 4.2 shows the Gantt chart of the remaining work. While the individual circuitry block designs reach completion in April, the top level assembly work, which involves connecting blocks together to assemble the complete chip with all the associated detailed checking that is required, will not be finished until June. This is a four month delay compared to the previous schedule.

The new schedule in Figure 4.2 is currently on track, with weekly phone meetings held to monitor design progress. Our CMS collaborators are kept informed through the regular systems meetings. This is important as the plan is still to fabricate the CBC3 in a shared run with another chip developed by the CERN microelectronics group, and the project requiring that chip will be held up if the submission slips beyond the middle of the year. Close contact is maintained since one of the CERN engineers involved in the design of that chip, and also responsible for organizing manufacturing submissions, is also responsible for coordinating the design of the PS module readout chip and therefore attends the systems meetings.

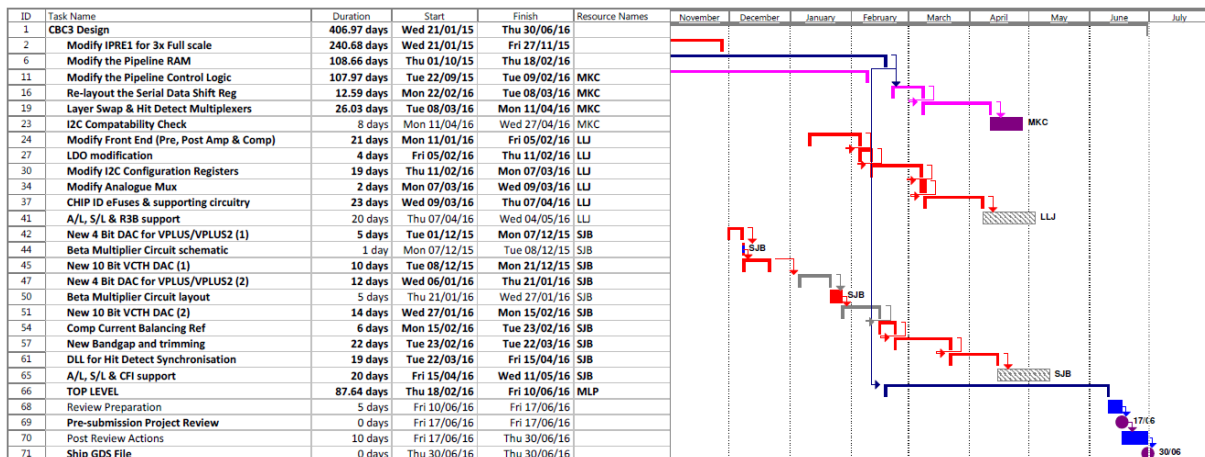


Figure 4.3. Gantt chart showing the CBC3 development plan through to completion.

FC7 developments

The FC7 (FMC carrier - Xilinx Series 7) AMC is based on the MP7 and CERN GLIB boards with the ability to host up to two FMC (FPGA Mezzanine Card) modules and support signalling rates up to 10Gbps. It is a flexible, general purpose card allowing it to be deployed across many applications in CMS and its development has been shared with engineers from CERN.

In our last report we described the solution to the difficulties we had experienced in operation which were traced to a minor error in the layout. The revised R2 design, which was manufactured using BBElectronics (Denmark) for assembly and PCBs by SOMACIS (Italy), has proven to be very successful with a high yield of good quality boards. The R2s were delivered on schedule in December, with 62 out of 65 working boards.

Some of them have also been subjected to accelerated lifetime testing, with no failures observed, and hence the R2 version of the FC7 is now the baseline design, and will be used in several CMS projects, including the Phase I pixel upgrade, the DAQ for the outer tracker module beam tests, and other projects. (The UK is not responsible for support, except for projects in which we have a direct interest.)

The numbers in use are growing fast, potentially limited by the allowed size of CERN orders without a full tender and Finance Committee approval: 185 in production (currently undergoing acceptance testing), 200 on order (July 2016). Among the major users, the CMS TCDS (Timing Control and Distribution System) is replacing their system with R2s (120 including spares), Pixels require 170 (including the forward proton spectrometer), HCAL request 25, GEM readout for the muon system expect to use 70 .

It may be worth noting that, with the experience in this R&D projects of the MP7, FC7 and other boards, we have gained a great deal of valuable first-hand experience of board manufacturing processes and potential problems, as well as procurement issues, and we should be well capable of embarking on large volume production of complex hardware, e.g. for the Phase II Tracker, HGC or future L1 trigger electronics. In addition, other projects have been able to benefit from our common developments; e.g. we have provided 15-20 boards for UK contributors to the g-2 experiment at FNAL, and about 10 for COMET.

4.3 Deliverables

The WBS for WP2 is included below. The items in red are those which will be delayed as a result of the CBC3 submission delay discussed above.

WBS	WBS L2	Start	Finish	Months	Task Description
2	Phase II tracker Readout	04/13	03/19	72	
2.1	system	04/13	03/14	12	definition of the CBC-based SS-Pt module readout
	2.1.1 specification definition	04/13	03/14	12	regular meetings with CMS collaborators to define overall system specification and interfaces
2.2	CBC2 test	04/13	03/15	24	CBC2 is final deliverable of the UK upgrade R&D
	2.2.1 CBC2 on-going testing	04/13	03/14	12	complete the detailed studies of the CBC2 chip, including irradiation and SEU tests
	2.2.2 CBC2 2S-Pt module prototype studies	04/13	03/15	24	a programme of SS-Pt module studies, in collaboration with CMS, including test beam
2.3	CBC3	04/14	03/16	24	CBC3 is specified for the final system
	2.3.1 CBC3 design	04/14	09/15	18	design period
	2.3.2 CBC3 production	09/15	03/16	6	production period
	2.3.3 test setup preparation	09/15	03/16	6	wafer and chip test setup preparation
2.4	CBC3 test	03/16	03/18	24	CBC3 chip and module testing
	2.4.1 early tests	03/16	09/16	6	chip verification tests to prior to module tests
	2.4.2 on-going testing	09/16	03/17	6	complete characterization, including irradiation and SEU tests
	2.4.3 CBC3 2S-Pt module studies	09/16	03/18	18	CBC3 based module studies in collaboration with CMS in lab and test beam
2.5	CBC4 design and test	09/16	12/17	15	CBC4 is the final version of the chip, fixing any remaining bugs found in the CBC3
	2.5.1 CBC4 design	09/16	12/16	3	design period
	2.5.2 CBC4 production	01/17	06/17	6	production period
	2.5.3 testing	07/17	12/17	6	tests to verify full and final functionality
2.6	CBC4 mass production preparations	01/18	12/18	12	a full wafer engineering run is required for CBC4 in preparation for mass production
	2.6.1 CBC4 final masks	12/18	03/18	3	mask preparation for full wafer engineering run
	2.6.2 CBC4 engineering run	03/18	09/18	6	production period
	2.6.3 CBC4 final production readiness verification tests	09/18	12/18	3	final functionality check
	2.6.4 procurement planning	01/18	12/18	12	detailed financial plans for mass production

Clearly there will be a knock-on delay affecting subsequent tasks, but there is still some contingency in the schedule since, depending on the success of the CBC3, the CBC4 iteration may not be needed or any necessary changes may be minor. As far as CBC3 based prototype module construction is concerned we are still reasonably well aligned with our collaborators developing the other module components.

4.4 Staff on project

The changes to the RAL TD staff on the project are described above in the progress report.

One post affected by the CG award was J. Fulcher, from Imperial College, the online DAQ expert dedicated to the maintenance and operation of the Tracker FEDs and online software, and who was 50% funded by this project. He resigned from Imperial in July 2015 to take up a CERN staff position.

Continuation of the 50% upgrade funding was given in a new STFC grant issued at the end of 2015 and an appointment process began in January. This has recently been concluded, with an offer accepted for a start date in September 2016 (G. Auzinger, currently a CERN Fellow). We were asked in the last OSC to comment on the activities proposed for the post. As hoped, we have recruited an individual who has expertise in tracker online software, particularly with respect to use of the FC7 (currently in the pixel upgrade project) and in support of upgrade module development activities and characterisation. We can therefore be confident that he has the profile to quickly adapt to our current activities in future 2S-module evaluations in test beams and laboratory tests, including irradiations, and to begin to develop a new data acquisition system for this purpose based on the FC7 (instead of the GLIB which has been used to date). This should begin to define the foundations for the future tracker data acquisition system and the interface to the track-finder where we also hope to have a substantial role in future.

4.5 Expenditure

The main expenditure continues to be on RAL TD staff. The submission should be in mid-2016, and most of the manufacturing cost should be invoiced by CERN in this financial year.

5. Work Package 3: Level-1 Trigger

5.1 Objectives

- Improvement of the current CMS calorimeter trigger in preparation for above-design-luminosity conditions.
- Provision of infrastructure to allow testing of an entirely new calorimeter trigger in parallel with the existing system.
- Design, construction and testing of a time-multiplexed hardware trigger for CMS, capable of implementing new and more selective algorithms.
- Design of a track trigger architecture for HL-LHC running, and construction of a technology demonstrator.

5.2 Progress to date

The Stage 1 calorimeter trigger for 2015 ran reliably, selecting physics events for CMS in proton-proton and heavy ion collisions, requiring very little support from UK personnel.

Since the last review commissioning of the trigger for 2016 has progressed very successfully. After taking data parasitically during the end of the 2015 run the upgraded trigger is now the primary trigger for CMS.

A programme of bi-weekly cosmic-muon runs was established by CMS and the trigger was included in all runs. More recently beam “splashes” and first collisions in 2016 have occurred and are being used to study performance. Figure 5.1 shows the online data monitoring for one such run.

All the electronics necessary for the UK contribution to the CMS trigger system, including spares, were installed and successfully commissioned before the last review. However, a number of extra MP7 boards were ordered for the muon and global trigger projects. Procurement and testing of the additional MP7s has now been successfully completed. A full summary of the MP7 production will be provided for the next review.

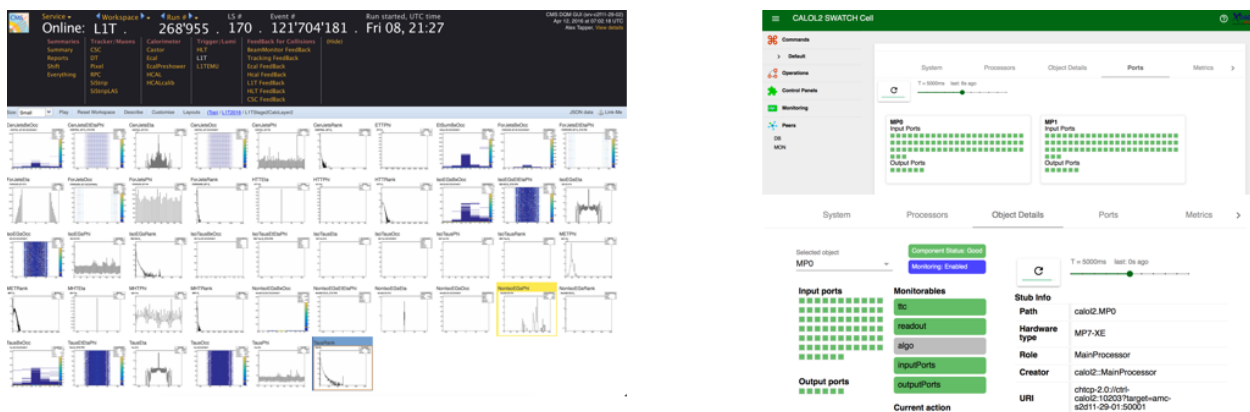


Figure 5.1: Screenshots from (left) online data monitoring for the first LHC collision run of 2016, showing data from the output of all calorimeter trigger algorithms, and (right) the online control system for the trigger electronics.

Final preparations for the 2016 run are now the main activity. These include preparing calibrations and tuning parameters for the expected performance of the LHC in 2016 and work on data quality monitoring.

At the time of the last review we reported a lack of manpower generally in the area of online software which had led to delays. The UK had already acted to strengthen this area, and since then other groups have also done so. The excellent design of the software control system, led by the UK, has allowed new manpower to be integrated efficiently, resulting in fast progress. Almost all the

online software functionality required for the 2016 run is now available and commissioned. There are some outstanding items, such as database integration, which are expected to be completed in time for the start of the run. Figure 5.1 shows a screenshot of the online software control system.

Looking towards the future, work has continued on the successor to the MP7 based on the Xilinx Ultrascale FPGA series and described in detail at the time of the last review. A final design review caught a potential problem with the design which has been corrected and an order for a small number of prototype boards has been placed. The first prototypes are expected to be delivered towards the end of May.

5.3 Overview of CMS plans

The CMS Level-1 Trigger project has formed a new working group to plan the trigger upgrade for Phase II. J. Brooke (Bristol) and R. Cavanaugh (UIC/FNAL) have been appointed to lead the group, which will have responsibility for performance studies, development of conceptual design, and the R&D necessary for an upgrade to the Level-1 Trigger system to operate in the HL-LHC era. This includes the integration of calorimeter and muon trigger data with Level-1 tracks delivered by the tracker. The outcome is ultimately to be documented in a Technical Design Report scheduled for completion in 2020.

5.4 Staff on project

No changes.

5.5 Expenditure

Overall spending is within the budget foreseen.

5.6 Deliverables

The deliverable list is appended below. Blue font means complete. Red font is delayed. PM represents duration of the task.

L1	L2	Start	Finish	PM	Task description
3.1	Stage-1 calorimeter trigger upgrade				
	3.1.1 Hardware development		07/13	6	Finalisation of production hardware module (48-link version)
	3.1.2 Procurement and testing	07/13	10/13	3	Procurement, production and acceptance tests of hardware
	3.1.3 μ TCA infrastructure		07/13	6	Completion of baseline IPbus / uHAL
	3.1.4 Online software development	04/13	10/13	6	Development of system-specific and trigger-wide online software (control, monitoring, DAQ)
	3.1.5 Algorithms and offline software	04/13	04/14	12	Development of stage-1 algorithms and corresponding emulator and DQM software
	3.1.6 Integration	07/13	01/14	6	Integration tests with other trigger components, DAQ, TTC
	3.1.7 Commissioning	09/14	03/15	6	Commissioning with cosmics and beam
	3.1.8 Support	03/15	01/16	9	Ongoing expert support and optimisation of Stage-1 system
3.2	Stage-2 calorimeter trigger (TMT) upgrade				
	3.2.1 Hardware development	10/13	04/14	6	Development and finalisation of production hardware module (72-link version)
	3.2.2 Procurement and testing	04/14	10/14	6	Procurement, production and acceptance tests of hardware
	3.2.3 Online software development	10/13	04/14	6	Development of system-specific and trigger-wide online software (control, monitoring, DAQ)
	3.2.4 Algorithms and offline software	04/14	04/15	12	Development of stage-2 algorithms and corresponding emulator and DQM software
	3.2.5 Integration	04/14	10/14	6	Integration tests with other trigger components, DAQ, TTC
	3.2.6 Commissioning	04/15	04/16	12	Commissioning with cosmics and beam
	3.2.7 Support	04/16	04/19	36	Ongoing expert support and optimisation of

					stage-2 system
3.3	Post-LS3 trigger R&D				
3.3.1	Design studies	04/13	10/14	18	Simulation studies of track trigger performance, and decision on final concept
3.3.2	Dataflow design	10/14	10/15	12	Detailed simulation, architecture design and technology choices for track trigger
3.3.3	Hardware development	04/16	10/17	18	Development of next-generation hardware modules for integrated L1 trigger
3.3.4	Algorithms and offline software	10/15	04/17	18	Development of algorithms and firmware for integrated L1 trigger
3.3.5	Integration and demonstration	10/17	10/18	12	Hardware slice test of integrated L1 trigger
3.3.6	Final system design	10/18	04/19	6	Production planning for final version of integrated L1 trigger

The status of the milestones which have changed or are late is given below in a little more detail:

- 3.2.3 As reported last time, online software development has been delayed but is now essentially complete. This is not only quite a substantial achievement, to have developed a new integrated online system under great pressure, but one where the UK team has played the very leading role.
- 3.2.6 Commissioning with cosmic-ray muon events is complete and commissioning with beam is underway. The upgraded time-multiplexed trigger is essentially complete and will be used for 2016 data taking.
- 3.3.1/3.3.2 These milestones are superseded by those proposed in Work Package 5.
- The other milestones listed are likely to evolve as CMS plans for the Phase II trigger become clearer.

6. Work Package 4: High Granularity Calorimeter

As introduced at the last meeting the HGC project was only recently approved by CMS. The UK was instrumental in establishing the project, and that leadership is visible in the organisation chart shown in the last OSC meeting report. Within the UK, we have chosen to focus on key aspects of the project, namely the front-end electronics, the trigger and the simulation performance studies, all of which are highly synergetic with the UK's existing leading roles in the CMS upgrade. To address these we have been successful in attracting STFC PRD and ERC funds to significantly boost the limited CG funded effort available. We had a significant input to the definition of the overall HGC milestones leading to the TDR, some of which are discussed in Section 6.6 later. A full matrix of those groups contributing to these global milestones is under development.

6.1 Objectives

- To play a leading role in producing the HGC TDR at the end of 2017, both in terms of overall project management and technical aspects in the key areas listed below.
- To contribute to the design and testing of the front-end electronics ASIC for the HGC in collaboration with the Omega/EP group in Paris.
- To develop the trigger primitive generator (TPG) and back-end readout electronics system, including algorithms, firmware and common hardware.
- To study the physics performance of the HGC and optimise the design parameters and in addition develop the reconstruction techniques to provide the best overall performance.

6.2 Progress to date

The HGC L1 Project Manager, T. Virdee, is from the UK, as are two of the L2 subproject coordinators. As such, we played a major role in producing the results for, and the writing of, the Technical Proposal in 2015. We expect to do the same for the TDR, which is due in November 2017.

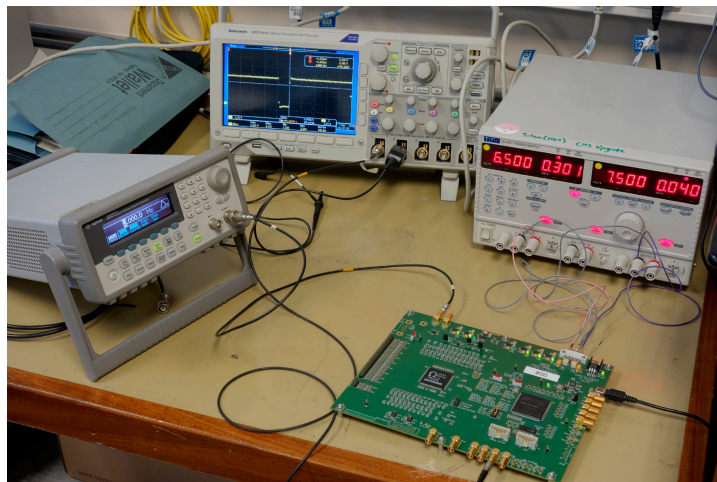


Figure 6.1. The test system in use at Imperial College for testing the Omega SPIROC chip. The ASIC under test is the one on the left of the PCB in the foreground.

Work on the front-end electronics design is new activity for the UK-HGC project. This has been started with the hiring earlier this year of a new analogue electronic engineer, Dr Johan Borg, at Imperial on the ERC Advanced grant. He has had several meetings with the Omega group who have led the front-end ASIC design so far. The V1 prototype of a chip, which could in principle be used for the HGC, is scheduled for submission in March 2017. This will be produced in the TSMC foundry 130 nm process. Before this, there will be two fabrications of test structures of components relevant to the ASIC in the same process. The new engineer has started by testing an existing design (arising from ILC activities) from the Omega group which has a similar architecture to the HGC chip (Figure 6.1) He will then contribute to the design of the test structures for the second fabrication round, which will

be submitted in September this year, and then also to the design of the V1 ASIC. Given the UK interests in the HGC trigger (see below), it is likely his contribution will be to design the part of the circuit which produces the TPG inputs.

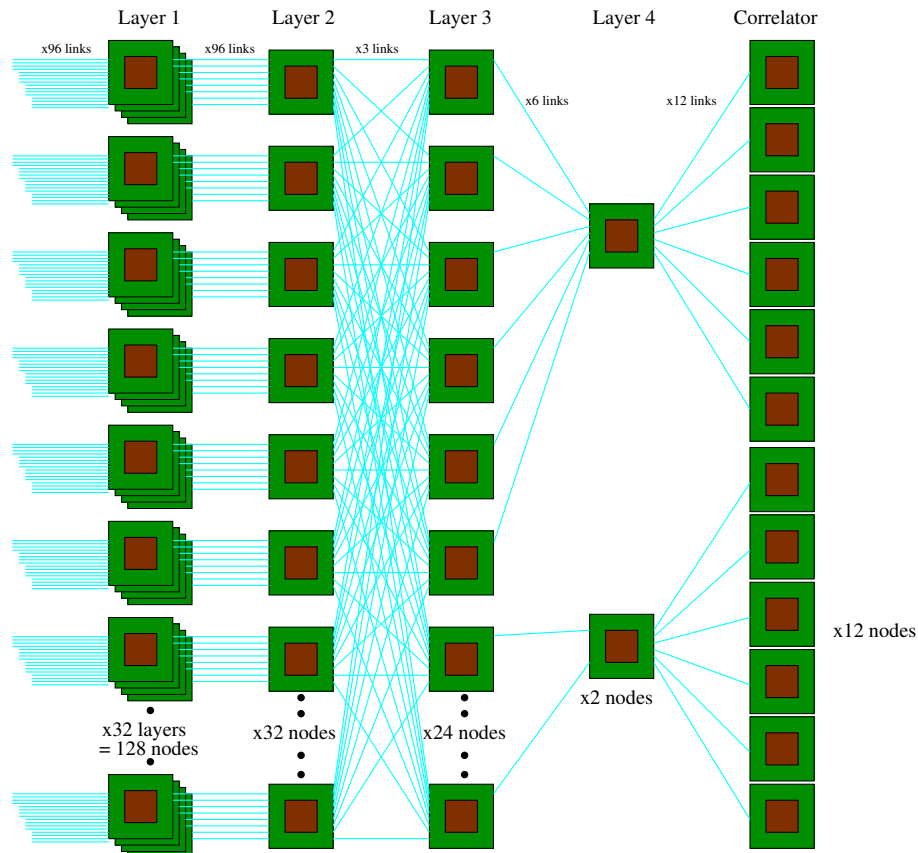


Figure 6.2 Possible architecture for the HGC trigger primitive generator. This is constructed from multiple copies of a common hardware board (the green boxes). All interconnects are via fibre optic links (blue lines). This architecture takes raw digital readout from trigger cells on detector and calculates clusters reconstructed in 3D for use in the central L1 Trigger.

The HGC TPG group is co-led by P. Dauncey. We have been working in this area for around a year. The main issues are currently understanding the algorithms which will be needed and studying architectures which would enable those algorithms to be implemented. The UK architecture concept is based on a high-throughput common hardware board, similar to the existing MP7 (Figure 6.2). It is foreseen that this board would be used by other systems in CMS; of particular relevance for the UK would be its use in the Level 1 Trigger and Tracker readout. Hence, we would be leading and defining a major part of the upgrade readout. The scope of the TPG in terms of board numbers, links, data flow, cost, etc., have been estimated based on several assumptions on the performance of the common hardware board. The numbers also depend on the design of the central L1 Trigger design and so the UK can exploit the common interests here to optimize both systems. Studies of TPG algorithms have first required the implementation of the complex HGC hexagonal cell and wafer geometry into the CMSSW simulation and we have contributed significantly to this technical effort. The first results from the new simulation are just becoming available, with a study of the pile-up correction of trigger objects having been done in the UK in March this year.

The HGC simulations and performance group for the TDR in November 2017 is co-led by C. Seez (Imperial, based in CERN). Our effort in this area has been mainly concentrating on the implementation and verification of the hexagonal geometry as mentioned above. However, performance studies (e.g. Figure 6.3) have been ongoing in the UK too. These include examining the effects of aligned and non-aligned cracks in the endcap mechanical structure) This demonstrated that

there are significant gains in resolution if the cracks are not aligned and has motivated a new concept for the endcap assembly.

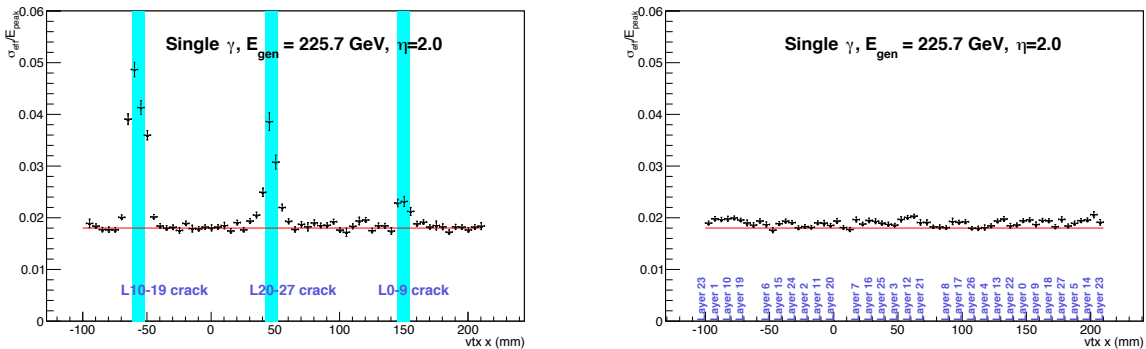


Figure 6.3. Effect on energy resolution of mechanical gaps as a function of ϕ if the gaps in layers are aligned (left) and non-aligned (right). The blue shaded areas show the positions of the gaps in the first case.

6.3 Overview of CMS plans

The preparation of the TDR is foreseen in the CMS upgrade planning. The evolution of those plans probably depends on the outcome of the next RRB in April 2016 (next week, at the time of writing) and the plans of the new CERN management for the LHC upgrades.

6.4 Staff on project

We have almost all the funded personnel now in post. This effort comes from the Imperial Consolidated Grant, an STFC PRD grant, and an ERC Advanced grant awarded to T. Virdee. The PRD grant is for two years and started in July 2015 while the ERC grant is for five years and started in October 2015.

The front-end effort is supported by an analogue electronics engineer (Borg), and the TPG effort by a digital electronics engineer (Palladino), both funded from the ERC grant. They both started earlier this year and are currently funded for four years. There are CG personnel involved in the TPG studies (Rose) and simulation studies (Magan, Seez and Zenz) as well as the academics (Dauncey, Davies and Virdee). A two-year RA position (Mastrolorenzo) funded by the STFC PRD grant contributes to both trigger and simulation work; he started in October 2015. We do not currently have any PG students working in this area.

The ERC grant has sufficient funds for a PG student and/or RA position; we are holding this in reserve for now, although it is likely to be most useful to extend Mastrolorenzo's position for up to another two years.

The management of the UK project part of the project is being overseen jointly by P. Dauncey and G. Davies, with Davies primarily focusing on front-end studies, and Dauncey responsible for the trigger-related studies. As described above C. Seez is steering simulation work.

6.5 Expenditure

Expenditure so far has been almost entirely on staff, and on travel to a lesser extent. We do not foresee significant equipment expenditure for some time in the projects with UK involvement. The ASIC fabrication will be funded by the French groups and for the trigger, the first prototype of a common hardware board is not expected to be produced until the end of 2018.

6.6 Deliverables

HGC milestones were defined from October 2015 onwards and hence have only been active for the last seven months. The major milestone to which we have made a significant contribution has been implementing the new geometry in the simulation, which is now completed. Upcoming milestones relevant to the UK effort over the next year are:

25 April 2016

- Submission of the front-end ASIC test structures in March and September 2016 and the V1 ASIC submission in March 2017.
- Preliminary definitions of the TPG raw data inputs, the primitive production algorithms and the output primitive definitions in June 2016 and preliminary results on the TPG performance in December 2016.
- Large scale production of fully simulated and reconstructed HGC events for physics and trigger studies in April 2016. This has not yet been achieved at the time of writing.

7. Work Package 5: L1 track finder

7.1 Objectives

- To design the architecture and technological implementation of a first-level track finder for the CMS Phase-II upgrade.
- To demonstrate and document a prototype track-finding system, as required for CMS review purposes, design reports, and integration exercises.
- To generate a construction plan for the CMS track finder and readout system, including any R&D required for final implementation decisions.

7.2 Progress to date

The UK has previously presented to the OSC a concept for a Level 1 track finder for Phase II, based on a time-multiplexed architecture. The demonstrator system we propose is based on a small number of MP7 boards and must be able to transfer Monte Carlo generated trigger primitives (high transverse momentum hit candidates, or stubs, eventually provided by the Phase II tracker) through a set of processor cards to generate fitted L1 tracks for a time slice of the full system. The demonstrator slice will also be regional, but should be able to process data from any region of the tracker transparently.

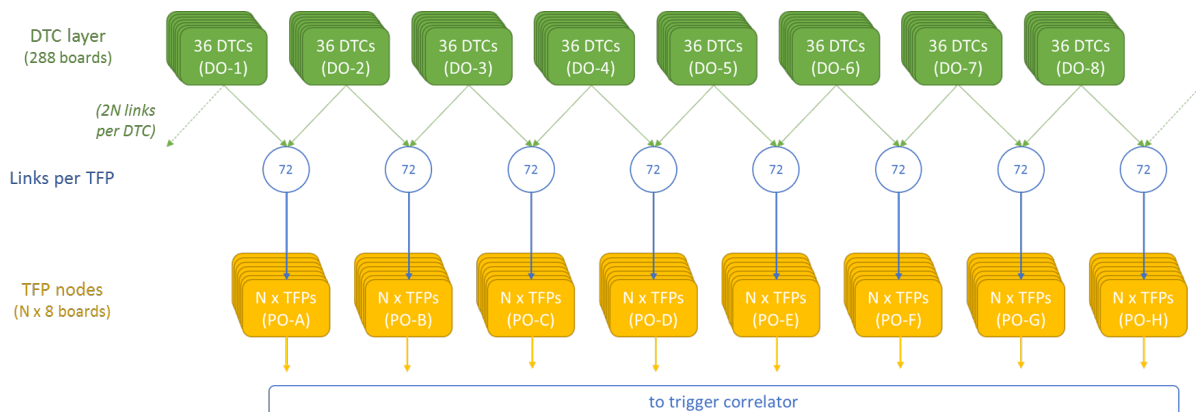


Figure 7.1: Updated architecture for the time-multiplexed track finder following division of tracker readout into ϕ octants. N is the scalable time-multiplexed period which itself is a function of link bandwidth. In a final system 25Gbps links could mean $N=12$ BX, whereas for a 10Gbps demonstrator, $N=36$ BX.

In recent months the tracker community has converged on a draft specification for the hardware layer that is to immediately process the data coming off-detector (as well as control the detector modules themselves). This Data, Trigger and Control (DTC) board forms the interface between the Phase II tracker and the track finding layer that we are demonstrating and now allows us to realistically map our system to a physical detector space. It is proposed the tracker will be cabled into ϕ octants so as a result we have also oriented our track finding regions into ϕ octants - emphasising the flexibility of our architecture (Figure 7.1). The architectural features remain the same (in fact, the symmetry in ϕ helps simplify the system): no data sharing between octants is required as this is handled by duplication which is made possible within the DTCs; data is processed independently within each region; data are time-multiplexed within each region with a single event being streamed into each Track Finder Processor (TFP), 1 optical link per DTC. (It is worth noting that this L1 track-finder demonstrator has the same basic concept as the HGC trigger discussed in Section 6.2, and so this work will help clarify issues for WP4 too.)

Figure 7.2 indicates how we are demonstrating a realistic slice of the final system. The duplicated data from two neighbouring detector octants (36 DTCs each) is time-multiplexed into a TFP. Two MP7s satisfy the role of the two detector octants, each implementing 36 virtual DTC

instances. One MP7 plays the role of a Sink (i.e. a downstream trigger) board. The system demonstrates one time slice and one processing octant.

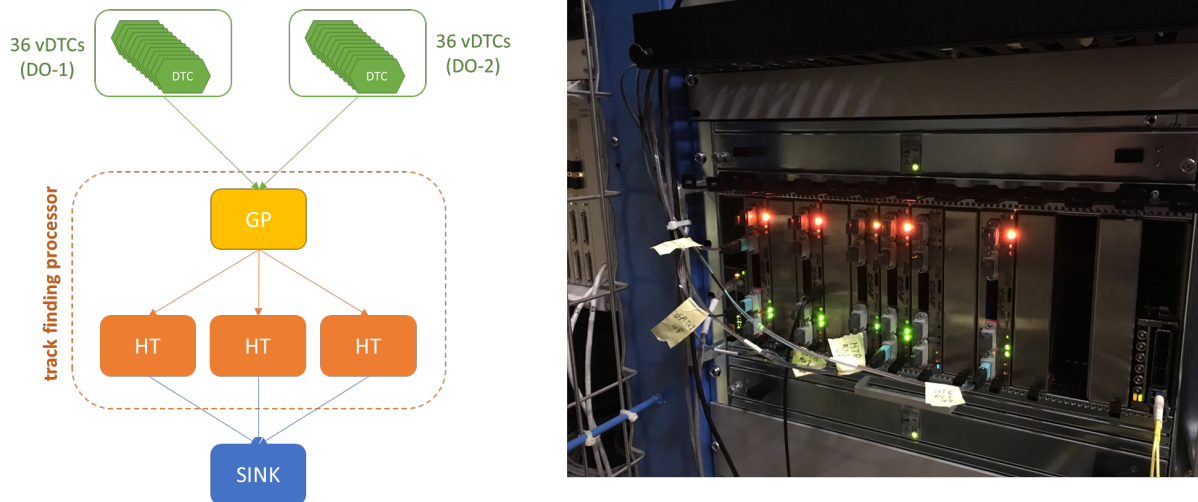


Figure 7.2: Demonstrator architecture (single octant, single time slice) using multiple daisy-chained MP7s fulfilling logically different operations (left). Physical demonstrator running at CERN (right).

The TFP receives an eighth of the stub data from the tracker over a 36 BX time-multiplexed period. By separating functionality into multiple hardware layers (MP7s), we are able to test the logical elements of the full track finding processor either independently in isolation, or in a full chain demonstrator with daisy-chained MP7s. The present CERN demonstrator (Figure 7.2), comprising 7 MP7s, includes the following elements:

- 2 DTC Detector Octants – buffers containing pre-formatted data as if it were coming from 36 independent DTC sources.
- 1 Geometric Processor – a logical element designed to assign stubs to regional segments in ϕ and η , and arrange them onto specific links.
- 3 Hough Transform Processors – each board implements 12 regional Hough Transform segments, carrying out track finding in the r - ϕ plane and grouping stubs into track candidates with a given ϕ_0 and p_T .
- 1 Sink Board – buffers track candidates from the HT track finder into a single board, for easy extraction and measurement of latency.

These logical elements have been developed separately but in parallel over the last several months. The Hough Transform Processor algorithm has been the focus of our track finding efforts to date. The majority of the testing of this component has taken place in the RAL demonstrator test stand and there are in fact multiple implementations of the firmware we wish to test in the full chain system. The aim over the next month is to continue to integrate these elements together – not only to demonstrate our progress to CMS, highlighting measurements such as the latency, track finding performance and comparisons with emulator software; but also to provide a stable working platform into which the equally important downstream processors can be included. There is sufficient hardware and infrastructure in the CERN demonstrator rack to be able to add these hardware layers as they become available.

In parallel with the demonstrator work outlined here, rapid progress has been made in defining the processing algorithms that follow the Hough Transform track finder:

- duplicate removal – the candidates from the Hough Transform tend to be duplicated across neighbouring cells, sometimes only differing by one stub; a duplicate removal algorithm is being tested in software to reduce this unnecessary additional rate.

- seed filter – seed pairs consistent with the interaction region are formed within track candidates, followed by a filtering stage in the r-z plane to ensure there are sufficient stubs across layers that are consistent with the seed projection; simulation results appear to show reasonable performance and firmware development has started.
- track fitting – a fit is applied to the remaining candidates to refine the 4 track parameters and possibly reject badly fitting stubs either using a global χ^2 or a combinatorial Kalman filter; the results from these fitting algorithms are being scrutinised and firmware development will begin soon.

Work will continue to accelerate in this area until the next period of integration in Q3 2016.

The reorganisation of the CMS L1 Track Finder Working Group was discussed in our previous report to the OSC. Since then the goals of the working group and demonstrator specifications have been better defined with input from each of the three approaches. Additionally, CMS tracker management are defining the review procedure that will take place this year.

Work on the track finder simulations and firmware development has been undertaken in collaboration with individuals from CERN, Vienna and Karlsruhe.

7.3 Overview of CMS plans

The decision on the preferred L1 track-finding architecture, alluded to in Section 2.3, will be taken at the end of 2016, and have a major influence on the future direction of UK work.

Further development and the subsequent construction of the selected design is a substantial task, which will require discussion and negotiations among the teams who wish to participate in the project following the decision, and a reassessment of UK resources in the context of the full range of Phase II upgrade activities and STFC future planning guidelines.

7.4 Staff on project

A number of people are presently working on the demonstrator, in many cases practically full time, with several others providing expert support as required; their names are listed below. As WP3 work on commissioning the 2016 trigger draws to a close, this will enable additional experts to participate in the L1 track-finding R&D.

- RAL:
 - L. Calligaris (post-doc) – emulator framework development, software and analysis
 - D. Cieri (student) – demonstrator software framework and algorithm development
 - K. Harder (physicist) – demonstrator software and integration (just returned from extended leave)
 - K. Manolopoulos (engineer) – firmware developer and tester
 - T. Schuh (student) – firmware developer and algorithm development
 - I. Tomalin – WP co-manager, and simulations and performance studies
- Bristol:
 - F. Ball (student) – firmware developer and algorithm development
 - E. Clement (student) – Monte Carlo analysis and track finder tools
 - S. Paramesvaran (post-doc) – demonstrator integration and system support
- Imperial:
 - G. Iles (engineer) – firmware developer and coordinator
 - T. James (student) – demonstrator integration, algorithm development and analysis
 - M. Pesaresi – WP co-manager, and demonstrator hardware and architecture
 - S. Summers (student) – firmware developer and algorithm development
- Brunel:
 - A. Morton (student) – software and algorithm development

I. Reid (staff) – software and algorithm development

- Additional earlier contributors:

P. Vichoudis (CERN), K. Uchida (Imperial), T. Matsushita (Vienna), A. Shtipliyski (Imperial)

- Managerial and technical support:

J. Brooke (Bristol), A. Bundock (Imperial), G. Hall (Imperial), P. Hobson (Brunel), D. Newbold (Bristol/RAL), A. Rose (Imperial), C. Shepherd (RAL), A. Tapper (Imperial), A. Thea (RAL).

7.5 Expenditure

Currently only modest expenditure has been required since the prototyping uses spare MP7s from the L1 trigger project and WP3, and related equipment. Some travel expenditure has been incurred on meetings in CERN and the UK.

7.6 Deliverables

The deliverable list is appended below covering the UK prototyping work until the end of 2016, when CMS takes a decision on the preferred architecture. The milestones listed are CMS Tracker milestones for this part of the upgrade project.

WBS	L2	Start	Finish	PM	Task Description
5.1	Algorithm Development				
	5.1.1	01/15	03/16	14	simple DTC, GP & r-phi HT basic algorithms and specifications for running Demonstrator I
	5.1.2	04/16	07/16	3	full DTC, GP & r-phi HT advanced algorithms and specifications required for Demonstrator II, including DTC demo (if required), HT duplicate removal and dealing with hot events
	5.1.3	02/16	07/16	5	r-z filter development simulations, specifications and requirements for using z information to reduce the fake rate in Demonstrator II
	5.1.4	02/16	07/16	5	track fit development simulations, specifications and requirements for using fitting algorithms in Demonstrator II
5.2	Software Framework & Analysis				
	5.2.1	12/14	12/16	24	MC software package development analysis software framework, sample management and algorithm development support
	5.2.2	03/16	06/16	3	sync exercise analysis generation of results using official software tools and samples, in combination with project framework
	5.2.3	09/15	09/16	12	demonstrator software development pattern writers/unpackers, online software, & software supporting demonstrator integration
	5.2.4	09/15	12/16	15	emulator software development emulator framework and software for each algorithm block
	5.2.5	05/16	12/16	7	demonstrator analysis running of sample data through demonstrators, collection of output and matching with emulators
5.3	Firmware Development				
	5.3.1	06/15	03/16	9	basic r-phi HT development, testing and debugging of main track finding element for Demonstrator I
	5.3.2	01/16	04/16	3	simple DTC & GP development, testing and debugging of data formatting stages for Demonstrator I
	5.3.3	05/16	09/16	4	advanced r-phi HT development, testing and debugging of advanced HT algorithm f/w for Demonstrator II

5.3.4	full DTC & GP	05/16	09/16	4	development, testing and debugging of full/final data formatting f/w for Demonstrator II
5.3.5	r-z filter	04/16	09/16	5	development, testing and debugging of z algorithm f/w for Demonstrator II
5.3.6	track fit/filter	04/16	09/16	5	development, testing and debugging of track fit f/w for Demonstrator II
5.4	Demonstrators				
5.4.1	r-phi demonstrator validation	01/16	04/16	3	testing with emulator & comparisons, f/w optimisation and debugging
5.4.2	demonstrator I definition	02/16	04/16	2	definition of initial full chain demonstrator
5.4.3	demonstrator I integration	04/16	05/16	1	construction, integration, debugging and validation of initial full chain demonstrator
5.4.4	demonstrator I data acquisition	05/16	05/16	0.5	run data samples through demonstrator
5.4.5	demonstrator II definition	07/16	09/16	2	definition of final full chain demonstrator
5.4.6	demonstrator II integration	09/16	11/16	2	construction, integration, debugging and validation of final full chain demonstrator
5.4.7	demonstrator II data acquisition	11/16	11/16	0.5	run data samples through full demonstrator
5.4.8	demonstrator note	09/16	12/16	3	documentation on hardware, simulations, results, scalability and final system cost

Milestone Date	Description
16Q4	presentation of demonstrator at CMS internal review
17Q2	documentation of track finder design as part of tracker TDR
17Q4	freezing of technical track finder design choices, including technology roadmap

8 Risk register

The risk register has not been reviewed recently, because the Phase 1 L1 trigger has now converged and MP7 production successfully completed. Hence most of the risks are no longer relevant. The FC7 production has now also been successfully completed, so the main remaining project risks concern the CBC development. New risks will arise for the new WPs but we are not yet ready to define them in detail; in particular WP5 has less than a year before a decision on the track-finding architecture is to be made when the future commitments from the UK to the upgrades can then be made more firm.

9 Finances

Expenditure is reported in the usual financial table.

The travel expenditure is close to the estimate for this year with additional LTAs in place. The Imperial equipment expenditure is dominated by MP7 and FC7 production. Consumables expenditure is relatively low, partly because of a credit from FC7s explained previously but also because much recent expenditure has been in CERN for items classified as equipment; this is expected to change in future as new boards are developed.

CBC3 manufacture is now foreseen for June 2016, and is still expected to be part of a MPW run. However, the actual cost of the run will depend on the sharing, which is not yet easy to define, as it depends on the size of the ASICs and how many can be optimally placed in the reticle.

The system of purchasing via CERN and invoicing Imperial College, with the aid of the CMS resource management team and a dedicated account in CERN, continues to work well.

Use of engineering design effort in RAL TD is running at about the level anticipated.

10 Gantt charts

The Gantt charts for WP2 and WP3 activities have not changed since the last report. Gantt charts exist for the HGC project and there is a plan for the L1 track-finder, as shown above.

11 Milestones

The deliverables from each work package are listed below. The milestones which were due have been highlighted in red font, or those met in blue. The column of revised milestone dates been for the CBC schedule, but only with provisional estimates.

Deliverable	Date	Description	Rev.Date
M2.1	PM12	System specification document produced	PM12
M2.2.1	PM12	Documented CBC2 detailed test results	PM12
M2.2.2	PM24	Documented 2S-PT module results	PM24
M2.3.1	PM12	CBC3 ready for production	PM39
M2.3.2	PM18	CBC3 produced & test setups ready	PM42
M2.4.1	PM24	Documented early CBC3 test results	PM45
M2.4.2	PM30	Documented CBC3 detailed test results	PM48
M2.4.3	PM60	Documented CBC3 2S-PT module results	PM60
M2.5.1	PM42	CBC4 ready for production	PM54
M2.5.2	PM48	CBC4 produced	PM57
M2.5.3	PM54	Documented CBC4 test results	PM60
M2.6.1	PM60	Final production masks prepared	PM64
M2.6.3	PM69	CBC4 ready for mass production	PM69
M2.7.3	PM72	First production modules available	PM72
M3.1	PM9	Stage-1 calorimeter trigger hardware tested and installed	PM21
M3.2	PM18	Stage-2 calorimeter trigger hardware tested and installed	PM28
M3.3	PM23	Stage-1 calorimeter trigger commissioned & system ready for physics	PM27
M3.4	PM30	Post-LS3 trigger dataflow design completed	PM30
M3.5	PM35	Stage-2 calorimeter trigger commissioned & system ready for physics	PM35
M3.6	PM54	Post-LS3 trigger prototype trigger modules produced and tested	PM54
M3.7	PM66	Demonstration of post-LS3 trigger slice	PM66
M3.8	PM72	Post-LS3 trigger construction plan delivered	PM72

12 Glossary

Following the request at a previous meeting, we compiled a list of acronyms in common use in the report, or during the oral session, or by CMS which we may have referred to.

AMC13	A μ TCA data concentration and clock distribution card specific to CMS.
AMC	Advanced Mezzanine Card (from the ATCA specification).
APD	Avalanche Photodiode
ASIC	Application Specific Integrated Circuit.
ATCA	Advanced Telecommunications Architecture.
BER	Bit Error Rate.
BX	Bunch crossing.
CBC(x)	CMS Binary Chip, version x, for the front-end ASIC for the outer tracker
cDAQ	Central Data Acquisition.
CMSSW	Compact Muon Solenoid Software, is the CMS experiment software package.
CPM	Central Partition Manager.
CPU	Central Processing Unit.
CRC	Cyclical-redundancy check, a family of algorithms for identifying data corruption.
CTP7	Calorimeter Trigger Processor 7 card, featuring the Xilinx Virtex-7 FPGA.
DAQ	Data Acquisition.
DAQ2	Upgrade to DAQ system during LS1.
DSP	Digital Signal Processor.
DTC	Data, Trigger and Control board
DPG	Detector Performance Group.
FB	Finance Board.
FC7	FMC Carrier Xilinx Kintex 7, a processor board hosting multiple FMCs.
FED	Front End Driver, a CMS data acquisition board.
FMC	FPGA Mezzanine Card, ANSI/VITA standard for cards which interface to FPGAs.
FPGA	Field-Programmable Gate Array.
FSM	Finite State Machine.
GBT	Gigabit Transceiver Project at CERN.
GBTX	Gigabit Transceiver ASIC developed at CERN.
GCT	Global Calorimeter Trigger.
GLIB	General purpose μ TCA card developed by the CERN microelectronics group.
GMT	Global Muon Trigger.
GP	Geometric Processor.
GT	Level 1 Global Trigger.
GTX	A version of the Xilinx high speed serial transceiver, found on the Virtex 7 FPGA.
HDL	Hardware Description Language.
HGC	High Granularity Calorimeter, the proposed new endcap CMS calorimeter.
HI	Heavy Ions, at the LHC refers to collisions between lead ions.
HL-LHC	High Luminosity LHC, the planned upgrade of the LHC machine around 2023.
HLT	High Level Trigger, a collection of software trigger algorithms.
HT	Hough Transform Processor.
I2C	Inter-Integrated Circuit chip-to-chip communications protocol.
IB	Institution Board.
IPbus	A protocol to control and communicate with Ethernet-attached xTCA hardware.
IPMI	Intelligent Platform Management Interface, a standardised computer system interface.
JTAG	Joint Test Action Group; test and diagnostic bus standard by IEEE1149.1.
L1A	Level-1 Accept.
LP-GBT	Low power GBT.
LS1	Long Shutdown 1, first LHC long shutdown from beginning 2013 to end of 2014.
LS2	Long Shutdown 2, second LHC long shutdown scheduled for around 2018.
LS3	Long Shutdown 3, third LHC long shutdown scheduled for around 2022.
MGPA	Multi-Gain Preamplifier ASIC, used to readout ECAL photosensors.

MIP	Minimum Ionising Particle
MMC	Mezzanine Management Controller, part of the μ TCA specification.
MP7	Master Processor 7 card, featuring the Xilinx FPGA Virtex-7 chip.
MTF7	Muon Track Finder 7 card, featuring the Xilinx FPGA Virtex-7 chip.
MPW	Multi Project Wafer manufacturing submission, for CMOS ASIC production.
μ GT	Micro Global Trigger.
μ HAL	Micro Hardware Abstraction Layer.
μ HTR	Micro HCAL Trigger and Readout Card.
μ TCA	Micro Telecommunications Computing Architecture.
O2O	Software to simplify the propagation of configuration online.
oRM	Optical Receiver Mezzanines.
oRSC	Optical Regional Summary Card
oSLB	Optical Synchronization and Link Boards.
PCIe	Peripheral Component Interconnect Express, a high-speed serial computer bus.
SerDes	Serialiser/Deserialiser chip.
SFP	Small Form-factor Pluggable standard for optical and other transceivers.
SFP+	Extension of the SFP standard to support up to 10 Gbps data rates.
SLINK	CERN specification for an easy-to-use FIFO-like data-link.
TCC	Trigger Concentrator Card.
TCDS	Trigger Control and Distribution System.
TFP	Track Finder Processor.
TMT	Time-Multiplexed Trigger, that processes events in parallel rather than sequentially.
TMTT	Time-Multiplexed Track Trigger
TPG	Trigger Primitive Generator.
TriDAS	Trigger and DAQ.
TTC	Trigger Timing and Control, a system for distribution of clocking and control.
UCG	Upgrade Cost Group.
μ HTR	μ TCA HCAL Trigger and Readout card.
VTRX	Versatile Link Transmitter/Receiver, optical transceiver developed by CERN.
VTTx	Versatile Link Dual Transmitter, optical transmitted developed by CERN.
XDAQ	Cross DAQ, a data acquisition software framework.
YETS	Year-End Technical Stop, a brief stop of the LHC during the winter holidays.