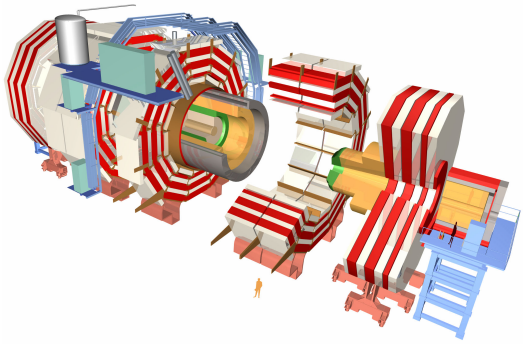
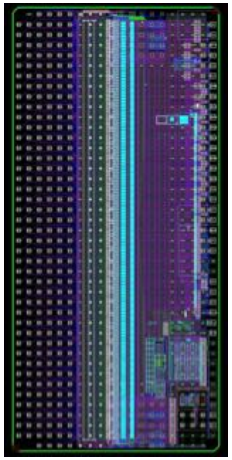




UK CMS Upgrade Oversight Committee

9 May 2017

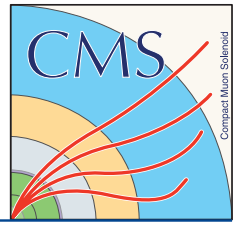
University of Bristol
Brunel University London
Imperial College London
Rutherford Appleton Laboratory

Overview

- Snapshots of LHC & CMS status
  - 2016 very successful production year with 41.1 fb^{-1} p-p and 186 nb^{-1} p-Pb delivered
    - UK L1 trigger upgrade operated successfully all year with excellent results
  - 2017 operations now restarting
    - CMS upgrades largely completed. Now commissioning new pixels, and rest of CMS.
- Summary of UK upgrade project
  - Recent WP progress, much quite significant
- Recent steps towards post-2019 construction project
- Matters arising from last OSC

from CMS Spokeperson at April RRB

EYETS Challenge Winter/Spring 2017

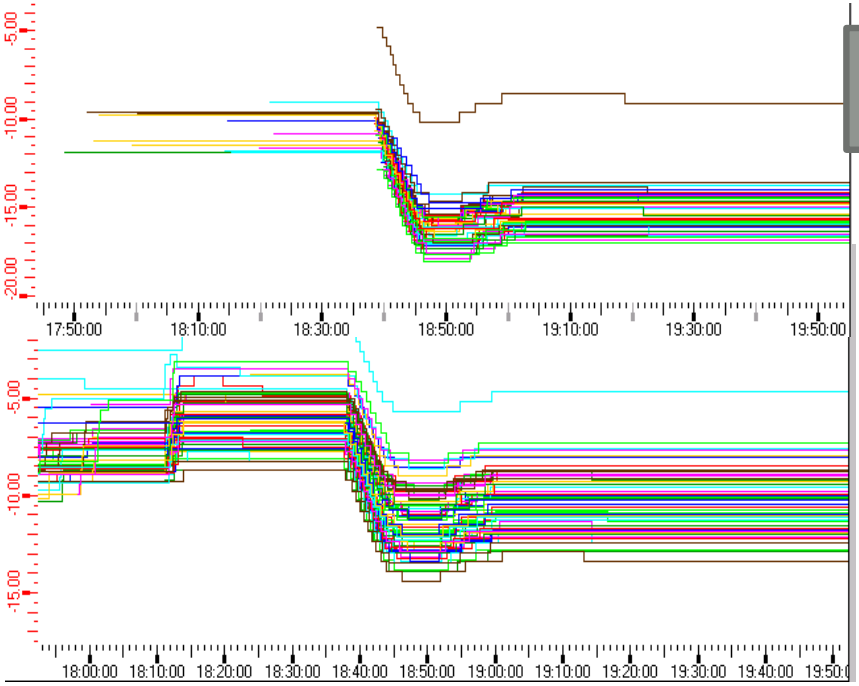


- **Install a new pixel detector**
  - Four layers in the barrel (BPIX) rather than three
  - Three disks in each endcap (FPIX) rather than two
  - **Better readout able to run up to 2-2.5x10^{34} cm^{-2} s^{-1} with almost no inefficiency (from hit loss) or dead time**
- Implement multianode feature of PMTs on Forward Hadron Calorimeter (HF)
  - Reject spurious signals that produce false MET
- **Replace the sensors in the Hadron Calorimeter Endcap (HE) with Silicon Photomultipliers (SiPMs)**
  - Improved light yield compensates for higher than expected radiation damage to the HE scintillator
  - More longitudinal segmentation
- Several other improvements/Additions (GE1/1 muon detector demonstrator, luminosity monitor replacement)

Plan Modified

Status of New Pixel Detector

- 2-phase CO2 cooling is working: new service in CMS
  - Connection checkout and functional validation of the cooling for detector is done
- Pixels are now included in running on cosmic rays
- **Green light was given to close CMS on March 24th**



FPIX and BPIX temperatures when set point changed from -15C to -20C: VERY smooth!

LHC schedule 2017

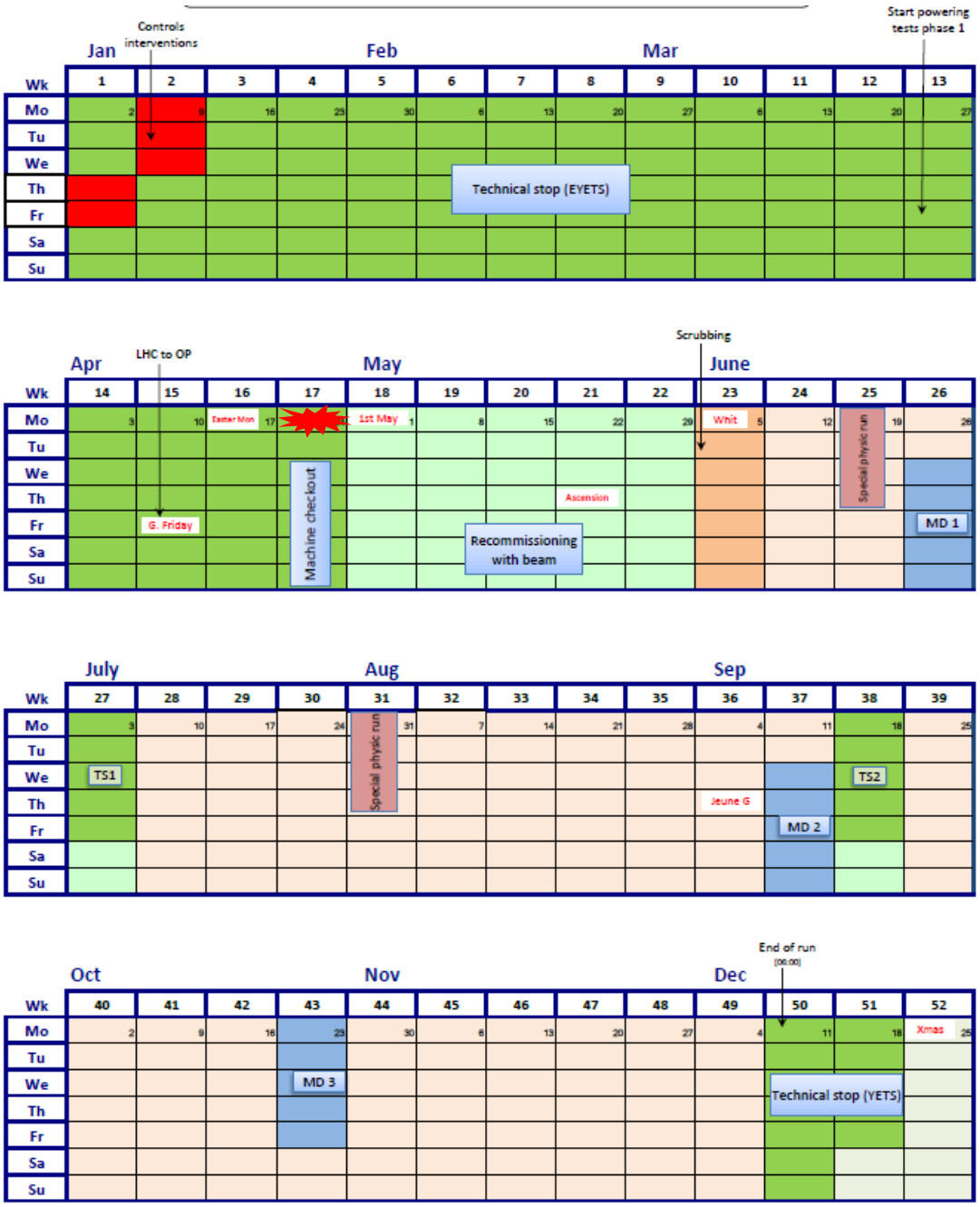
a new p-p production year at 13 TeV

Goal 45fb^{-1}

keeping the LHC availability close to 50% (stable beams)

Initially 15 days of MD; later during 2017 according integrated luminosity : + 3 days ?

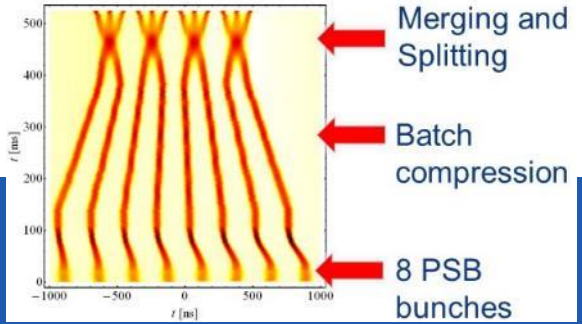
Special runs: VdM scans,… and … LHCC recommendations



2017 scenarios

	Nominal	BCMS	BCMS+
Beta* (1/5) [cm]	40	40	33
Half crossing angle [urad]	185	150	170
No. of colliding bunches	2748	2544	2544
Proton per bunch	1.1e11	1.2e11	1.2e11
Emittance into SB [um]	~3.2	~2.3	~2.3
Bunch length [ns]	1.05	1.05	1.05
Peak luminosity [$cm^{-2}s^{-1}$]	~1.1e34	~1.7e34	~1.8e34
Peak pile-up	~28	~48	~52
Luminosity lifetime [h]	~24	~15	~14

BCMS = **B**atch **C**ompression **M**erging and **S**plitting



April 2017 RRB: author forgot to update footer

UK R&D status

Last 6 months

- WP2: Tracker ASIC and readout
  - CBC3 delivered November and successfully tested since then
    - minor features require correction
    - TID radiation tests done, and SEU tests soon
- WP3: L1 trigger complete
  - focus now on remaining R&D
  - MP-Ultra working well & ATCA developments underway
- WP4: HGCal
  - Snapshots of recent progress required for TDR in late 2017
- WP5: L1 track-finder
  - Very successful TMTT FPGA-based demonstrator completed
  - Decisions on implementation remain somewhat controversial
    - All-FGPA solution recommended, following technical task force

WP2 status

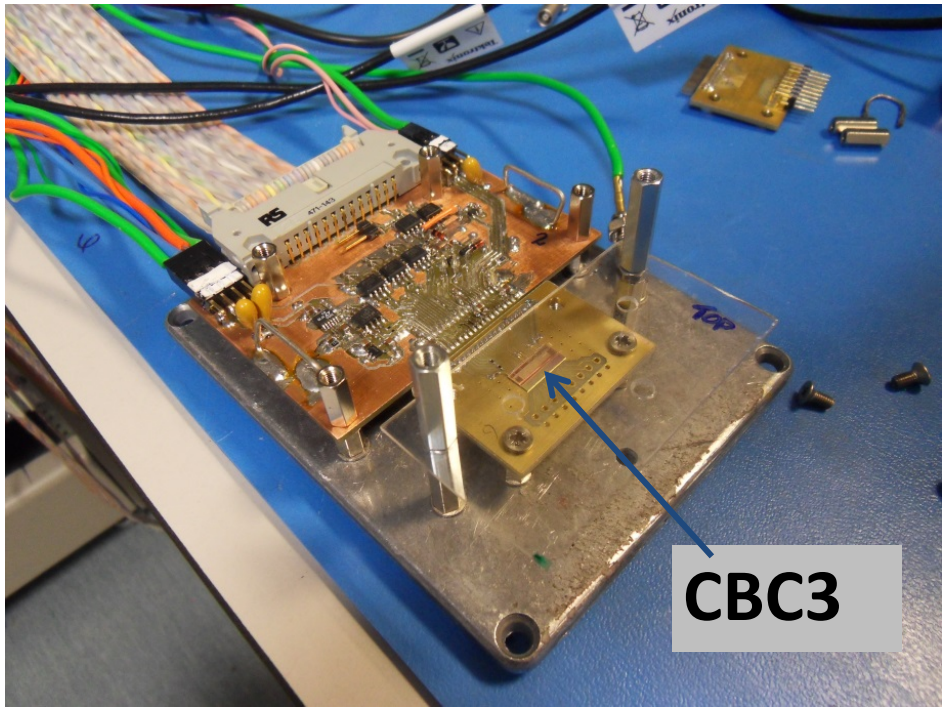
9 wafers delivered - 1 diced

wire-bonded onto chip carrier board

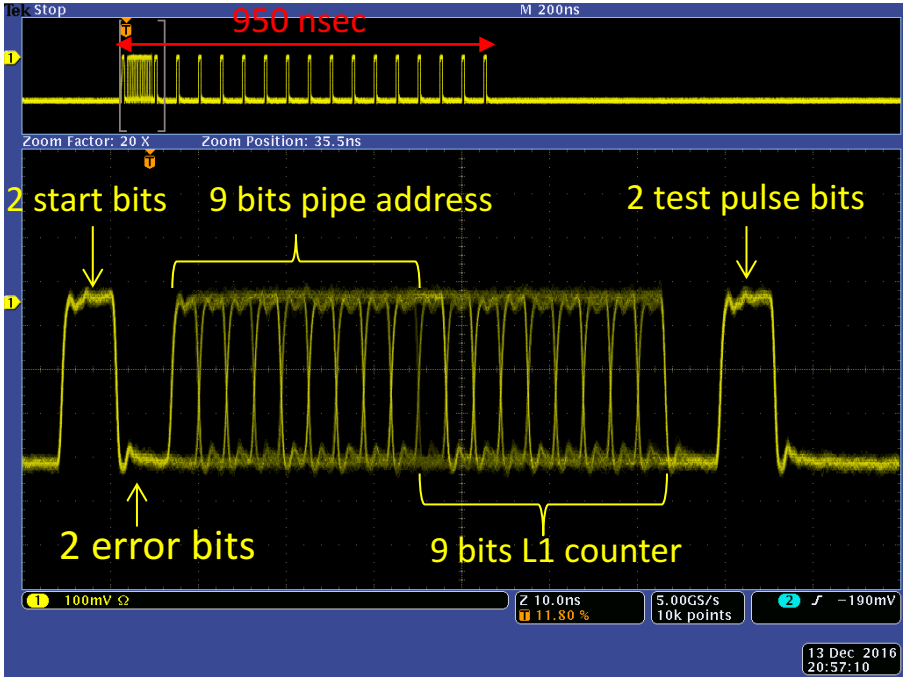
single chip test setup enables:

- functionality to be verified
- wafer probe tests to be developed
- ionizing and SEU tests to be carried out

single chip test setup



scope picture of output data



full functionality confirmed

5 wafers tested and sent for bump-bond processing

SEU testing imminent

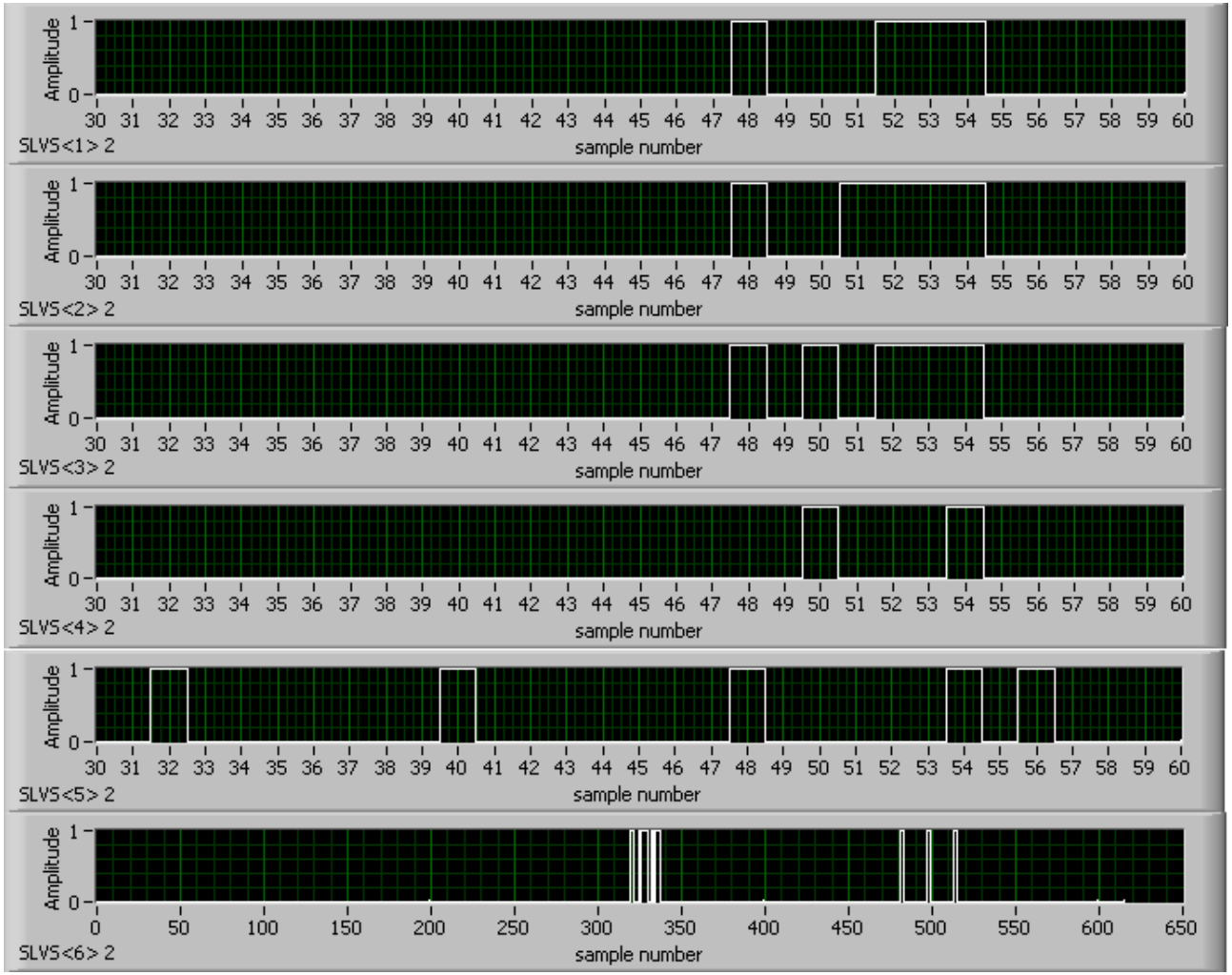
CBC3 digital functionality

CBC3 outputs data on 6 diff. pairs at 320 Mbps

up to 3 stubs addresses + bend information per 25 nsec BX

+ triggered readout data frame

digital data acquired - 3 stubs generated using on-chip test pulse



pT stub address 1

pT stub address 2

pT stub address 3

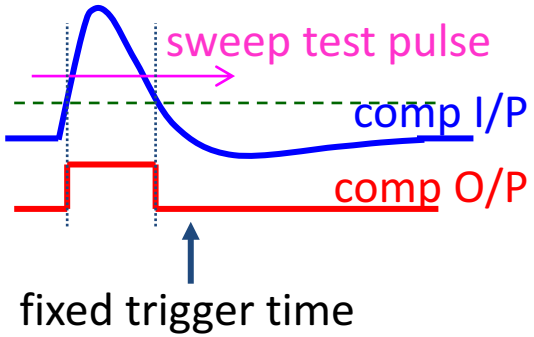
pT stub 1 & 2 bend info

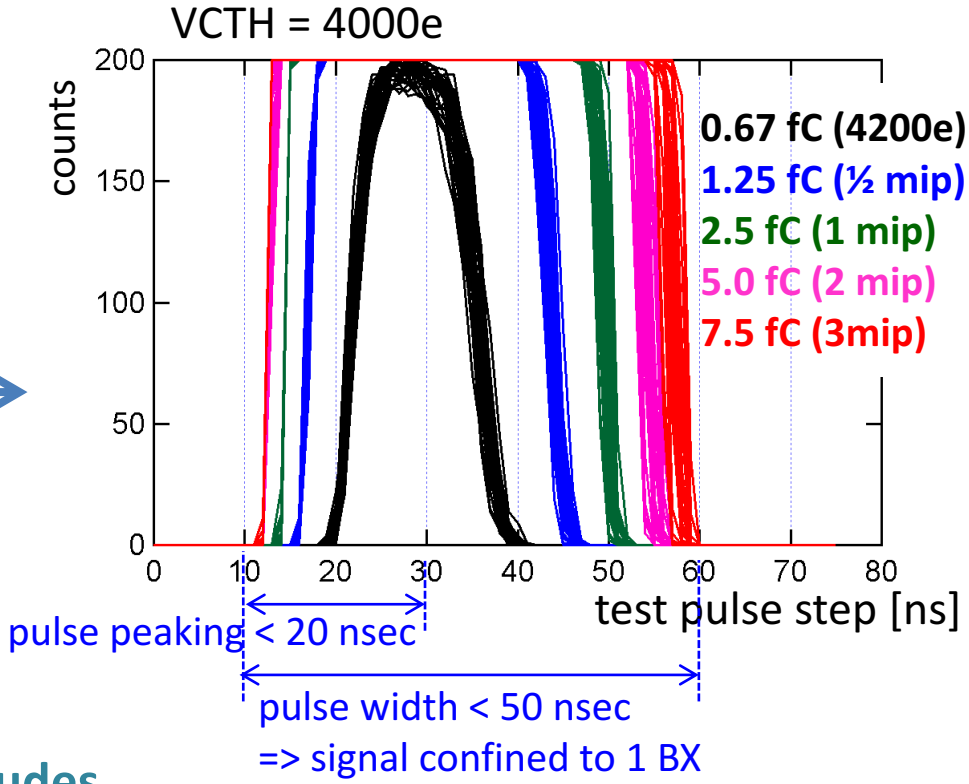
pT stub 3 bend info + sync

L1 triggered data

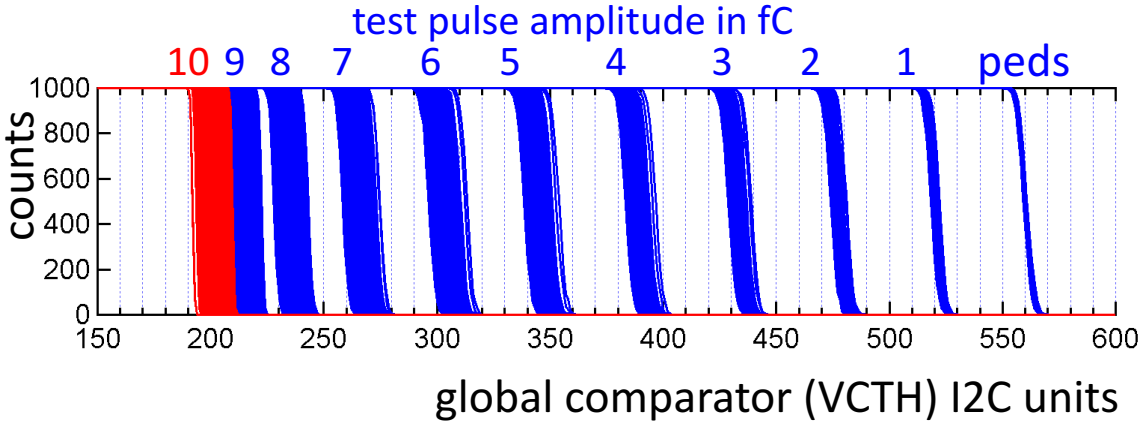
CBC3 analogue functionality

front end amplifier performance verified using on-chip test pulse





s-curves for different test pulse amplitudes



channel offsets can be tuned & s-curves well-behaved

Wafer probe tests

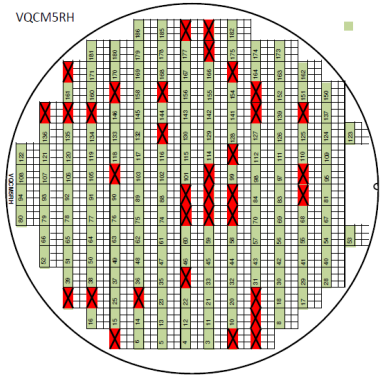
5 wafers: average yield ~ 85%

now being processed for bump-bonds

chips expected in June

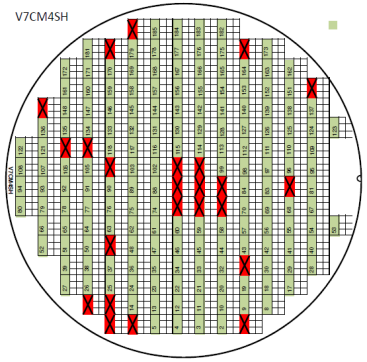
2-chip hybrids designed

expect bump-bonded hybrids and mini-modules (with sensors) later in summer



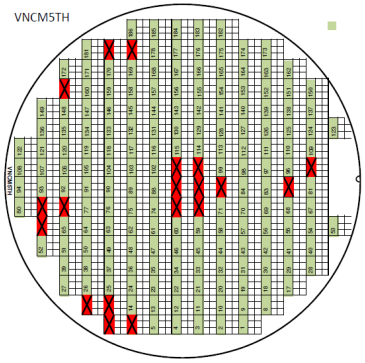
152 passes
34 failures
81% yield

failed chips



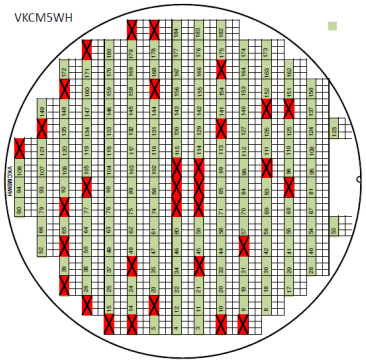
162 passes
24 failures
87% yield

failed chips



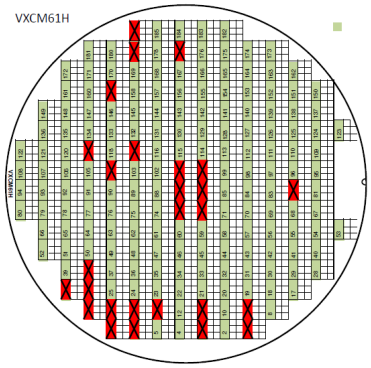
167 passes
19 failures
89% yield

failed chips



154 passes
32 failures
83% yield

failed chips

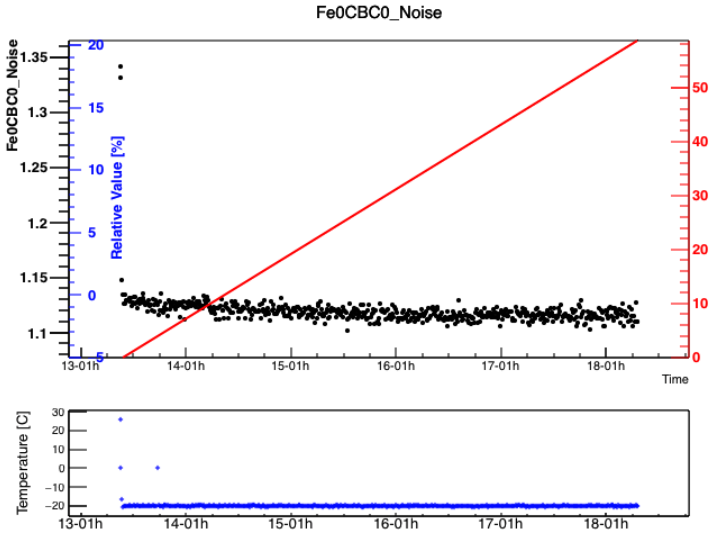


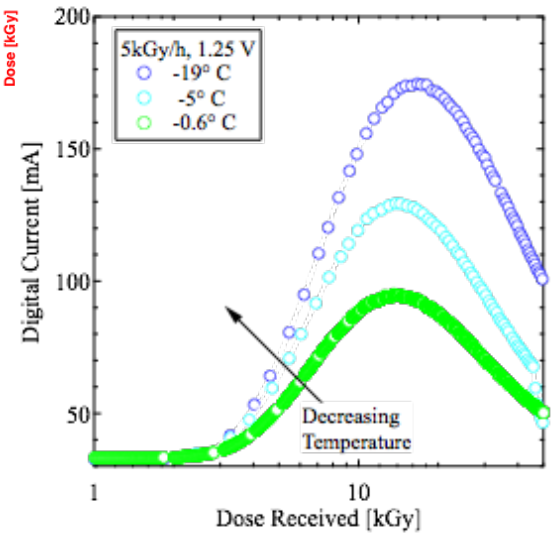
159 passes
27 failures
85% yield

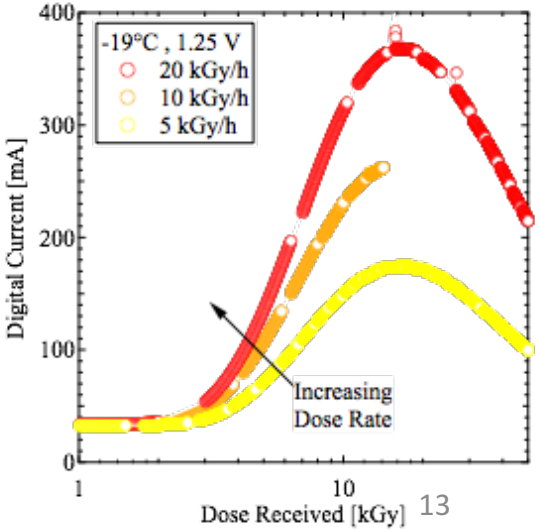
failed chips

CBC TID tests

- Two recent one-week x-ray irradiations (thanks to CERN source!)
  - forced to explore much higher dose rate than LHC
  - expected current increase from digital logic observed
    - parameterisation necessary to extrapolate to HL-LHC (4 Gy/h @ -10C)
  - no change in performance to high doses
  - infer ΔI/I ≤ 1% under realistic conditions

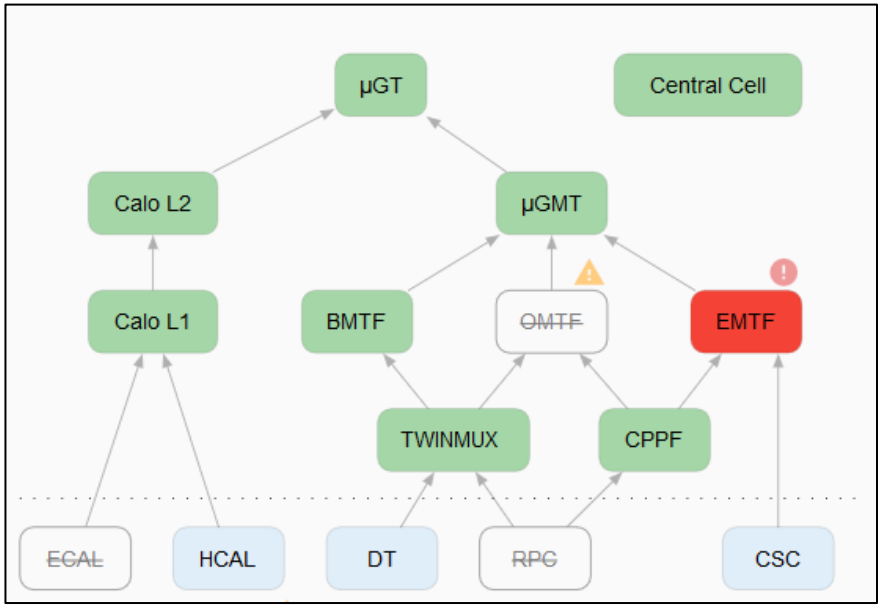






WP3: Phase I & II L1 trigger

- Phase-I Upgrade running successfully during 2016
  - Less than 10% of downtime due to L1 Trigger
  - 96% of data (luminosity weighted) taken by CMS certified as good for physics
  - Only 3% of the 4% marked bad due to L1 Trigger – 0.1% of data taken.
- Excellent result for a complex system, combining data from many subsystems.

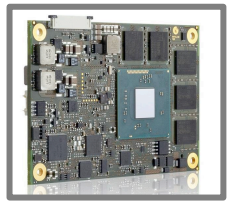


- Phase I upgraded trigger now considered completed and an operations project

New monitoring page for trigger to aid rapid fault diagnosis and resolution

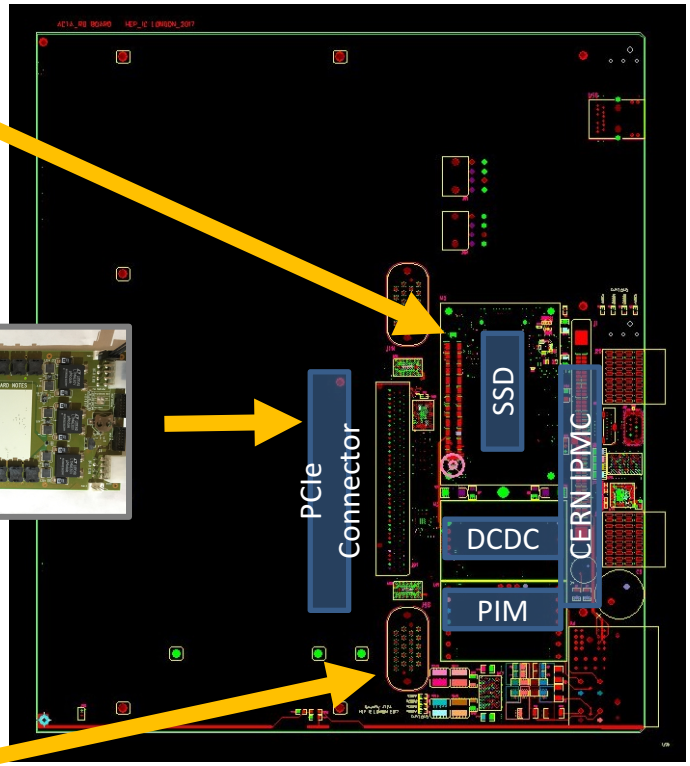
WP3: ATCA test card

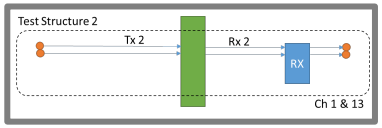
- Service Card in manufacture
  - Full size ATCA prototype
    - PCBs produced
    - Assembly pending 25Gbps backplane connectors
  - MP-Ultra(s) now fully assembled
    - working but some delays in evaluation due to illness and late delivery
- Allows ATCA services (infrastructure) to be validated
  - low cost card, includes:
    - 25Gbps test structures
    - Thermal analysis test vehicle
    - PCIe connector to host MP-Ultra



COM Express

MP Ultra

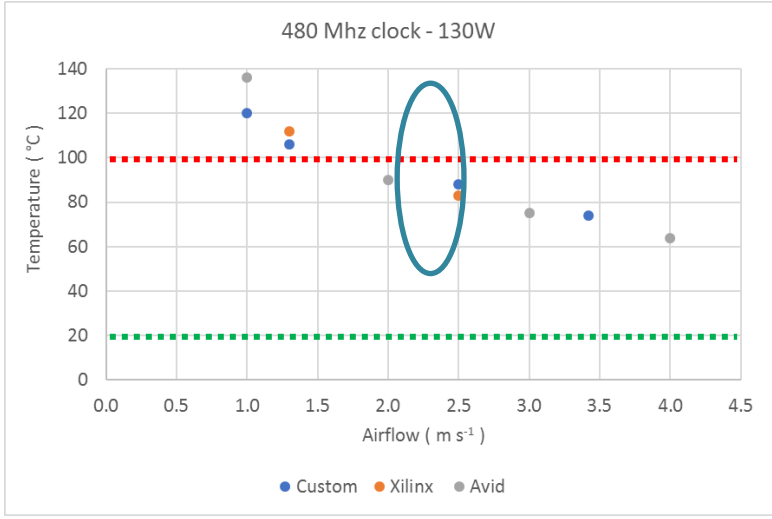


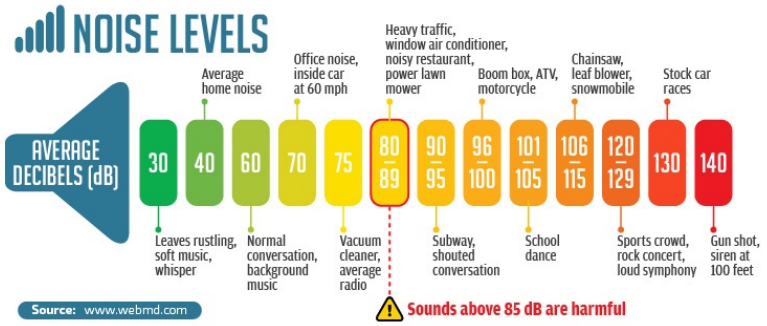


25Gb/s Test Structure w/wo Retimers (PCB & Backplane)

WP3: ATCA

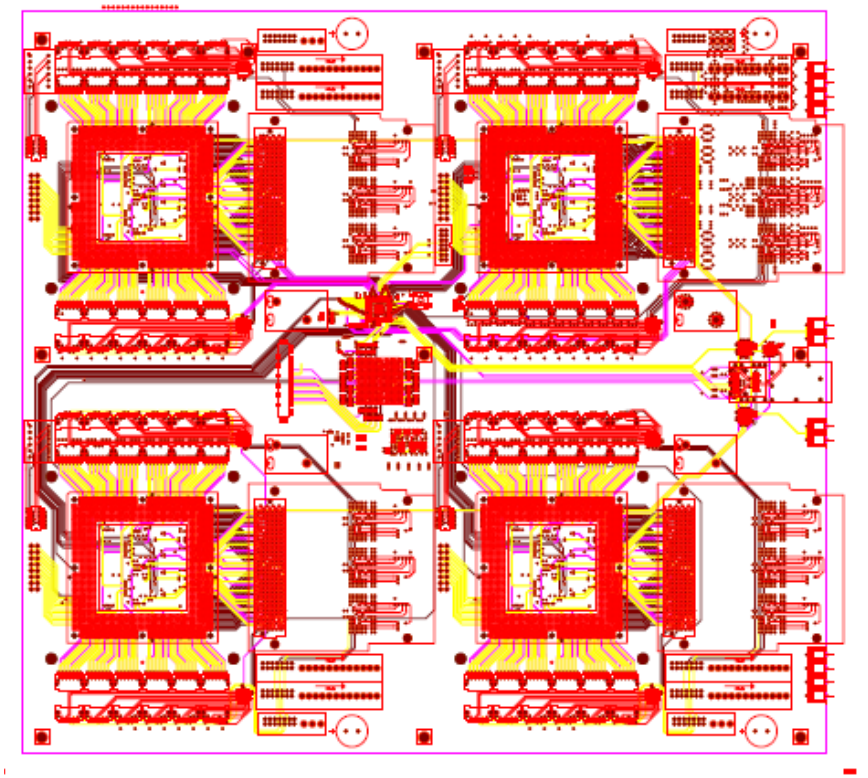
- Potentially important practical issues arise
  - Latest FPGAs may require significantly more power
    - Up to 130W, although 60W-100W more likely
    - Current designs typically 40W
  - ATCA offers better cooling via higher air speeds, but generates significant noise:
    - 87dBA per rack, 97 dBA in counting room and requires substantial power: 25% of load.
    - Alternatively, run hot (80-90 C) with large area heatsinks (10cm x 10cm)
    - If highest air speeds are required we need to ensure that we can safely operate systems underground.





WP3 planning

- R&D following 3 strands:
  - Develop firmware/software infrastructure about MP-Ultra
    - for algorithm development and validation
  - Validate Service Card infrastructure
    - such as COM Express control
  - Launch Prototype Card – Serenity –
    - to explore modular FPGA mounting and Rack Mount Chassis form factor



- More complete work plan in preparation
  - taking in account constraints from CMS planning and decisions

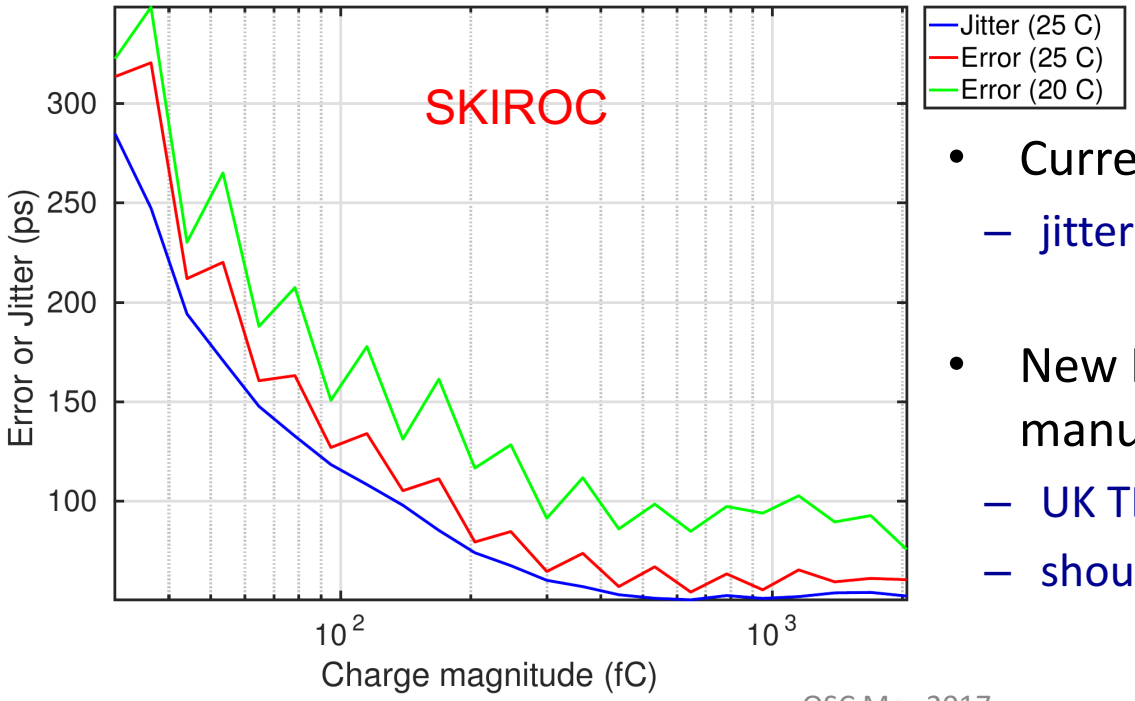
WP4: HGCal

- Present objectives
  - Front end electronics evaluation
  - Trigger primitive design
  - Physics performance and design optimisation

- All for TDR in late 2017
  - some snapshots of recent progress

HGCal FE ASIC design

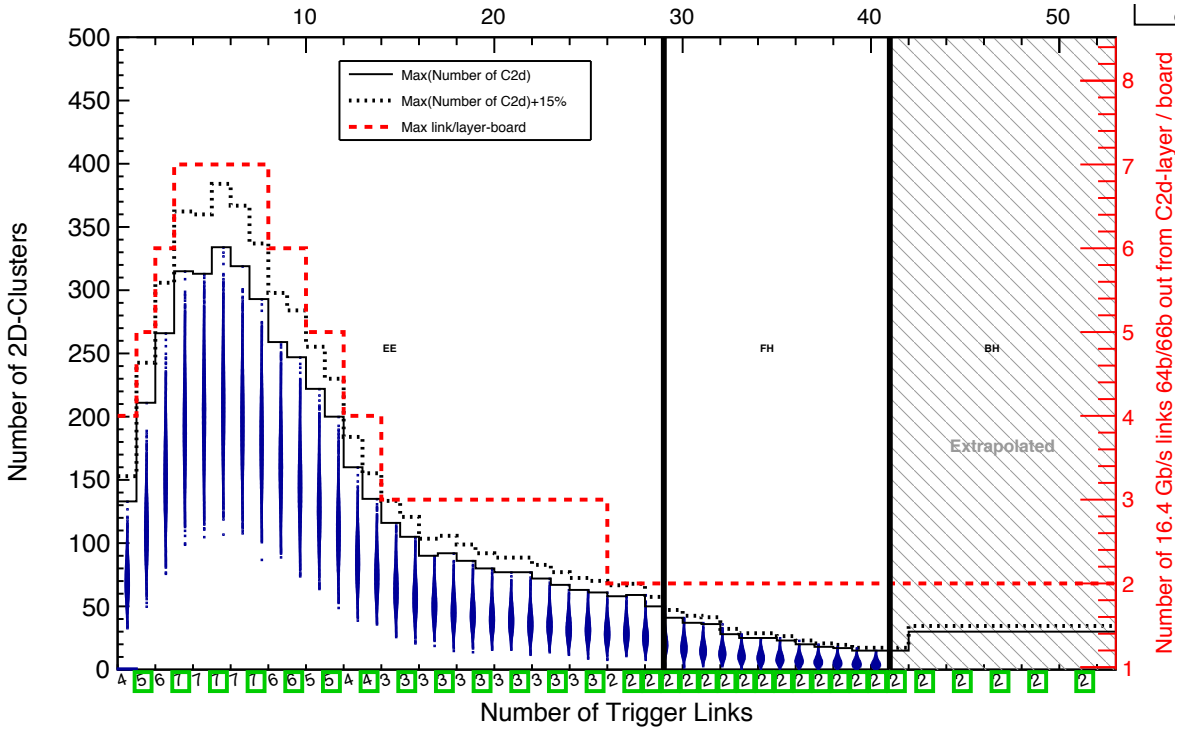
- FE ASIC uses TDCs for two applications
  - Time Over Threshold for large signals out of ADC range
    - extends energy range by factor ~100
  - Time Of Arrival measurement for precision timing
    - allows vertex association and background pileup removal
- Target: <O(50ps) resolution for large signals



- Current SKIROC (existing ILC ASIC)
  - jitter ~50ps for signals >500 fC
- New HGCal-specific ASIC due for manufacture
  - UK TDC design
  - should improve for smaller signals

HGCal bandwidth calculations

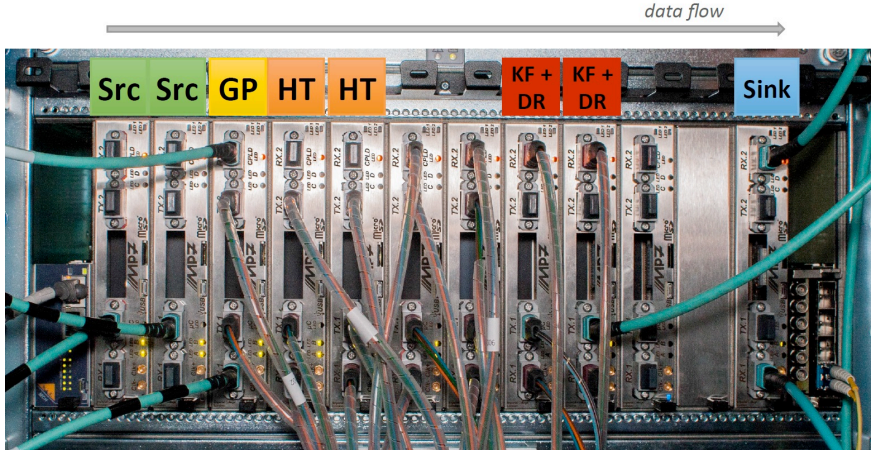
- Decision on HGCal electronics architecture (December) allows realistic bandwidth calculations for trigger system
  - working through different stages of trigger, updating BW requirements
    - report shows BW calculation for on-detector to trigger stage-1
  - here, BW for stage-1(2D clustering) to stage-2 (3D clustering)



- Blue: simulation of top pair events showing number of 2D clusters in each layer produced in trigger stage
- Red : BW allocation per layer
- Total bandwidth fits within constraint of input of stage-2

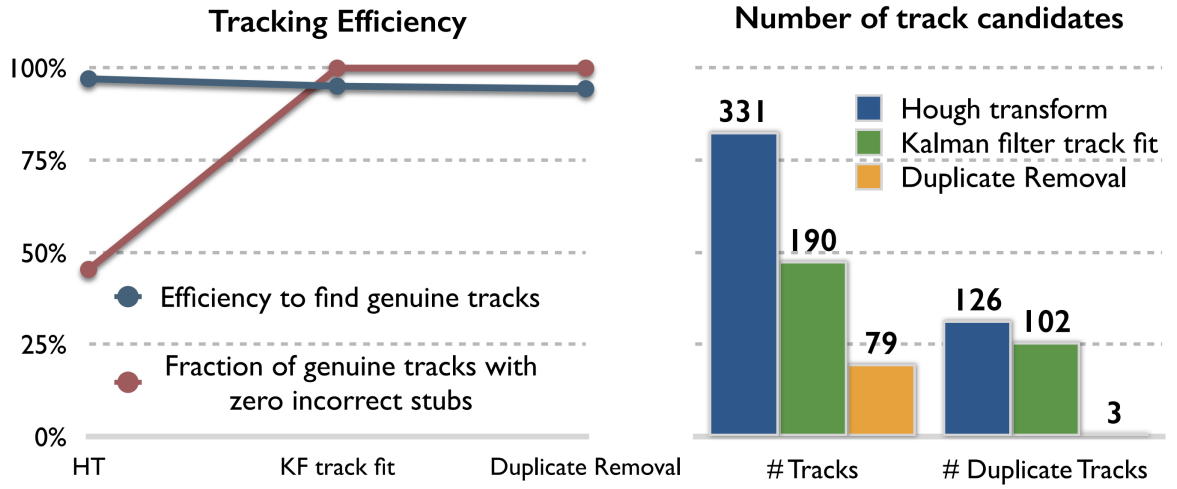
WP5: L1 track-finder demonstrator

- TMTT track finding slice completed in December
  - MP7-based system in CERN, injecting stubs generated in MC
    - scalable TM design allows extrapolation to future system, scale and cost
- Novel algorithms, or implementations, in challenging conditions
  - track finding down to 3 GeV/c, from input of O(20,000) stubs, within 4 μs
  - all firmware and application of algorithms unique to TMTT concept
    - Plenty of new ideas; continual development and improvements
    - Many contributors from several different groups



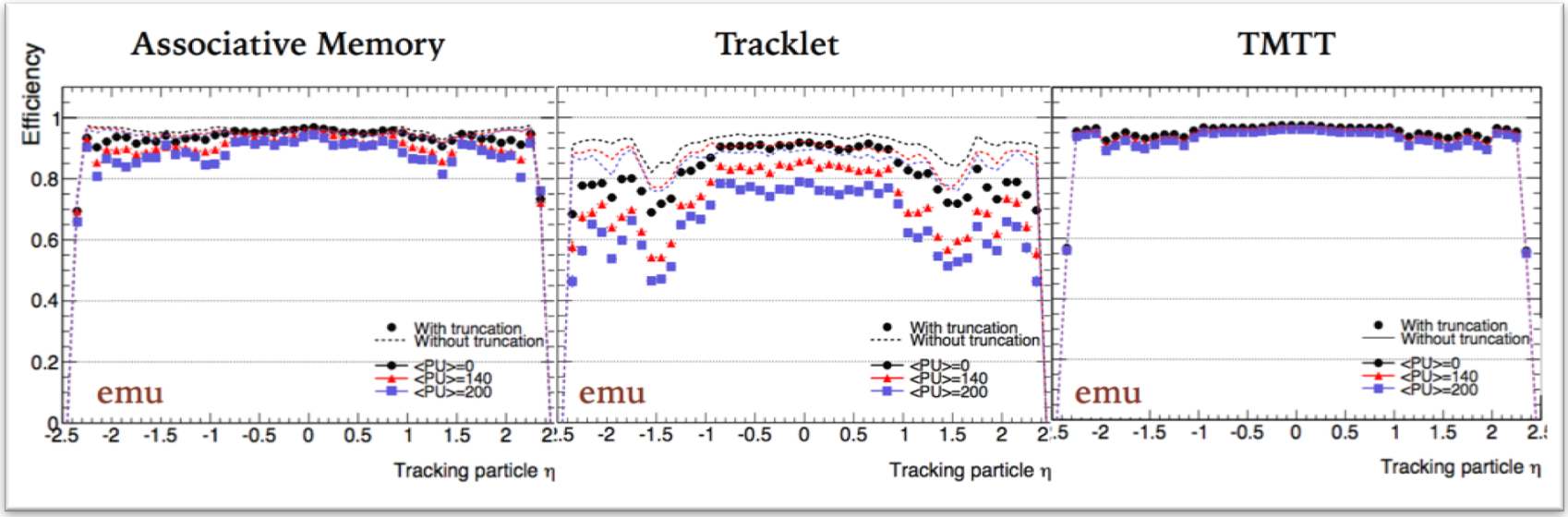
Demonstrator components

- Geometric Processor
  - pre-process stubs and assign to sub-regions
- Hough transform
  - coarse 2D tracking in r-ϕ plane to reduce downstream processing load
- Kalman filter
  - combined combinatorial filter/fitter in 3D rejects fakes and provide track parameters
- Duplicate removal
  - simple algorithm to remove duplicates generated by Hough transform



Review 8-9 December

- TMTT one of three approaches tried
  - acknowledged by review committee to be **only complete** demonstrator
  - overall latency measured 3.5µs (first in-first out)
    - pre-agreed specifications to ensure direct comparisons
  - can run t-tbar 200PU events without degradation, due to truncation in processing time
    - also expected to be least expensive option, with modest further R&D for optimal design



Review outcome

Summary from (internal) CMS Tracker Comprehensive Review 24-25 April

Review of system demonstrators – December 2016

- The review took place as advertised in the past CR
  - *During December TK week*
  - *Dates had been known for nearly 1 year and had been widely advertised*
  - *The charge of the review was attached to the agenda of the past CR*
  - *The review was open to the whole CMS and the attendance was very large!*
- Exhaustive results were shown by all three groups, addressing performance and robustness (up to 200 PU)
- A first reliable indication of the achievable latency was derived
- For all three methods, the results exceeded expectations in all respects!

- FPGA-based methods fully proven in hardware
- AM+FPGA emulated the missing chip in a Kintex Ultrascale FPGA (1'000 patterns instead of 250'000)

Review panel

D. Abbaneo – CMS TK Upgrade Coordinator
F. Vasey – CMS TK upgrade Electronics Coord
E. Perez – CMS Track Trigger Integration Coor
C. Foudas – CMS Trigger
A. Marchioro – CMS Expert
R. Van Berg – External Expert

Conclusions of the panel (unanimous)

Thanks to the remarkable efforts of the participating groups over the past months, **the results achieved demonstrate that track reconstruction at Level-1 is a realistic option for CMS at HL-LHC**. Although substantial optimization work remains to be done, the demonstration systems that have been realized have shown that **the three proposed methods can meet, and even exceed, the demanding requirements of the CMS trigger, with the necessary margin and robustness**.

While the **AM-based method requires a challenging chip development** in a novel (for HEP) technology, **carrying many unknowns that may significantly impact cost and schedule**, a method **based only on commercial FPGAs can be considered as low-risk**, provided that the required developments are **properly planned and managed**.

Follow-up

- In short, AM proponents don't yet want to accept review recommendations
  - main pressure comes from FNAL.
  - INFN seem to accept technical outcome, but has already invested in further AM design.
  - US universities mostly also either want to join FPGA project or recognise reality
- Technical task force met over last three months
    - Pesaresi, Tomalin, Rose (Iles) from TMTT
  - Conclusion that "compromise" board gains nothing and is impractical
  - All teams invited to join All-FPGA design in TK Phase II MB 26 April
    - AM proponents offered to continue with alternative "insurance"
- Next steps
  - Proposal from Tracker management to TK MBs in 16 & 17 May
  - Endorsement by TK Institution Board in June CMS week
  - Tracker management now seems determined to adopt FPGA solution

UK construction project

- Science Board: positive feedback on outline construction project
  - accepted plan but PPRP peer review needed
  - submission in October for January meeting

  - need L1 track finding conclusion soon to prepare final proposal
  - very limited development costs in construction project so aim to maximise progress on FPGA R&D in remaining two years of R&D project

Matters arising in November

- Financial status
  - SBS Oracle issue resolved soon after November meeting
  - Expenditure within targets with WA still intact
  - Now plan to release some of WA for CBC design work and travel
    - NB these funds retained in Imperial equipment allocation
- Breakdown of effort vs WP in separate table
  - NB WP5 demonstrator work essentially complete
- Revised risk register, with explanations
- Track-finder outcome
  - WP5 long term future to be decided
    - outline track-finder plan presented in CMS (only one!) so expect to refine UK activities in next six months

Conclusions

- All progress very positive

- Now optimise use of remaining resources and planning
  - may require STFC help in redistributing some funds

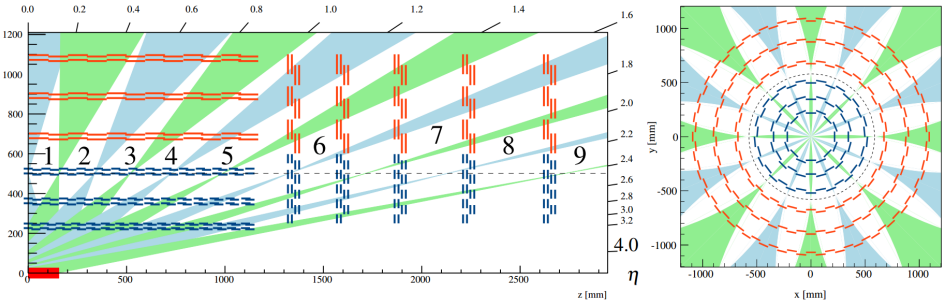
Further information

GP

HT

KF

DR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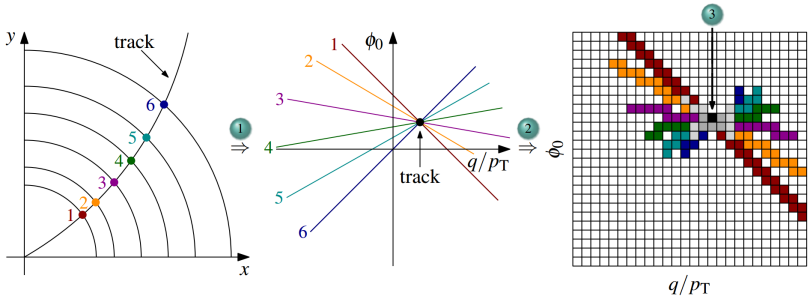
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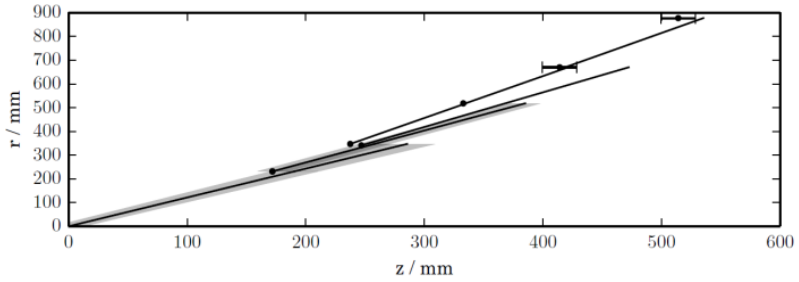
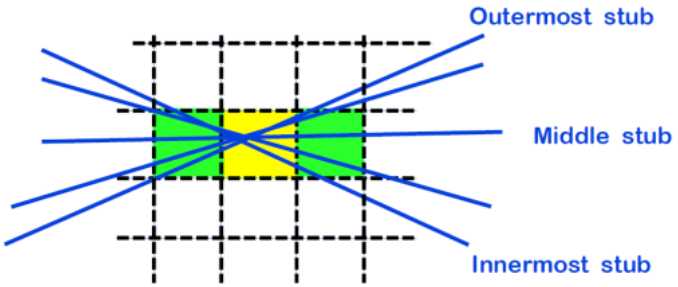
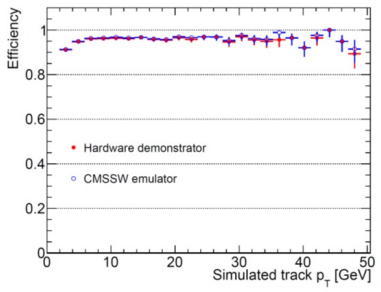
ϕ_0
q/p_T

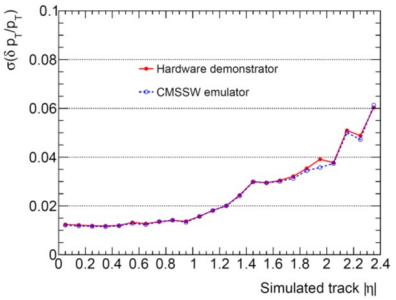

r / mm
z / mm

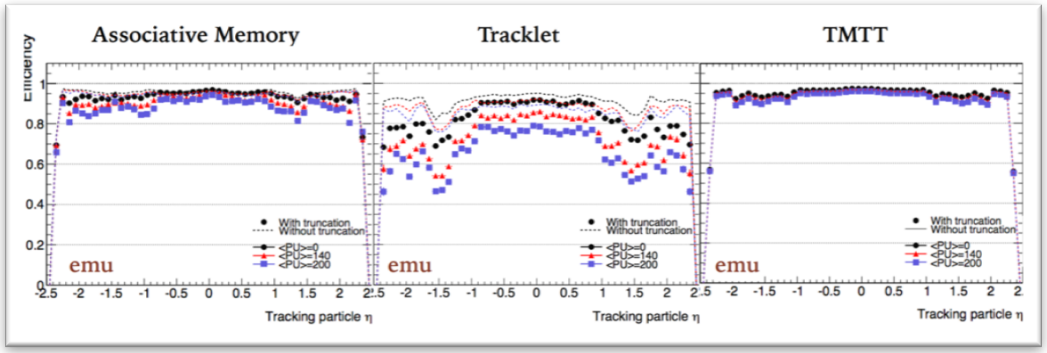

Outermost stub
Middle stub
Innermost stub

L1 Tracking Review 8th-9th December

- One of three demonstrator approaches
- TMTT acknowledged by committee as only complete demonstrator
- Overall latency **3.5us** (first-first)
- Pre-agreed specifications ensured like-for-like comparisons of results
- Can run ttbar+200PU event samples without degradation of performance, due to truncation in processing time







	conservative	baseline	advanced
link speed	10 Gbps	16 Gbps	25 Gbps
T	36 BX	18 BX	12 BX
$N_{DTC\_links\_out}$	72	36	24
$N_{TFP\_links\_in}$	64	64	64
$N_{TFP\_links\_out}$	8	4	2-3
N_{TFPs}	288 (8x36)	144 (8x18)	96 (8x12)
production cost	6.9 MCHF	4.3 MCHF	?