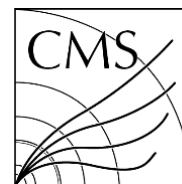


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Upgrades of the Tracker and Trigger of the CMS experiment at the CERN LHC

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1 Executive Summary

The new project started in April 2013; it continues work on the tracker and trigger begun in the previous R&D project. L1 track finding and endcap calorimeter work packages were added in 2016, but they rely on resources already within the R&D project, or on new external resources, from ERC and PRD grants. The Phase I upgrade of the L1 calorimeter trigger was completed in 2016. The project is now in its final year.

In the last six months there has again been significant further progress:

- CBC3 ASICs were bump-bonded to in-house designed hybrids at Imperial College in October 2017 and a couple of single-sensor modules successfully tested in a beam in November.
- Significant delays in metallizing CBC3 wafers and constructing hybrids were experienced in the last year. A mini 2S-module was assembled in CERN in November 2017, and tested in a beam in Fermilab in December.
- An additional lot of 24 CBC3 wafers was ordered at the end of 2017 for module development, mainly funded by CMS. However, Global Foundries are reporting long manufacturing lead times and the wafers are scheduled for delivery from the foundry at the end of June 2018.
- The latest version of the CBC (CBC3.1), which is hoped to be the final one, was submitted in February. We have learned from Global Foundries only as this report was being finalised that the delivery date is expected to be the same as the CBC3, i.e. 25 June.
- The first ATCA prototypes of the common hardware development have made several steps forward.
- The first set of prototype cards for the Serenity ATCA platform have been delivered and are under test, with promising results.
- Preliminary firmware and software infrastructure has been developed and the firmware and software stack milestone for Xilinx UltraScale devices was met on time.
- The common hardware planning foresees production of a larger number of boards later this year, to be shared with collaborators (recovering costs or reciprocating expenses). This should expedite the work of UK projects which plan to utilise this hardware, as well as ensure the commitment of CMS to this collaborative model of hardware development, which is a novel enterprise.
- The Phase-II L1 Trigger Interim Technical Design Report was approved by the LHCC in November 2017 and plans are now under way for the full TDR which is due at the end of 2019. The UK contributions to the upgraded trigger should profit from the common hardware developments and successful innovations from our R&D, such as time multiplexing and algorithm developments.
- The HGCAL Technical Design Report was submitted last November and reviewed by the LHCC and Upgrade Cost Group. The project is now approved.
- Work on the HGCAL has included evaluation of a UK-designed low-power TDC circuit in the HGCROC ASIC which was delivered in December. The TDC is working correctly and would be a viable choice for the final ASIC.
- The TDR reviews raised no significant issues related to the HGCAL back-end electronics, based on our common hardware.
- Further simulations have optimised HGCAL trigger performance and a new 2D clustering algorithm has been developed. Trigger firmware development will commence soon using the Serenity hardware.
- The paper describing the UK-led L1 track-finder demonstrator system design and results has been published.
- Further optimisation of the track-finder algorithms and firmware continues, including adaptation to the tilted barrel tracker geometry and architectural constraints from detector cabling and infrastructure.

- Algorithms have operated at higher frequencies taking advantage of FPGA technology improvements now accessible which increase processing margins in the system.
- The CMS UK proposal for a five year construction project from April 2019 has been reviewed by the PPRP, and we await the outcome. Although not the direct concern of this project, we draw attention to the fact that making a smooth transition to the construction project, including planning deliverables, employment of staff and recruitment of students, will be influenced by timely knowledge of the new project allocations.

2 Project history and recent developments

The LHC upgrade is proposed to take place in two main stages, with an increase in luminosity reaching $\sim 2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ in LHC Run 2 now under way, then after a shutdown from the end of 2023 to mid-2026 in LS3, to $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ levelled luminosity, denoted as Phase II at the High Luminosity LHC (HL-LHC). During LS2, which starts at the end of 2018, the LHC energy will also increase to 14 TeV. In runs following LS3, a total of 3000 fb^{-1} in integrated luminosity over about a decade is the goal. This should lead to a typical pileup of 140 events/BX but in view of the possibility to increase the luminosity even higher, or accommodate fluctuations without much degradation in performance, CMS aims to be operable at up to 200 events/BX corresponding to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ levelled luminosity.

Interestingly the CERN accelerator team continues to extend the goals. The baseline remains as described above. However, they report an “ultimate goal” to deliver $320 \text{ fb}^{-1}/\text{year}$ with luminosity levelled at $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and pileup of 200, aiming for an integrated luminosity of 4000 fb^{-1} . In addition, studies are under way to possibly achieve a further increase in the energy to 15 TeV.

The current phase of the project began on 1 April 2013. The technical work packages are WP2 for Phase II outer tracker readout R&D, WP3 for Phase I calorimeter trigger construction, now complete, and R&D aimed at Phase II, now with a strong common hardware element, WP4 on the high granularity forward calorimeter project and WP5 on L1 track-finding.

2.1 LHC operations and progress

CMS p-p operations in 2017 ended successfully with a harvest of good quality data, despite some challenges both from machine operations and some detector-related problems which emerged during the autumn. CMS recorded 45.1 fb^{-1} of good quality p-p data at 13 TeV centre of mass energy (Figure 2.1) with an LHC injection scheme, to overcome cryogenic problems reported last time, which generated very high peak pileup of up to 80. ATLAS and CMS agreed to level the luminosity at around $1.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, which corresponded to pileup values around 55.

Overall efficiency in 2017 was over 93% which included the commissioning of the new pixel detector, and dealing with problems also reported last time, which began in October.

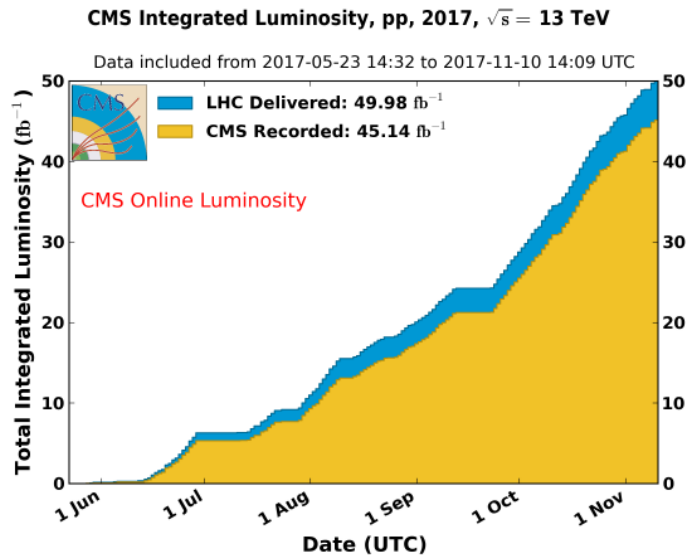


Figure 2.1. LHC and CMS integrated luminosity status in 2017.

Starting in early October, failures were observed in pixel DC-DC power converters, reaching 5% of the total by the end of the year. The impact on data quality was marginal, thanks in part to redundancy introduced by the additional fourth layer in the new detector. It proved impossible to identify the origin of the failures with the detector installed and the malfunction could not be reproduced in laboratory tests. CERN and the other LHC experiments agreed to start the year end technical stop (YETS) one week earlier to extract the detector and gain access to broken samples before the end of year lab closure. Detailed studies during the lab closure, with help from the CERN chip designers, confirmed the location of the failure inside the FEAST DC-DC converter ASIC, but still did not identify the cause of the failure. In addition, further investigations identified unusual (high current) I-V characteristics below the turn-on threshold in about 30% of the converters, that could be a precursor of failure. After further discussion with CERN the YETS was extended by a further week, allowing all the power converters to be replaced with newly produced ones before the detector was re-installed for 2018 operation.

Clearly this remains a concern for operation this year and has involved intensive work, not only from the tracker but from Technical Coordination and expert panels, to review the situation. Until the cause of the failure is identified it also has potential implications for the HL-LHC upgrades, where DC-DC converters of the same type will be widely deployed.

At present, both pixel and strip tracker subsystems have been recommissioned after the repair and re-installation of the pixel detector. The strip system stays unchanged at an active channel count of 96.3%, while the pixel good channel count increased to about 97%, i.e. by almost 2% with respect to spring 2017. To mitigate high leakage currents due to irradiation in the strips system on a few channels with degraded cooling contacts, the operation temperature has been successfully reduced from -15°C to -20°C .

The Level-1 Trigger operated very well in 2017. In addition to the usual collision runs, several special runs, a proton-proton reference run for the heavy ion program, a low pile-up run including TOTEM and the first LHC Xe-Xe ion collision run, required custom Level-1 Trigger settings, and were achieved very successfully. CMS also took a fill without luminosity levelling, providing data up to mean pileup values of around 80, to study future LHC running scenarios.

At the end of the 2017 run, work over the year-end technical stop began. This consisted primarily of software updates, and some maintenance and consolidation of the system. The improvement of calibrations and optimization of parameters for conditions expected in 2018 is on track, and we expect to run up to an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ in 2018 with improved physics efficiency in

comparison to 2017. Further proposals from physics groups are being discussed and preparations are also underway for the lead-lead run later in the year.

The restart of the trigger system after the year-end technical stop proceeded without any significant problems. The Level-1 Trigger ran successfully in the several mid-week cosmic-ray runs, with various tests and minor upgrades being made when the system is not required to provide triggers for CMS global running.

2.2 CMS planning

Following a description of the overall scope of the CMS Phase II Upgrade in the Technical Proposal approved in 2015, CMS has submitted Technical Design Reports (TDRs) for each of the major projects. TDRs for the Tracking System, Barrel Calorimeters, and Muon Systems have been reviewed by the LHCC and UCG and the projects approved by the Research Board. The TDR for the Endcap Calorimeter has been reviewed by the LHCC and the project planning information reviewed by the UCG. Approval has been given by those bodies.

Interim TDRs were submitted and reviewed for the L1 Trigger and the DAQ/HLT systems, with their full TDRs planned for 2020/2021. These projects require shorter production periods and can profit from progress in commercial technology in the next few years. In addition, a Technical Proposal (TP) was submitted for the addition of a dedicated precision timing detector to the Phase II scope, the MTD (Minimum-ionising particle Timing Detector). The TP was reviewed by the LHCC, and the Research Board approved the project to proceed to the TDR stage, with submission of the TDR expected for late 2018 or early 2019.

These documents include extensive simulation studies to demonstrate physics performance, describe system design and remaining technical choices, and present the project schedule and cost. Accompanying each TDR, detailed cost and schedule information, a risk assessment and an estimate of the manpower needs were reviewed by the Upgrade Cost Group.

The funding model for the upgrades has been updated with the current information on project costs and on contributions from the Funding Agencies. Following TDR approvals, agreements on funding and on construction responsibilities will be described in Memoranda of Understanding (MoU), anticipated later in 2018. In addition to the progress through this approval process, all projects continue to make excellent technical progress, progressing from baseline design and technology demonstration to advanced prototypes and detailed engineering design.

2.3 UK adaptation to CMS planning

Our construction plan for the period 2019-2024 was submitted to STFC in October 2017 and has been extensively reviewed by the PPRP. We now await the decisions and recommendations to allow a smooth transition to the next phase of the UK upgrade work.

It is probably worth noting that the scope of the project has evolved over the last couple of years, as the plans for the full CMS upgrade have been made more concrete as the TDRs have been completed. WP2 (tracker ASIC) and WP3 (now common back-end electronic hardware) have both developed specifications which have changed considerably from what was foreseen at the outset of the project.

The CBC ASIC was not originally expected to provide L1-trigger data and the original ideas for L1 trigger primitives from the tracker were much less ambitious than is now the case, driven by evidence from simulations that *full track finding* at L1 would be needed. Thus the chip has evolved to provide this data from 2S-modules, but also to maintain compatibility with ASICs for the PS-modules and those providing onward transmission of data off-detector, which are some way behind in their development. This has somewhat slowed the CBC development as well as increasing the complexity of the ASIC and the modules, and sub-components such as hybrids, which are needed to assemble working modules.

WP3 originally expected to focus on the Phase-II trigger in the final phase of the R&D, but without a clear picture of how this would differ from the present trigger system. With our success with time-multiplexing in the Phase-1 calorimeter trigger upgrade, it became clear that this concept had applications elsewhere, and a once contentious subject has become effectively the baseline in many discussions. Our progress with the MP7 and FC7 FPGA hardware showed that such boards were very flexible, and increased our confidence in our capabilities, including with firmware for algorithms and infrastructure, and led to the model of common hardware developments, rather than competing initiatives at the group or agency level. The prospects for this model of future hardware developments now look very promising.

The two more recent work packages on the HGAL and L1-track finding have been focusing their recent activity on implementations in the construction project. As such, their activities have used UK-hardware and firmware developments from the R&D as a solid foundation for further growth (and as entries to leadership roles in the relevant CMS projects). Both these WPs are firmly aimed at the construction project and not at developing new, unique components but at exploiting those which evolve from the common activity of WP3. Thus the milestones and deliverables are no longer self-contained within this R&D project, but reflect the longer term plans of CMS beyond March 2019 when this project ends.

These points are noted partly because of some repercussions. As already mentioned, the transition into the construction project is imminent and to allow that to proceed smoothly the final approval of the construction funding is needed. Another consequence is that activity in all areas is steadily increasing, with collaborative work with our international colleagues already at quite a high level – e.g. with tracker modules in beam tests, tracker DAQ developments based on FC7 hardware, and significant software development needed. Simulation studies for the L1 trigger, including the HGAL, are proceeding apace, evidently to be closely followed by algorithms in firmware. The design of the back-end systems for the tracker, of which the L1 track-finder is only one part, is now proceeding rapidly, and all these are based on collaborating with our CMS colleagues internationally.

The funds remaining for the final phase of the project seem to be sufficient, but some of them will probably be deployed slightly differently than originally foreseen. In particular, the travel budget is now under pressure, which was not really anticipated. After underspending compared to the plan in the early years, last year saw a major increase and it can now be seen as an inevitable consequence of our progress and success, and as a result of the increased activity as our work evolves toward the upgrade construction.

3 Work Package 1: Management

A reminder of the project management is included below. G. Hall remains PI, since January 2017 working 50%. G. Davies is now the UK CMS PI since January 2018. D. Newbold will be the PI for the CMS upgrade construction project, with funding requested to start from April 2019.

WP	Manager	Institute	Role
1	G Hall, PI	Imperial	Overall management, budgetary responsibility and supervising procurements, interface to UK CMS PI. Tracker Management Board member.
2	J Borg	Imperial	Overall responsible for CBC specifications, interface to module design team, chip testing and module evaluation.
	M Prydderch	RAL TD	Manager of ASIC design team in RAL
3	G Iles	Imperial	Based in CERN with responsibility for L1 calorimeter trigger operation, as well as future hardware development.
	J Brooke	Bristol	Supervision of UK trigger upgrade activities.
4	P Dauncey	Imperial	Jointly coordinating UK HGCAL developments, with G Davies. DAQ and L1 trigger coordinator for the HGCAL.
	G Davies	Imperial	Also, UK representative on the HGCAL IB and FB.
5	M Pesaresi	Imperial	Coordinating demonstrator integration activities, hardware/firmware specifications, and general project planning.
	I Tomalin	RAL PPD	Maintaining and running the Monte Carlo analysis software, tracking algorithms and oversight of RAL L1 track finder activities.

4 Work Package 2: Outer Tracker Readout

4.1 Objectives

- To complete the development of a readout and triggering chip suitable for the 2S-PT module, bringing the chip to a final state ready for mass production.
- To develop the hardware and software required for the large-scale production testing procedures, and to deliver tested wafers to the CMS experiment.
- To play a major role in construction, definition and evaluation of prototype modules.
- To contribute to development of ancillary chips required for the 2S-PT module, and to participate in the PS-PT module development.
- To contribute to the future large-scale module production programme, and to participate in integration and commissioning activities.

4.2 Progress

The CBC3 is the latest prototype of the 130 nm CMOS bump-bondable front end readout chip for 2S-modules in the outer silicon tracker. The previous version of the chip (CBC2) was very successful, allowing R&D on (the rather complex) hybrid technologies suitable for the construction of 2S and PS modules to progress, and proof-of-principle demonstration of the pT stub triggering approach in beam tests. As discussed previously, the CBC3, with its optimized front-end and enhanced stub logic has also been a success. Over the past year this circuit has been subjected to numerous tests, including analogue and digital tests, total dose irradiation and SEU studies, and tests of the hybrid modules, both stand-alone and with sensors, and most recently tests with particle beams of various kinds. The minor issues identified during these tests have now been addressed by RAL (discussed further in section 4.4). The design changes for the CBC3.1 were completed by the end of January 2018, and it was subsequently submitted for manufacturing. Very recent communication from the manufacturer indicates that we can expect delivery at the end of June.

In parallel the work to develop wafer test procedures continues, as does the work to refine the documentation. Our collaborators at CERN are currently finalizing the design of the first 8CBC3 modules, which should become available late 2018.

One of the main issues last year was the late delivery and low quality of the metallization for bumping of the CBC3 chips. A decision was taken by CMS to metallize both CBC3 and PS-module ASICs using an external manufacturer, as Global Foundries, who purchased the IBM foundry, seemed unwilling to provide the bump metallization service previously offered by IBM. PS-module ASICs are manufactured by TSMC in a 65 nm process and TSMC also could not provide the metallization service (in this case because incompatible wire-bond and bump-bond metallization are both required). Hence, CERN, who are responsible for hybrids and their assembly, saw an opportunity to evaluate other sources of the service to be used for both types of ASIC. PacTech, a German company, answered the (lengthy) tendering process with a bid and were selected. However, various problems occurred and the quality of the work was poor, including even incorrect tracking of known good die, which had been provided to them from our wafer probing results. Three of five manufactured (shared) CBC3 wafers were used (with two used only for setup purposes); only about 200 usable CBC3 chips were delivered from about 800 good die. (We would have expected almost 100% yield from IBM.)

The situation appears to have improved; a second order for metallized chips using 3 remaining wafers was delivered with significantly higher quality than the first lot. Nevertheless, because of these issues, the metallization of the wafers currently on order (24 CBC3 wafers and the CBC3.1 wafers) will instead be the responsibility of the semiconductor manufacturer (as was the case for the CBC2, where the bump quality was excellent).

After negotiation with CERN procurement services, Global Foundries have agreed to maintain the service which IBM previously offered, and it is expected that this will later be the case for production

wafers. The only difference from the past is that the metal is lead-free¹, which is an advantage because it has a lower melting point than leaded solder, which has allowed us to assemble hybrids at Imperial (Fig 4.1) using a reflow station designed for ball-grid array repairs. (Another source will be sought for metallization of PS-module ASICs.)

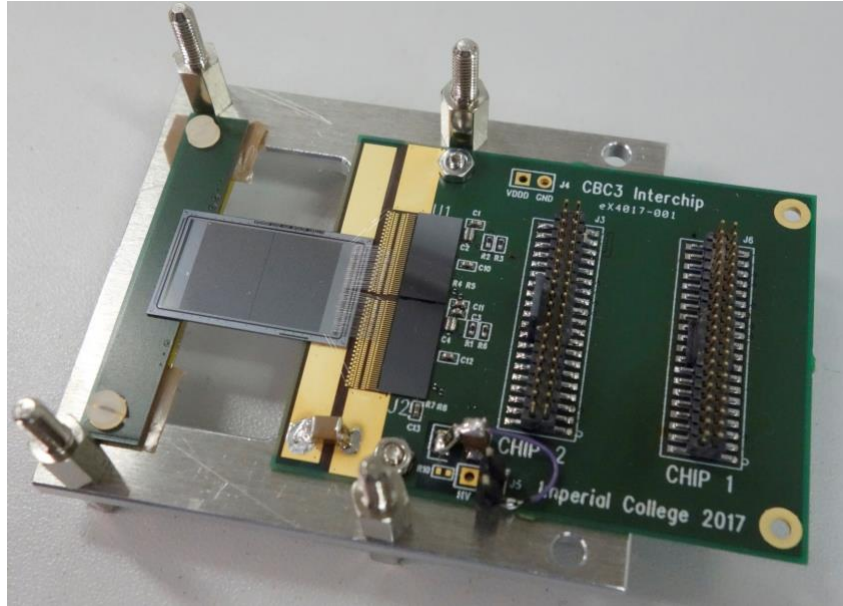


Figure 4.1. A 2CBC3 module with a single sensor, where the CBC3 were bump-bonded at Imperial College, using an in-house designed hybrid. This module was studied in a test beam in CERN in November.

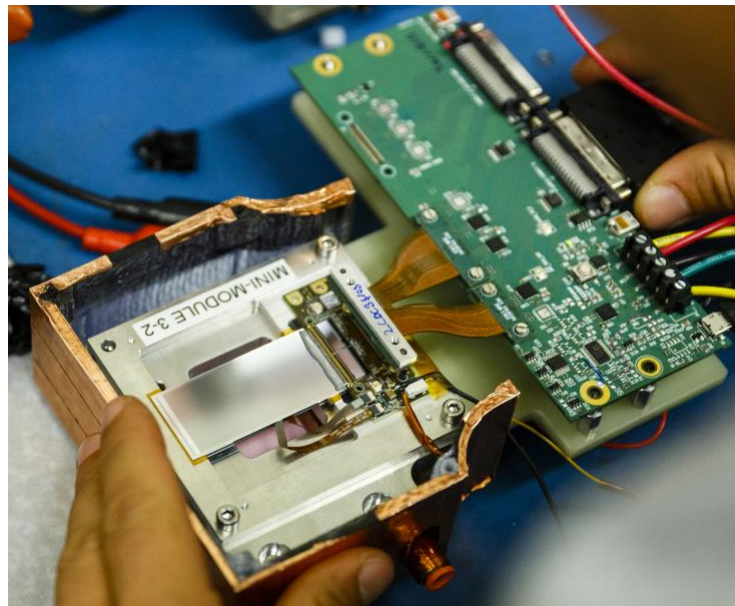


Figure 4.2. A 2CBC3 mini 2S-module used in the beam test in Fermilab in December 2017.

¹ Eutectic lead solder used for general electronic applications is typically 60/40 Sn/Pb with a melting point around 188°C. However, the CBC2 solder bumps used an alloy of 97/3 Pb/Sn with a melting point in excess of 300°C. Pure lead has a melting point of 327°C. The CBC3 bumps will be lead free, an alloy of 98/2 Sn/Ag with a melting point of 200-220°C.

Partly due to the problems with metallization, but also due to delays at CERN with hybrid design and procurement, the 2CBC3 modules were delayed, and only became available in November 2017 (Fig. 4.2), but in time for a successful beam test at Fermilab using 150 GeV protons.

4.3 CBC3 test results

Last time we reported on the completion of tests of the analogue performance, the digital functionality, as well as total ionizing dose and single-event upset robustness, and the resulting design changes. The continued testing has focused on verifying the 2CBC3 modules and tests in particle beams.

Tests of the CERN 2-sensor 2CBC3 module (fig 4.2) revealed an issue with some of the lines used for communication between CBC3 chips not being connected in the correct order. A RAL staff transition (when D. Braga left) meant that the inverted ordering of lines required at one side of the CBC was omitted. A correction on the module PCB is non-trivial and would have increased the cost of the hybrids significantly. Thus, since it required a minor design change, it was incorporated on the CBC3.1.

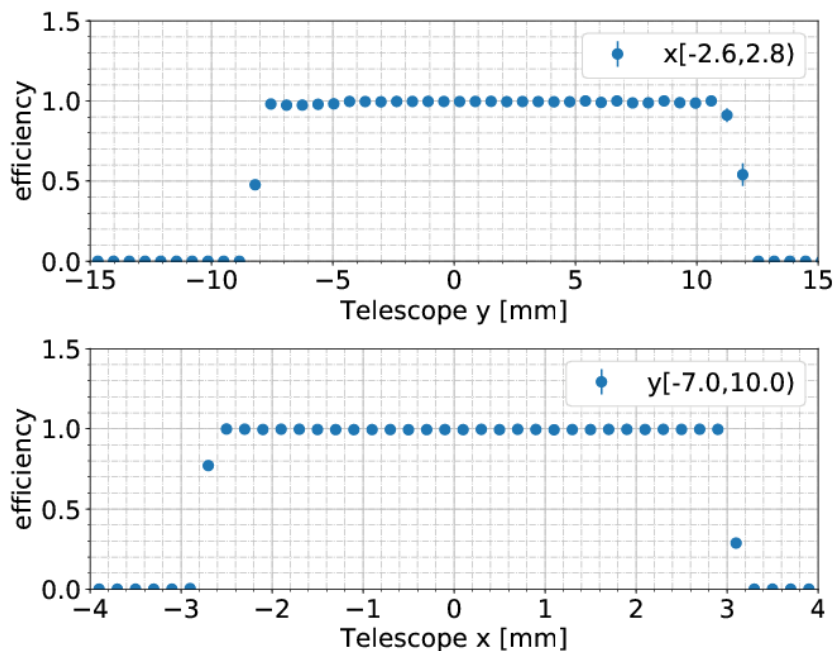


Figure 4.3. Hit detection efficiency of the CBC3 as a function of spatial position when operated with a small silicon strip sensor in a 180 GeV pion beam in CERN.

Tests of the CBC3 with particle beams were performed on different occasions over the winter, using beams of pions, protons and xenon ions. For example, Fig. 4.3 shows the detection efficiency of the CBC3 module built at Imperial when exposed to 180 GeV pions, and Fig 4.4 shows the (expected) effect of mistiming the sampling of the signal.

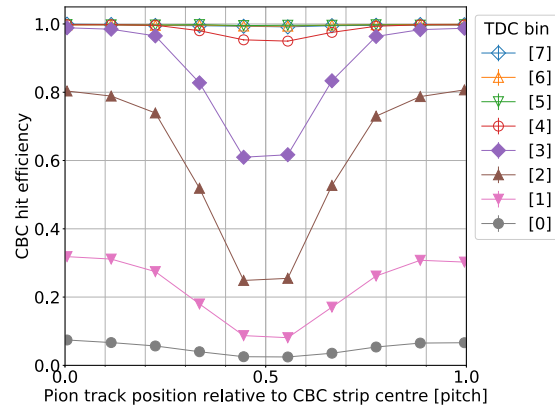


Figure 4.4. Hit efficiency with respect to the incident beam position relative to CBC3 strip centres, which are located at 0 and 1. Each set of data points has a different delay with respect to the Hit Detect signal. The data are grouped into 3.125 ns bins.

4.4 CBC3.1 design changes

During initial testing the CBC3 was found to output repeated stub addresses and bend codes for a few locations. Additionally, invalid stubs formed by clusters outside the correlation window were allowed to be output with an invalid bend code identifier. The relevant circuit has now been modified to remove the bad addresses and bend codes. The simulated results have been plotted so as to replicate the test results, to be confident that the issue has been corrected. The circuit has also been modified to reject stubs that have an associated bend code that is invalid. It has been simulated and presented to a design review including the Imperial team. Tests also showed an issue for the Parallel-In Serial-Out (PISO) circuit that outputs the L1 triggered data from the pipeline. This issue only arose for a few phase settings of the on-chip recovered 40 MHz clock, and only when triggers were spaced less than 1 μ s apart, indicating a timing issue. The PISO circuit was modified to improve timing robustness. Additional control functions that allow active clock edge selection for certain settings of the 40 MHz phase have also been added. This circuit has been thoroughly simulated and independently checked, and also presented at the design review.

The origin of the SEUs in the I2C registers experienced during the Louvain study in May was investigated. Simulations confirm the test results, and show that the cause is related to a single reset buffer in the register design. The registers have been modified to increase the threshold for upset on the reset line substantially.

Two I2C-controlled test circuits have been added to the chip in order to allow testing inter-chip digital inputs and outputs during wafer probing. The e-fuse circuitry has been modified to include a pull-up resistor on the power supply so that the 3V power line is never allowed to float to ground, which has an effect on reliability of the fuse detection circuit, especially under irradiation. The Fast Reset control signal has also been extended in time to ensure consistent reset of the L1 counter circuit.

Finally, some signals for communicating hits in neighbouring chips have been reordered, and delay circuits were inserted to improve the phase matching between the data lines from the CBC. After extensive simulations to verify the updated design it was submitted for manufacturing early 2018, with delivery of bumped wafers expected during the summer of 2018.

The overall conclusion is that, for such complex ASICs, small issues in the design do occur and extremely careful scrutiny is necessary at chip, module and even system level to identify them in a timely way and eliminate them. We are confident that this process is almost complete, with the remaining uncertainties expected to be resolved with the delivery of the CBC3.1, which should then be ready for large scale manufacture.

4.5 Staff on project

No recent changes.

4.6 Expenditure

The main recent expenditure has been on RAL TD staff working on implementing and verifying the required changes to the CBC3.1. Pending the CBC3.1 evaluation we expect a reduced expenditure in the future as the role of RAL shifts to support and documentation of the CBC3.1. However, verification of the CBC3.1 success will not be possible until autumn 2018. The working allowance would still permit additional TD staff effort if required, as well as further fabrication.

4.7 Deliverables

The WBS for WP2 is included below. Items 2.3 and 2.4 have been completed, but delayed compared to the original planning and have had an unavoidable knock-on effect on the schedule. The final goal to be ready for full-scale production by the end of the project involves a risk, which we believe to be small.

The delays have mainly been caused by late deliveries of the hybrids and modules and our inability therefore to sign off a fully tested module. There are actually other ASICs in the module schedule which are on the critical path for CMS construction, including especially a concentrator chip (CIC), which will be used by both 2S and PS modules. It is the responsibility of Lyon, and is in a 65 nm technology. This has been a concern to us for some time, but we have emphasized the importance of factorizing the CBC and CIC development. Since the operation and data flow from the CBC in the 2S-module is much simpler than that from the PS-module, this is possible, and has been accepted by CMS.

WBS item 2.5 refers to the CBC3.1 which we expect to be the final version, with no further iterations required. If successful, the masks for its manufacture should be those needed for production.

WBS item 2.6 has been separated, on the assumption that WBS 2.5 is successful. Final validation of the CBC3.1 requires modules to be assembled, and it is unclear whether this can be achieved within the duration of this project, as it depends on other ASICs and sensors being available, which is uncertain. However, we would not expect any further requests for CBC changes.

WBS item 2.7 is a contingency iteration in case of any unexpected remaining bugs. The remaining time is short, but any change is expected to be very minor to allow production masks to be finalised.

WBS item 2.8 has also been separated out. It belongs in part to the construction project but, given the pressures which are already emerging on the construction schedule, it is important to anticipate contracts and major procurements. Hence we have already instigated discussions of the schedule and milestones, partly because few people have experience of such procurements. Provided the CBC masks are finalised, it should be relatively straightforward to move to the production phase.

WBS	WBS L2	Start	Finish	Months	Task Description
2	Phase II tracker Readout	04/13	03/19	102	
2.1	system	04/13	03/14	12	definition of the CBC-based 2S-PT module readout
	2.1.1 specification definition	04/13	03/14	12	regular meetings with CMS collaborators to define overall system specification and interfaces
2.2	CBC2 test	04/13	03/15	24	CBC2 is final deliverable of the UK upgrade R&D
	2.2.1 CBC2 ongoing testing	04/13	03/14	12	complete the detailed studies of the CBC2 chip, including irradiation and SEU tests
	2.2.2 CBC2 2S-PT module prototype studies	04/13	03/15	24	a programme of SS-Pt module studies, in collaboration with CMS, including test beam
2.3	CBC3	04/14	03/16	24	CBC3 is specified for the final system
	2.3.1 CBC3 design	04/14	09/15	18	design period
	2.3.2 CBC3 production	09/15	03/16	6	production period
	2.3.3 test setup preparation	09/15	03/16	6	wafer and chip test setup preparation
2.4	CBC3 test	03/16	03/18	24	CBC3 chip and module testing
	2.4.1 early tests	03/16	09/16	6	chip verification tests to prior to module tests
	2.4.2 ongoing testing	09/16	03/17	6	complete characterization, including irradiation and SEU tests
	2.4.3 CBC3 2S-PT module studies	09/16	03/18	24	CBC3 based module studies in collaboration with CMS in lab and test beam
2.5	CBC3.1 design and test	09/16	12/17	15	CBC3.1 is the final version of the chip, fixing any remaining bugs found in the CBC3
	2.5.1 CBC3.1 design	09/16	12/16	3	design period
	2.5.2 CBC3.1 production	01/17	06/17	6	production period
	2.5.3 CBC3.1 testing	07/17	12/17	6	tests to verify full and final functionality
		07/17	11/18	3	expedite functionality tests
2.6	Final validation	12/18	04/19	4	
	CBC3.1 2S-module	12/18	04/19	4	
2.7	CBC3.2 iteration	11/18	04/19	5	Only if correction is required
	2.7.1 CBC3.2 final masks	12/18	01/19	2	mask preparation for full wafer engineering run
	2.7.2 CBC3.2 engineering run	02/19	08/19	6	production period
	2.7.3 CBC3.2 final production	09/18	12/18	3	final verification in post project period
2.8	Production planning				
	2.8.1 procurement planning	01/18	04/19	15	detailed plans for mass production

5 Work Package 3: Level-1 Trigger

5.1 Objectives

- Improvement of the current CMS calorimeter trigger in preparation for above-design-luminosity conditions.
- Provision of infrastructure to allow testing of an entirely new calorimeter trigger in parallel with the existing system.
- Design, construction and testing of a time-multiplexed hardware trigger for CMS, capable of implementing new and more selective algorithms.
- Design of a track trigger architecture for HL-LHC running, and construction of a technology demonstrator.

5.2 Progress to date

5.2.1 Phase I trigger operation

The Phase I upgrade to the Level-1 trigger has been running successfully since May 2016. Since our last report, the system has been operating smoothly and reliably with negligible contributions to downtime or data marked as bad.

The final components of the data quality monitoring system for the Phase I calorimeter trigger have been commissioned, including performance monitoring via comparisons of offline reconstructed objects with L1 trigger objects, as well as validation of the trigger data processing by comparison with offline emulation. In addition, a software framework for prompt analysis of the trigger data in case of unexpected problems has been developed, completing the suite of tools required to operate the trigger system for the rest of its lifetime.

There have been changes requested for the Heavy Ion run in November this year. While some changes are small software changes other are more complex and will require firmware effort to make the modifications.

5.2.2 Next generation hardware development

The first set of prototype cards (v1) for the Serenity ATCA platform have been delivered and are under test. It is worth noting that manufacture took 3 months - 8 weeks for PCB manufacture, 4 weeks for assembly and 1 week for shipping. The lengthy period can be partly attributed to the Christmas break and some of the new challenges faced by the assembly company (e.g. specialised jig required); however, it is significantly more than the ~6 weeks that is normally allocated for manufacture.

Testing has proceeded well and most of the basic functionality is up and running – power, communication and low-level control (and continues to progress rapidly as this report is being written). The FPGA processing units have yet to be tested, but that is expected in the coming days as soon as the power sequencing is verified. In parallel, the firmware and software infrastructure has been developed using the MP-Ultra and commercial development cards. The Q1 2018 milestone for a preliminary firmware and software stack (build tool, slow control and documentation) for Xilinx UltraScale devices was met. At present we seem on schedule to deliver Serenity prototype v1 at the end of Q2 2018 alongside basic infrastructure (i.e. slow control and payload only), but there is little margin.

5.2.3 Plan for 2018-2019

Our plan over the next year is to equip ourselves and our collaborators with the Serenity platform, including processing sub-units and optical links. There will be cards for ourselves at Imperial, RAL and CERN, plus a common integration/development area in the existing Tracker Integration Facility at CERN. Cards will also be distributed to our key collaborators so that they can expand and test the capabilities of Serenity (e.g. testing of an additional processing sub-unit at KIT and timing analysis at Saclay), as well as develop algorithms for the projects we are involved in (e.g. HGCal firmware by

TIFR). Some locations, such as the Tracker Integration Facility, will have multiple Serenity cards, but populated with different optics and processing units, depending on the target application.

Significant testing of the Serenity hardware is already complete and thus the plan is to fix the few bugs and produce 20 cards (v1.1), which will preferably commence before the summer shutdown at some of the manufacturing facilities. A first batch of 3, perhaps 5 cards would be delivered in October, with the remaining cards in January. Some of our own facilities would need to be equipped with ATCA crates, but most would use our benchtop adapter unit, which avoids the cost of additional crates and provides better access for debugging.

Our final milestone is to provide a v2 prototype (renamed v1.1) with full firmware & software infrastructure set (i.e. slow control, payload, link and diagnostics) at the end of Q2 2019. This may be quite challenging to meet because much of the effort that would normally be available may be devoted to algorithm development – both software simulation and firmware implementation, in addition to the changes required for phase-1.

A summary of the plan is given below in tabular form, along with the expected costs of the major components. We intend to share the boards where appropriate with collaborators, both to expedite progress but also to cement this model of development and ensure that everyone is committed to it, as there is an inevitable risk that other groups may prefer to compete, rather than collaborate. At present, partly because of excellent UK progress, this risk seems slight and there are no visible alternatives at present. Where boards are delivered outside the UK groups, we expect to be recompensed, or balance our contribution against reciprocal expenses.

The most visible risk to hardware delivery is the failure to have the v1.1 PCBs manufactured before the summer shutdown, which could potentially add a 2-3 month delay to the project. This in turn is dependent on testing being complete and the necessary revisions having been made to the design. The remaining risk is more technical (i.e. we encounter some unexpected issue that needs to be addressed). It is harder to quantify but would almost certainly require design changes and thus a similar delay (i.e. 3-6 months).

Date	Deliverable
May 2018	All electrical and optical testing complete. Revised design – v1.1 ready for manufacture.
June 2018	Basic firmware and software infrastructure (i.e. slow control and payload only)
July 2018	PCB manufacture complete Preliminary results from thermal mock-up and simulation
Sep 2018	Assembly of 3-5 base and daughter cards complete Preliminary results from mechanical mock-up
Nov 2018	Validate v1.1 Cards
Jan 2019	Assembly of remaining base cards and daughter cards complete
Mar 2019	Full firmware and software infrastructure (i.e. slow control, payload, link and diagnostics)

	Cost (£k)
Card manufacture, including components and assembly	83
FPGAs	66
Optical Components	33

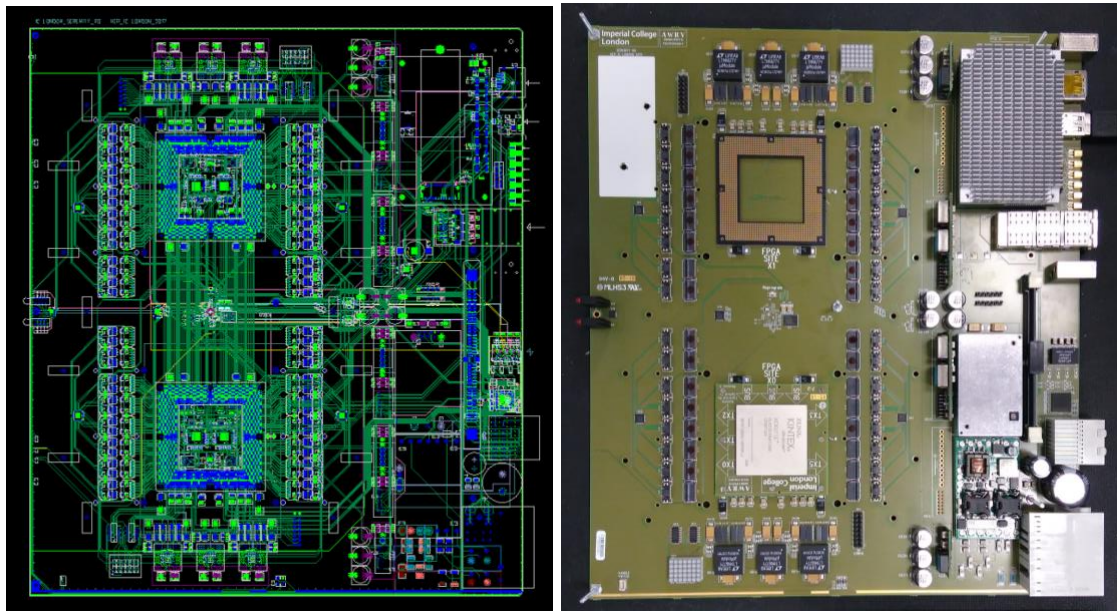


Figure 5.1. Left: The PCB layout of Serenity. The two large mounting sites for FPGA daughter cards are clearly visible, as are the optical engine mount points on either side (blue columns). Right: Serenity after manufacture with bottom FPGA site populated, but optics unpopulated.

Some of the issues now under study will have potential repercussions in the longer term but the new hardware will soon allow us to make even better informed comments on potential difficulties which may be encountered. CERN will have a major responsibility in maintaining and operating off-detector electronic systems in CMS and naturally has already dedicated efforts to study issues involved in locating and operating them in the underground areas. Following some of these studies, CERN felt strongly that CMS should adopt the ATCA format.

Our concerns about the cooling of ATCA systems mentioned in the last report remain. The most challenging aspect is ensuring that the optical modules remain at less than 50°C and ideally less than 40°C to have a reasonable lifetime. While we expect that this can be achieved for 16 Gb/s systems it becomes increasingly more difficult as the link speed and power dissipation increase (e.g. the optics required to use the newer Xilinx Ultrascale parts at 28 Gb/s). The topic was discussed at xTCA user's forum at CERN, but at present few participants wish to consider alternatives. The situation is made more complex because the electronics must operate 100 m underground with limited space and primary cooling systems that have their own constraints.

Thermal simulations of the ATCA card by Karlsruhe Institute of Technology (KIT) indicate that a potential problem does exist. To validate the simulation a mock-up of the card is being created that will use kapton heaters (thin, flexible PCBs) to dissipate power in a similar manner to the real optics and FPGAs. The heaters and thermal test cards have already been manufactured and a sensor data logging system assembled at CERN with the help of INFN, Italy.

The other problematic issue with ATCA is the large amount of power devoted to fans (up to 20%) and significant noise they generate (significantly more than 85 dBA – the legal limit before noise mitigation solutions are required). The current proposed solution for those underground in USC is to wear dedicated headsets for ear protection, to communicate with colleagues and to hear alarms. For all the reasons above, we shall continue to keep cooling options under review because we need to make sure that the full system, which will involve many crates, is a viable option for the underground service cavern.

The second area of concern is the availability of high bandwidth, high density mid-board optics (i.e. placed close to the FPGA for optimal signal integrity), which is a niche product. At present we are reliant on a single supplier and we would like to lessen that risk by looking at alternative companies. This would potentially require that another version of the Serenity card should be manufactured.

There are some issues about how this activity should evolve and be managed, which mainly concern the construction project from April 2019, rather than the remaining R&D activity. While the common hardware development has generated enthusiasm in CMS, as an activity spanning multiple sub-detectors, it does not have a very specific mandate and may prove challenging to coordinate in the long term. At present, the two main issues are:

- the technical choices facing the UK for Phase-2 back-end systems and the timely delivery of the technology for our own interests - i.e. tracker, HGCal and L1-trigger.
- the wider international context, in which we form a collaboration to provide additional support to the Serenity platform and encourage others to develop common solutions to the hardware, firmware and software tasks facing us.

A bi-weekly meeting has been held since November 2017 to coordinate the activities between the international groups contributing, and has been working well. It has led to a common code repository and associated documentation. It has ensured that the Q1 2018 milestone for a preliminary firmware and software stack was met on schedule. The group is now active in extending the firmware/software stack for the Q2 2019 milestone, developing additional daughter cards (TIFR & KIT) and investigating the thermal aspects (INFN).

5.3 Overview of CMS plans

The Phase-2 L1 Trigger Interim Technical Design Report was approved by the LHCC in November 2017. The submission of the document was led by J. Brooke (Bristol) and R. Cavanaugh (UIC/FNAL), but both are now near the end of their terms. The TriDAS IB have proposed that A. Zabi (LLR) and J. Berryhill (FNAL) lead the next phase of project, which will lead to the publication of a full TDR at the end of 2019. The MB will be asked to endorse the candidates in May.

The main focus of the interim document was a baseline specification of the interface between sub-detectors and the central L1 trigger. Options for the architecture of the future L1 trigger were also presented, including the use of time-multiplexing based on the success of the Phase I calorimeter trigger. The document also describes progress on trigger algorithms, including the use of “particle-flow” techniques, whereby individual particles are reconstructed using the full detector information.

For the upcoming TDR milestone, the key decisions required include finalisation of the processor specification, system architecture, and baseline algorithms. These will be informed by ongoing algorithm studies, using both physics simulation and firmware emulation, as well as hardware R&D. Good progress is being made on all these fronts, and we do not anticipate problems meeting the milestone. In particular, good progress has been made in showing that particle-flow techniques are feasible and profitable in the L1 trigger, within the constraints of bandwidth, firmware resources, and latency.

Plans for UK contributions to the Phase II trigger have been consolidated, focusing on the Correlator system, where central tracks, calorimeter clusters, and muon tracks are matched to form the final physics objects used in the L1 trigger decision. We will collaborate with US institutes (FNAL, UIC, MIT) and CERN, on the correlator hardware and particle-flow algorithms, and are in the process of building this collaboration. We will contribute to the core particle-flow algorithms via vertex identification, as well as identification of jets, energy sums and electrons. The UK is already contributing to Correlator design studies, with a focus on vertex identification; milestones are described later.

The optimal hardware configuration for the Correlator will ultimately depend on the choice of algorithms and how they are implemented. A series of workshops will be held to determine the optimum Correlator configuration and to discuss the simulations and implementations of the Phase-II Level-1 algorithms. The first of these workshops will be held at Cosener’s House, Abingdon, UK in mid-June this year.

5.4 Staff on project

There are no staff changes.

5.5 Expenditure

Overall spending is within the budget foreseen.

5.6 Deliverables

The original milestones for the long term trigger R&D were defined at the outset of the project well before the present picture evolved and, in particular, the possibilities for common hardware developments, some of which were not foreseen, such as the L1 track finder and the HGCAL. The milestones which are listed below were proposed for the remainder of the project. The overall objective is to be compatible with the proposed schedule of the UK CMS construction project and the overall CMS sub-detector milestones.

For the hardware development:

- Q1 2018: preliminary Firmware Software Stack for Xilinx UltraScale Devices (build tool, slow control and documentation).
- Q2 2018: prototype v1 hardware available with basic infrastructure (i.e. slow control and payload only).
- Q2 2019: prototype v2 (now called v1.1) hardware available with full infrastructure set for prototype card (i.e. slow control, payload, link and diagnostics).

For the development of the system design: the CMS milestones for this activity during the remainder of the grant period are to benchmark the simulated performance of selected algorithms by Q2 2018, followed by the full suite of baseline algorithms by Q1 2019, in preparation for a hardware demonstrator programme. The UK will focus on vertex and jet performance for the Q2 2018 milestone, then expand to include energy sum and electron identification for Q1 2019.

- Q2 2018: benchmark performance of selected algorithms.
- Q1 2019: benchmark performance for all core algorithms.

Work Package 4: High Granularity Calorimeter

6.1 Objectives

- To complete the testing of the UK parts of the design for the front-end electronics HGCROC ASIC.
- To play a long-term leading role in the HGCAL, in terms of both overall project management and technical aspects, specifically in the two areas listed below.
- To develop the trigger primitive generator (TPG), including contributing to the algorithms, firmware and HGCAL-specific hardware.
- To study the physics performance of the HGCAL and optimise the design parameters and, in addition, develop the reconstruction techniques to provide the best overall performance.

6.2 Progress to date

The HGCAL Technical Design Report (TDR) was submitted last November, just after the previous OSC meeting. Since that time, the TDR has been reviewed at CERN, first by the LHCC (for the technical aspects) and following this by the UCG (for costs, management, schedule and risk). These reviews lasted from December 2017 to April 2018. The recommendations have not yet been approved by the CERN RB and so are not public, but the HGCAL project can be considered approved.

The UK work on the front-end electronics has continued since the last OSC meeting. A UK engineer (J. Borg) designed a low-power (<1 mW) 50 ps resolution TDC circuit for digitizing the time-over-threshold (TOT) signal based on gated ring-oscillators. This circuit was included on the HGCROC V1 ASIC which was returned from fabrication in December. A test PCB was designed and Borg has been testing the TDC performance for the last two months. These tests show the TDC is working correctly and this design would be a viable choice for the final ASIC version. It is likely this would have to be picked up by non-UK groups, because in the CMS-UK Phase II upgrade proposal, due to funding constraints, we have chosen to restrict future UK HGCAL effort to the two remaining topics described below.

The LHCC and UCG reviews raised no significant issues related to the HGCAL back-end hardware. These boards will be based on the common hardware, for which the status has been described under WP3. As such, there has been excellent progress but none of this is HGCAL-specific. We expect to start on technical firmware developments for the HGCAL itself during the next six-month period.

Hence, most of the HGCAL trigger work since the last OSC has focused on improving the simulation performance. A very significant development was a new 2D clustering algorithm, which forms shower clusters in each layer from the raw trigger cells. The previous algorithm was found to be sometimes forming very large clusters, particularly near the inner edges of the HGCAL, due to adding many overlapping background (pileup) deposits to the signal cluster. The weighted average position of the total cluster was then very far from the signal cluster, causing the 2D cluster to be missed and hence significant energy to be lost in the overall 3D cluster. The 2D algorithm was changed to limit transverse cluster growth, which fortunately will also make it easier to implement in firmware. This change improved the background rejection significantly for both electromagnetic and jet clusters without any impact on signal efficiency; “before and after” plots are shown in Figure 6.1.

The UK work on simulation and reconstruction had concentrated on calibration methods and detector optimisation, both of which were crucial topics during the review. The UK leadership in these areas meant UK personnel gave these presentations throughout. The next big study for detector optimisation is to look at the changes in performance with variations of the thickness of the absorber

material between the sensitive layers. This is critical to finalise the mechanics design and is expected to take the next nine months.

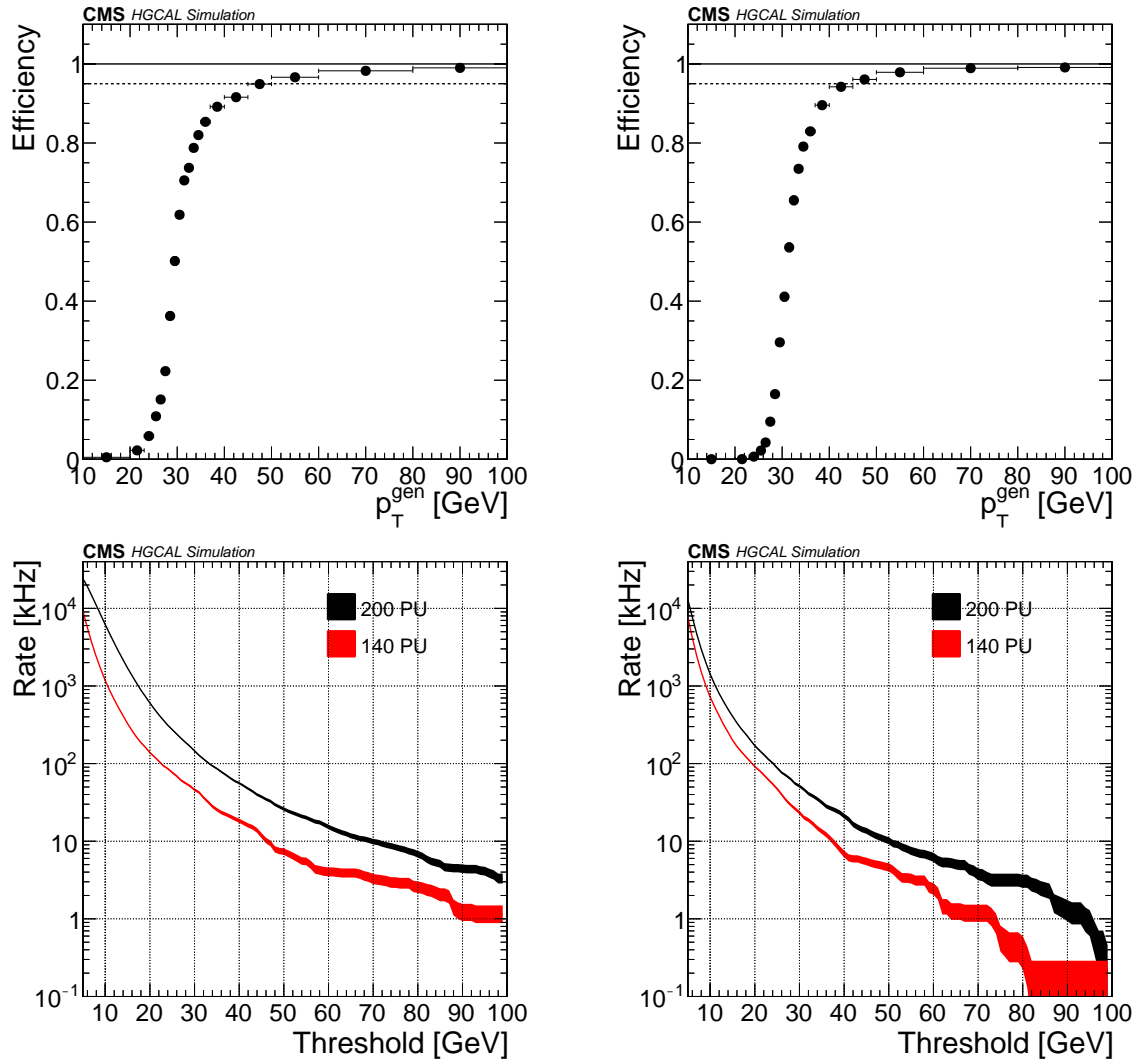


Figure 6.1(a). L1 trigger results for electromagnetic objects using old (left) and new (right) 2D clustering in the presence of an average pileup of 200 events. Top: efficiency with a trigger threshold of $p_T = 30$ GeV. Bottom: background rates as a function of trigger threshold.

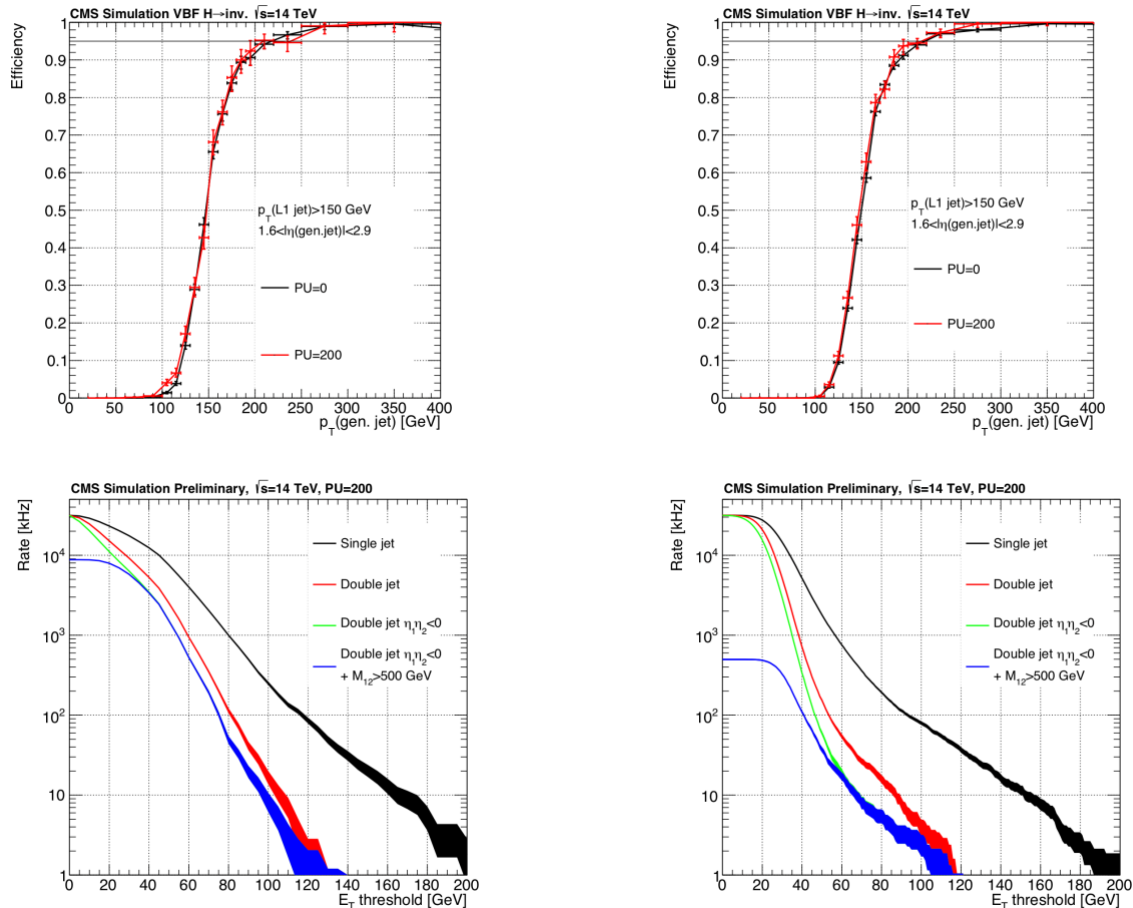


Figure 6.1(b). L1 trigger results for jet objects using old (left) and new (right) 2D clustering in the presence of an average pileup of 200 events. Top: efficiency with a trigger threshold of $p_T = 150$ GeV. Bottom: background rates as a function of trigger threshold for single and double jet triggers.

6.3 Overview of CMS plans

The production and successful review of the HGCAL TDR was a very significant milestone for the project. We now need to look ahead to the next major milestone, namely the Engineering Design Review (EDR) in July 2020. The UK will be heavily involved in documenting the back-end electronics designs for this review, as well as producing new and updated simulation results. Prototypes of boards for both the DAQ and TPG applications will need to be tested thoroughly (including the interfaces to the other systems such as central DAQ and L1T) in time for this review.

6.4 Staff on project

There have been no personnel changes in the HGCAL-UK effort since the last OSC.

6.5 Expenditure

Expenditure so far has been almost entirely on staff, and on travel to a lesser extent, mainly using non-project (ERC and PRD) funds. However, this is beginning to change as the HGCAL funds have contributed to the prototypes of the common hardware baseboards and in future will contribute to the HGCAL-specific daughterboards. The latter will be relatively expensive, as they will each hold a large FPGA (Xilinx Ultrascale+ VU9P). We foresee around £50k from the ERC grant being spent on these components plus some infrastructure required for testing during 2018.

6.6 Deliverables

These are as follows for the three areas in which the UK is involved:

- The main remaining UK deliverable for the front-end electronics work is documenting the evaluation of the Imperial-designed TDC implemented in the HGCROC V1 ASIC.
- Over the next year, the main deliverable for the TPG is the manufacture and testing of a generic baseboard and daughterboard to produce a functional prototype of the TPG board.
- The main near-term deliverable for the UK within the simulation is the detector optimisation study of the mechanical layer thicknesses.

All pre-TDR HGCAL milestones defined up to November 2017 were achieved. The HGCAL future milestones cover the detector construction from January 2017 to December 2025. There are no explicit milestones yet for the future simulation work. The full list of TPG high-level milestones are shown in Figure 6.2. The main near-term hardware milestones relevant to the UK effort are:

- Medium level: Prototype board hardware, firmware and software basic validation in April 2019. This is the next significant milestone for the TPG project. To meet this, we aim to have a functional prototype assembled before the end of 2018. Note, this milestone is just after the end of the current STFC upgrade R&D grant.
- High level: Prototype board functions and interfaces validated in October 2019. To meet this, all I/O from the HGCAL-specific board, including those to the DAQ and L1T, will need to be checked. Fulfilling this milestone will allow us to document the design for the EDR review in 2020.

TPG and back-end electronics (BE)		
Prototype functions and interfaces validated	CE.BE.4	07-Oct-19
Specification of BE system documented in EDR	CE.BE.5	20-Apr-20
Preproduction functions and interfaces validated	CE.BE.6	01-Nov-21
BE hardware production readiness review	CE.BE.7	11-Jul-22
Production functions and interfaces validated	CE.BE.8	25-Dec-23
BE electronics production complete	CE.BE.9	23-Dec-24
HGCAL integration with central DAQ and L1T complete	CE.BE.10	30-Dec-25

Figure 6.2. High level milestones of the HGCAL Backend electronics project.

7. Work Package 5: L1 track finder

7.1 Objectives

- To design the architecture and technological implementation of a first-level track finder for the CMS Phase II upgrade.
- To demonstrate and document a prototype track-finding system, as required for CMS review purposes, design reports, and integration exercises.
- To generate a construction plan for the CMS track finder and readout system, including any R&D required for final implementation decisions.

7.2 Progress to date

While the original objectives of this WP have been met, the UK continues to build upon the concepts and results presented to date in preparation for the anticipated construction project.

As recorded in a previous report, by December 2016 the UK had successfully demonstrated an FPGA-based system, based on MP7 hardware, for reconstructing tracks from the future Phase II tracker within a latency requirement of 4 μ s, such that they could be used as input to the L1 trigger decision. The priority for this WP is now to ensure that this demonstration can be ported to next-generation (Ultrascale) FPGAs, based on the prototype hardware under development in WP3. In parallel the UK continues to refine and improve upon the track finding reconstruction algorithms deployed, adapting to the evolving hardware design where necessary. Progress since the last report and active areas of work can be summarised as follows:

- Publication of a paper describing the UK-led demonstrator, system design and results <https://doi.org/10.1088/1748-0221/12/12/P12019>
- Adaptation, improvement and optimisation of the demonstrated algorithms and firmware, ensuring compatibility with the latest tracker geometry (tilted barrel), system design (9 detector regions x 18 time-multiplexed nodes), architectural constraints (detector cabling, CMS-wide system constraints) and infrastructure constraints (defined by WP3 firmware developments).
- Porting of demonstrated algorithms to higher frequencies (from 240 MHz to \leq 480 MHz); taking advantage of Ultrascale enhancements over previous generations of FPGA, and increasing processing margin in the system (fig. 7.1).
- Porting of key elements in the algorithm firmware to use the Xilinx High Level Synthesis (HLS) language; enabling faster development turn around, easier validation against simulation and potentially faster and smaller logical implementations (e.g. Kalman Filter).
- Contributions to development of software tools used by the CMS L1 track-finding community.
- Refinement of the Tracker off-detector architecture, system and hardware specifications.

7.3 Overview of CMS plans

The reorganised CMS working group structure presented in the previous report is now established, bringing together institutes previously working on the various track finding approaches, alongside others with commitments to the wider off-detector data processing system.

The ‘top-level’ Data Processing WG (P. Wittich [Cornell], F. Hartmann [KIT]) is responsible for interacting with a CMS committee tasked with ensuring the FPGA-based approach is sufficiently robust under non-standard operating conditions. It is expected that these robustness tests will be concluded within six months, after which this working group will disband.

The ‘lower-level’ System Development WG (M. Pesaresi [Imperial], K. Hahn [Northwestern]) is responsible for defining the system architecture and carrying forward hardware design of the different processing boards in the off-detector system, as well as organising the software and firmware effort

required both for the algorithms and for the overall system infrastructure. The initial focus of the group has been on planning towards the construction project, and accelerating the pace of development on the hardware R&D in order to meet the group’s first major milestone of defining the system specification towards the end of 2019.

Part of the effort towards a system specification definition implies the adoption of baseline track-finding algorithms, both for performance studies with other CMS subsystems (e.g. L1 trigger) and for proof-of-concept demonstrations. As such, a strong focus for the project this year is to seek convergence amongst the remaining track finding algorithm developments and this is being directed via a dedicated task-group (I. Tomalin [RAL], L. Skinnari [Cornell]) representing the existing concepts.

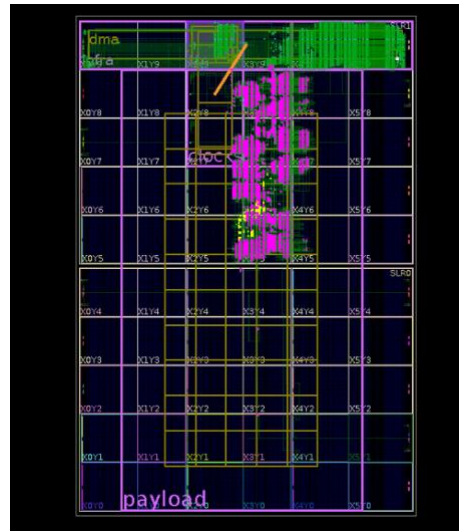


Figure 7.1. Implementation of one of the demonstrated algorithm sub-blocks (pink) in a KU115 design with infrastructure and services blocks derived from WP3 (green).

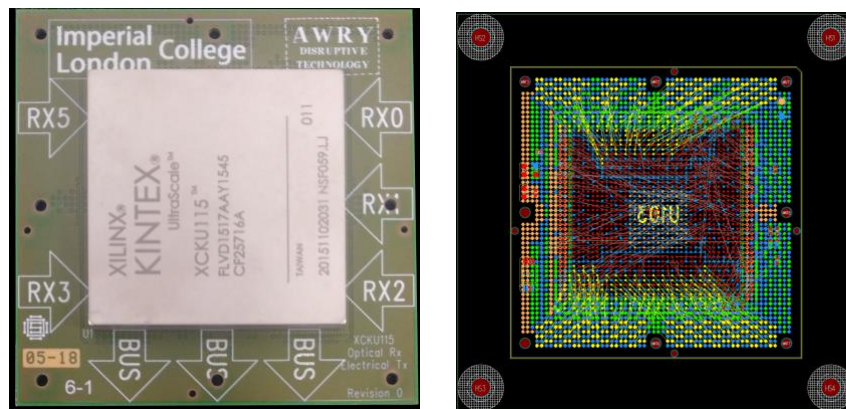


Figure 7.2. Left; The KU115 daughtercard (Imperial), and Right; the KU15P daughtercard under development (KIT), both of which can be deployed on WP3 hardware for demonstration of track finding systems.

A workshop organised by the System Development WG and hosted at RAL (Cosener’s House) took place in February 2017 to directly address the priorities for 2018, and to organise and direct effort within the group to the areas in need. It was well attended, with participants from all interested countries, and succeeded in its aims to kick-start joint activities, according to the project plan defined by the WG. These include studies of thermal loads on ATCA hardware, evaluation of alternative

optical transceiver modules, discussion and definition of on-board control and auxiliary processing requirements, development of common software and tools to support algorithm development, as well as development of hybrid track finding solutions and simulation tools.

At the end of 2017, the Tracker Upgrade TDR was approved by the CERN RB after LHCC and UCG review. This process included approval of the construction plan for the CMS track finder and readout system, as defined and presented by the System Development WG conveners. The most relevant upcoming CMS-wide milestones for the project are the Outer Tracker EDR and the L1 TDR submission, both in March 2020. The UK will be involved in documenting the back-end electronics designs in preparation for these milestones, as well as producing updated simulation results for the L1 track-finding system.

7.4 Staff on project

As mentioned in previous reports, most effort has been transferred from WP5 to WP3, profiting from the significant overlap in hardware R&D between these two WPs. Both M. Pesaresi and I. Tomalin continue to devote the majority of their time to WP5, with support from C. Manolopoulos, T. James and S. Summers. Both James and Summers completed their PhDs on the L1 Track Finder this year and are now funded on short term posts until the end of the grant. An STFC-funded PhD student started in January 2018 at Brunel working on FPGA firmware.

Several people outside the UK remain active on the project. This includes a strong collaboration with KIT, particularly in the fields of firmware and hardware development.

7.5 Expenditure

Some travel expenditure has been incurred on meetings in CERN and the UK, including the workshop at RAL.

7.6 Deliverables

The new deliverables list, as set out in the previous report after Tracker Management approved the FPGA-based L1 track finding solution, is listed below. Blue font means complete. These milestones are consistent with CMS project planning as defined by the System Development WG.

Milestone Date	Description
16Q4	Presentation of demonstrator at CMS internal review
18Q4	Demonstration of track-finder elements using Ultrascale FPGAs
19Q2	Demonstration of the track-finder chain using Ultrascale FPGAs

The main focus for WP5 this year is to demonstrate that the track finding algorithms under optimisation can be ported to the Xilinx Ultrascale architectures. The FPGA under consideration for the Track Finder Processor (TFP) is the Kintex Ultrascale KU115, where a daughtercard has already been produced for the ATCA base-board, as described in WP3 (fig. 7.2). For the Data, Trigger and Control (DTC) card, as the first stage in the track finder chain, the Kintex Ultrascale+ KU15P FPGA is being considered. A daughtercard for this FPGA is currently being designed by our collaborators in KIT. Gaining experience with both Ultrascale and Ultrascale+ architectures at this early stage will be important for defining the system specifications at the end of 2019.

All necessary infrastructure firmware and software required to wrap the algorithms for testing and demonstration needs is provided as part of WP3. On the other hand the ability to run and test realistic algorithms in WP5 is already proving useful to help advance and validate the infrastructure development in WP3.

8 Risk register

The risk register has again been reviewed and revised. No new risks have been added, or any retired. However, minor adjustments have been made to several risks to adapt them to the realities of the schedule. For example, risk 3.2 now includes delays in the ASIC foundry, and risk 8.3 refers to the laboratory move in the Imperial Physics department, which is ongoing but should not interfere significantly with the work of WP2 given the foundry delays. Minor changes have also been made to the likelihood and impact of some risks, but the overall picture is not much changed.

9 Finances

Expenditure is reported in the usual financial table.

As reported before, RAL PPD staff costs are somewhat higher than originally expected.

As discussed in the last two OSC meetings, £100k of the Working Allowance was used to cover extra TD staff costs for the remainder of the project. Provided there are no significant design changes after the CBC3.1, the remaining TD expenditure should be quite small. As mentioned earlier, travel expenditure in the last year was higher than foreseen, partly because of work carried out on L1 track finder activities. There is no other travel budget than that for upgrade R&D but the extent of this activity was not foreseen at the outset of the project. After discussions with STFC office, it was previously agreed that overspends on travel and TD staff will be reconciled against equipment underspends at the end of the project.

We have made estimates of the major items of expenditure remaining, using current exchange rates, which preserves much of the working allowance for the present, until the situation with the need for more TD staff effort is clearer. Note that the difference between funds available and required must also cover the £140k already effectively transferred to TD effort and travel.

Note that additional expenditure mentioned for the HGCAL from the ERC grant are not included in these estimates, as the ERC funds are expected to be applied to subsequent HGCAL-specific prototyping after this grant, such as for dedicated high-range FPGAs or board manufacture.

Item	£k	Comment
CERN expenditure in pipeline	19.2	To be invoiced soon
Commitments at Imperial	35.5	
CBC_final	296.5	NRE and at least 12 wafers: CORE
Ultrascale development	185.0	budgeted
Total required	536.2	£805.2k available

10 Gantt charts

Most of our work now aims to match overall CMS, or sub-detector, planning. The schedule included in the tracker TDR has recently been revised to take account of a few issues which had arisen. These include a significant delay in the design of the CIC ASIC, which is crucial for both 2S- and PS-modules, and some other delays, as well as an assumption about the installation date of the pixel system which was too early. It already illustrates some of the pressures which will arise soon, as modules must be completed before the major orders for components can be placed.

While the CBC is unlikely to be affected by any possible problems which arise elsewhere, there must be a decision about when large scale production orders can be placed and thus when wafers will first be delivered to Imperial for testing. Even if some parts of the schedule, such as module assembly, can be compressed, it is not desirable, or probably even possible, to expedite ASIC testing significantly. We had foreseen a testing period of about two years, with a throughput of about 500 wafers, testing one complete wafer per day. However, if other components are not as ready as the

CBC, which is certainly the case at present, it is not clear at what point the authorisation for the CBC orders will be given by CMS (and the funding agencies, at least indirectly).

For the completion of this R&D project, this is not a great concern, but it will become more important for the construction project, starting in 2019. We have already been pressing this point in internal management discussions to achieve a clearer common understanding.

11 Milestones

The deliverables from each work package are listed below. The milestones which were due have been highlighted in red font, or those met in blue. We have identified M3.6 with the delivery of the Ultrascale prototypes.

For reference, the reporting date of May 2018 corresponds to PM62.

Deliverable	Date	Description	Rev.Date
M2.1	PM12	System specification document produced	PM12
M2.2.1	PM12	Documented CBC2 detailed test results	PM12
M2.2.2	PM24	Documented 2S-PT module results	PM24
M2.3.1	PM12	CBC3 ready for production	PM39
M2.3.2	PM18	CBC3 produced & test setups ready	PM42
M2.4.1	PM24	Documented early CBC3 test results	PM45
M2.4.2	PM30	Documented CBC3 detailed test results	PM48
M2.4.3	PM60	Documented CBC3 2S-PT module results	PM66
M2.5.1	PM42	CBC3.1 ready for production	PM58
M2.5.2	PM48	CBC3.1 produced	PM66
M2.5.3	PM54	Documented CBC3.1 test results	PM72
M2.6.1	PM60	Final production masks prepared	PM66
M2.6.3	PM69	CBC3.1 ready for mass production	PM72
M2.7.3	PM72	First production modules available	***
M3.1	PM9	Stage-1 calorimeter trigger hardware tested and installed	PM21
M3.2	PM18	Stage-2 calorimeter trigger hardware tested and installed	PM28
M3.3	PM23	Stage-1 calorimeter trigger commissioned & system ready for physics	PM27
M3.4	PM30	Post-LS3 trigger dataflow design completed	PM30
M3.5	PM35	Stage-2 calorimeter trigger commissioned & system ready for physics	PM35
M3.6	PM54	Post-LS3 trigger prototype trigger modules produced and tested	PM54
M3.7	PM66	Demonstration of post-LS3 trigger slice	PM66
M3.8	PM72	Post-LS3 trigger construction plan delivered	PM72

12 Glossary

Following the request at a previous meeting, we compiled a list of acronyms in common use in the report, or during the oral session, or by CMS which we may have referred to.

AM	Associative Memory.
AMC13	A μ TCA data concentration and clock distribution card specific to CMS.
AMC	Advanced Mezzanine Card (from the ATCA specification).
APD	Avalanche Photodiode.
ASIC	Application Specific Integrated Circuit.
ATCA	Advanced Telecommunications Architecture.
BER	Bit Error Rate.
BX	Bunch crossing.
CBC(x)	CMS Binary Chip, version x, for the front-end ASIC for the outer tracker
cDAQ	Central Data Acquisition.
CIC	Concentrator Integrated Circuit, which follows the CBC.
CMSSW	Compact Muon Solenoid Software, is the CMS experiment software package.
CPM	Central Partition Manager.
CPU	Central Processing Unit.
CRC	Cyclical-redundancy check, a family of algorithms for identifying data corruption.
CTP7	Calorimeter Trigger Processor 7 card, featuring the Xilinx Virtex-7 FPGA.
DAQ	Data Acquisition.
DAQ2	Upgrade to DAQ system during LS1.
DSP	Digital Signal Processor.
DTC	Data, Trigger and Control board
DPG	Detector Performance Group.
FB	Finance Board.
FC7	FMC Carrier Xilinx Kintex 7, a processor board hosting multiple FMCs.
FED	Front End Driver, a CMS data acquisition board.
FMC	FPGA Mezzanine Card, ANSI/VITA standard for cards which interface to FPGAs.
FPGA	Field-Programmable Gate Array.
FSM	Finite State Machine.
GBT	Gigabit Transceiver Project at CERN.
GBTX	Gigabit Transceiver ASIC developed at CERN.
GCT	Global Calorimeter Trigger.
GLIB	General purpose μ TCA card developed by the CERN microelectronics group.
GMT	Global Muon Trigger.
GP	Geometric Processor.
GT	Level 1 Global Trigger.
GTX	A version of the Xilinx high speed serial transceiver, found on the Virtex 7 FPGA.
HDL	Hardware Description Language.
HE	Endcap Hadron Calorimeter.
HF	Forward Hadron Calorimeter.
HGCAL	High Granularity Calorimeter, the CMS Phase-2 endcap calorimeter.
HI	Heavy Ions, at the LHC refers to collisions between lead ions.
HL-LHC	High Luminosity LHC, the planned upgrade of the LHC machine around 2023.
HLT	High Level Trigger, a collection of software trigger algorithms.
HT	Hough Transform Processor.
I2C	Inter-Integrated Circuit chip-to-chip communications protocol.
IB	Institution Board.
IPbus	A protocol to control and communicate with Ethernet-attached xTCA hardware.
IPMI	Intelligent Platform Management Interface, a standardised computer system interface.
JTAG	Joint Test Action Group; test and diagnostic bus standard by IEEE1149.1.
L1A	Level-1 Accept.
LP-GBT	Low power Gigabit Transceiver.

LS1	Long Shutdown 1, first LHC long shutdown from beginning 2013 to end of 2014.
LS2	Long Shutdown 2, second LHC long shutdown scheduled for around 2018.
LS3	Long Shutdown 3, third LHC long shutdown scheduled for around 2022.
MGPA	Multi-Gain Preamplifier ASIC, used to readout ECAL photosensors.
MIP	Minimum Ionising Particle
MMC	Mezzanine Management Controller, part of the μ TCA specification.
MP7	Master Processor 7 card, featuring the Xilinx FPGA Virtex-7 chip.
MTF7	Muon Track Finder 7 card, featuring the Xilinx FPGA Virtex-7 chip.
MPW	Multi Project Wafer manufacturing submission, for CMOS ASIC production.
μ GT	Micro Global Trigger.
μ HAL	Micro Hardware Abstraction Layer.
μ HTR	Micro HCAL Trigger and Readout Card.
μ TCA	Micro Telecommunications Computing Architecture.
O2O	Software to simplify the propagation of configuration online.
oRM	Optical Receiver Mezzanines.
oRSC	Optical Regional Summary Card
oSLB	Optical Synchronization and Link Boards.
PCIe	Peripheral Component Interconnect Express, a high-speed serial computer bus.
SBS	Shared Business Services.
SerDes	Serialiser/Deserialiser chip.
SFP	Small Form-factor Pluggable standard for optical and other transceivers.
SFP+	Extension of the SFP standard to support up to 10 Gbps data rates.
SLINK	CERN specification for an easy-to-use FIFO-like data-link.
TCC	Trigger Concentrator Card.
TCDS	Trigger Control and Distribution System.
TFP	Track Finder Processor.
TMT	Time-Multiplexed Trigger, that processes events in parallel rather than sequentially.
TMTT	Time-Multiplexed Track Trigger
TPG	Trigger Primitive Generator.
TriDAS	Trigger and DAQ.
TTC	Trigger Timing and Control, a system for distribution of clocking and control.
UCG	Upgrade Cost Group.
uHTR	μ TCA HCAL Trigger and Readout card.
VHDL	VHSIC Hardware Description Language
VTRX	Versatile Link Transmitter/Receiver, optical transceiver developed by CERN.
VTTx	Versatile Link Dual Transmitter, optical transmitted developed by CERN.
XDAQ	Cross DAQ, a data acquisition software framework.
YETS	Year-End Technical Stop, a brief stop of the LHC during the winter holidays.