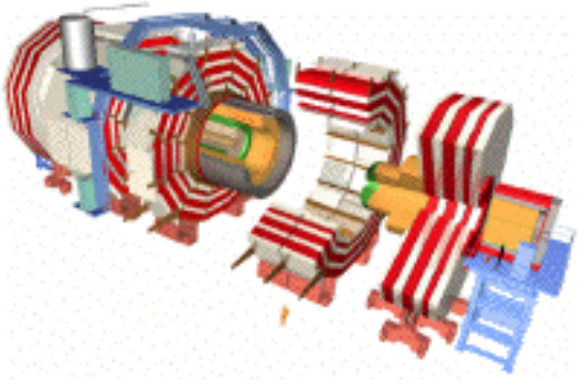
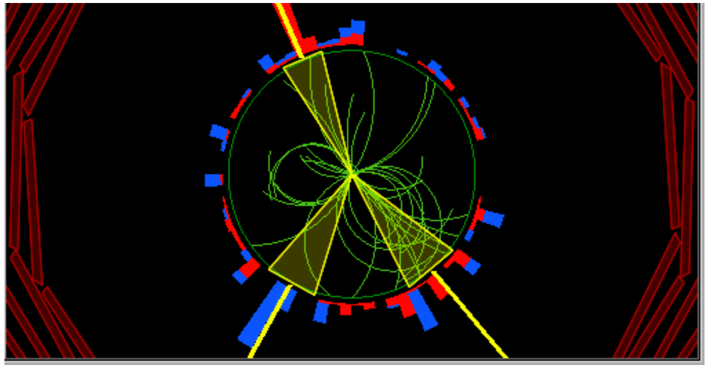




UK CMS Upgrade Oversight Committee

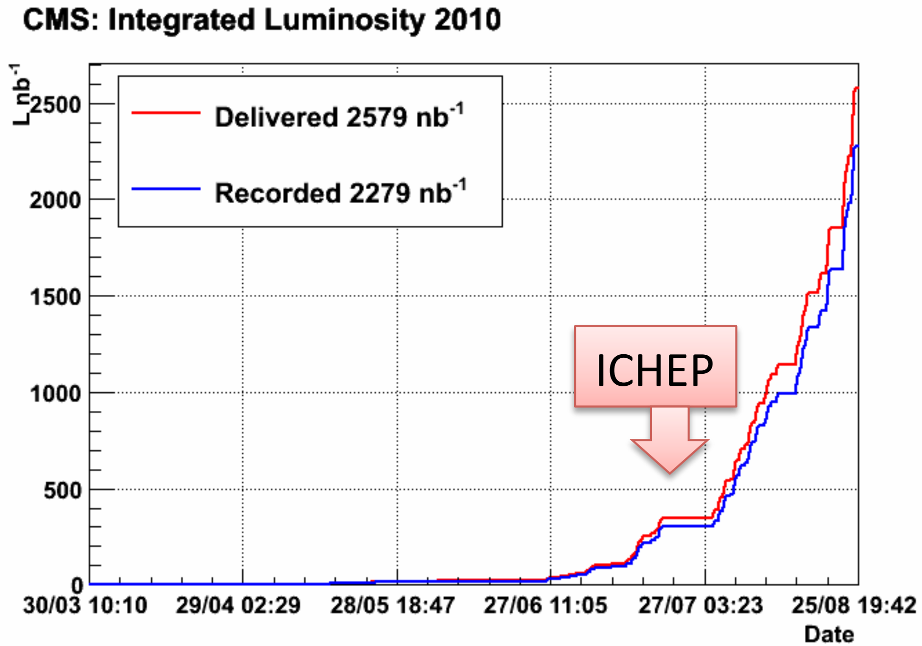
1 September 2010

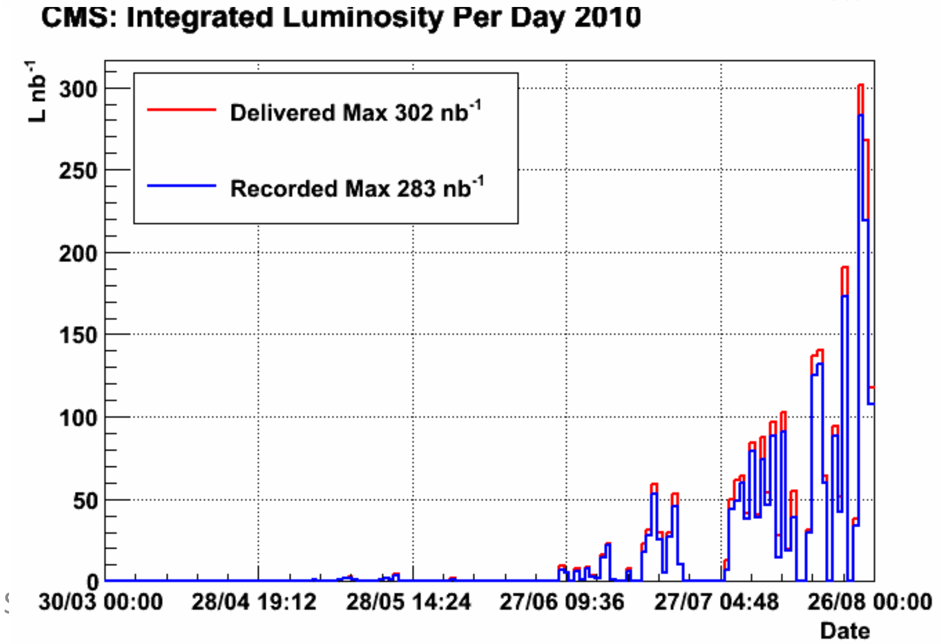
University of Bristol
Brunel University
Imperial College London
Rutherford Appleton Laboratory

Geoff Hall

Overview

- CMS status
  - good summary at ICHEP
    - omit if not needed
- LHC status and future plans
- UK R&D progress report
- Finances
- Future
  - CMS plans
  - UK CMS plans
- Issues

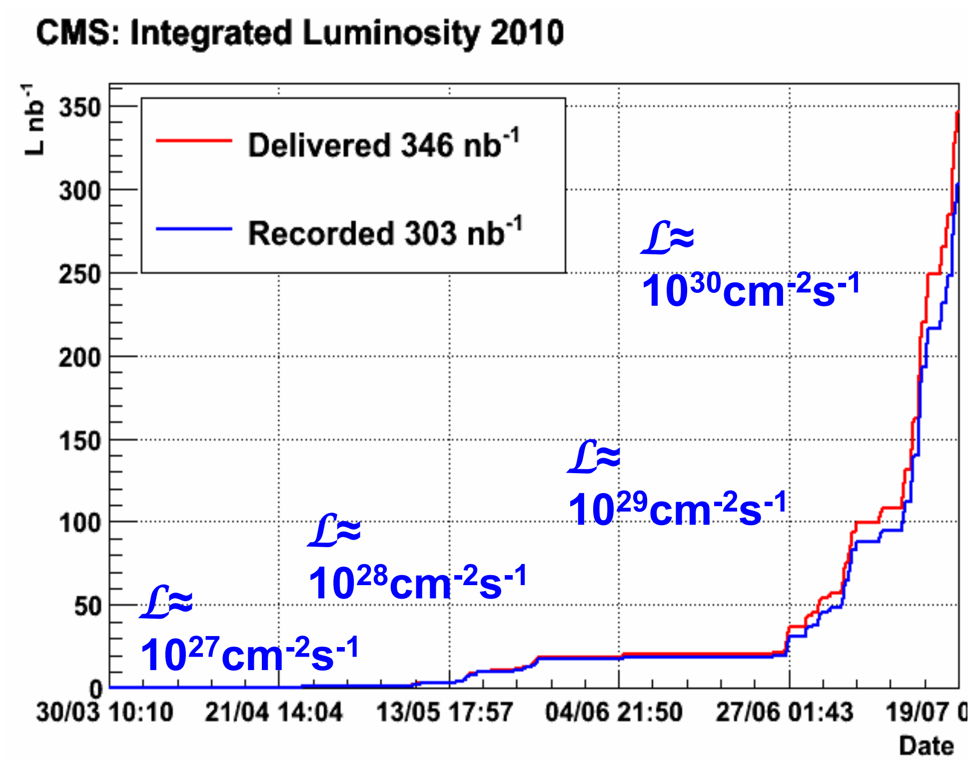


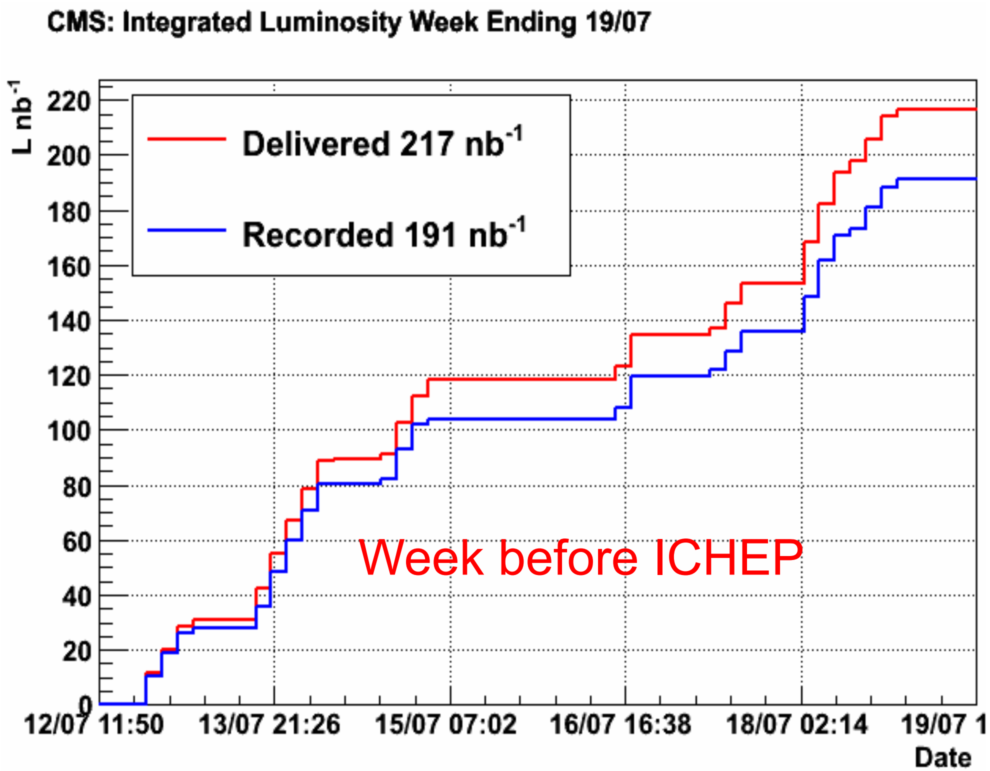


Recent progress

7 TeV operations since March 30

About **346nb^{-1}** delivered by LHC and **~303nb^{-1}** of data collected by CMS. Overall data taking efficiency **~88%.**

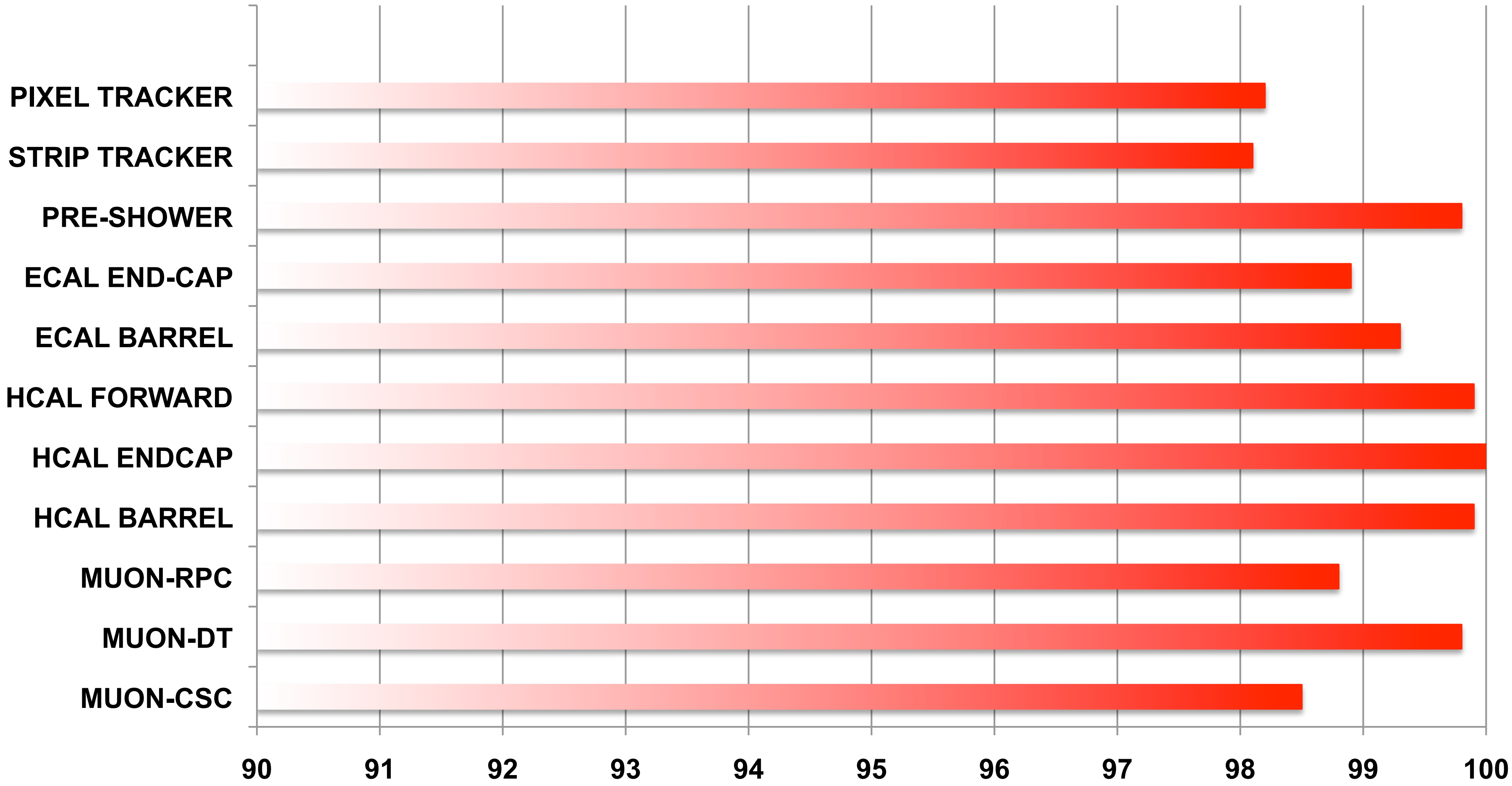




Good performance of CMS in coping with the 3 orders of magnitude increase in instantaneous luminosity. Additional challenge: most of the luminosity used for ICHEP results delivered in the last week(s).

281nb^{-1} good data for muon based analyses; 254 nb^{-1} validated for any analysis.

Sub-detectors operational status

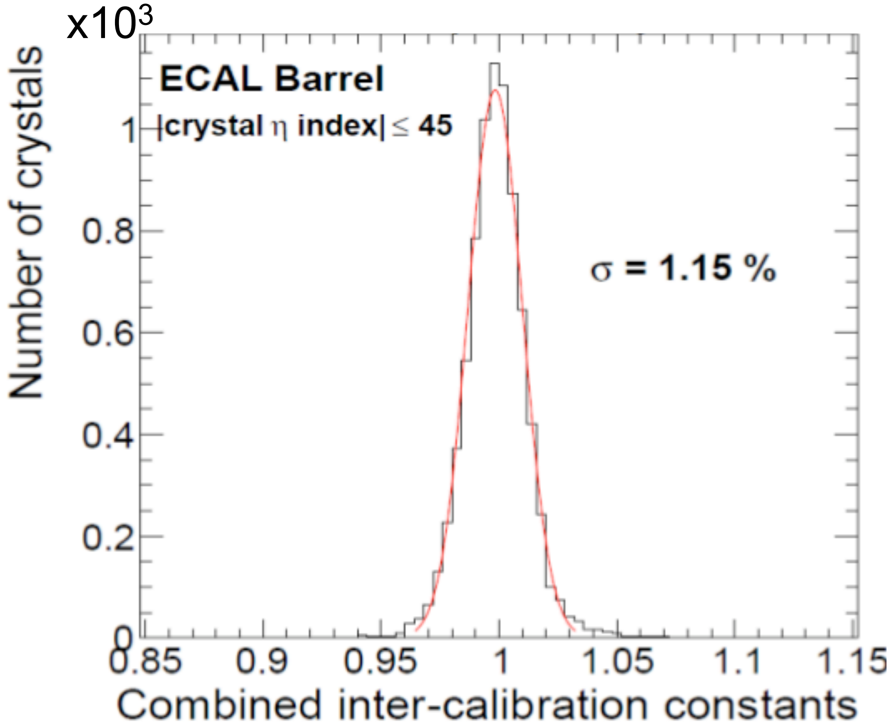


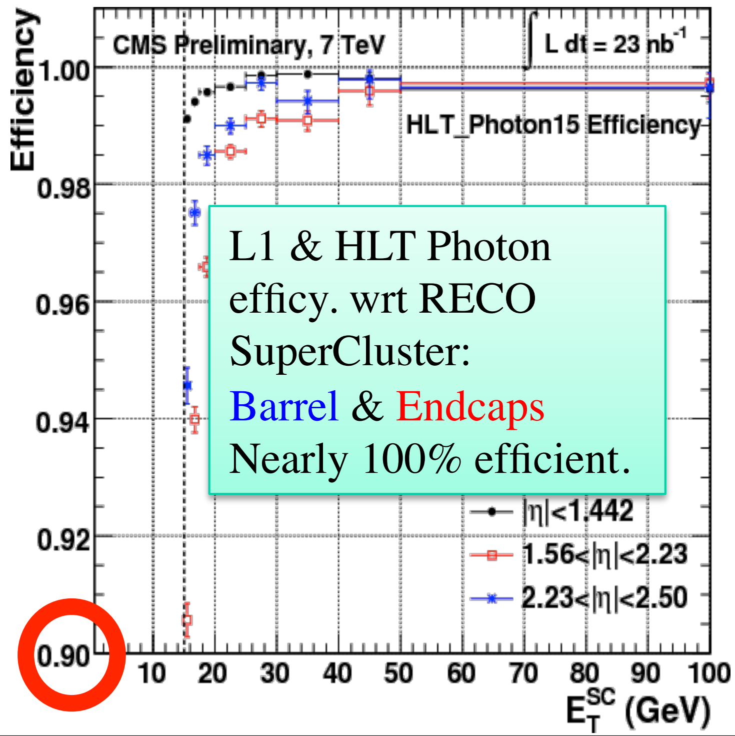
	MUON-CSC	MUON-DT	MUON-RPC	HCAL BARREL	HCAL ENDCAP	HCAL FORWARD	ECAL BARREL	ECAL END-CAP	PRE-SHOWER	STRIP TRACKER	PIXEL TRACKER	
Series1	98.5	99.8	98.8	99.9	100	99.9	99.3	98.9	99.8	98.1	98.2	

L1+ HLT Triggers

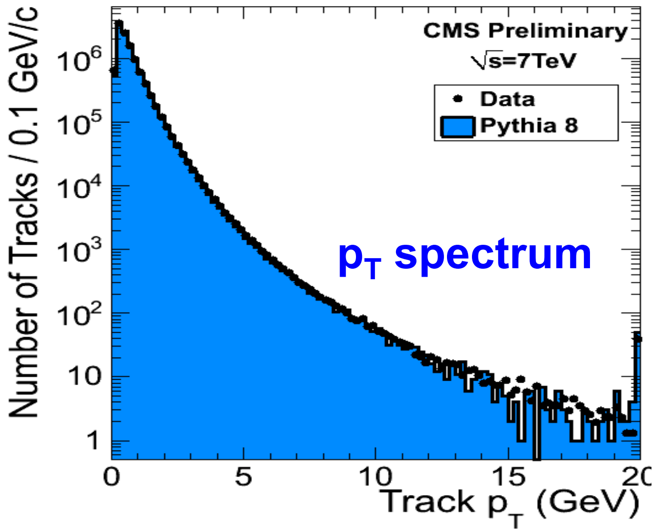
- **Successfully deployed HLT menus for 2-4-8x10^{29}cm^{-2}s^{-1} and 1.6x10^{30}cm^{-2}s^{-1}.** Each one has a factor 2 of safety margin. Very smooth running throughout. In preparation/validation **HLT menus for 10^{31}-10^{32}**.
- Processing time per event to **~50 ms/ev at a lumi of ~10^{30} cm^{-2}s^{-1}**
- (Farm Capacity ~100ms/evt at L1 rate of 50kHz)

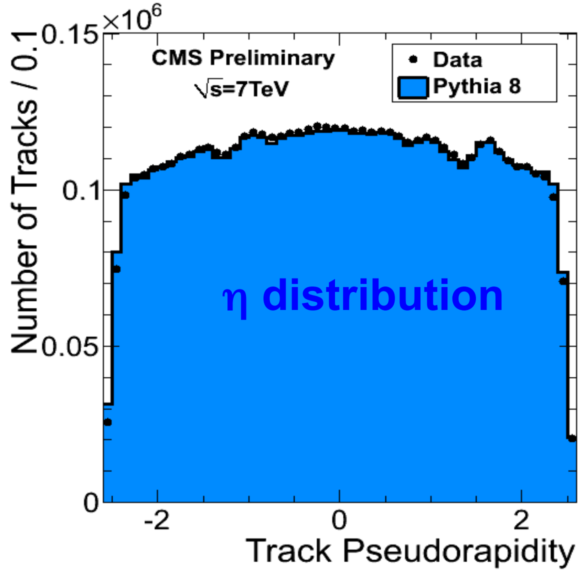
Special stream to collect π^os for the calibration of ECAL: >100 π^os/crystalxday @10^{30}. Relative calibration already close to 1%. Goal is 0.5% (>10pb^{-1})

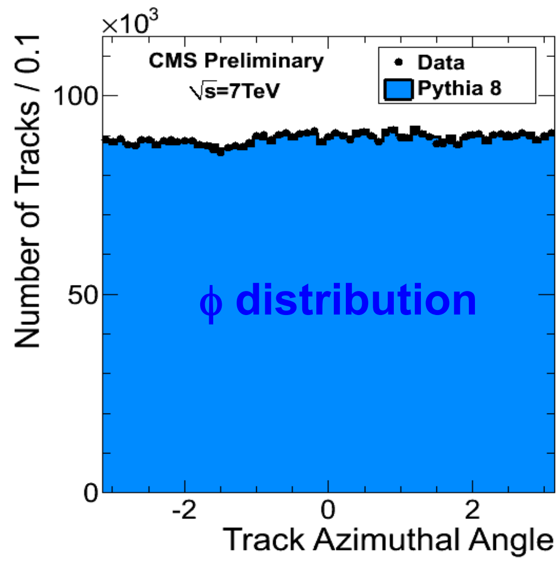


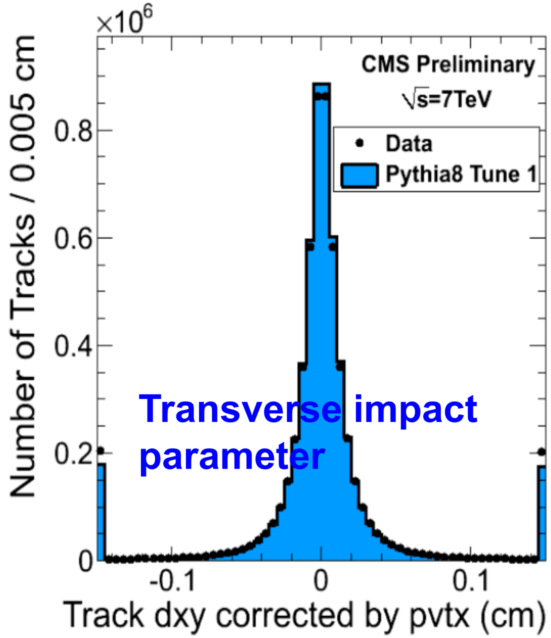


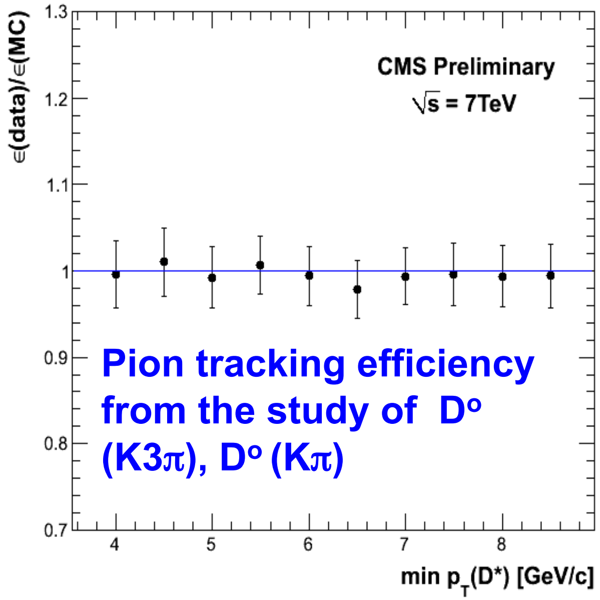
Understanding the Tracker Performance

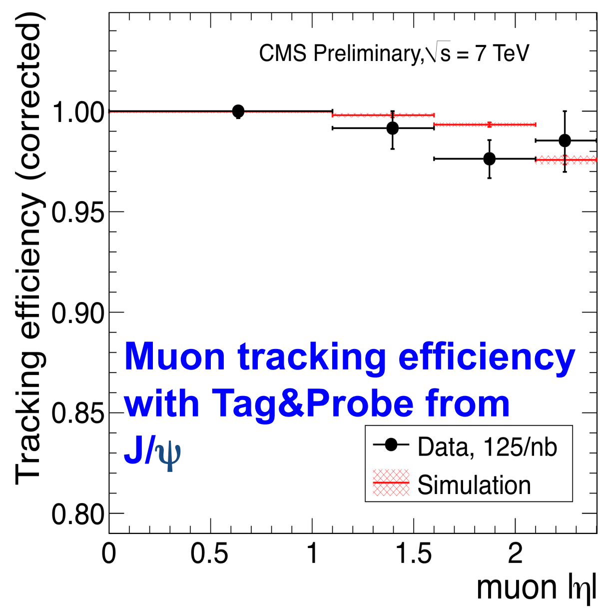




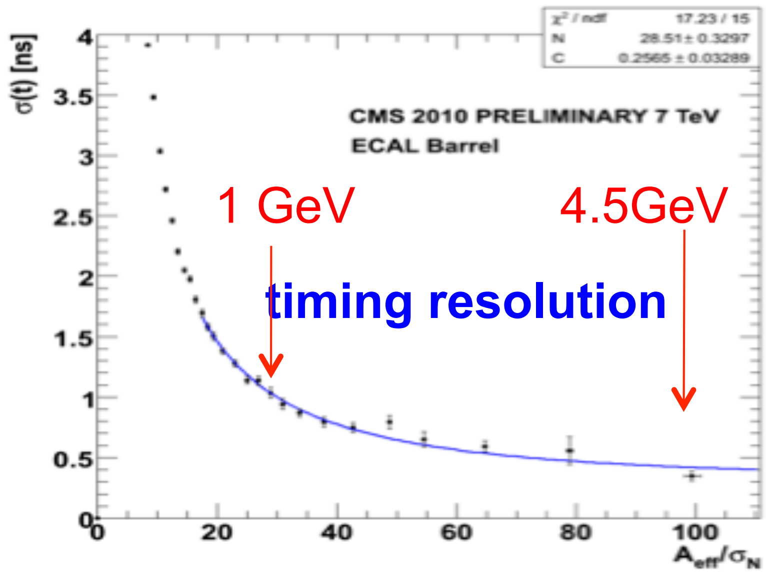


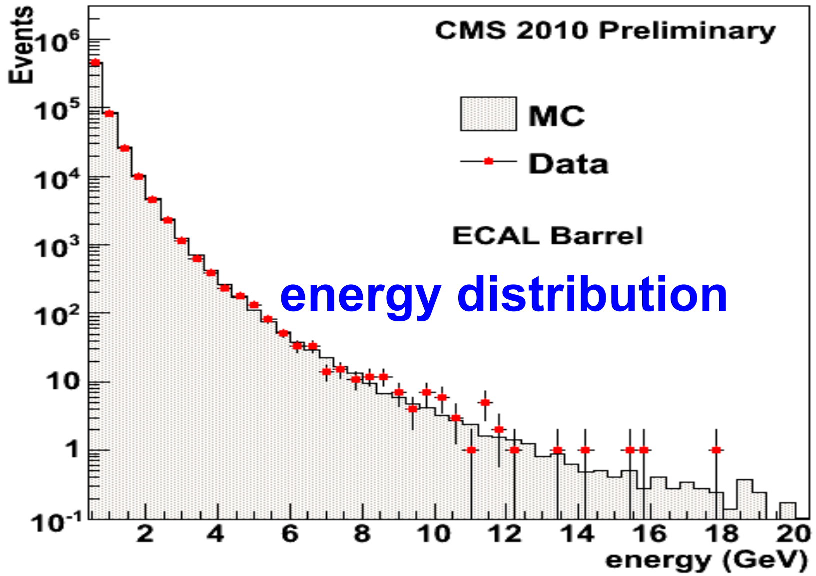


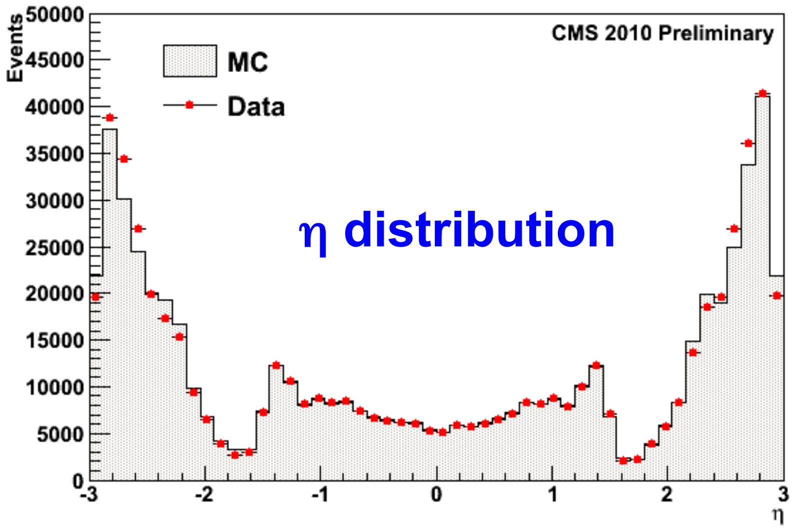


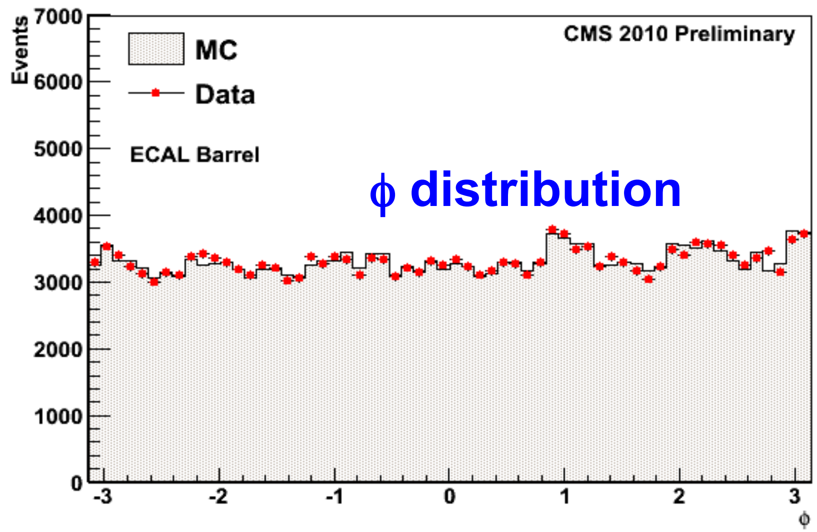


ECAL clusters (electrons and photons)





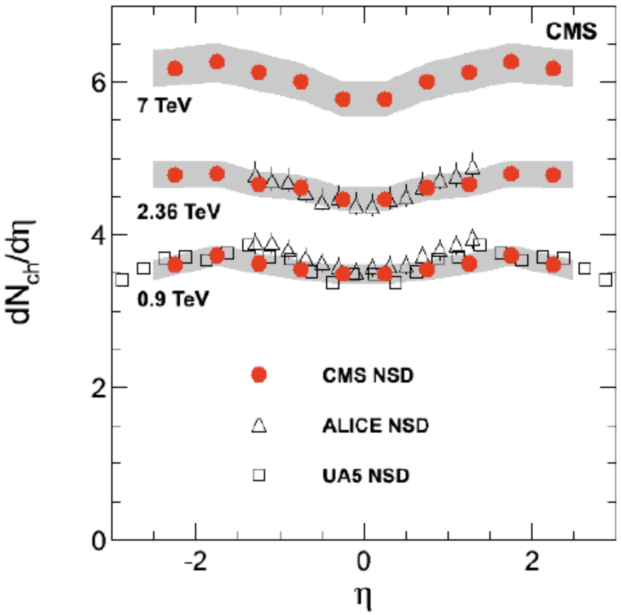


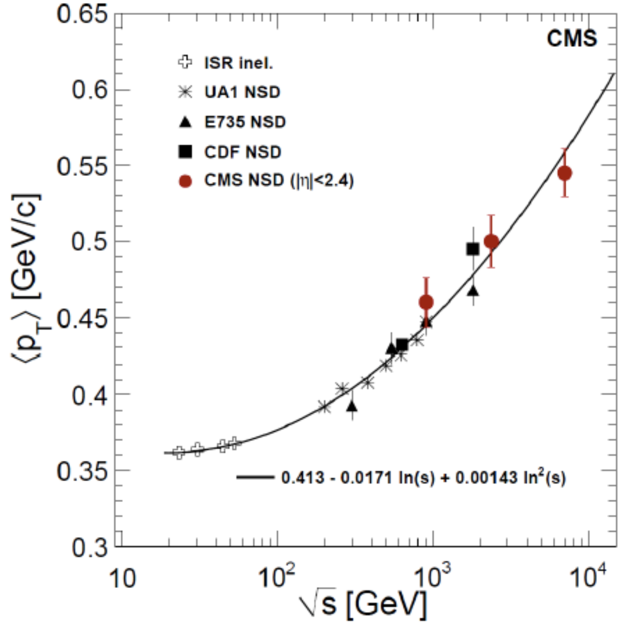


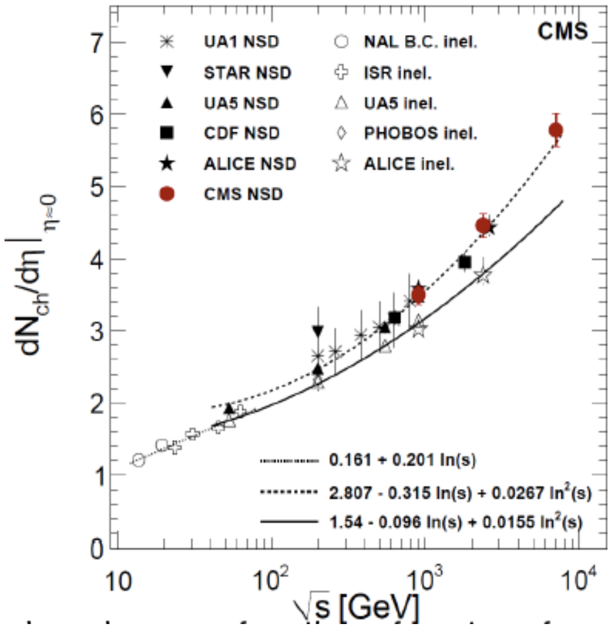
Charged Hadrons

"Transverse Momentum and Pseudorapidity Distributions of Charged Hadrons in pp Collisions at √s=7TeV" Phys. Rev. Lett. 105, 2010.

Minimum bias events
Non single-diffractive event selection (correction 6%→2.5% systematic error)
Really soft QCD (p_T tracks down to 50MeV)



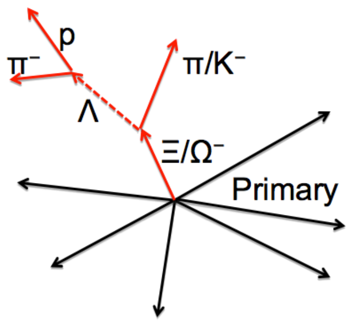




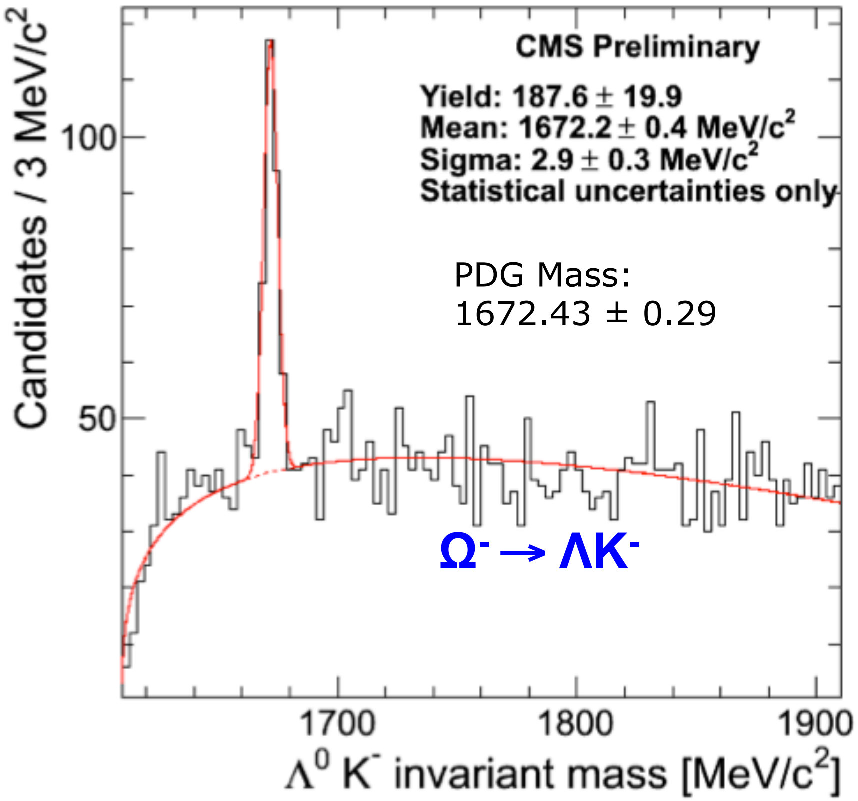
Rise of the particle density in data stronger than in model predictions.
Careful tuning effort of the MC generators ongoing.
Marginal impact on high p_T physics.

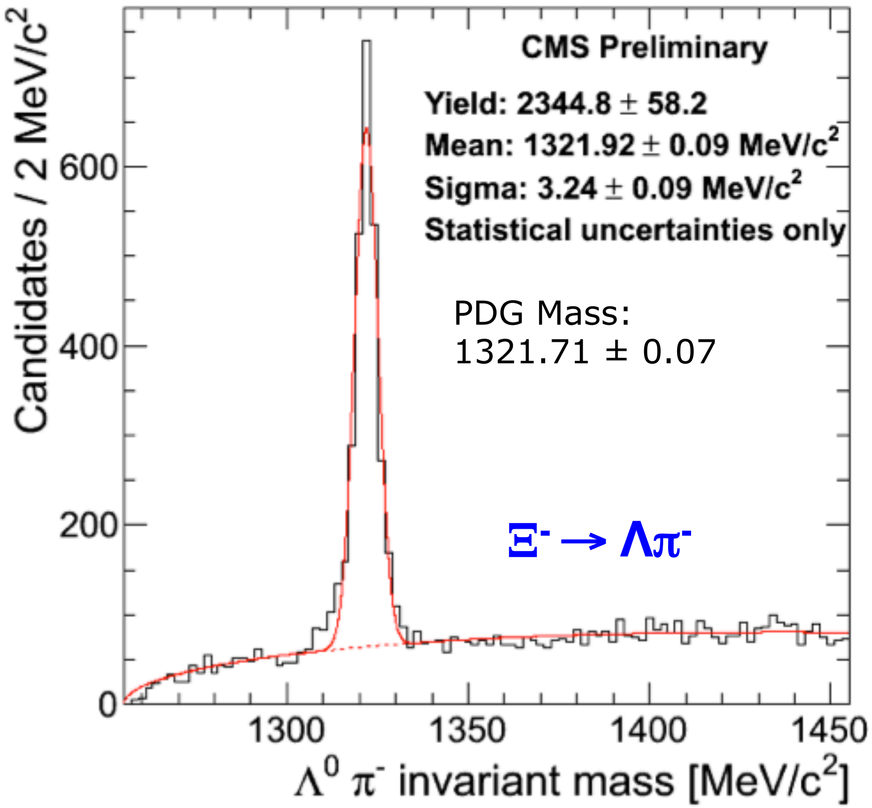
Low mass resonances

- Tracks displaced from primary vertex ($d_{3D} > 3\sigma$)
- Common displaced vertex ($L_{3D} > 10\sigma$)

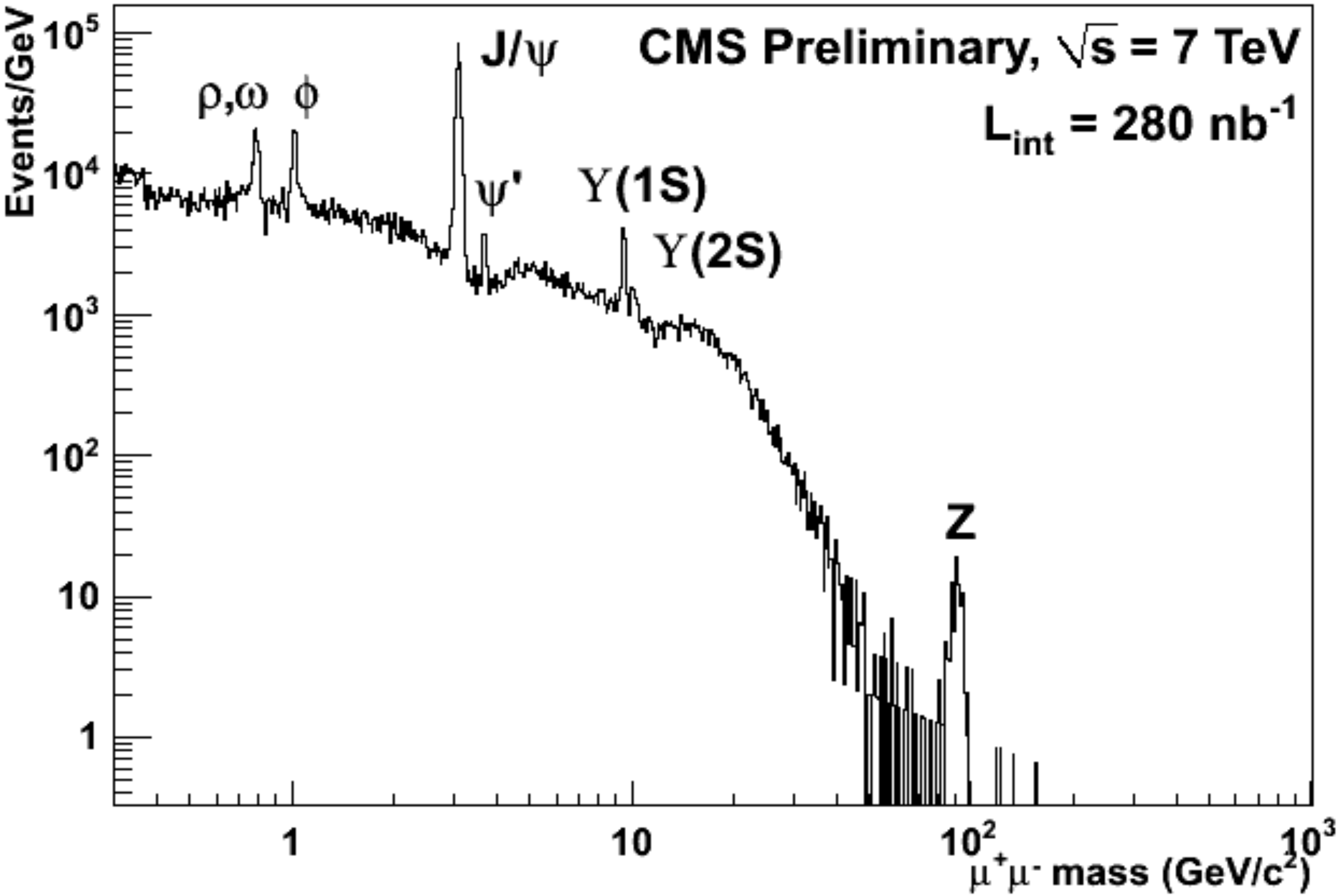


Invariant mass distribution for different combinations ($\Omega^{\pm} \rightarrow \Lambda K^{\pm}$ or $\Xi^{\pm} \rightarrow \Lambda\pi^{\pm}$) fit to a common vertex.





Here is the Compact Muon Solenoid



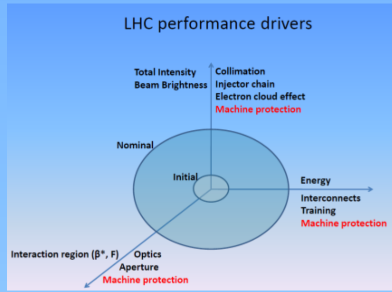
LHC status and future plans

- Reached L = 1.6 10^{30} $cm^{-2}s^{-1}$ in mid July, 1.07 10^{31} $cm^{-2}s^{-1}$ in late August
  - Stable running over summer
- Increase to ~10^{32} $cm^{-2}s^{-1}$ during autumn
  - 1 fb^{-1} by end 2011
- 2012: Shutdown ~ 15 months for splices
- 2013-2015: 6-7 TeV operation
  - perhaps reaching ~10^{34} $cm^{-2}s^{-1}$ in 2015
- 2016: Shutdown for collimators, Linac 4
- From 2017: increase above nominal luminosity to ~2 10^{34} $cm^{-2}s^{-1}$
- Around 2020-2022: shutdown for Phase II
  - Objective: levelled luminosity ~ 5 10^{34} $cm^{-2}s^{-1}$ to deliver 3000 fb^{-1} by 2030

- Uncertain: LHC operation at 50ns
  - worsens experimental conditions: pileup, occupancy, trigger isolation, …

Getting to nominal (dates indicative)

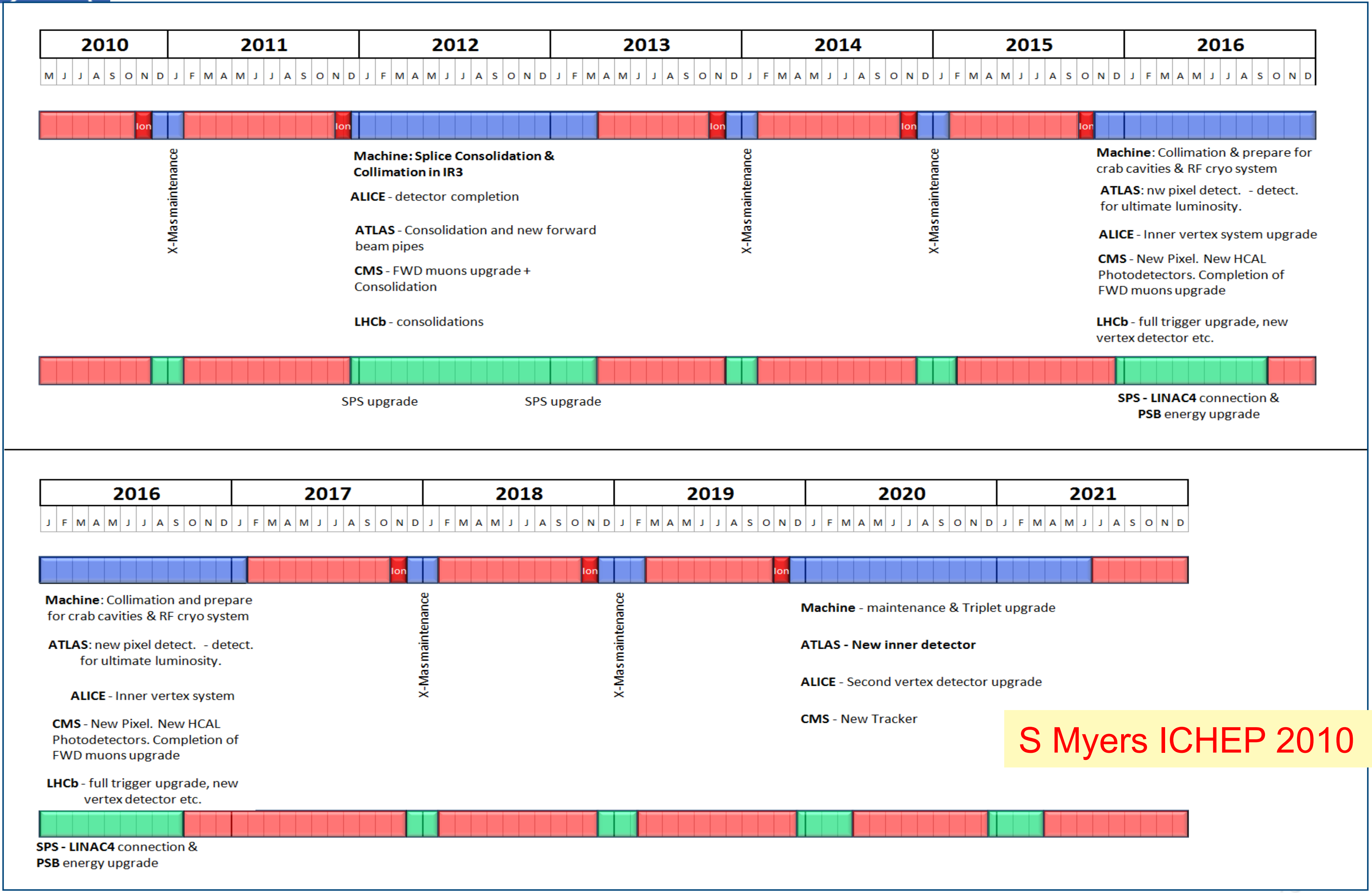
$$L = \frac{N^2 k_b f}{4\pi\sigma_x\sigma_y} F = \frac{N^2 k_b f \gamma}{4\pi\varepsilon_n\beta^*} F$$



2010	2011	2012	2013	2014	2015	2016
Energy3.5TeV		Splices, Collimators in IR3	Increase Beam Energy to 7TeV			
β^* of 2m			Decrease β^* to 0.55m			
20% of I_{nom}			Increase k_b to 2808			
Initial			Nominal			
10^{32}			10^{34}			
1 fb^{-1}			≤ 50 fb^{-1}/yr			

R Bailey ICHEP 2010

The 10 year technical Plan



S Myers ICHEP 2010

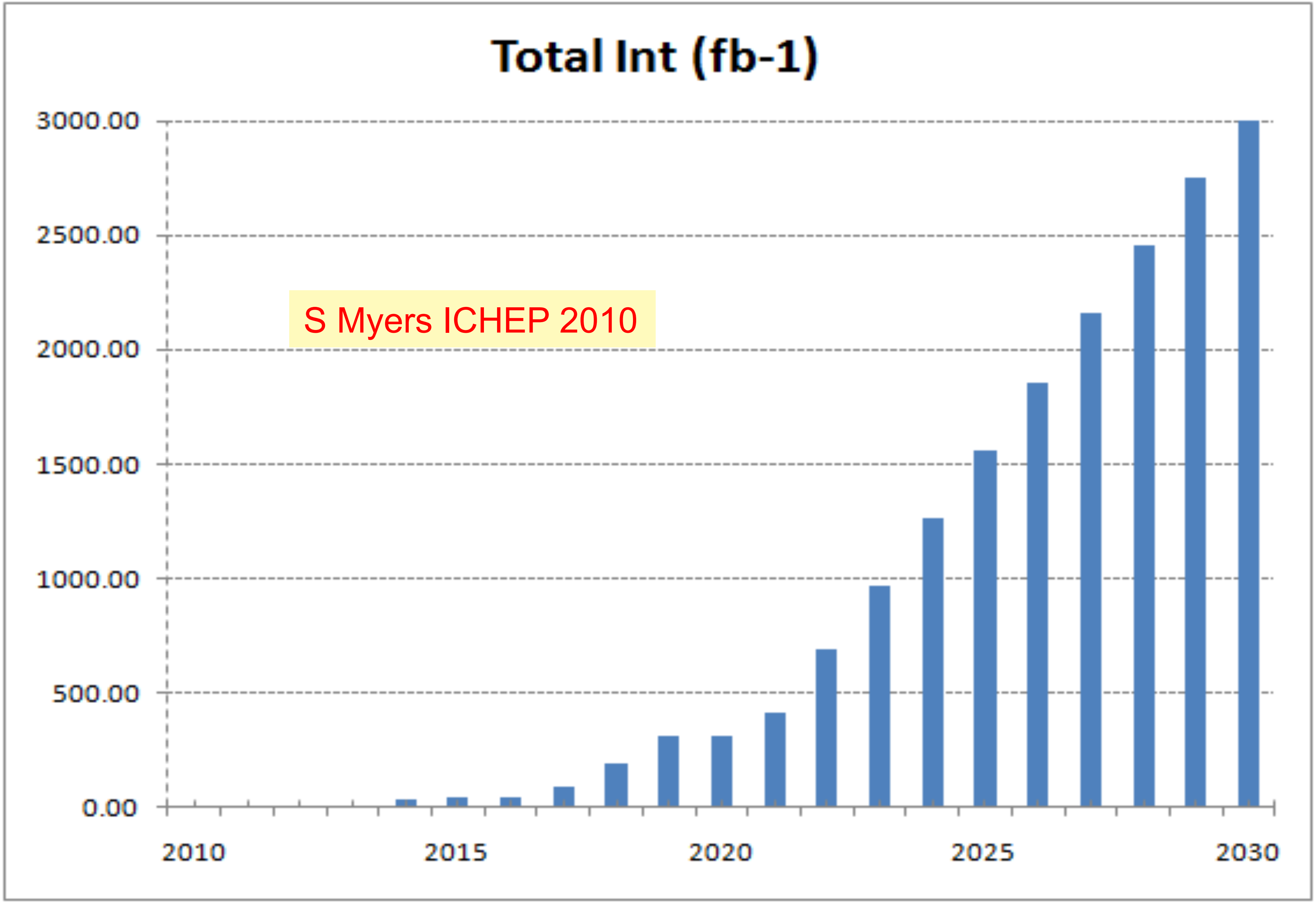
Preliminary Luminosity Predictions

Year	TeV	OEF	β*	Nb	Ib	Itot	MJ	Peak luminosity	Pile up	pb-1/day	Physics Days	Integrated (fb-1/year)	Total Int (fb-1)
2010	3.50	0.20	2.00	796	8.0E+10	6.4E+13	36.0	1.886E+32	1.2643	3.3	20.0	0.1	0.07
2011	3.50	0.25	2.00	796	8.0E+10	6.4E+13	36.0	1.886E+32	1.2643	4.1	240.0	0.98	1.04
2012												0.0	1.0
2013	6.50	0.20	0.55	796	1.15E+11	9.2E+13	96.1	2.632E+33	17.6429	45.5	180.0	8.2	9.2
2014	7.00	0.20	0.55	1404	1.15E+11	1.6E+14	[illegible]	5.000E+33	19.0000	86.4	240.0	20.7	30.0
2015	7.00	0.20	0.55	2808	1.15E+11	3.2E+14	365.0	1.000E+34	19.0000	172.8	210.0	36.3	66.3
2016											0.0	0.0	66.3
2017	7.00	0.25	0.55	2808	1.15E+11	3.2E+14	365.0	1.000E+34	19.0000	216.0	240.0	51.8	118.1
2018	7.00	0.28	0.55	2808	1.30E+11	4.2E+14	476.1	1.701E+34	32.3251	411.6	240.0	98.8	216.9
2019	7.00	0.30	0.55	2808	1.70E+11	4.8E+14	539.6	2.185E+34	41.5198	566.4	210.0	118.9	335.8
2020											0.0	0.0	335.8
2021	7.00	0.20	0.20	2808	1.70E+11	4.8E+14	539.6	4.006E+34	76.1197	692.3	150.0	103.8	439.7
2022	7.00	0.27	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1257.3	220.0	276.6	716.3
2023	7.00	0.27	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1257.3	220.0	276.6	992.9
2024	7.00	0.29	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	1290.0
2025	7.00	0.29	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	1587.1
2026	7.00	0.29	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	1884.2
2027	7.00	0.29	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	2181.3
2028	7.00	0.29	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	2478.4
2029	7.00	0.29	0.25	2808	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	2775.5
2030	[illegible]	[illegible]	[illegible]	[illegible]	1.80E+11	5.1E+14	571.3	5.390E+34	102.4060	1350.5	220.0	297.1	3072.6

Very preliminary with large error bars

S Myers ICHEP 2010

Preliminary Long Term Predictions



UK & CMS upgrade progress

- WP1
  - simulation code in use for Phase I pixel and physics studies
  - online software for WP3 and new architecture for future
- WP2
  - Full chip CBC submitted in July, wafer delivery late September
  - expect die for testing in October
- WP3
  - excellent progress with Mini-T5
  - candidate for trigger, Phase II tracker and possible Phase I pixel FEDs
- CMS Technical Proposal due for submission 9 September
  - detailed but outline summary of CMS plans for period to 2020
  - most relevant items for UK: Trigger, Pixel Tracker and overall planning
    - installation of proven systems during 2016 shutdown
      - DAQ upgrade might have repercussions for Tracker FED
    - Phase II Tracker R&D overview also included

WP1

- Objectives were to study upgraded inner tracker, with trigger in mind
  - NB no Phase I or Phase II envisaged originally
- Work focussed on tool development and design studies
  - now being deployed for Phase I tracker simulations and Physics for TP
  - progress on track-trigger studies but still far in future

- Compatibility with overall UK programme
  - online software needed for WP3 trigger activities
    - will also benefit WP2 evaluation studies
  - results and developments are clarifying role and potential contributions to Phase I upgrade
    - these new software architecture ideas complement ongoing work and provide a basis for effective future developments - discuss under WP3

Tracking Simulation: Current Status

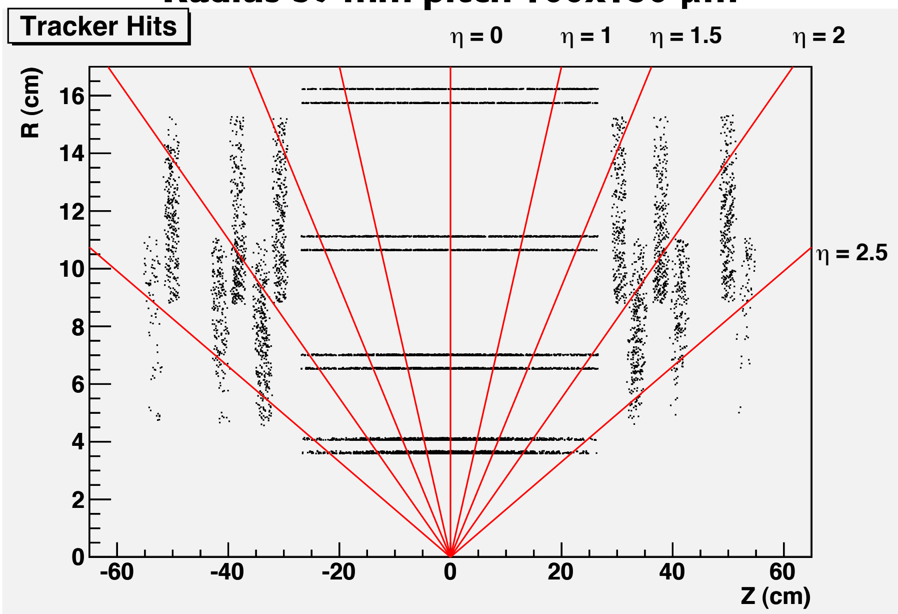
Slide from Joel

The Phase I pixel upgrade will have 4 barrel layers and 3 forward disks. Currently investigating the effects of two parameters:

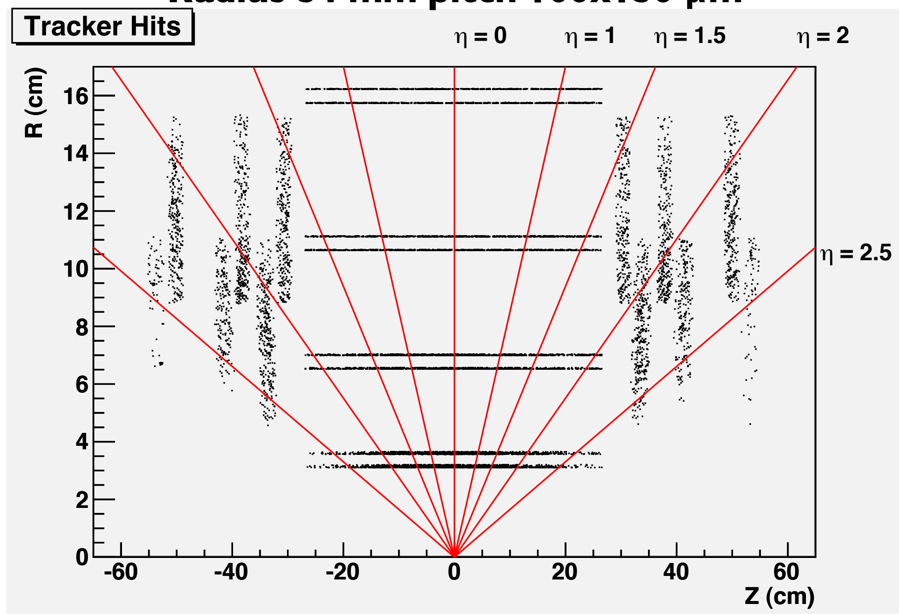
- Inner layer radius of either 34 or 39 mm
- Inner layer either with a pitch of 100x150 um and thickness of 285 μm; or pitch of 75x100 μm and thickness 220 μm

With the standard geometry this gives 5 different configurations for any one simulation. The Phase I geometries have recently (June 22nd) been updated to reflect the material in Roland Horisberger's models.

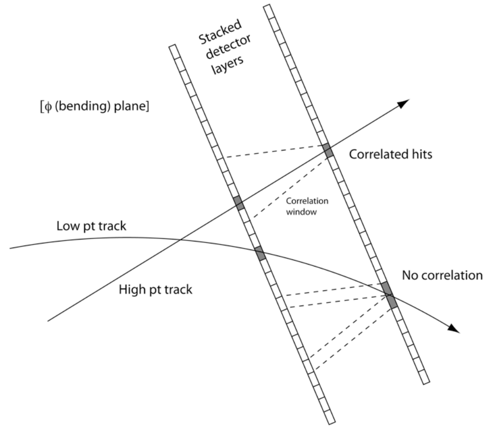
Radius 39 mm pitch 100x150 μm



Radius 34 mm pitch 100x150 μm



Tracking Trigger Studies



- Active in this area:
  - Dave Newbold, Kristian Harder, Rob Frazier, Jim Brooke
- Original goals
  - Approximate, but ultra-fast, study of stacked track trigger parameter space
    - {Layer count, granularity, spacing} versus {occupancy, rate reduction, efficiency, fake rate}
  - First investigation of 100 / 200 / 400 pileup regime
  - First investigation of the endcap triggering issues
- Achievements
  - Confirmation of basic relations between parameters and performance
  - First study of the trade-offs in the endcap – appears feasible
  - First assessment of real data rates (with resolution, truncation, fixed busses)
  - First study of isolation cone electron triggering
- Currently being written up

WP2

- ASIC (CBC) development
  - CBC now submitted on MPW (with RAL XFEL ASIC) and preparing for testing
  - Less TD effort than anticipated but schedule acceptable
- Future FED development
  - TD effort only available in recent months
  - Delay has allowed maturing of GBT and evolution of Mini-T
    - initially evaluate GBT firmware, then evaluate Mini-T for Tracker
- Powering studies (Bristol) now concluded
  - CMS decision to adopt DC-DC as baseline
  - Good progress to date in CERN with components so alternatives not high priority
  - Effort now to testing CBC – matches WP1/WP3 activity
- Module development
  - Collaboration with other CMS institutes, especially CERN, ongoing
  - Decisions in coming year on priorities for CBC

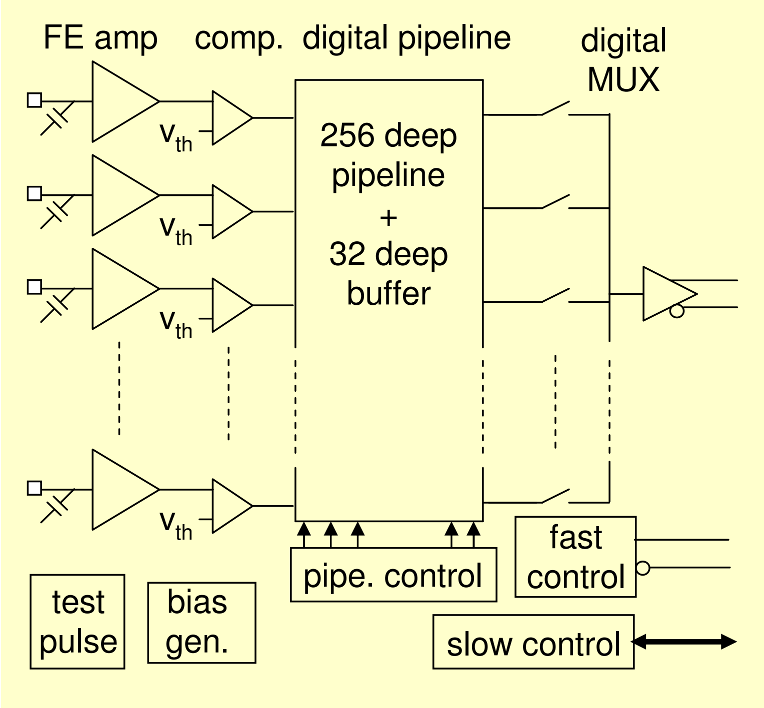
architecture choice

binary un-sparsified architecture -> **CMS Binary Chip**
simplicity/robustness, lowest power

main functional blocks
- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- output mux and driver (SLVS)
- fast (SLVS) and slow (I2C) control interfaces

some target specs (see * for full list)
- both signal polarities
- DC coupled to sensor – up to 1 uA leakage
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF

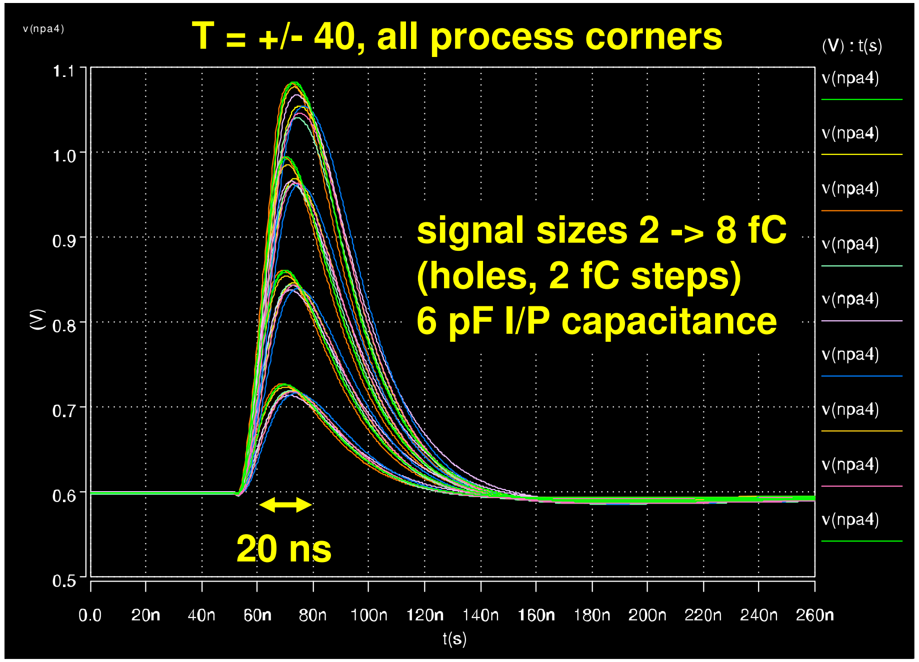
CBC



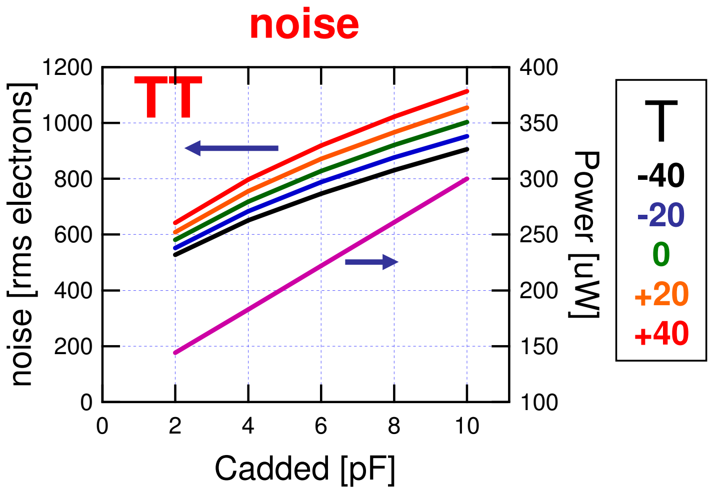
* *http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_specifications.pdf*

3

postamp output pulse shape & noise



~ 20 nsec peaking, ~ 50 mV / fC
robust to temperature (-40 -> +40) and process variations
electron signal gives opposite polarity



preamp input device power varied with Cadded (added input capacitance) to maintain constant pulse shape

(otherwise preamp risetime increases with Cadded and overall pulse shape affected)

for 1 uA leakage current add 440e in quadrature

6

layout

actual submission size 7 x 4 mm^2

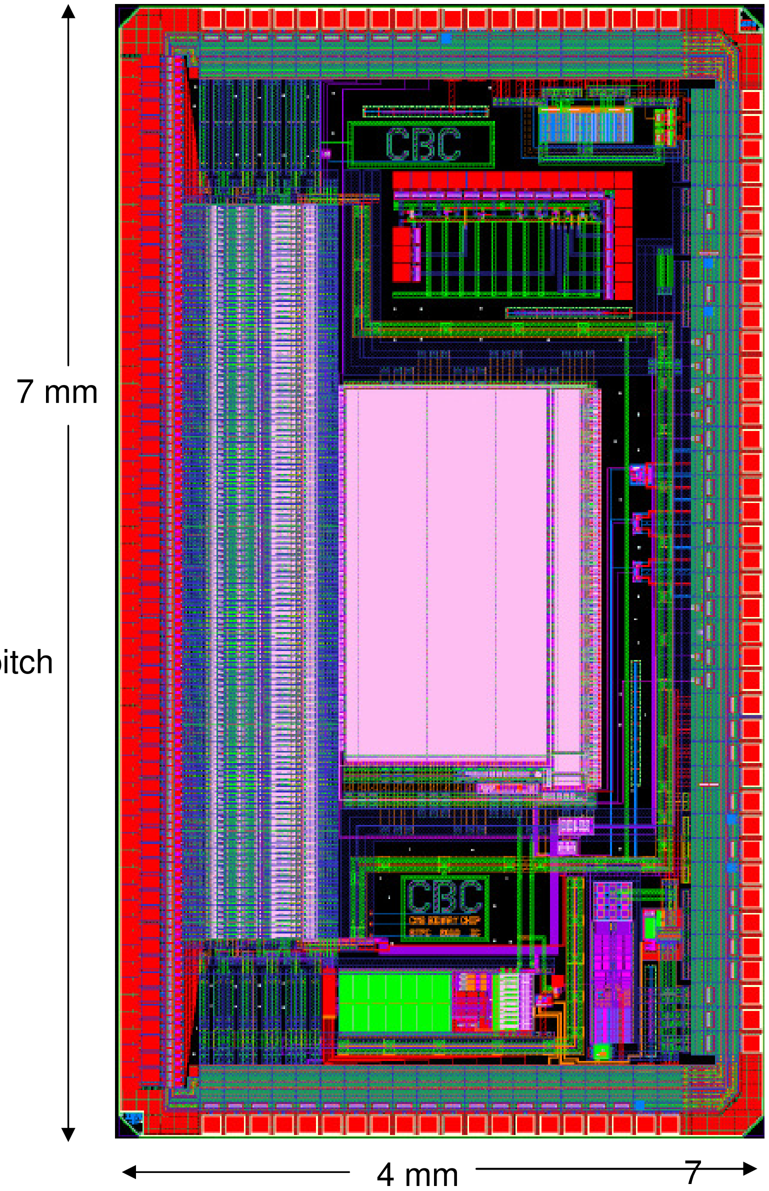
for MPW dicing reasons – 7 x 3.5 possible

input pads on 50 um pitch

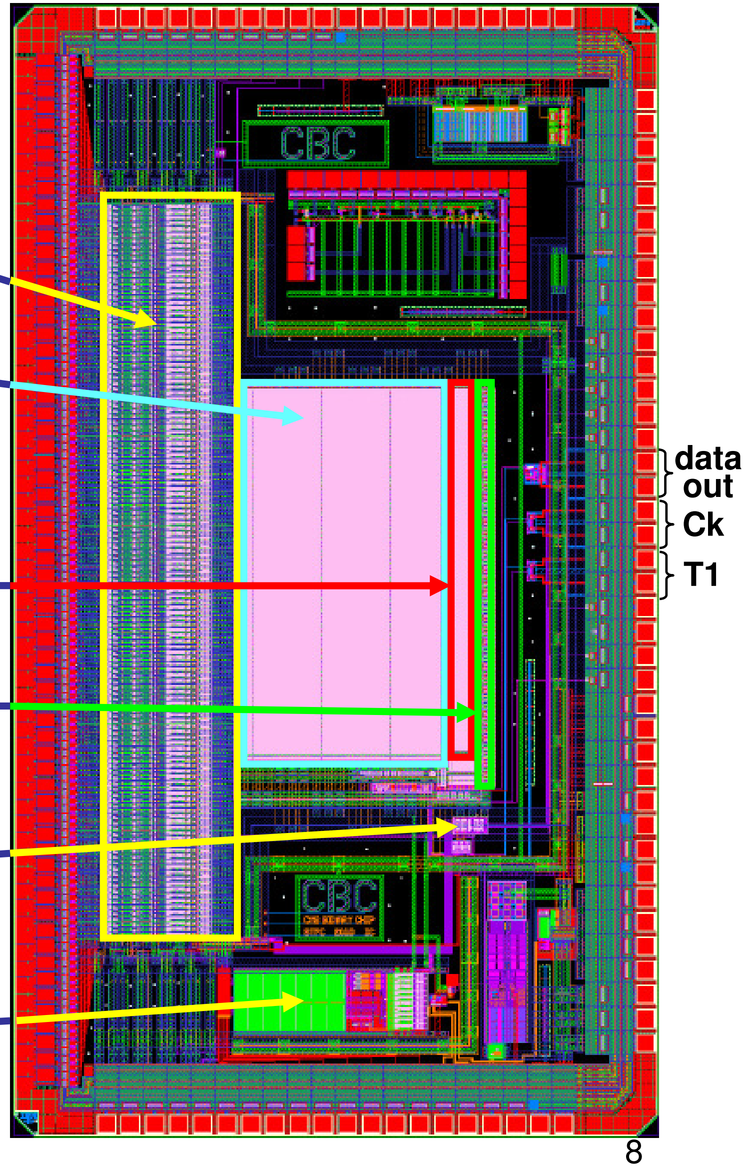
2 staggered rows on 100 um pitch

note: no power pads on front edge

all other pads (top, bottom, right hand side) on 150 um pitch



some blocks



128 preamp/postamp/comparator channels
- including DAC for individual postamp O/P offset

256 long pipeline (RAM)

pipeline control logic (underneath pipeline)
- "write" and "trigger" counters separated by programmed latency – decoded beneath pipeline columns to control read/write access

32 deep buffer for events awaiting readout
- data transferred to this buffer on receipt of L1 trigger

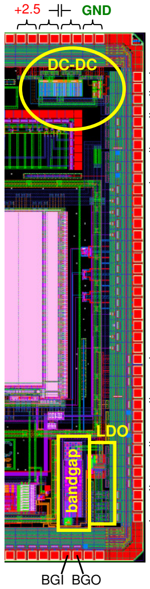
output shift register
- triggered data shifted serially off-chip (channel order)
- preceded by digital header
  - (includes triggered pipeline column address)

I^2C interface
- for programming bias registers, 128 channel 8-bit offsets, latency, polarity select register, …

bias generator
- 7 currents, 3 voltages

Options and plans

CBC powering options

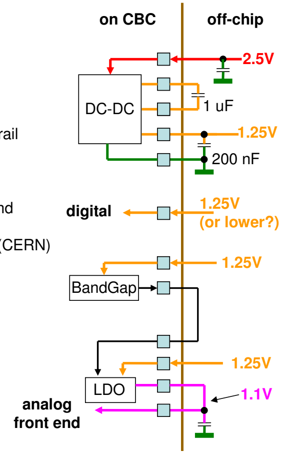


can explore some powering options

switched capacitor DC-DC (CERN) [1]
converts 2.5 -> 1.25
could use 1.25 to provide CBC digital rail

LDO (low drop-out) linear regulator
converts 1.25 -> 1.1
provides regulated rail to front end
giving supply noise rejection [2]
needs bandgap reference input (CERN)

can incorporate without risk
can be overidden
all pads accessible



1 http://indico.cern.ch/getFile.py/access?contribId=3&resId=0&materialId=slides&confId=85278
2 http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/LDO_PWG_Sep09.pdf

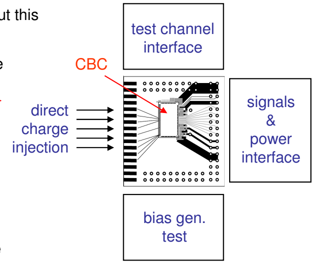
9

testing plans … only just begun thinking about this

at IC will want to verify detailed chip functionality and performance

will probably make something like this
fineline chip carrier board (chip + capacitors only)
+ interface boards for signals and power

may need different versions to test different functionalities
e.g. with/without different powering options



for DAQ can use old APV system – VME based/Labview interface

CERN VI2C card for I2C
digital pattern generator to provide clock/trigger
ADC to acquire output data (even though just binary)

Bristol plans

will focus on module and system tests using daughter board on FPGA development platform

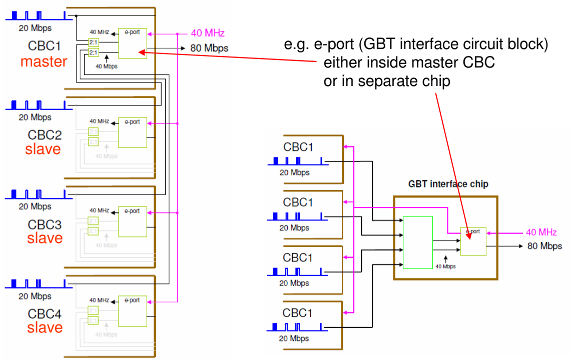
see talk by David Cussans (16th June 2010 Power Working Group)
http://indico.cern.ch/getFile.py/access?contribId=3&resId=0&materialId=slides&confId=97972

14

future chip developments (1)

CBC prototype designed to be complete working readout chip
but some system functionalities not yet present

system aspects have been discussed in TUPO meetings
e.g. how to combine data and interface to GBT
discussions will continue, but more than one viable option exists



15

future chip developments (2)

128 -> 256 back-to-back

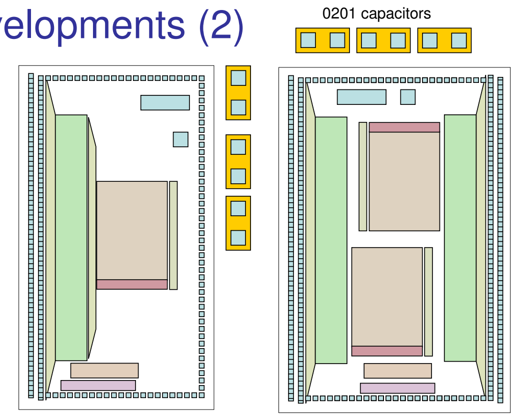
can share some functionality
e.g. power, control
but not much else

reduced area, cheaper

less pads available on 256 version

less flexible

overall power consumption
probably not much different



conclusions

256 back-to-back probably not impossible
but more detailed study may yet reveal difficulties
e.g. hard to see where DC-DC conversion can fit without causing problems
(interference & room for external capacitors)

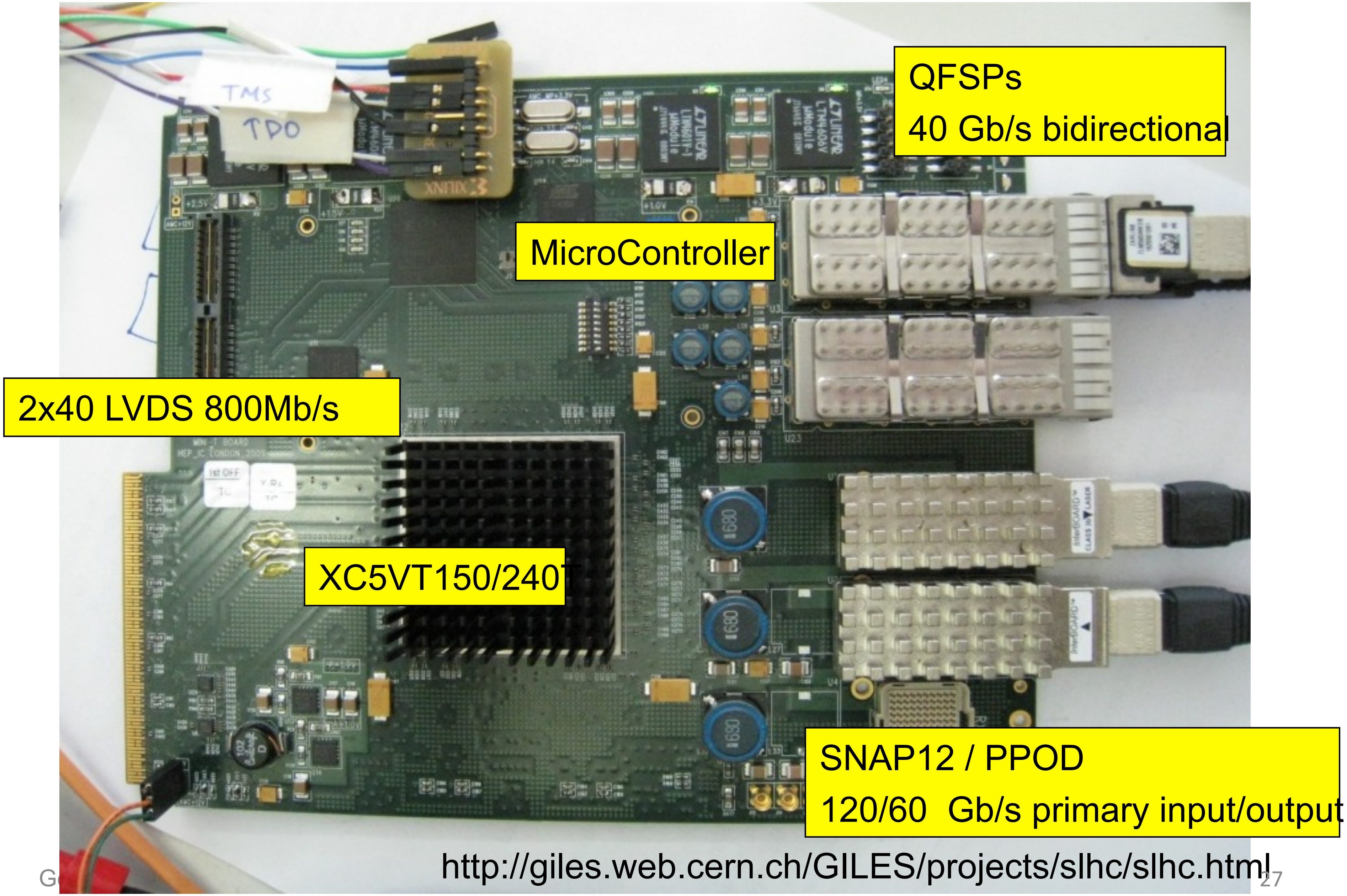
16

WP3

- Mini-T5 card manufactured – delivered before last OSC
  - extensive, successful testing since March
  - further production of a series of extra boards being prepared
    - share with collaborators, especially other WPs
  - excellent progress on firmware & software

- CMS Phase I trigger upgrade
  - Mini-T5 (or subsequent version with Virtex 7) could already form basis for required hardware
    - and substantially ahead of other developments in CMS
  - New idea for time-multiplexed trigger implementation
    - not yet adopted by CMS but system hardware/firmware is agnostic
  - New ideas - with WP1 - for software architecture being developed
    - based on experience from CMS GCT and other developments
    - standardise, improve flexibility and adaptability, ensure quality

Hardware: MINI-T5



http://giles.web.cern.ch/GILES/projects/slhc/slhc.html

Hardware: Work in progress

- Results
  - GbE operating inside a development crate from Schroff
  - All 32 data links operating at 5Gb/s
  - AVR32 MicroController and JTAG CPLD OK
  - PROM missing a wire. Not critical.

- Next
  - Rev1 of MINI-T5 to go out as soon as optics availability confirmed
  - Test system at Bristol and Imperial
  - Infrastructure firmware:
    - Finish link synchronisation firmware
    - Demonstrate and measure latency
    - Integrate algorithms into firmware
    - Add DAQ capability – just via Ethernet

Firmware Algorithms: Work in progress

- Based on Wisconsin algorithms
  - Fully implemented & verified
    - 2×2 cluster finder
    - Electron/Photon ID module
    - Cluster overlap filtering
    - Cluster weighting
  - Work started (but postponed to allow SW development
    - Cluster isolation
    - Jet finding

Software objectives:

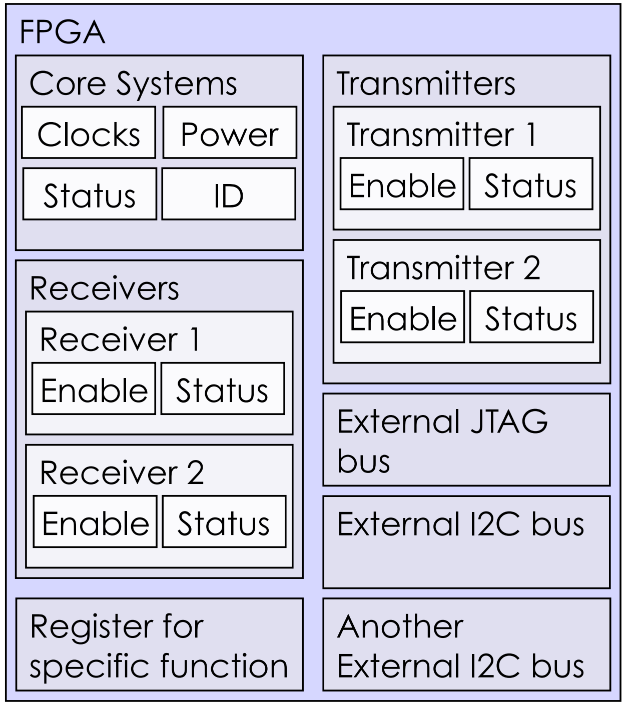
- To build a library of **common, re-useable** software and firmware elements to improve the **quality** and **maintainability** of the system over what currently exists
- To ensure that all elements are **properly documented** and **unit-tested/testable**

Online Software: Dream

Motivation

Common WP1 & WP3 activity

- Firmware is (or at least should be!!!) partitioned into logical subsystems
- These subsystems can contain further subsystems, and so on, all the way down to the register level
- Want a software architecture that reflects this : configurable at both register and subsystem levels
- Aim is to create a library of standard SW and FW elements for drag-and-drop design

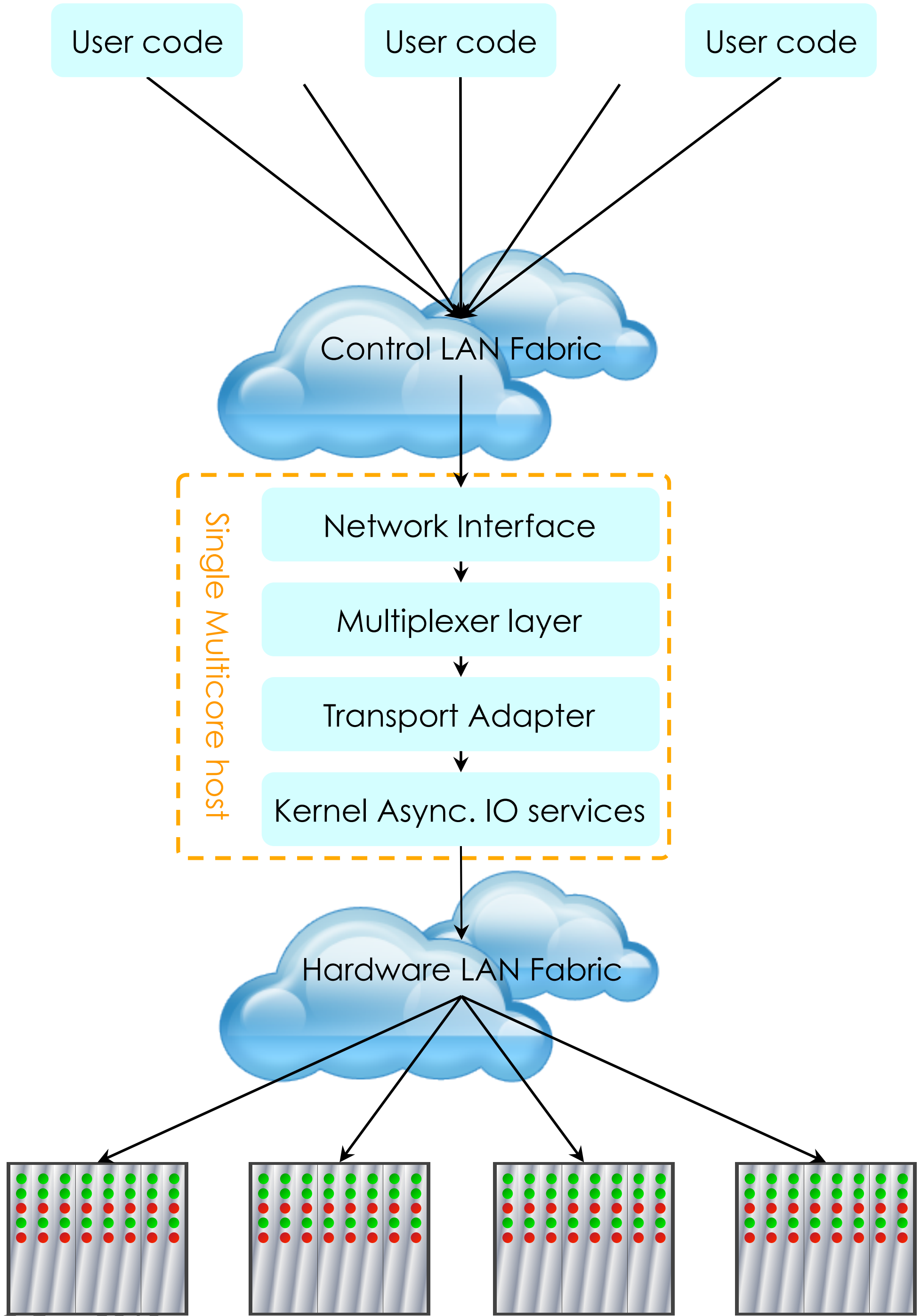


Software: Architecture

- Hardware controller PC separates the Control LAN and the User code from the Hardware LAN and the devices

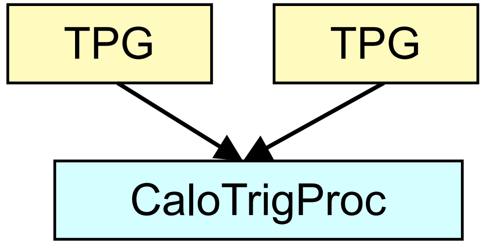
- Unlike current TS architecture, all network traffic hidden from end user

- Made possible by common interface layer within the firmware and mirrored within the software



Objective for the Autumn...

- Simple system to validate core aspects
  - Only 3 cards (same hardware):
    - 2x Pseudo Trigger Primative Generators (TPG)
    - 1x CaloTrig Processor



- Small system, but large amount of work.
- Requires:
  - Working hardware (i.e. MINI-T5)
  - Slow Control (i.e. Ethernet)
  - Link Functionality (i.e. GTX transceivers)
  - Basic Algorithm (e.g. Electron, Not Jets)
  - Basic DAQ

Single uTCA card, but lots of firmware developers !

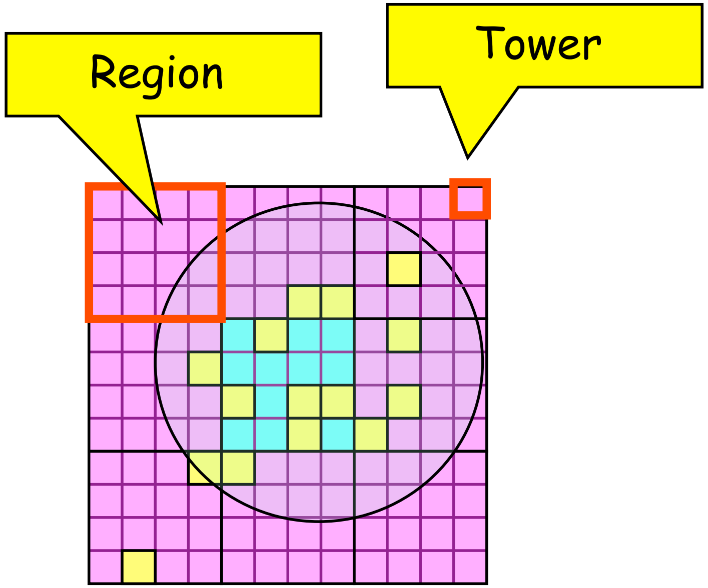
e.g. PseudoTPG & CaloTrigProc use same hardware

New ideas for trigger implementation

- Ideally all jet + electron clustering in single FPGA

- To contain jet centred on middle region requires 3x3 regions
  - i.e. 36 links at 5Gb/s
  - i.e. single region requires large FPGA

- 14x18 regions (excluding HF)
  - More than 252 cards



Extremely inefficient -> Big, expensive system

Data duplication headache (x9)

Conventional

- Process entire detector on each bx
- Deal with electrons/taus first.
- Build jets from earlier energy clustering or take tower data and coarse grain to 2x2 towers.
- Pros:
  - Simple design
- Cons:
  - Less flexible, but does it matter...

Time Multiplexed

- Akin to HLT processor farm
  - Process entire detector over ≈10bx
  - Switch between 10 systems operating in round robin method.
- Latency impact of 10bx regained by fewer serialisation steps
- Pros:
  - Jet+Elec processing in single fpga
  - Processed/boundary area max
  - Scalable: 10 identical systems
  - Redundant: Trigger keeps operating if partition lost, albit at 90%
- Cons:
  - Never been done before

CMS Phase I planning

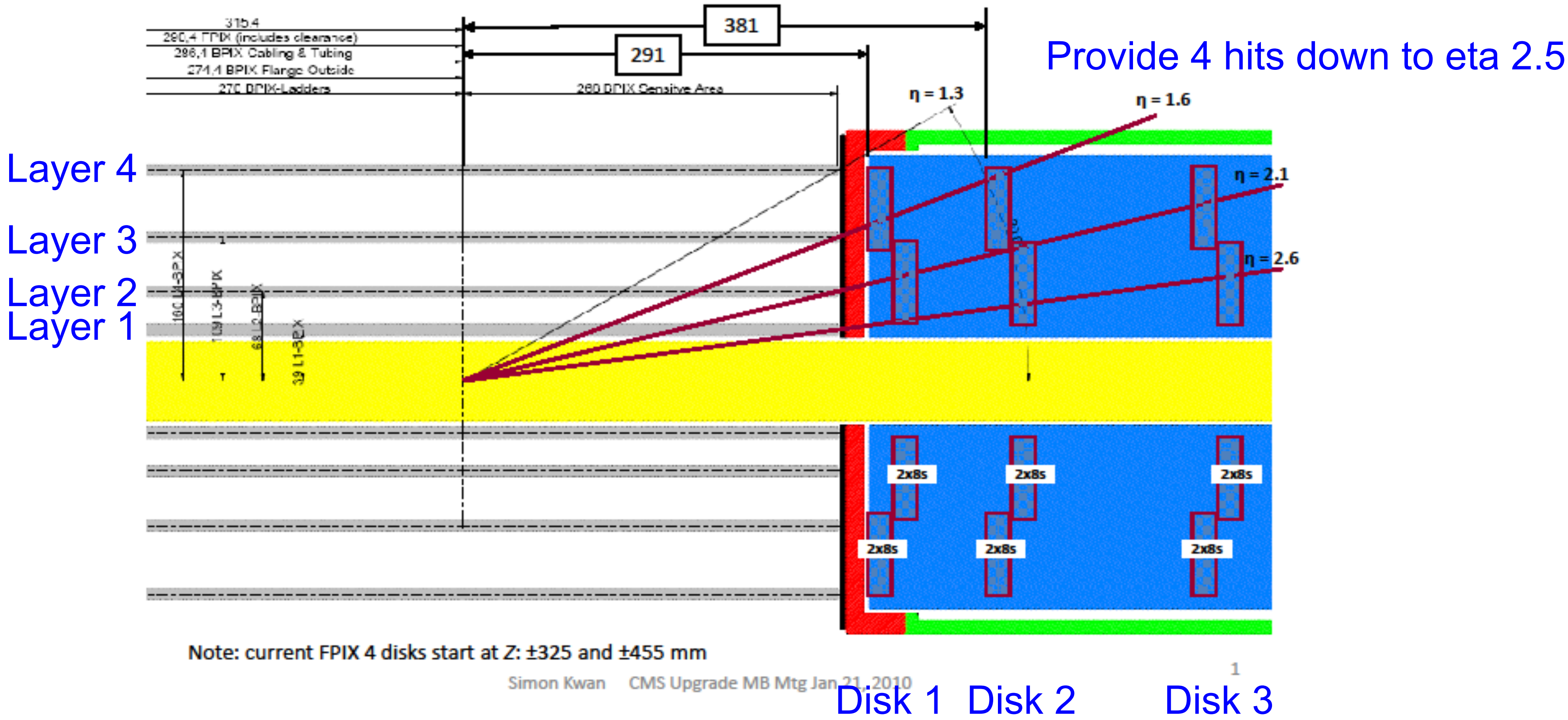
- Replacement pixel detector
  - 4 barrel layers, 3 endcap disks, but substantially reduced material budget
  - enhances track seeding and overall efficiency, impact parameter, b-tagging
- Upgraded (CALO) trigger
  - profit from GCT and technology developments for calorimeter trigger
  - clusters and improved isolation to cope with 2-4 x worse conditions than nominal
- Both systems to be installed in advanced stage of commissioning
  - Pixels to be operated at TIF for 9 months
  - Trigger to operate in parallel with existing system
- Improve performance and minimise negative impact on data
  - be ready for worse case conditions 2×10^{34} $cm^{-2}s^{-1}$ & 50ns bunch spacing
- UK role under discussion
  - pixel needs match DAQ/online expertise, with possible role for mini-T
  - trigger progress more advanced than elsewhere: hardware/firmware/software
- Phase II R&D (CBC and trigger) remains very high priority

Pixel Upgrade: Mechanical layout r-z view

Material budget reduction
~ factor 2.5

All Identical disks (disks in locations to maximize 4-hit eta coverage)

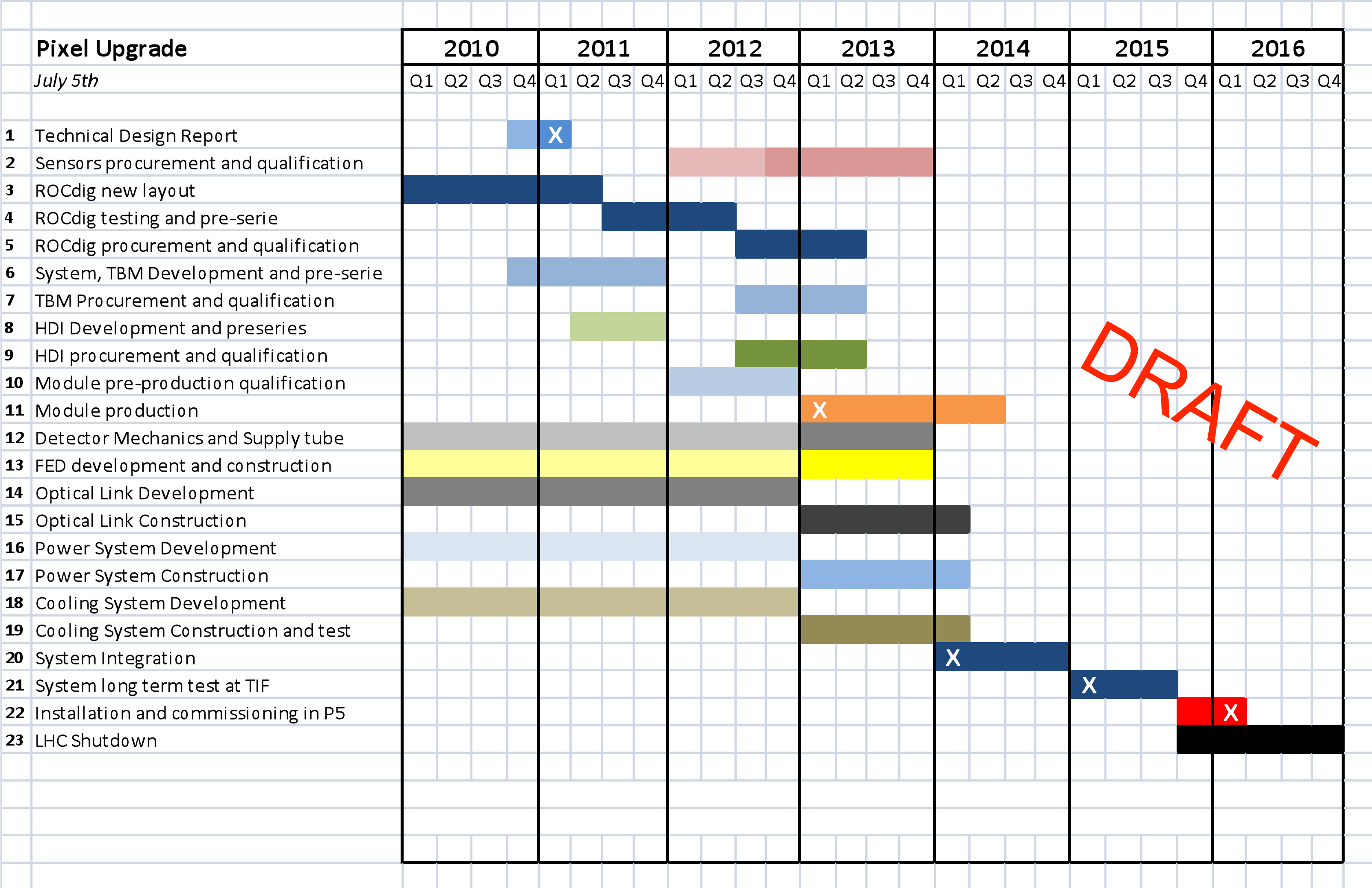
6 disks = (6x68) outer + (6x44) inner = 672 2x8 modules (10752 ROCs)



Note: current FPIX 4 disks start at Z: ±325 and ±455 mm

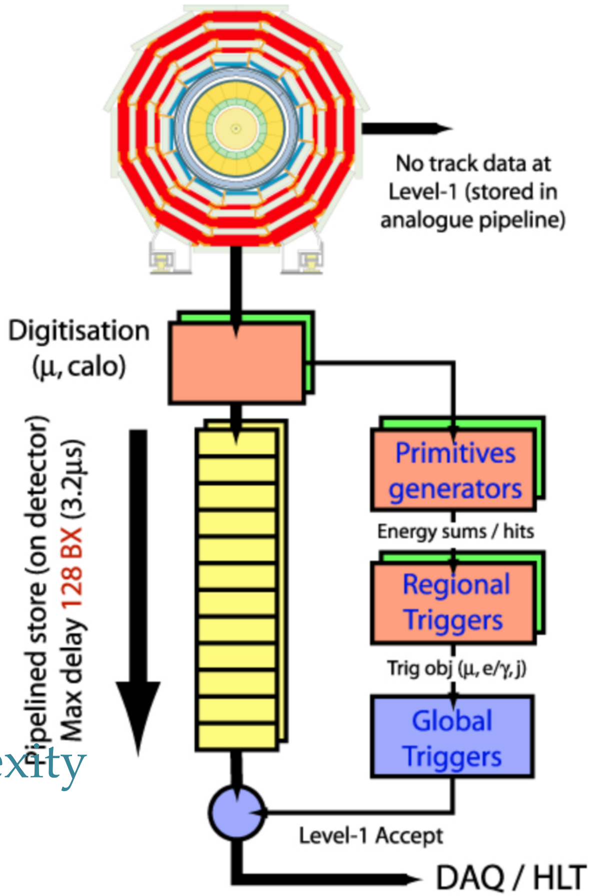
Simon Kwan CMS Upgrade MB Mtg Jan 21, 2010

Proposed Draft Upgrade Plan and Milestones



L1 Trigger: Current Status

- Role of the L1 trigger
  - Unmanageable raw data rate (80TB/s at L=10^{34})
  - Rapid online event selection is necessary
    - Specialised hardware achieves ~400-fold reduction in data volume
  - Preserve significant events (physics, bg, calib) with high and well-understood efficiency
- Trigger implementation
  - Trigger designed to operate to L=10^{34} only
  - This task was at the edge of late-90's technology
  - Some compromises made in current hardware
    - Reduced granularity; inflexibility; hardware complexity
  - The physics performance is limited by communications and processing bandwidth
    - Defined by selection efficiency versus background rejection
  - Substantial improvements possible in modern technology, even at high lumi



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Drivers for L1 Upgrade

- Improve physics performance
  - Increased processing power gives finer space / energy resn for trigger objects
  - Trigger algorithms operate more efficiently, with more stringent isolation criteria
  - Make use of additional detector elements in muon system & HCAL
- Improve robustness & safety at high lumi
  - Increased margin against a range of instrumental effects at high lumi
  - Less impact on algorithms from increasing noise & occupancy in the detector
- Simplify and consolidate hardware & software
  - Replace large and complex electronics with compact common hardware modules
  - Common software tools for allow rapid debugging & performance monitoring
- Pave the way for the Phase-II upgrade
  - Updated trigger architecture should allow inclusion of track data at later time
  - Improved calo / muon performance vital for matching with tracker data

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Schedule

- 2010 – 2012
  - R&D on common trigger hardware platform - under way
    - Based on large FPGAs with many optical serial links; first implementation is the UK Mini-T card
  - R&D on online software / firmware to support common hardware - under way
  - Technology demonstrator and architecture choices: Dec 2011
- 2012 – 2014
  - Installation of 'parasitic' trigger slice alongside current system
  - Production of new trigger hardware & corresponding firmware / software
  - Full stand-alone system test: Dec 2014
- 2015 –
  - Installation and commissioning of upgraded L1 systems
  - NB: 'commissioning' period for current L1 was ~2 years

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Summary and Issues

- Overall good progress
  - no significant technical concerns at this point
- Finances
  - slow initial spend but as expected given uncertainties in last 1-2 years
  - financial risk: limited due to good technical progress
    - Working Margin (£230k) allows redeployment of funds should it be necessary
    - will be released gradually with progress
- Staff changes
  - C Foudas (Imperial), C Hill (Bristol) have now left
- CMS and LHC upgrade planning
  - schedule now much clearer but will still depend on progress with LHC machine
  - UK planning is overall very compatible
  - Details of contributions to Phase I upgrades to be clarified in next 6-12 months
    - with all other collaborators, within context of LHCC approval process
- Largest uncertainty at present remains overall economic circumstances