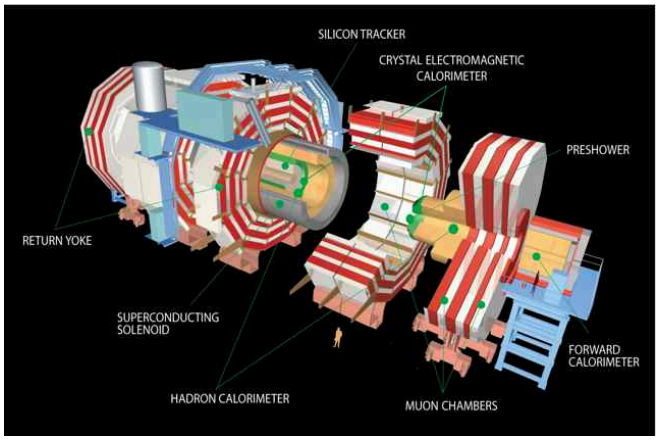
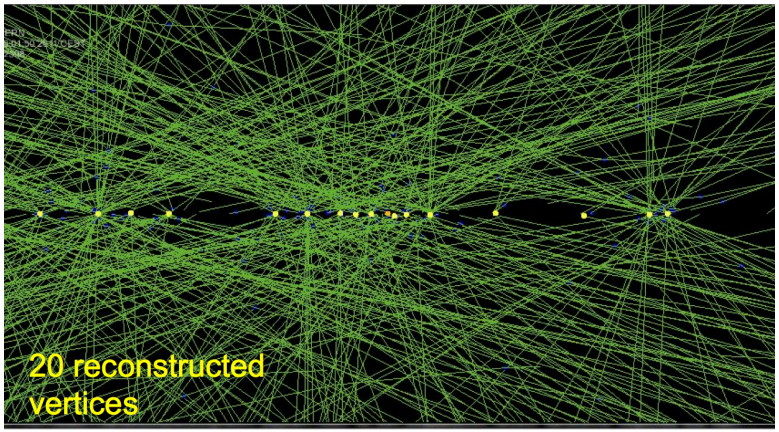




UK CMS Upgrade Oversight Committee

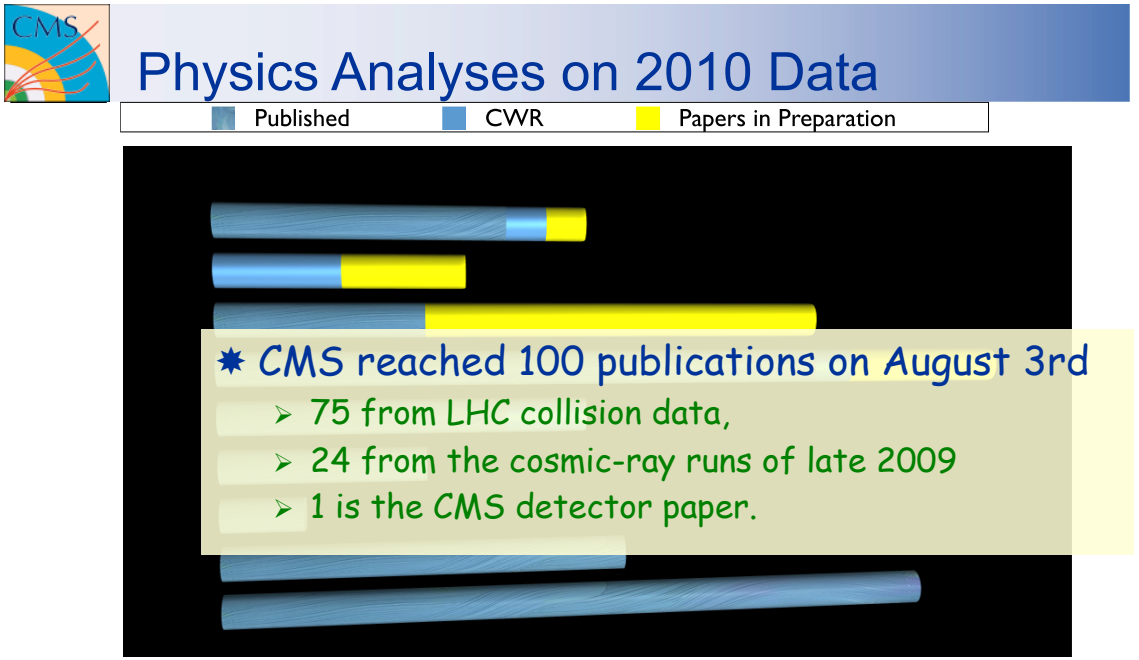
5 October 2011

University of Bristol
Brunel University
Imperial College London
Rutherford Appleton Laboratory

Geoff Hall

Overview

- CMS status
- LHC status and future plans
- UK R&D progress report
- Finances
- Future
  - CMS plans
  - UK CMS plans
- Issues



69 published, 7 in CWR, 18+ in preparation
https://twiki.cern.ch/twiki/bin/view/CMSPublic/PhysicsResults
Papers, and Physics Analysis Summaries (PAS): http://cdsweb.cern.ch/collection/CMS

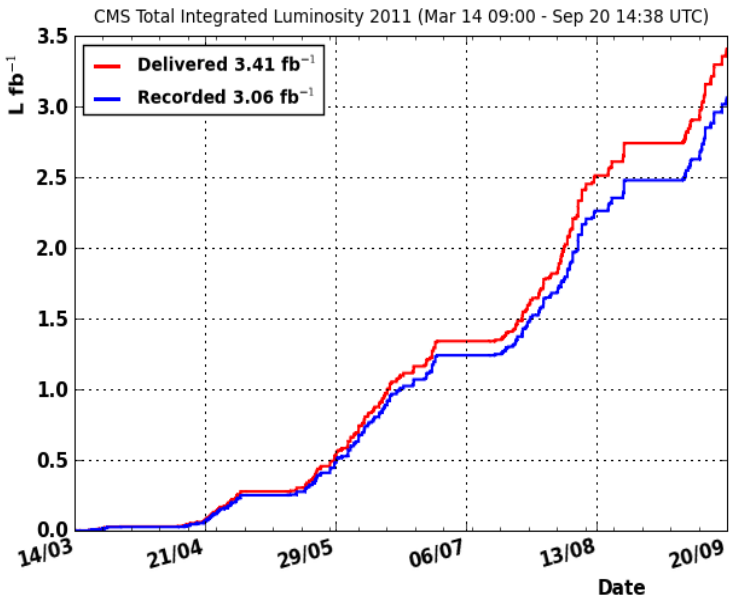
21 September 2011 LHCC CMS Status Report -- D. Acosta UF University of Florida 7

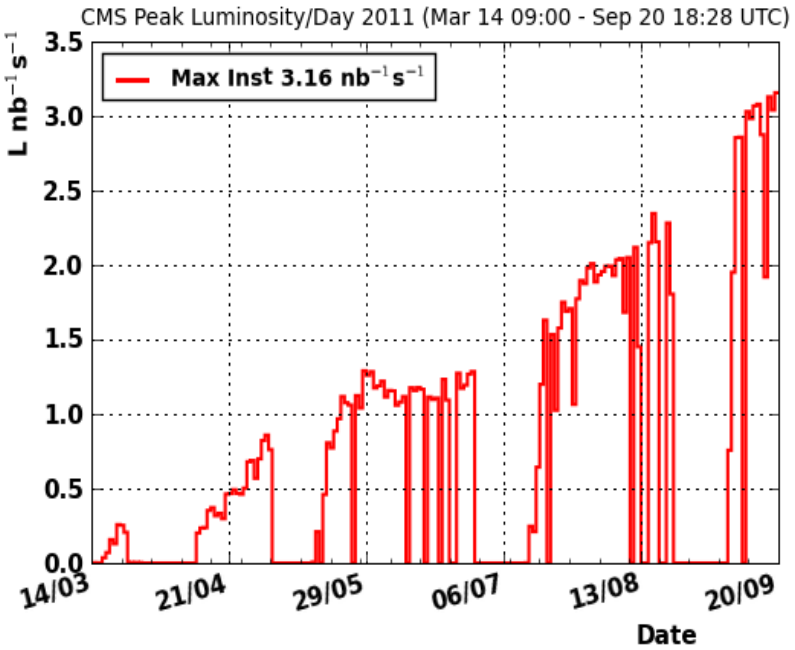
CMS status

- 2011 has progressed very well indeed
  - conservative LHC performance assumptions have proved to be so
- LHC (recent summaries at EPS and Sept LHCC)
  - instantaneous luminosity records continue to be broken
    - takes time to recover from MDs but performance is excellent
  - 5 fb^{-1} very likely by end of p-p running
- Physics
  - steady, high output of publications
- Detector
  - efficient operation, with no significant problems

LHC operation

CMS perspective





Prompt recovery from the last Technical Stop. β^***=1m** commissioned.

New record inst. Luminosity 3.29x10^{33} [cm^{-2}s^{-1}]. New records in integrated luminosity delivered in a single fill (117.4pb^{-1}); recorded by CMS (113.4pb^{-1}) 96.5% efficiency.

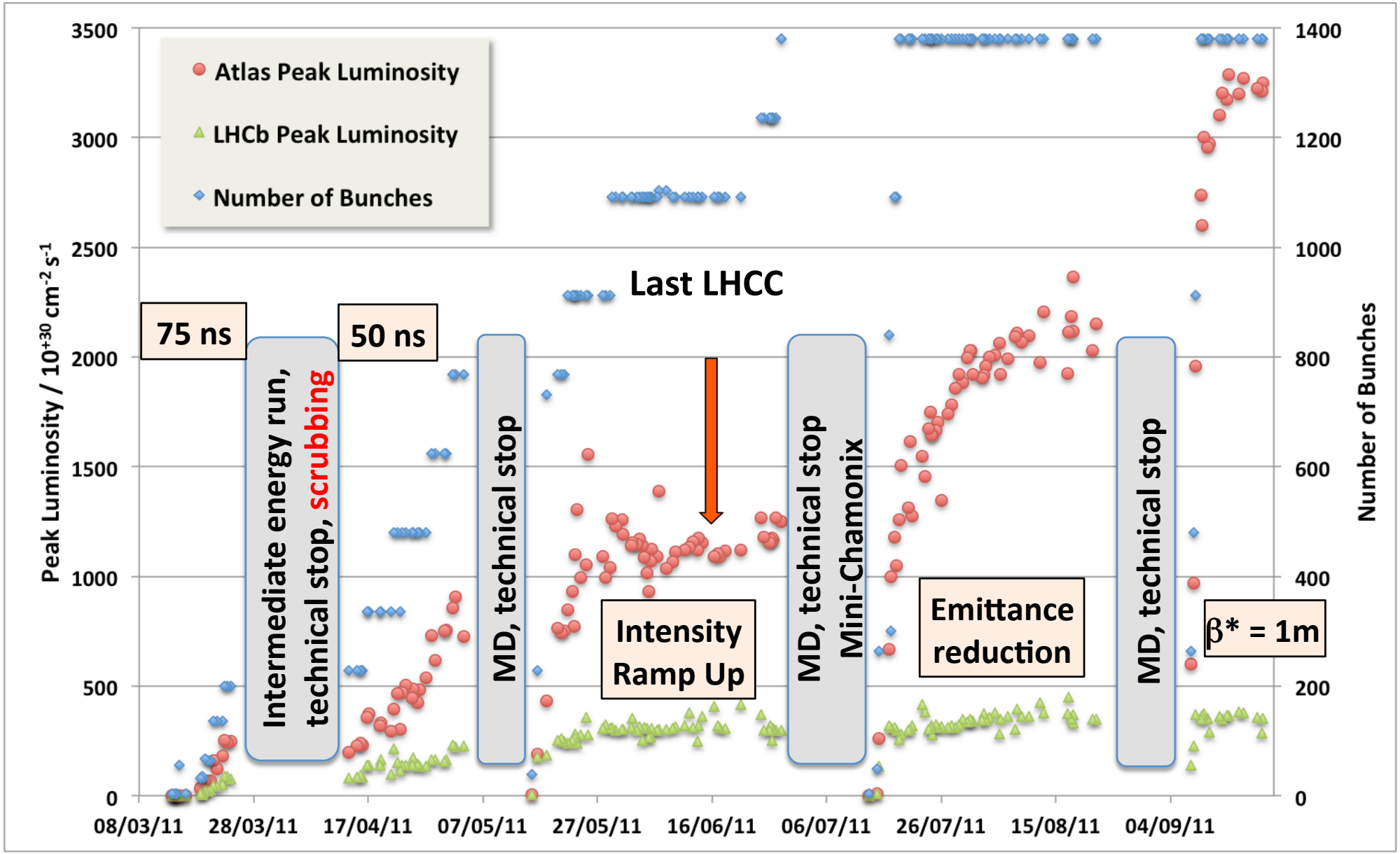
3.41fb^{-1} delivered by LHC and **3.06fb$^{-1)}$** recorded by CMS (90% eficiency).

707pb^{-1} delivered in 13 days (54pb^{-1}/day and 37 days to go).

By maintaining or increasing this pace it seems possible to reach or exceed **5fb^{-1}** by the end of October.

LHC Status : 2011 – so far ...

Machine perspective



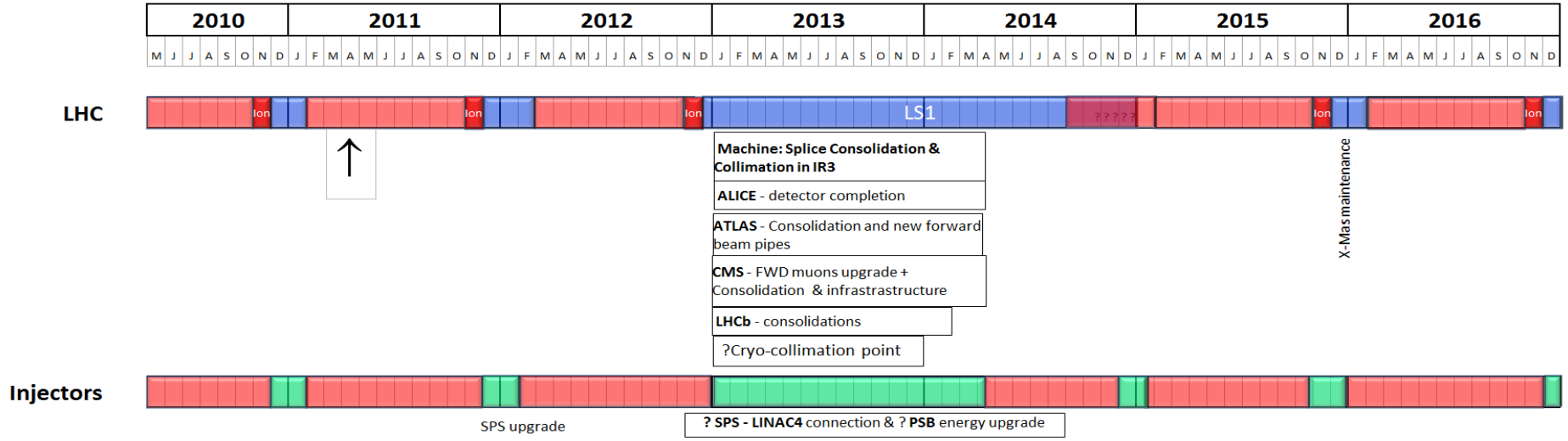
LHC future plans

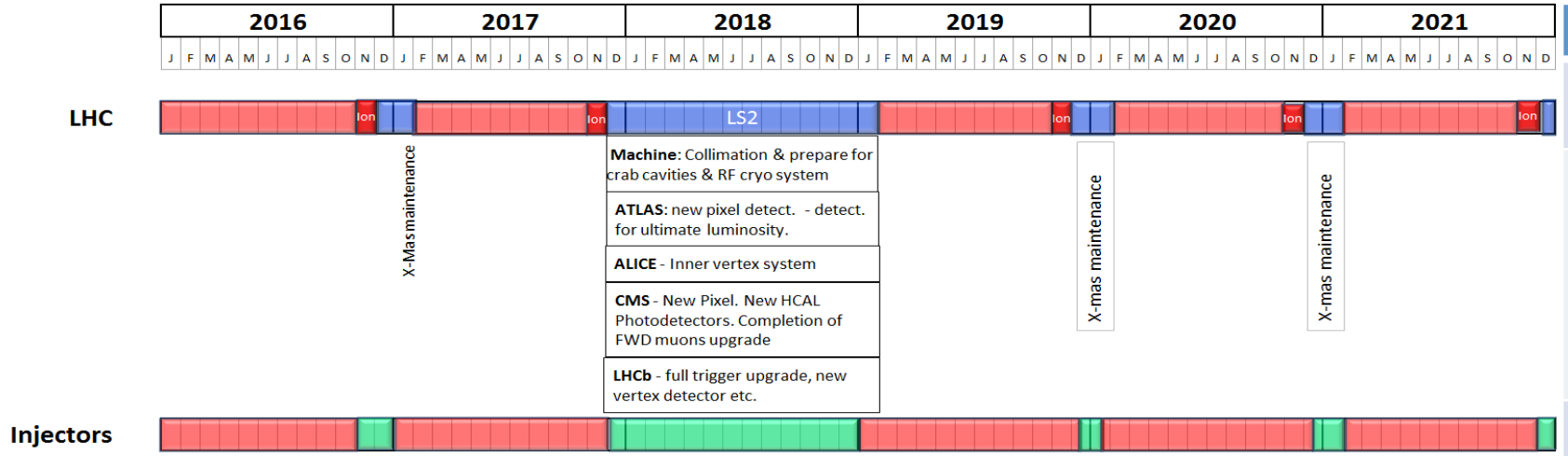
- LHC operational conditions in 2012 still to be defined
  - possible increase in energy
    - to be evaluated at Chamonix 2012 (Feb)
  - operation at 25 or 50 ns?
- Latest 10 year plan presented at EPS in July

- Long Shutdown dates
  - LS1: 2013-2014 (2012-2013 in July 2010 planning)
  - LS2: 2018 (2016)
  - LS3: 2022- (2020-)
    - significant delays compared to previous plans – impact under study
    - complex mixture of scheduling, budgeting, technical considerations

New rough draft 10 year plan

Not yet approved!





2022

LS3

Installation of the HL-LHC hardware.
Installation of LHeC
Preparation for HE-LHC

Previous schedule in backup slides

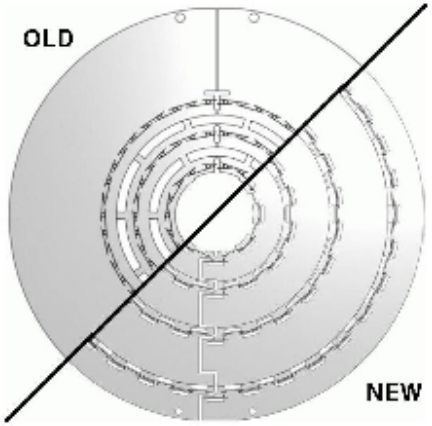
UK & CMS upgrade progress

- WP1
  - contributions to CMS Tracker software optimisation and performance studies
  - continued excellent collaboration with WP3 firmware and software
- WP2
  - excellent CBC results from detailed testing
  - CBC-sensor module operated in test beam in September
  - progress with FED-related firmware
- WP3
  - further production of Mini-T5
  - demonstrator system in operation in lab
  - excellent promise for Time Multiplexed Trigger architecture
- WP4 - new pixel-related activity
  - early foundations laid for DAQ involvement, in common project
- the word “excellent” may be overused above but genuinely indicates the promise for UK role in CMS upgrade

WP1: Overview

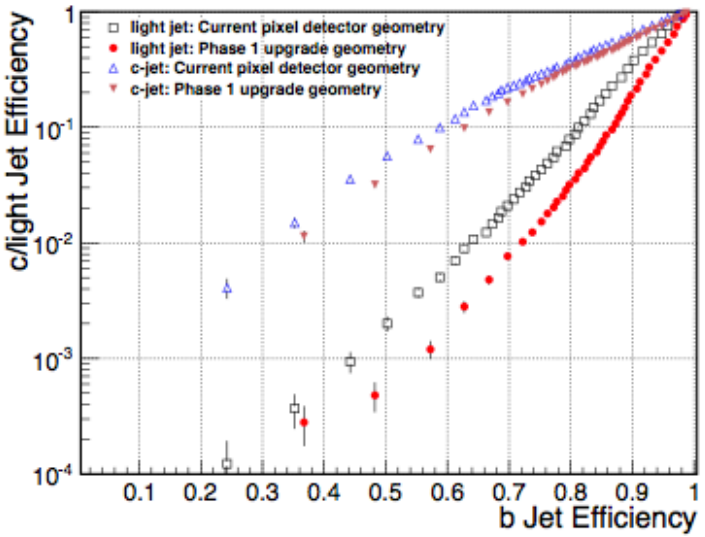
- Triggering
  - Provision of online software & 'core' firmware
  - MicroHAL / IPbus system becoming widely adopted
  - Emphasis on support & incremental improvements to performance / functionality
  - Studies of upgrade L1 calo trigger algorithms
  - Note published on upgrade architectures
    - Including near- and longer-term upgrades for calo, muons, tracking

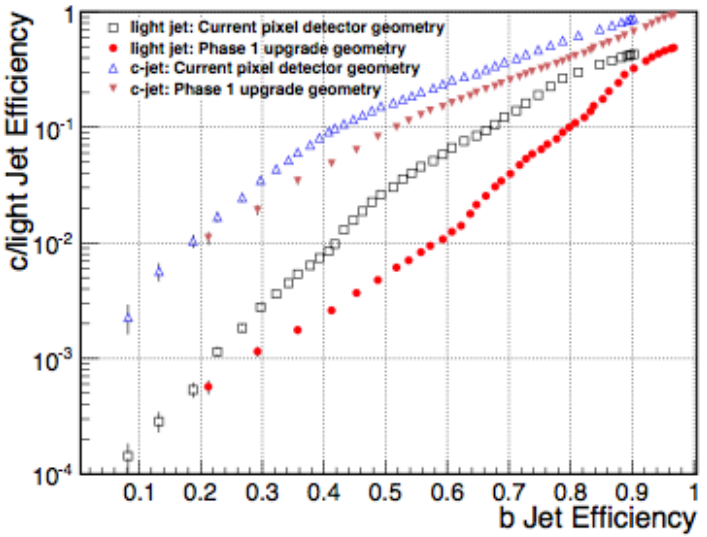
- Tracking (Phase 1)
  - Optimisation / layout studies continue after TP
  - Optimisation of tracking algos & code performance
  - Integration of upgrade and baseline tracking code
  - New techniques to validate tracking performance
  - Significant work for near-term high PU runs
    - 'Upgrade' issues now becoming relevant in 2011



WP1: Tracking Progress

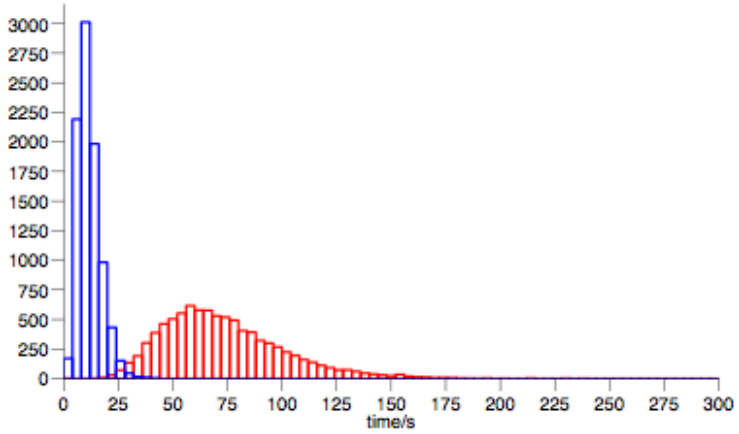
b-tag performance at <n>=0 PU

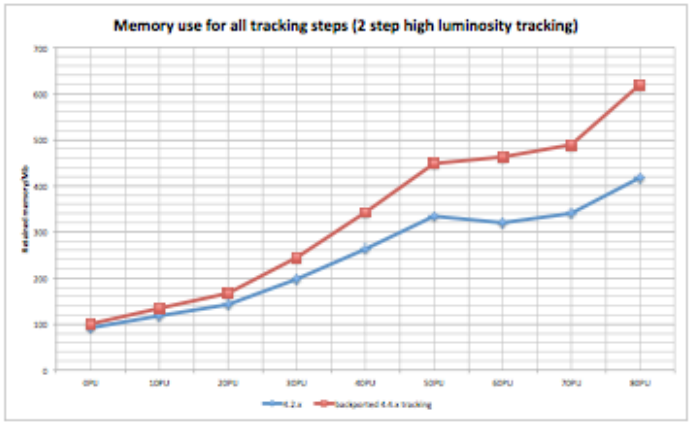




b-tag performance at <n>=50 PU

CPU time evolution (s / evt)

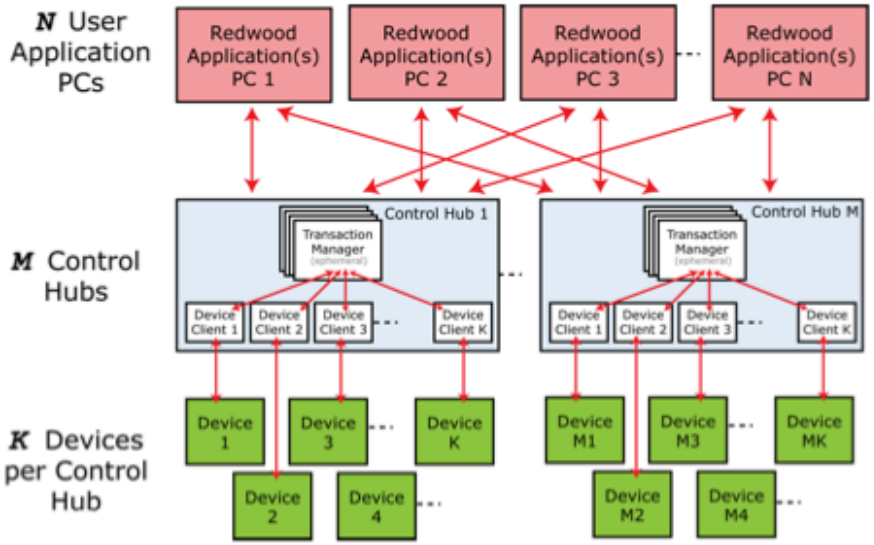




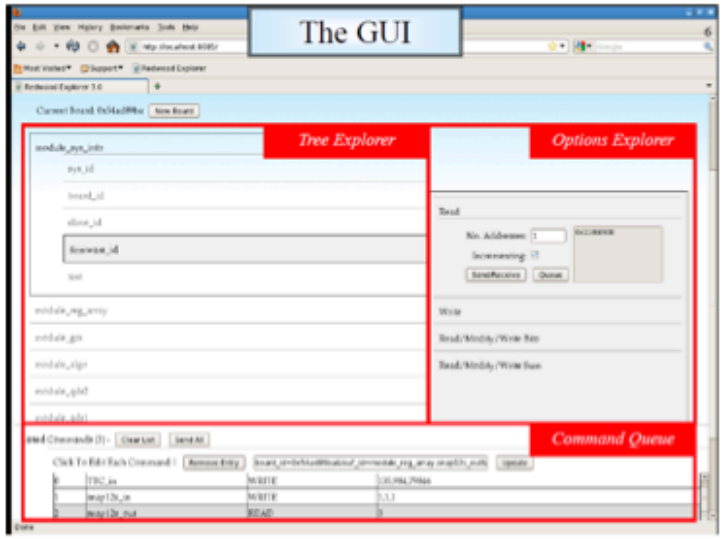
Retained memory evolution

- Significant progress on performance tuning / resource usage
  - CPU under control, but memory consumption a serious issue

WP1: Trigger Progress



Overall IPbus architecture



Redwood Explorer (MicroHAL GUI)

Software / firmware validation platform at Bristol

WP2

- Detailed testing of CBC
  - select a few example results
    - last report showed results from first week only
  - radiation tests – total dose and SEU – for 2012
    - temperature studies ongoing – (Bristol: looks good)

- Module and system development
  - continues with other CMS institutes, especially CERN
  - aiming for short-strip PT modules for triggering **and** tracking
    - expect to use C4-type bump bonding
  - discussions on how to adapt also for a strixellated trigger module

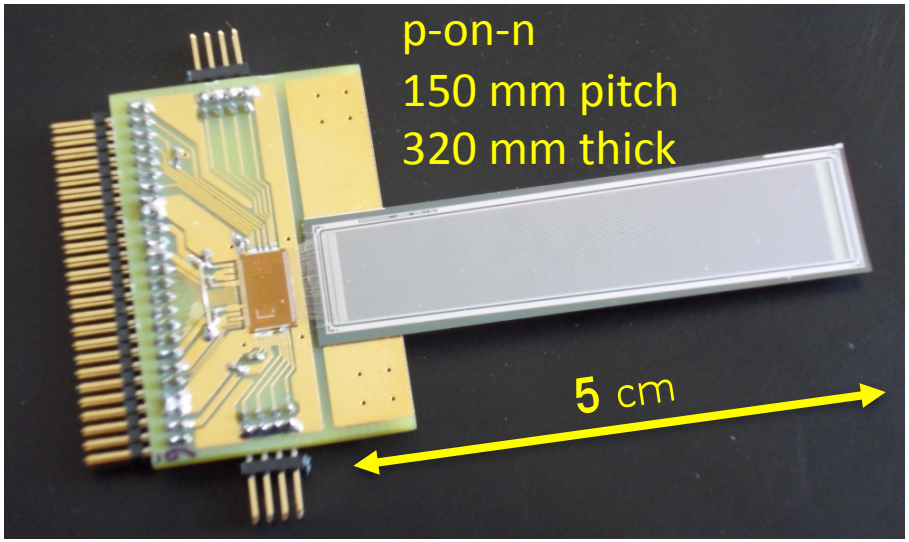
More details and plots in backup slides

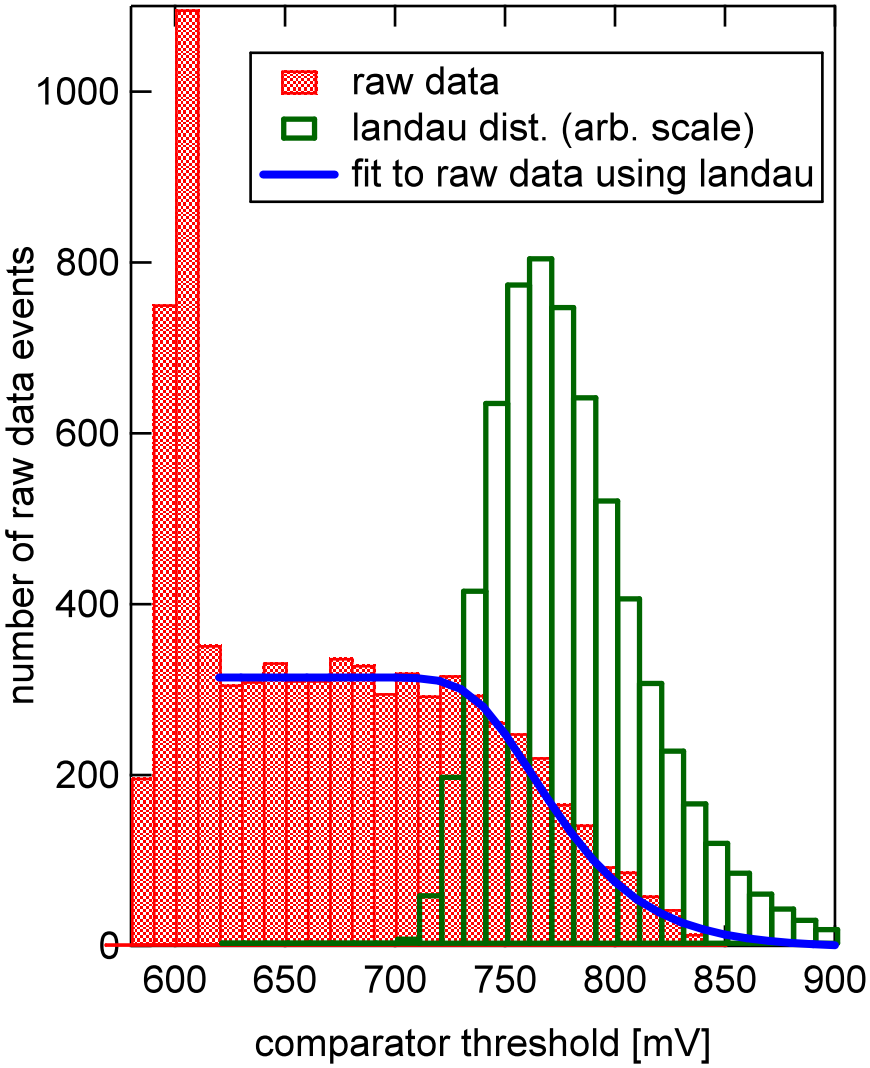
CBC principal results

- Fast low power (SLVS) and slow (I2C) interfaces
  - data/clock/trigger and control
- Binary, so scan thresholds for gain and linearity ("S-curves")
  - individual channel thresholds tuned for uniformity
- Powering
  - chip includes LDO regulation (excellent performance) and DC-DC conversion (very promising but details of impact under investigation)
- Power consumption
  - analogue in good agreement with simulations
  - digital much less than (pessimistic) estimates: <50µW/channel
  - $P_{total} < 180 + 21 \times C[pF]$ µW/channel - ie. < 300µW for C = 5 pF

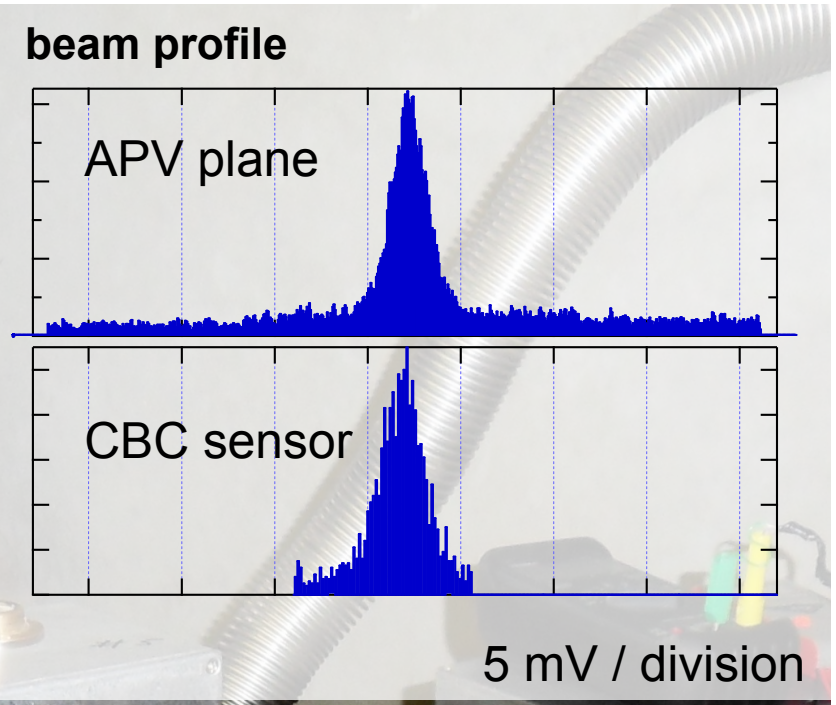
CBC-sensor module

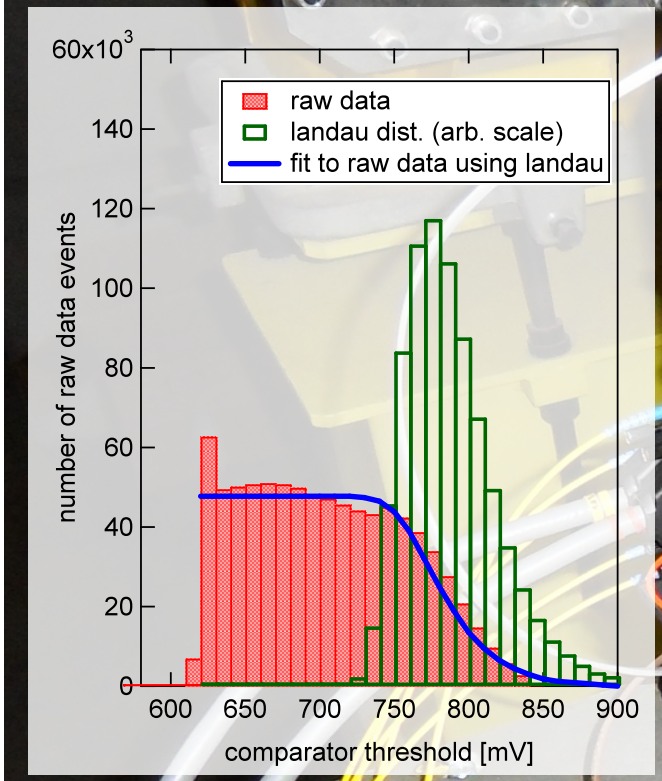
- Lab measurements with Sr β source and time-stamped scintillator trigger
  - σ_{noise} = 836 e
- sweep comparator threshold for pulse height spectrum





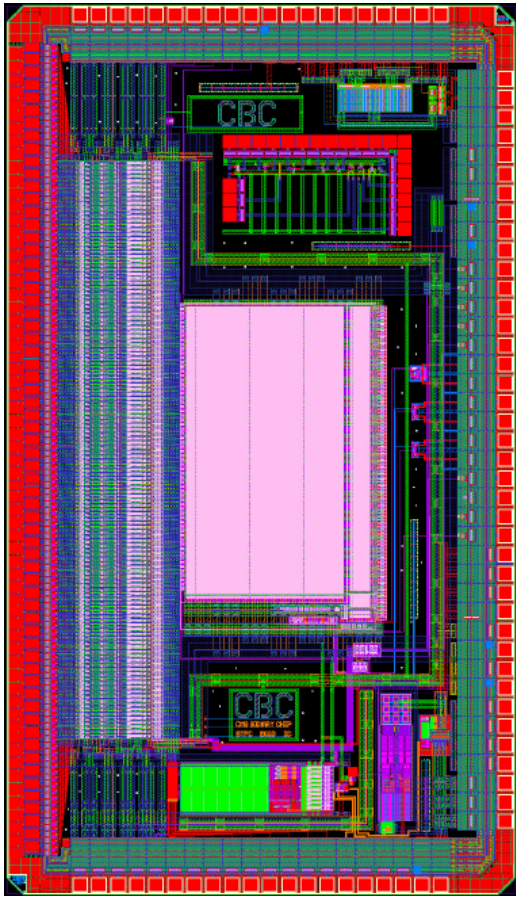
test beam - first results





Next CBC design

- C4 (coarse pitch, low cost) bump bonded
  - double-layer, short-trip pT module
  - submission Q1 2012



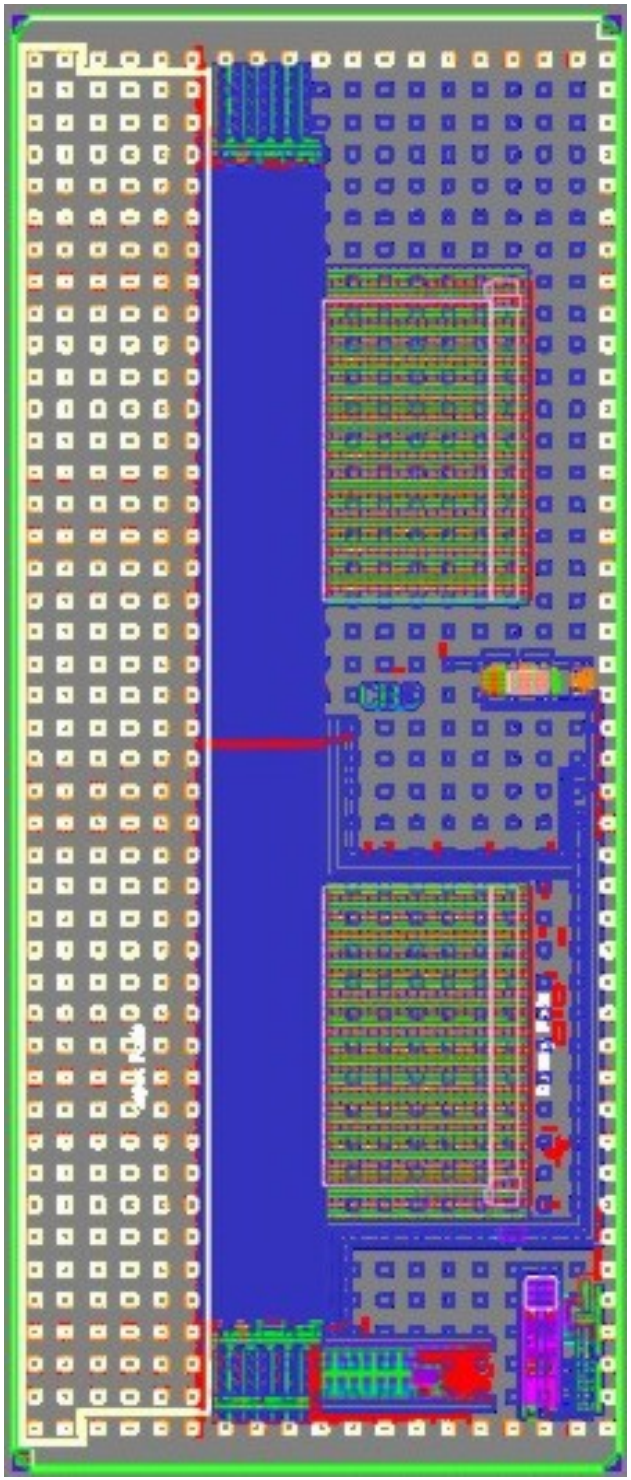
V1

128 channels wirebond:
50 µm pitch
7mm x 4mm

V2

256 channels bump-bond:
250 µm pitch
11.4mm x 4.75mm

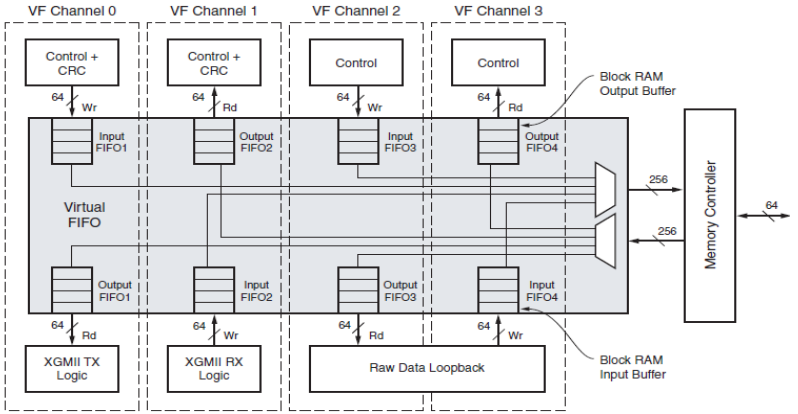
layout by
Davide Braga (RAL)



WP2: SFED Progress

- GBT FPGA Interface:
  - CERN GBT module design ported to Xilinx Virtex 6 development board

- Memory Interface FPGA Firmware
  - Implemented DDR3 Memory Interface.
  - Based on Xilinx Virtual FIFO core.
  - Made benchmark measurements.
  - Adapting for multiple GBT streams.



Virtual FIFO DDR3 Interface

- PC Controls
  - Integrated the CMS IPbus control firmware.
  - Adapted Python scripts.
  - Allows control and monitoring via GbEthernet.
  - Makes design compatible with Mini-T card.

- Carried out short feasibility study for Pixel Readout card

WP2: SFED Plans 2012

- Port GBT and Memory Interface to Mini-T5 µTCA card:
  - establish µTCA crate with Mini-T hardware and firmware.
  - Adapt existing design for QDRII memory added to Mini-T5.
  - Test data transfer over Mini-T5 optical links.

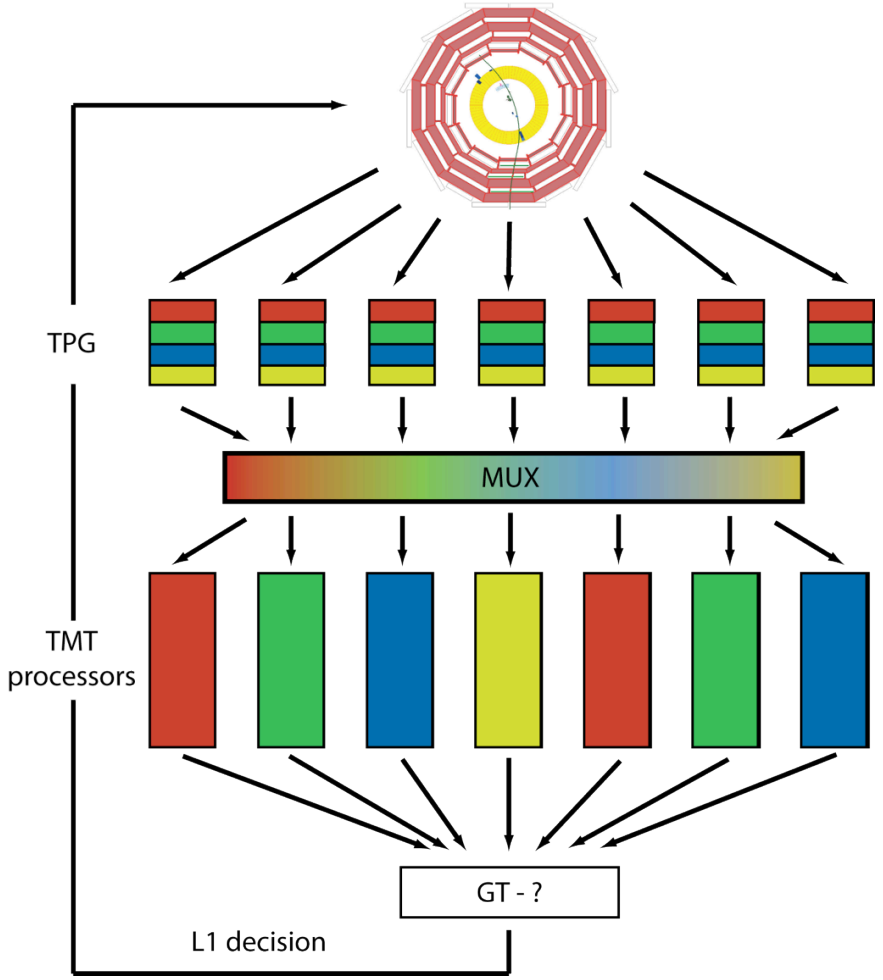
- Integrate SFED firmware with CBC module control and readout
  - Work towards system test.

- Possible test with CERN GLIB µTCA card
  - Virtex 6 with DDR3.
  - Develop FPGA Mezzanine Card for CBC link interface

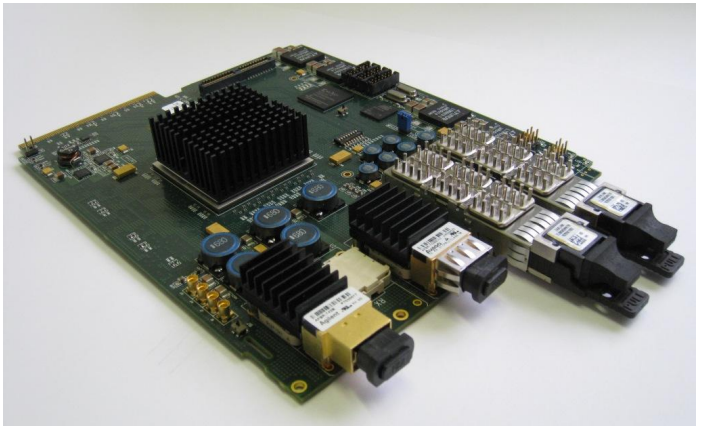
- Now ready to integrate activity more into mainstream
  - profit from WP1 & WP3 progress

WP3: Trigger Development

- Demonstrator system
  - Operating in lab, with firmware, and well supported software framework from WP1 collaboration
- Architecture decision imminent
  - (by Christmas?)
  - CMS review committee formed with mandate from Trigger PM
  - First meeting 14 October, with presentations



WP3: MINI-T5 Development



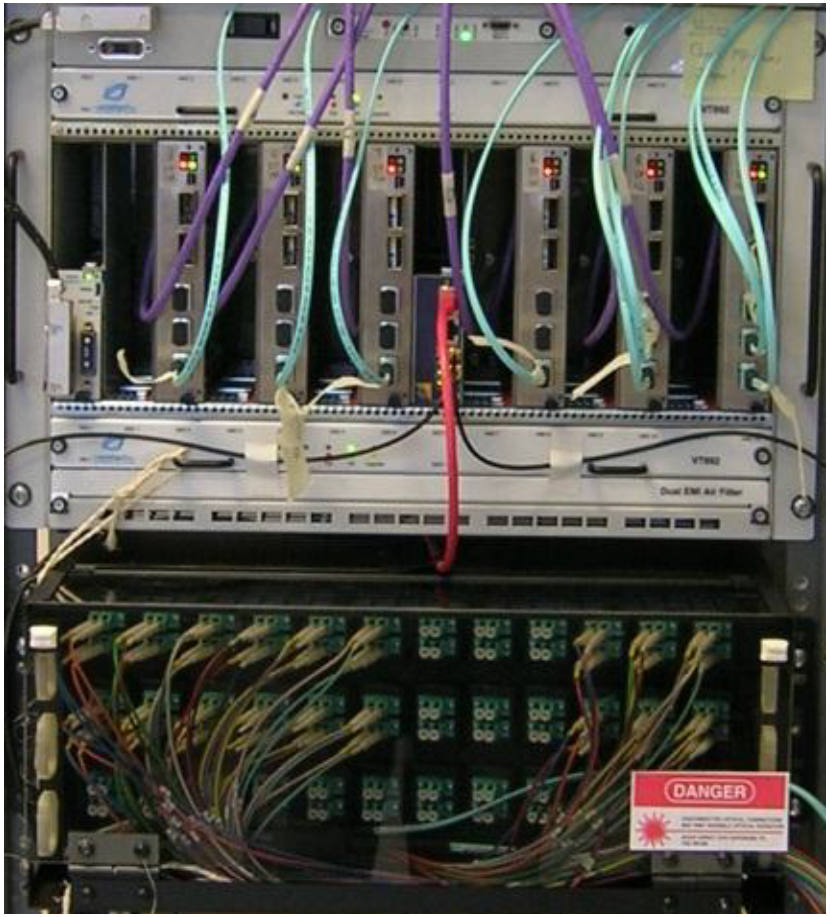
- Three card types produced:
  - Rev 0: Original
  - Rev 1: Alternate optics (supply issue)
  - Rev 2: QDR II RAMs added (request)

- 12 Rev-2 cards manufactured with the target FPGA
  - 3 batches of R2 cards (2+5+5) to mitigate risk
  - 10 pass all basic tests (i.e Optical links, QDR II, PROM, uC, CPLD, Ethernet)
  - 2 will require rework because of faulty power modules

- Core development system at Imperial will require 6-8 cards.
  - Additional cards distributed to Bristol, RAL, and CERN (Meyrin and Integration Hall)

WP3: Demonstrator System

- All parts installed except US card (AMC13)
  - should arrive within a few months (prototypes exist)
  - Parts include hardware such as MINI-T5, but also less visible parts, such as MicroHAL (communication & control system) and the firmware
- Gain experience of all aspects of complete system
  - Communication, Fast Control & Feedback, Clock, System Updaters…



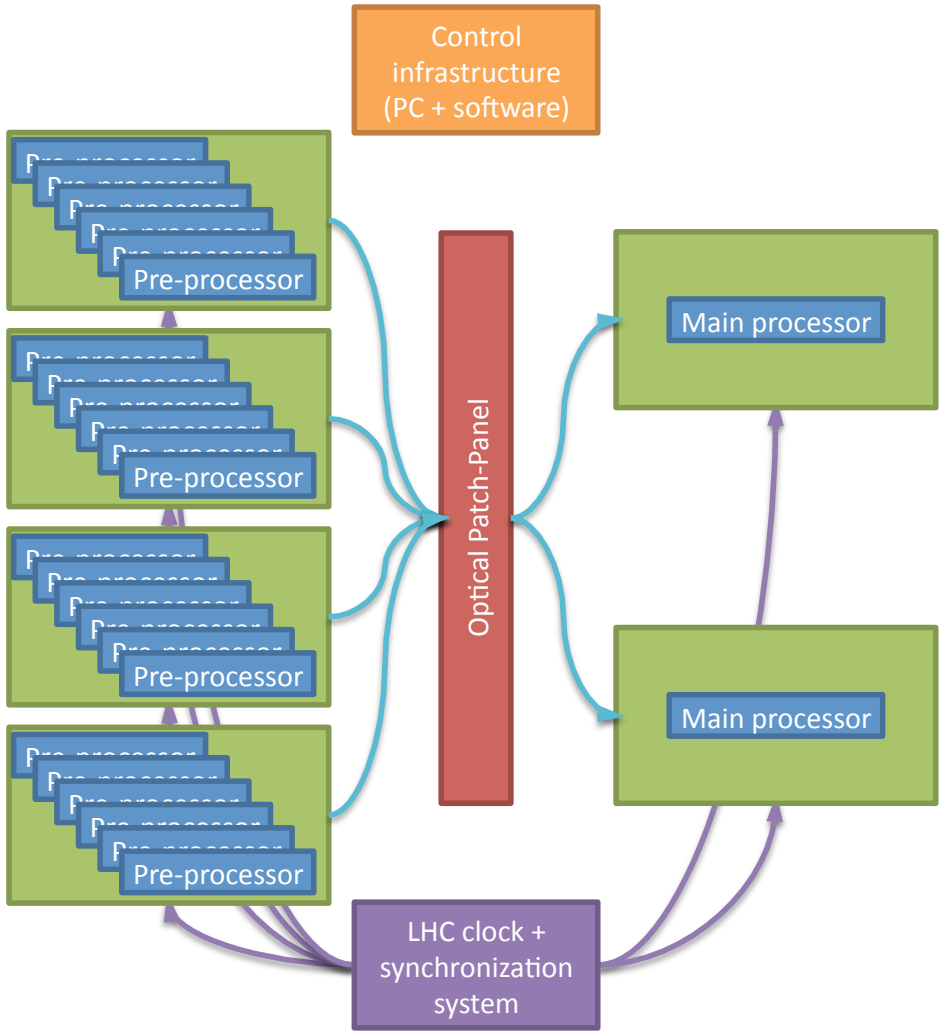
WP3: Demonstrator System (continued)

…includes all the key hardware of a full time-multiplexed system:

- 24 independent pre-processor firmwares spread across 4 Mini-T5 boards
- 2 of the 12 outputs from each pre-processor firmware connected to optical fibre
- "Cross-over" of links in optical patch-panel
- 2 main processor boards each receive 24 fibres, one from each pre-processor firmware

Send test patterns to demonstrate correct interconnection and synchronization

Send Monte-Carlo data to demonstrate receipt of an entire event and to test algorithms



Has successfully demonstrated transmission, capture and synchronization of time-multiplexed data

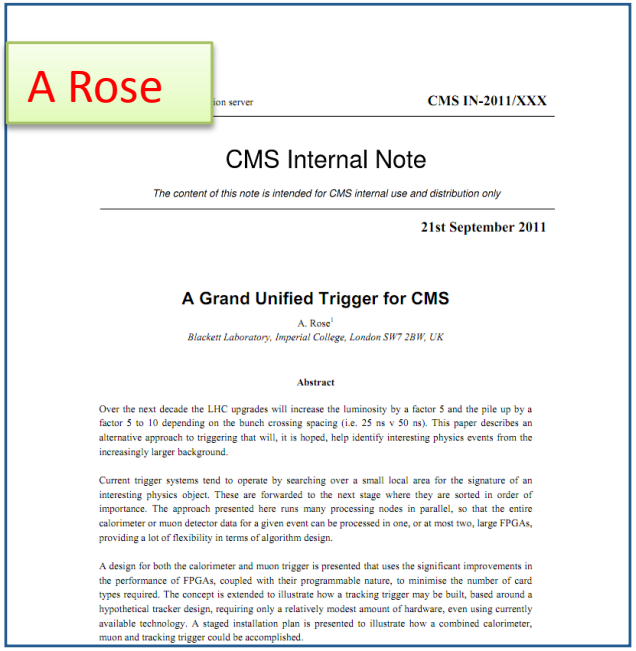
WP3: Triggering strategy development

- Beyond the Phase I upgrade

- Comprehensive study looks at underlying assumptions for triggering and limitations of the current system

- CMS muon trigger may be built with the same hardware as the CMS calorimeter trigger
  - Fewer card types = lower technological risk, lower production cost, better validation, easier to maintain
- requires approx. ¼ as many new boards for trigger upgrades as a conventional trigger architecture
- shows potential to adapt generic tracking trigger

A Rose



CMS IN-2011/XXX

CMS Internal Note

The content of this note is intended for CMS internal use and distribution only

21st September 2011

A Grand Unified Trigger for CMS

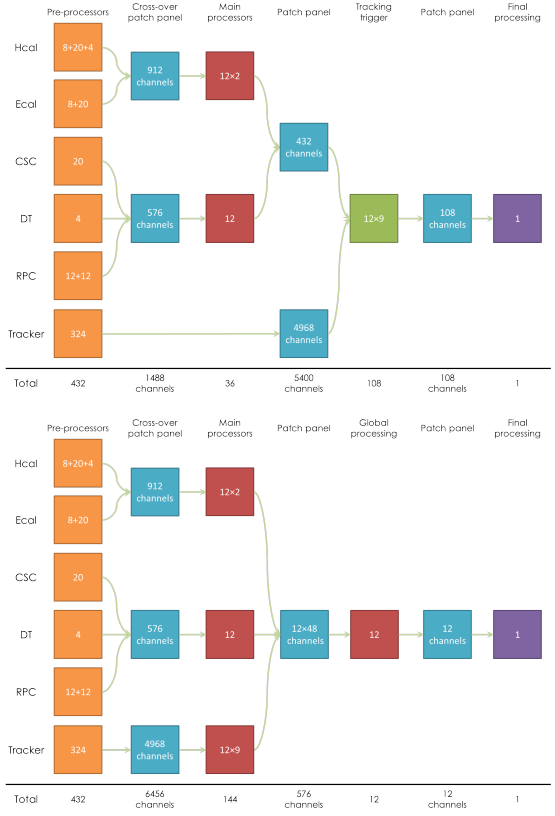
A. Rose[1]
Blackett Laboratory, Imperial College, London SW7 2BW, UK

Abstract

Over the next decade the LHC upgrades will increase the luminosity by a factor 5 and the pile up by a factor 5 to 10 depending on the bunch crossing spacing (i.e. 25 ns v 50 ns). This paper describes an alternative approach to triggering that will, it is hoped, help identify interesting physics events from the increasingly larger background.

Current trigger systems tend to operate by searching over a small local area for the signature of an interesting physics object. These are forwarded to the next stage where they are sorted in order of importance. The approach presented here runs many processing nodes in parallel, so that the entire calorimeter or muon detector data for a given event can be processed in one, or at most two, large FPGAs, providing a lot of flexibility in terms of algorithm design.

A design for both the calorimeter and muon trigger is presented that uses the significant improvements in the performance of FPGAs, coupled with their programmable nature, to minimise the number of card types required. The concept is extended to illustrate how a tracking trigger may be built, based around a hypothetical tracker design, requiring only a relatively modest amount of hardware, even using currently available technology. A staged installation plan is presented to illustrate how a combined calorimeter, muon and tracking trigger could be accomplished.



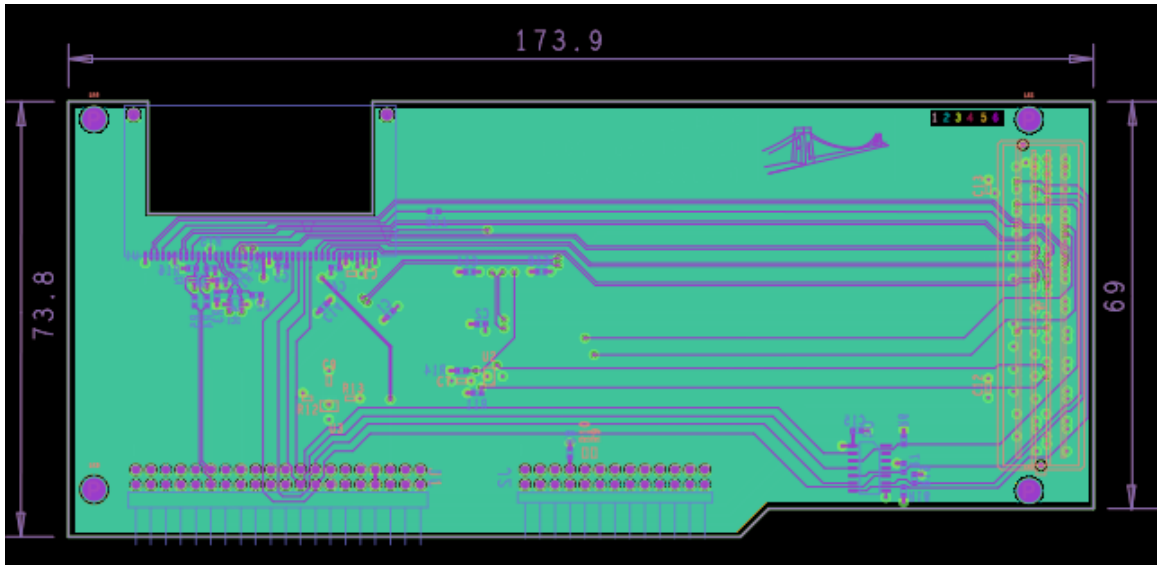
WP3: 2012 Plans

- Demo/Dev system will continue to play an important part
  - Limited number of Main-Processors in test system allows us to create many virtual PPs in a single card.
  - Can simulate the detector with RAMs and play data through time multiplexer and test algorithms.

- Focus has now shifted to final system and hardware requirements
  - Despite preference for TMT, developments remain flexible wrt choice of architecture (i.e. Conventional or Time-Multiplexed Trigger)

WP4 : pixel detector DAQ and test system

- RAL PPD has been exploring opportunities to contribute to pixel testing
  - with objective of eventual role in pixel DAQ (requested by pixel management)
    - K Harder, T Durkin, G Zhang, D Sankey
- Upgrade of existing USB test board
  - developing new version to match digital ROC – first versions in hand
  - firmware under development
- Expect working system within weeks
  - allows months of testing before next ROC available



WP4 future plans

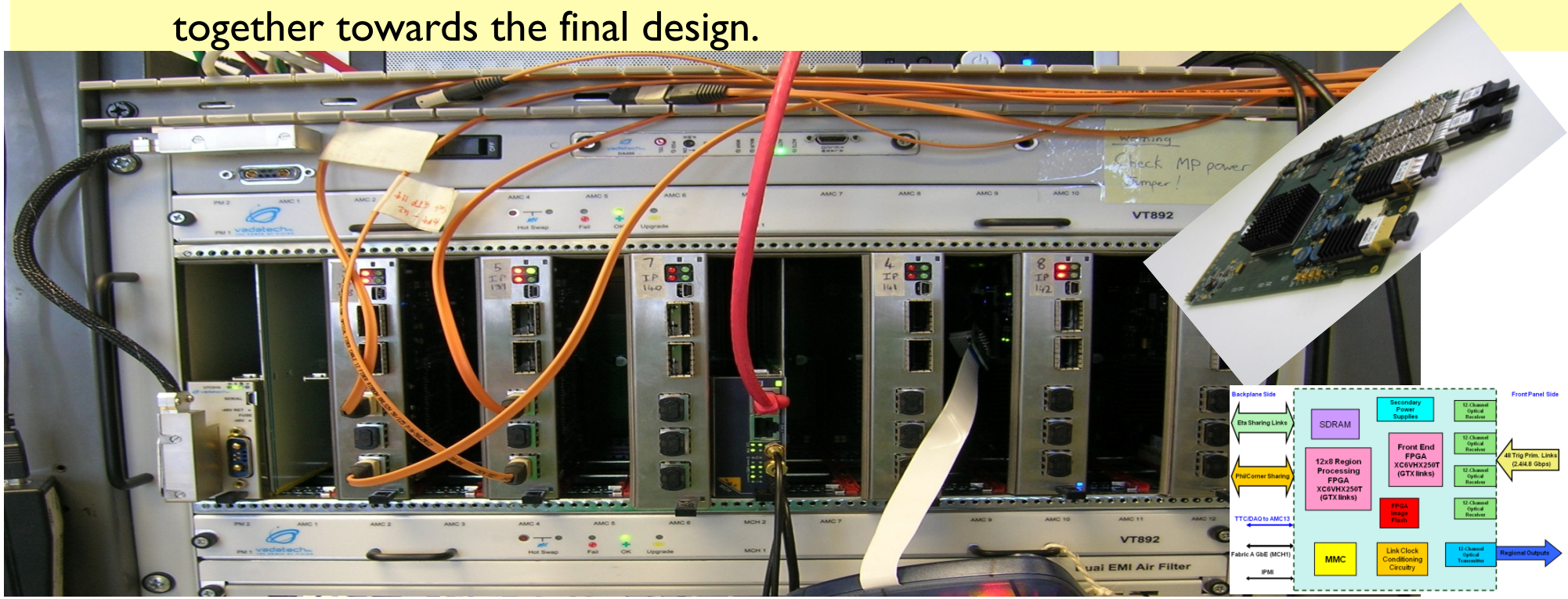
- Near term
  - firmware & software for digital DAQ test boards
  - contribute DAQ hardware & firmware in beam tests of new ROC in 2012
- Longer term - depending on resources - under discussion
  - DAQ for pilot blade test
  - contribute to modified FEDs with digital readout
- Proposal to strengthen overall DAQ activities with working group covering both SST and pixels
  - builds on existing strengths (Tracker FEDs, APVe, ReTri)
  - and staff with relevant expertise:
    - J Fulcher, M Pesaresi,… (Imperial - Tracker)
    - K Harder et al (RAL PPD)
    - with other potential interested parties (Bristol, RAL TD WP2)

CMS planning

- FNAL Upgrade workshop Nov 2011
  - Phase I progress and preparation of detailed scheduling
  - Phase II R&D, including detailed discussions of track-triggering
- Funding
  - provisional (ie subject to FA approvals) money matrix at next RRB
- Upgraded Calorimeter trigger
  - architecture decision is crucial to planning the PPRP bid
- Tracker planning
  - FED back-end upgrade almost certain & UK pixel role to be confirmed
    - best addressed by common DAQ team effort, which is now beginning
- Long term R&D remains very high priority
  - emphasis on track-trigger matches UK interests

Calorimeter Trigger Designs

- Several prototype uTCA trigger cards have been built and have been shown to work. Working demonstrators at the crate level exist also.
- Two calorimeter trigger architectures are under consideration.
- We have organised a review for the two Calorimeter Trigger architectures. The aim of the review is:
  1. to select the architecture which best serves CMS for the next decade.
  2. Produce a plan for the two relevant groups (Wisconsin-Imperial) to work together towards the final design.



Trigger Upgrades Schedule

- 2011:
  - Produce the first Prototypes of OptoSLB (Lisbon)
  - Design the first SP for the CSC trigger (Florida)
- 2012:
  - Working versions of OptoSLB and SP cards
  - Start Production and testing for both
  - Will need to procure a number of uTCA crates
  - Test CSC SP board
- 2013-2014 LS1.
  - Install OptoSLBs at P5 – ECAL ONLY
  - Install Trigger Fibers from both HCAL uTCA and ECAL OptoSLB at P5.
  - Install the trigger crates at P5.
  - Connect CSC SP and test using the fibers from the detector electronics
- Meeting this schedule enables us to produce and commission the new trigger electronics in parallel with data taking in the 3-4 year period after the start of the 14 TeV run in 2014.

UK upgrade planning

- Activities now clear and coherent
  - Trigger Phase I, Tracker Phase II, DAQ for pixel+SST
  - with long term vision for track-trigger based on all of above
- PPRP proposal
  - prepare Q1 2012 (in parallel with Rolling Grant)
  - submit end Q1, early Q2 (tbc)
  - should ensure funding **in institutions** by end Q1 2013 – (STFC to endorse)
- State of UK groups
  - Imperial – stretch funds to end of grant [A Rose-> Zorba (RG) appointment]
  - Bristol – key posts end soon – Frazier, Grimes
  - Brunel – WP1 staff funding now exhausted
  - RAL PPD – anomalous re funding and currently subject to uncertainty
    - i.e. RG posts but treated as project-like, so permanent staff funded on "new" funds, requiring PPRP approval
    - PPD review reported. Implementation tbd.

WP1: Future

- Current WP1 planning:
  - One post (I. Reid) has ended; two Bristol posts end in Q1-2012
    - Work at Brunel continues on best-effort basis using temporary funds
  - Capital and consumables funds remain
  - The financial situation with RAL posts is unclear
- Use of remaining funds
  - We have requested permission to move remaining funds to posts
  - This will give us between 3-6 months additional effort
- 2012 and beyond
  - We have important and highly visible responsibilities in upgrade software
    - Demonstrated by the take-up of UK deliverables across the CMS upgrade effort
  - We anticipate a new funding request (across all upgrade activities) in 2012
  - However, all WP1 posts are likely to end before new funds are in place
  - We wish to explore how this work can be maintained in the long term
    - As an essential part of a coherent future UK upgrade construction project

Bridging funding request

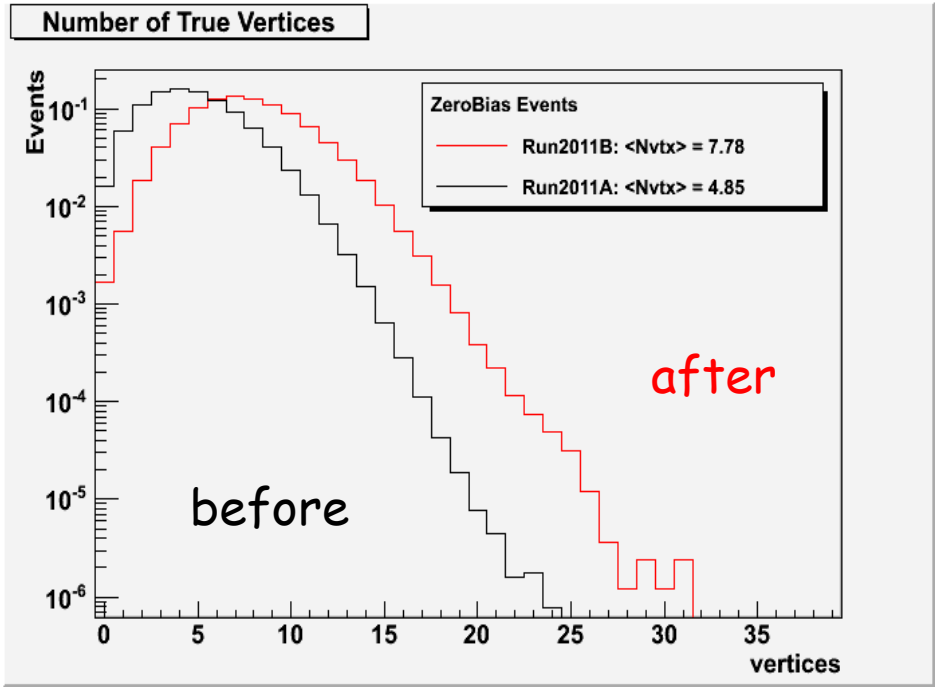
- Additional slides to be presented at the meeting

Summary

- Very good progress continues in all WPs
- CMS and LHC upgrade planning
  - schedule changed again, but clear picture beginning to emerge
- Finances
  - spending increased, larger commitments expected in 2012
    - Working Margin (£230k) reduced to £210k
  - Bridging to next period for construction and long term
    - discussion today
  - RAL PPD
    - crucial to understand resources available

Further information

Pile-Up



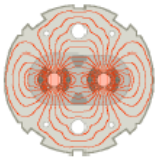
- The number of reconstructed vertices after the August Technical Stop increased by factor 1.5 (β^*=1.5m →1m)
  - Fills start with ~15 pile-up interactions
  - Vertex reconstruction still quite linear with luminosity
- Total inelastic cross section also has been measured from pile-up
  - **σ_{inel}(pp)= 68.0 ± 2.0 (Syst) ± 2.4 (Lum) ± 4 (Extrap.) mb.**

Averaged over fills.

$N_{rec} \sim 0.7 \times N_{pu}$

(PAS FWD-11-001)

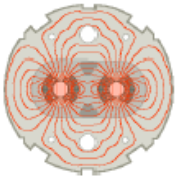
Luminosity Upgrade Scenario

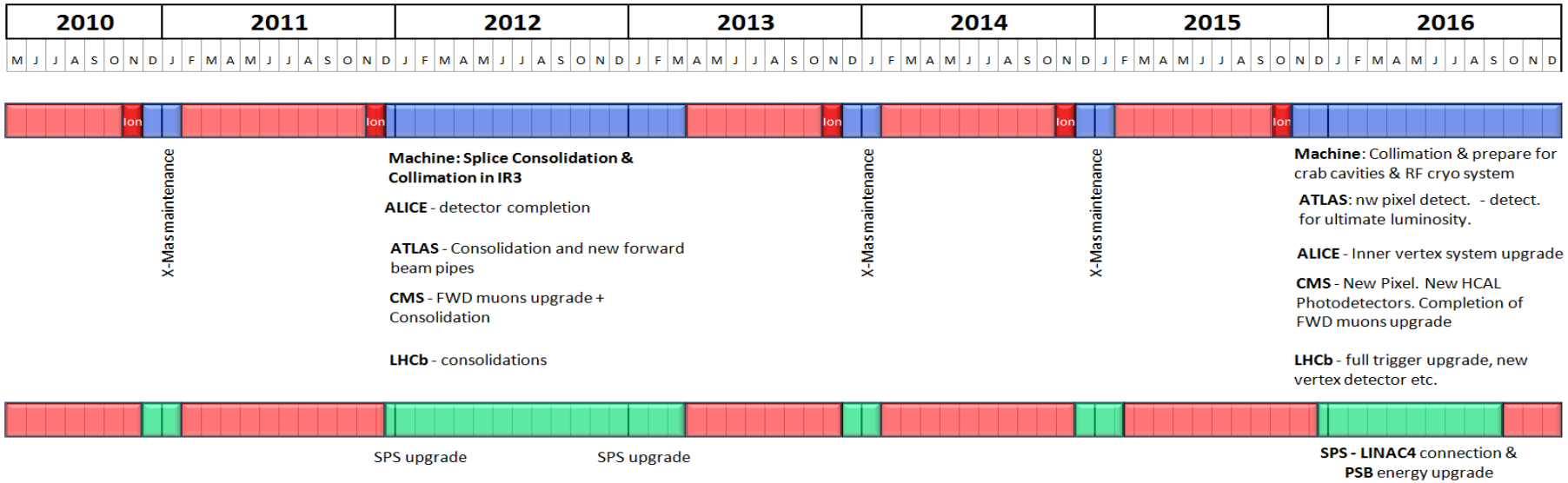


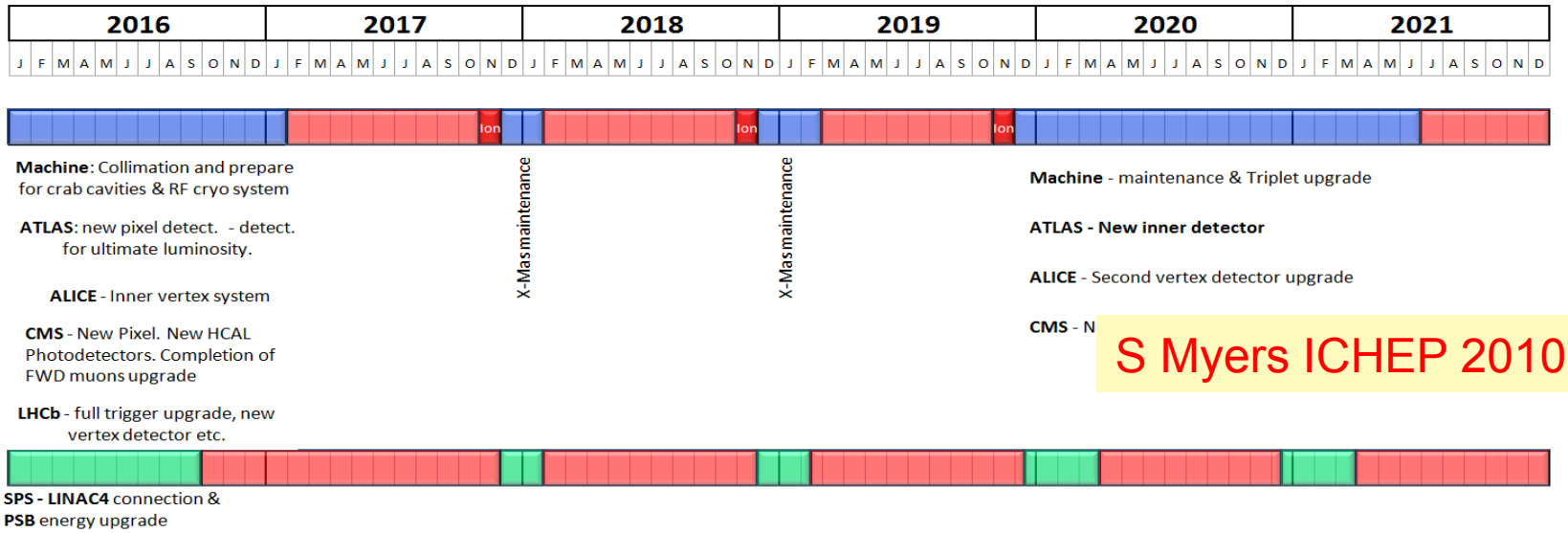
- For LHC high luminosities, the luminosity lifetime becomes comparable with the turn round time ⇒ Low efficiency
- Preliminary estimates show that the useful integrated luminosity is greater with
  - a peak luminosity of 5×10^{34} cm^{-2} s^{-1} and a longer luminosity lifetime (by luminosity levelling)
  - than with 10^{35} and a luminosity lifetime of a few hours
- Luminosity Levelling by
  - Beta*, crossing angle, crab cavities, and bunch length
  - ??? Off steering
- Goal 200-300fb^{-1} per year

July 2010

The 10 year technical Plan





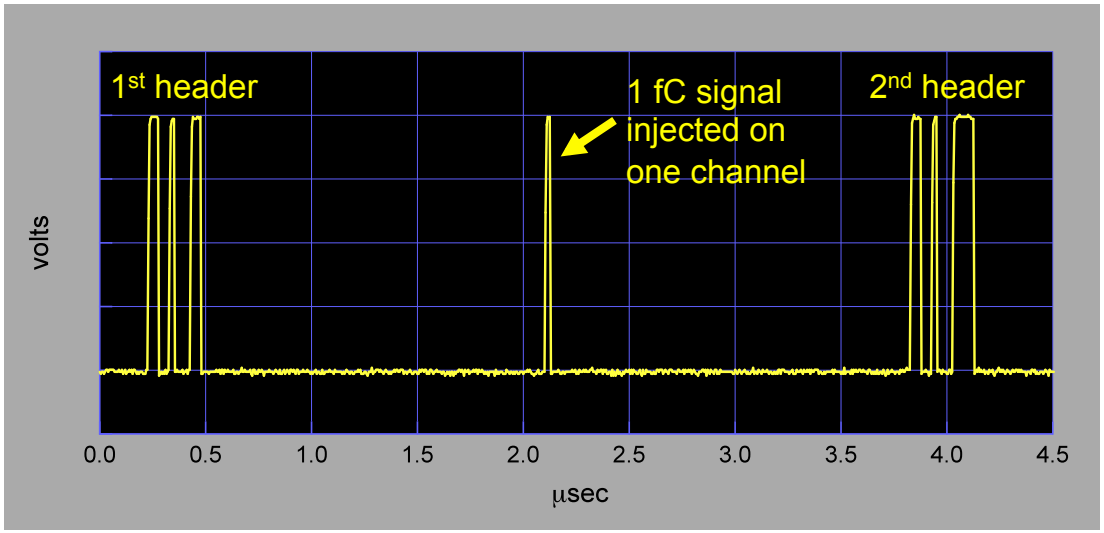


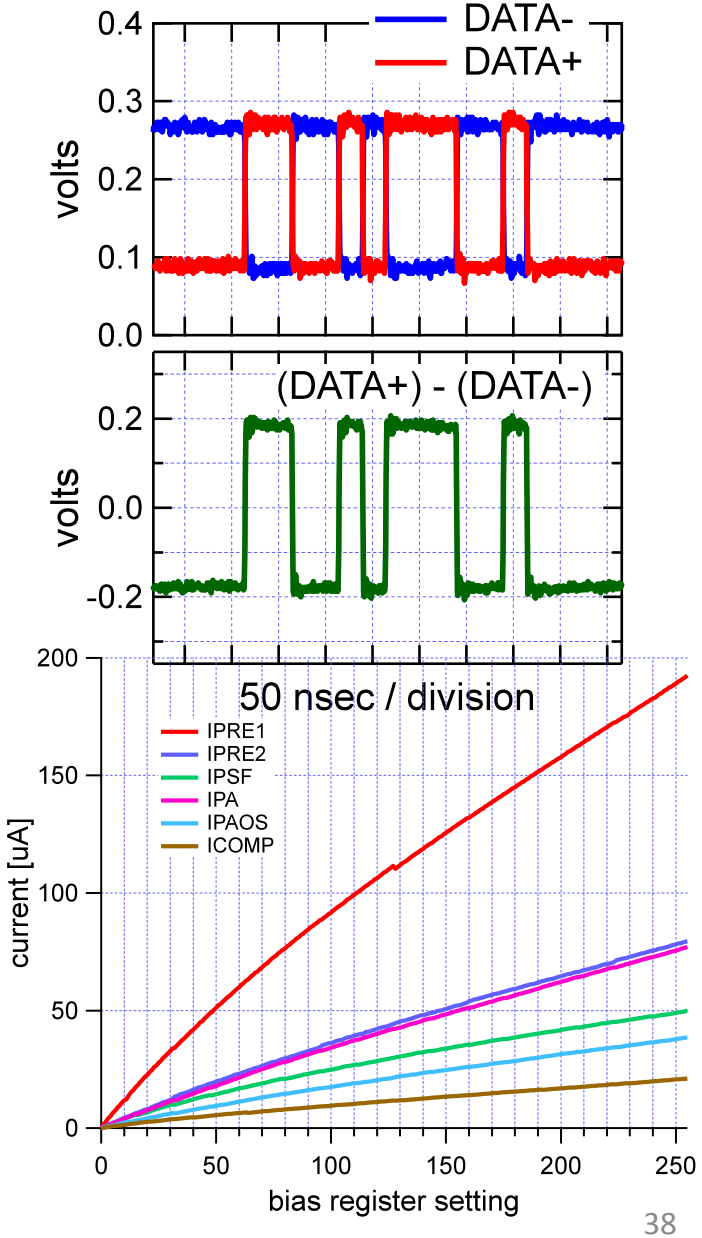
S Myers ICHEP 2010

CBC – basic functionality

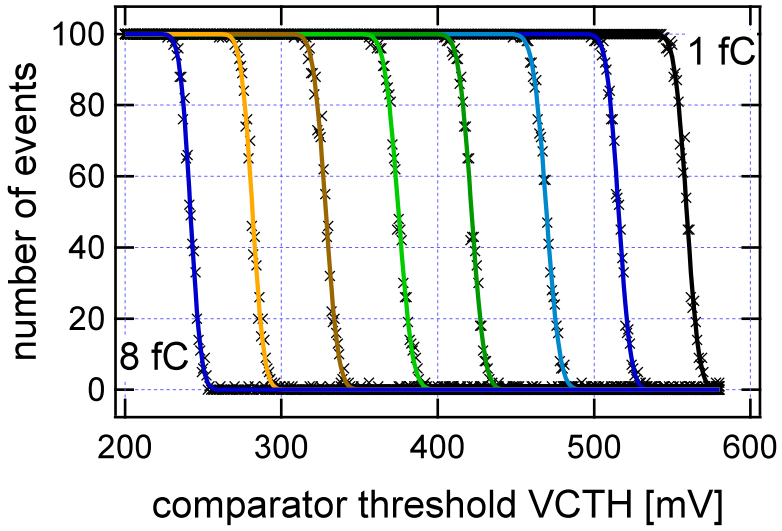
- SLVS Fast interface: Clock, Trigger, data
- I2C slow interface: program settings

- output data frame
  - 12 bit header
  - 2 error bits
  - 8 bit pipeline address
  - 128 channel binary data

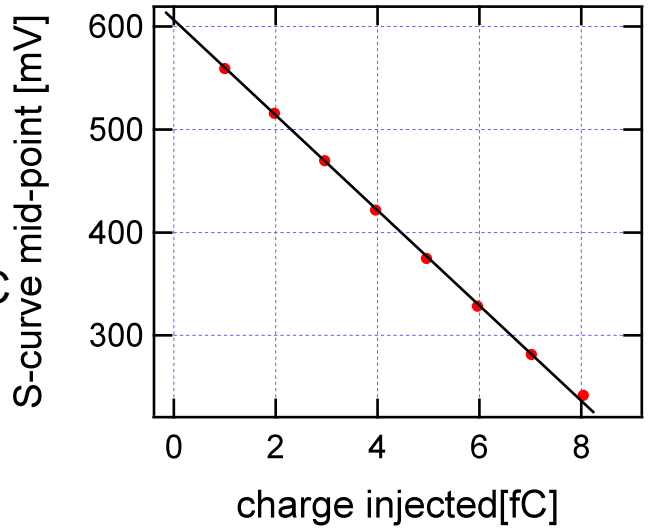


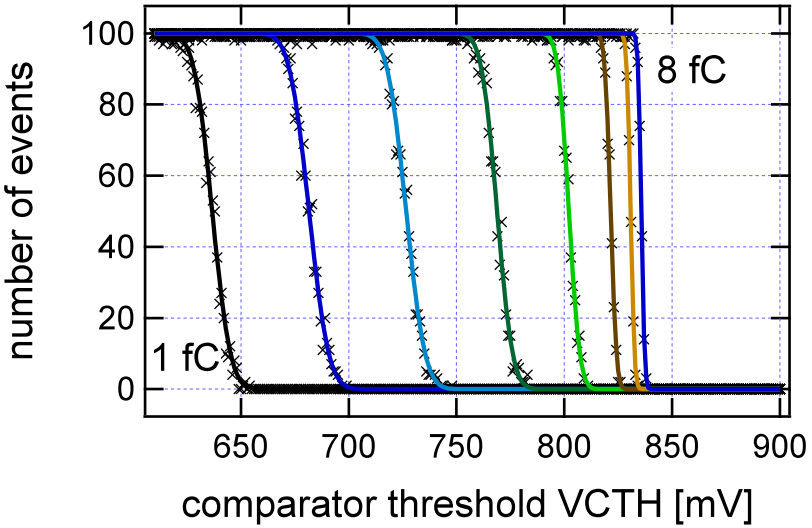


S-curves and gain



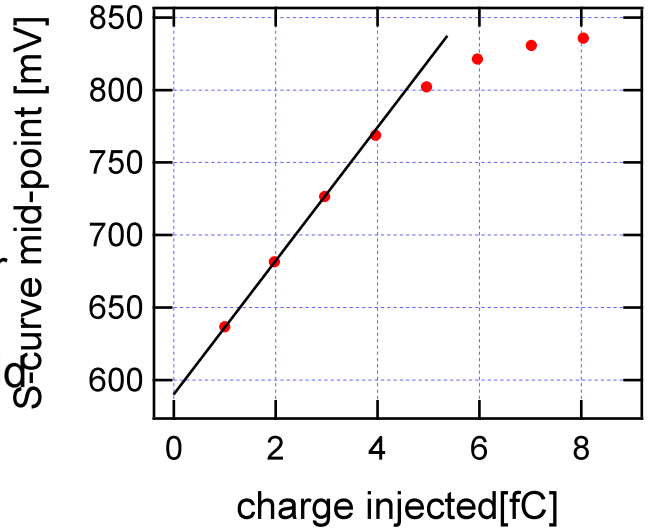
electrons mode
gain ~ 50 mV / fC
signals in range 1 - 8 fC
in 1 fC steps





holes mode
gain ~ similar

dynamic range more limited - but still linear in region where normal comp. threshold will be set



comparator - threshold uniformity & tuning

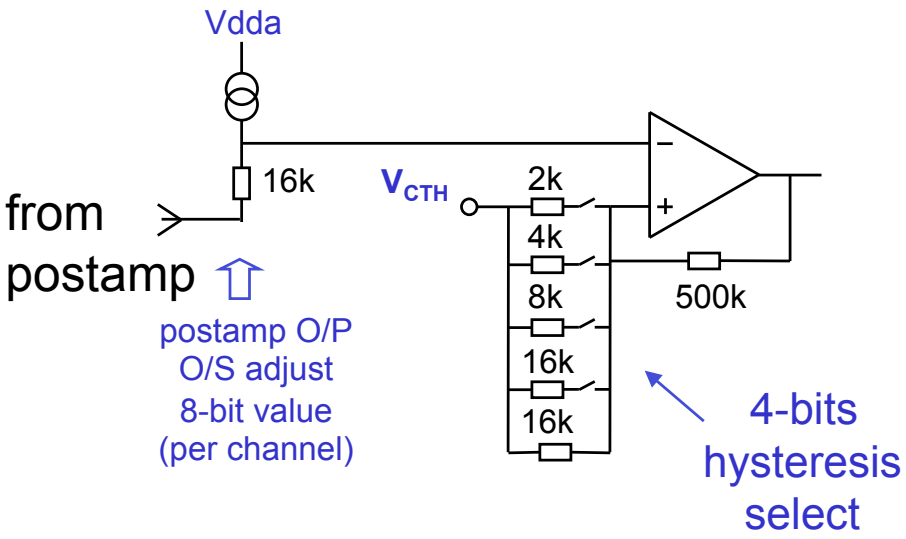
all channels have same global threshold

individual channel tuning achieved by introducing programmable offset at postamp output

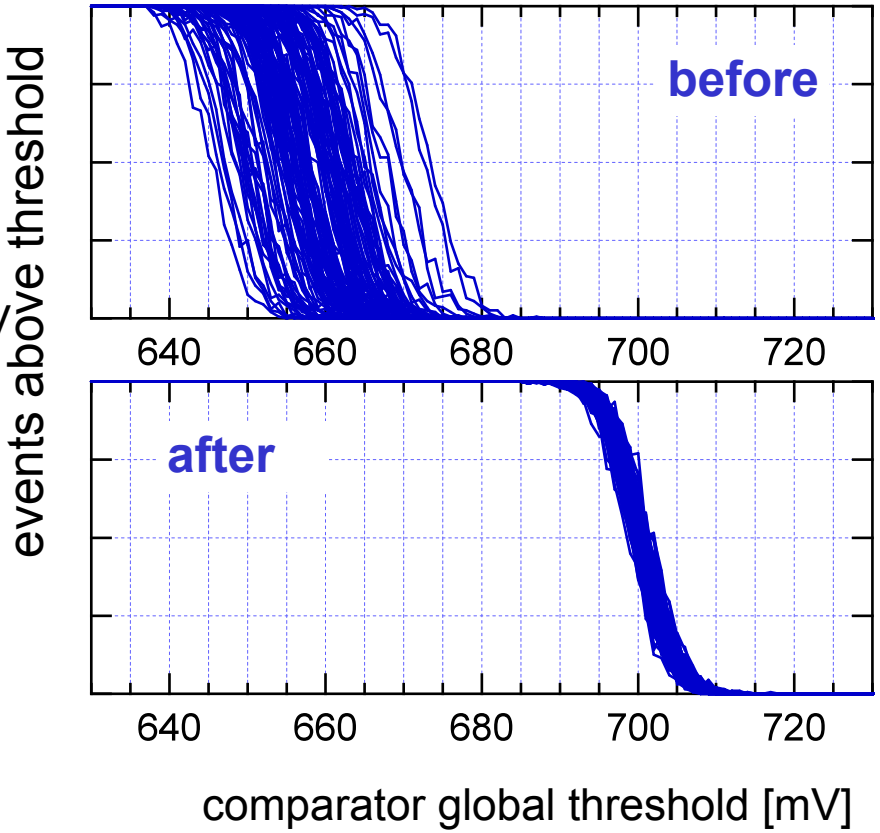
128 registers, 8-bit precision

before tuning pk-pk threshold spread ~30 mV (< 1 fC)

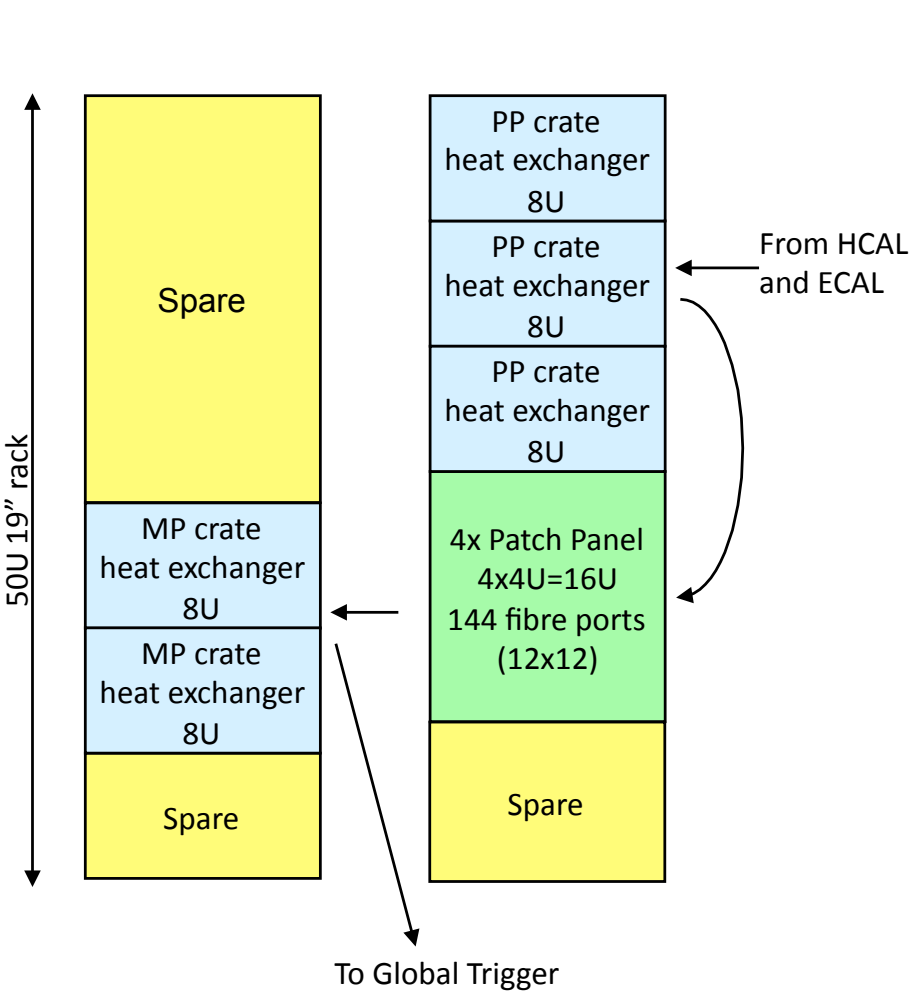
tuning reduces spread to ~ mV level

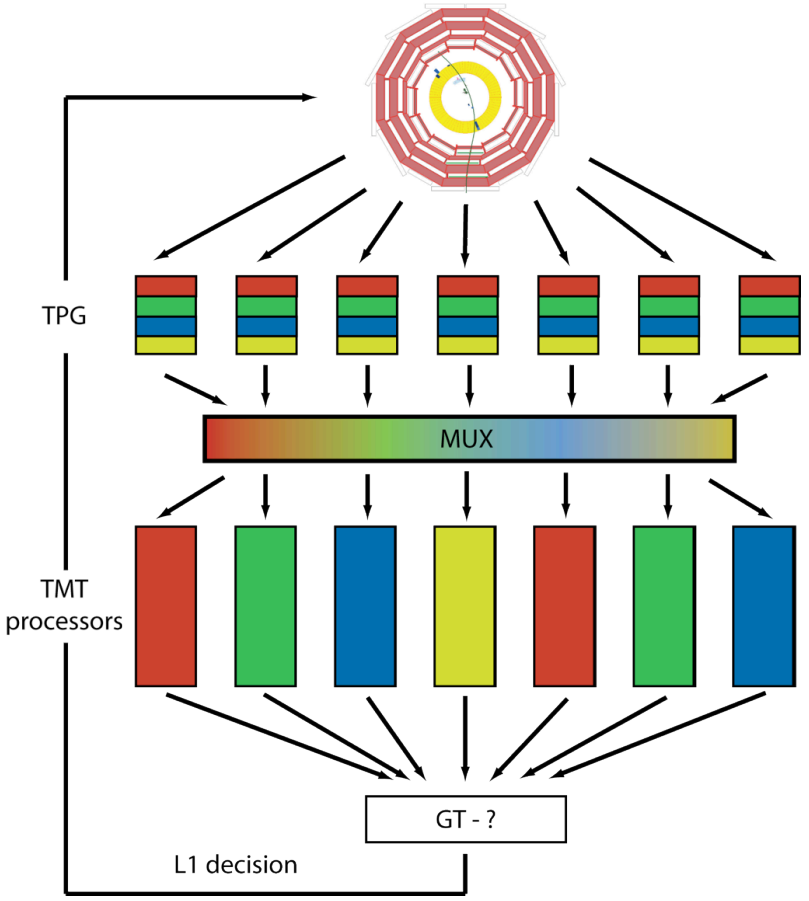


128 comparator channels threshold tuning



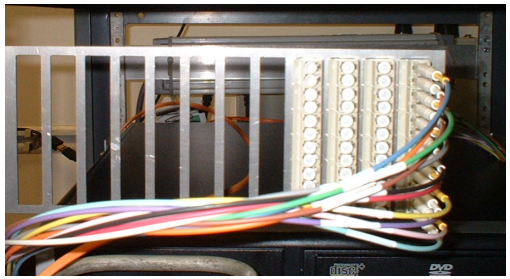
Final system



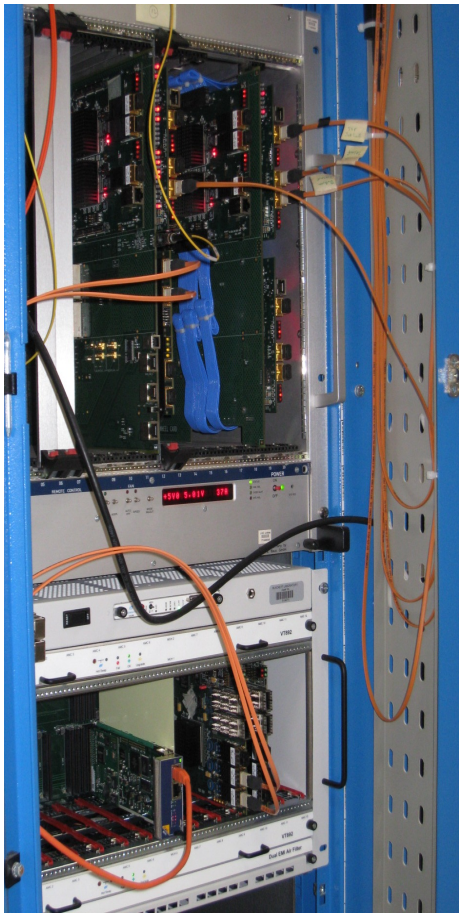


Assigning 16bits per tower: 36 Pre-Processor cards and 12 Main-Processor cards in 2 racks.

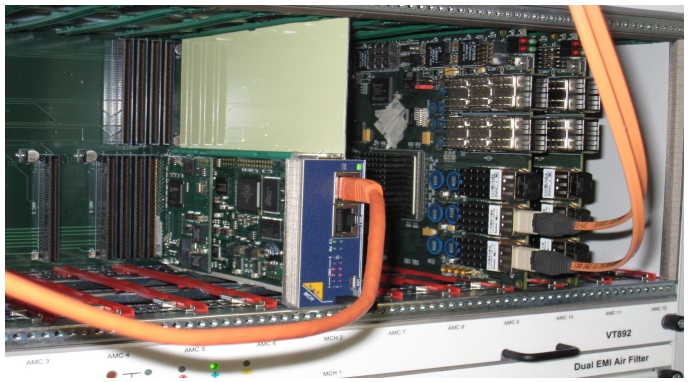
WP3 Extra pics



Considering practical aspects of final system e.g. custom ultra high density patch panels



Small demo system in CMS test & dev area (904, CERN) Allows inter-system testing

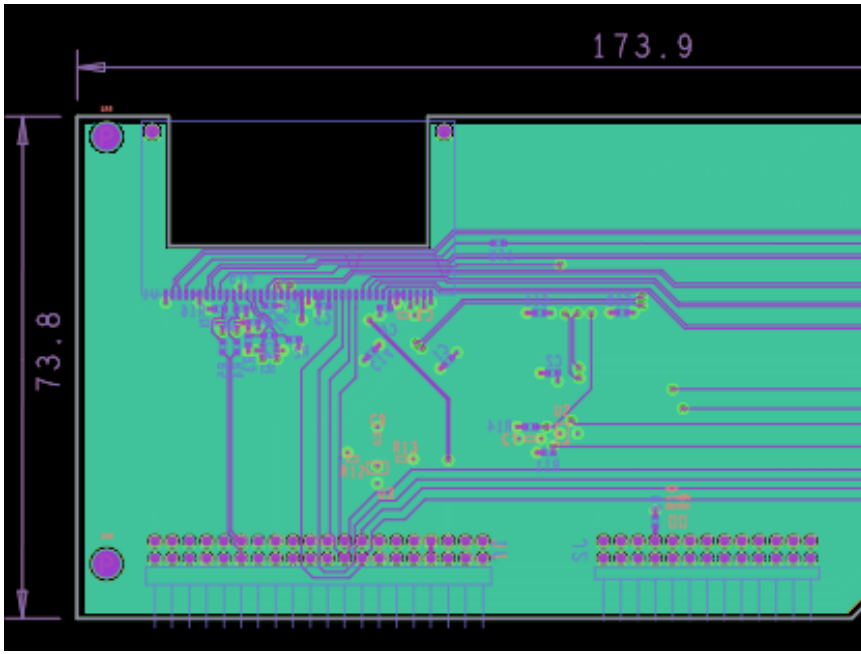


WP4: Pixel detector DAQ and test systems

RAL group is in charge of test DAQ systems for phase 1 pixel upgrade activities and will contribute to full pixel DAQ.

Current project: DAQ testboard upgrade for digital chips:

- Faster output (USB2) for DAQ testboard:
  Built two working prototypes.
  Now working on firmware to optimize throughput.
- Deserializing input adapter for digital chip:
  Three assembled PCBs expected at RAL today.
  Deserializer firmware works in simulation.
  Adapter also compatible with analog chip
  (for detailed testing before availability of digital chip).
- Digital chip/module emulator:
  Based on FPGA evaluation board.
  Several 100 example readouts in memory.
  Up to 400 Mbit/s output stream.
  Hardware and firmware ready for testing.



Expect to have a working readout system for digital chips in a few weeks.
Allows several months of testing before arrival of first chips.

WP4: Pixel work plan

Near-term programme:

- Develop firmware+software for digital DAQ testboards
  For UK and for PSI hardware
- Responsibility for DAQ hardware and firmware in
  first beam tests of the new digital readout chip (2012)

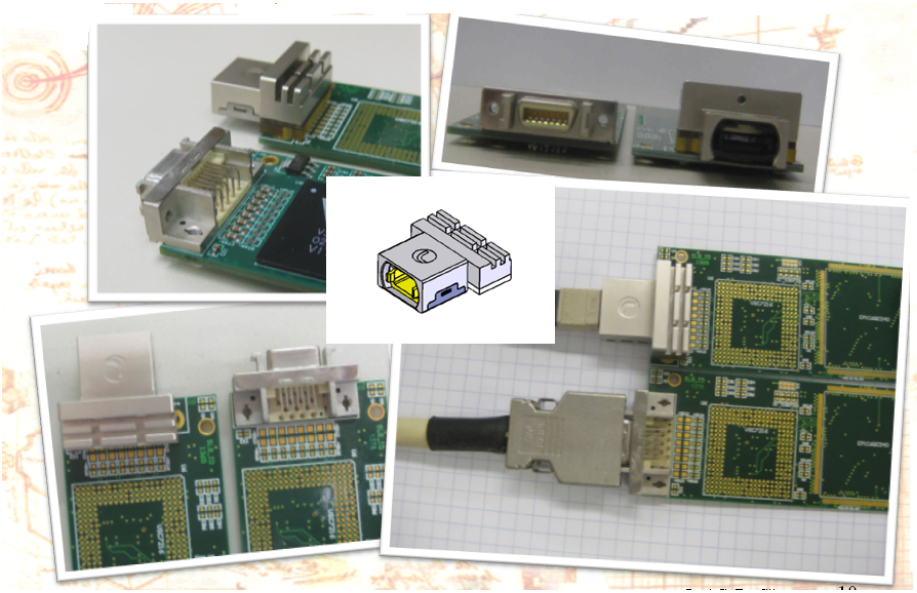
Longer term:

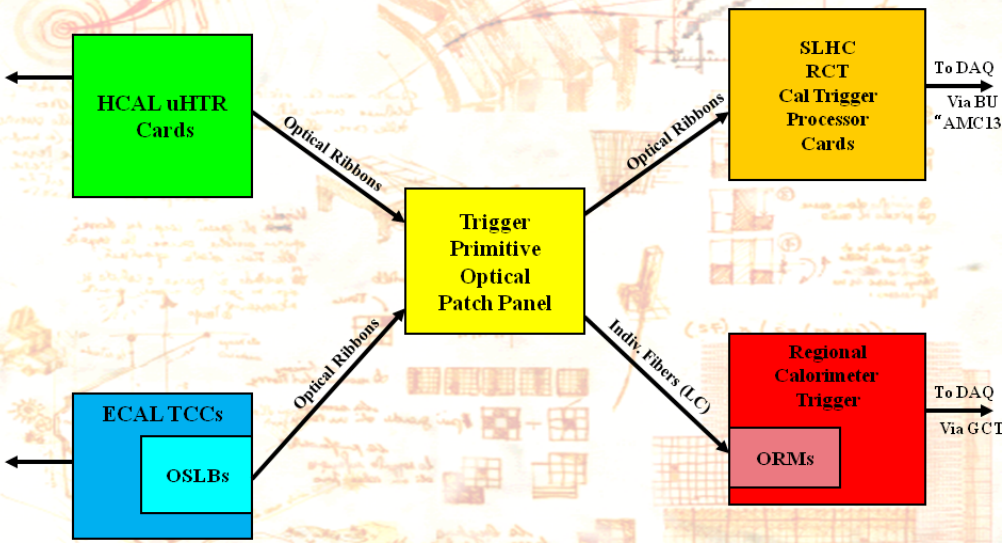
- providing DAQ for pixel pilot blades
  (needs prototype of digital FED)
- modification of pixel FEDs for digital readout
  (potentially a full redesign later on:
  - Combine FED and FEC?
  - Common (or similar) design for pixel and strip FEDs?

CMS is forming a working group looking to combine upgrade efforts for pixel and strip tracker DAQ. Some upgrades required very soon because limitations almost hit even with current beam conditions.

- K. Harder (RAL) represents pixel upgrade community
- UK planning to play a role in defining and building new readout system (hardware, firmware, software)

ECAL–Trigger Interface - OptoSLB





- Converts ECAL copper signals to 4.8 GBps optical and allows to keep using the current ECAL Trigger electronics after 2014.
- Bought 4 optical devices for evaluation.
- Design effort for the card has started.
- First prototypes have been promised late in 2011 early 2012.
- Production should start in 2012.