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R&D in preparation for upgrades of the CMS detector for High Luminosity LHC

1 Executive Summary

The proposal was approved in Spring 2008, and effectively began in April 2009. Notable progress since the last report includes:

The CMS Upgrade Technical Proposal has been reviewed and approved by the CERN LHCC.

Again there has been further evolution of the LHC schedule for the next decade, along with continuing very successful LHC operation. The most recent plan was presented in July and foresees the major Technical Stops and running periods to 2022.

There has been continued steady progress in developing software for upgrade simulations, especially for the Phase I tracking performance. In addition, the online software and firmware developments for the trigger upgrade have been especially noteworthy, allowing laboratory trigger prototype systems to be demonstrated.

The CBC (CMS Binary Chip) has been extensively tested in the laboratory with excellent results over the last six months. A CBC-sensor module has been constructed and operated successfully in a CERN test beam. Work has continued designing basic FPGA building blocks for the tracker readout system; a VHDL design has been developed on a Xilinx Virtex-6 FPGA development board for testing data.

Two major objectives have been achieved in the trigger developments in the last six months with the completion of a large demonstrator system operating in the laboratory, and an Ethernet communication package composed of both firmware cores and software. Discussions continue on the architecture to be selected by CMS for its upgrade trigger systems.

A new work package involving RAL PPD staff has been defined to support the pixel upgrade drawing on effort originally assigned to other activities; progress is reported for the first time.

Because of the different durations of the project work packages, assigned on approval, there is concern that posts of key individuals contributing to software developments will terminate soon. We will address this during the OSC meeting.

2. Project history and recent developments

The original proposal was submitted to STFC in October 2007 with an upgrade of the LHC peak luminosity from 10^{34} cm^{-2}s^{-1} to 10^{35} cm^{-2}s^{-1} about ten years after start-up in mind. The accelerator upgrade has since been proposed to take place in two main stages, with an increase in luminosity to 2 x 10^{34} cm^{-2}s^{-1} being Phase I, occurring in 2016 in the most recent CERN ten-year plan, and a further major increase in the next decade.

The LHC had a very successful year of operation in 2010, delivering 47 pb^{-1} of integrated luminosity to CMS. The formal targets for 2011 were set conservatively at 2 x 10^{32} cm^{-2}s^{-1} and 1 fb^{-1} integrated luminosity. 2.6 fb^{-1} had been delivered to CMS by the end of August and at the time of writing the machine is steadily converging on the latest goal of an instantaneous luminosity of 3.3 x 10^{33} cm^{-2}s^{-1} while the integrated luminosity could reach 5 fb^{-1} by the end of the year. The LHC parameters being targeted are 1380 bunches, β^* = 1m, 1.2 x10^{11} p/bunch and a crossing angle of 120 μrad, operating at 50 ns bunch spacing. The emittance has usually been around 2.3-2.5 μm. Only the β^* value exceeds what has already been achieved this year. This is expected to lead to ~15 pileup events per crossing early in each run.

With 5 fb^{-1} of data the Standard Model Higgs discovery, or exclusion, range should cover 114-600 GeV, combined with ATLAS. Another month of heavy ion running with Pb ions is also expected at the end of the year.

The UK CMS hardware continues to be generally very reliable. The trigger needs modest regular attention, some related to hardware issues. One or two cables from RCT to GCT fail annually (poorly manufactured, but not noticed at the time). There are enough spares and a special tester for validating new cables. Supposedly "high reliability" SFP optical transmitters fail at a rate of approximately 4-5 per year. This is far higher than specified but the parts can be hot-swapped easily.

Typically the software is regularly upgraded to improve fault diagnostics and reduce downtime. The current examples considered the most critical are masking part of the trigger (i.e. to operate the GCT in degraded mode while a fix is applied) and alarms to indicate a fault, such as an SFP failure.

The Tracker FED firmware is also regularly upgraded with minor amendments to stay abreast of other changes in the CMS system; mostly this has been related to CMS re-synchronisations. For example, the most recent firmware upgrade fixed a long-standing, occasional failure of VME readout during a re-synchronisation. Mostly these are caused by pixel requests, originating in beam gas events. About one failure per day occurred due to a clash between the monitoring VME transactions and the re-synchronisation operations within the FEDs. Now both VME and resynch commands can be issued simultaneously without problems.

2.1 LHC upgrade schedule and planning

The latest machine operation schedule was released in July 2011. The LHC will run for the whole of 2012, with the exact operational conditions, including beam energy, to be decided in January 2012 and cease operations at the end of the year, to replace the current-carrying splices, modify the collimation system and carry out other maintenance tasks. This will prepare the machine for operation at its full energy of 7 TeV per beam. The exact duration of the Long Shutdown (LS1) is not completely certain but may be as long as two years. It seems most likely that Linac 4 and the PSB will be connected during LS1.

The second major shutdown, LS2, is now foreseen to start at the end of 2017, following the annual heavy ion run. This would prepare the LHC for higher luminosity operation beyond the nominal 10^{34} $cm^{-2}s^{-1}$ starting in early 2019. Although 25ns operation is still the baseline, this cannot yet be fully proven, so there still remains the possibility that LHC operations would be at 50ns, with consequent adverse impact on the pileup. The machine would run for a further three years and shut at the end of 2021 (LS3) for the major upgrade to very high intensity with an objective of a *levelled* peak luminosity of 5×10^{34} $cm^{-2}s^{-1}$ aiming to deliver up to 3000 fb^{-1} in the following decade to 2030.

2.2 CMS planning

CMS is adapting its planning to the LS1 duration when the pixel tracker will be replaced and the trigger upgraded but does not have a fully detailed overall schedule. This will certainly be developed in the coming year; many of the upgrade activities, for example in the muon system, need careful scheduling yet are constrained by finances. Project plans are being developed for the later trigger and pixel tracker upgrades. The main clarification required which will affect UK activities is how and when the upgraded trigger will be installed and commissioned.

The two main issues we foresee affecting our future planning are the physics justification of the Phase I upgrades, particularly the trigger, and the trigger architecture to be adopted. These are actually correlated since a more flexible architecture, such as the Time Multiplexed concept proposed by us, is obviously well adapted to future trigger changes, yet the benefit should be set against the possible impact of changing the overall design and the likelihood of requests for new physics triggers.

To address this, the Trigger Project Manager in conjunction with the Trigger Upgrade Manager have set out the criteria by which the choice of calorimeter trigger architecture will be made, and are constituting a panel of CMS experts to advise on the choice. This is expected to take place over the next few months with a decision likely in the early part of 2012. After the final architecture is chosen the calorimeter trigger group will be invited to make a schedule and milestones for the new project.

The appointment of a new Spokesperson, who takes up his position in January 2012, includes new appointments to several major positions. The Trigger PM and Upgrade Manager will change; the new Trigger Upgrade Manager will be Alex Tapper from Imperial College. The Tracker PM will remain in post for at least another year, along with his team. The CMS Upgrade management team will change but should have a modest influence over details of sub-detector activities with the exception of experiment integration, since the main central management task should be concerned with global CMS issues and coordinating inter-related or competing activities, such as installation tasks.

2.3 UK adaptation to CMS planning

Broad-brush plans for most sub-detectors were summarized in the Technical Proposal. Trigger and Tracker Technical Design Reports are expected in the next 1-2 years but no definite dates have yet been agreed. However, the Tracker has a reasonably clear picture of its Phase I planning, and the trigger is making an effort to develop a master plan. It has been hampered by the fact that the requirements - driven by the machine expectations, such as 50/25ns and likely instantaneous luminosity as well as the physics objectives, which reflect the expectations of discoveries - are hard to pin down. For example, more physics channels are proposed for the trigger menus than initially expected during the construction phase of CMS and there are such questions as whether improved tau hardware triggers can be developed. Meanwhile, the trigger is certainly presently operating within the design specifications. So the challenge is to anticipate the future trigger requirements as well as the expected LHC operational conditions.

There is no change in the UK focus on Tracker and Trigger. However, over the period of this project there have been very significant changes in the LHC plans, the time foreseen to be available for R&D, the upgrade detector and trigger concepts, among other things. This is to be expected in an R&D project of this type and the challenge, which we believe has been met successfully, is either to adapt, or lead, the programme so that UK contributions remain relevant and, if possible, notable. However it does make the tracking of original milestones a rather moot point. The main areas for our possible future contributions remain:

Replacement of more advanced Tracker FED transition cards and associated S-links. CMS central DAQ will upgrade the S-links used between FEDs and the central switch (via FRLs). The transition cards themselves are a modest hardware project but with significant implications for the FED firmware and maintenance, and for our long term commitment to the Tracker DAQ which is crucial to CMS. This upgrade remains very likely and should be confirmed in the next few months; attention has focused primarily on the much more challenging pixel replacement.

For the Phase I Tracker, the UK has expressed interest in contributing to the pixel DAQ; the evolution of this work is under active discussion with the CMS pixel management. A pixel module assembly project now seems very unlikely. A new Work Package has been defined which deploys RAL PPD staff on a task associated with pixel module testing and might become part of the pixel DAQ project. The cost and detailed implications of a pixel DAQ activity in the UK have been evaluated for the period remaining on the grant.

Although Phase II, or the evolution of the LHC to high luminosity running, is still remote, the need to replace the entire Tracker means it is of the utmost importance to maintain the R&D progress and prototyping activities of WP2.

The Phase I Trigger upgrade should be based on μTCA hardware, where UK developments are very advanced and there is leading-edge expertise. There are both new ideas for implementation of the trigger and much more advanced hardware, and software and firmware developed to meet the requirements. We are collaborating closely with other trigger institutes to define the future calorimeter trigger which remains a hot issue in view of the alternative architectures and different levels of progress.

The date for a submission of a UK construction project proposal, including long term Phase II R&D, has been discussed, with an aim to be coherent with the rest of CMS. It now looks as though the target should be the end Q1 2012 or just after so that funding could be in place in early 2013, allowing continuity of key posts for the upgrade work, and requests for any others. To make this possible, we require CMS to have clarified its position on the trigger upgrade architecture and timing, and the actual tracker upgrade requirements.

We seek comment from the Oversight Committee to advise STFC on the possibility of bridging funds which are needed to sustain work under way in WP1 while the longer term plans for construction are better defined. The key point is to retain some critical staff posts; more details will be provided at the meeting.

3. Work Package 1: Tracker and Level-1 Trigger Simulations and Software

3.1 Objectives

The objective of WP1 is to support with software tools the design, optimisation and prototyping of replacement detector and electronic systems for the CMS tracker and L1 trigger. The project is now mainly focussed on the Phase-I upgrade; however, the tools and ideas for Phase-II which were developed in the early part of the project continue to be exploited as a background activity.

The top-level work package goals are as follows:

- Development of tools for simulation and optimisation of upgraded tracker and trigger systems in a very high luminosity environment
- Investigation and optimisation of tracking detector layout and inclusion of tracking data into the CMS trigger decision
- Provision of online and offline software tools and firmware to support the design and operation of upgraded electronics systems for Phase-I, including the construction and operation of hardware prototypes.
- Assessment of the performance of the upgraded CMS detector against key physics requirements and with realistic background conditions.

In the last report, we proposed a change of WP1 deliverables and redeployment of RAL PPD effort, to permit a provisional role in the CMS Phase-I pixels upgrade project. A proposal for this work was described in a separate document submitted over the summer. We report progress in that area in a separate section of this report, as a distinct work package.

3.2 Progress to date

WP1 has made substantial progress against deliverables in the last six months. We note that all aspects of the work have recently been presented at international workshops and conferences. A further target for the remainder of 2011 will be to document the work in peer-reviewed journal publications.

Simulation tools: The UK has provided leadership in refactoring the CMS tracking software for upgrade simulations, and recent work has focussed on two areas. Firstly, the code has been extensively profiled in order to understand the evolution of processing time and memory requirements with increasing levels of in-time and out-of-time background. Critical sections of the code have been rewritten, resulting in significant improvements. However, it remains clear that computing resources will be a substantial issue in the future simulation programme; for instance, the computer time required for simulation increases by more than a factor of ten when going from <n>=50 to <n>=100 background events. A far more substantial re-architecting of the CMS simulation framework is likely to be required even before the Phase-I upgrade, and this will rely heavily on UK expertise built up so far.

Secondly, the process of convergence between the upgrade simulation and reconstruction software, and the mainstream CMS codebase, has continued, with many benefits in both directions. In recognition of the UK contribution in this area, M. Grimes (Bristol) has recently been appointed code librarian and software release manager for the overall CMS upgrade.

Physics performance studies: CMS is currently beginning a series of more detailed physics performance studies, based upon the Phase-I detector designs described in the Upgrade Technical Proposal. This effort has proved technically challenging, due to the large space of potentially interesting physics models and detector configurations. Nevertheless, it is vital in order to correctly steer the optimisation of the upgraded detector. The UK has responsibility for production of large simulation samples, for provision of validation tools for comparison of reconstructed objects with Monte Carlo truth, and profiling of simulation and reconstruction performance. In addition, a number of students and RAs will undertake detailed studies of specific physics channels in the coming months.

A new effort on simulation of Level-1 trigger algorithms has started, with the goal of guiding the architecture choice of the Phase-I upgraded trigger (A. Rose and M. Pioppi, Imperial). This work has acquired additional urgency due to the observed shifts in trigger performance with increasing levels of pileup, and the possibility of a more substantial hardware replacement at the LS1 shutdown than originally foreseen. Current work is focussing on evaluation of new jet trigger algorithms with online pileup subtraction.

Trigger software: Under the leadership of R. Frazier (Bristol), a hardware demonstrator system of realistic scale has been constructed as a test-bed for the combined online control software / firmware project being pursued by WP1 and WP3 (see figure below). This system comprises six highly specified FPGA evaluation platforms, configured with internal Ethernet switching such that several crates of μTCA hardware may be emulated. Using this platform, all components of the new online control system were evaluated, and demonstrated to work at the required scale and with a negligibly low rate of errors. Improvements made as part of this test programme were included into a new public release of the system. The firmware and software have been adopted by an increasing number of projects inside and outside CMS, and form the baseline approach to system control for the CMS electronics upgrades. For instance, the system has been adopted by the HCAL readout upgrade, and for the CERN GLIB readout platform, both substantial and long-term projects which are central to the upgrade programme. There is interest from a wide range of other projects. Future developments will focus on improving performance, maintainability and hardware requirements of the code, with a new and experienced collaborator (D. Sankey, RAL) having joined this effort during the reporting period.

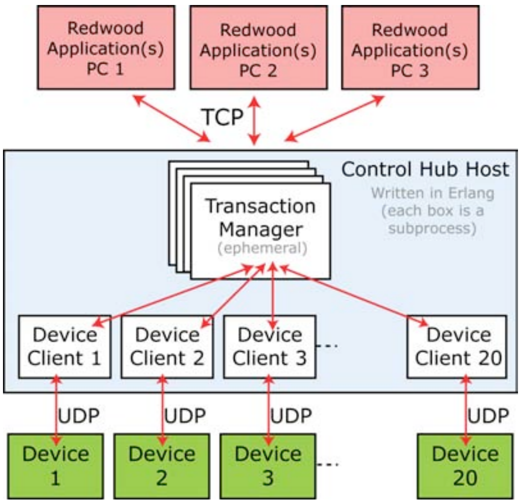

Fig 3.1 The Bristol test-bed for the software-firmware platform

3.3 Deliverables

The progress against the project milestones is summarised below. Depending on progress with the pixel module readout project, it will be appropriate to introduce a new milestone for Year 3 in this area. We note here that milestones indicated as 'Year 3' are in fact due for delivery before the end of WP1 funding at 1 January 2012.

Year 1:

The contribution to the stacked-tracking simulation programme has been successfully completed, and further work assigned a low priority.

The studies of overall tracker / trigger performance, and the identification of benchmark SLHC physics channels, have been subsumed into the overall CMS activity towards preparation of the Phase-I Upgrade Technical Proposal, with substantial UK leadership. This milestone was with the publication of the TP in late 2010. Detailed physics performance measurements are ongoing, with a next report to LHCC due in March 2011.

Year 2:

A CMS-wide release of the full simulation code for the upgraded tracker, and the emulation package for the upgraded L1 calorimeter trigger has been made, with significant UK contribution in each case.

Year 3:

An initial full-simulation performance study of a Phase-I upgraded detector was carried out using two physics benchmark channels which are representative of high-luminosity Higgs and SUSY searches respectively. These results were incorporated into the CMS Upgrade Technical Proposal.

More detailed and extensive physics studies are continuing, as are investigations of new trigger algorithms with the potential to improve performance of the Level-1 trigger in the medium term. These algorithms will be evaluated in simulation, and then demonstrated using the prototype trigger hardware developed in WP3.

3.4 Staff on project

Reported in tables. All WP1 staff posts are due to terminate under the currently allocated grants by March 2012. In the absence of any changes to funding, the subsequent report from WP1 will therefore be the final one. In the document submitted over the summer requesting changes to WP1 deliverables, a request was made for the virement of funds from consumables and capital budgets into staff support. This will allow the project to continue for some three months further, and full use of those funds to be made.

WP1 has been a successful venture for the UK, with all milestones met on time (some ahead of time). The resources available have been less than originally anticipated because of external circumstances which particularly affected RAL PPD recruitment. The work package was set up with challenging and concrete deliverables, each of which has been fulfilled. CMS has benefitted from new software and firmware systems, improvements to both upgrade and baseline software, leading contributions to public documents, and substantial contributions to the coordination and leadership of the upgrade programme in the areas of software, physics and triggering.

Within the UK project there has been an extremely fruitful collaboration with WP3 on the firmware and software framework which has expedited the production of a working prototype trigger system and, we believe, has laid substantial foundations for the management of trigger firmware and software independent of the chosen hardware architecture. It is important that we do not lose expertise in this area because of historical anomalies in the duration of different WPs.

We therefore propose to seek new funding for the continuation and expansion of our activities in each of these areas, and welcome input and discussion on the correct route for this request.

3.5 Expenditure

The expenditure to date is reported in the financial tables; WP1 is dominated by staff costs, with some travel. Expenditure required in the integration of WP1 online software with prototype trigger and readout hardware in WP3 and WP2 is generally covered in the budget of those WPs.

4. Work Package 2: Outer Tracker Readout

4.1 Objectives

The objectives of WP2 are to develop a readout chip suitable for the outer tracker, to study options for providing Level 1 trigger data from a new Tracker, and to contribute to development of a complete readout system, including off-detector components for the front-end DAQ.

4.2 Progress to date

Front end chip

The CBC readout chip (CMS Binary Chip) development is for short silicon microstrips (2-5 cm) to be used in the outer tracker region (r > ~50 cm). The 130nm CMOS CBC was designed in collaboration by RAL TD and Imperial College. At the time of the last OSC report (March 2011) the CBC return from manufacture was imminent so no results could be reported, but it was possible to show preliminary indications of functionality in the subsequent OSC presentation.

The main features of the CBC are:

- a fast front end amplifier, with 20ns peaking time,
- ability to match both sensor polarities
- ability to tolerate leakage currents up to 1 μA
- comparator with programmable threshold,
- 256 deep pipeline,
- 32 deep buffer for triggered events,
- unsparsified binary readout for chip and system simplicity
- output MUX and driver, using a low power signalling standard (SLVS),
- fast (SLVS) and slow (I2C) control interfaces.
- on-chip DC-DC switched capacitor power block
- low dropout regulator to supply analogue stages
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Since the delivery of the chips in March a substantial test effort has been under way. Aspects of the chip performance that have been verified in some detail so far are:

- digital functionality: fast (SLVS) and slow (I2C) interfaces are fully operational
- front end analogue functionality: pulse shape, noise, linearity dependencies on input capacitance are all close to simulated expectation, for both polarities of input signal. Up to 1 μA leakage current tolerance for both polarities has also been verified.
- comparator functionality: time walk is close to expectation. Individual channel threshold tuning works well, and good subsequent uniformity is achievable.
- power consumption: 0.3 mW/channel has been measured for a mid-range input sensor capacitance of 5 pF, which compares very favourably with the 0.5 mW target.
- powering features: The on-chip low dropout regulator is performing well.

Overall the results so far are very encouraging. A few design problems have been identified, but nothing to compromise the testing programme, and relatively simple workarounds have been found. The results from the testing to date have been presented at the ACES workshop[1] (March 2011), the CMS Upgrade week[2] (May 2011) and the CMS Tracker week[3] (May 2011).

We are currently preparing a test beam study (Sept. 2011) of a simple single CBC + sensor module, which has (at the time of writing) been inserted into the beam telescope described in the last OSC report and is producing useful data.

[1] http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/ACES_CBC_status_Mar_2011.pdf
[2] http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_CMS_Upgrade_May_11.pdf
[3] http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_Tracker_Electronics_May_11.pdf

Some aspects of CBC performance that need further study are:

- temperature dependence: Bristol have prepared a test setup to facilitate investigation of performance at the low operational temperatures expected at SLHC.
- tests with sensors: Apart from the imminent test beam, further studies will be conducted using a pulsed laser setup (Bristol)
- radiation: Ionising and SEU sensitivity studies are required but not yet scheduled.
- on-chip switched capacitor DC-DC conversion. This circuit has been verified to be functioning, but detailed chip performance studies are required.

Work is continuing on the development of the next phase of CBC ASIC design to incorporate improved test features, C4 bump bond compatibility, cluster width discrimination, coincidence finding and improvements identified through testing of the first prototype. Although the C4 bonding is known to be robust and inexpensive, it has not been much used in the HEP world and many questions concerning, e.g., testing and handling.

RAL TD have investigated the architecture for an asynchronous shift register for use with the fast readout of coincidences, including full parasitic level simulations for realistic timing. They have simulated coincidence logic and designed a test input circuit using a 25 element Delay Locked Loop for timing. They have also been actively producing floor plan options for the bump bonding and module layout, working closely with CERN to establish and optimum layout. This has meant producing several preliminary layouts and investigating cross talk issues. More recently they started modifying the comparator circuit to improve performance.

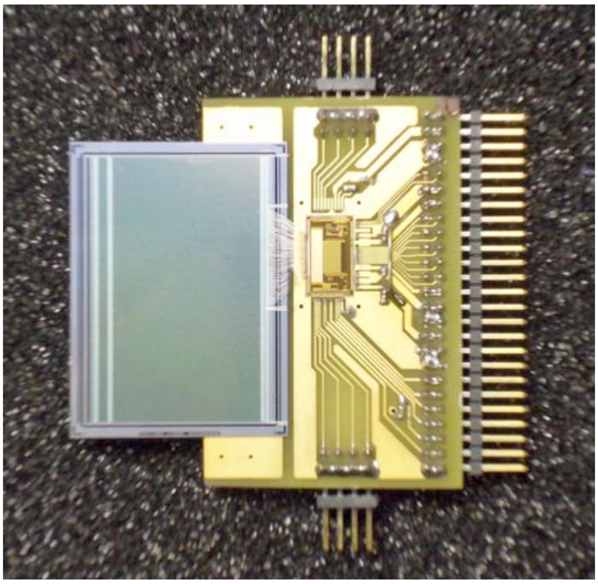

Fig 4.1 The CBC-sensor module used in the September beam test.

A weekly telephone meeting is held to communicate regularly between RAL and Imperial and both groups participate in dedicated Tracker Upgrade meetings, which are held mostly in CERN.

Further to the work on developing the ASIC, RAL have been involved in discussions regarding the readout schemes for the trigger information and analysing the various proposals. This has involved looking at the merits of both a synchronous and asynchronous readout scheme from the perspective of power, speed and data loss. An improved input test signal circuit was also designed.

In the next six months we will hold design reviews prior to the next submission, which is expected to be a C4 bump bondable version of the CBC with a target submission date of February 2012; this has been added as a new milestone.

The milestone status is summarised in the deliverables section below. Milestone 2.2.5 (review options for further CBC development) was deferred to 9/11 because of delays in the delivery of the CBC. We continue to discuss options for further CBC developments to address the requirements of L1 triggering and module assembly. The most promising approach to the triggering problem in the outer tracker is a double microstrip layer module where correlations between signals from particles traversing both layers can be brought together in one chip where a PT cut can be made. The on-chip logic required to make the trigger decision is straightforward and compatible with the existing CBC design. Issues of assembling trigger information and subsequent off-detector transmission are under study. We have also begun to actively study the issues of designing a 256 channel bump-bondable version of the CBC, and are collaborating with CERN groups to identify a suitable module substrate for the double layer module.

Milestones M2.3.2, M2.3.2 and M2.3.3 are all due 03/12 and relate to results from the present CBC prototype, and since this is working well we can be optimistic about meeting them.

We currently expect to submit the next chip prototype early in 2012, in line with milestone M2.3.4 (03/12).

4.3 Deliverables

For the front end chip component of WP2, a summary of the milestone status is:

Year 1

M2.1.1 (09/09): Documented system conceptual design and performance specifications; although the outer tracker readout system is not specified in final detail, it has been agreed to use the GBT link system which is documented in detail by CERN. The specifications for the CBC have been agreed with collaborators and are available by URL.

M2.1.2 (03/10): The requirement for front end and other test structure circuits has been removed since a decision was taken to go for a full chip submission on the first iteration.

M2.1.3 (03/10): Documented results of preliminary investigations of powering schemes have been reported.

Year 2

M2.2.1 (end Y2): Documented results of test structure evaluations. This milestone was cancelled because of the decision to submit a full chip prototype.

M2.2.2 (03/11): Full chip prototype submitted for fabrication and test setups prepared. This milestone has been met.

M2.2.3 (03/11): Final report on powering scheme tests. This milestone was retired since CMS has selected DC-DC conversion as the baseline choice for SLHC tracker powering.

M2.2.5 (09/11): Review options for further CBC development. This milestone was deferred from 03/11 because of the late delivery of the CBC. Options for future chip submissions are still under discussion, and design concepts for triggering and bump-bonded versions of the chip have been developed and are being discussed with CMS collaborators.

Year 3

M2.3.1 (03/12): Review results from prototype tests to ensure adequate functionality.
M2.3.2 (03/12): Documented preliminary chip results.
M2.3.3 (03/12): Documented results of prototype chip evaluation & prototype module and system tests.
M2.3.4 (03/12 – under review): Final pre-production chip designed & submitted for fabrication and test setups prepared.
M2.3.5 (03/12): Prototype system design.

Year 4

M2.4.1 (09/12): Documented results of final prototype.

SFED developments

Work is continuing designing basic FPGA building blocks for the tracker fast data readout system. A VHDL design has been developed on a Xilinx Virtex 6 FPGA development board for testing data buffering to external DDR3 memory modules. The aim is to provide a fast FIFO buffer interface for multiple GBT data streams in and out of external memory before output to the central DAQ.

Benchmark rate performances for various data transfer block sizes and clock rates have been measured and a report written. The interface now operates with 2 FIFO data channels with each channel in principle able to handle the data bandwidth from up to 4 GBTs. Systems with 4 FIFO channels are now being developed.

We have also integrated CMS IPbus standard firmware into this design. This allows access to the control registers and to data monitoring using the Gigabit Ethernet link on the Xilinx development board. Python scripts have been developed based on examples provided by Bristol to provide the software interface from the PC. The goal of developing FPGA code for external memory interface and integration with CMS control firmware was met.

Adding the IPbus makes the design compatible with development systems used on the Mini-T board. We are expecting to obtain a Mini-T board from the next production run to use as a test platform. We had also planned to test using the CERN GLIB μTCA development system, but these will not now be available until next year.

A short feasibility study for the proposed WP4 pixel readout mezzanine card was also carried out.

L1 trigger system

CMS remains committed to using Tracker data in the level 1 trigger at highluminosity and ideas are still under discussion. Strips of ~5 cm length installed in modules assembled as two layers could provide a means of transverse momentum selection, similar to long-pixel modules, but in a technically safer, lower cost and easier to implement manner. We continue to discuss this in regular meetings. At present the emphasis is on the "short-strip PT module" using the next version of the CBC.

4.4 Staff on project

Listed in the tables. Despite the departure of Chris Hill, Bristol have continued to contribute to the CBC testing, particularly at the module level and in the recent beam test. There has been a replacement of O. Zorba (Imperial College engineer); see WP3 report.

4.5 Expenditure

Most spending since the last ASIC submission concerned preparations for CBC testing in the lab and in the H8 test beam. The next major item is expected to be the next ASIC submission and it is not yet certain if this will be an MPW run, or if it will be necessary to take a large share of an engineering run.

4.6 Comparisons with CMS activities elsewhere

As explained in previous reports, the effort on both Tracker ASICs and FEDs is limited to a few institutions. The most active are RAL-Imperial and CERN. Lyon have recently been contributing a few engineers to ASIC developments; at present they are in an early phase and their contribution is still under discussion. Similarly, the FED work is expected to remain the responsibility of institutes who constructed the previous system.

5. Work Package 3: Design of Level-1 Calorimeter Triggers at the SLHC

5.1 Objectives

Work Package 3 is developing a demonstrator for upgraded Level-1 Trigger electronics and studying new trigger algorithms using this system. The main goal is to provide a standard device for all calorimeter Level-1 triggers which can be adopted during the Phase I upgrade in the first instance.

The platform now widely adopted in CMS without controversy is the µTCA standard which is used by the telecom industry and whose data transfer capabilities are in the multi-Gbps range. Our system consists of generic modular devices based on FPGAs and optical links and is the first prototype of off-detector trigger electronics for SLHC.

5.2 Progress to date

The last 6 months has seen the completion of two major objectives: a large demonstrator system for development work (M3.2.2) and an Ethernet communication package composed of both firmware cores and software (M3.3.5).

At the beginning of the year the MINI-T5 card was upgraded (version R2) to include dual QDR II SRAMs and, after a validation period (i.e. QDRIIs operating at 500Mb/s per pin), a batch of 12 has been produced. They were assembled in 3 sub-batches to mitigate risk. The bulk of these cards now make up the core demonstrator/development system at Imperial College. The remaining cards are used for development at University of Bristol, CERN and soon RAL.

µTCA crates, with modifications for vertical airflow (i.e. for CMS rack compatibility) and organised by the UK, have arrived. These crates have also been adopted by numerous other groups (multiple groups at CERN, US and Vienna). The crates are undergoing extensive performance tests at CERN, and initial results are good. The airflow is substantially better than an initial development crate and the decision to opt for 12 full size slots is being vindicated (i.e. maximum number of slots and extra height for components and cooling).

A prototype AMC13 card, developed by Eric Hazen at Boston University, to supply core CMS services to the crate (e.g. clock, control, feedback and DAQ capability) is under test. It is the last key hardware infrastructure component needed for the full system. We should receive a card within the next few months. In the meantime the clock has been distributed via the primary MCH and the control/feedback network has been implemented with external cables. DAQ is currently being routed via Ethernet, although a front panel optical interface would also be possible.

In parallel to the hardware & firmware development there has been substantial progress on MicroHAL - the robust, high performance and scalable Ethernet Hardware Access Layer (HAL). The first full package release (v1.3 beta) will be released in the coming weeks. It consists of both a firmware core; IpBus (prototype supplied by Jeremy Mans, Minnesota, but now substantially modified for performance & robustness) and several distinct software packages; ControlHub (packet routing hub built on Erlang, telecommunication language), Redwood (high performance, full featured C++ client side interface) and PyChips (simple, yet high performance, python client side interface for test/debug). Parts of this package are already being used by multiple CERN & US groupsThis package has required substantial resources, but the effort has been worthwhile as it is a key component of the system. We had expected the DAQ group at CERN to take the lead in developing an Ethernet HAL, as they did with the VME HAL, but this did not materialise.

The UK staff working in WP1 and WP3 have made major contributions to this effort, which is vital to the success of WP3 and, we expect, the future trigger:

microHAL (A. Rose) is a C++ library which is designed to distance the user from network protocols, packing of data, etc. and maximize code reusability. The software also allows the user identical control over hardware connected to a remote PC as to hardware physically connected to the PC.

The Control-Hub Host (R. Frazier) acts as the crate-controller for a µTCA system. The Control-Hub Host is physically a PC with two gigabit Ethernet interfaces; one of which is connected to a general purpose network and the other connected to the µTCA crate, via the MCH card. In this way the custom hardware is isolated from the "outside-world". The Host also performs the necessary arbitration between simultaneous attempts to access any hardware by multiple users. The software for the Control-Hub Host is written in the specialist, parallel-processing telecom's programming language, ERLANG.

Responsibility for the IPbus firmware (D. Newbold) has been acquired from the U.S. collaboration and large amounts of the original implementation rewritten to improve reliability and throughput. An upgraded bus specification has been developed (which is planned to be implemented at the end September, after the conference season) which offers even better performance and offers robustness which is not possible in the existing specification.

All three components are routinely used together in laboratory setups in Bristol, Imperial and CERN. R. Frazier has developed a validation framework, to ensure correct functioning whenever any component is changed, and is developing a release procedure so that compatible components may be tagged and released to the community as a package.

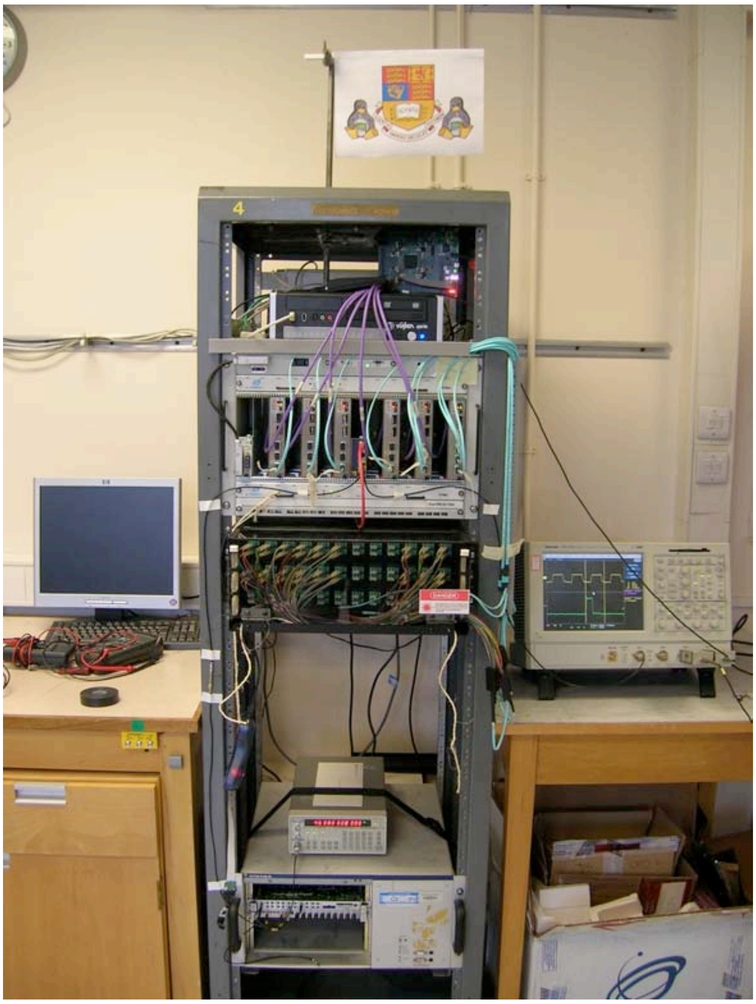

Fig. 5.1. MINI-T5-R2 cards, designed at Imperial College and manufactured by eXception PCB Ltd (Tewkesbury, UK) and Cemgraft (Newbury, UK) undergoing system tests at Imperial College.

The upcoming challenge over the next year will be to adapt to whatever trigger architecture CMS pursues; the TMT architecture and the extra processing capability it provides or the CT architecture with its reduced technical requirement. This choice is driven by a complex mesh of physics requirements, machine schedules, machine expectations, cost, etc.

The intention is to create a multi-purpose card that would be the Global Calorimeter Trigger card in the CT architecture and the Main Processor card in the TMT architecture. A baseline design has already been selected and layout should commence shortly so that we may have a final card in the middle of next year.

5.3 Deliverables

Of the proposed milestones, the following have been met or effectively retired, as summarised above.

Year 1:

Design of the main processing card ready for production.

Backplane design ready for layout. (no longer relevant)

Preliminary version of the firmware ready.

Year 2:

Working prototypes of processing card and backplane ready.

Core firmware infrastructure implemented (Ethernet, link control, pattern rams and DAQ) and tested with electron/tau time multiplexed trigger algorithm.

Control software infrastructure developed.

Alternative trigger architecture note distributed (Time-Multiplexed Trigger).

Year 3:

First μTCA demonstrator system ready. Working prototypes of processing card and backplane ready

Client side software

5.4 Staff on project

Reported in accompanying tables. Since the departure of the WP manager, C. Foudas, in August 2010, the PI has taken responsibility for overall supervision of WP3 activities. Recently, he has been supplemented by Dr Alex Tapper part time but from the beginning of 2012 Tapper will be dedicating much of his time to the trigger upgrade, as Trigger PM, and will take over the responsibility for WP3.

After an open recruitment exercise, Dr Andrew Rose has accepted the engineer post which became vacant on the departure of Osman Zorba. He continues to work full time on the upgrade project. He has been working closely with an Imperial internal part-time PhD student (Simon Fayers, who is a graduate electrical engineer with significant computing skills) implementing the microcontroller code necessary to make the μTCA boards standard compliant, including features such as power-management, temperature control and IPMI messaging. For ten weeks over the summer an Imperial undergraduate has been working very successfully with Andrew Rose producing a web-browser based GUI for visualizing and controlling firmware modules within a running board for the purpose of rapid system development and interactive debugging.

5.5 Expenditure

The major items of expenditure are the optical connectors, FPGAs and Mini-T5 / Maxi-T7 card orders, which are not yet invoiced, but the overall spend is still well within the foreseen envelope.

5.6 Comparisons with CMS activities elsewhere

At present the Mini-T card is a technically more advanced card than anything else in CMS (and perhaps even beyond in LHC) but there are other (US) groups who are aiming to increase their technical capabilities in the digital hardware and firmware areas.

The Wisconsin group have manufactured a μTCA card, currently with only DAQ functionality in mind. It does not use optical links and is limited to 16 transceivers at 3Gb/s, so significantly less powerful than the Mini-T. Wisconsin have played a big role in the present trigger and are responsible for the Regional Calorimeter Trigger (RCT), based on GaAs ASICs and electrical ECL links, so now rather dated and with limited spares as components become obsolescent. They are gaining firmware expertise, although it has not so far been used in CMS.

The Minnesota group have developed a μTCA FED for the HCAL upgrade. The Minnesota card (MINI-CTR2) is also based on a Virtex5 with GTX transceivers (up to 6Gb/s). However the MINI-CTR2 has 16 links whereas the Mini-T has 40; the Mini-T also a large parallel connection to provide a low latency interface that makes it more challenging to design and manufacture (but so far very successfully).

Regarding the trigger philosophy, we have advocated a new approach of time multiplexing the data which has significant benefits while others favour a more conservative approach that would retain the current structure. Time multiplexing concentrates the entire calorimeter trigger data for a given bunch crossing into a single FPGA and dispenses with boundary conditions between processing nodes and thus the custom backplane. (It is analogous to event building by the CMS DAQ which transfers data from many inputs to a single location for processing.) It makes the system extremely flexible (e.g. there are no limits on algorithms due to limited input data as in a conventional trigger). The entire trigger would remain a very powerful image processor that could be reconfigured by simply changing the data selected within the multiplexing units. It also allows special triggers to be placed in parallel with the main triggers for custom searches (e.g. with dedicated hardware).

6. Work Package 4: Pixel tracker development

6.1 Objectives

This report refers to the milestones contained in the pixel project document submitted to the oversight committee in July 2011. The CMS pixel detector upgrade is scheduled to be completed in 2016/17. The initial activities to be undertaken by the RAL PPD team were arrived at in discussion with the CMS pixel detector upgrade project manager, R. Horisberger, and reflect items where the project should benefit from RAL expertise. The UK contribution for calendar year 2011 is principally the development of test stand data acquisition hardware, firmware and software for the upgrade pixel readout chip. The first batch of this chip is expected in early 2012. In the following, the status of the project is specified with respect to the subtasks and milestones listed in the proposal:

6.2 Progress to date

1.1: Set up test stand for existing pixel readout chip at RAL.

1.2: Tune test-board parameters and characterize readout of chips at RAL.

Done.

Laboratory space and two separate test setups are available at RAL.

1.3: Provide technical support for pixel detector test stands in CMS.

Ongoing.

RAL expertise has been deployed to assist in the set up of pixel test areas at CERN. RAL has also resolved several assembly mistakes with test-boards produced in Taiwan. More recently, two malfunctioning test-boards from CERN were repaired at RAL. The RAL group is now responsible for the data acquisition software for the pixel test stands and currently setting up an SVN software repository for official code releases.

2.1: Determine specifications for new DAQ test-board hardware.

Done.

Areas where the current hardware needs to be modified and improved have been identified in discussions with the groups involved in the pixel upgrade project. Electrical and preliminary communication protocol characteristics of the new readout chip and token bit manager chip have been obtained from the respective developers.

2.2: Evaluate possibility of modifying existing DAQ test-board.

Done.

Immediate work, coupled to the development of a new readout chip, requires modification of the existing 50 test-boards. (Ultimately a new test-board will be designed.) Following detailed study of the existing hardware, the RAL group concluded that an adapter approach for the existing board is feasible, using a low-cost FPGA to deserialize the input data stream for use by the existing test-board hardware. The group decided to make the transition from existing test DAQ hardware to a full redesign for the new readout chip in three stages:

• Build a small number of adapter prototypes based on a commercial FPGA evaluation board with a simple add-on PCB to prove the concept in practice.

• Once the adapter has been proven to work, merge FPGA and add-on PCB into a single adapter board for upgrade of all existing DAQ test-boards.

• Merge functionality of adapter and existing DAQ test-board on a redesigned single-PCB test-board for the upgrade readout chip. This will only be required once full-scale production of new readout chips and modules is beginning, in at least a year from now.

The early prototype allows the testing of the adapter design quickly while still retaining flexibility for specification changes concerning the connection to and communication with the readout chip.

2.3: Evaluate possibility to upgrade USB1.1 link between test-board and PC.

Done.

The existing board PC interface (USB1.1) is too slow and on board memory insufficient for the upgraded data rates. This is being modified to a USB2 connection. The RAL group has built two prototype USB2 mezzanine cards for the test-board and modified the DAQ software to interact with them. Both prototypes are operational.

2.4: Design adapter board for connection to single readout chips.

Done.

Schematics and PCB layout for the prototype adapter board were designed by RAL and the University of Bristol. This PCB revision features a connection for a single readout chip on a carrier board that is already in use for the existing chip.

2.5: Design adapter board for connection to pixel modules.

Deferred due to missing input from other groups. Not critical for progress of the project.

The connector for interface to an entire pixel module has yet to be specified by the groups responsible. The firmware functionality for the module readout is already being implemented by RAL and can be tested with a module emulator. Modifications of the adapter board for pixel modules will then be limited to accommodating an additional connector on the PCB.

3.1: Build adapter board prototypes.

Nearing completion. Was planned for Sept 2011.

The prototype adapter PCB has been submitted for production, and is expected to be available for tests in late September or early October 2011. High-speed deserializer firmware for the adapter board is being written at RAL. It is largely complete and is being tested on an FPGA simulation. An emulator to enable tests before the new readout chip is available has been created by the RAL group. This uses a standard FPGA evaluation board and generates data patterns provided by PSI chip designers.

3.2: Modify firmware of existing test-board to accommodate input of new readout chip.

Work beginning now. Due Nov 2011.

Firmware modifications are required for the deserialized input and the USB2 output interface to enable desired data rate performance. Work has begun on this.

In summary, the test stand data acquisition hardware project for the CMS pixel detector upgrade is on schedule and proceeding as planned. Work on the other proposed projects (test beam programme for the upgrade readout chip, pixel pilot modules) has begun on a low level (planning for test beams, participation in existing pixel detector operations through pixel shifts) but will mostly become relevant in 2012.

6.3 Deliverables

Presently there are no formal milestones for this Work Package.

6.4 Staff on project

Reported in accompanying tables. RAL PPD is presently the subject of a review and further cuts in staff are expected, but the outcome of the review is not yet public. However, the impact on CMS and the upgrade project is not yet known and may be modest. We hope to report on this at the OSC meeting.

6.5 Expenditure

The only expenditure is staff costs in RAL PPD, originally allocated to WP1, and at present there is no other budget allocation.

6.6 Comparisons with CMS activities elsewhere

The possible role of RAL PPD and other groups with interests in the same area is under discussion. The pixel DAQ and module testing is a significant effort and will likely need multiple contributions.

7 Risk register

The current version of the project risk register is v4.0, revised from the version presented at the last meeting. Each line of the risk register has been reviewed recently and comments have been added where appropriate.

Overall progress continues to be good, and the delay in delivery of the CBC chip has effectively been superseded by its success.

The major risks remain unchanged, namely possible shortfalls in funding and loss of key staff. A new component of that is the uncertainty regarding the future of RAL PPD and a new risk item has been added.

The overall timescale of the High Luminosity LHC has changed once again, as noted. The overall timescale for the full high luminosity project may continue to change; however the Phase I part which involves a major contribution is becoming more definite.

Regarding the assignment of red/amber/green to risks discussed at the last meeting, it may be worth bearing in mind that the risk values assigned have so far referred to the *final upgrade* of the LHC and CMS. However, if they are considered only to apply to *this* R&D project, then they are certainly much reduced.

8 Finances

The financial report is summarised in the attached tables.

The STFC finance reporting system via the Research Councils Shared Services Centre now seems to be reliable enough to extract figures for RAL PPD and Technology Department spending, which has allowed reporting to the end of the last quarter (30 June 2011). However, the staff costing model used for PPD required some adjustment of the figures for 2010/11 only (approximately £28k reduction compared to the SSC reports) for internal STFC accounting reasons.

Travel spending has remained modest, partly due to the fact that many trips are combined with other CMS business. Upgrade travel spend is now increasing, with beam tests and more frequent meetings in CERN; a US CMS upgrade workshop is foreseen in October 2011 and more conference presentations are expected.

Equipment spending, which covers mainly ASIC foundry costs and trigger board manufacture, still lags behind early forecasts. The first CBC was manufactured on a Multi-Project Wafer (MPW) run, whose cost was dominated by a large prototype chip designed by RAL for XFEL. How much sharing will be possible in the next submission in 2012 is not yet clear, but is likely to require a greater share of the investment. The production of further trigger boards is steadily increasing and will increase the rate of expenditure considerably in the coming year. We plan an internal review of the remaining spending in WP2 and WP3 in the coming months to optimise our use of resources.

Engineering staff spending at RAL has also ramped up considerably in the last financial year, as expected.

For WP1, staff spending within university groups is approximately as expected. The Brunel allocation is exhausted. Bristol funding will run out at the end of 2011. This puts posts, and further work, in jeopardy.

In the last financial year, RAL PPD has used most of the staff effort originally allocated to WP1 in support of the pixel development and proposes to use the remaining funds in the same way.

The Working Allowance currently stands at £220k, with the reserve held for Bristol equipment reduced from £10k to zero.

For clarity, the end dates of the different grants, reflecting the approved duration of each grant and the start date reported to STFC, are:

Institute	Contributing to WPs	Start date	End date
Brunel	WP1	1-Jan-2009	30-Jun-2011
Bristol	WP1 & WP2	1-Jul-2009	30-Jun-2012
Imperial	WP2 & WP3	1-Jun-2009	28-Feb-2013
RAL PPD	WP1	1-Jan-2009	30-Jun-2012
RAL TD	WP2	1-Jun-2009	28-Feb-2013