

UK CMS Upgrade Oversight Committee

12 November 2013

University of Bristol
Brunel University
Imperial College London
Rutherford Appleton Laboratory

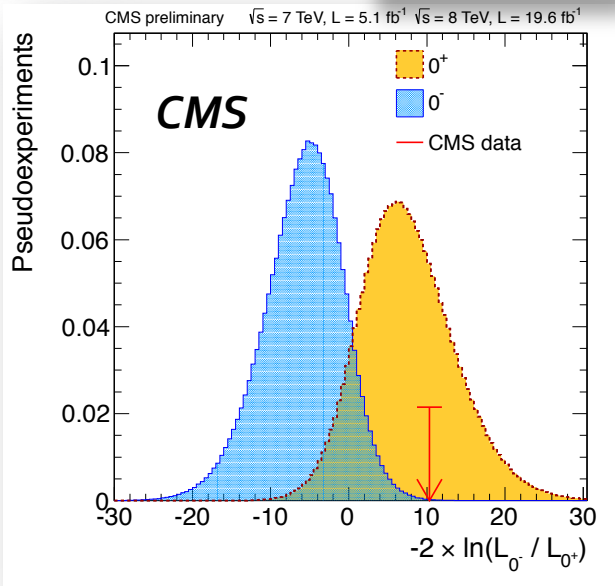
Geoff Hall

- Snapshots of CMS & LHC status
 - Recent summaries at October RRB & ECFA HL-LHC workshop
 - LHC: LS1 on schedule and machine very confident to be ready for restart
 - Plans beyond that are still uncertain
 - funding & scheduling issues
 - overview of experiment requests compiled by S Bertolucci for RRB
- Summary of UK upgrade project
 - Recent WP progress
- Finances and other issues



Spin-Parity

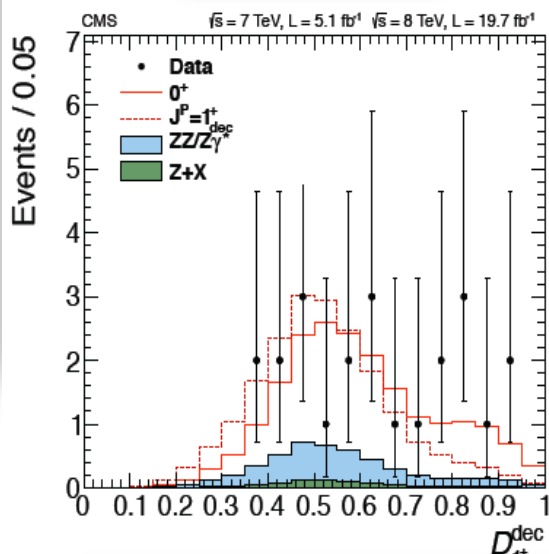
0^+ vs. 0^-



0^- Excluded @ 99.8% CL

ALL ARE CONSISTENT WITH $J^P = 0^+$

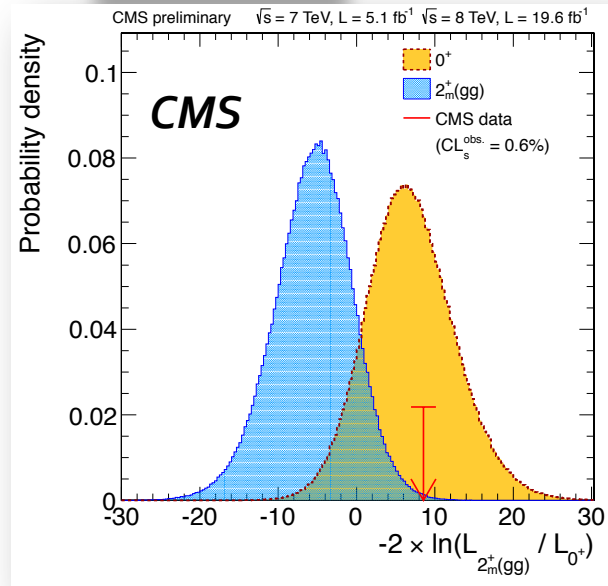
0^+ vs. 1^+



New Spin 1 Exclusions

1^-	$q\bar{q} \rightarrow X$	0.001%
1^-	any	0.001%
1^+	$q\bar{q} \rightarrow X$	0.03%
1^+	any	0.01%

0^+ vs. 2^+

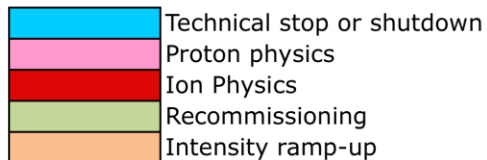


New Spin 2 Exclusions

2^+_{m1}	$gg \rightarrow X$	0.04%
2^+_{m2}	$q\bar{q} \rightarrow X$	0.03%
2^+_{m3}	any	3.0%
2^+_b	$gg \rightarrow X$	0.9%
2^+_h	$gg \rightarrow X$	3.1%
2^-_h	$gg \rightarrow X$	1.7%

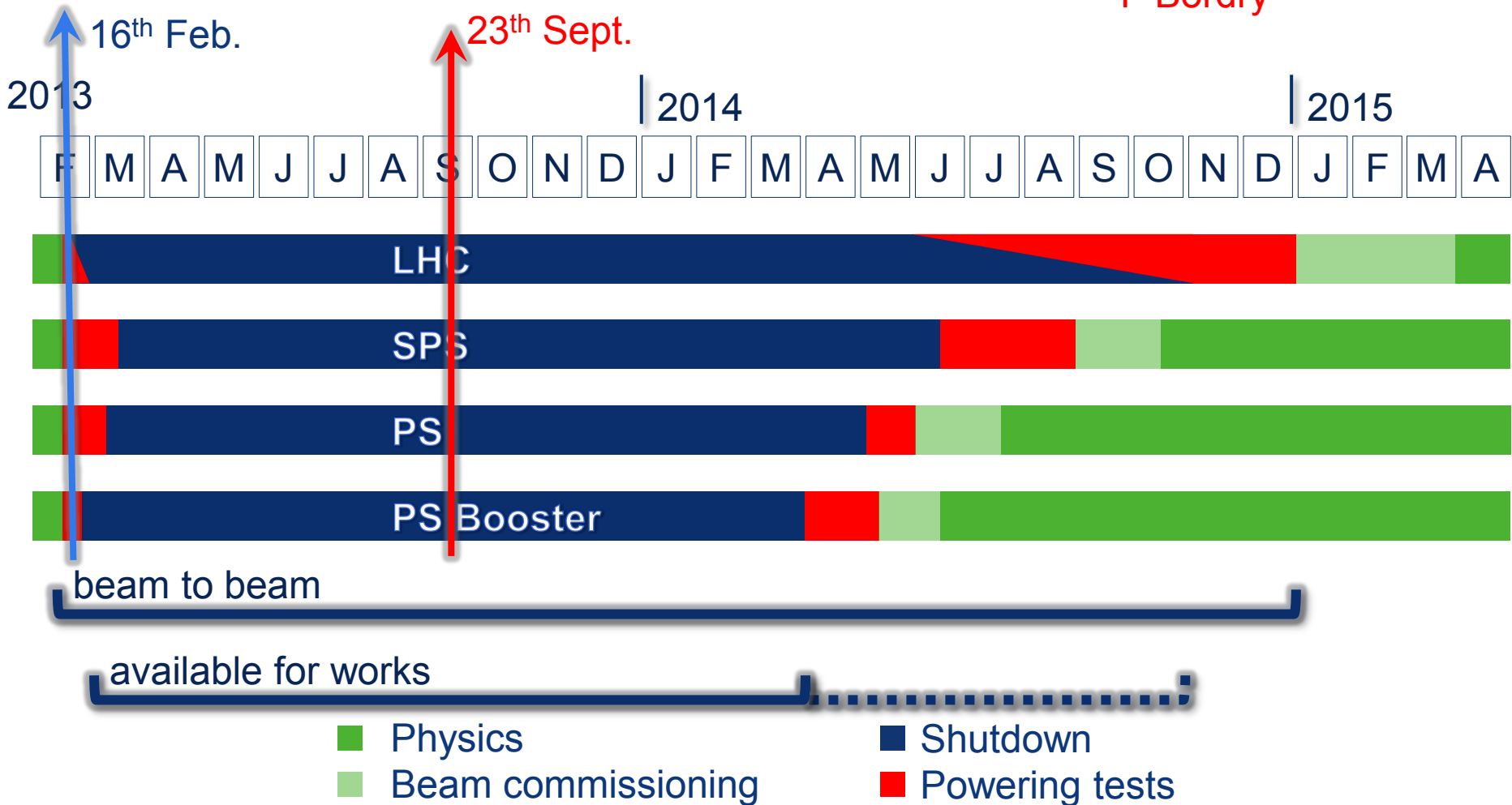
“Baseline”

	J	F	M	A	M	J	J	A	S	O	N	D
2011		1	2	3	4	5	6	7	8	9	IONS	
2012			1	2	3	4	5	6	7	8	9	
2013	IONS	IONS	LS1 - SPLICE CONSOLIDATION									
2014												
2015	CHECK-OUT	RECOM	RECOM	RAMP-UP	2	3	4	5	6	7	IONS	
2016		RAMP-UP	1	2	3	4	5	6	7	8	IONS	
2017		RAMP-UP	1	2	3	4	5	6	7	8	IONS	
2018	LS2 (LIU UPGRADE: LINAC4, BOOSTER, PS, SPS...)											
2019	RECOM	RECOM	RAMP-UP	1	2	3	4	5	6	7	IONS	
2020		RAMP-UP	1	2	3	4	5	6	7	8	IONS	
2021		RAMP-UP	1	2	3	4	5	6	7	8	IONS	
2022	HL-LHC UPGRADE											

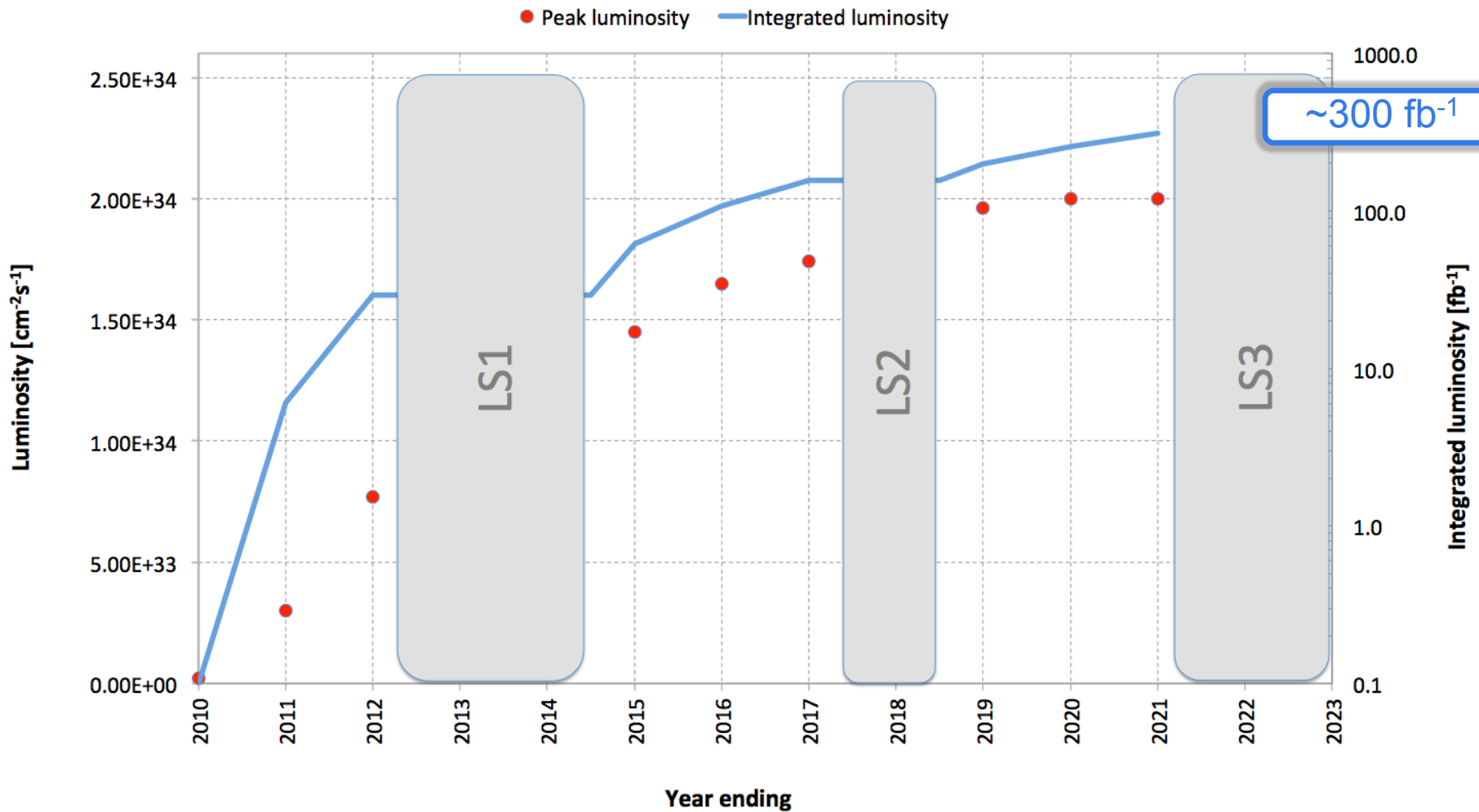


LS 1 from 16th Feb. 2013 to Dec. 2014

F Bordry



“Baseline” luminosity





LHC experiments on same page

	ATLAS		ALICE		CMS		LHCb	
YETS 2016-17 duration	Min needed by LHC		Min needed by LHC		4.5 mo (i.e. 6w more)	Pixel upgrade	Min needed by LHC	
Preferred LS2 start	end 2017	Trigger upgrade	end 2017	ITS,TPC & readout upgrade	end 2018.	HCAL upgrade	end 2018	Readout upgrade
Required LS2 duration	14 mo	Trigger upgrade μ Small wheels	18 mo	ITS, TPC 4GEM, MFT	14 mo	HCAL upgrade & Phase 2 start .	18 mo	VELO, RICH, Tracking, 40MHz readout.
Preferred LS3 start	end 2021	Tracker replace- ment ready	3 y after LS2 end		end 2022 < 500fb-1		3 y after LS2 end	
Preferred LS3 duration	27-35 mo		Min needed by LHC		30-35 mo	Tracker, EE and HE repl.	Min needed by LHC	

Answers (from RLIUP) to Important Questions

- Radiation Limit for detectors and machine
 - 300 – 500 fb⁻¹ (machine possibly more critical)
- LS2 needs ~18-24 months
- LS3 needs ~24-36 months
- Run2 should last for 3 years

What needs to be done with some urgency

- Decide on the shutdown scenario
(Management of CERN and detectors)
- Implementation of new plan
 - A global resources loaded schedule for accelerators and experiments
 - Limitations imposed on personnel by radiation
 - Improve access to tunnel
- Start now with requests, to identify and strengthen weak areas of expertise



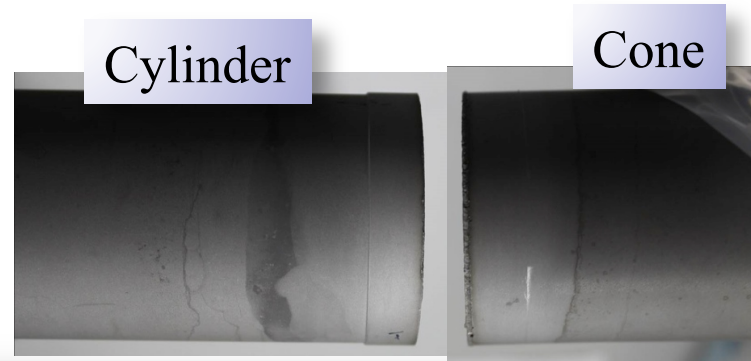
CMS Status in a Nutshell

- **Phase 1 Upgrades**
 - Common item costs were reviewed and revised downward
 - Much progress and on schedule
- **Long Shutdown 1 (LS1), including many phase 1 upgrade tasks**
 - Work goes well
- **Run 1 Physics**
 - Analyses well on track to meet our goals
- **Run 2 Preparations**
 - Progress on cpu-efficiency, tools and procedures
- **Phase 2 Upgrades**
 - Preliminary scope and cost has been documented, presented today



Technical Coordination: LS1 project

- Cost to complete LS1 common project is within original estimates.
- Activities at P5: On-going with good progress
 - *Tracker colder*
 - *ME 1/1 revision*
 - *HCAL revision part I*
 - *YE4 installation*
- Other activities progressing well too
 - *CSC assembly, testing, installation*
 - *RPC assembly and testing*
 - *Pixel cooling system pre-assemblies*
 - *Beampipe*



- All OK, except for delay recovering beampipe incident, again!
 - On two occasions, during removal from the EB welding-facility, pipe broke at a weld.
 - Discussing with vendor to make sure to get it right this time.
 - Specialized tooling for conical section probably necessary
 - Still can make schedule if it does not happen a third time.
 - All costs being borne by vendor



CMS Upgrade program in one slide

J. Incandela October 2013 CMS Status and Upgrades Financial Plan 37th Resource Review Board



LS1 consolidation: Complete/consolidate for nominal LHC beam conditions: Prepare for: 13 TeV, 10^{34} Hz/cm², Ave. Pileup (<PU>)~25

- Complete Muon system (4th endcap station) and improve readout electronics
- Replace HCAL photo-detectors and backend electronics in a couple of regions
- Make it possible to operate the Tracker at -20°C

Phase 1 upgrades: Prepare for 1.6×10^{34} Hz/cm², <PU> ~40, ≤ 200 fb⁻¹ by LS2 Prepare for 2.5×10^{34} Hz/cm², <PU> ~ 60, ≤ 500 fb⁻¹ by LS3

- New L1-trigger system ready for 2016 data taking
- New Pixels ready for installation in 2016/17 Year End Technical Stop (YETS)
- Install new HCAL photodetectors and electronics in 2015 YETS and LS2

Phase 2 upgrades: Prepare for $\geq 5 \times 10^{34}$ Hz/cm², PU 140 to 200
Total of 3000 fb⁻¹ in ~10 yrs operation

- Replace subsystems that no longer function due to radiation damage
- **Tracker including Pixels, Endcap calorimeters**
- Maintain physics performance at very high PU
- **New Electronics and Trigger, enhanced detector coverage**

- **CMS Phase 2**
- The minimal set of upgrades that replace degraded systems and provide requisite physics sensitivity for the highest priority physics goals in the face of 140 pileup events per bunch crossing, and to assure the ability to run up to at least 3000 fb⁻¹



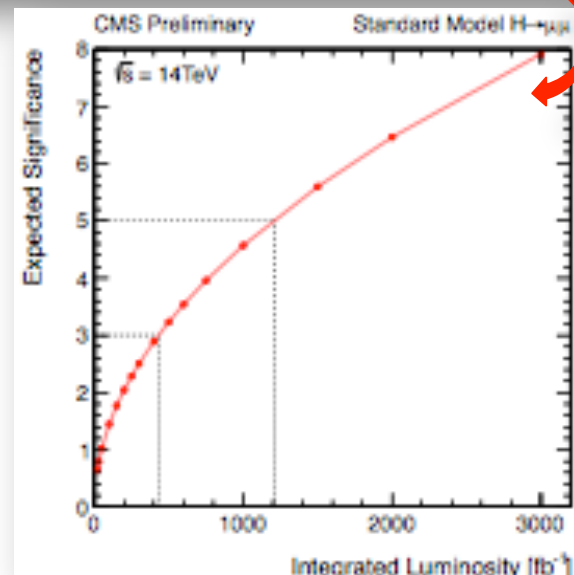
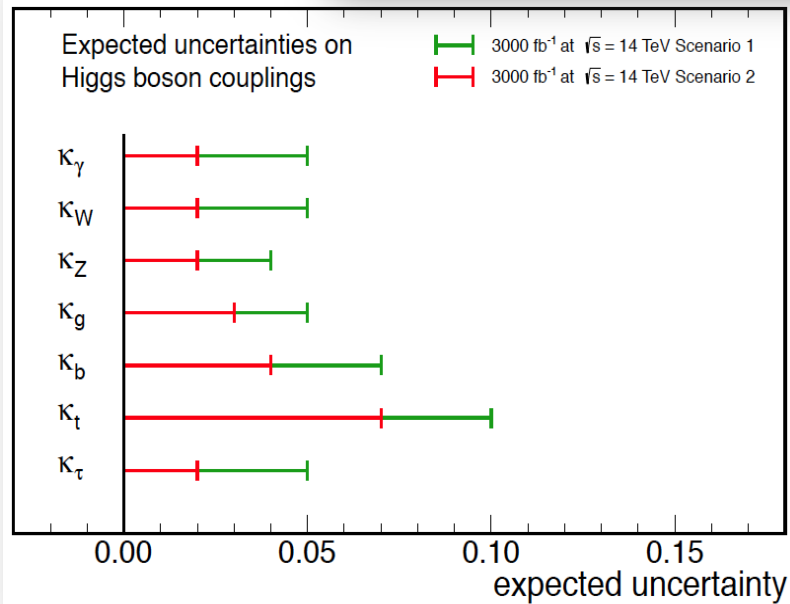
CMS@HL-LHC

- Projections for Higgs couplings
 - 2-10% with HL-LHC
- Rare Higgs decays studied*
 - $H \rightarrow \mu\mu$ at $> 5\sigma$ with HL-LHC
- Low Mass Stops
 - Already with 300 fb^{-1} , discovery potential direct production mode up to $\sim 900 \text{ GeV}$

2-10% precision
on Higgs
couplings

L (fb^{-1})	κ_γ	κ_W	κ_Z	κ_g	κ_b	κ_t	κ_τ	$\kappa_{Z\gamma}$	κ_μ
300	[5,7]	[4,6]	[4,6]	[6,8]	[10,13]	[14,15]	[6,8]	[41,41]	[23,23]
3000	[2,5]	[2,5]	[2,4]	[3,5]	[4,7]	[7,10]	[2,5]	[10,12]	[8,8] new

CMS Projection





Phase 2 Upgrades

Muon system

- GEM Glass RPCs
- Extended η coverage
- New DT minicrates

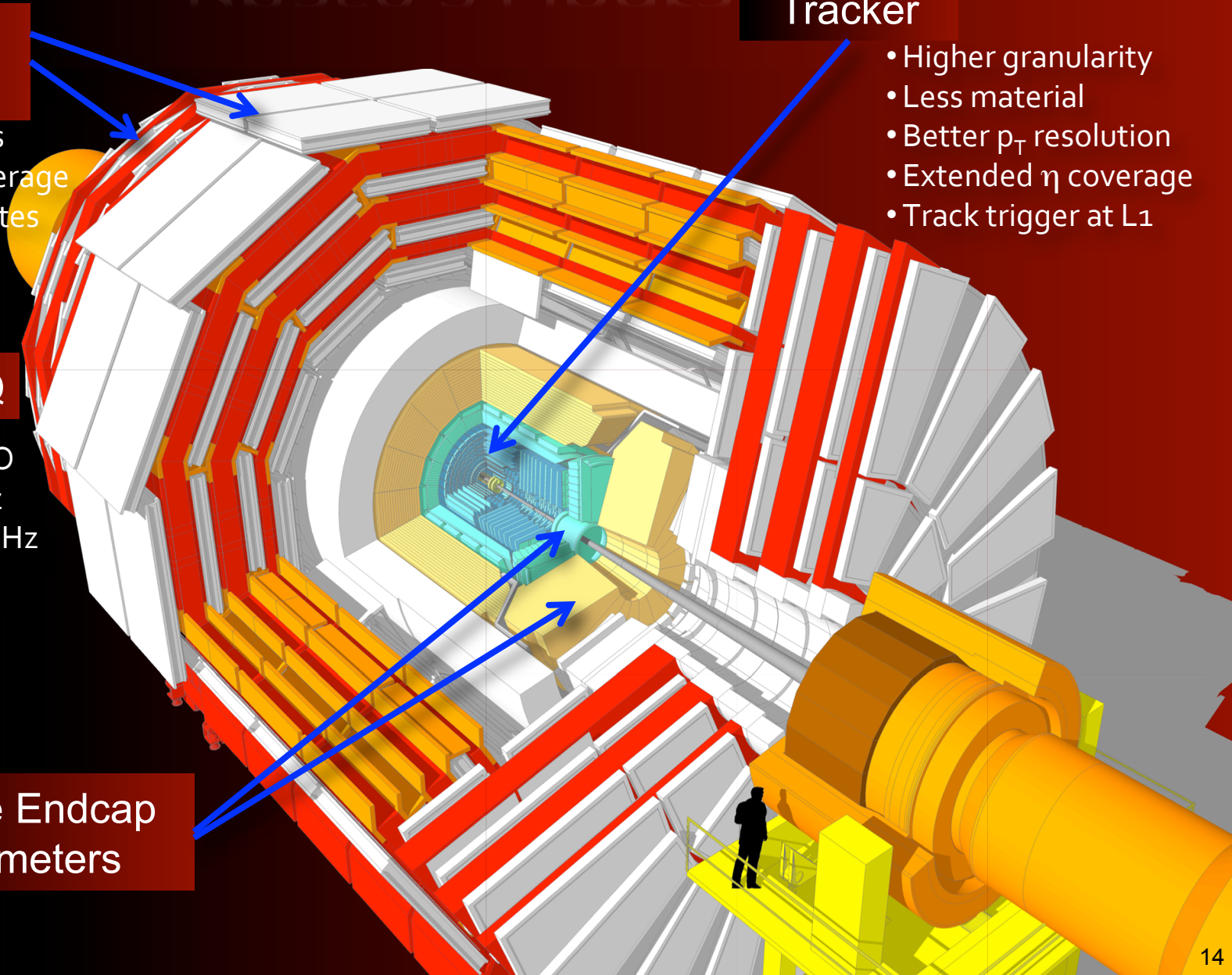
Tracker

- Higher granularity
- Less material
- Better p_T resolution
- Extended η coverage
- Track trigger at L1

Trigger/DAQ

- New FE and RO
- L1 up to 1 MHz
- HLT up to 10 KHz
- Tracking at L1

Replace Endcap Calorimeters





CMS Phase 2: Conclusions Thus Far

- Systems that do not need to be replaced
 - Barrel calorimeters, HF and muon chambers will perform to 3000 fb^{-1}
- Systems that must be replaced are
 - Tracking system and Endcap calorimeters must be upgraded in LS₃
 - Neither survives much beyond LS₃
 - Endcap calorimeters:
 - Extensively studied ways to recover EE crystals.
 - *No practical solution found.*
 - With phase 1 upgrades the HE survives until LS₃ but not much beyond.
 - Electronics for specific subsystems

Relatively
new
requirement



Phase 2 Tracker: conceptual design

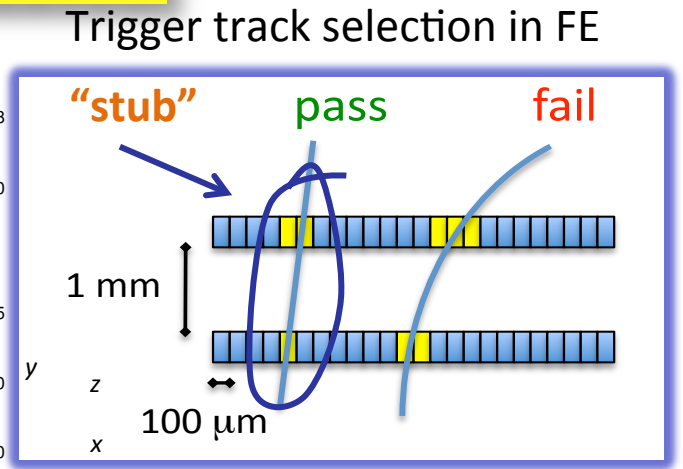
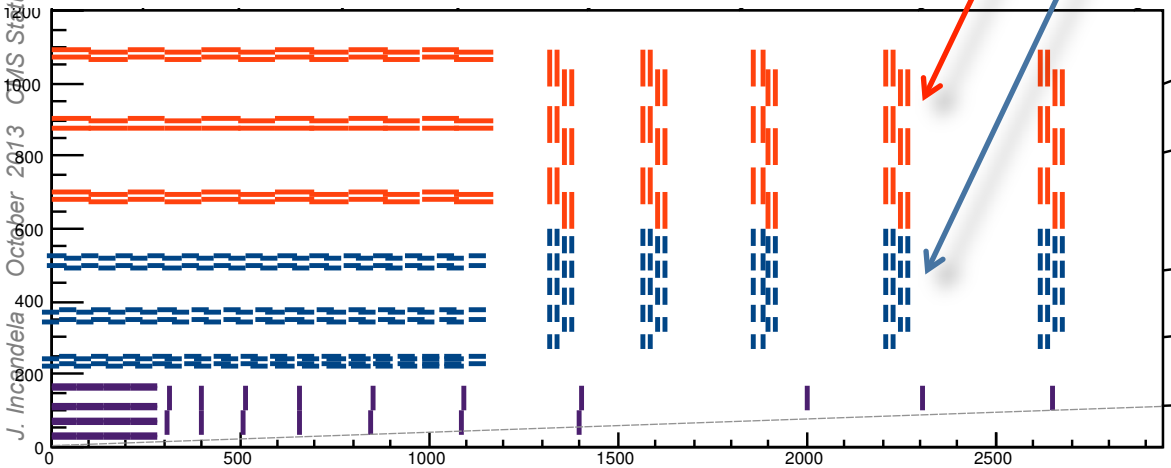
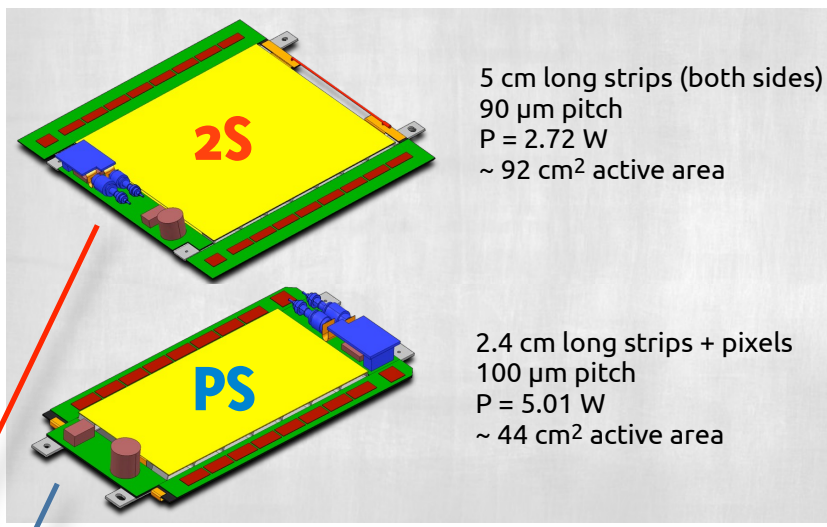
37th Resource Review Board

October 2013 CMS Status and Upgrades Financial Plan

J. Incandella

- Higher granularity, less material
 - Track reconstruction at PU 140 and beyond
 - 2 sensor "Pt-modules" to provide L1 trigger information at 40 MHz for $Pt \geq 2\text{GeV}$
- Pixels: sensors 100 μm thick
 - Smaller pixels: $\sim 30 \times 100 \mu\text{m}$
 - 4 barrel layers, 10 disks to cover up to $|\eta| = 4$
- R&D activities: All components
 - Sensors and readout electronics
 - Prototype of 2S modules ongoing
 - BE track-trigger tbd

Trigger - major new endeavour





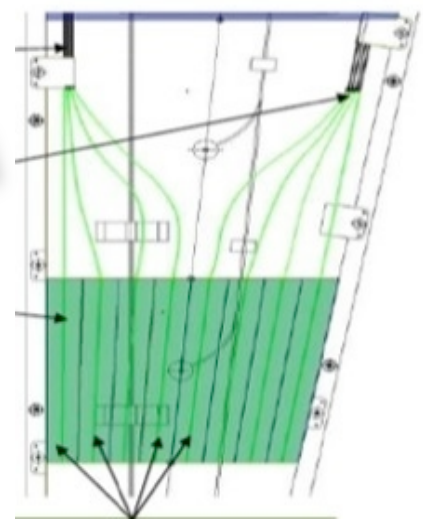
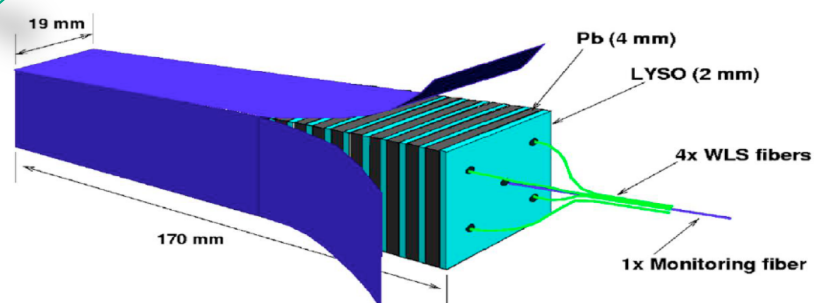
Early stage.
R&D urgent

Endcap Calorimeters

Two approaches

1. Maintain tower geometry - develop rad-tolerant solutions for 3000 fb⁻¹

- EE towers e.g. in Shashlik design (crystal scintillator: LYSO, CeF)
- Te build HE with more fibers, and rad-tolerant scintillator



2. Alternative geometry/concepts

- Potentially improved performance and/or lower cost
 - Dual fiber read-out: scintillation & Cerenkov (DROC) – alla DREAM/RD52
 - Particle Flow Calorimeter (PFCAL) – following work of CALICE

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Phase 2 Cost Exercise

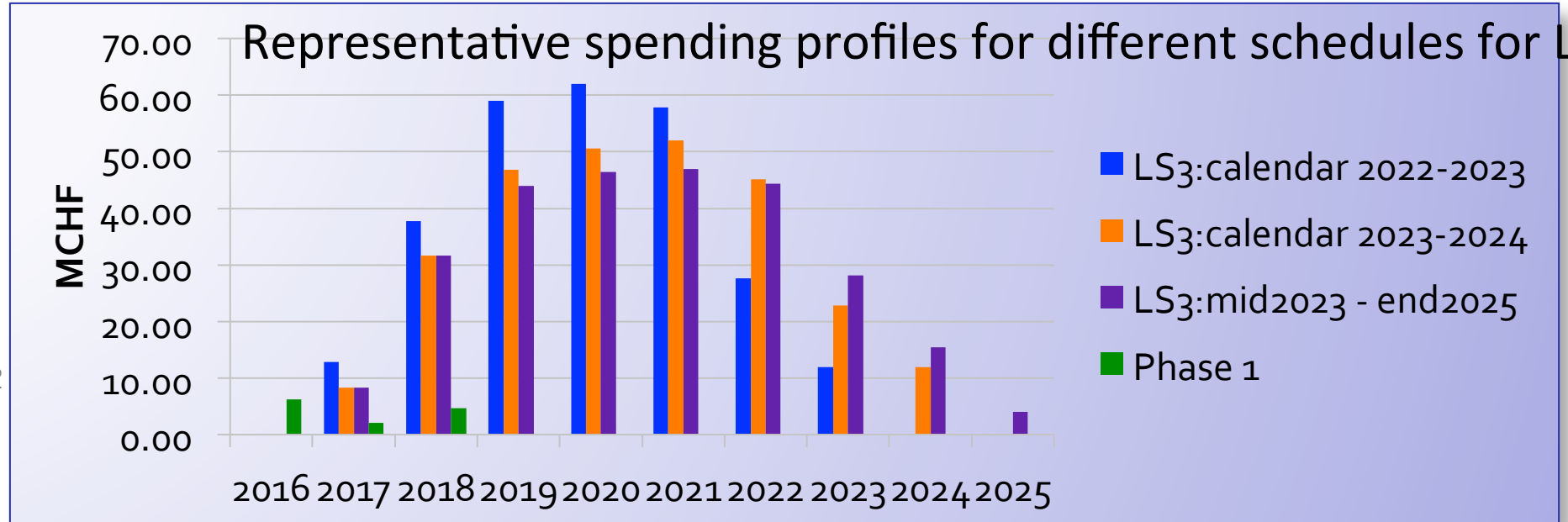
- Used reasonable assumptions
 - Materials, channel counts, etc.
 - No contingency included
- Breakdown of costs
 - Replacement of radiation damaged detectors ~ 75%
 - Retaining performance in very high pileup environment ~ 15%
 - Extending coverage < 10%
- Staging under study
 - Options are limited

Summary of Phase 2 Costs		
Item	Sub-item	Estimated CORE Cost (MCHF 2013)
Tracker	Silicon Tracker	94
	Pixel Detector	34
		127
Calorimeters	Endcap Calorimeter Upgrade: EM & HAD	67
	HF upgrade to 4-channels per PMT	2
		69
Muon System	DT Electronics	7
	Endcap Muon System Upgrade	12
	High Eta Muon Tagging Station	6
		25
Trigger System and Front-end Electronics	L1-Trigger	7
	EB Frontend Electronics	11
		18
DAQ and HLT	DAQ system: Clock, Readout, Network	5
	HLT	6
		11
Infrastructure and Common Systems	Shielding Changes for HL-LHC	6
	Tooling, rail systems, cranes for LS3 work	5
	Common Systems and Installation	9
		19
Total		269



Phase 2 Spending Profile

- Profile driven to a large extent by the LS3 start and duration
 - Tracker and Endcap calorimeters need to be competed in LS3*



- An extra year flattens the profile. Diminishing impact beyond that.
- Phase 1: 66% of spending will be complete by end of 2014**

Blue = the current LHC baseline schedule. **Orange** and **Purple** represent alternative LS3 dates.

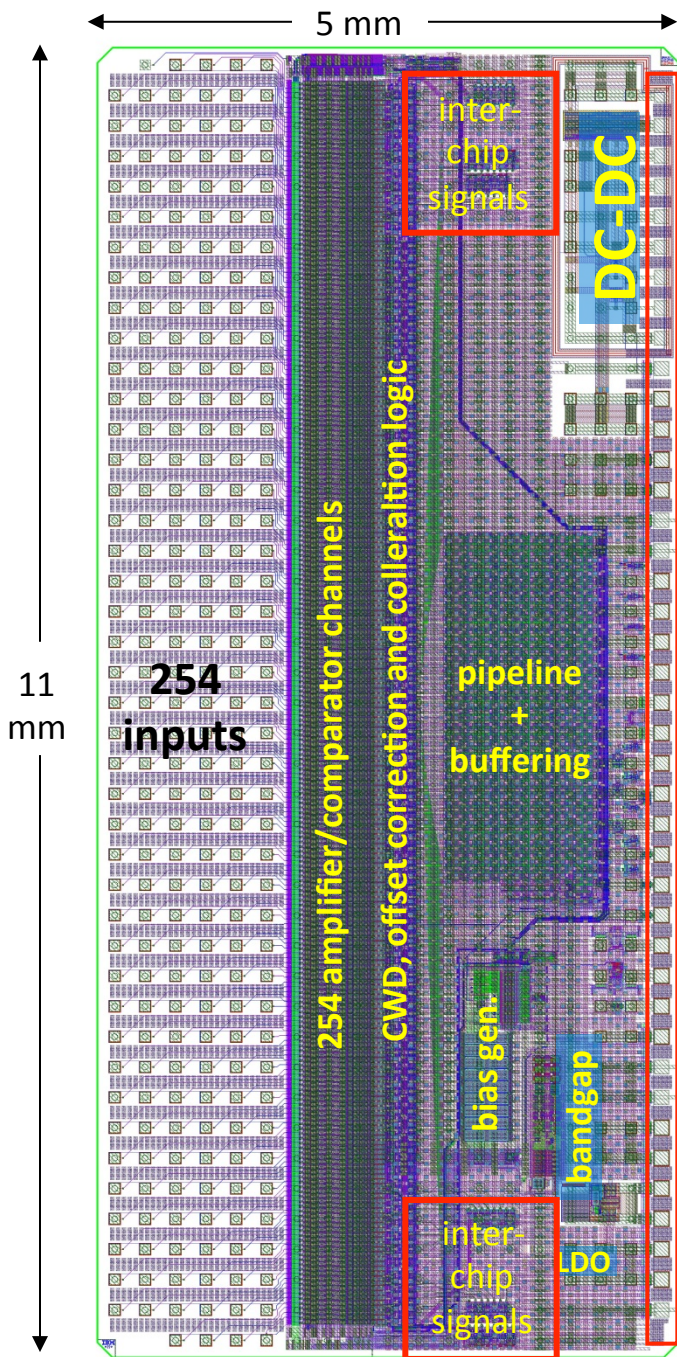
UK R&D status

Evolution of objectives

- Original goal
 - new – improved - tracker with similar angular coverage, constrained by re-using existing services
 - provide some part of tracker data to L1 trigger to contain rate to 100 kHz
- More recent developments
 - Baseline Tracker design now adopted
 - “conventional” barrel-endcap layout looks optimal
 - but CMS exploring enhancing forward region physics as well as standard physics programme
 - uncertainty if L1-track triggering will reduce rate to 100 kHz in $6.4\mu\text{s}$
 - ideas (and detector requirements) not yet validated by simulations
 - possible objective of L1 readout up to 1 MHz/10-20 μs
 - both approaches require on-detector data reduction

WP2 objectives and status

- Complete CBC & 2S-module development for construction project
 - development, with collaborators, of 2S module, and evaluation studies
 - to be ready for mass production with hardware and software for large scale acceptance tests
 - contribute to PS-module readout development
 - FC7 for CBC module readout
 - generic-type board, to be utilised by multiple projects, in collaboration with CERN
- Good progress with CBC2 evaluation
 - chip is functioning well and suitable for prototypes
 - 2 wafers so far tested. Plenty of chips in hand
 - First (ever!) beam test of PT-module imminent
 - DESY 25-30 November



Geoff Hall

Reminder only

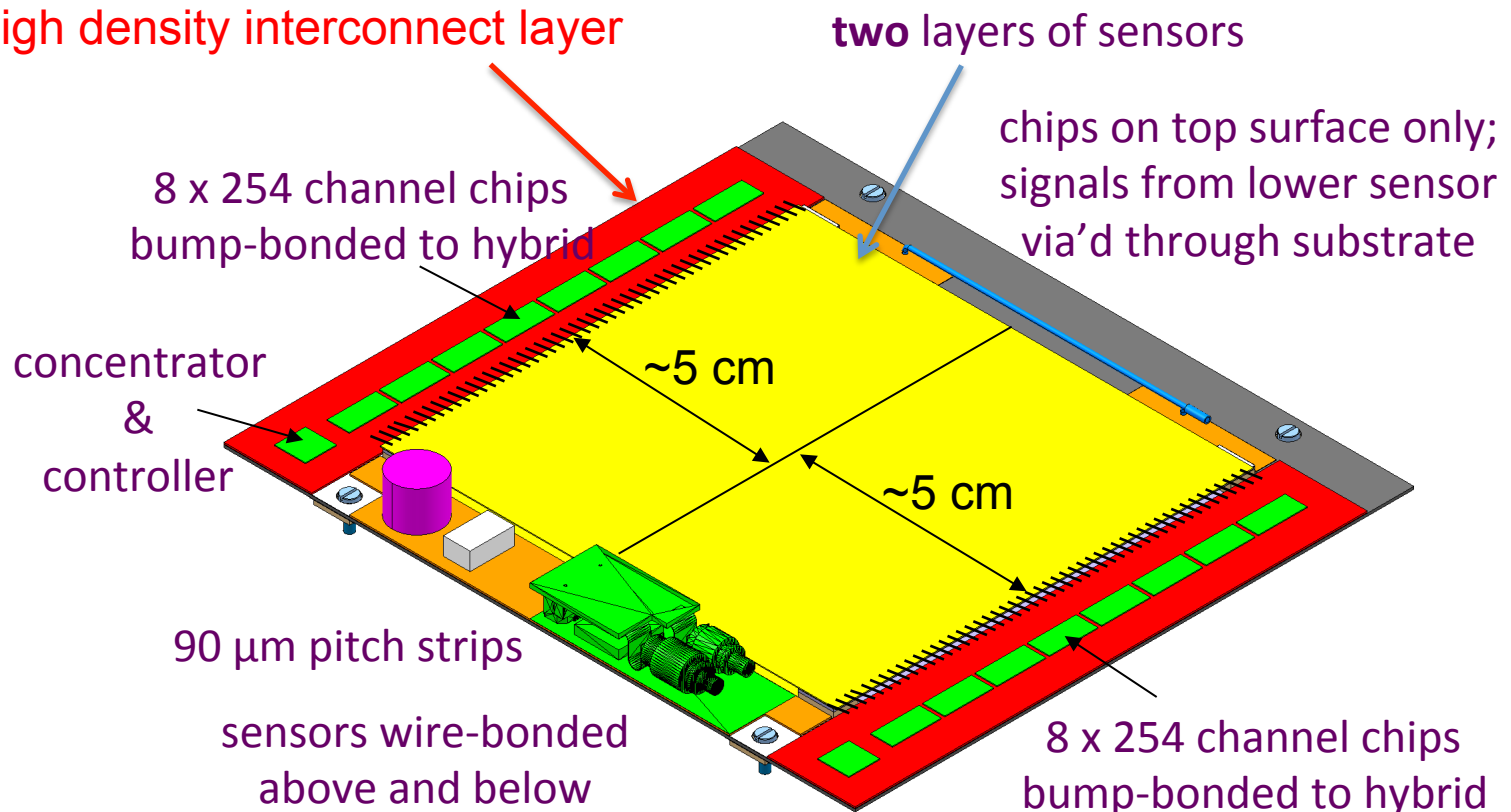
CBC -> CBC2: New features

- 250 μ m pitch C4 layout
 - aim for commercially assembled module
 - some gains in bond inductance
 - back edge wire-bond pads for wafer probe
- 254 channels for 127 + 127 strips
- correlation logic for stub formation
 - between top & bottom strips
 - vetoes wide clusters
- Test pulse
 - no time to implement on CBC
 - & other minor circuit improvements
- Improved DC-DC (CERN)
- received Jan 2013 – fully functional

Reminder only

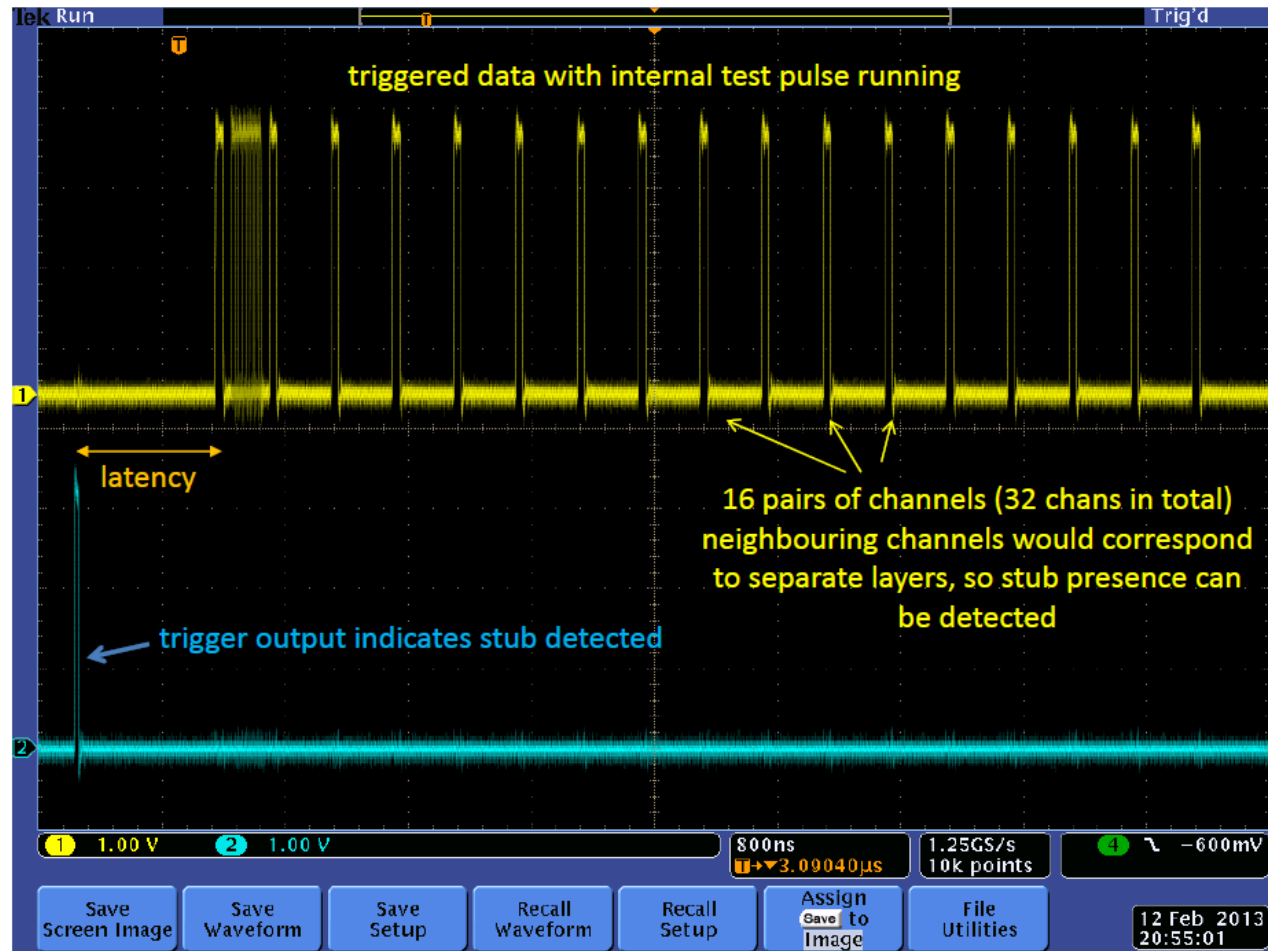
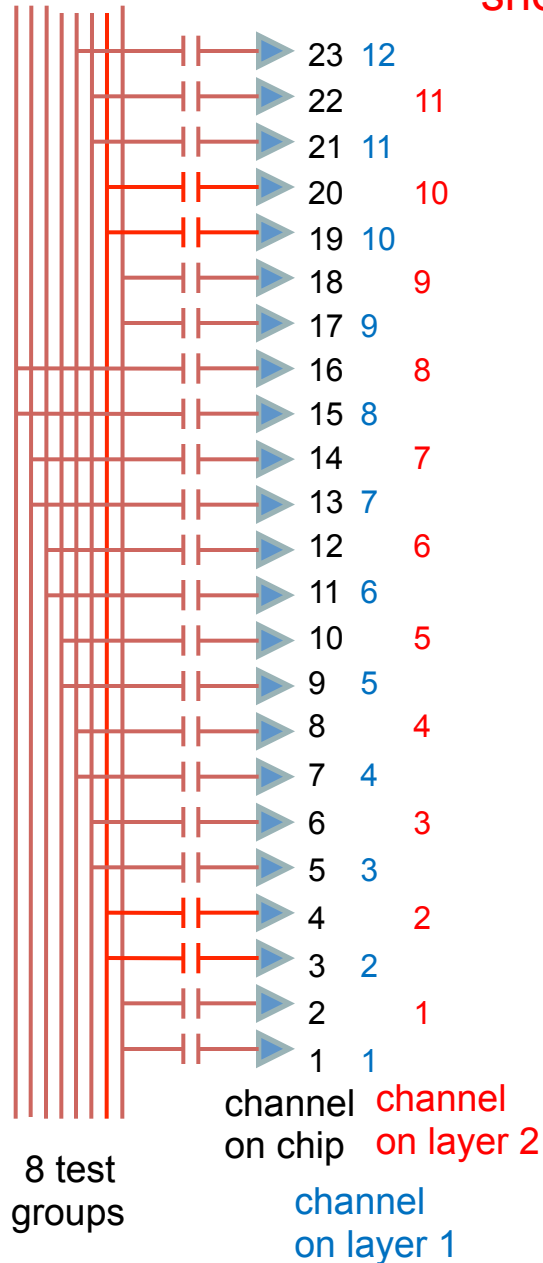
2S PT-module with CBC2

- **Track & trigger** μ strip module for outer tracker region
 - CBC2 logic correlates hits on two sensors to reject those from low p_T tracks



shown in March OSC

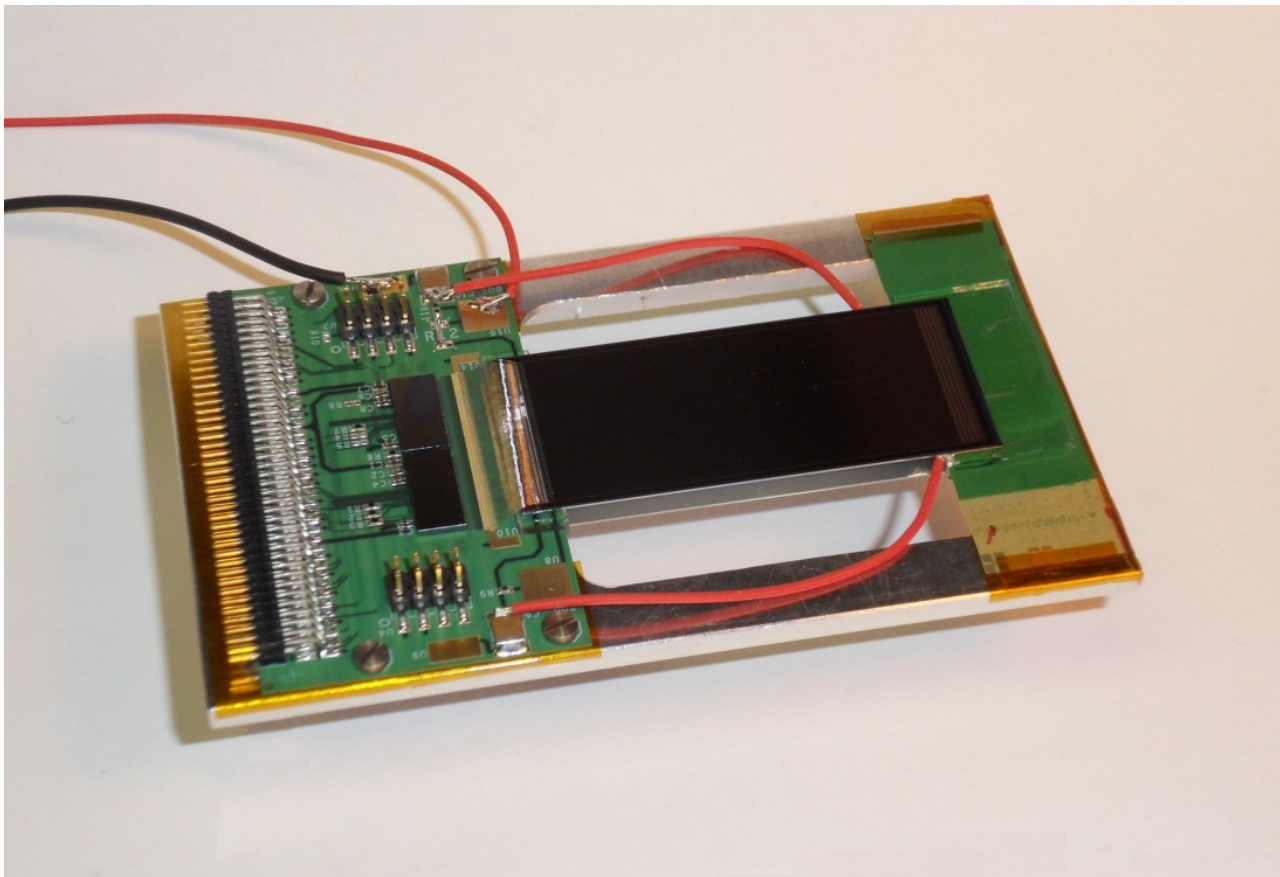
Result with test pulse



– Proves basic functionality

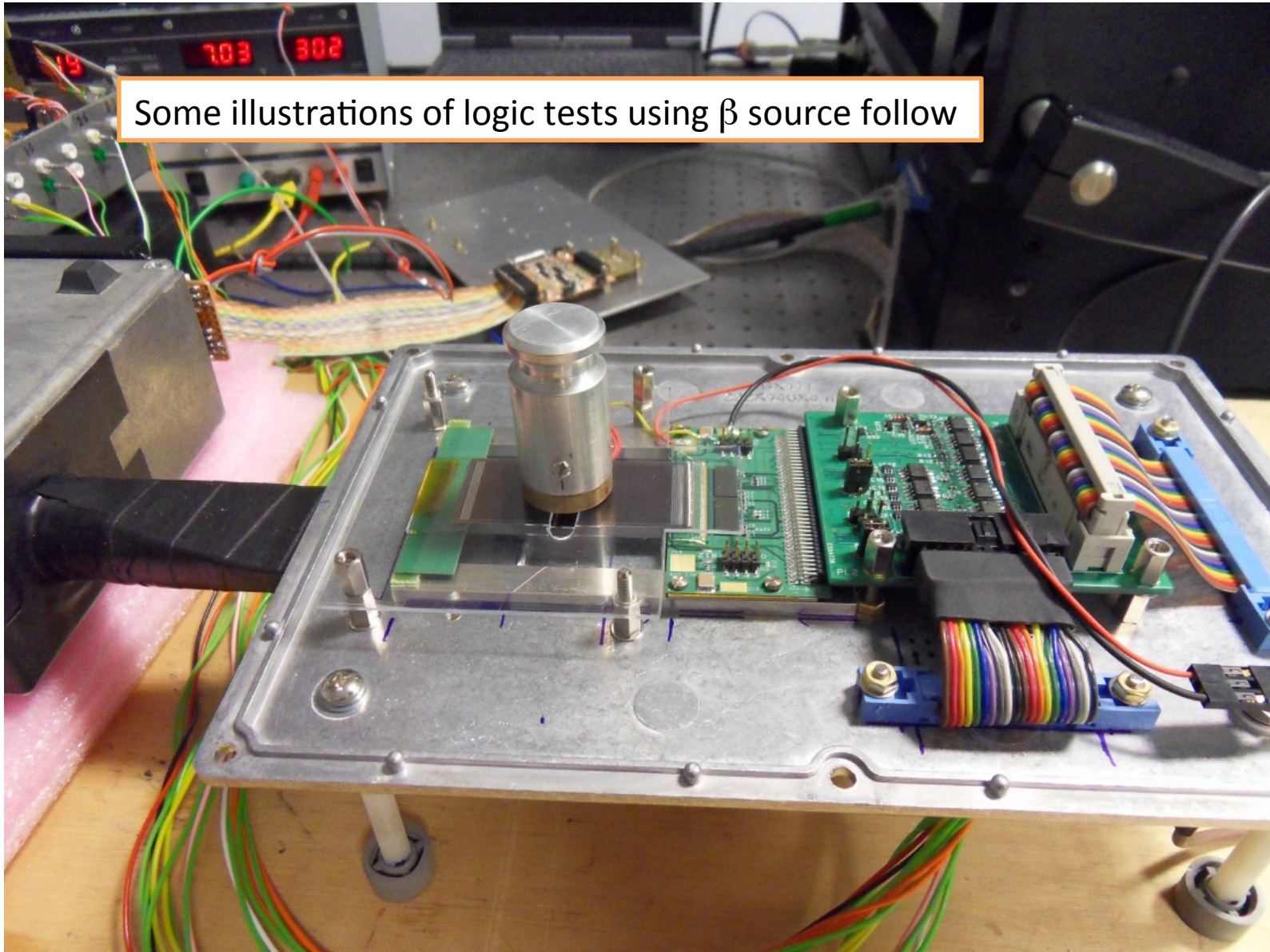
2S mini-module

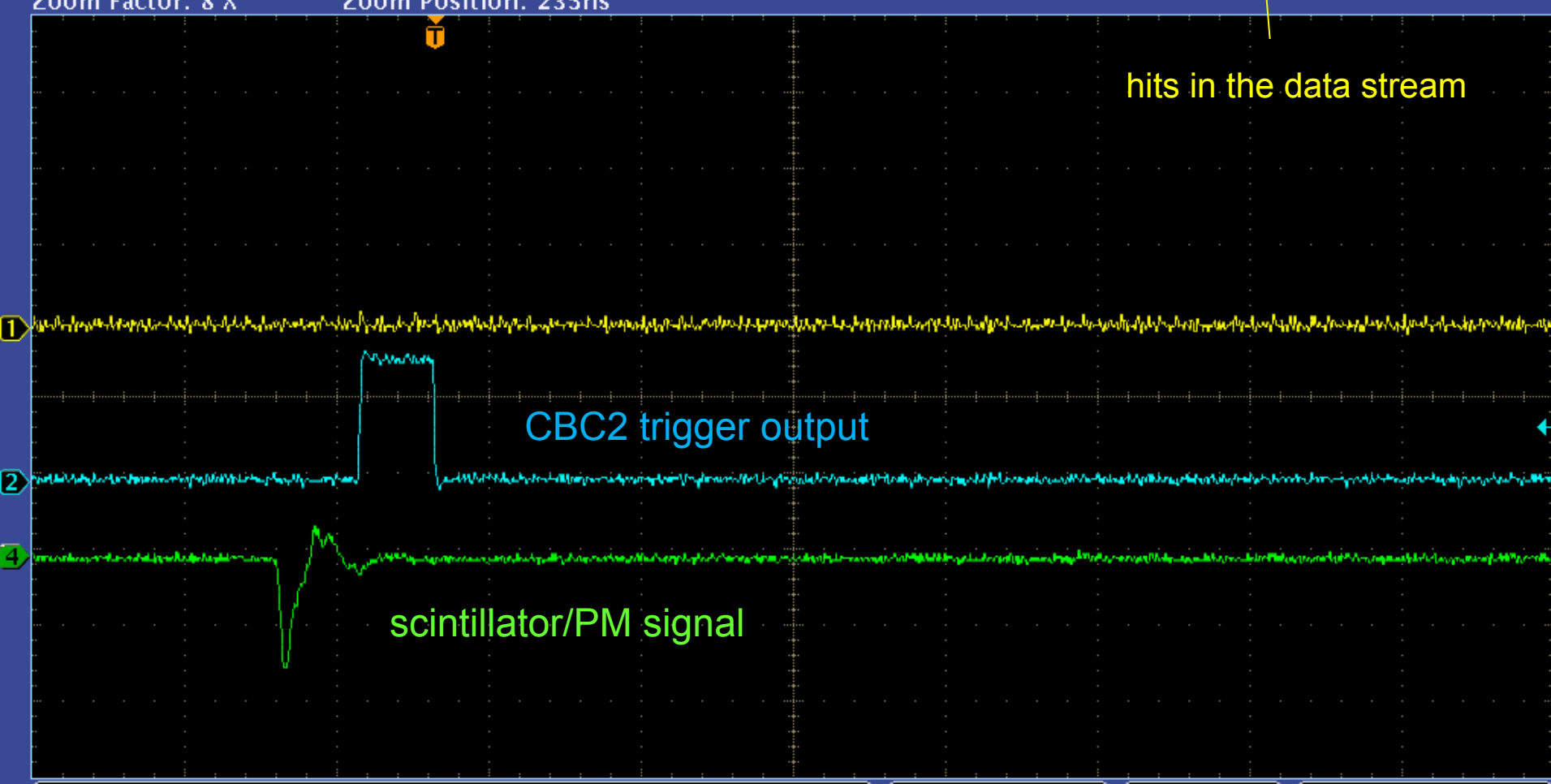
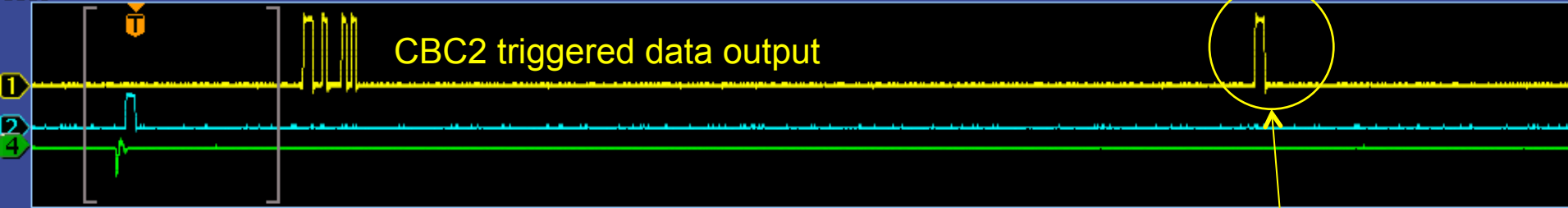
- Several prototypes assembled with two sensors
 - Under test in lab since July
 - Preparing for DESY beam test in two weeks time



2S mini-module in lab

Some illustrations of logic tests using β source follow

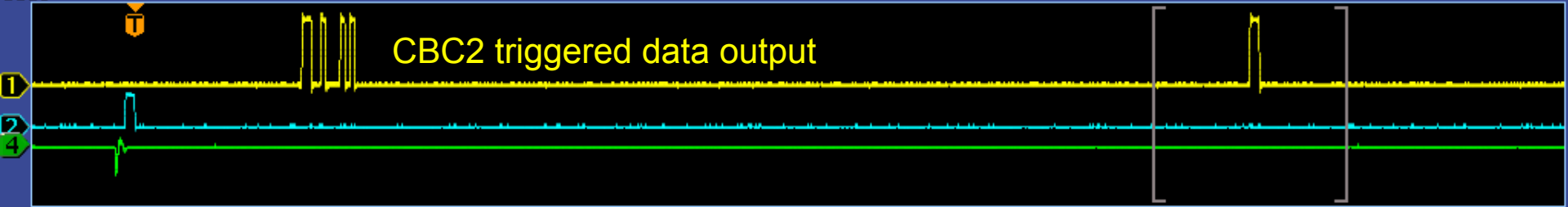




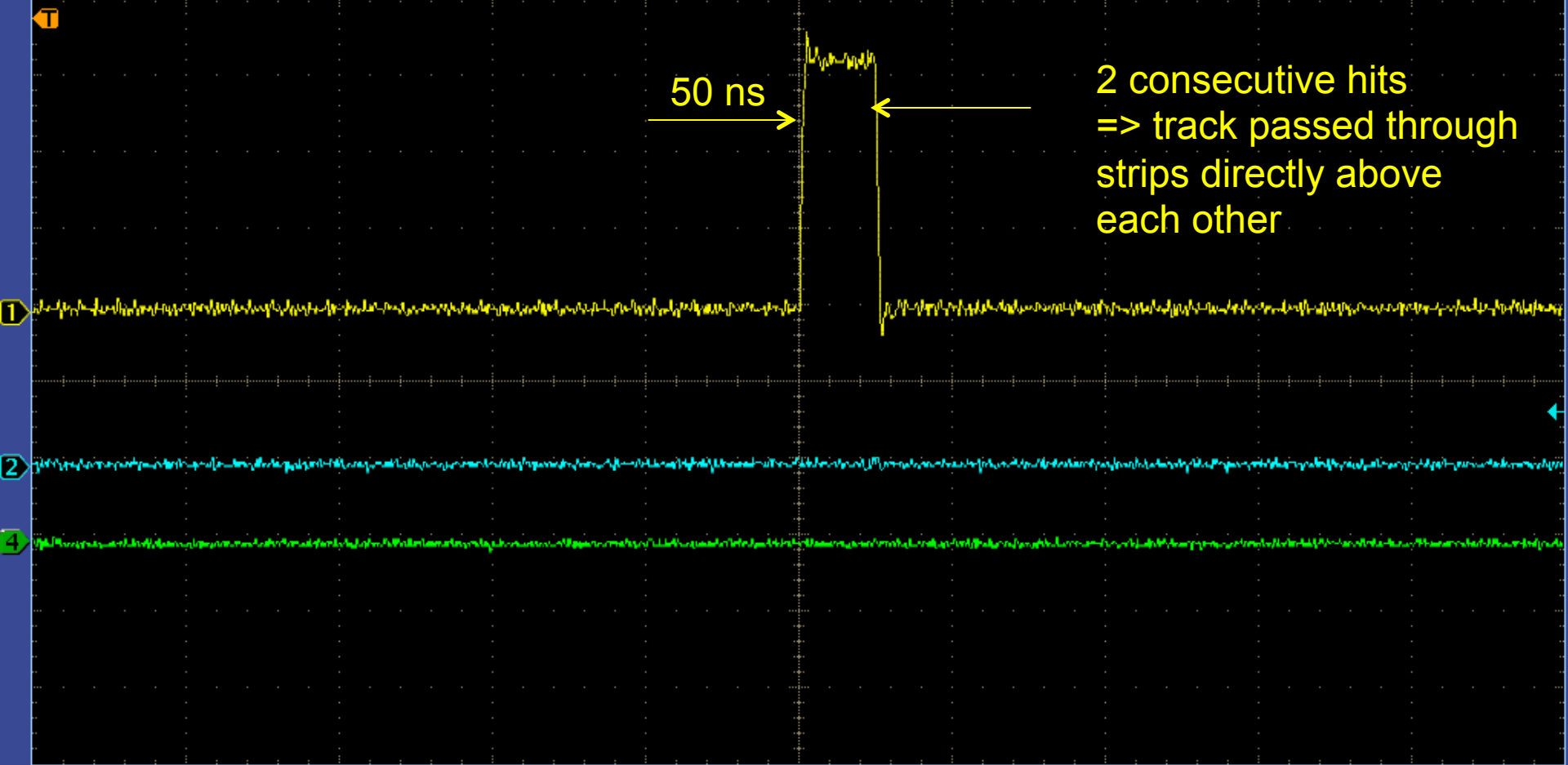
1 1.00 V 2 2.00 V 4 100mV Ω Z 100ns 1.25GS/s 2 \sim 1.44 V

6.700 % 10k points

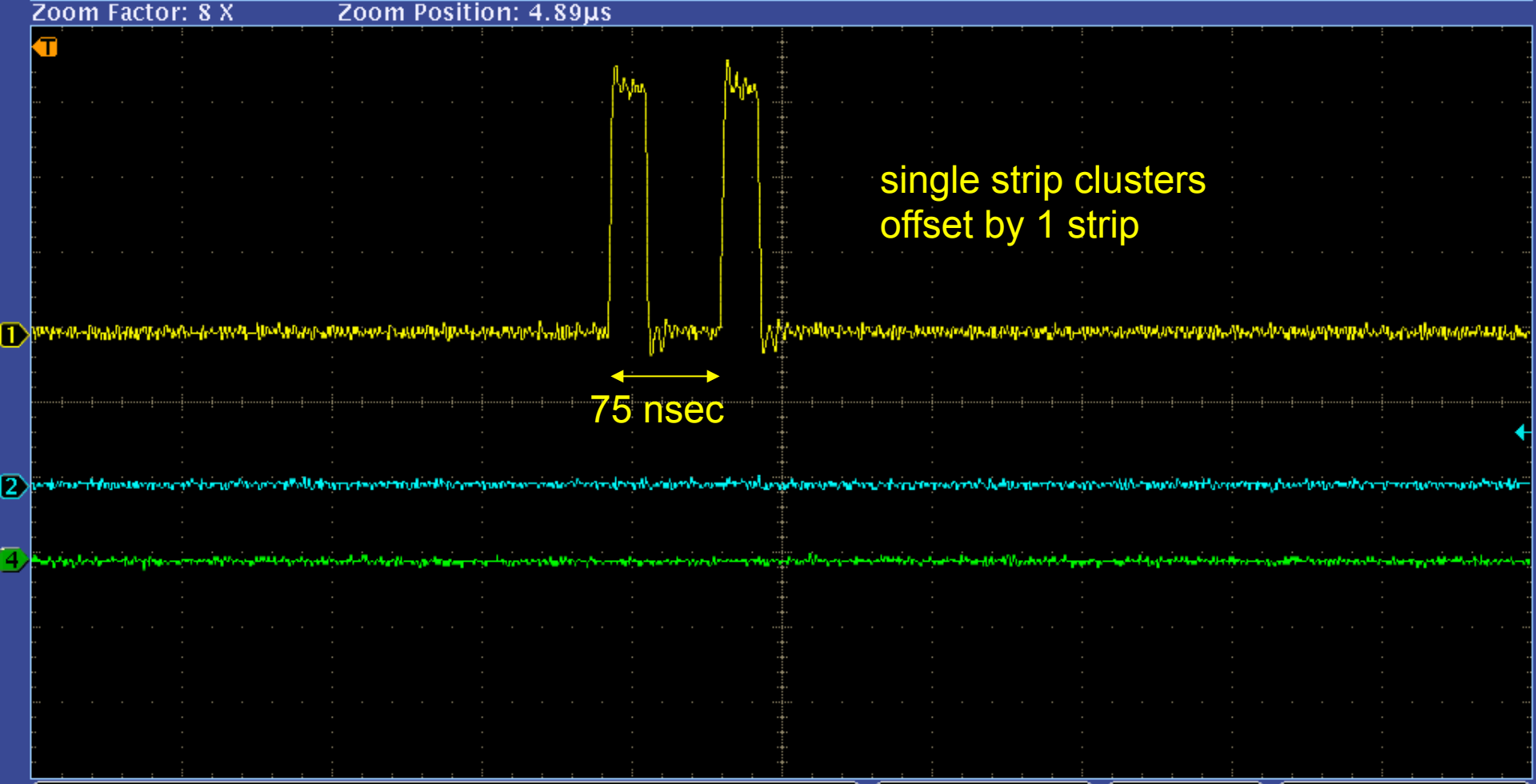
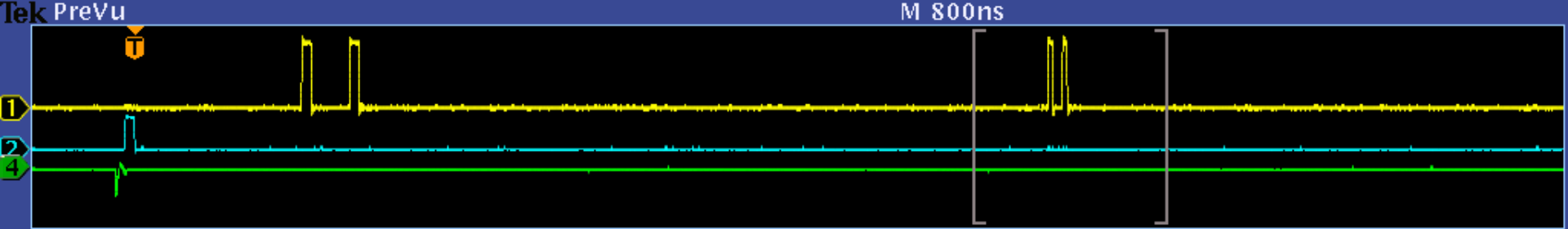
CBC2 triggered data output



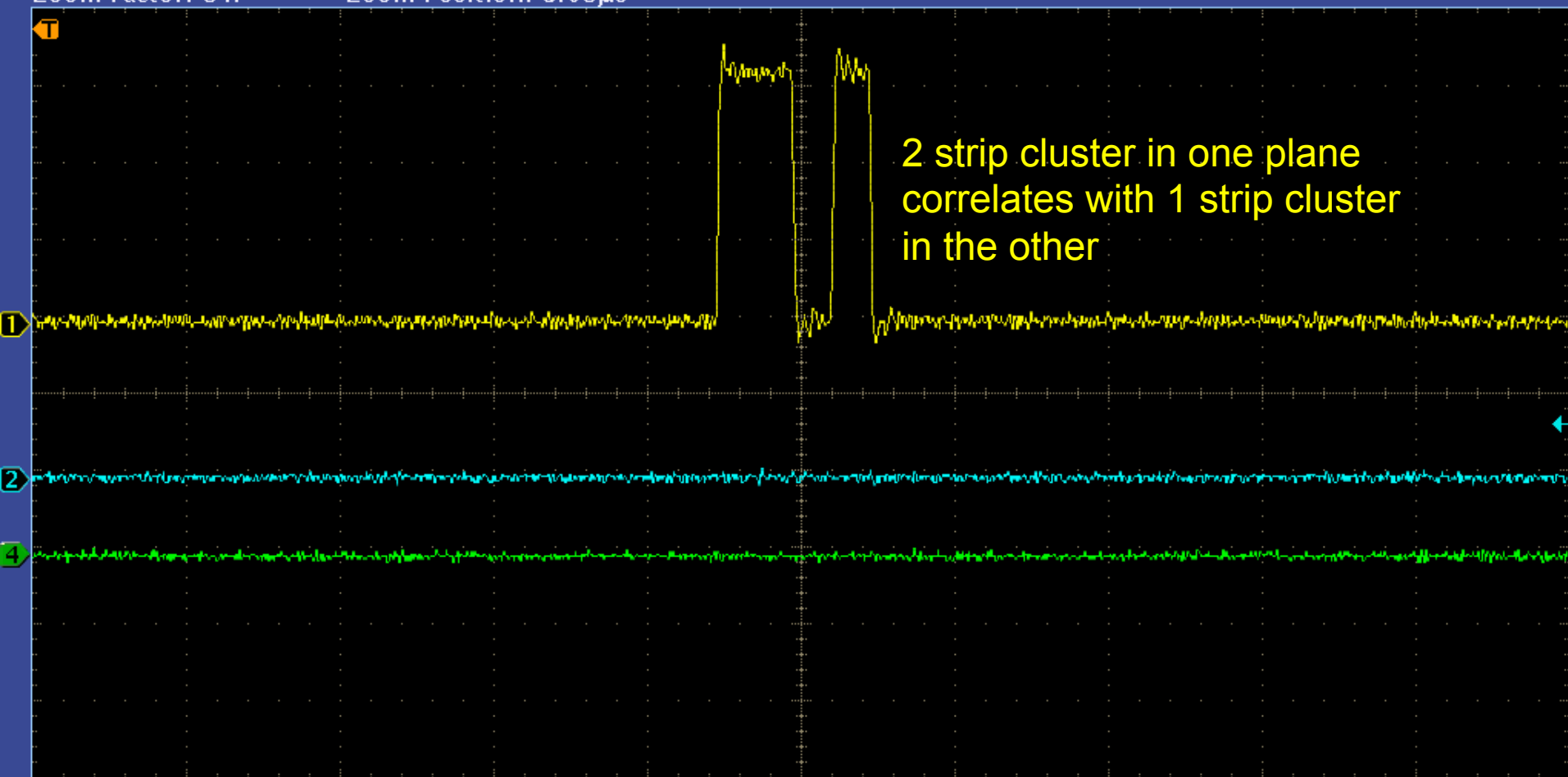
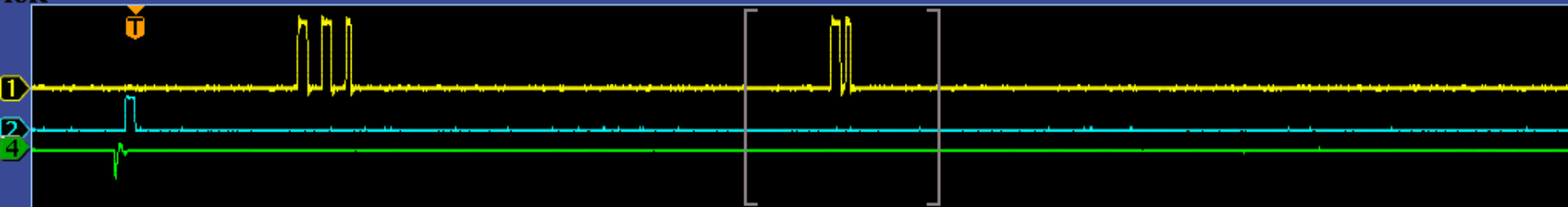
Zoom Factor: 8 X Zoom Position: 5.82μs



1	1.00 V	2	2.00 V	4	100mV Ω	Z	100ns	1.25GS/s	2	1.44 V
						I	6.700 %	10k points		



1 1.00 V 2 2.00 V 4 100mV Ω Z 100ns 1.25GS/s 2 1.44 V
6.700 % 10k points



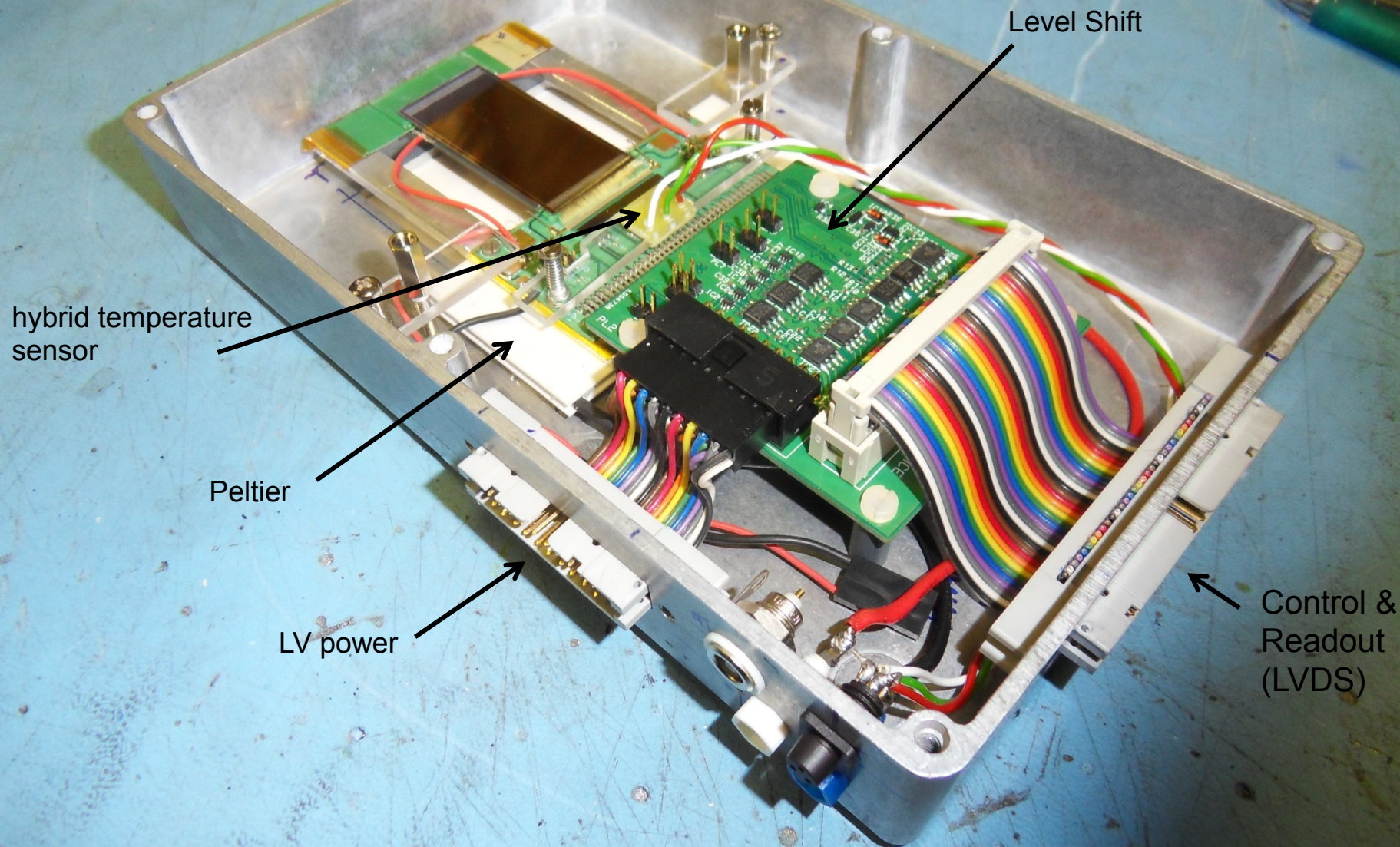
1 1.00 V 2 2.00 V 4 100mV Ω

Z 100ns
I 6.700 %

1.25GS/s
10k points

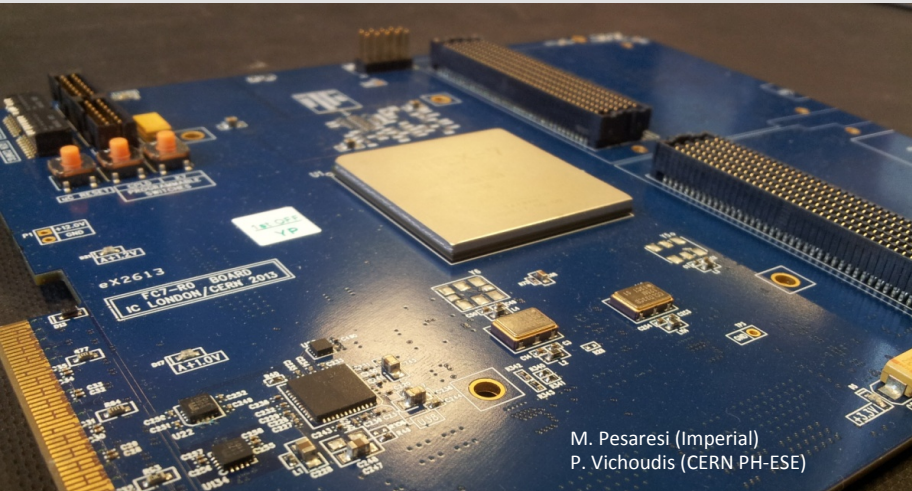
2 \sim 1.44 V

test-beam module



FC7

new generic μ TCA DAQ board



M. Pesaresi (Imperial)
P. Vichoudis (CERN PH-ESE)

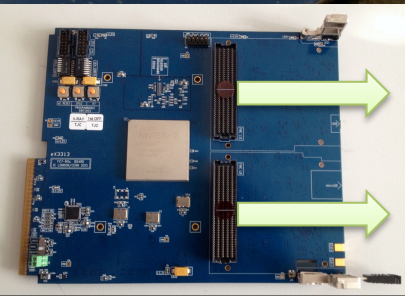
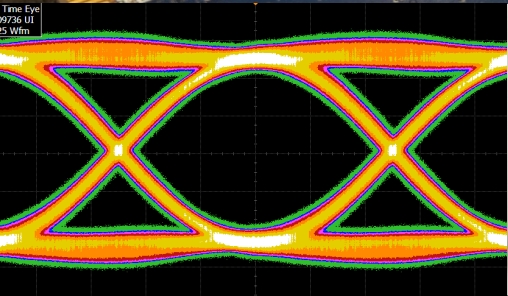
flexible – support two FMC-compatible mezzanine cards accessible from the front panel, compatible with μ TCA and μ TCA for CMS

will replace TTC system in 2014,
pixel FEDs & FECs in 2017;
future DAQ for Phase II proto-CBC modules

status: first prototypes passed initial testing, all serial links running well at 10Gbps, all I/O validated

0.2 Tb/s bandwidth over 20 front panel serial links

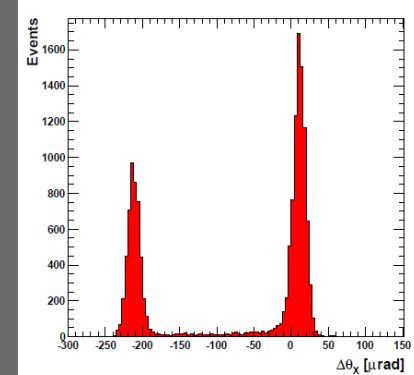
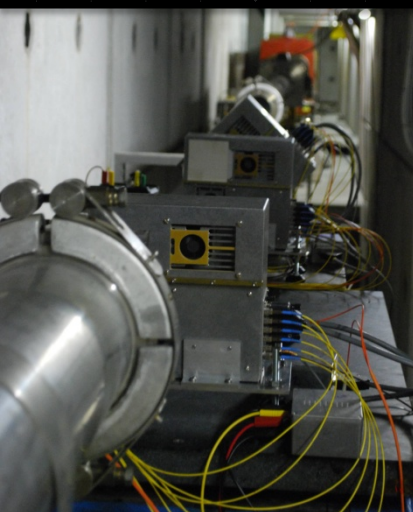
128 front panel user I/O, up to 1.2 Gb/s per pair



CMS upgrades – beam telescope

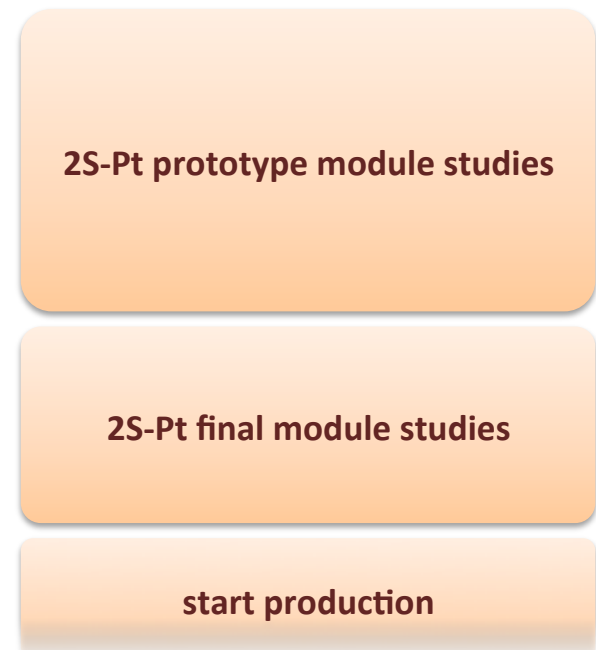
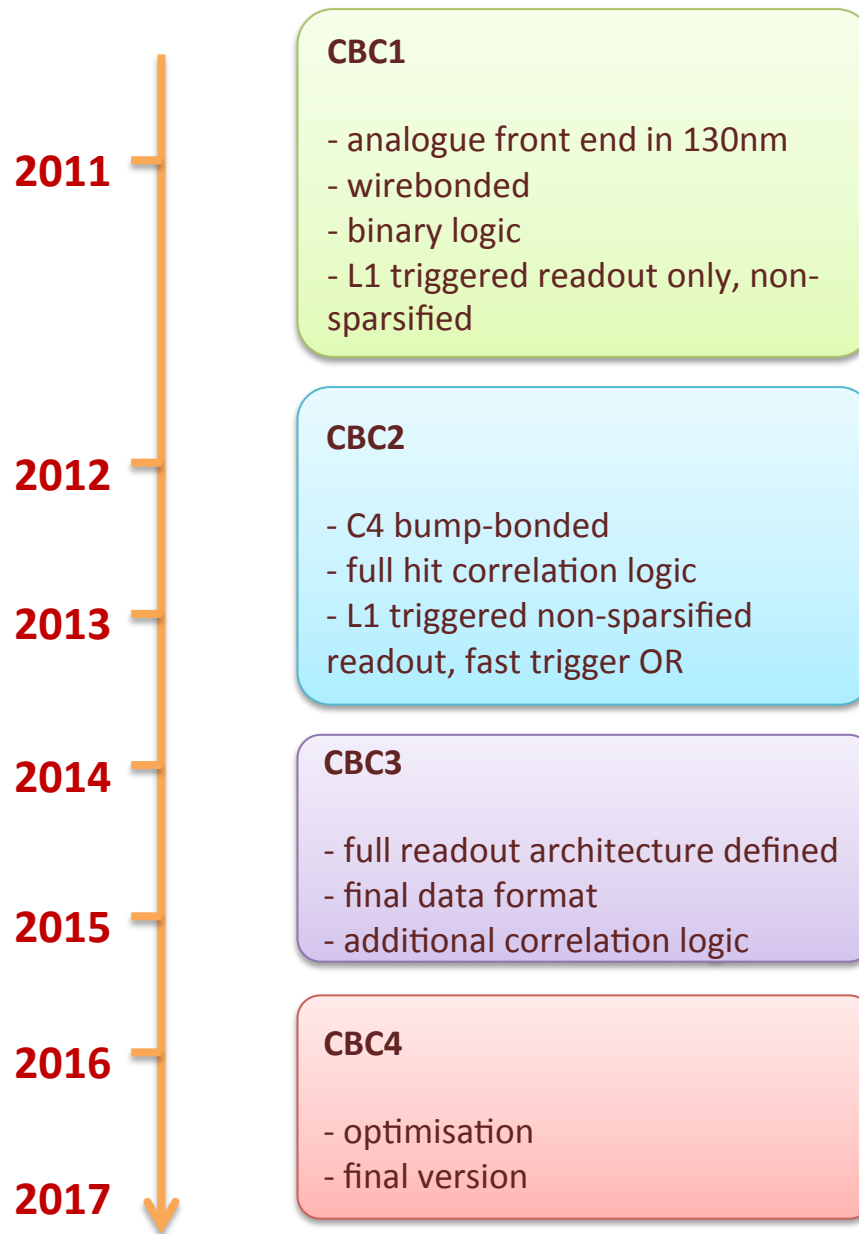
for qualifying CBC ASICs & prototype modules in beam

also used for making precise measurements on performance of next generation LHC collimators



Rough road map

as foreseen in proposal



WP2 planning

- CMS goals based on TP [2014] and Tracker TDR [2016], then construction
- Excellent CBC progress begs some questions:
 - can we rely on this schedule, given planning & funding situation?
 - will be CBC be ready too soon? could the requirements change?
 - will engineering effort be used too soon?
 - can the tracker construction (or TDR) start without proven PS module?
- no urgency at present for CBC3
 - would finalise data format and improve a few details
 - plenty of CBC chips available for modules
 - much to be done in evaluation both module and chip
 - 2S and logic performance
 - SEU and irradiation
- review milestones and objectives in coming months before next OSC

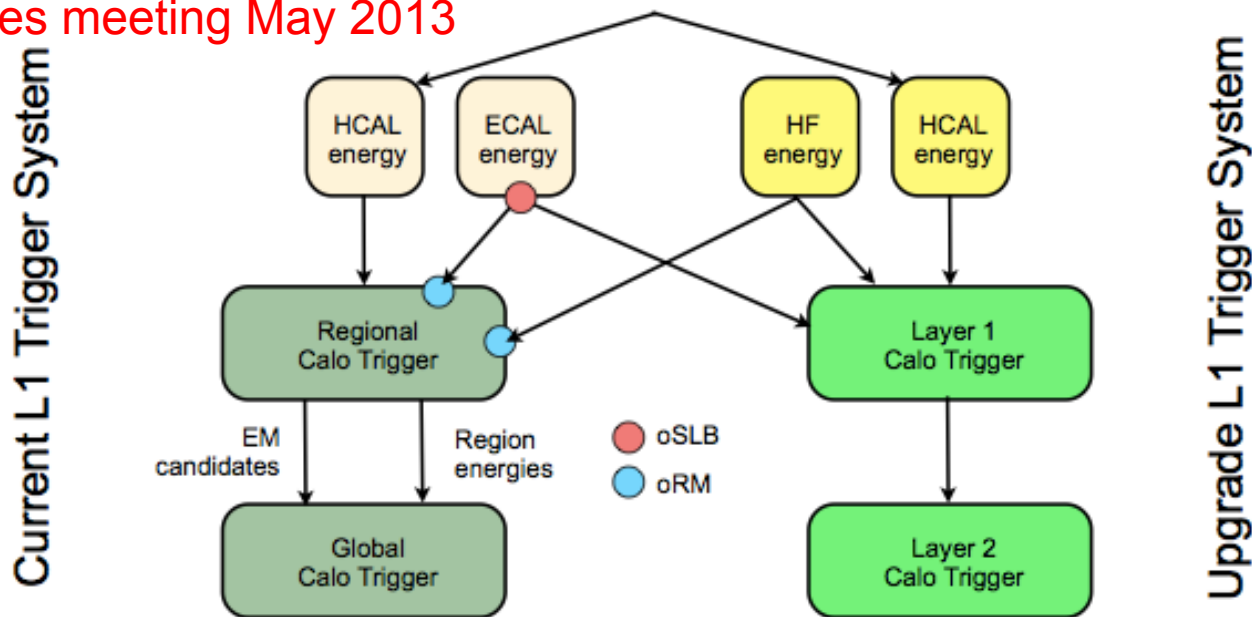
WP3 objectives and status

- Improvement of calorimeter trigger for next running period
 - based on
- Time Multiplexed Trigger (now adopted)
 - commissioning in parallel with operation of existing trigger
- Design of track-trigger for HL-LHC
 - and technology demonstrator
- Recent progress
 - **Very** successful TMT slice test at end September
 - UK hardware used for both Layer 1 & Layer 2
 - A lot learned about firmware & tools
 - Algorithms implemented and latency measured
 - Significant simulation work on future algorithms
 - Several iterations of MP7
 - some fabrication issues which need care, but not show-stoppers



Overview: calorimeter trigger

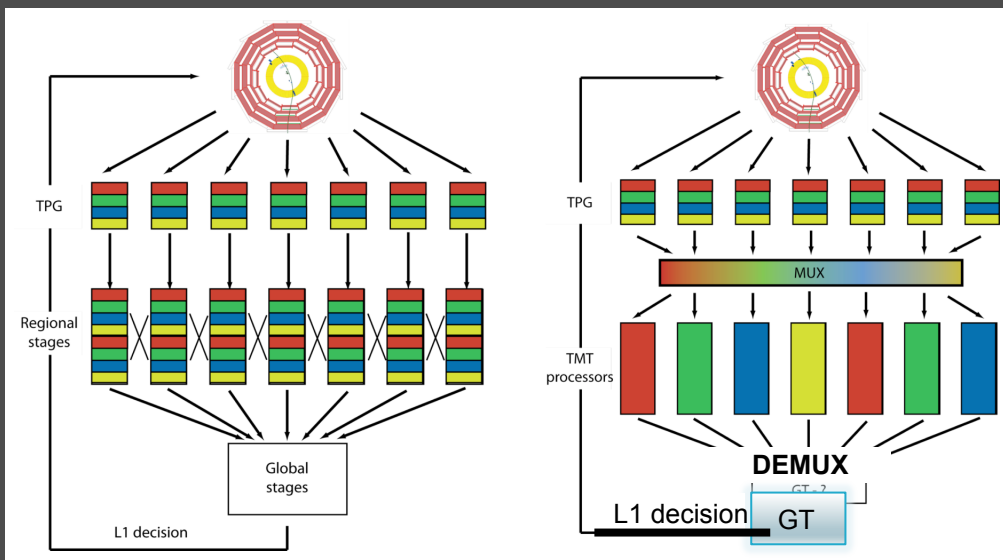
A Tapper
LHCC referees meeting May 2013



- Commissioning of calorimeter trigger in parallel in 2015

- Necessary to install oSLB/oRM during LS1 (complex operation)
- Necessary to install passive optical splitters for HCAL (LS1 and YETS)

Time-multiplexed trigger



Conventional
Trigger

Time-Multiplexed
Trigger

- The Time-multiplexed architecture allows all data to arrive in geometric order:
 - Towers at given φ are always the same bits on the same optical links
 - Towers arrive in order of increasing $|\eta|$
- This converts a 2D geometric problem to a 1D problem
- Also only need to develop 1 FPGA design

- Chosen by CMS as architecture of Phase 1 Trigger upgrade
- Project milestone from TDR to demonstrate working concept in September 2013
- TMT test took place starting 30th September in building 904
- Bristol, Imperial, RAL, LLR involved
- Complete set of results @
- <https://indico.cern.ch/getFile.py/access?contribId=6&sessionId=1&resId=0&materialId=slides&confId=277887>

TMT layout

MP7's used here as PP's, CTP7's to be used in final system

TPG input to PP
not part of test

Test set-up @ 904

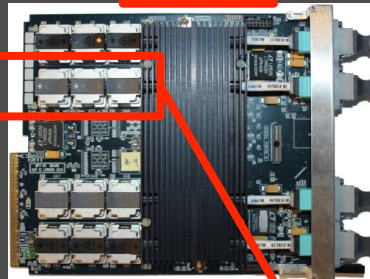
oSLB



uHTR

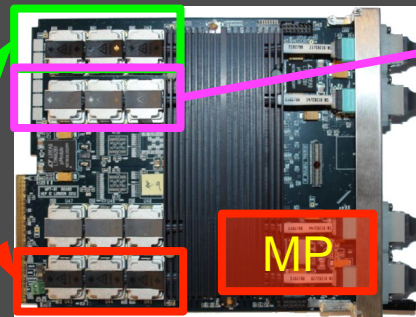


PP-B

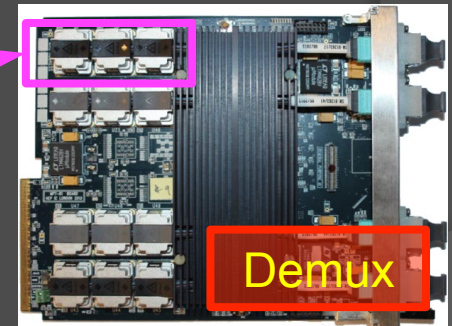


Simulating multiple PP cards with a single MP7

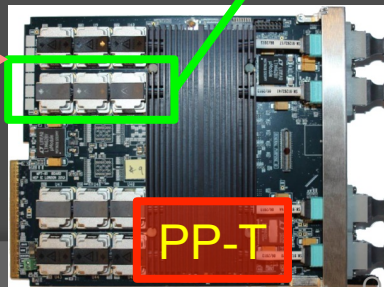
MP



Demux



PP-T



Simulating multiple PP cards with a single MP7

Results compared to objectives - 1

7. Test criteria:

A Pass of the TMT test requires the following objectives to be met:

- Reliable transmission of data @ 10Gbps asynch between PP and MP (36 links with full error checking) - “reliable” to mean running for a series of at least 6 hour runs with zero alignment errors
- Successful alignment of all links

The stability of the MP7 links was extensively tested several times overnight for 8 hours at a time, 72 links operating, monitoring the CRC counters and the alignment flags.

0 CRC errors 0 alignment errors

- Verification of latency and how it compares to TDR value -in particular the SerDes link

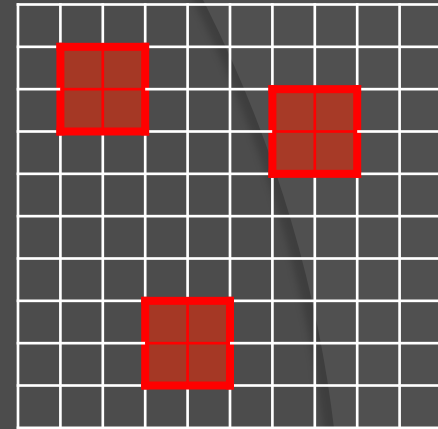
Source of Latency	BX (TDR)	BX - measured in Sept 2013
L1 processing + TM	10	7
L1/L2 SerDes (Tx+Rx) @ 10Gbps	5	5
L1/L2 SerDes Align Data	1	1
L1/L2 cable (20m)	4	4
L2 Processing	8	5.5 (clustering, jets, ring sums)
L2/GT SerDes (Tx+Rx)	5.5	5 (identical link to L1/L2 above)
L2/GT SerDes Align Data	1	1 (identical link to L1/L2 above)
L2/GT cable	0.5	0.5
De-multiplex	6	7
TOTAL	41	36

OSC Nov 2013

Algorithms used in TMT test

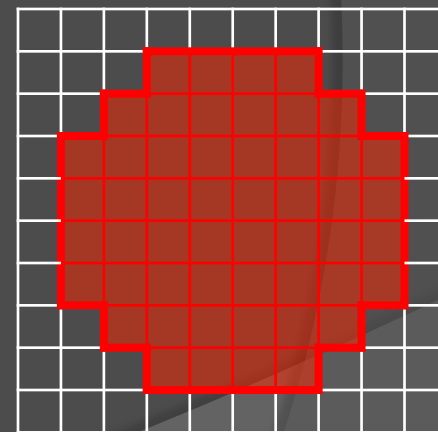
Clusters

- 2x2 clusters
- Overlap filtering and e/ γ / τ identification logic available but not used
- Candidates sorted in ϕ by E_T before output
- Sort in η available but not used to increase statistics for validation



Jets

- 8x8 circular jets (biggest under consideration)
- Candidates sorted in ϕ by E_T before output
- Sort in η available but not used to increase statistics for validation



Sums

- Scalar and vector sum of energy in each ϕ ring of towers
- Number of “towers over threshold” in each ring calculated (potential PU estimator)

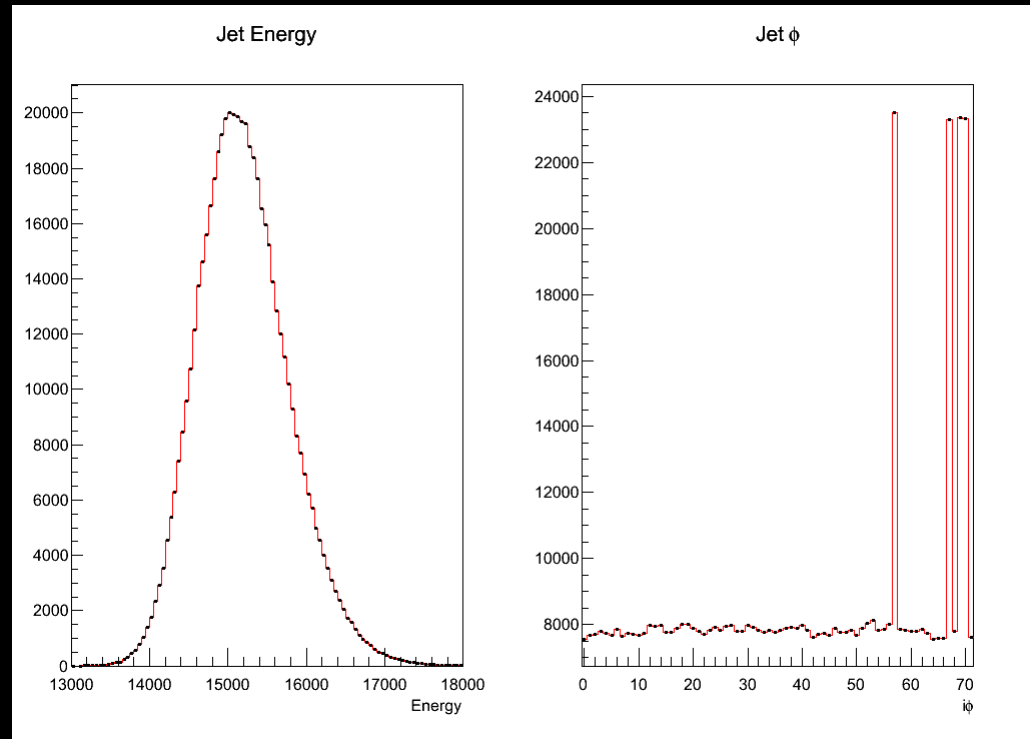
Results (2)

- Implementation of an algorithm and successful transmission of data through it
- Random data passed through an emulator was used in the testing of the algorithms



Compared emulated results with those from the MP7

Emulator and hardware match precisely



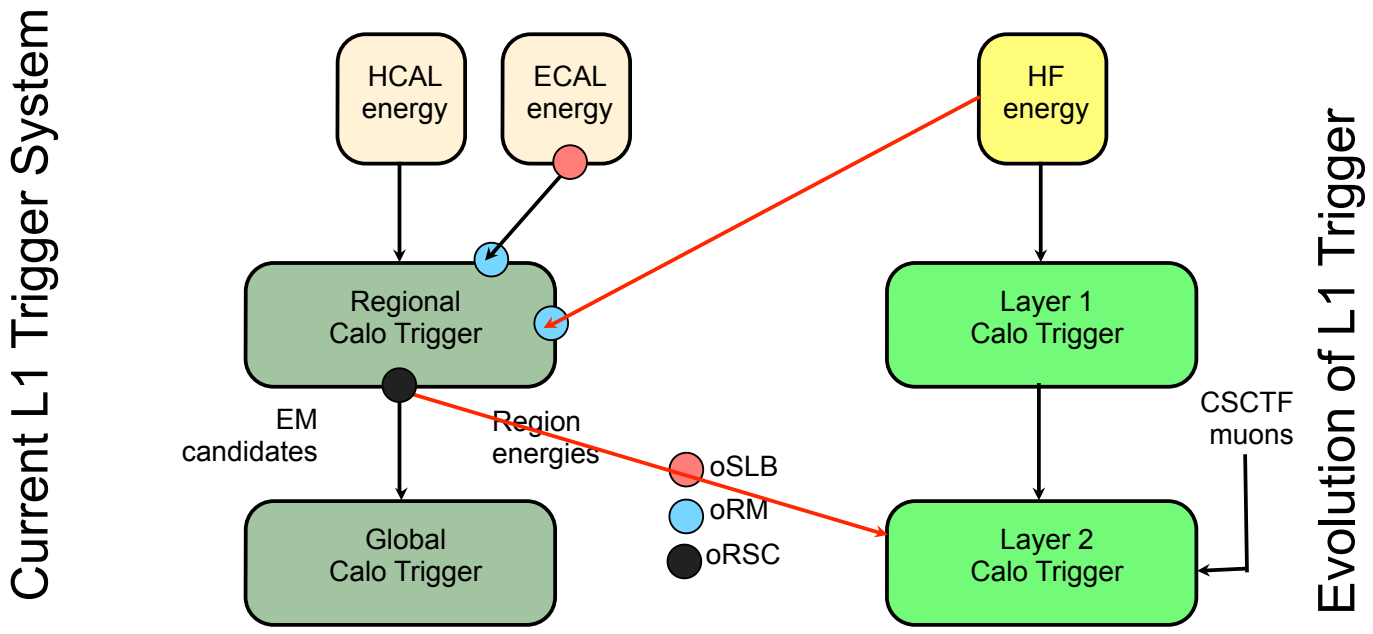
WP3 planning

- Issues for calorimeter trigger
 - US readiness & funding
 - CTP7 for Layer 1 is only at layout stage (just gone to fabrication)
 - Planning for 2015
 - US proposed short term interim upgrade but all aspects of development (hardware, firmware, software) are late and behind full upgrade planning
 - oSLB and oRMs installation in LS1 is crucial for full upgrade
- EDR 12 & 13 November
 - propose revision of planning when outcome is known
- Discussions started for HL-LHC Track-trigger planning
 - in Tracker community. MP7/TMT are promising test-bed



Intermediate trigger - 2015

- Limited to use current RCT and current GT



- Significant performance improvements possible in $e\gamma$, τ and jets
- Prototype processor cards and (new) oRSC cards to duplicate signals
- Retains data to legacy GCT for easy rollback with just reconfiguration

Finances

- All RA posts now filled
- Expenditure as expected
 - continuing orders of MP7 and FC7 prototypes
 - μ TCA hardware
 - materials for 2S-modules and beam test
- Looking for OSC feedback on
 - financial table format
 - how to include CG grant spending
 - milestone reporting
 - risk register

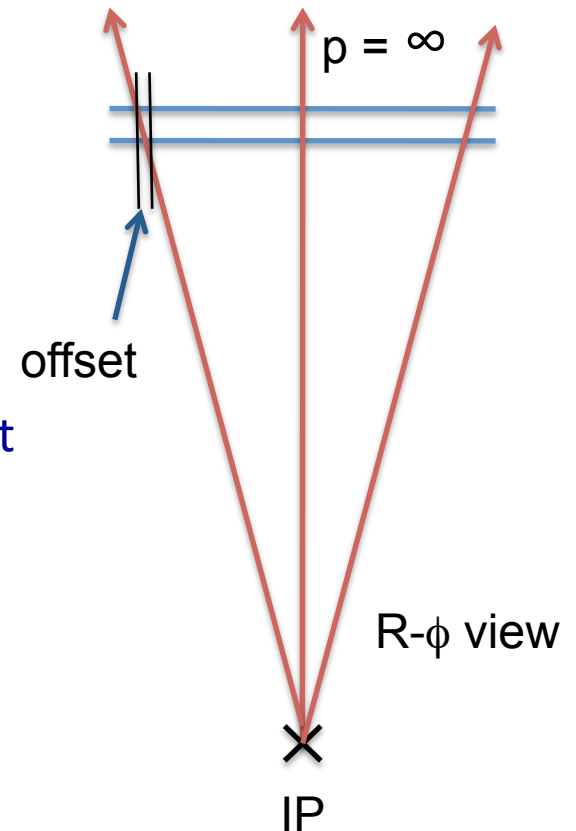
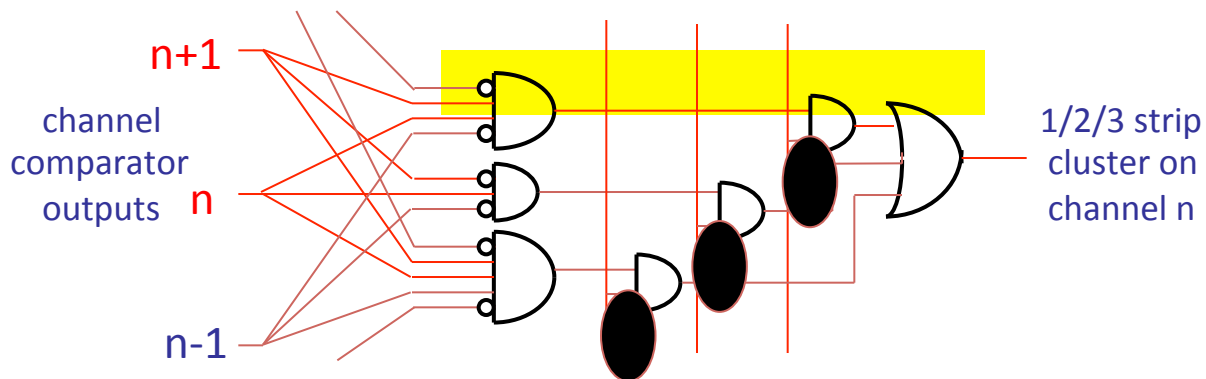
Conclusions

- The next phase of the project is well on track
 - continued good progress
- Main issues concern adaptation to LHC schedule
 - it is unlikely that there will be much new information about long term schedule and planning very soon
 - perhaps at next RRB?
- Propose revision of milestones within next six months
 - expect feedback from trigger EDR and possible strategic decisions
 - evaluate options for Phase II tracker developments

Further information

Stub logic features

- Cluster width
 - exclude clusters wider than 3 strips
- Offset correction and correlation
 - programmable window, selects pT
 - up to ± 8 channels
 - programmable offset, adjust lateral displacement
 - up to ± 3 channels



analogue front end amplifier

- re-examine pulse shape for dead-time issue
 - maybe postamp feedback resistor tweak necessary
- check optimum input transistor dimensions for 5 cm strips
 - 5 pF was original target
- try and adjust for 1.0 V operation
 - can't guarantee success

slow ADC?

- with "band-gap accuracy" can at least get an accurate value for the voltage biases
 - probably useful but is it worth it?
 - probably not if have to develop from scratch

comparator

- 2 comparators/channel? 5 sigma and 3 sigma thresholds?
 - (1 chan > 5σ) OR (2 neighbours > 3σ) => hit
 - some issues of what to do with comparator outputs
 - 5/3 sigma pipeline, or 2x pipeline
 - what to do with 5 sigma neighbouring 3 sigma (different combinations)
 - more signals to cross chip boundaries?
- likely extra 50 uW / channel

biases

- linear enough? monotonic enough? enough resolution?

hit detect

- keep existing circuit but plan to run in variable mode only
- then need additional circuit to suppress hips - if comparator output high for longer than 3 BXs (4 BXs?)

mask to pipeline

- needed somewhere if moving to sparsified system, not necessarily on CBC but probably best place can be separate to mask for correlation logic

pipeline

- length increase to 25 usec or thereabouts
- issues of SEU and ionizing sensitivity (if minimum size devices)

trigger rate capability to 1 MHz

output data format

- how many lines at what rate?, differential/single-ended? - baseline 12 lines @ 160 Mbps

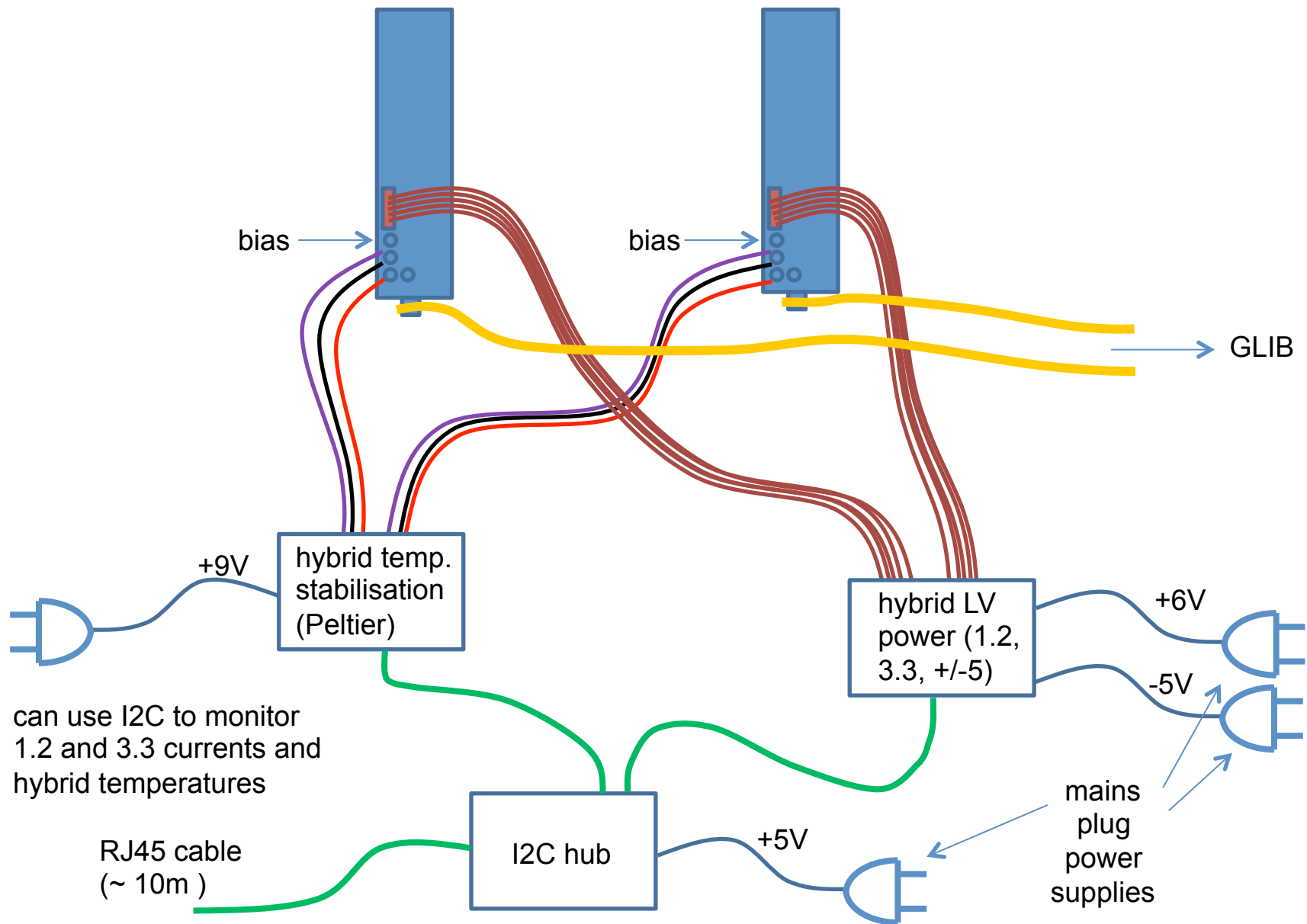
offset correction

- 4 domains / chip (only 2 in CBC2)

correlation

- +/- 8 channels, $\frac{1}{2}$ strip resolution => 8 bit address
- 5 bit bend information
- priority encoding of highest 3 pT stubs (Mephisto)

module test-beam system



CBC3 - the "final prototype"

next version of chip should incorporate all features required for HL-LHC

- **final choices for front end**

- 1/2 strip cluster resolution
- 2 strip cluster position assigned to mid-point

- **stub data definition**

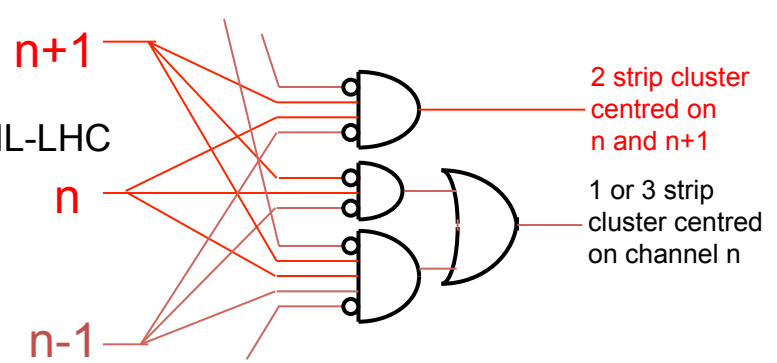
- 8 bits address (for 1/2 strip resolution) of cluster in bottom layer
- 5 bit bend information
- address of correlating cluster in top layer

- **stub data formatting & transmission to concentrator**

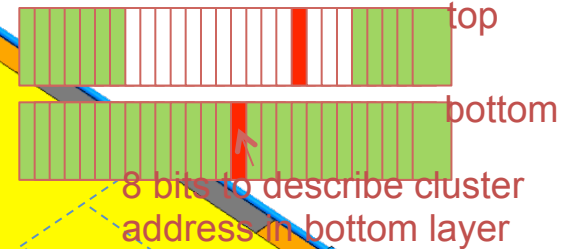
- 13 bit / stub, up to 3 stubs/BX => 39 bits
- +1 bit unparsified L1 triggered readout data
- => 40 bits / 25 nsec
- e.g. 10 lines at 160 Mbps. (per chip)

- **other useful features**

- e.g. slow ADC to monitor bias levels
- ...



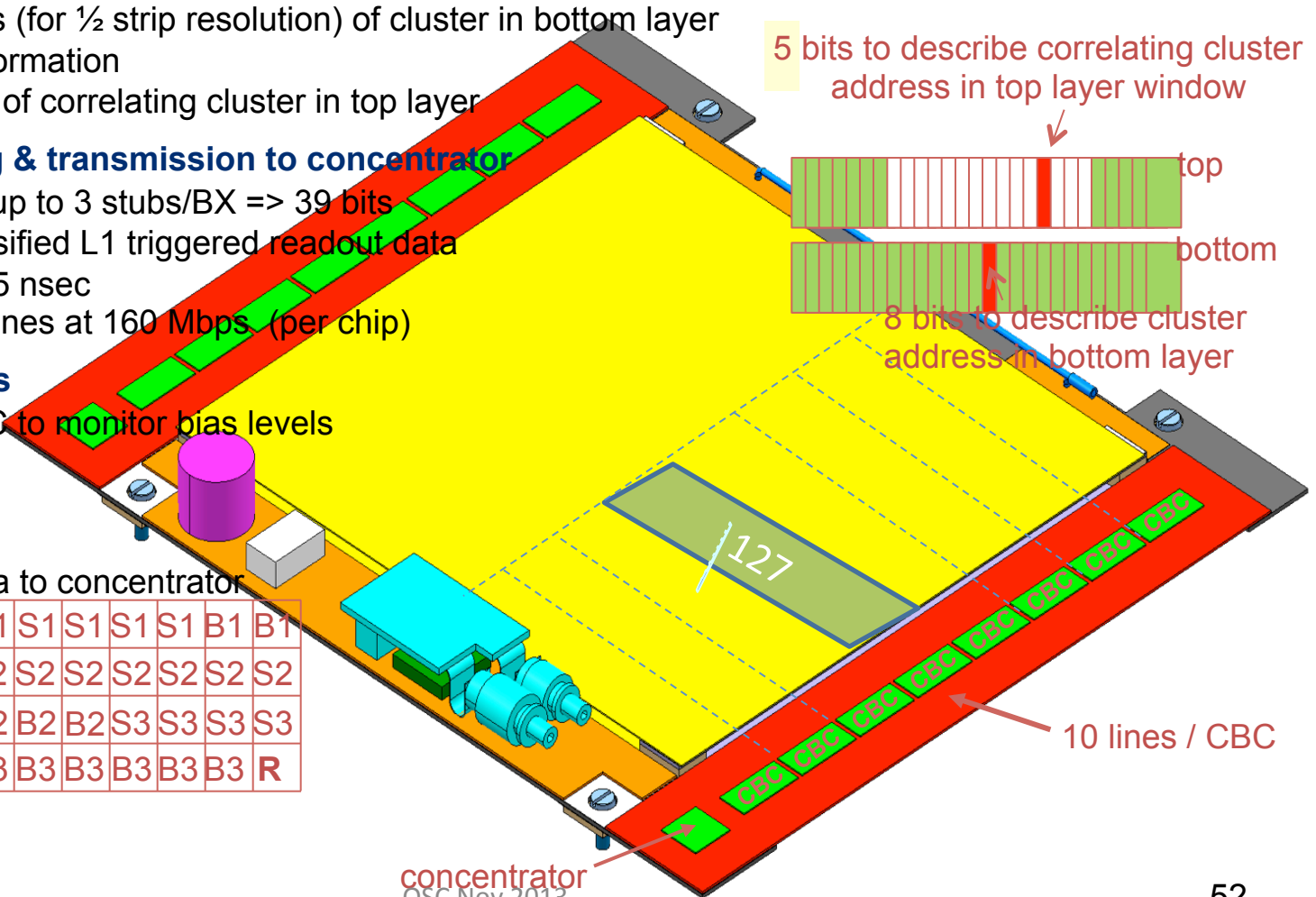
5 bits to describe correlating cluster address in top layer window



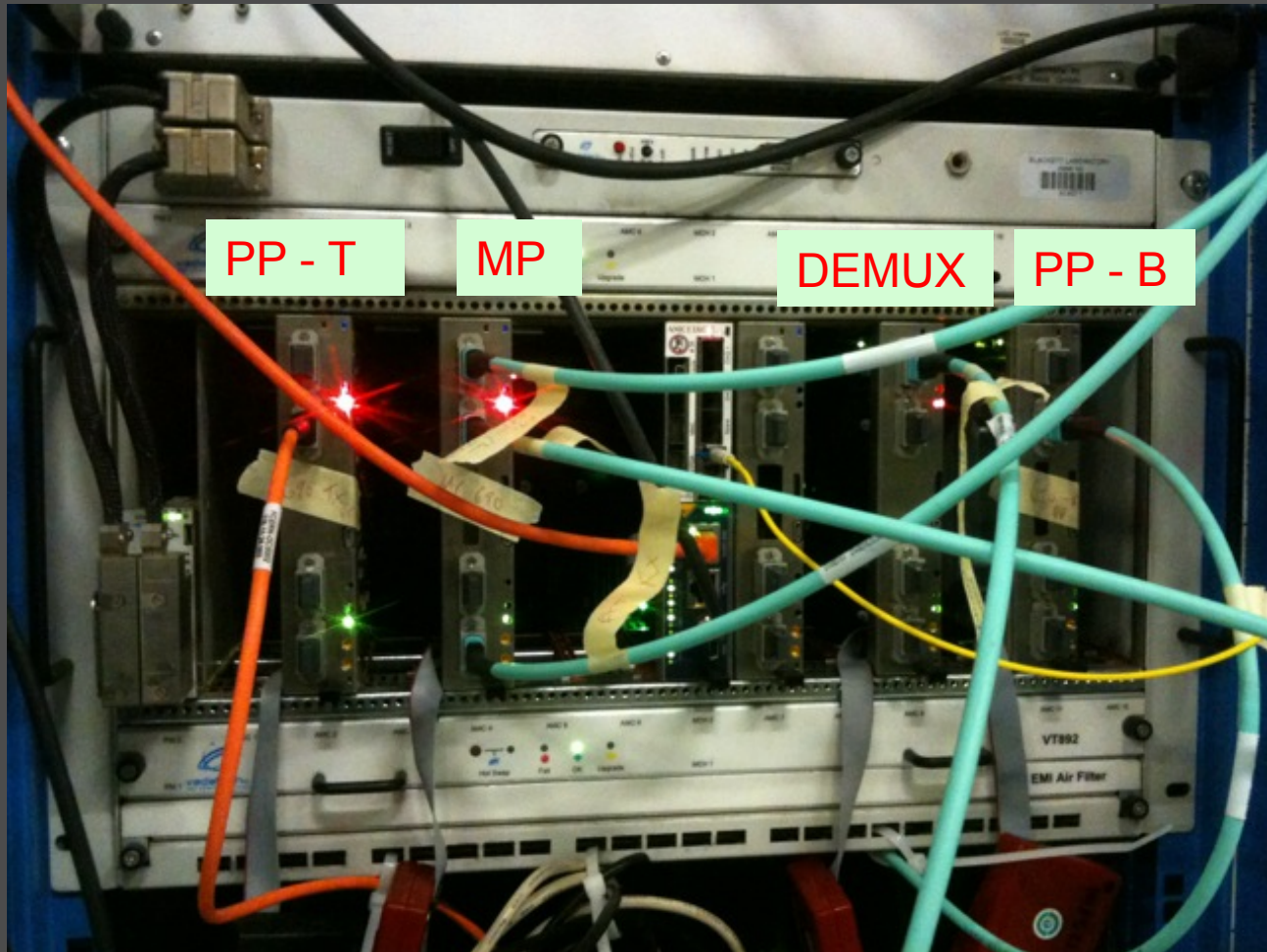
CBC data to concentrator

S1	S1	S1	S1	S1	S1	S1	S1	B1	B1
B1	B1	B1	S2	S2	S2	S2	S2	S2	S2
S2	B2	B2	B2	B2	B2	S3	S3	S3	S3
S3	S3	S3	S3	B3	B3	B3	B3	B3	R

25 ns



TMT-test setup @ 904



- 720 Gbps of data going through the MP board
- The MP is processing data from the entire calorimeter

Floorplan of FPGA

DAQ

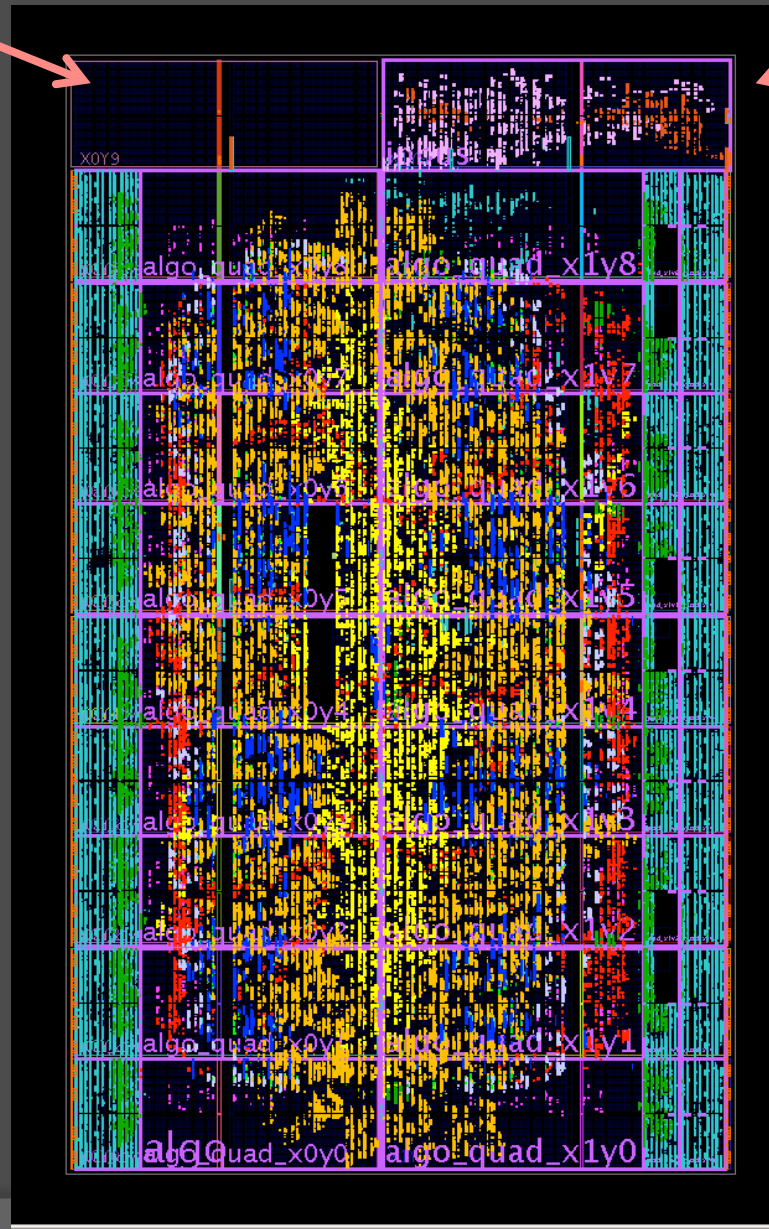
Communication

Algorithms

- Clusters
- Towers
- Jets
- Sorting

Infrastructure

- MGT's
- Buffers



Resource usage of FPGA

Entire FPGA

	Infrastructure	Algo + Infrastructure	
Registers	9%	21%	
LUTs	19%	36%	
DSPs	0%	8%	
BRAM	12%	12%	

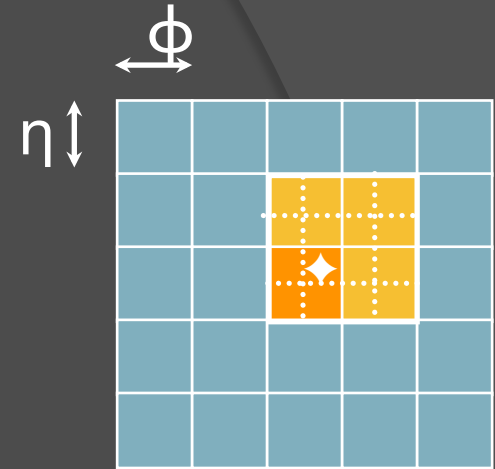
All Algos and Infrastructure
: 7 hour
build-time

Algo area only

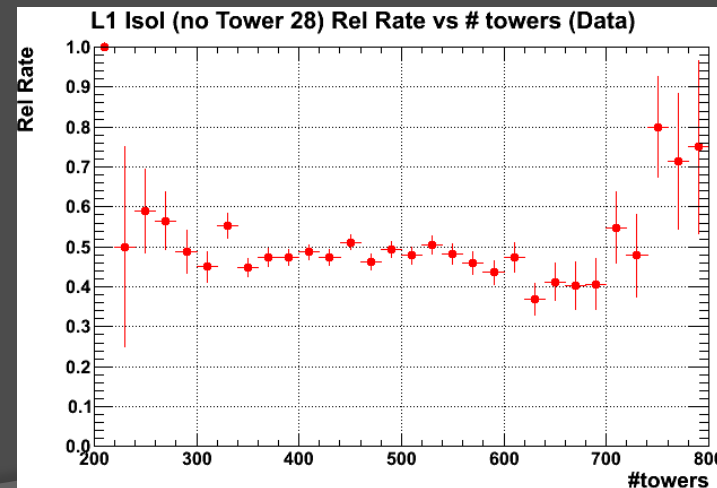
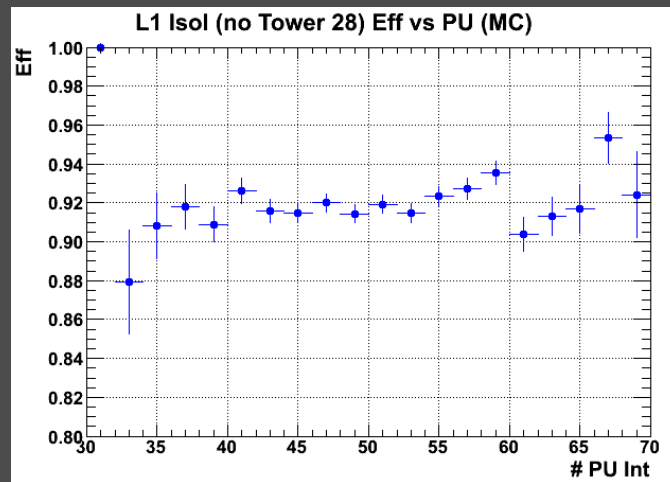
	Infrastructure	
Registers	20%	
LUTs	35%	
DSPs	13%	
BRAM	0%	

E/gamma Algorithm

- Baseline Stage 2 EG algorithm :
 - **2x2 Trigger Tower clusters**
 - Cluster position reported to $\frac{1}{2}$ tower precision
 - Default isolation region : $5\eta \times 9\phi$ towers
- Current focus on PU subtraction for isolation
 - **Need to estimate the 90% percentile of PU E_T distribution**
 - # towers over threshold shown to work well (below)
 - Currently evaluating a range of other algorithms



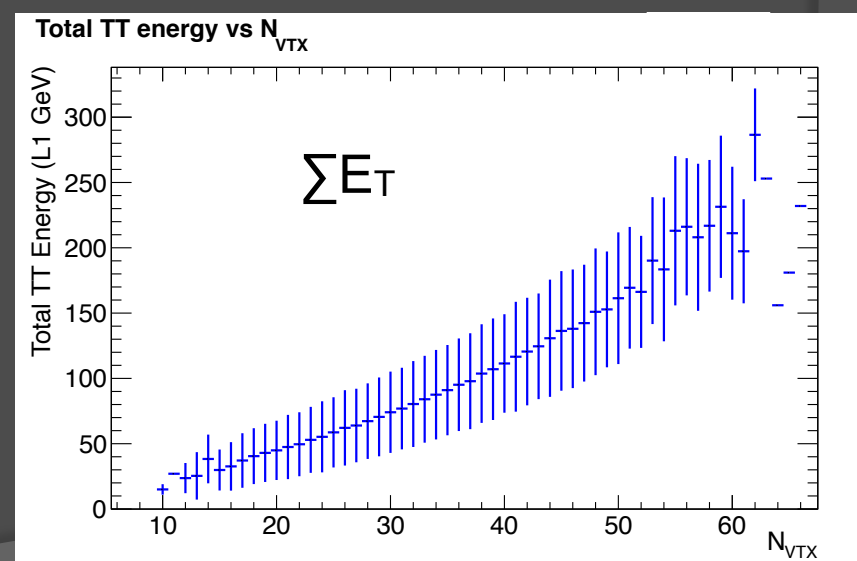
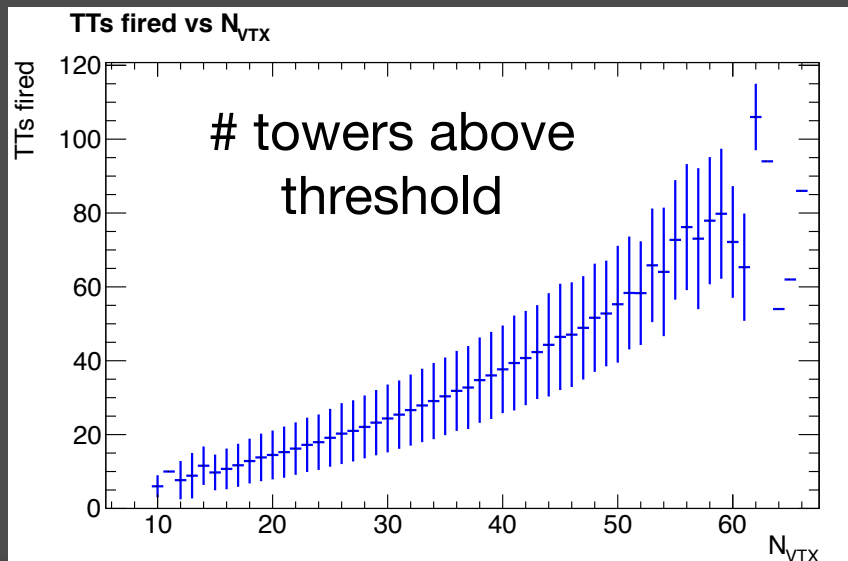
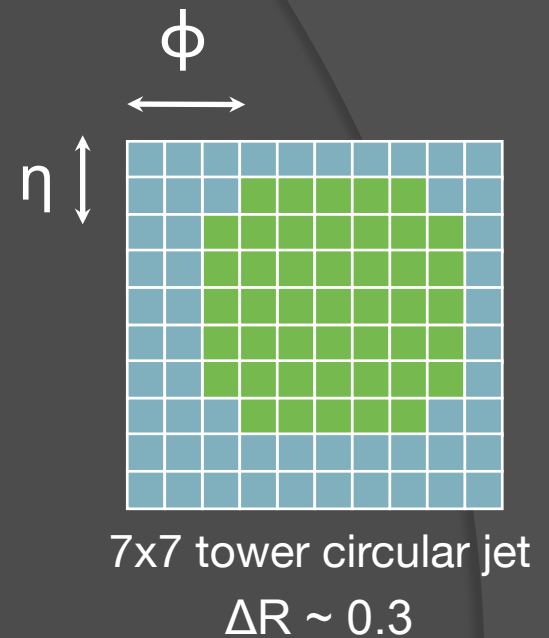
$\Delta R \sim 0.18$



Efficiency & rate stable with PU using # towers as estimator

Jet Algorithm

- Baseline stage 2 jet algorithm :
 - **$N \times N$ tower circular jets (up to 8×8)**
 - Approximates a fixed cone algorithm
- As for EG, current focus is PU subtraction
 - **Need to determine mean E_T of PU distribution**
 - EG/jets may need different PU estimation methods
 - Range of algorithms under study
 - **Expect to choose baseline algorithm soon**



Performance of different estimators for N_{vtx}