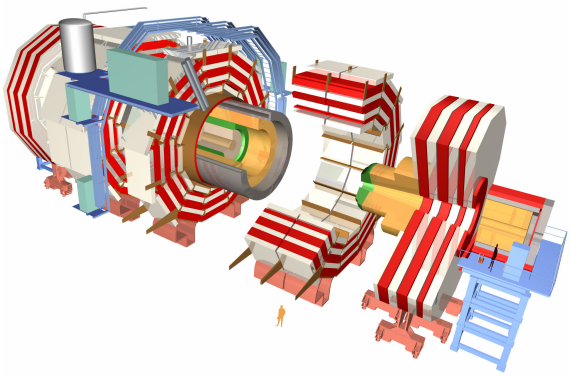
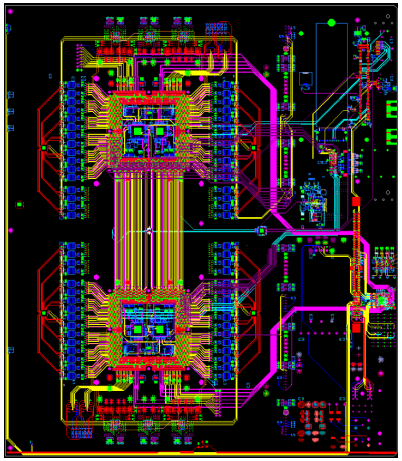
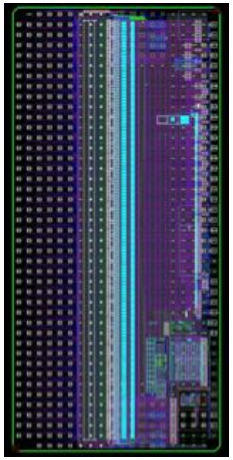




UK CMS Upgrade Oversight Committee

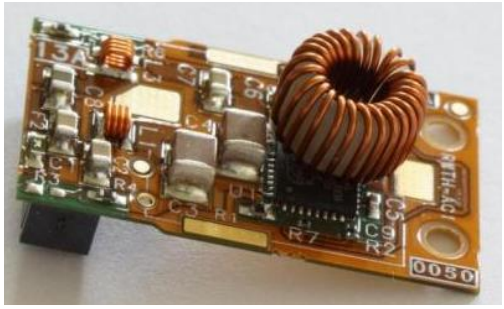
13 November 2017



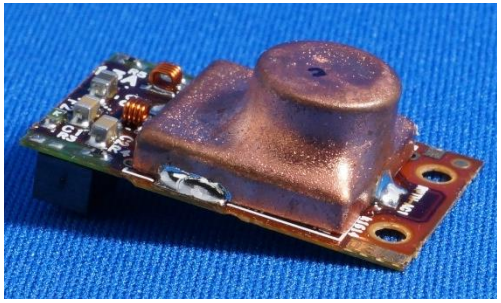
University of Bristol
Brunel University London
Imperial College London
Rutherford Appleton Laboratory

Overview

- Snapshots of LHC & CMS status
  - LHC has delivered (30 Oct) its 45 fb^{-1} p-p target for 2017 (and ~3μb^{-1} Xe-Xe)
    - Some minor problems resulting in special operation modes which increased pileup
    - CMS pixels commissioned, and some operational problems overcome
    - Recently a new pixel problem of failing DC-DC converters



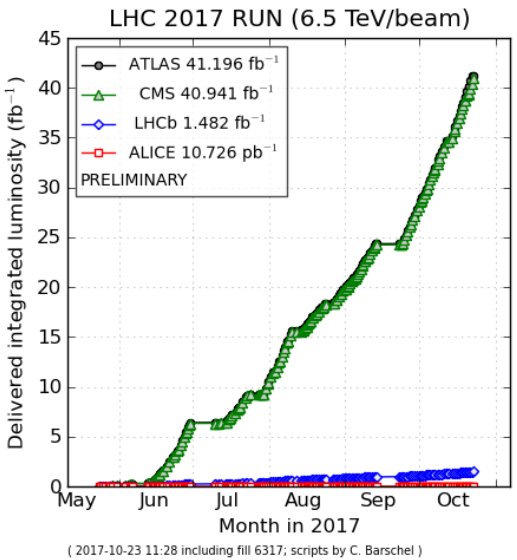
- Summary of UK upgrade project
  - Steady WP progress
- UK CMS Construction project proposal submitted to PPRP
  - PPRP meeting 24 January

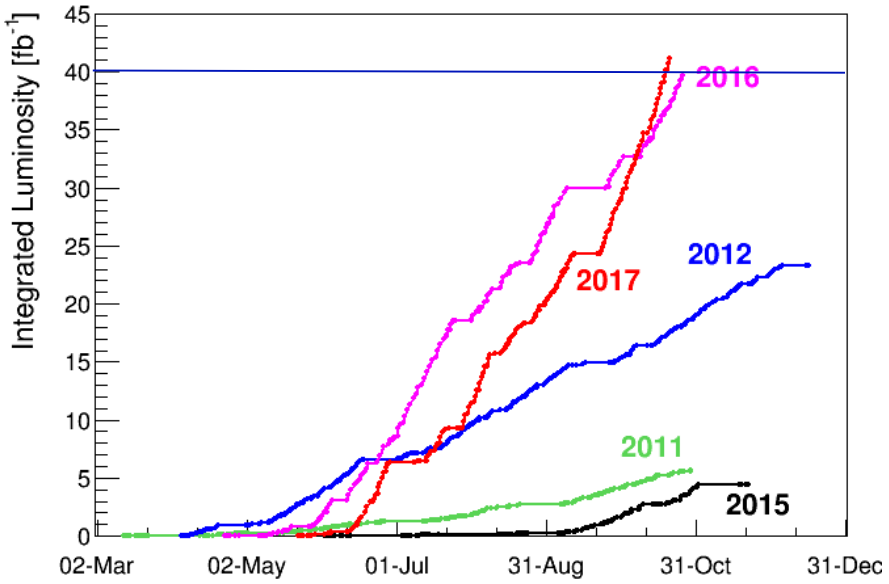


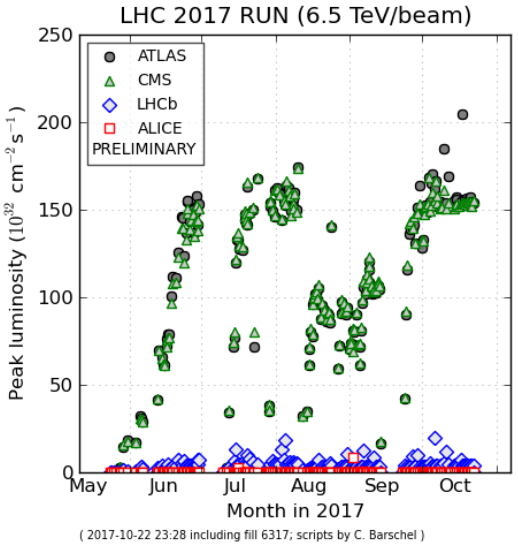
- Matters arising from last OSC

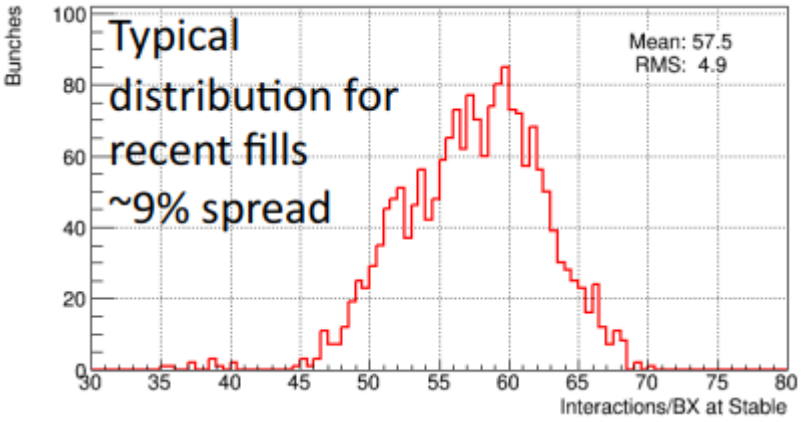
LHC 2017 : Integrated Performance (up to 23rd October)

> 41 fb^{-1}

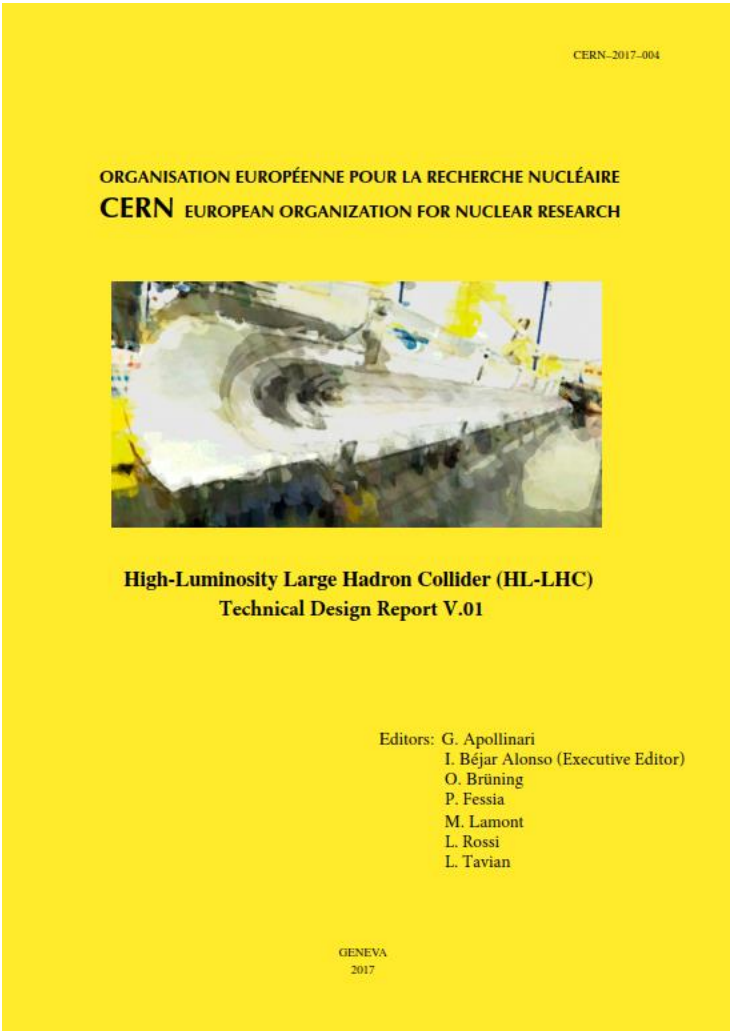








HL-LHC: TDR V0.1 (TDR V0, August 2016)



Printable Version on EDMS 183344 (565 pages)

https://edms.cern.ch/ui/file/1833445/0.1/HL-LHC_TDR_V.01.2017.08.04.h18.030.pdf

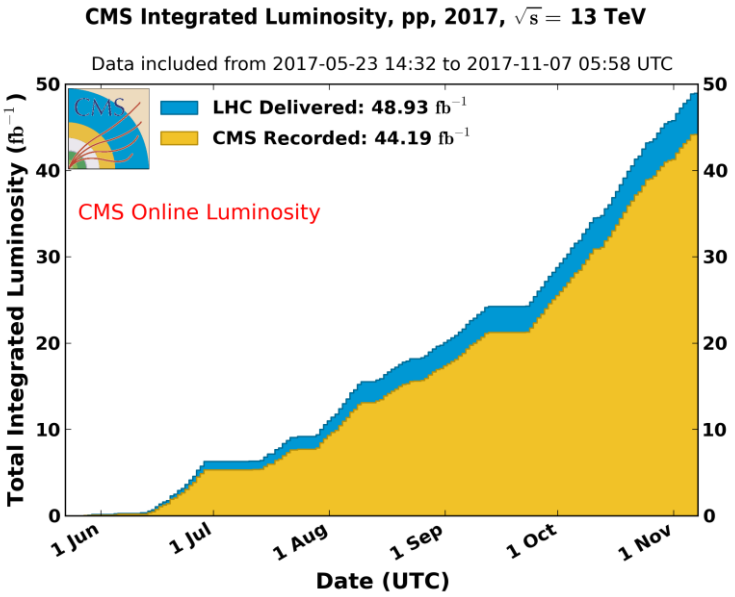
TDR V1 after the Cost &Schedule Review (March 2018).

CMS operations 2017

- After initial reduced efficiency during new pixel detector commissioning, CMS achieved good overall efficiency
  - despite operating with high pileup, $L_{inst} > 1.5\ 10^{34}\ cm^{-2}s^{-1}$
    - trigger performance very satisfactory
  - SEU issues in pixel TBM ASIC required regular power cycling
- However, starting 5 October a new problem in the pixel detector emerged
  - failing DC-DC converters, apparently linked to power resets
    - 1 Nov: 38 DC-DC converters had failed (3.2%) affecting ~6% modules
  - despite intensive investigation, problem is not yet understood
    - tracker task force, and technical incident panel
  - CMS requested one week earlier end to LHC operation to access the detector

- Important not just for operations but because DC-DC converters widely used in all Phase II upgraded LHC experiments

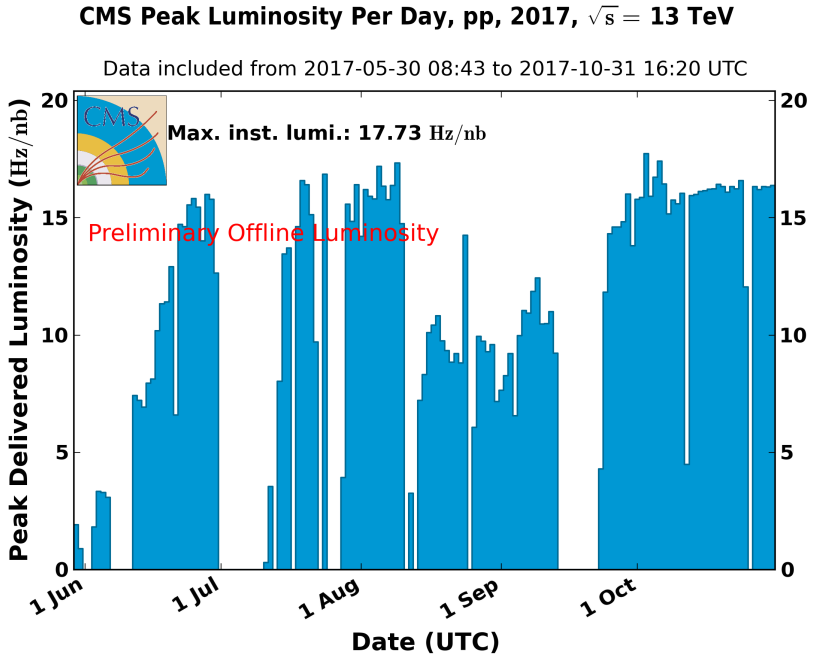
CMS data taking



About 49 fb^{-1} delivered in 2017

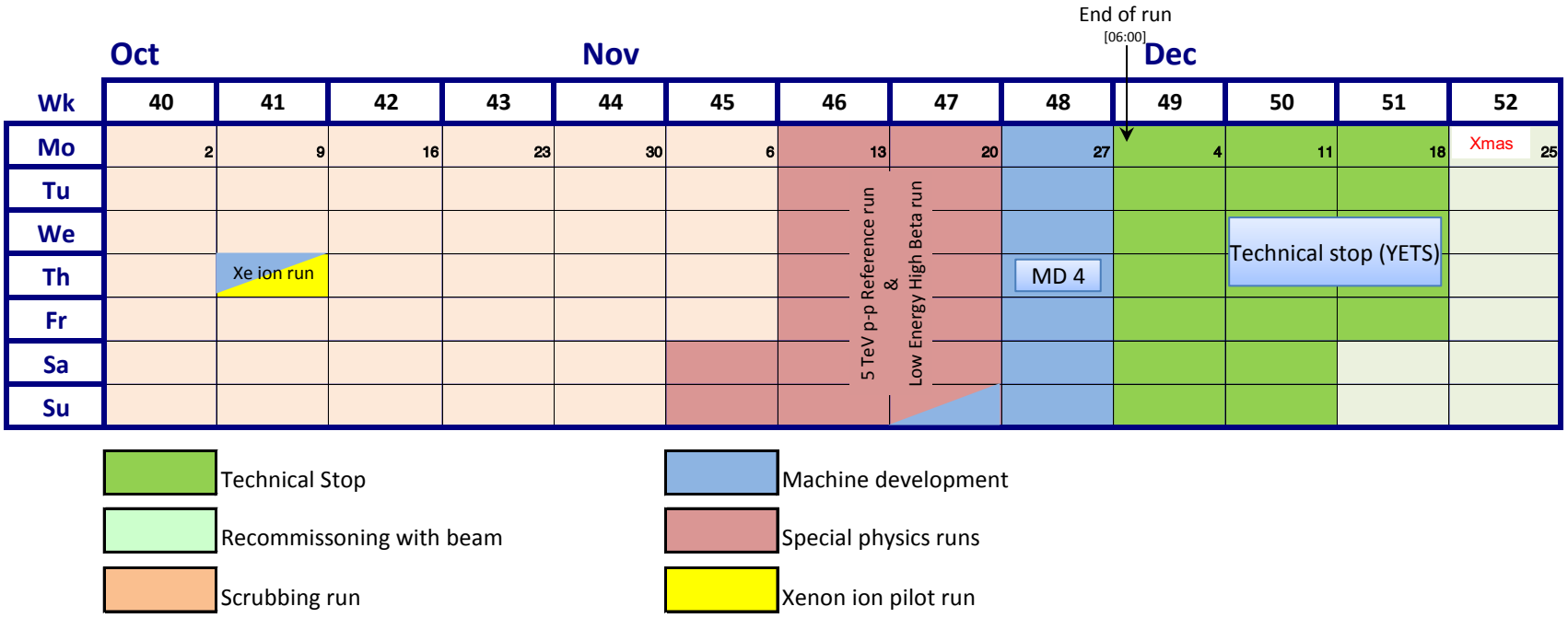
- Total recording efficiency just above 90%
- Compared to 92% in 2016, corresponds to having lost 1 fb^{-1}, at the end a small

- Last week about 3.2 fb^{-1} delivered
- Recording efficiency about 93%



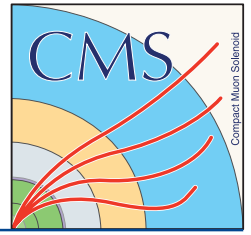
Schedule 2017

- Remainder of year as of 3 November



2 November CMS WGM report by SP

Conclusion on Pixel DC-DC converter problems



- We do not understand the problem despite strenuous efforts which now include the chip designers
- Doing nothing in the shutdown is not an option
  - unless a diagnostic breakthrough occurs allows us to halt the development of the problem by some external procedure
- We have a baseline plan to open the CMS, extract the pixel detector, FPIX and BPIX, which requires a 17 week minimum YETS
  - Must start on Dec. 4, for 11 Dec start, can't reach a configuration that is useful for pixel before key resources vanish
- Plan MUST be reviewed again in Jan based on diagnostics of the first failed units

9 November WGM: No big news since.
Slightly lower failure rate but statistics small.

UK R&D status

Last 6 months

- WP2: Tracker ASIC and readout
  - Very late arrival of bump-bonded die and new hybrids
    - CBC3 design changes correcting known faults almost complete
    - planning CBC3.1 submission, which may be last one
- WP3: L1 trigger and future hardware
  - L1 operation very satisfactory (reported only to confirm)
  - Hardware development continues & adapting to UK construction project needs
- WP4: HGCal
  - Snapshots of recent progress required for TDR in November
- WP5: L1 track-finder
  - Conclusion that FPGA-based system is the baseline
  - WP objectives achieved. Work will continue on system development
- close collaboration between WPs

WP2: CBC3 testing summary

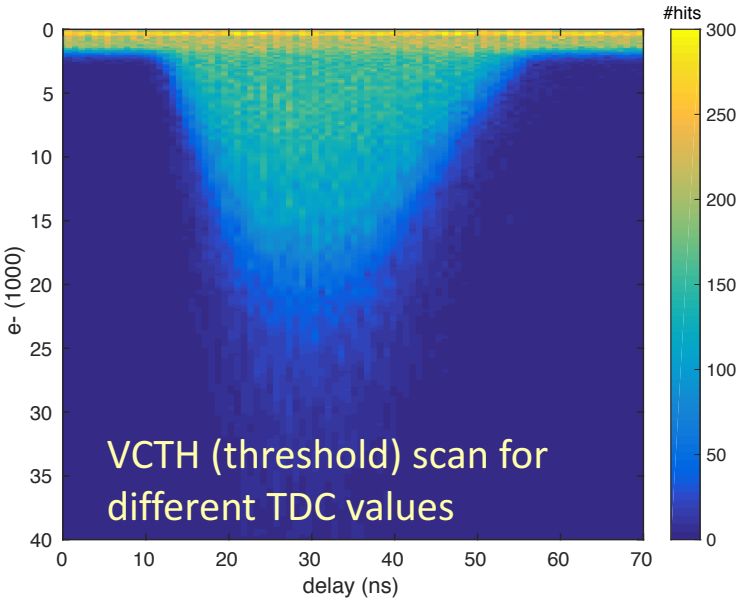
- Functional tests and improvements
  - Minor issues with stub and inter-chip logic identified
  - Data serializer (PISO) unstable for some delay settings
    - Much diagnostic work from Mark Raymond, now retired. Johan Borg replaces him

- Total ionizing dose tests
  - No performance degradation
  - Minor increase in power consumption over HL-LHC lifetime

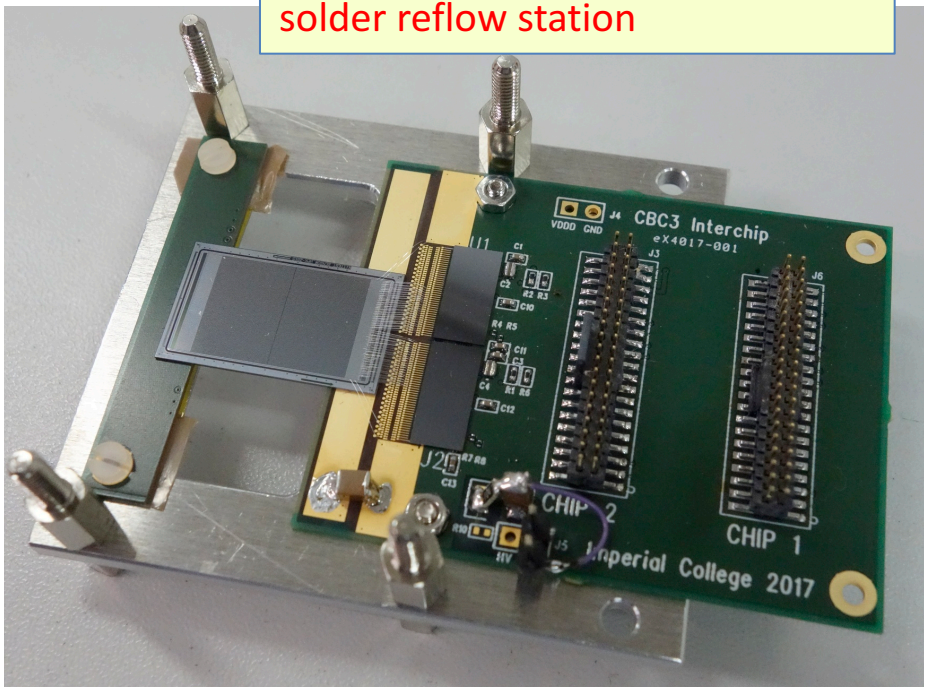
- SEU tests
  - Significant improvement compared to CBC2
  - Sufficiently robust if periodic reconfiguration is employed
  - Possible circuit modification for enhanced robustness has been identified

CBC3 beam tests

- First module test at CERN H8 π beam in October (including Xe ions)
  - High efficiency, using single layer module
  - HIP suppression logic tested with xenon ions
- More comprehensive test planned at FNAL in December
  - First 2S-module (double layer) test of CBC3
  - Further tests to verify detection efficiency
  - Extensive tests of stub logic

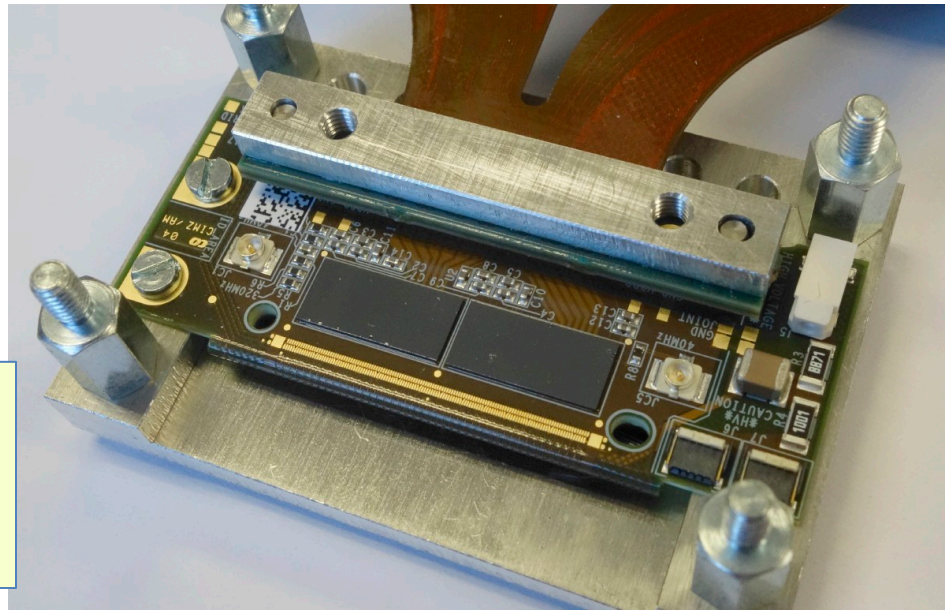


Hybrid manufactured by Imperial with CBC3s bump-bonded using solder reflow station



WP2 future

- CBC3 2S module tests continue
- CBC3.1 submission for manufacturing in January 2018
  - Stub and inter-chip logic fixes almost complete
  - PISO register improvements
  - Logic for wafer testing of inter-chip logic
- Testing of CBC3 wafers ordered by CERN (expected March?)
  - FC7-based wafer test system under development
- CBC3.1 verification (Q2 2018)



First CERN-designed 2CBC3 hybrid with CBCs commercially bump-bonded.

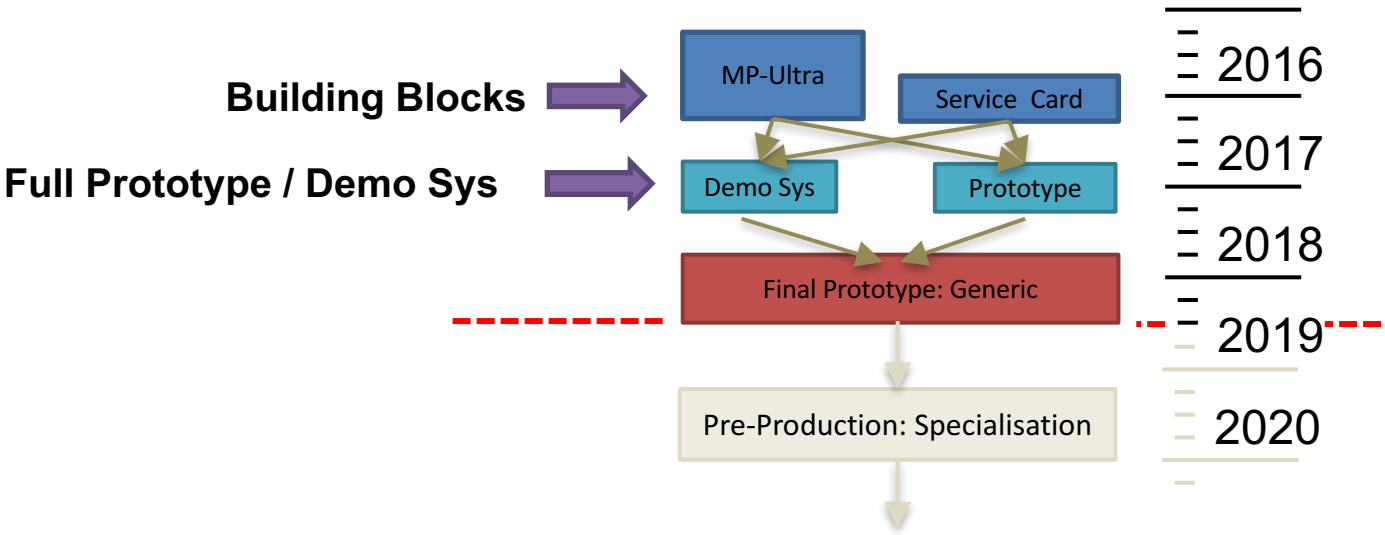
2S-module recently verified.

WP3: future hardware

- Prototyping continues, but overall plan is adapting to the needs of the expected construction project
- Three main users from UK, not all at same stage of development
  - L1 track finder and tracker DAQ (TDR “approved”, costs under review)
  - HGCAL (TDR submission November)
  - L1 trigger (Interim plan, TDR 2020)
- It is also likely that other CMS users will profit from developments
  - e.g. CMS DAQ
  - as well as aiming for common CMS standards, which are still being formulated
- Hence, attempting to plot a suitable course
  - prioritising UK projects where possible

Roadmap Part I

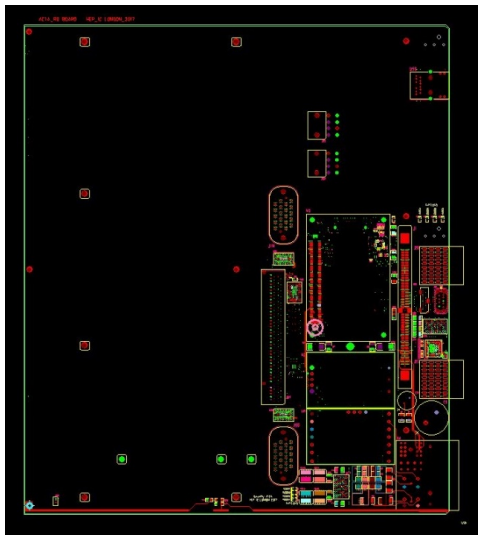
- Building block stage complete
  - MP-Ultra: Technology demonstrator
  - ATCA Services: Form factor test vehicle
- Design, manufacture and validate prototype over next 9 months
  - Card should be handed over to UK construction WPs Q2 2019
  - Accelerated compared to original planning - challenging

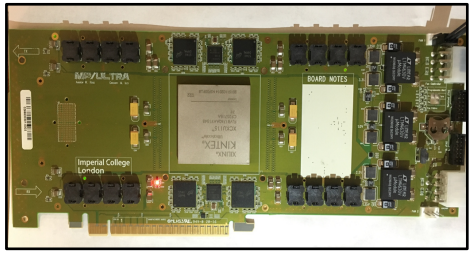


Building Blocks

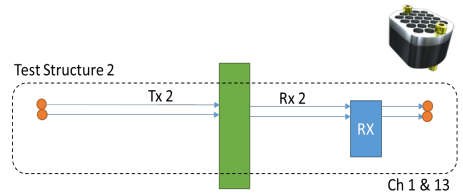
- Functionality verified using a series of prototypes
  - extensive use of COTS (Commercial Off The Shelf) parts

ATCA Service Card – May 2017



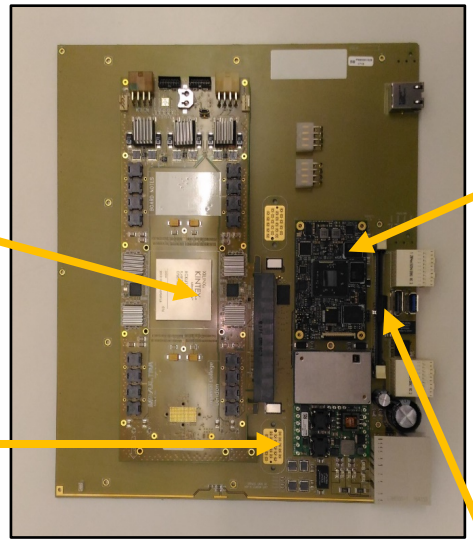


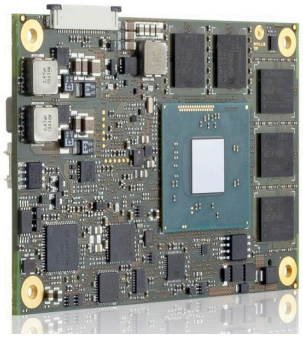
PCIe Card (e.g. MP-Ultra)



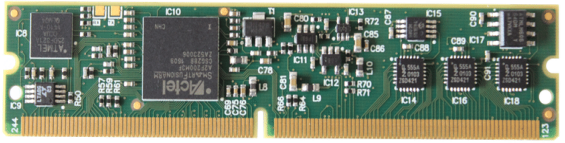
25Gb/s test structure w/wo re-timers (PCB & Backplane)

ATCA Service Card – Nov 2017





COM Express (COTS) High Level Control



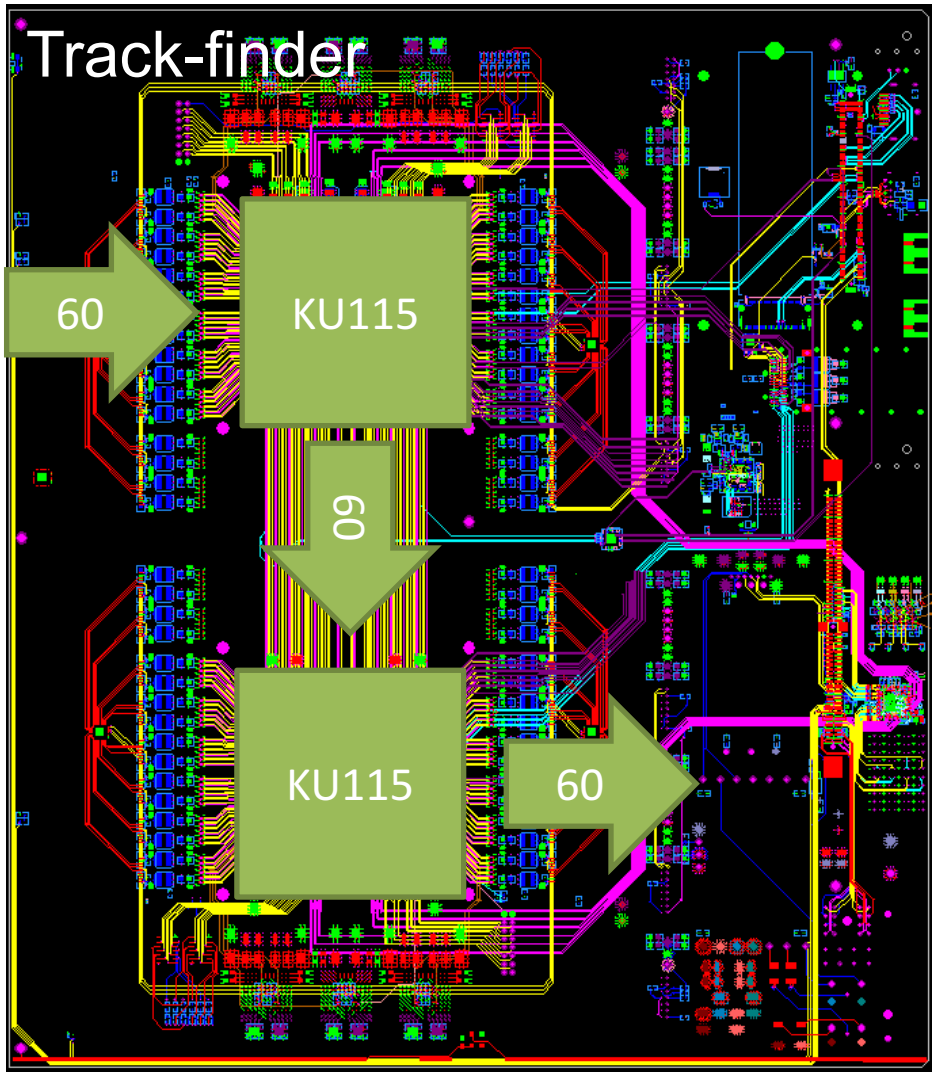
IPMC from CERN (COTS) Low Level Control

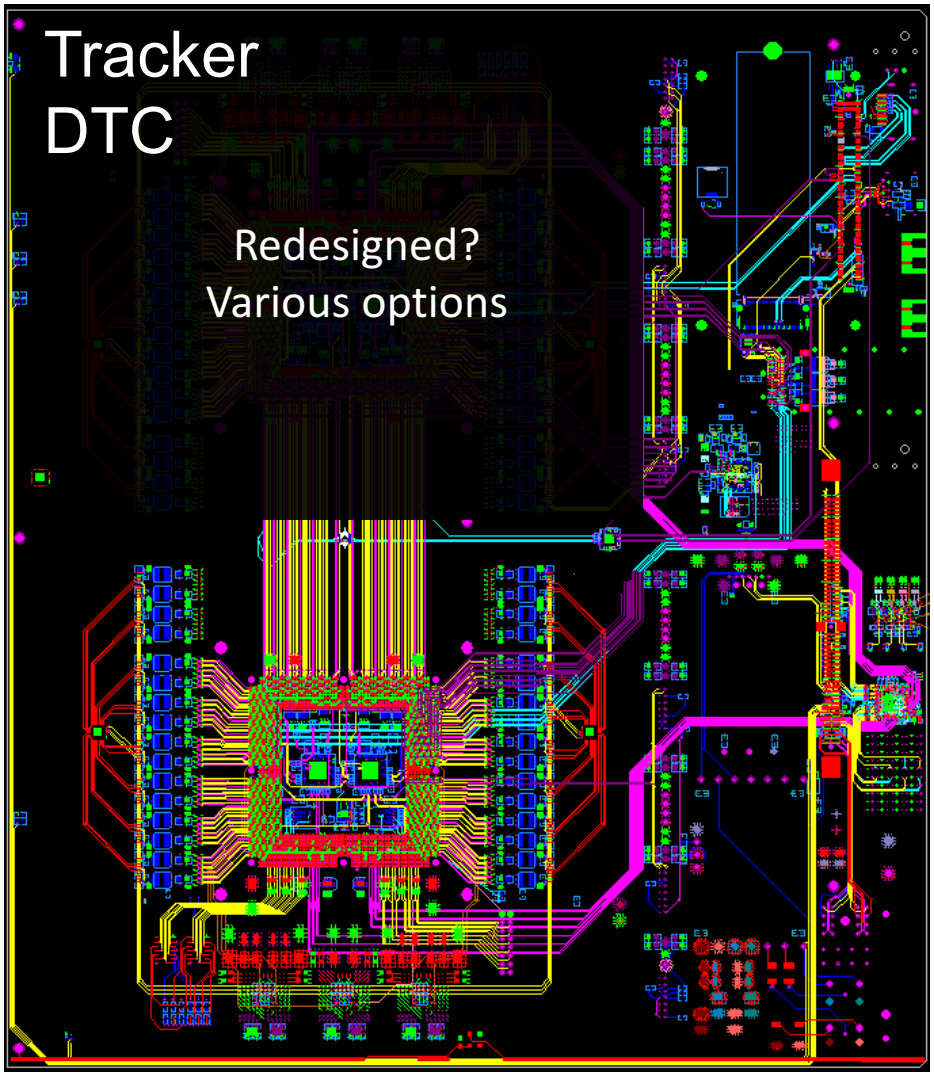
Requirements

	Application	FPGAs	Optics
Core UK projects	Track-finder	2× XCKU115 (daisy-chained)	60+60 @ 16Gbps
	HGCAL Cluster-finder	XCVU9P	96 @ 16Gbps 72 & 2+2 @ 16Gbps
	HGCAL DAQ	2× XCKU115 (independent)	96+96 @ 10Gbps 12+12 @ 16Gbps
	Trigger	being defined	being defined
	Tracker DTC	Various options being explored	
Wider collaborations	DTH	CERN DAQ group want to work with us to profit from our experience	
	Barrel muons	Keen to use UK hardware as per Phase-1	

- e.g. motivates concentrating design variation on the FPGA daughter-cards
  - attention needed to conform with practical constraints, e.g. cooling or relatively high cost and risk using large FPGAs

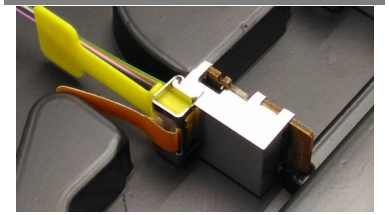
Tracker variants



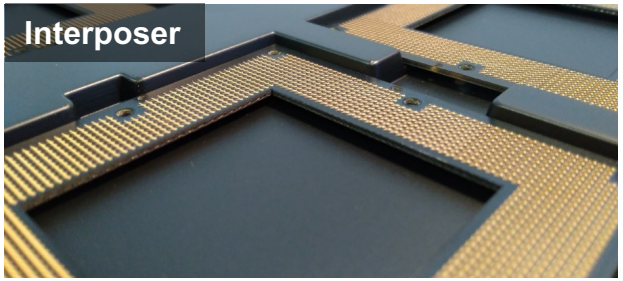


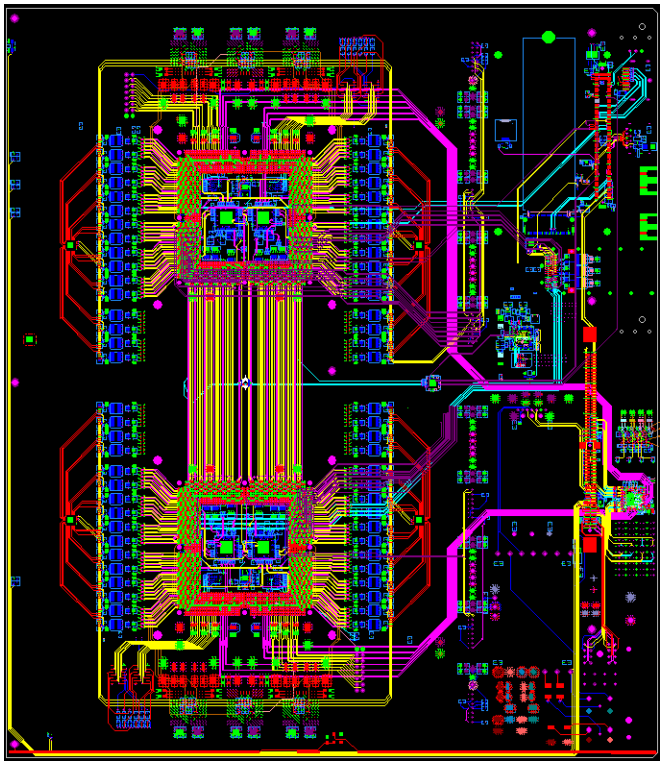
Hardware development status

- Refocused Rack Mount Chassis design to ATCA
  - Possible issue is air impedance of the underground counting room with Rack Mount Chassis design
  - ATCA form factor is a potential constraint



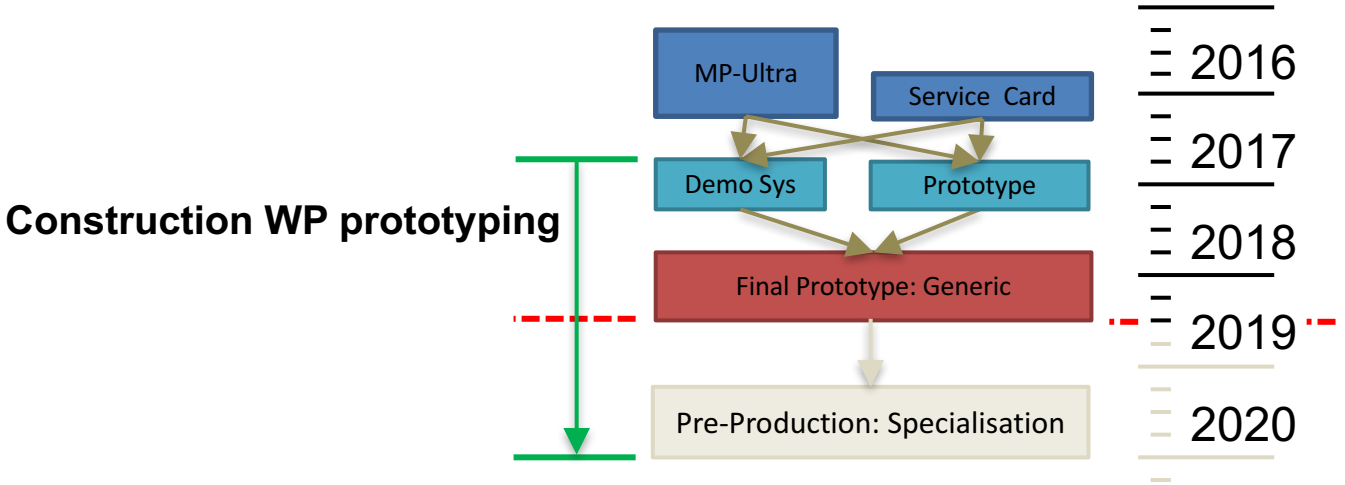
- Novel use of new connector technology to mitigate risk and provide flexibility with generic baseboard
  - Different link topologies & FPGAs available





Roadmap Part II

- Prototype
  - Manufacture Dec 2017 - Feb 2018
  - Deliver card & basic infrastructure Q2-2018
- Required for construction project protyping until Q4-2020
  - i.e. until Phase-2 Pre-Production v1 Card is available
  - approximate hardware roadmap defined with Phase-2 WPs
  - Reduce cost during R&D period by sharing hardware resources in common test-stand
    - Good precedent from L1 Track Finder
- Build team for firmware & software, involving UK & non-UK groups.
  - Provisional plan created



WP4: HGCAL

- Present objectives
  - Front end electronics evaluation
  - Trigger primitive generator design
  - Physics performance and design optimisation

- Studies under way for TDR in November
  - Snapshots of recent progress, which are important to confidently specify hardware design to meet physics objectives
  - Prototype hardware needs and delivery dates have been defined for the TDR in coordination with WP3

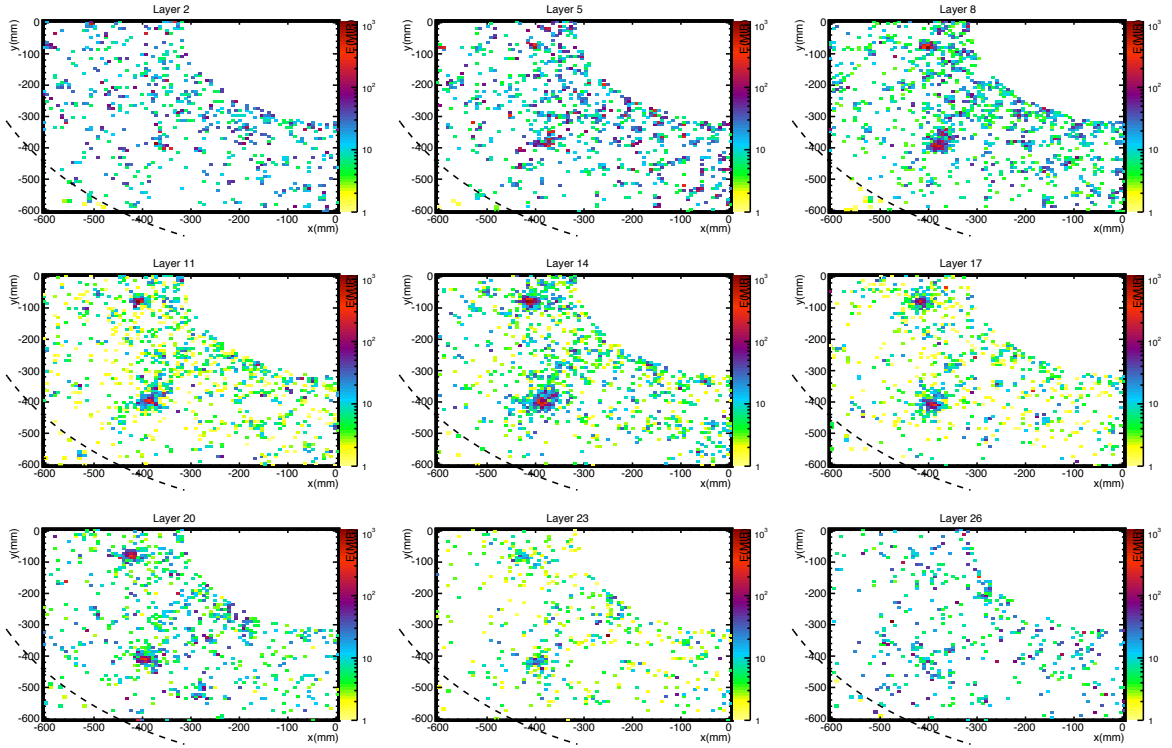
WP4: Photons and jets in the HGCAL

- Higgs plus VBF jet event, with H-> $\gamma\gamma$ at 200 pileup
  - Layer-by-layer event display showing quadrant near inner radius, i.e. highest pileup

Upper feature: Higgs decay photon with E_T = 22 GeV.
Clearly visible in layers 8-20

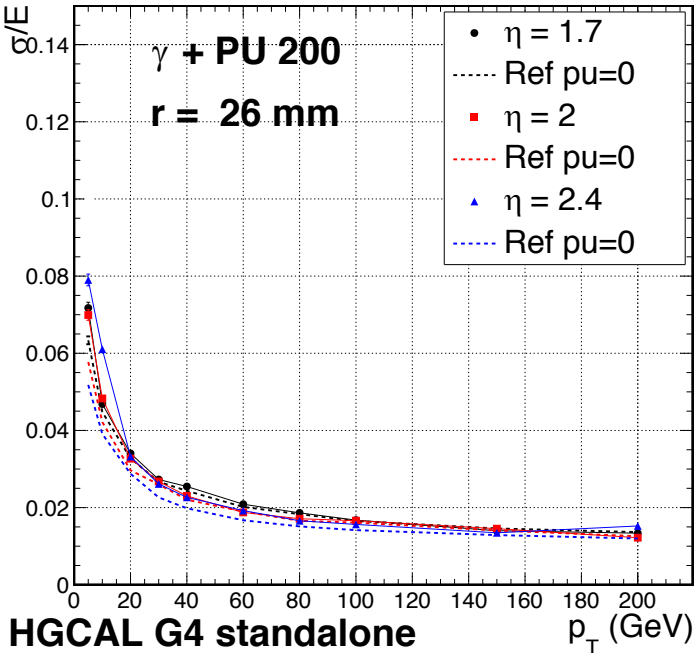
Lower feature: VBF jet with E_T = 118 GeV.
VBF jets are narrow with a similar width to photons so hits for both can be tightly selected in position to reduce pileup contamination

Distance between photon and jet illustrates power of high granularity in events, even with large pileup



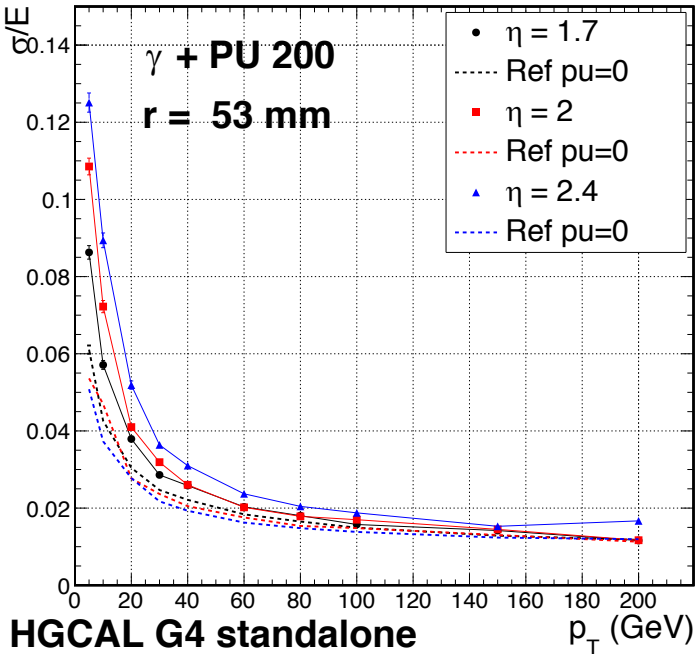
WP4: Electromagnetic resolution

- σ/E from offline reconstruction of γ energies at 200 pileup
  - Long-standing area of UK involvement



Hits associated with the photons are collected in a fixed radius, here 2.6 or 5.3 cm.

Resolution depends strongly on radius, due to inclusion of pileup



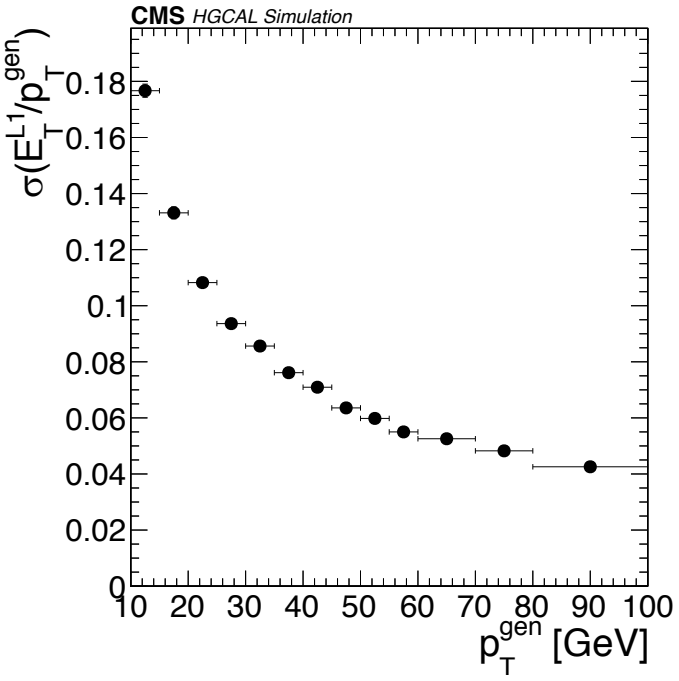
Optimal radius found to be 2.6 cm

Doubling to 5.3 cm includes ~4x pileup, degrading resolution by a factor of ~50%

Studies drive small HGCAL cell sizes of ≤ 1x1 cm^2

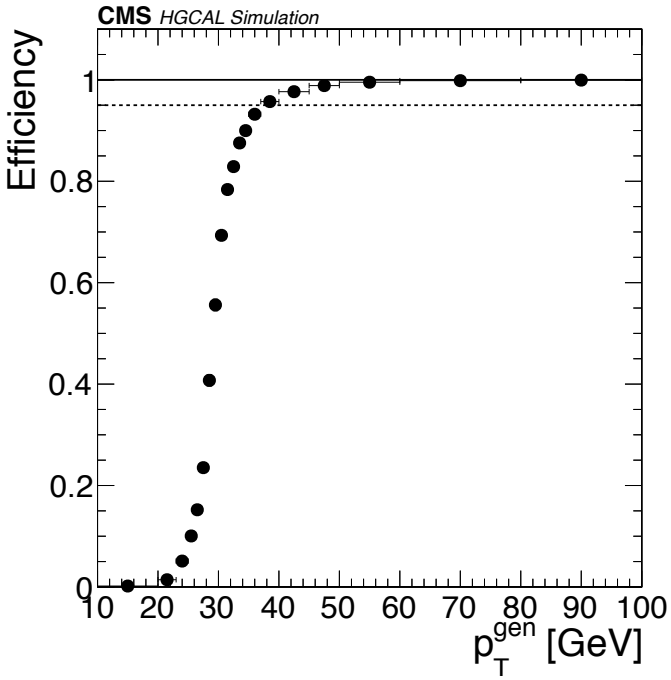
WP4: Trigger electromagnetic resolution

- σ/E from trigger reconstruction of γ energies at 200 pileup



Trigger information must be coarser than the HGCAL cell sizes to keep detector bandwidth affordable

Trigger cells are 2x2 or 3x3 sums of the basic cells



Trigger turn-on curve gives acceptable performance and background trigger rate

Further optimisation may be possible

WP5: L1 track-finder

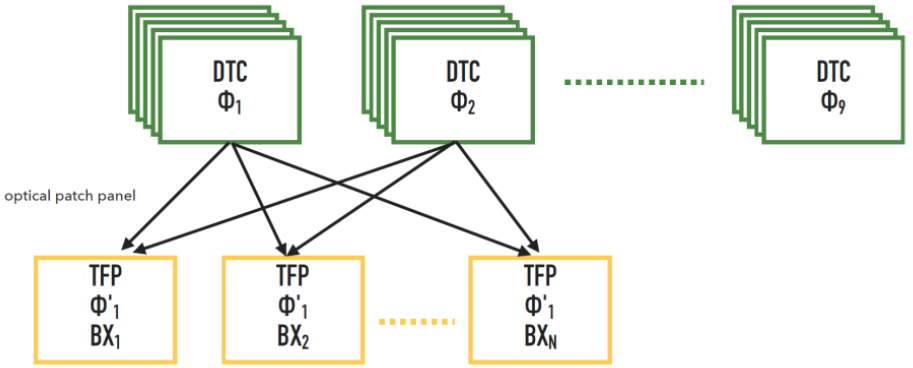
- Status reported at last OSC, following December 2016 review
  - UK successfully reconstructed tracks from emulated HL-LHC tracker hit data
    - demo system based on MP7 cards (= Virtex7 FPGA)
  - Tracking efficiency > 94% & latency = 3.7 µs for events at 200 pile-up
    - satisfies CMS requirements for L1 tracking
- CMS Tracker decision, May 2017, endorsed at CMS MB
  - FPGA-based solution chosen for L1 tracking (not AM)
    - New groups to manage Tracker BE electronics, with M Pesaresi coordinating BE System WG

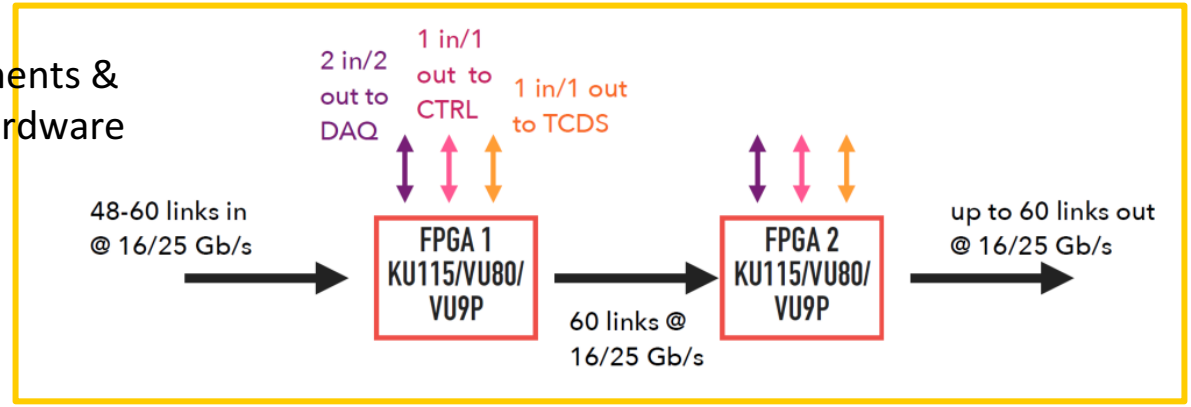
Data Processing WG
- Coord. with Tracker, Trigger, Physics
- Track-Finder robustness tests

BE System Development WG
- Tracker DTCs + firmware
- Track-Finder + firmware + algorithms

L1 track finder concept

- Next steps
  - Track-Finder architecture based on UK time-multiplexed concept
    - Enables factorisation of hardware development from algorithm R&D
    - Enables progress on defining all aspects of the system, including DTC
    - TF algorithm development can proceed, within TF processor (TFP) constraints
  - R&D
    - ATCA developments based on Ultrascale-gen FPGAs (in WP3)
    - Track Finding algorithm developments & optimisation aligned with WP3 hardware





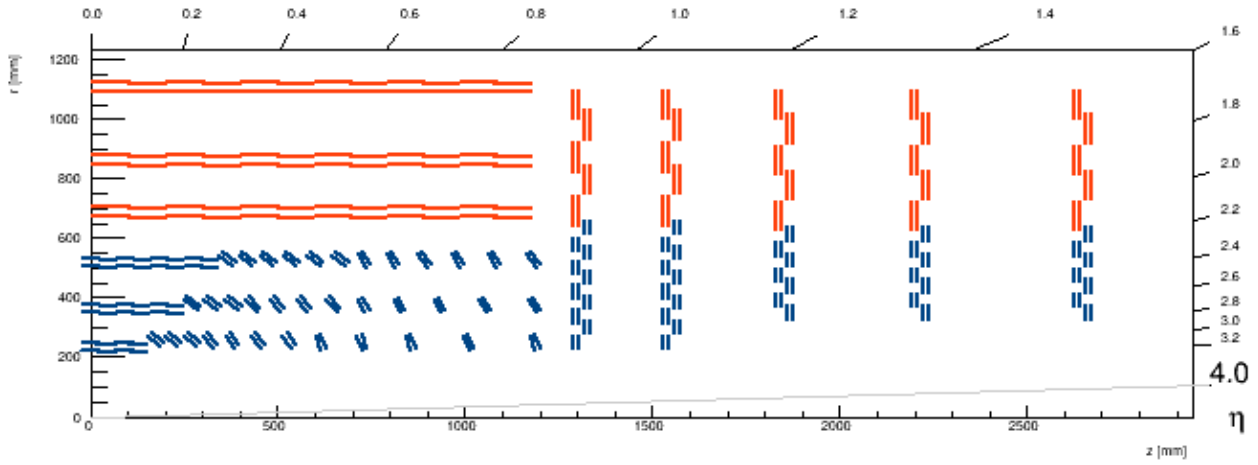
Deliverables

- Original WP5 deliverables have been met
  - Define new deliverables, aligned to hardware developments in WP3 and longer term construction interests
- Focus is on:
  - TF algorithm development & optimisation through simulations
    - in close coordination with L1 trigger algorithm development in WP3
  - Porting TF firmware to run on next-generation FPGAs (Ultrascale)
    - aligned with WP3 hardware & firmware developments
    - taking advantage of new features, e.g. UltraRAMs, clock skew management to run logic faster etc.

Date	Description
18Q4	Demonstration of L1 Tracking using Ultrascale FPGAs
19Q2	Demonstration of DTC+L1 Tracking chain using Ultrascale FPGAs

Ongoing work

- Modifying firmware to run at higher frequency (480 vs. 240 MHz) in Ultrascale devices
  - Reduces logic use, more flexibility for improvements/feature requests
  - Reduces latency
  - Allows FPGAs to process data from higher speed opto-links (16 vs. 8 Gb/s)
    - ~50% of L1 tracking logic already running at 416-500 MHz
- Algorithms modified in simulation to cope with new Tracker geometry, & tilted modules
  - Tracking efficiency preserved, with welcome reduction in data rate
    - ~30% in some elements of L1 tracking chain



UK construction project

- Proposal to PPRP submitted October
  - closely follows outline construction project, September 2016
    - presentation January 2018
- Four construction WPs, plus management activity
  - WP2: Common technology
  - WP3: Silicon tracker
  - WP4: Calorimetry
  - WP5: Trigger

- Most of activities based on developments from this R&D project
  - especially using common hardware, or family

Matters arising in May

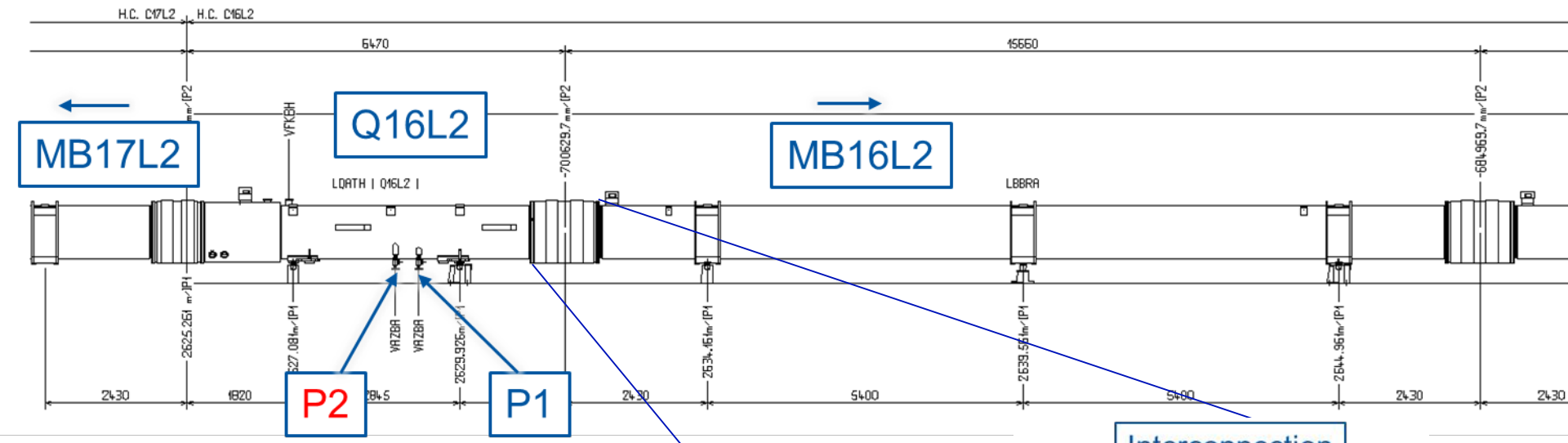
- L1 track finder issue resolved as explained
  - Very satisfactory outcome for UK, and credit due for very big efforts
- Financial status
  - Expenditure within targets with part of WA still available
  - Part of WA for CBC design work and travel to be released
    - agreed with STFC how to handle this
- Another effort vs WP snapshot provided
- Revised risk register, with explanations in report

Conclusions

- Steady progress and hopefully auspicious start to construction phase
  - from April 2019, subject to PPRP approval

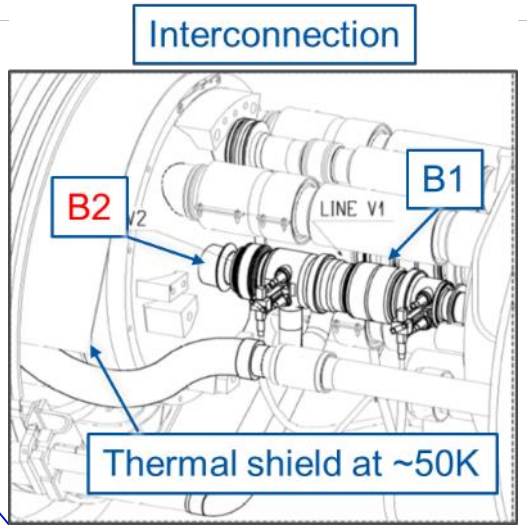
Further information

LHC “16L2”: Air inlet as “most probable” cause



Air inlet through **both** pumping ports while magnet cold masses, beam screens and thermal shields already at operating cryogenic temperature.

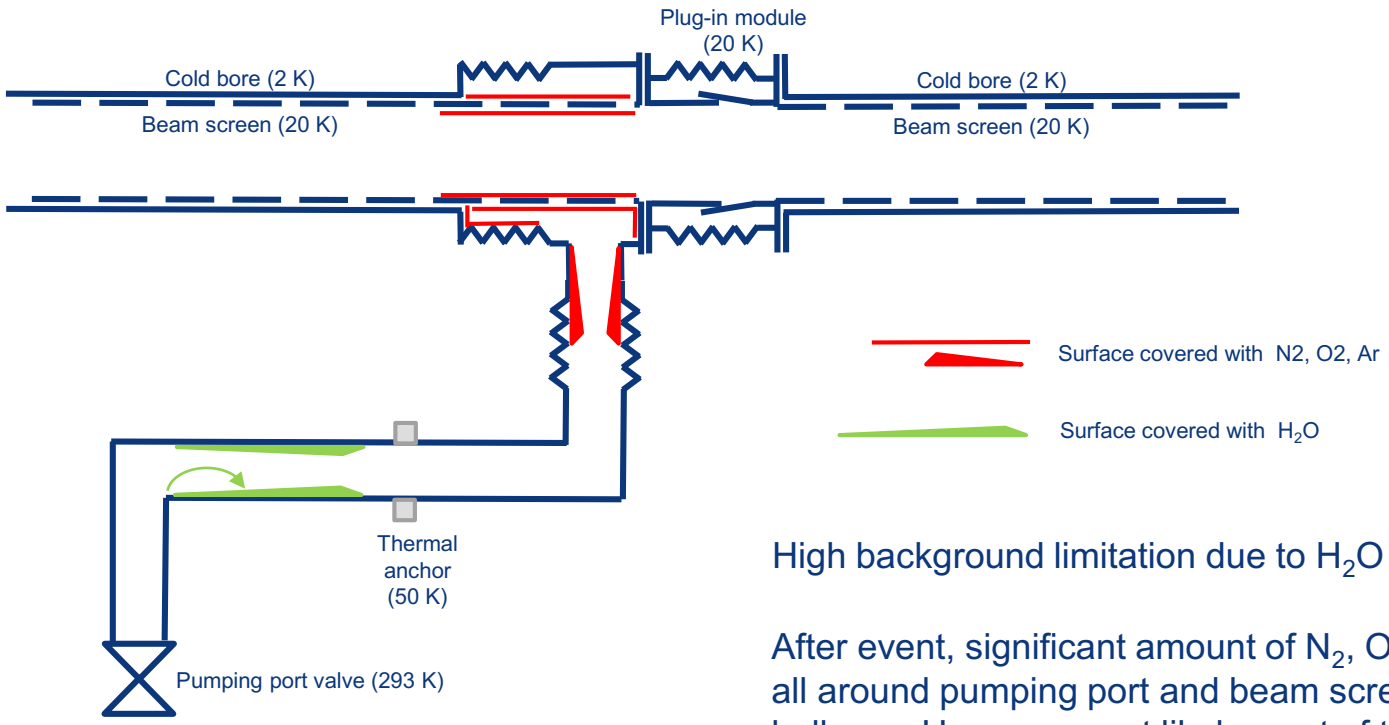
To be noted that gasses have a reduced mobility at those temperatures, explain why was not immediately identified.



LHC “16L2”: Air inlet as “most probable” cause

Event (accidental air inlet with BS at 20 K)

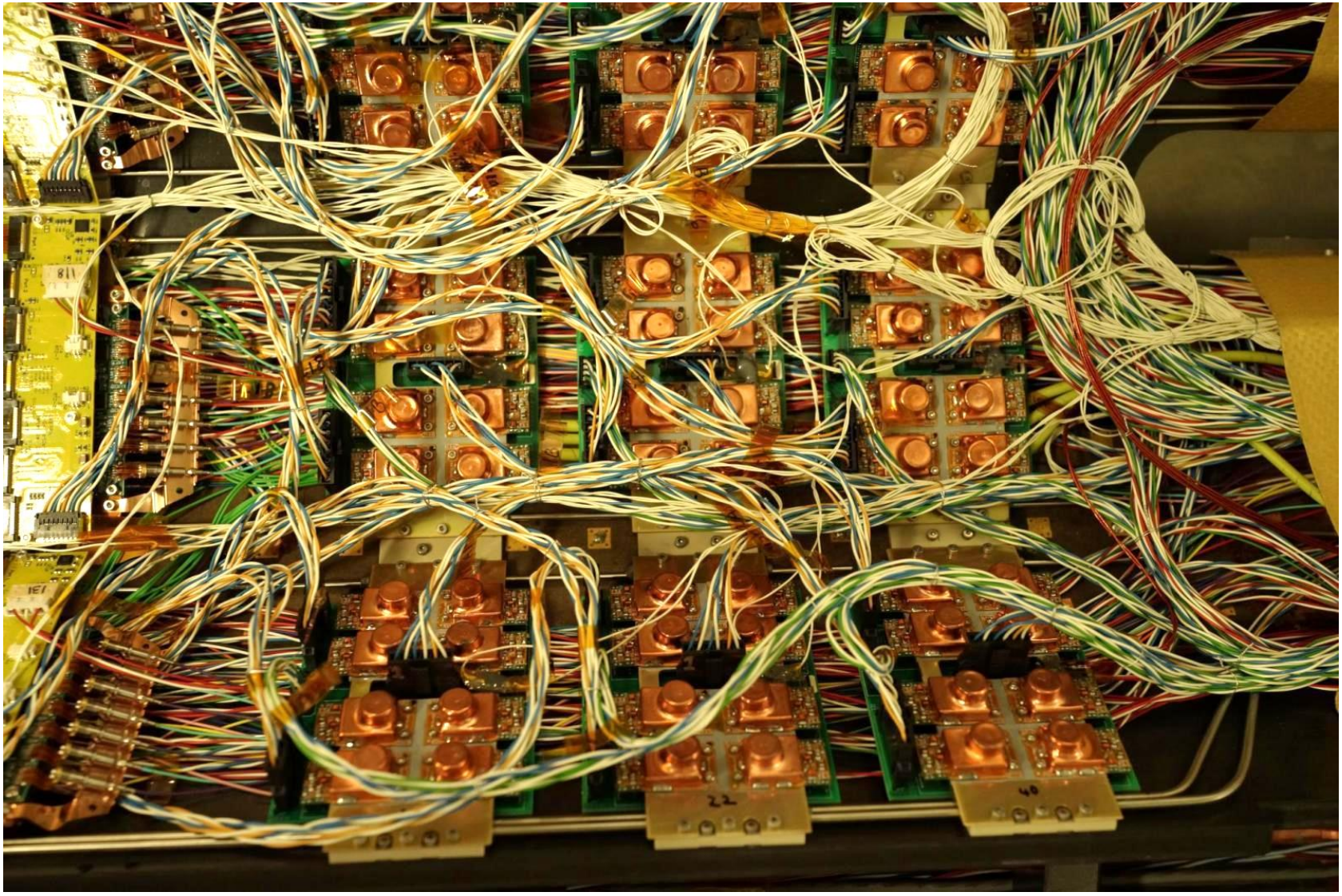
(same pumping group pumping beam 1 and beam 2)

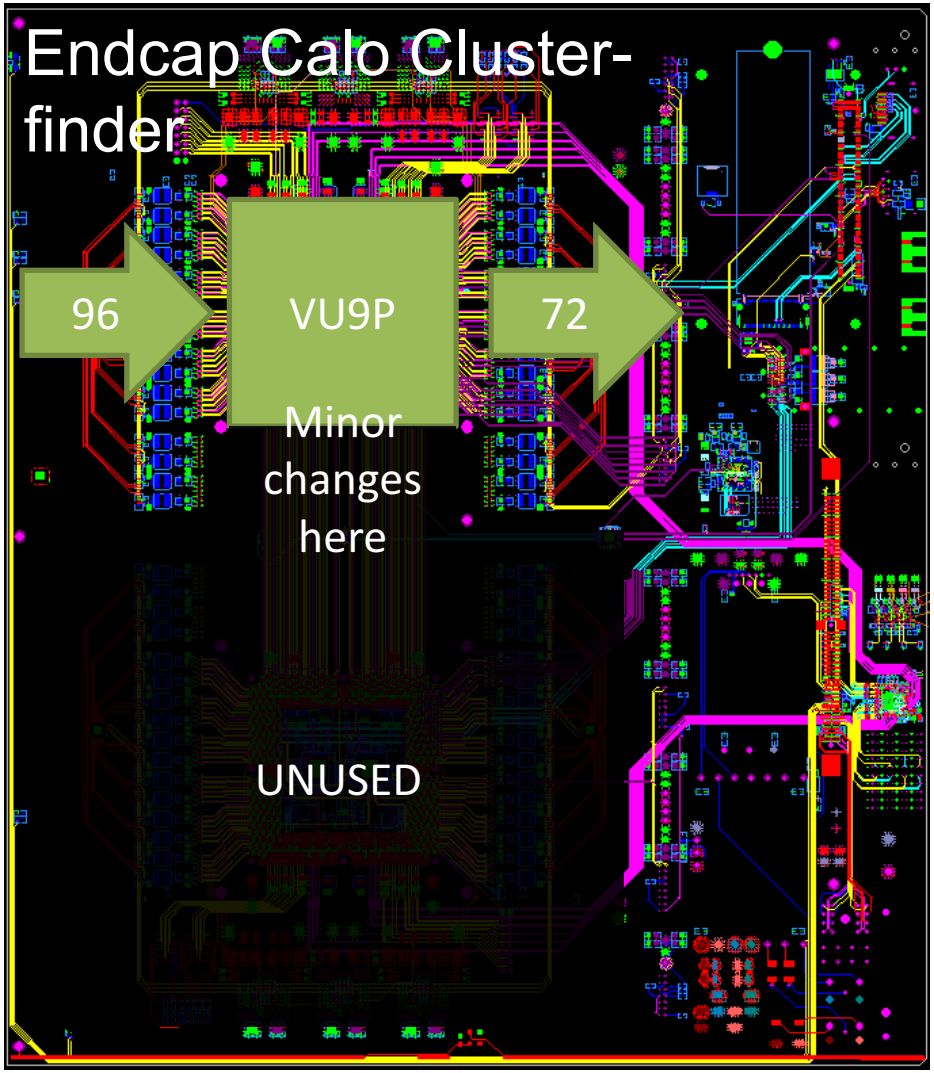


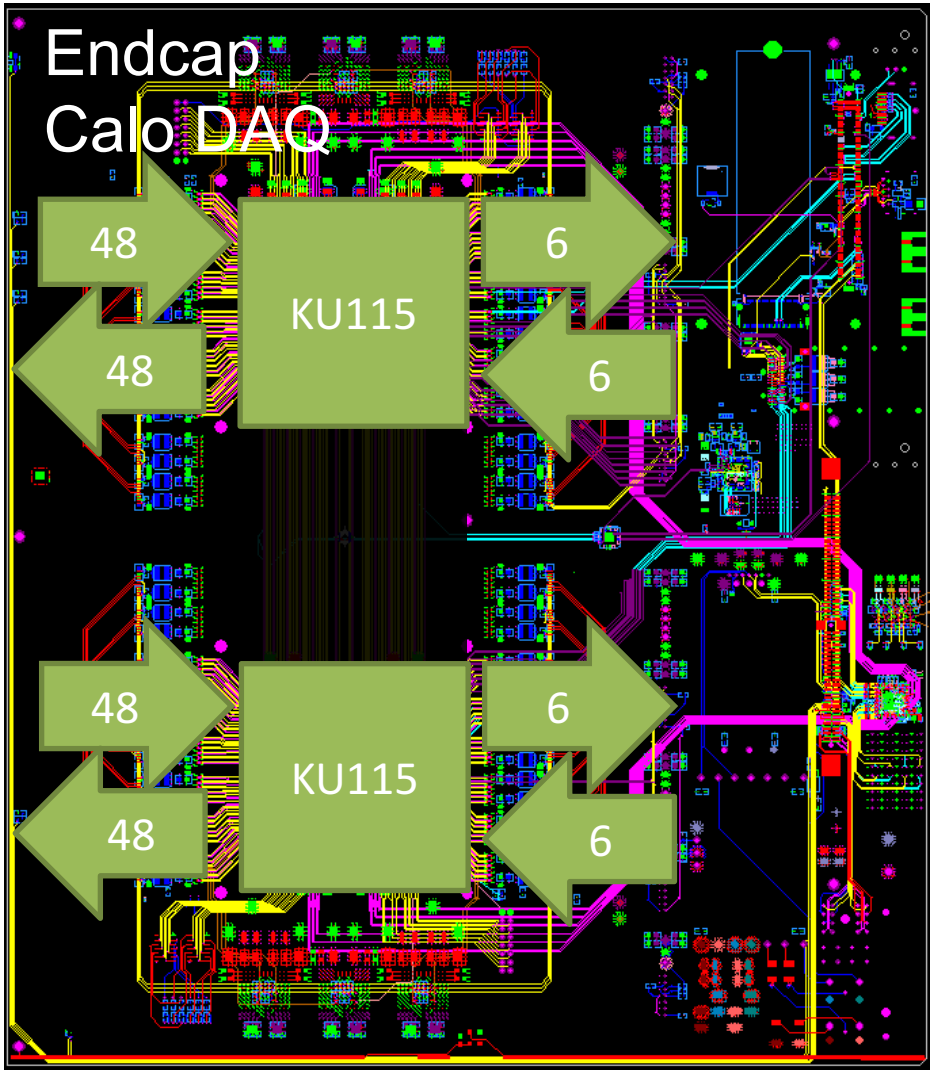
High background limitation due to H_2O from air.

After event, significant amount of N_2, O_2 and Ar all around pumping port and beam screen bellows. However most likely most of those gases stick on the pumping port bellows.

Installed FPIX DC-DC Converters

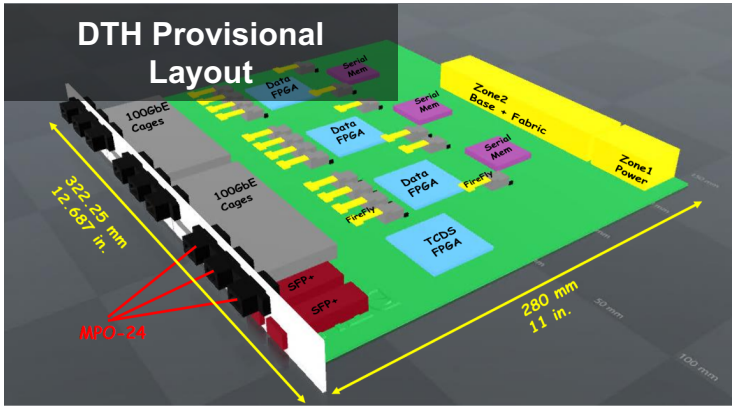



Endcap Calo Cluster-finder
96
VU9P
72
Minor changes here
UNUSED


Endcap Calo DAQ
48
48
KU115
6
6
48
48
KU115
6
6

CMS issues

- Several important constraints
  - electrical or optical interface?
    - DAQ now plans 16G-25G optical interface to sub-detectors
    - Backplane performance requirements relaxed
    - Simpler PCB manufacture



  - ATCA form factor
    - Cooling, real estate and noise yet to be fully addressed and issues may arise in future
    - May change to be more suitable for underground counting room
    - Existing R&D work compatible with both ATCA and 19" Rack Mount Chassis