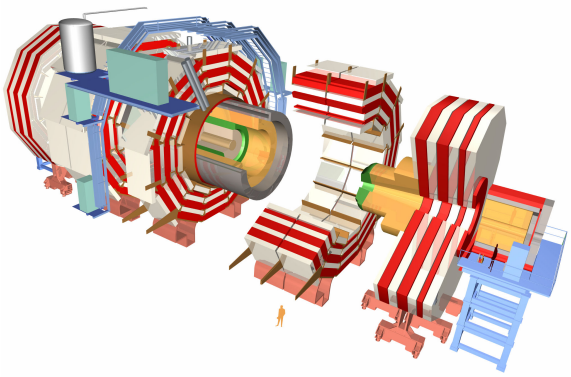
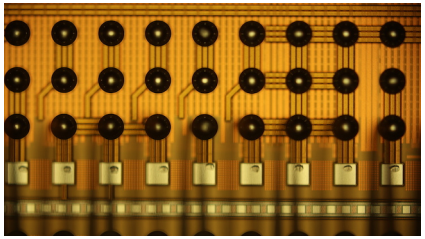
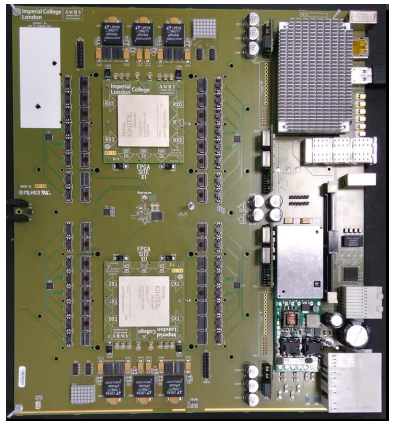




UK CMS Upgrade Oversight Committee

21 November 2018



University of Bristol
Brunel University London
Imperial College London
Rutherford Appleton Laboratory

Overview

- Snapshots of LHC & CMS status
  - LHC achieved the Run2 target of >150 fb^{-1} p-p
    - CMS recorded 63 fb^{-1} p-p @ 13 TeV in 2018
    - Pb-Pb data taking now under way – several UK contributions to operations
    - The pixel problem of failing DC-DC converters was understood

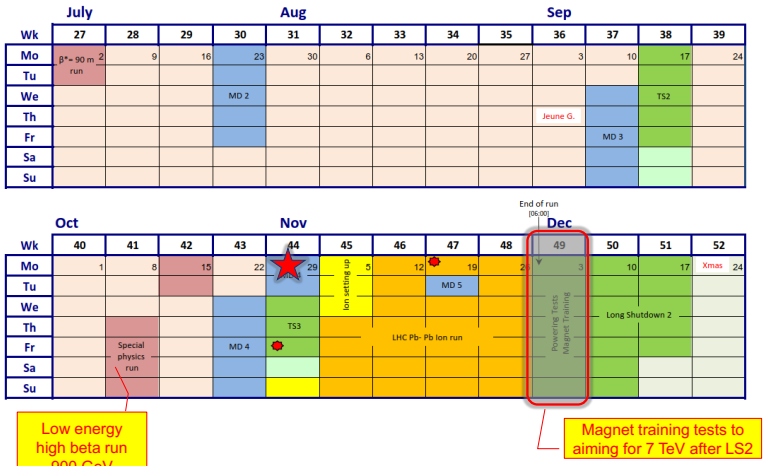
- Summary of recent progress in UK upgrade project
  - Short look back as we approach the last part of 10 years R&D
    - Including some valedictory remarks
  - UK CMS upgrade construction project due to start April 2019
    - A new team to oversee the next phase

LHC machine

LHC Beam parameters achieved

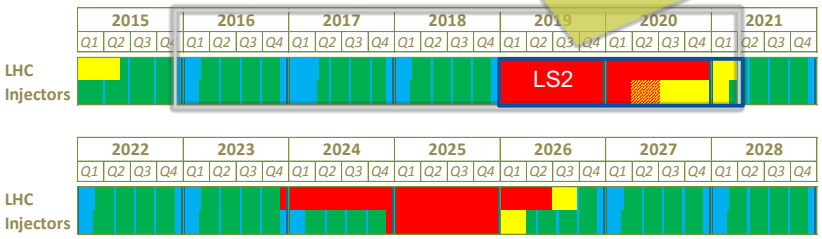
Parameter	2018	Design
Energy [TeV]	6.5	7.0
No. of bunches	2556	2808
Max. stored energy per beam (MJ)	312	362
β* [cm]	30→25	55
p/bunch (typical value) [10^{11}]	1.1	1.15
Typical normalized **emittance** [μm]	~1.8	3.75
Peak **luminosity** [10^{34} cm^{-2}s^{-1}]	2.1	1.0

LHC: outlook on rest of 2018



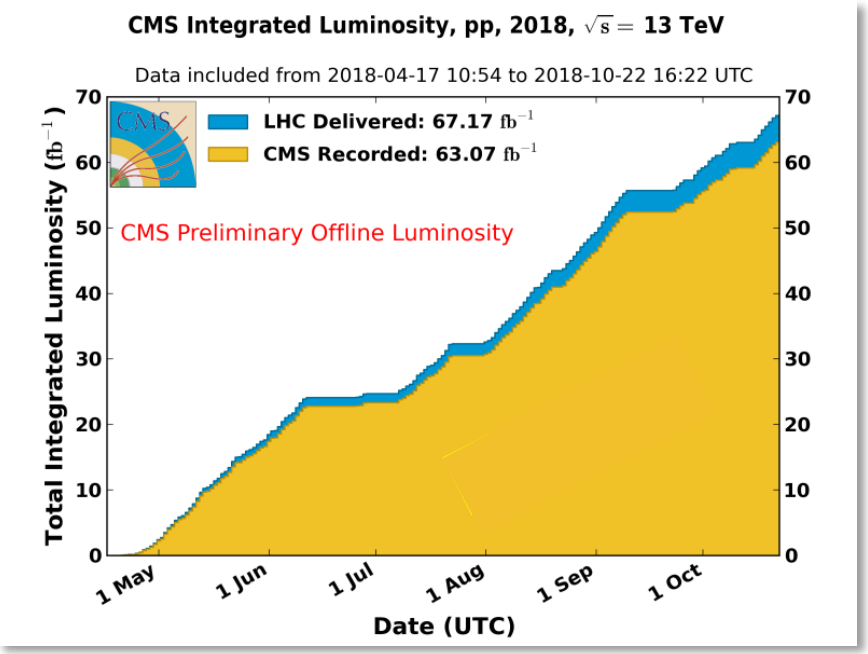
The Long Shutdown 2 (LS2)

- **Perform major Maintenance and Consolidations**
- **Increase intensity/brightness in the injectors to match HL-LHC requirements (LIU Project)**
- **Increase injector reliability and lifetime to cover HL-LHC run (until ~2035) closely related to consolidation programs (in synergy with LIU Project)**
- **Anticipate HL-LHC work**



CMS in 2018

- **Excellent performance of LHC** and of CMS
  - LHC goal of 150 fb^{-1} in Run 2 reached, several weeks before moving to Heavy Ions program
  - above 94% recording efficiency, record high in CMS
  - Aggressive use of the DAQ bandwidth with B-parking
    - With smooth computing operations



Many thanks to LHC !

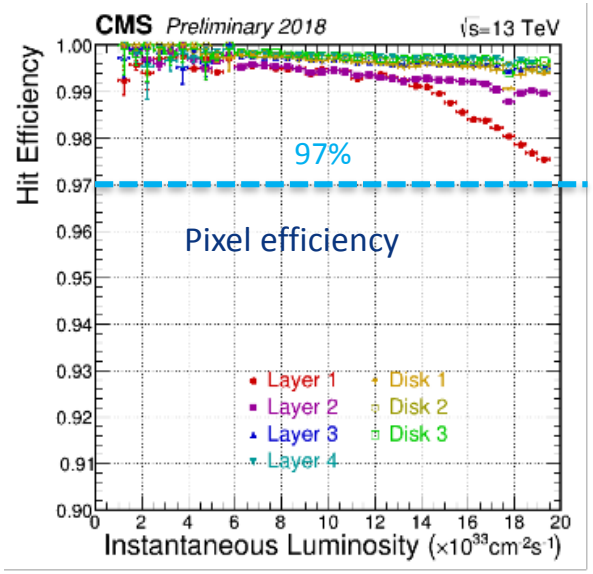
Quality of data

CMS is taking excellent quality data, including in **several special runs**

- VdM scans, 90m β^* CMS-TOTEM joint run, Low PU run (HI run is next)

DC/DC converters, **failure mode understood** as the combined result of irradiation and use of the enable/disable feature

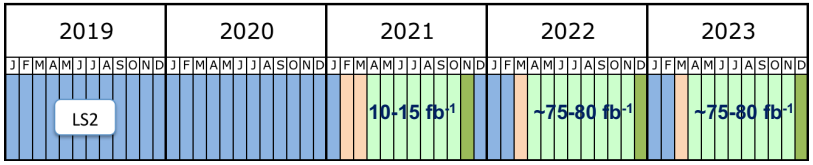
- **This understanding allowed us to prevent it to happen in 2018**
- Many thanks to the CMS Tracker Team, Technical Coordination , and the CERN FEAST design team



LHC plans

Run 3 outlook

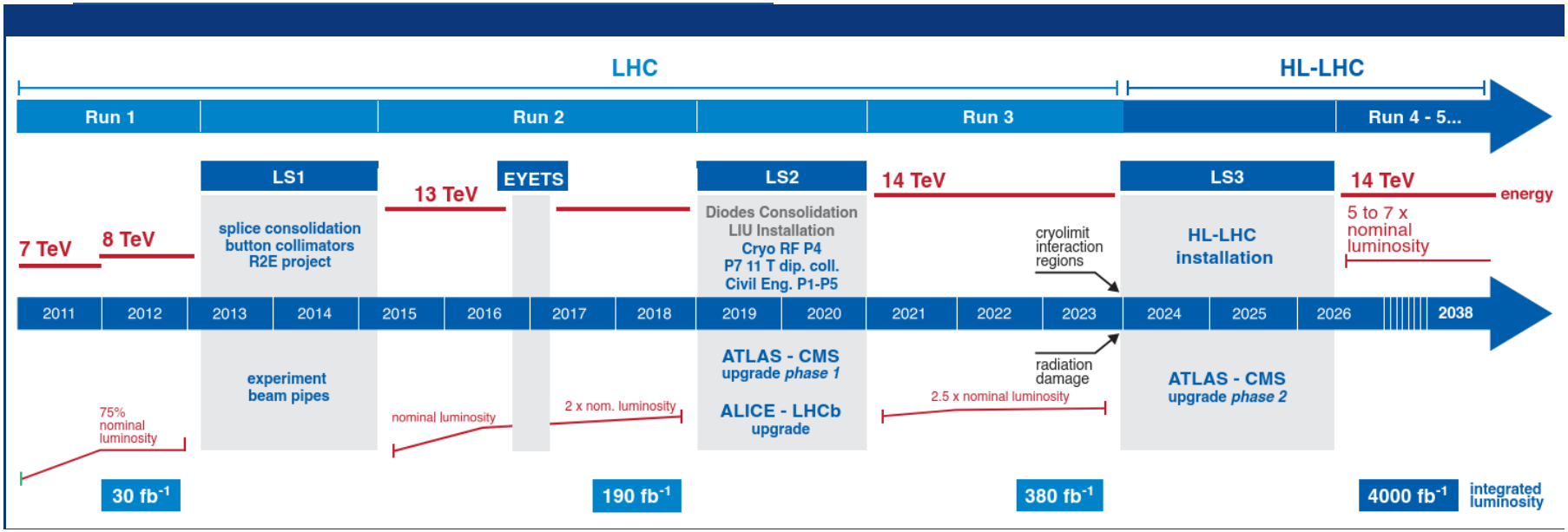
∑(Run1 + Run2 + Run 3) > 300 fb^{-1}



2021: beam commissioning in the injectors after LIU upgrade
LHC 14 TeV commissioning and operation

2022-2023: production years at 14 TeV ;
Lpeak ~ 2.0-2.2 10^{34} cm^{-2}s^{-1} ; luminosity levelling

>350 fb^{-1}

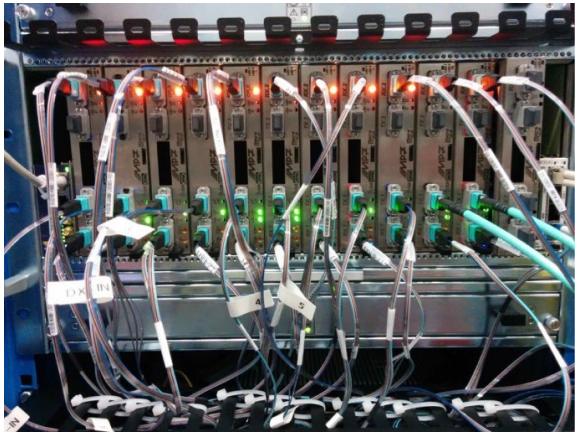


Brief historical recap

- First phase of project started 2009
  - CBC ASIC for outer tracker readout (but not trigger data)
  - Hardware for future CALO trigger & tracker DAQ
    - Work underway on track-trigger ideas (eg M. Pesaresi, A. Rose PhD theses 2009)
- Second phase from 2013, by which time:
  - PT-modules throughout tracker & CBC2 ASIC for 2S-modules (data for trigger)
    - Substantial increase in trigger rates from 100->750 kHz, latency -> 12.5 µs
  - Upgrade of Calo trigger planned, based largely on UK µTCA hardware (MP7)
    - Time Multiplexed Trigger demonstrated in slice test Sept 2013
  - MP7 & CBC2 both state-of-the-art developments (well ahead of others)
    - and successors (Serenity, CBC3) still are
  - FC7 spinoff (with CERN) general purpose DAQ board (pixels, TCDS, HCAL, g-2,…)
  - MP7 track-finder demonstrator December 2016
    - proved FPGA-hardware could deliver real time TF in latency, performance, budget
    - common hardware applicable throughout CMS (tracker, HGCAL, trigger,…)

Calorimeter trigger upgrade

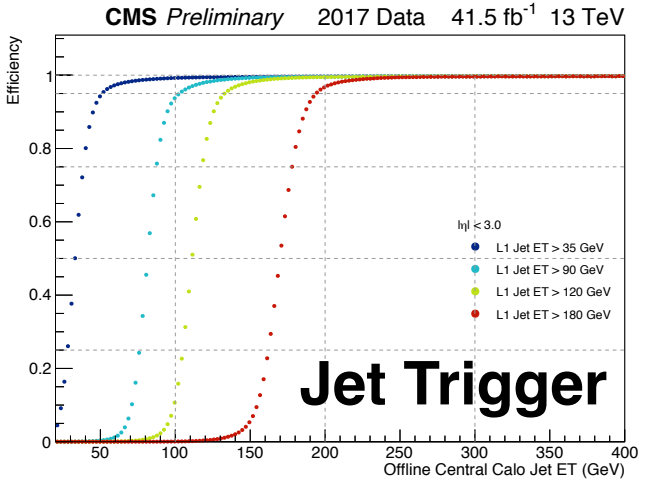
- System installed at P5 in 2014
  - 10 MP7 boards + spares installed ✓
  - Fibre connections installed and validated ✓
- Commissioning
  - Interconnection tests ✓
  - Pattern test campaign in 2015 ✓
  - Data taken in CMS global running in 2015 ✓
    - Over 7 billion events in pp running
  - Cosmic runs and splashes in 2016 ✓
  - First collisions in 2016 ✓
  - **Start 2016 physics run** ✓
- Misc
  - Additional MP7s for project delivered ✓

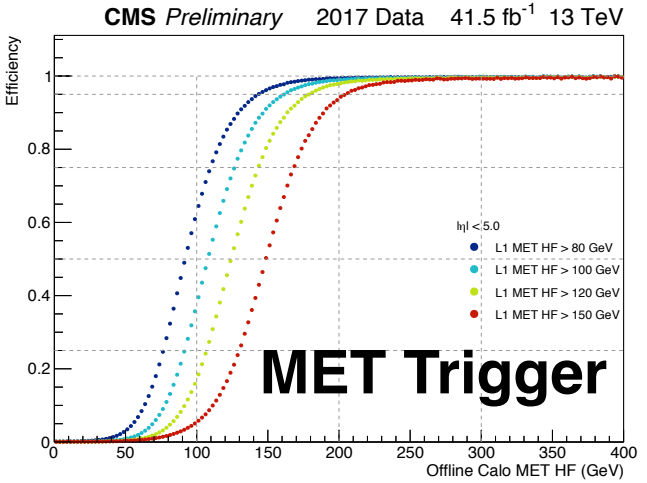


The use of the fibre shuffle boxes (fibre networks built by robots) was a first in HEP. It reduced a hand-crafted rack of fibre patch-panels down to just 3 pre-assembled boxes, installed in minutes.

Calorimeter trigger upgrade

- Running very reliably and efficiently since 2016 — low maintenance
- UK leading jet and MET algorithms → linking to UK physics interests
- Flexibility to adapt to LHC conditions e.g. higher pileup from change in bunch structure in 2017
- Significant changes made to optimise for Pb-Pb run in 2018





UK R&D status

Current status

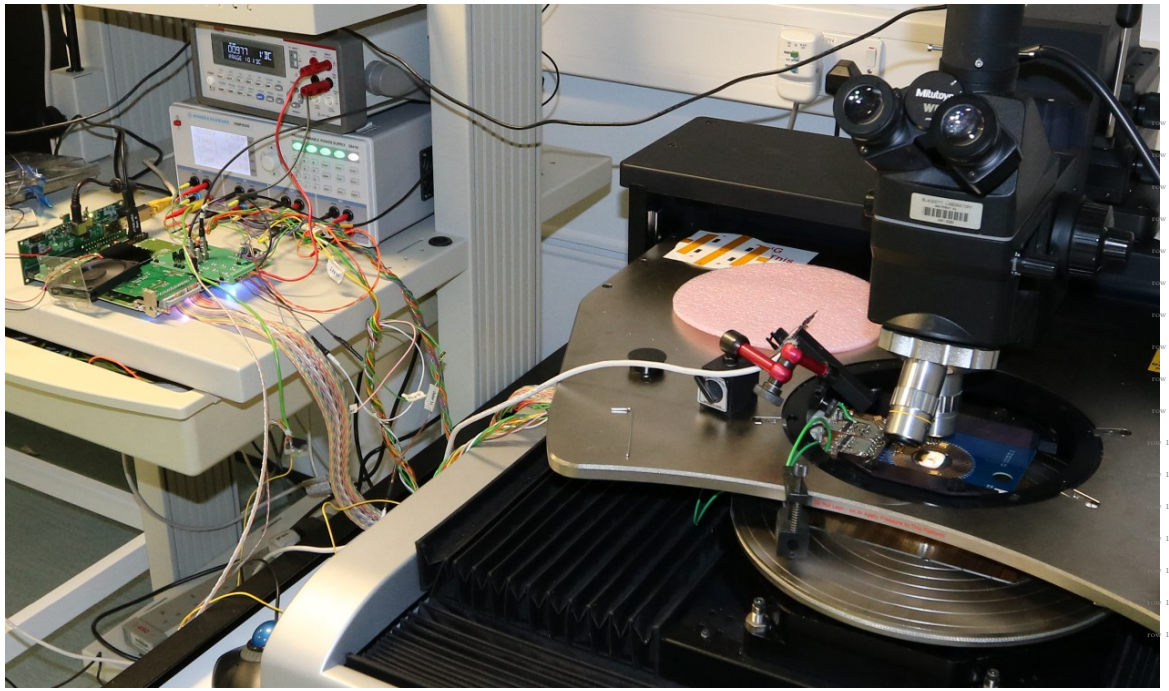
- CBC3.1 delivered September
  - Tests confirm design changes successful
  - Should be final version, ready for production
- Serenity 1.0 proven
  - Serenity 1.1 expected imminently
    - And eagerly awaited to be used in multiple CMS applications
  - Common hardware paradigm seems to be taking root
- Rapidly developing collaborations across projects on BE systems
  - CMS workshop June, TK workshop November
  - Engagement from L1 trigger & HGCAL
  - Evolving work on hardware, firmware and software

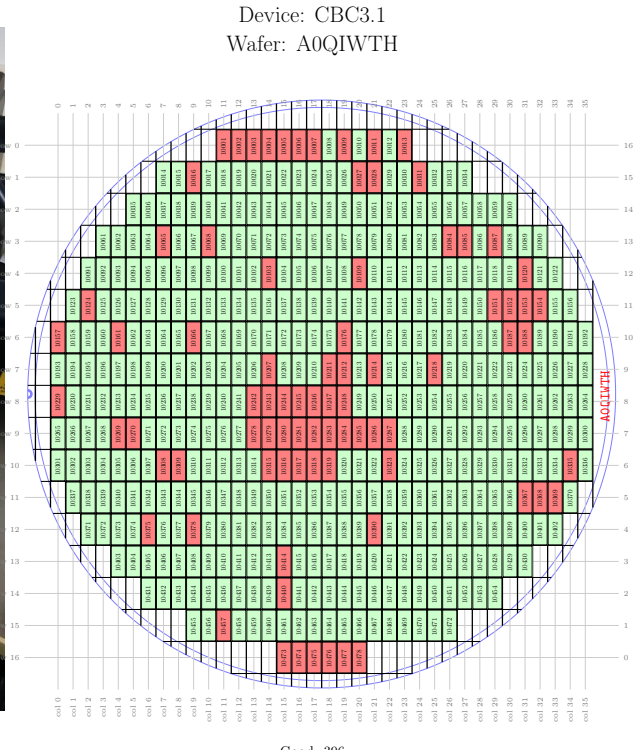
Last 6 months

- WP2: Tracker ASIC and readout
  - CBC3.1 returned and initial tests carried out
    - TID x-ray tests in CERN 12-16 November
  - CBC3.0: 24 wafers delivered and probe tested, for prototype modules
    - NB both many months late, plus previous delay in CBC3.0 hybrids (~1 year)
- WP3: future hardware
  - Serenity 1.1 subject to manufacture delays but expected soon
- WP4: HGCAL
  - Cluster algorithm implemented in firmware
- WP5: L1 track-finder
  - Work on system development continues
  - Stress test passed
- Summarise WP3-WP5 together

WP2: CBC3 status

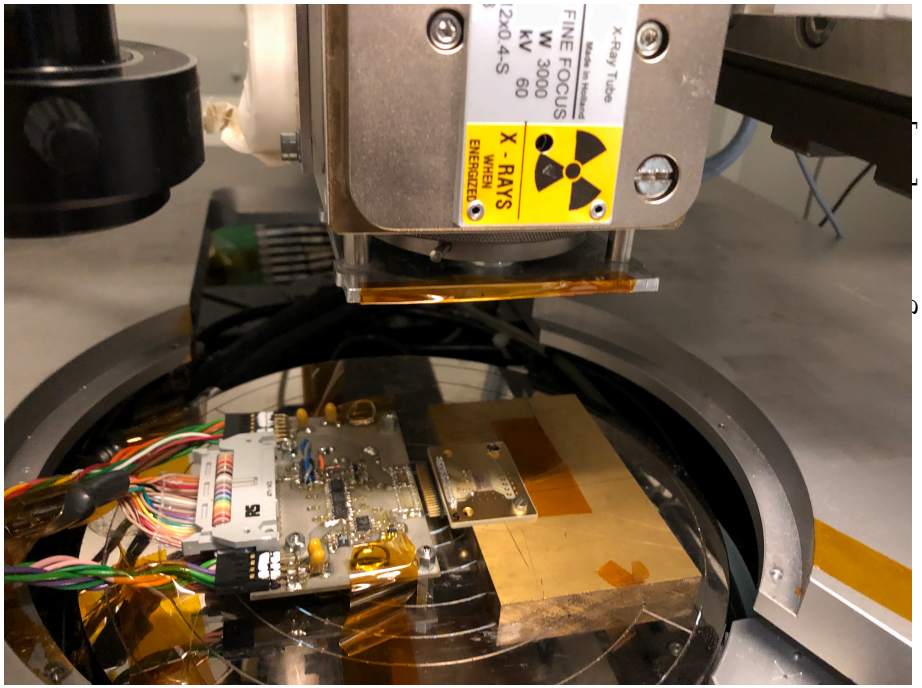
- Wafer probing with revised setup
  - FC7-based DAQ and new firmware and software
    - Very comprehensive set of tests on each CBC3.1 site (486 per wafer)
  - Yield under study & preparations for final validation (SEU, full modules,…)

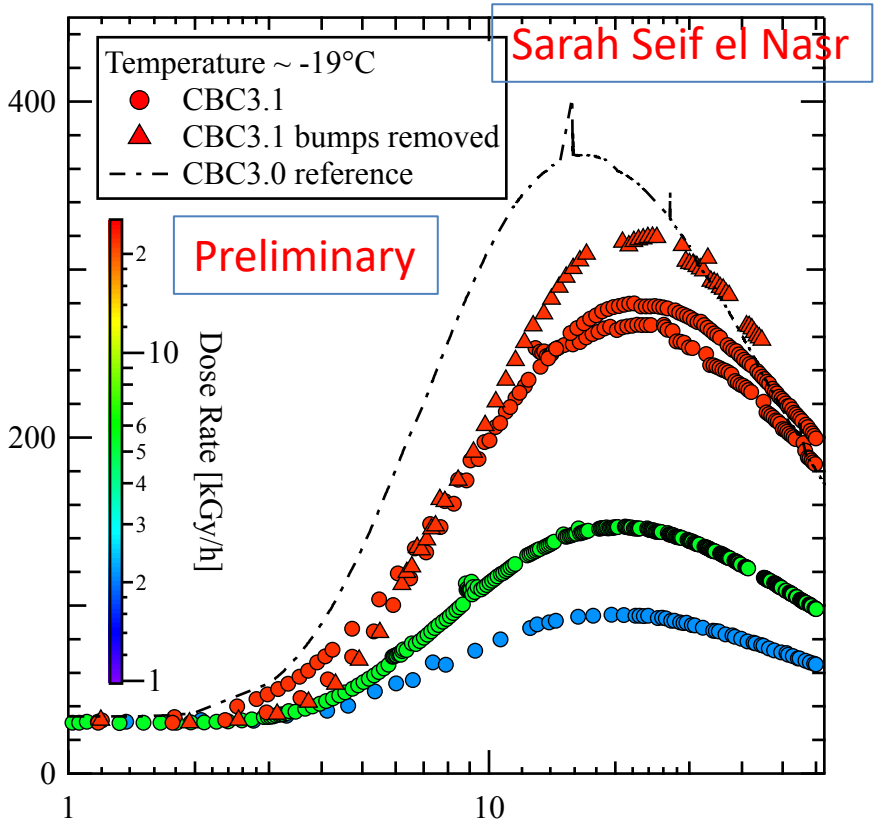




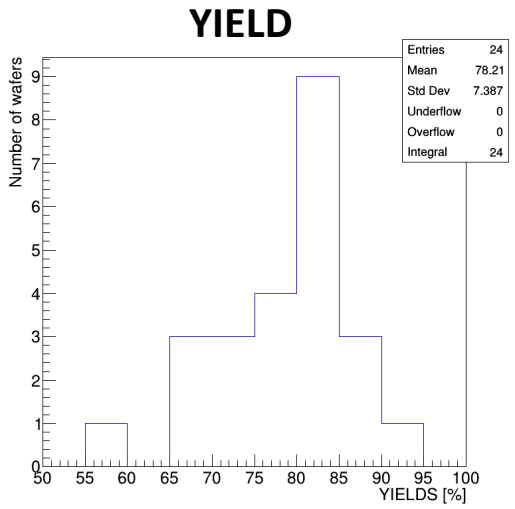
CBC3.1 TID tests

- X-ray irradiation ongoing in CERN - to confirm previous results
  - NB data await full analysis
    - Including detailed comparison of conditions, e.g. T, bump-bond presence,..
  - Modelling needed to extrapolate to LHC dose rate and T, with annealing
    - Much smaller effect than visible here

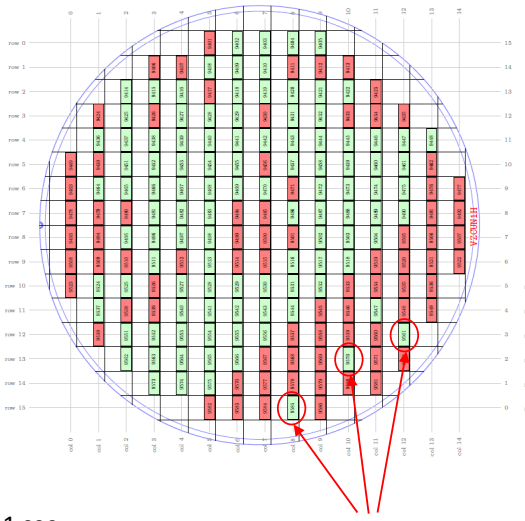




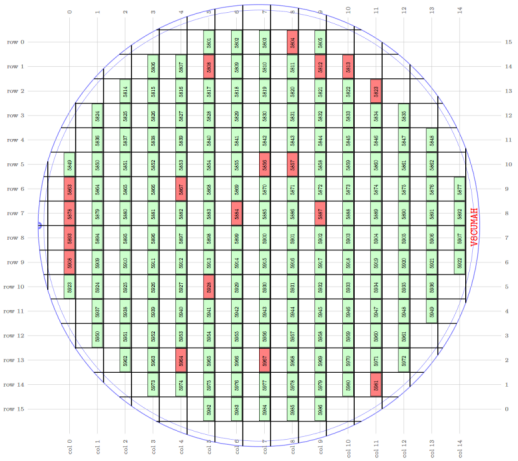
CBC3.0 wafer probing



VZCUN1H
Worst yield 58%



V8CUMAH
Best yield 90%



Some offsets are bad (most channels are working).

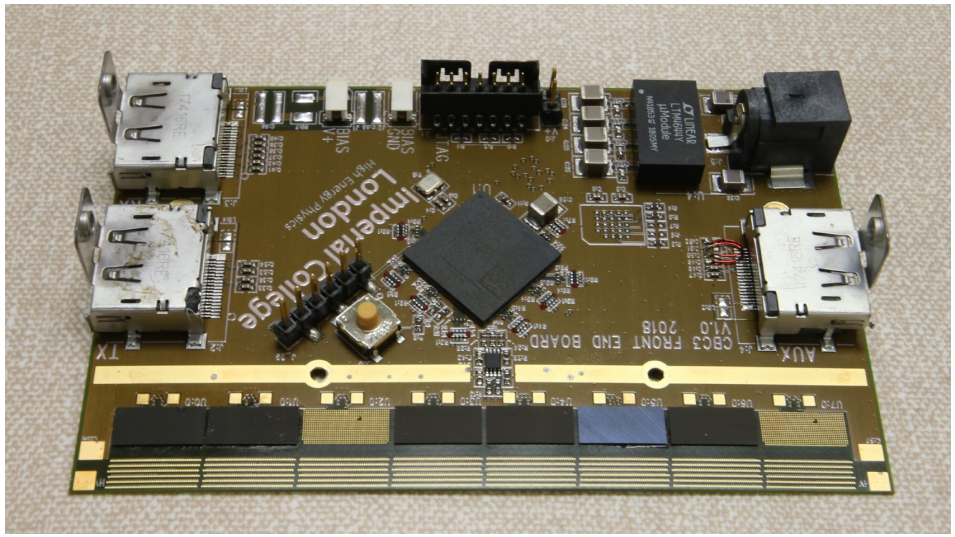
Breakdown for the tests which take more than 1 sec

Test	Time [sec]
S-curve check for pedestal and test pulse, gain check	7
Measurements of all individual AMUX parameters	6
Sweeping settings and measure the bias voltages	5
Offsets and pedestal tunings	3
Stub checks	2
Sweeping settings and measure the bias currents	2
Bandgap tuning, bandgap and chip ID register fuse blowing	2
Sum of above	27
Total time for a single chip wafer testing	30

186 CBC3.0 per wafer
(shared with SCA)

WP2 future

- Early tests on assembled hybrid bump-bonded at Imperial
  - Confirm inter-chip communication, which is less accessible on prober



  - SEU tests early 2019 – to confirm CBC3.0 results
  - 8CBC3 hybrids for 2S-modules in manufacture by CERN

– Planning orders of 24 wafer lots: check yield & confirm production readiness

– CIC1 (Lyon/CERN) expected late November

  - Diced and assembled on carriers for tests in December

WP3-WP5: common hardware

- Activities now ramping up considerably
  - Planning for integration of hardware
  - Genuine collaborative activities under way
    - Including firmware and software
  - Spreading hardware developments, based on common platform

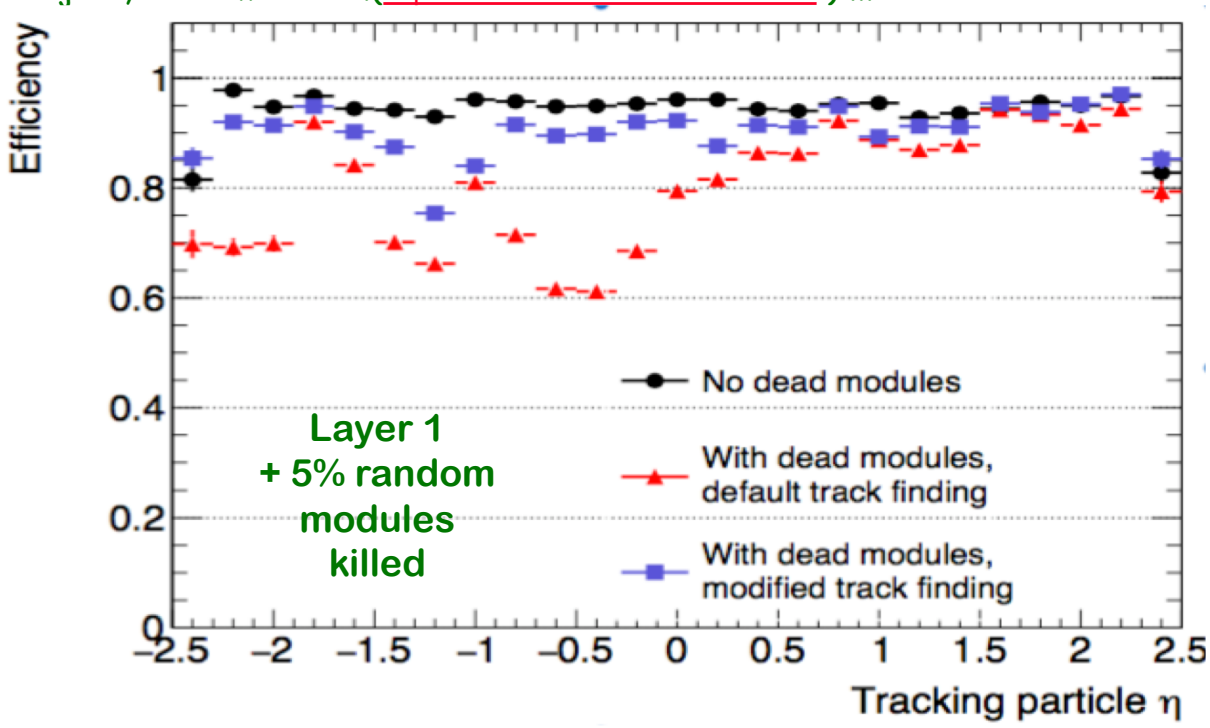
  - Some snapshots of work in progress

L1 track-finder stress test

- Simulated system (well) beyond actual operational expectations

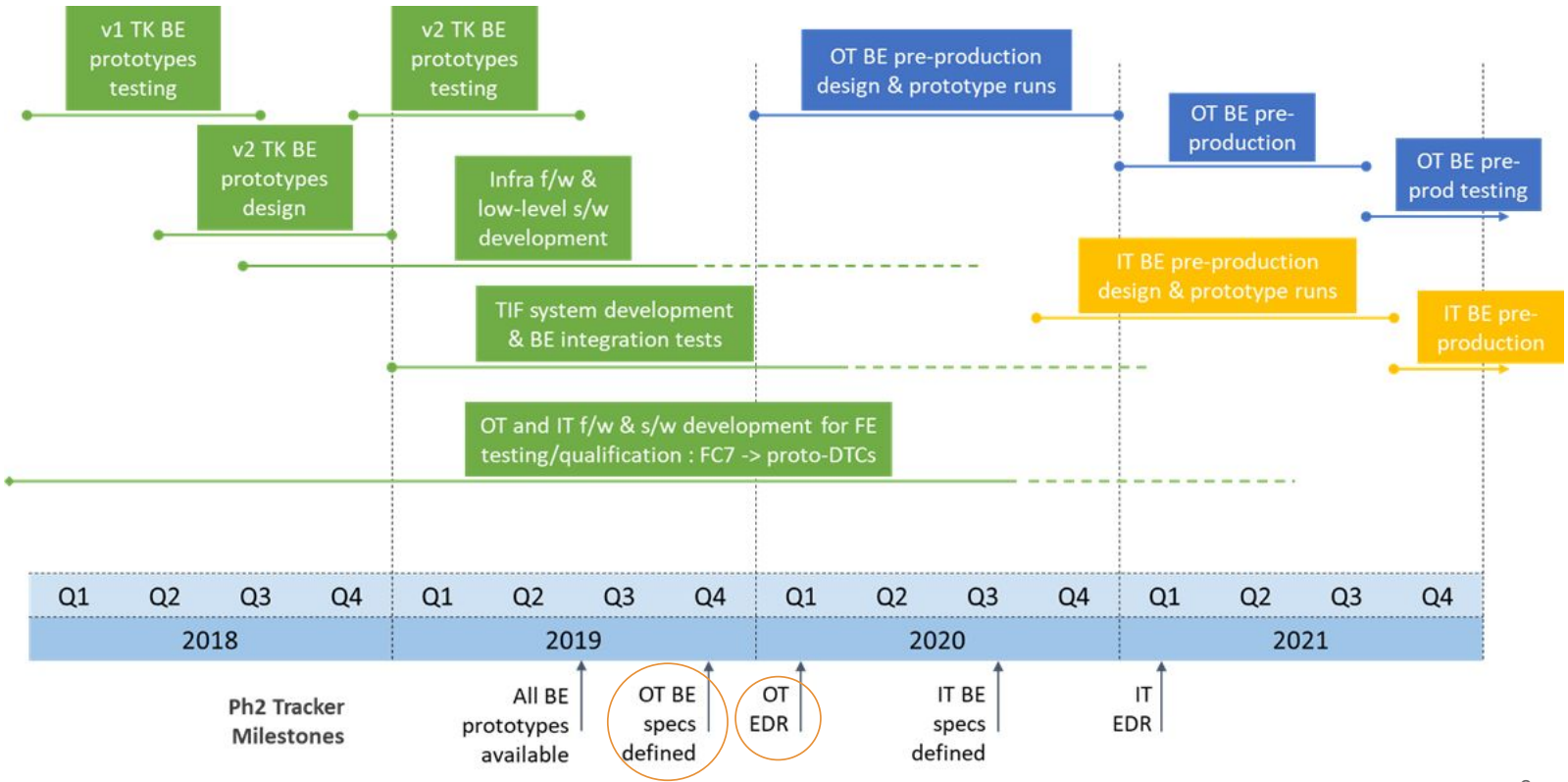
Stress Test – finished!

- e.g. Successfully demonstrated FPGA solution can cope with 300PU, high Pt jets, dead modules .(https://indico.cern.ch/event/704625/) …



WP3-WP5: common hardware

- e.g. schedule for next stages of Tracker BE development
  - Need real hardware (& firmware/software) to make progress



3

Common hardware

- From CMS workshop June 2018

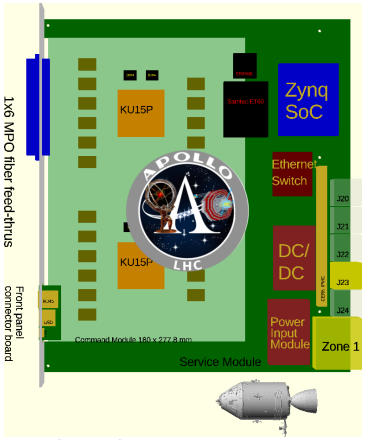
R&D Efforts

Two principal development platforms to:

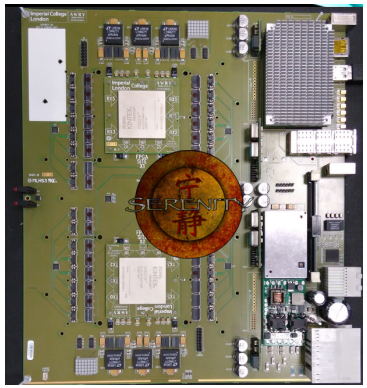
- Carry forward R&D and develop prototypes for system specification
- Support demonstrations / integration tests as required
- Explore different mechanical / configuration options

We expect these R&D efforts to evolve into the 3 tracker back-end deliverables

- Hardware may not be identical but they share many common features and will be supported by similar/identical common firmware/software frameworks



APOLLO



SERENITY

No prizes for guessing which hardware actually exists and is operational

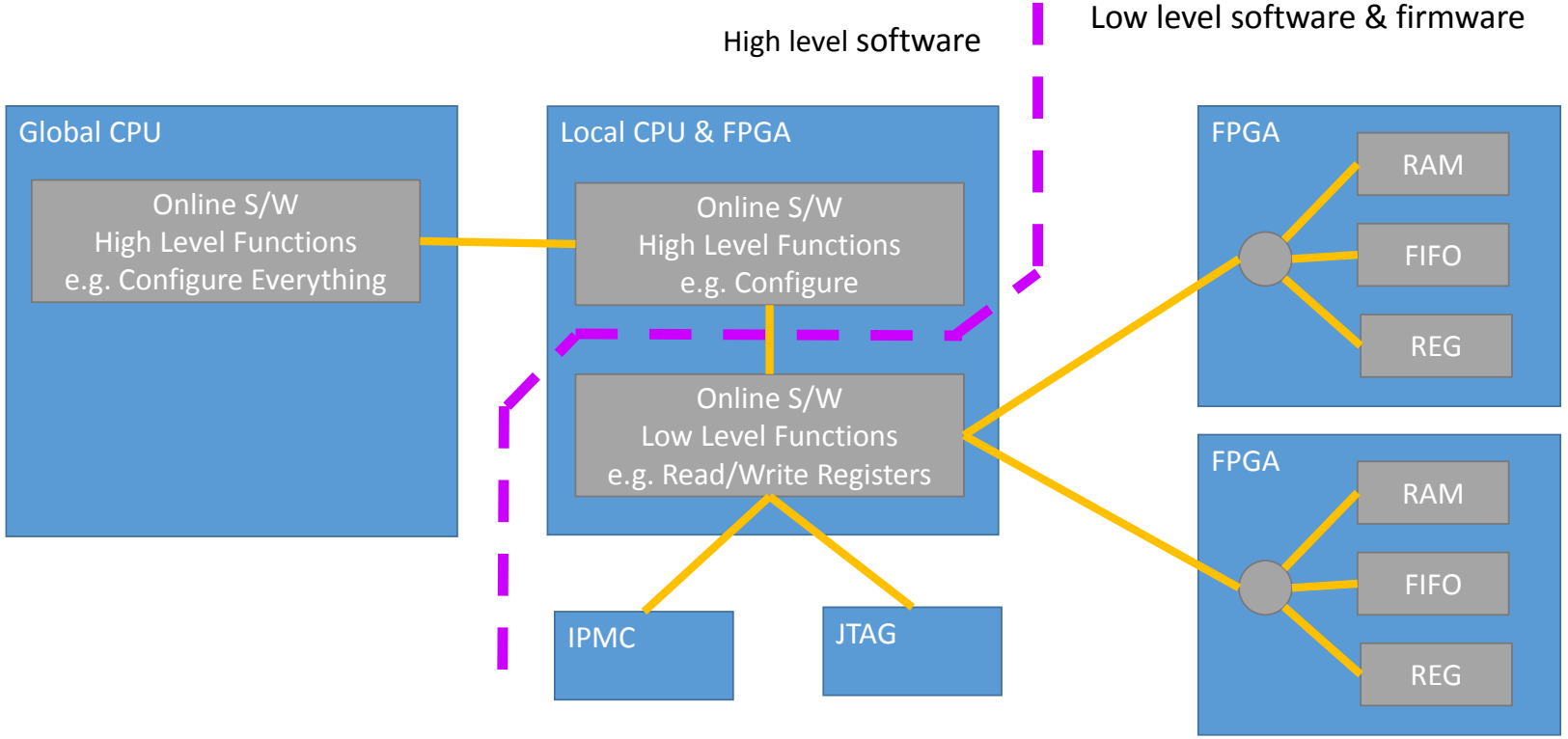
Firmware development

- Work on algorithms and infrastructure is needed
  - NB example of strong overlap between projects, benefiting from commonality

G Iles November Tracker workshop

Where is infra firmware?

Infrastructure
Low level software & firmware



Algorithm development

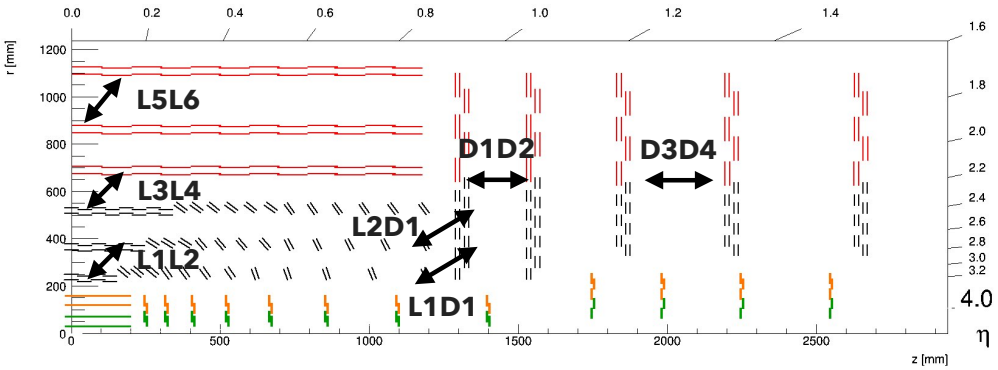
- Productive ideas still evolving

HYBRID ALGORITHM

2

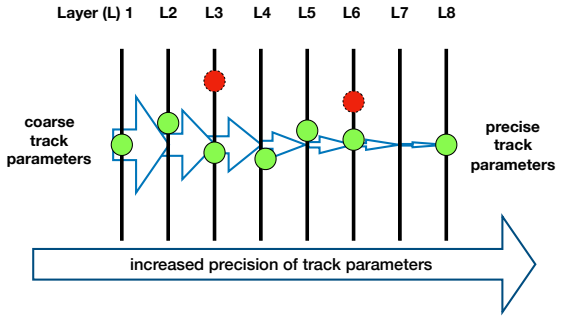
Combines the best of both approaches?

Tracklet seed & search



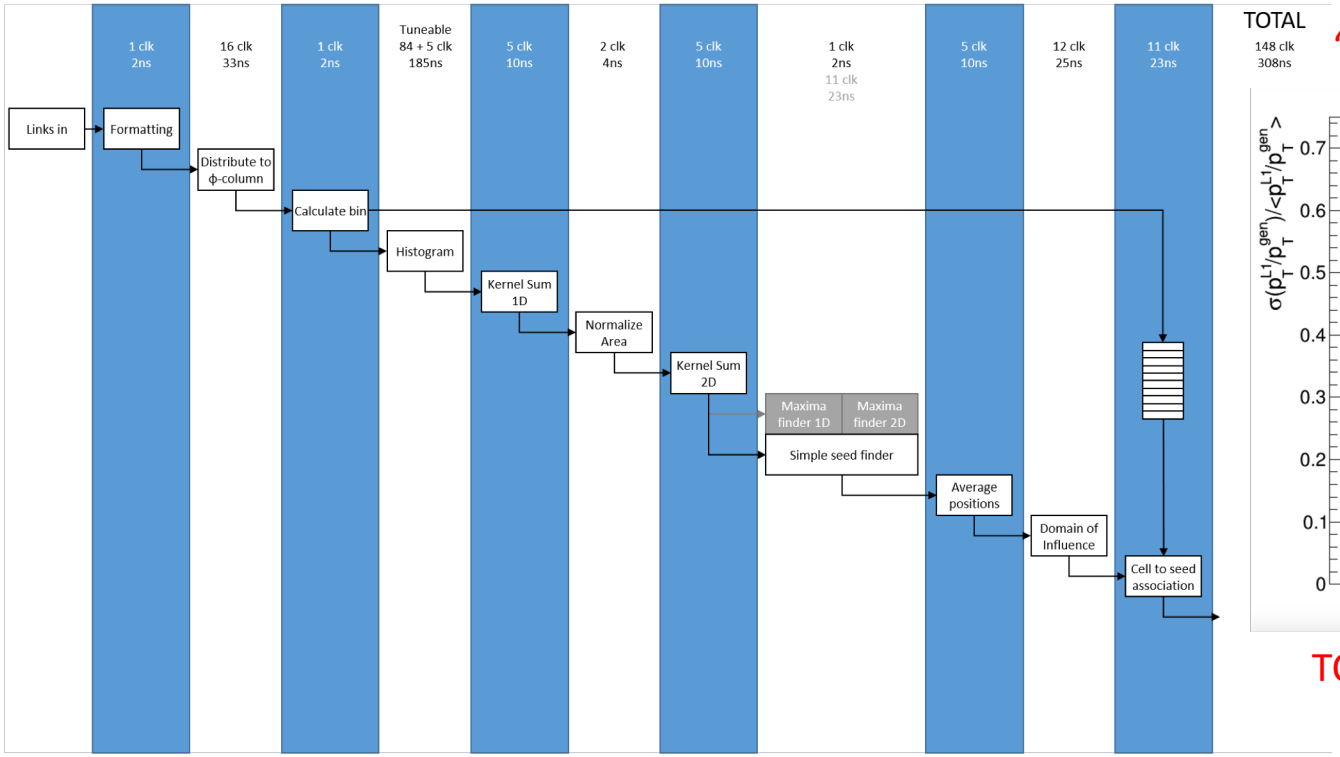
+

Kalman Filter

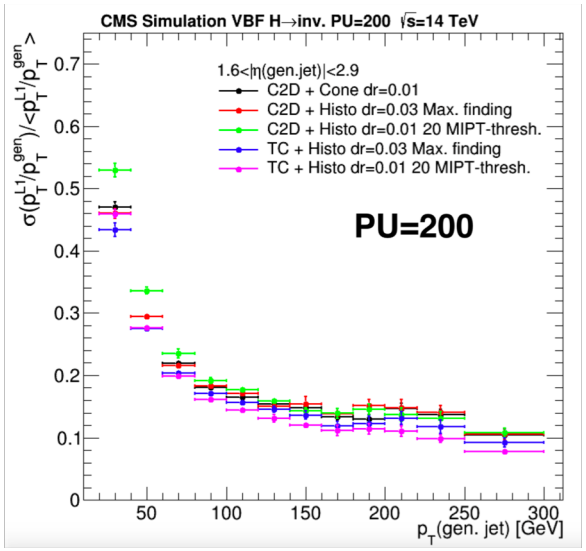


Algorithm development

- In HGCAL – “firmware-friendly” algorithms implemented
  - 3D clustering using raw data, gains in performance within available resources



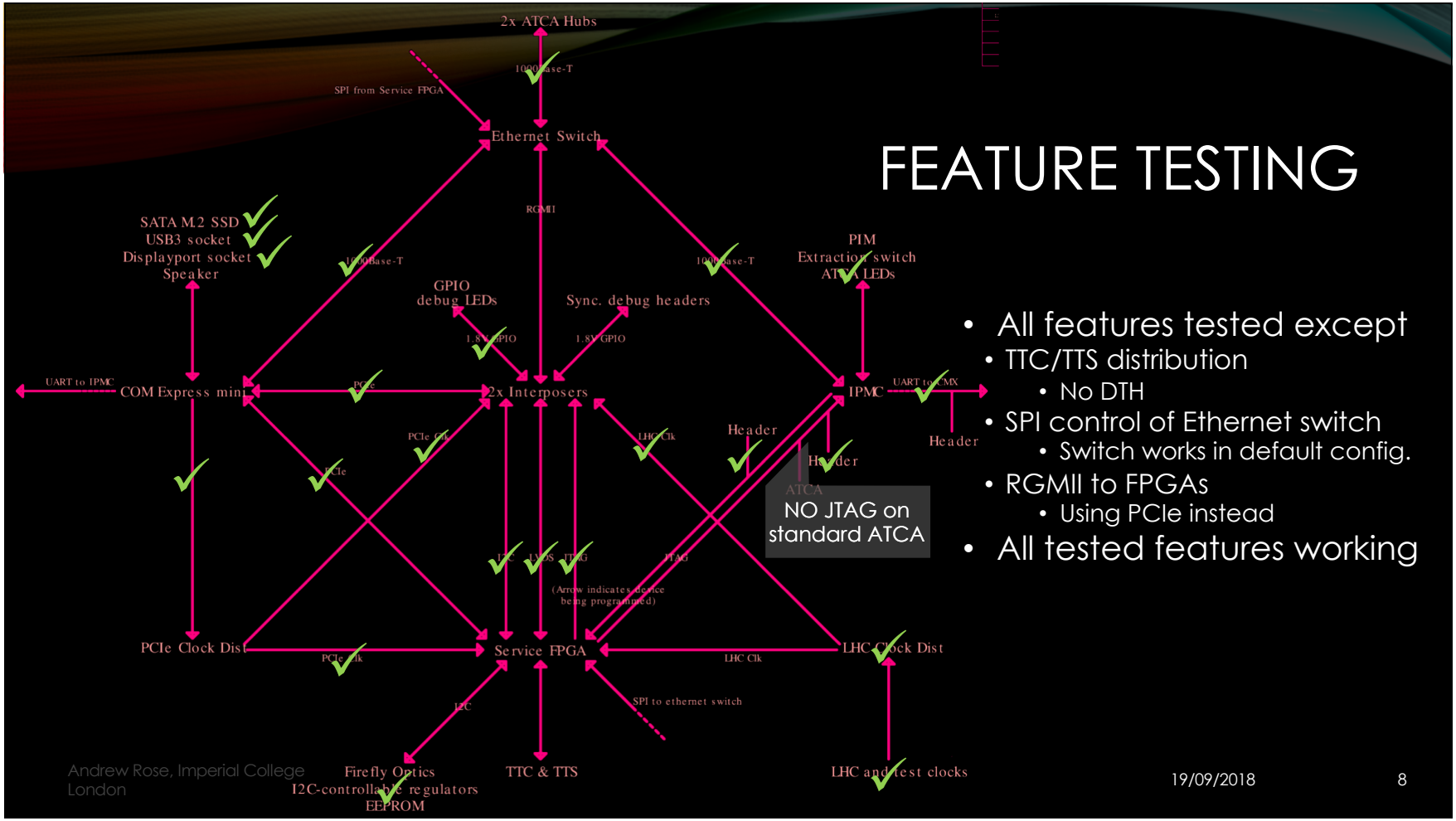
“Cone” vs “histo” algorithms



TC uses raw trigger cell data

Serenity 1.0 status

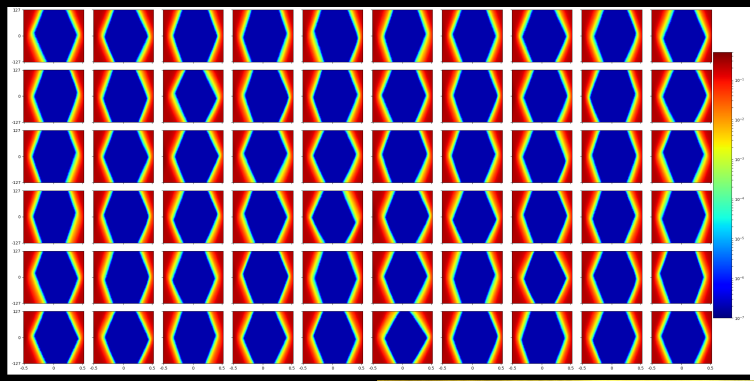
- September 2018



Serenity performance examples

COPPER LINKS – EYE DIAGRAMS

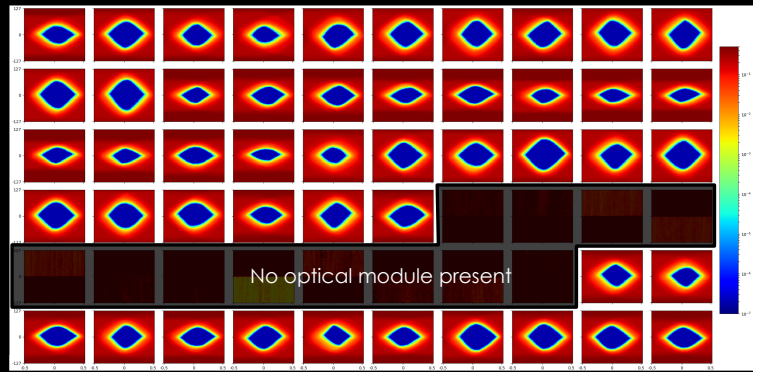
- Inter-interposer bus
- Two independent FPGAs
- 16Gbps, DFE disabled, No Pre- or Post-Cursor
- Each link passed 8e14 bits – No errors



Andrew Rose, Imperial College London

OPTICAL LINKS – EYE DIAGRAMS

- Firefly optics
- Two independent FPGAs
- 16Gbps, DFE disabled, No Pre- or Post-Cursor
- Default optical module settings
- 10m optical fibre
- Each link passed 8e14 bits – No errors



FPGA 1 → daughter-card → interposer → motherboard → firefly → MTP → 10M optical cable → MTP → firefly → motherboard → interposer → daughter-card → FPGA 2

Andrew Rose, Imperial College London

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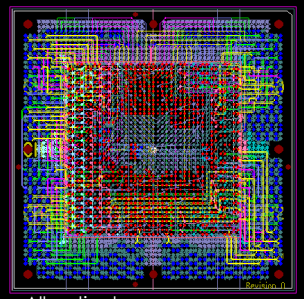
Common developments

- Note complementary contributions now appearing

CAN DIFFERENT GROUPS PRODUCE DAUGHTER-CARDS?

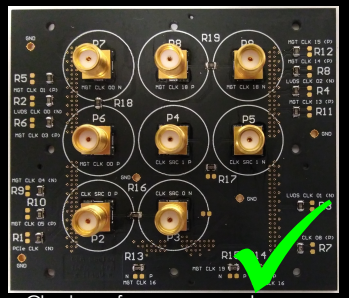
- IC - Xilinx KU115: Symmetric & Daisy Chained
- KIT - Xilinx KU15P
- TIFR - Xilinx VU9P
- Saclay – a clock-network analysis daughter card



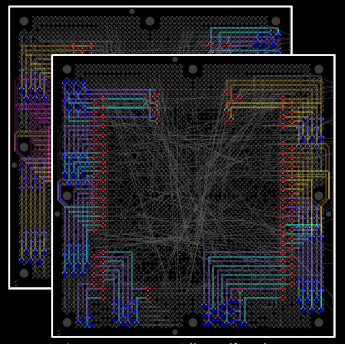
All optical
KU115, Imperial

Andrew Rose, Imperial College London

Mixed optical/electrical
KU15P, KIT

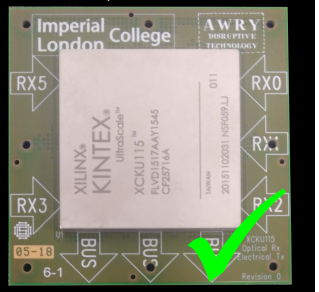


Clock-performance analyzer
CEA Saclay



In progress, All optical
VU9P, TIFR

Daisy-chain, optical in
KU115, Imperial



Daisy-chain, optical out
KU115, Imperial

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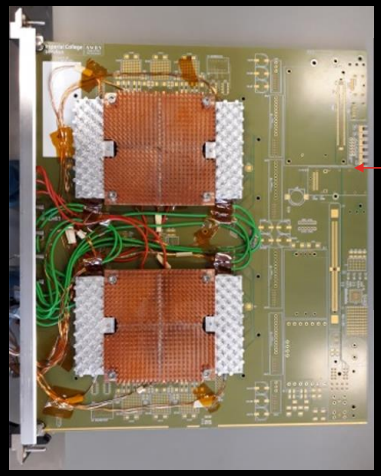
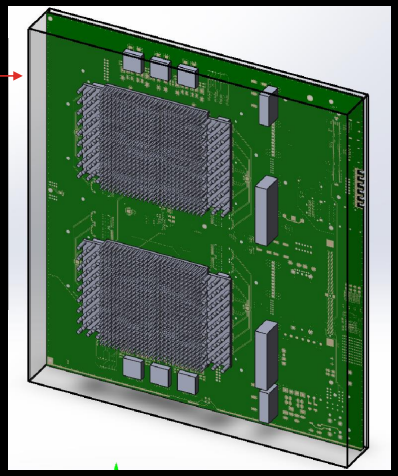
Other shared work

- Investigations of thermal behavior and cooling issues



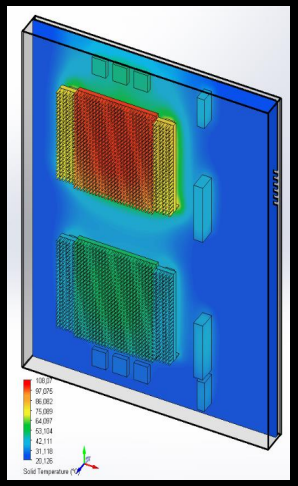
- Thermal simulations at KIT
- Physical thermal studies at CERN by INFN Pisa
- Mechanical component design, studies into stress on FPGA solder balls and stress on PCBs under way at IC

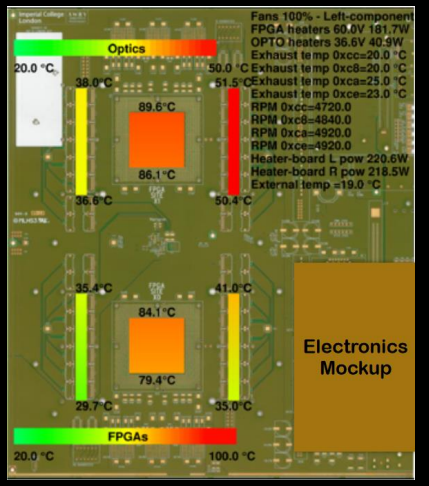


Andy Rose, Imperial College London

THERMAL TEST RESULTS

- Off-the-shelf heatsink
  - Dual Site
  - 100W + 90W
- Optimised - Dual Site
  - 120W + 100W
- Optimised Single Site
  - 120W - 200W





Andy Rose, Imperial College London

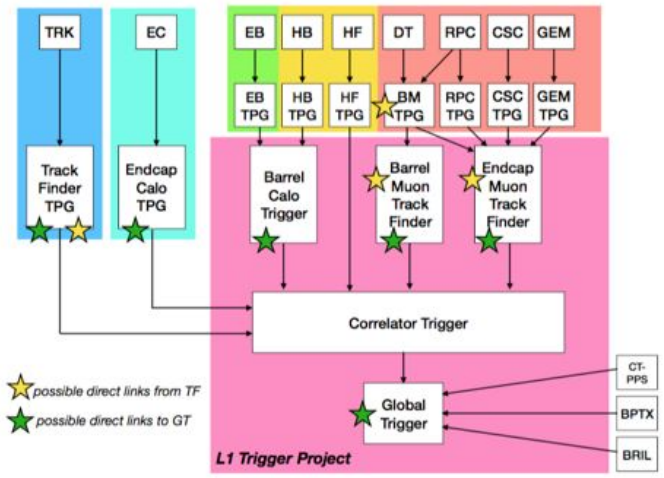
L1 trigger

- Plenty of places for Serenity applications

A Zabi LLR
November Tracker workshop

Level-1 Phase II Trigger Project: The System

→ ***Achieving the best possible physics selectivity from the upgraded CMS detector*** → *Organisation of the dataflow and overall infrastructure of the trigger revisited to benefit from the sub-detector upgrades*



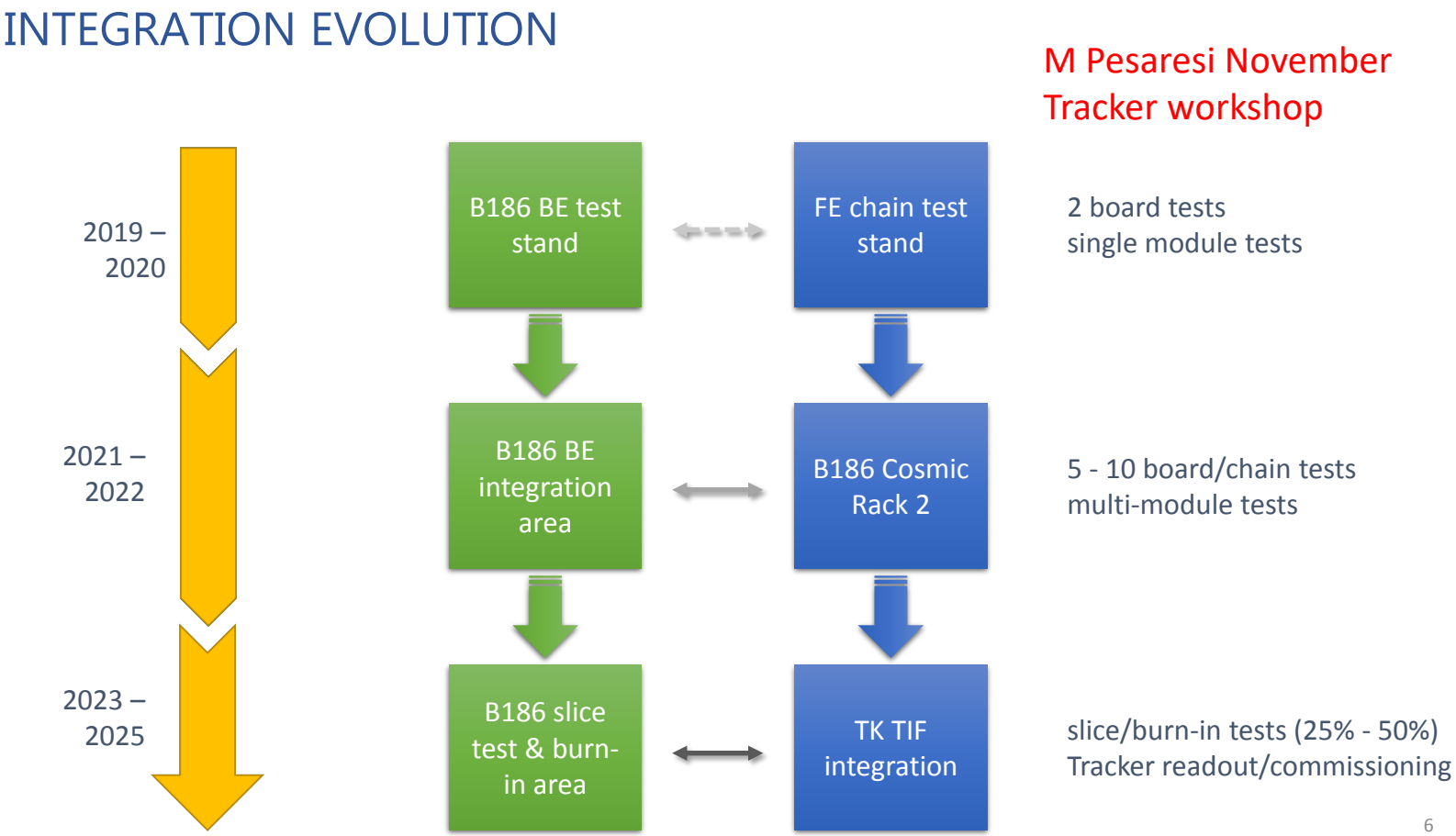
Improved triggering with full detector view:
Trigger decision includes calorimeters, muons & tracker (~5us latency)
→ L1Rate 750 kHz & 12.5 us latency
→ Sophisticated clustering algorithms deployed in the detector back-end electronics.
→ Building trigger objects @ Correlator level. Bringing HLT @ Level-1 (including higher-level objects: PF)
→ Bandwidth: Phase II ~ 50 Tb/s (1.8 Tb/s in Phase I)
Offline capabilities = Increased selectivity achieved

From Phase I experience: flexible architecture to adapt to LHC conditions & physics program, large computing power (FPGA) for highest bkg rejection and global detector view (high-speed links) to mitigate pile-up, calculate global quantities etc.

3

Further common work

- Integration activities centred in CERN



Transition to construction project

- CBC development is complete (subject to final tests)
  - Later than originally planned, as explained, for reasons outside our control
  - Production orders in 2020?
    - Automated wafer probing, data analysis, storage etc are close to final
- Serenity family & common hardware paradigm are progressing well
  - Next steps are on track for applications
  - Final hardware and algorithms - and infrastructure - can evolve as required
- In general, some delays are already evident
  - Eg component availability, manufacturing delays, integration, problems,…
    - However UK deliverables started in good time and have made excellent progress
  - Handover to construction activities should be straightforward
- Nevertheless, delays have had consequences
  - Cautious spending, especially on ASIC submissions, to avoid excess risk
    - Hence it is desirable to allow extra time for final purchases and invoicing

Finances

- Details in financial table and report
  - Recall WA was integrated into Imperial grant (strictly capital)
    - Request to allocate additional funds to TD & travel (& return underspend from IC)
    - Some local infrastructure expenditure to support CBC & Serenity, which was held back to avoid risk, is desirable
    - Hence remaining WA should evolve to zero, with no-cost extension

Item	**£k**	
CERN commitments in pipeline	118.8	Not yet invoiced
Commitments at Imperial	85.7	Awaiting deliveries and invoices
3x24 CBC3.1	148.1	estimate @ $2675 per wafer
Serenity further evaluation studies	62.0	optical components, FPGAs, PCBs
"Overspend" on consumables	15.0	Some capital items mis-classified
subtotal	**429.6**	
Overspend on RAL TD effort	100.0	Agreed at past OSC
Overspend on travel	40.0	Agreed at past OSC
Additional RAL TD effort	20.0	
Additional travel FY 2018	44.0	
Total	**633.6**	
Remaining Working allowance	**54.6**	
Original Working allowance	386.6	For comparison

Summary

- The project deliverables evolved since the original proposal in 2007, but actually in a way which brought them closer to the original objectives, e.g.
  - shared FPGA hardware, to focus on applications
  - FPGA applications for tracker DAQ and trigger processing
- The early track-trigger ideas proposed to use only a few tracker points
  - Simulation studies demonstrated this would be insufficient to contain rate
  - The track-finder needed to use many tracker layers
- Thus full track reconstruction in real time with low latency was essential
  - in a hugely demanding environment – but now proven by us
- The L1 calorimeter trigger upgrade was a vital step for CMS and the technology
  - Time-multiplexing is now an accepted model, and widely deployed
- The UK can take credit for many crucial elements of the Phase II upgrade
  - The CBC has evolved to deliver Outer Tracker data for track-trigger primitives
  - Our FPGA processing boards meet the requirements for multiple applications
  - Both of these provide the only existence proofs so far of fundamental elements of the new CMS tracker, HGCAL trigger and L1 trigger
  - The STFC investment in R&D we proposed has been timely and successful

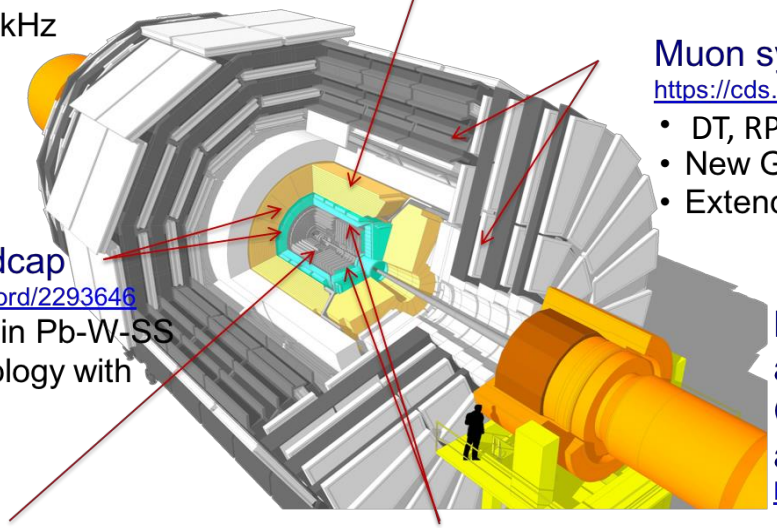
Further information

This will be a beautiful & powerful detector

L1-Trigger/HLT/DAQ
https://cds.cern.ch/record/2283192
https://cds.cern.ch/record/2283193
- Tracks in L1-Trigger at 40 MHz for 750 kHz PFlow-like selection rate
- HLT output 7.5 kHz

Barrel Calorimeters
https://cds.cern.ch/record/2283187
- ECAL crystal granularity readout at 40 MHz with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards

Muon systems
https://cds.cern.ch/record/2283189
- DT, RPC, CSC new electronics
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \simeq 3$



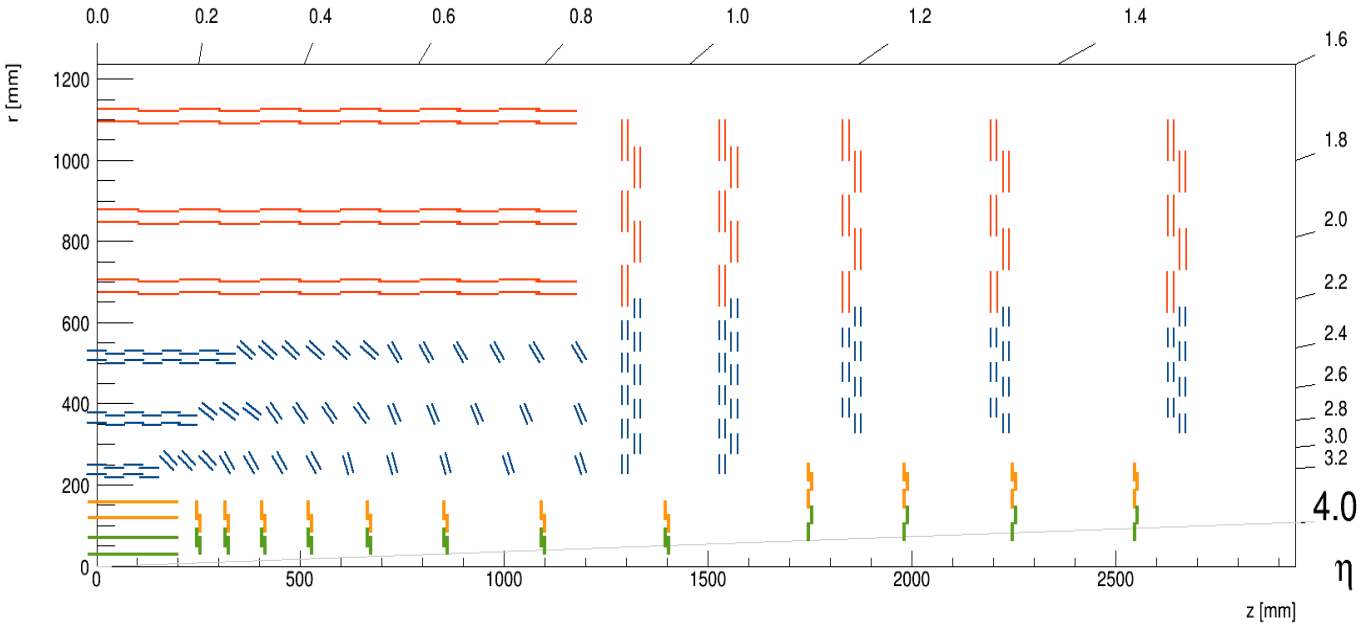
Calorimeter Endcap
https://cds.cern.ch/record/2293646
- Si, Scint+SiPM in Pb-W-SS
- 3D shower topology with precise timing

Beam Radiation Instr. and Luminosity, and Common Systems and Infrastructure
https://cds.cern.ch/record/2020886

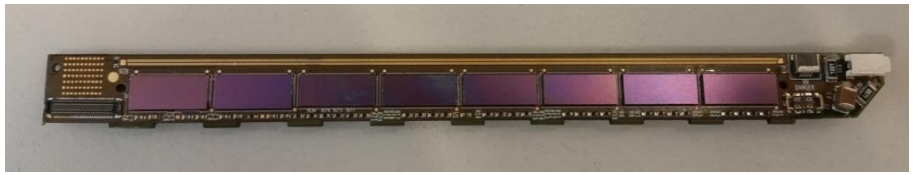
Tracker https://cds.cern.ch/record/2272264
- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \simeq 3.8$

MIP Timing Detector
https://cds.cern.ch/record/2296612
- $\simeq$ 30 ps resolution
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

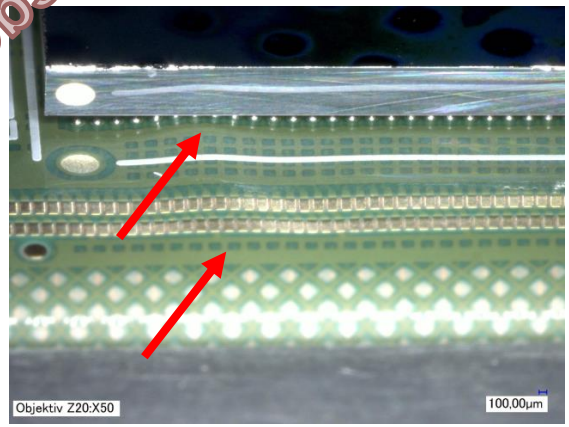
TDR Layout



- Tracking performance studied with CMSSW full simulation
- Complemented with b-tagging and some physics channels



Observations



Recent 2S and PS hybrids suffer from warpage and/or bow during assembly process:

- Waves on flex, compromises bump bonding.
- Compromises also wire bonding.
- Process needs to be improved.

Affected hybrids

- PS-MCK: all variants.
- 8CBC2Flex: recent variants.

All contractors concerned