Analogue to Digital Conversion

•Turns electrical input (voltage/current) into numeric value

•Parameters and requirements

Resolution

the granularity of the digital values

Integral Non-Linearity

proportionality of output to input

Differential Non-Linearity

uniformity of digitisation increments

Conversion time

how much time to convert signal to digital value

Count-rate performance

how quickly a new conversion can begin ofter a previous event

Stability

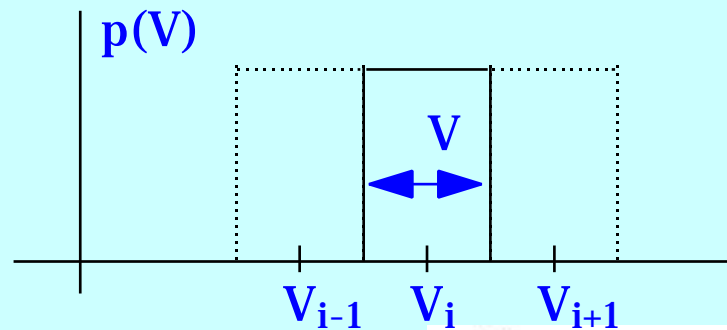how much values change with time

Resolution

- To convert an analogue value, eg voltage, to digital two parameters are required
  <u>range</u> and <u>number of bits</u>

  quantum = $V = (V_{max} - V_{min}) * 2^{-N}$ referred to as 1LSB (least significant bit)

- eg 10 bits = 2^{10} = 1024, $V_{max} - V_{min}$ = 1V   =>   V = 1V/1024   1mV

- Ideal ADC behaviour

  probability vs amplitude
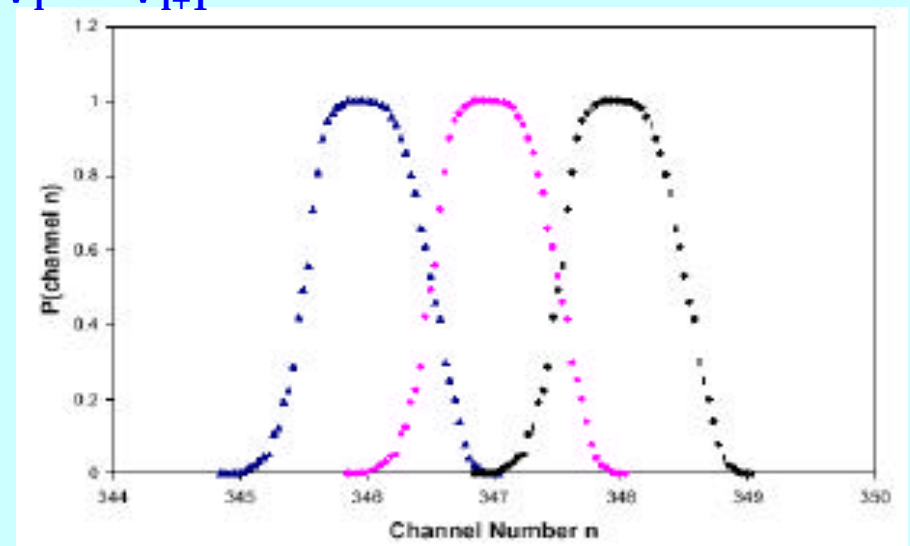
$p(V)$

V

V_{i-1} V_i V_{i+1}

- Real ADC behaviour

  noise in digitisation process

  smears resolution

  $_{noise} <$ V/4

Speed vs resolution

• from Analog Devices ADC selection guide

bits per sec (or samples per sec)

Throughput rate (bps)						
Resolution (bits)	<10k	10-100k	100k-1M	1-10M	10-100M	>100M
17	|	-------	-------	-------	-------	-------
14-16	|	|	|	|	|	-------
12-13	-------	|	|	|	|	|
10-11	-------	|	|	|	|	|
8-9	-------	-------	|	|	|	|
8	-------	-------	-------	-------	|	-------

Maximum speed 200Mbps 12 bits 1.3W single channel

210Mbps 10bits 2.4W single channel

Maximum resolution 24 bits 6.4kbps

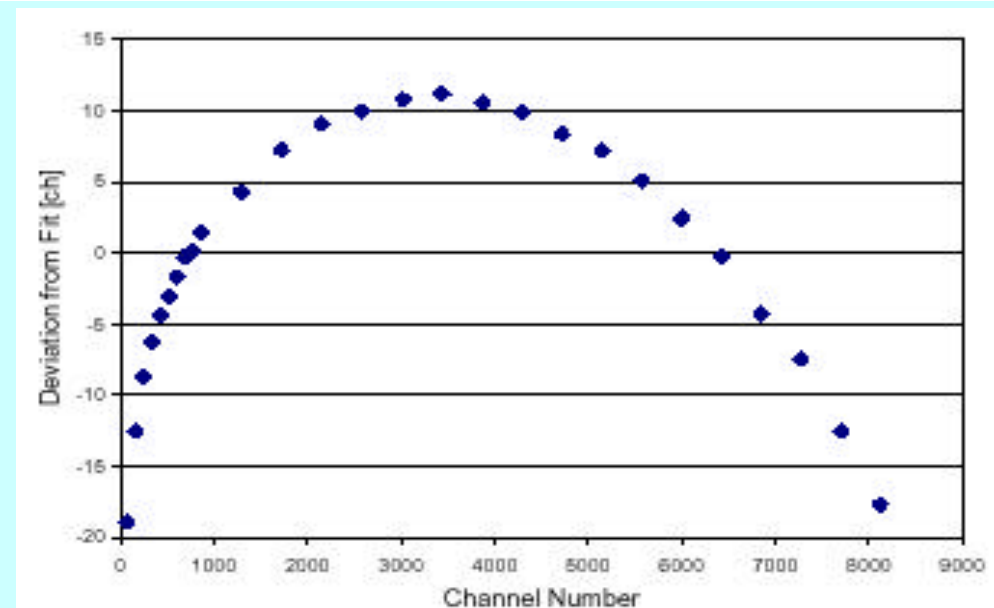• What determines this relationship?
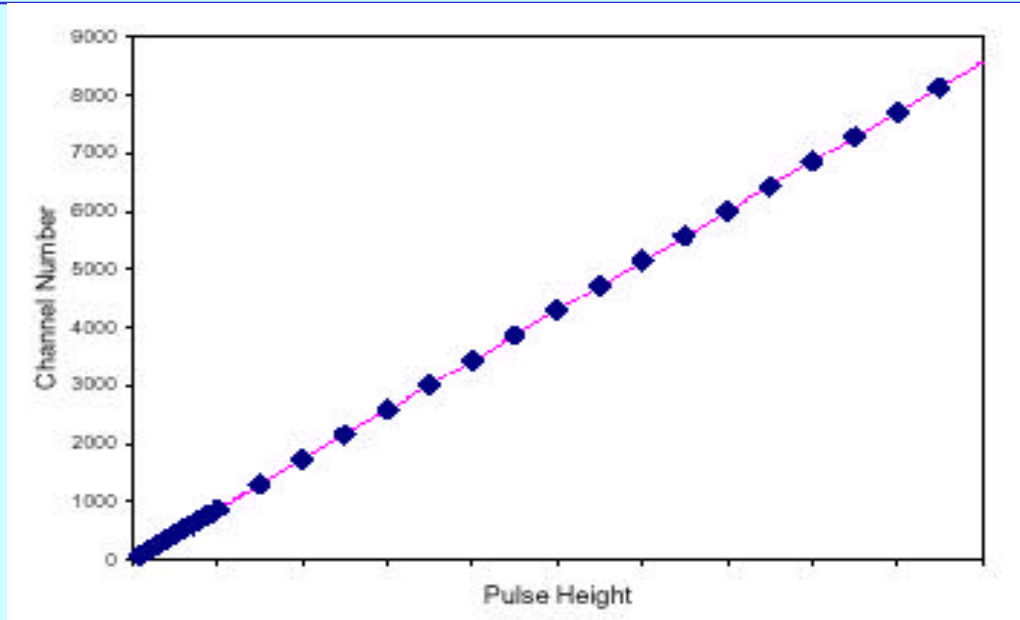
Integral non-linearity

- Output value D should be linearly proportional to V
  - check with plot
  - for more precise evaluation of INL
  - fit to line and plot deviations
  - plot $D_i - D_{fit}$ vs n_{chan}

Differential non-linearity

- measures non-uniformity in channel profiles over range
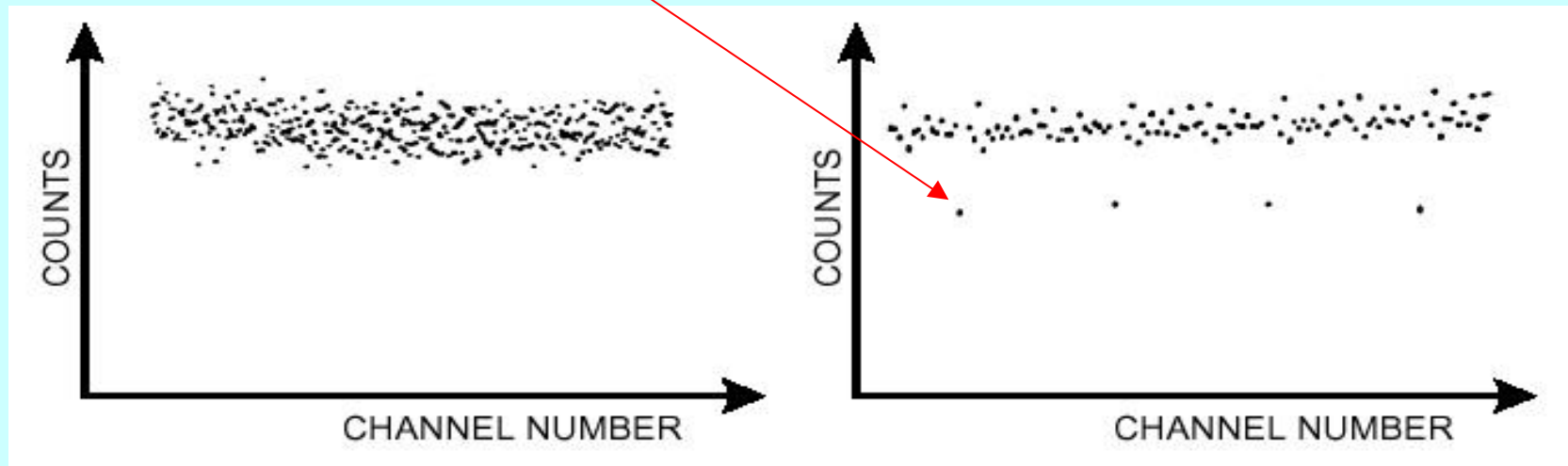
  DNL = $V_i / \langle V \rangle - 1$

  V_i = width of channel i

  $\langle V \rangle$ = average width

- rms or worst case values may be quoted

  DNL ~ 1% typical but 10^{-3} can be achieved

  can show up systematic effects, as well as random

Other variables

- Conversion time

  finite time is required for conversion and storage of values

  may depend on signal amplitude

  gives rise to dead time in system

  ie system cannot handle another event during dead time

  may need accounting for, or risk bias in results

- Rate effects

  results may depend on rate of arrival of signals

  typically lead to spectral broadening

- Stability

  temperature effects are a typical cause of variations

- A partial solution to most of these problems is regular calibration, preferably under real operating conditions, as well as control of variables

Parallel (Flash) ADC

- Input value is compared simultaneously...
- against a set of comparators

  2^N comparators required for N bits

  Threshold values defined by

  resistor chain

  relative accuracy important,

  not absolute values

- Pros

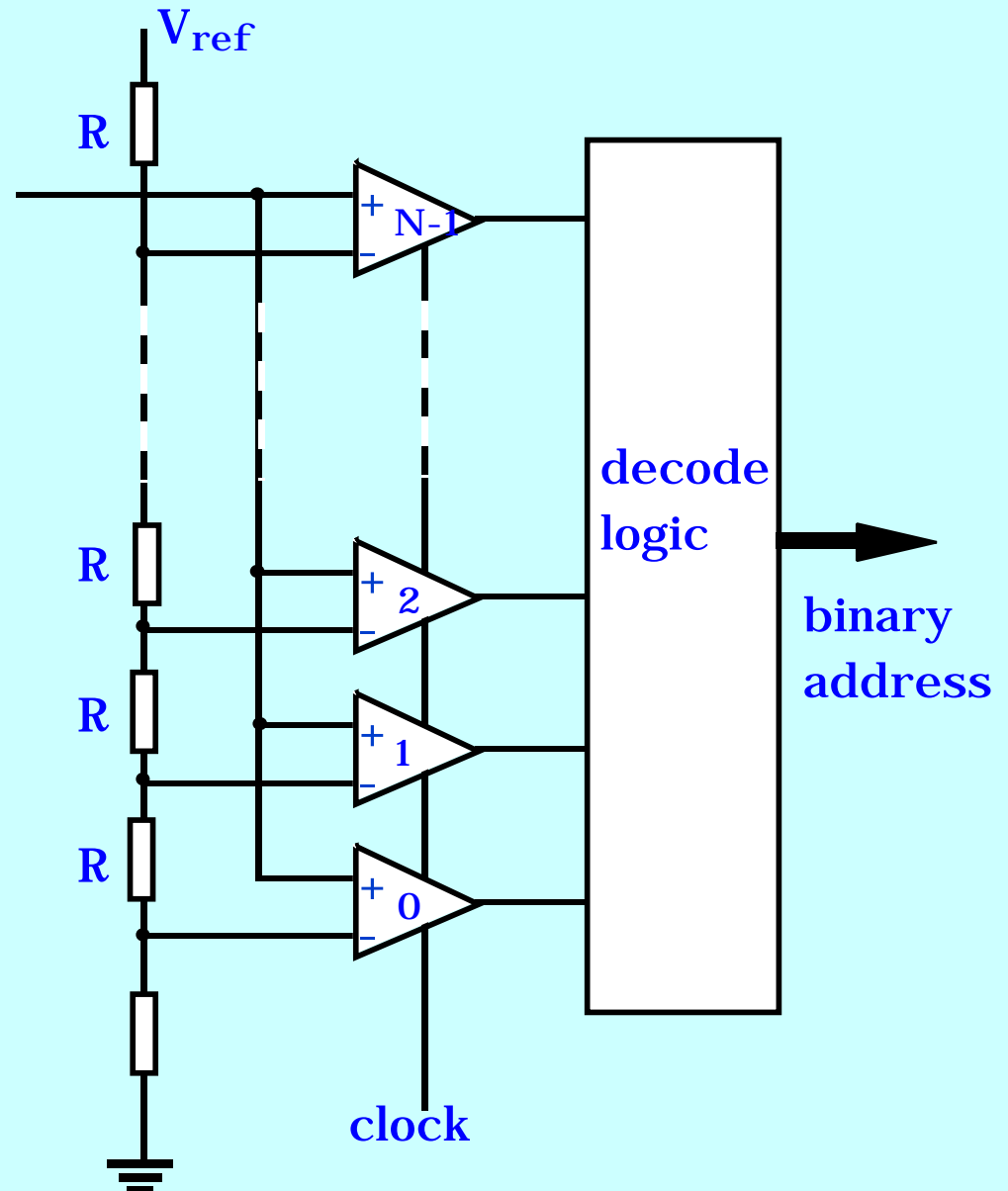 short conversion time
  eg 10bits @ 40MHz

- Cons

  limited resolution,
  size of IC grows with N

  DNL ~ 1%

  power consumption

Successive approximation ADC
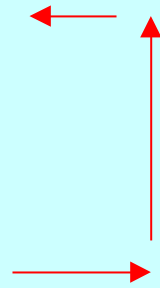
- **analogous to binary search**

  generate $V_{ref} = V \times (2^{N-1}, 2^{N-2}, \ldots 2^0)$ in N steps

  set bit = 1

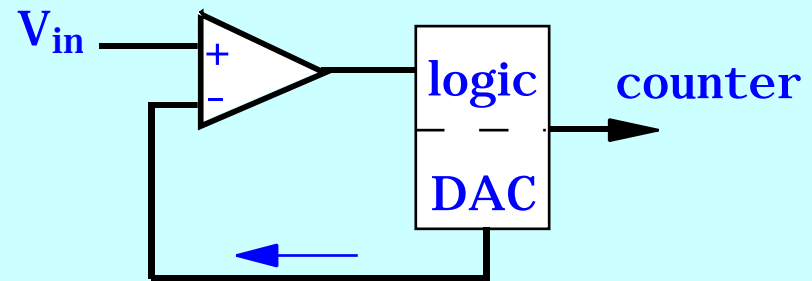 if $V_{in} > V_{ref}$

      leave

  else bit = 0

- **Pros**

  speed ~ µsec

  high resolution

- **Cons**

  DNL 10-20%

  very precise resistors required with DAC for V_{ref}

V_{in} +   logic   counter

     −   DAC

DAC = digital to analogue converter ie number -> voltage

Single slope (Wilkinson) ADC

- Single slope conversion

    input signal charges capacitor

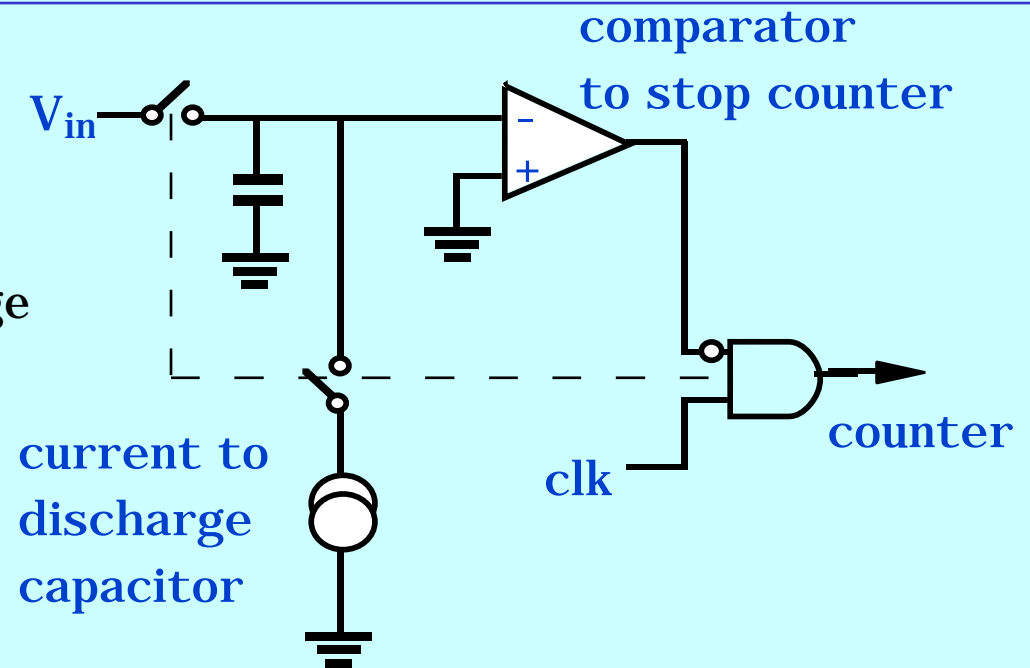   discharged by constant current

    counter (eg 200MHz) times discharge

- Pros

    Excellent DNL

- Cons

    modest absolute accuracy

    slow, and conversion time depends

    on amplitude

    $T_{conv} = nT$ eg T = 10ns, 13 bits $T_{conv} = 82\mu s$

comparator
to stop counter

V_{in}

current to
discharge
capacitor

clk

counter

- Dual slope conversion reduces systematic (absolute) errors

    charge C with constant current and then measure time for discharge

    charge and discharge subject to same comparator and capacitor variations

Sigma-delta ADC

- Digitise the signal with 1-bit resolution at a high sampling rate (MHz).

  useful for high resolution conversion of low-frequency signals, to 20bits

  low-distortion conversion of audio signals

   good linearity and high accuracy.

- Operation - At t = 0, assume $V_{ref} = 0$

  V_{out} high

  integrator charges -ve

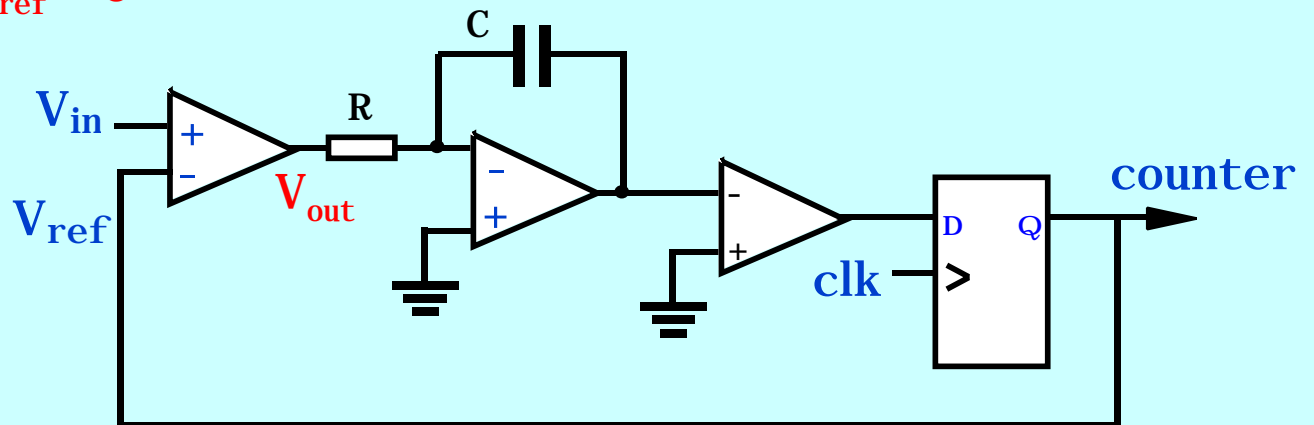   at rate ~ V_{in}

  comparator flips

  counter goes low

   clock increments... etc,...

  $V_{in} = 0$ => output = 000000...

  $V_{in} = (1/2)V_{in}(max)$ => output = 101010...

  $V_{in} = V_{in}(max)$ => output = 111111...

  the higher the input voltage, the more 1's at the serial digital output.

Non-linear A-D conversion

- Some high speed systems also need high resolution and dynamic range

  however do they need the same resolution at all amplitudes?

- Dynamic range - eg 15 bit

  is set by largest and smallest signals to be observed

- Resolution on energy

  determined by requirements, noise and physics

  eg statistics (counting or E resolution) => $/E)_{stat} = a/\ E$

  $_{noise}(E) = constant$ so $_{noise} = b$

  Resolution $/E)_{total} = a/\ E$

  $/E)_{total} = [a^2/E + b/E^2]^{1/2}$ **a** term eventually dominates

- thus build multi-gain system prior to ADC

  so smaller signals digitised with

  lower effective resolution

V_{in} — x1, x2 → select signal in range → to ADC
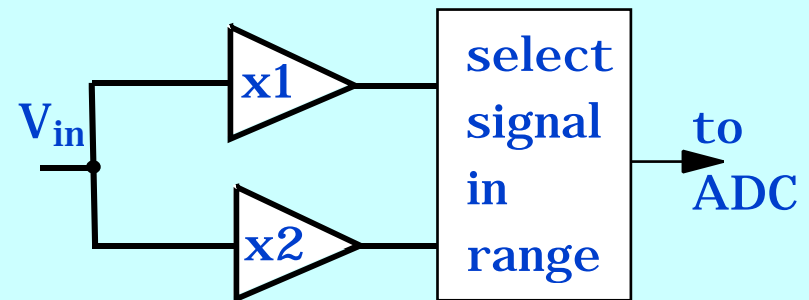
Example of non-linear ADC

- A integrating system for measuring x-ray photons for crystallography, measuring spots. The most intense spots contain up to $\sim10^9$ photons, the weakest just a few. Measure N in spot

  aim: achieve 1% resolution

  using a 10-bit ADC (cost)

  assume 1V range

  1V = largest signal, defines G_1

  $N < 10^4$ $(N)/N > 1\%$
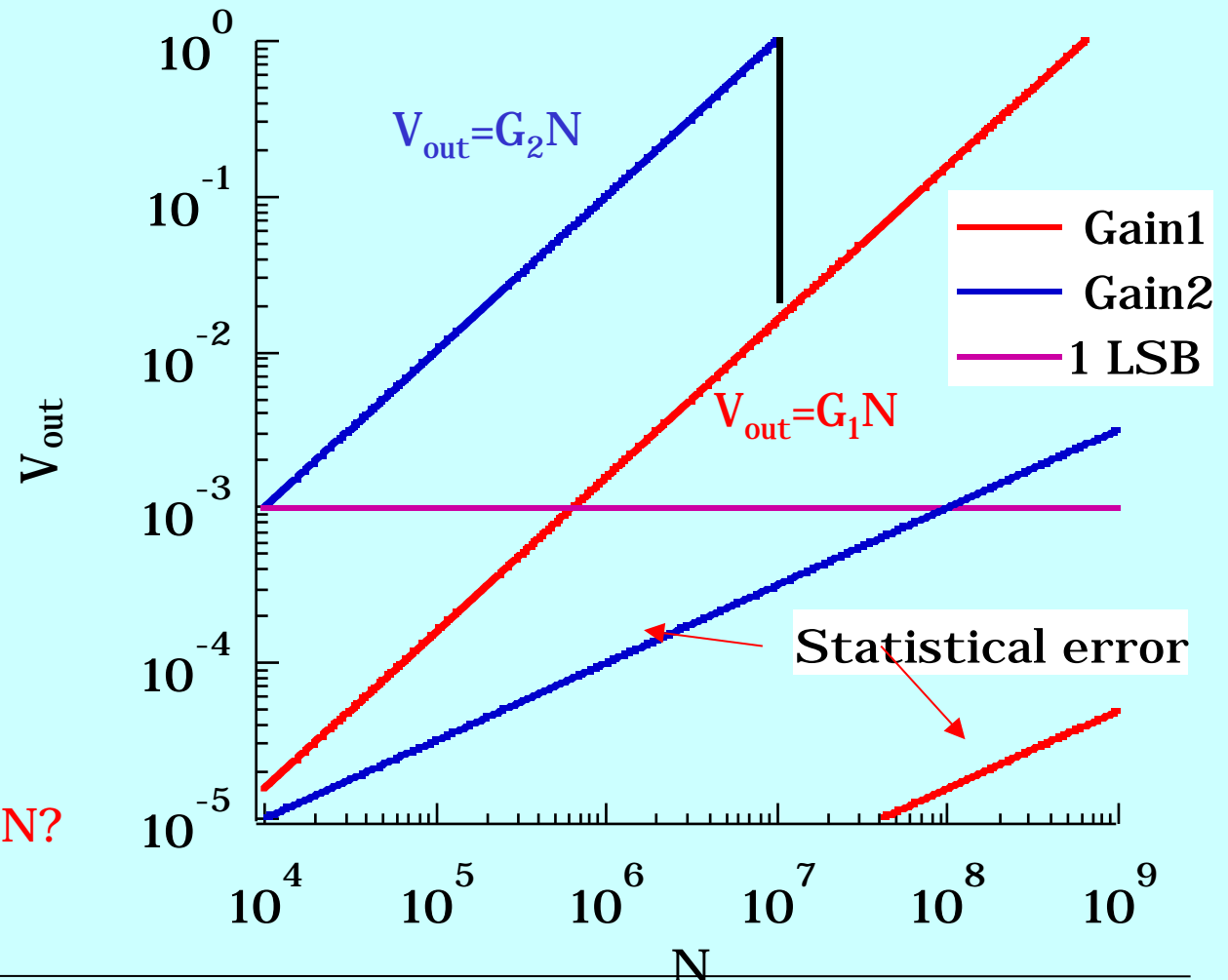
  defines smallest signals

  but ADC LSB > signal

  Increase small signal gain G_2

  Select output in ADC range

- Is 1% resolution achieved for all N?

  If not… ?

$V_{out}=G_2N$

$V_{out}=G_1N$

Gain1
Gain2
1 LSB

Statistical error

V_{out}

N

Time to Digital Conversion (TDCs)

- Count clock pulses between start and stop pulses

    up to ~1GHz, limited by technology so $\Delta t \approx 1ns$

    capable of digitising more than one hit in an acquisition
      provided logic is sufficient

- Analogue ramp

    for greater precision, $\Delta t \approx 10ps$

    charge capacitor with constant current source

    start pulse: turns on current

    stop pulse: turns off

    then measure V on storage capacitor using ADC
      can't accept more than one signal in digitising period

Digital to Analogue Conversion (DAC)

• Several techniques - generally similar (inverse) to ADC
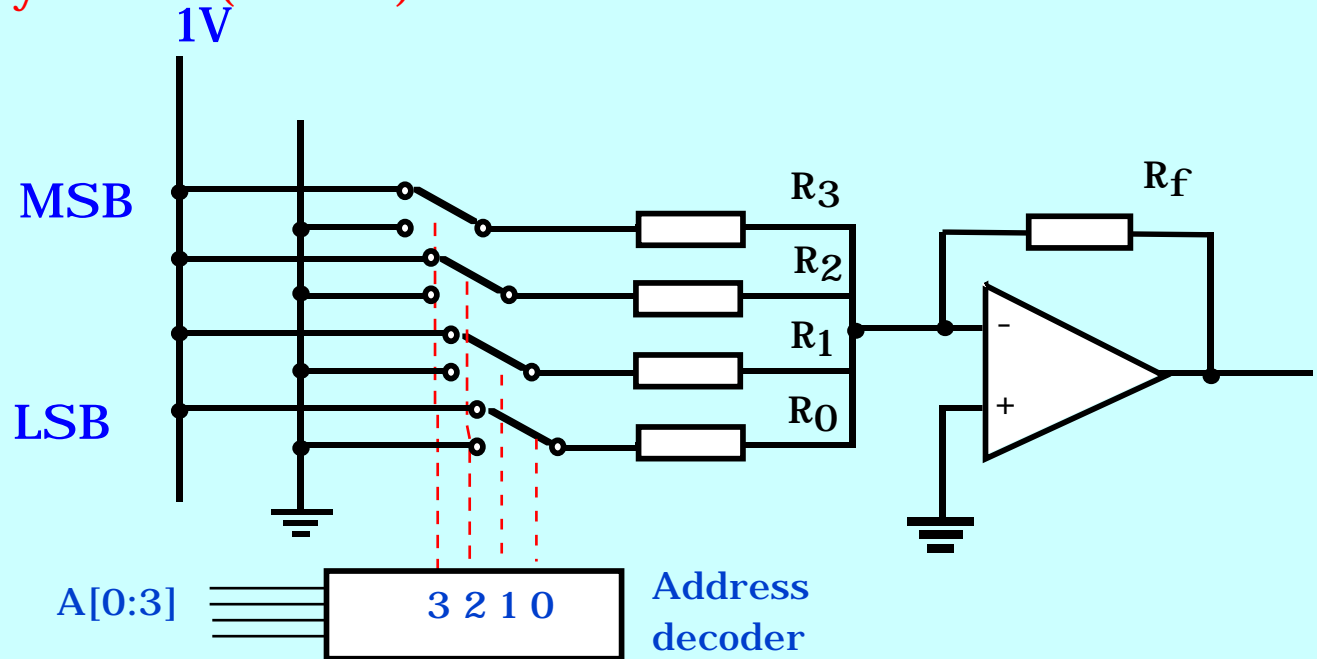
eg summing amplifier

$R_0 = 2*R_1$

$= 4*R_2$

$= 8*R_3$

but precision of smallest

resistor must be better

than LSB

$$MSB = \quad (V/R_3) < LSB = V/R_0$$

OK for a few bits but becomes difficult for N large

other techniques required... eg

R-2R converter

- relies on matching of resistor values

  consider point on resistor divider

  switch open or closed

  always see 2R in parallel with 2R

  = R to ground

  (start from right and work left)